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Surface Defect Passivation of Silicon Micropillars

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Reactive ion etching (RIE) used to fabricate high-aspect-ratio (HAR) nano/microstructures is known to damage semiconductor surfaces which enhances surface recombination and limits the conversion efficiency of nanostructured solar cells. Here, defect passivation of ultrathin Al_2O_3-coated Si micropillars (MPs) using different surface pretreatment steps is reported. Effects on interface state density are quantified by means of electrochemical impedance spectroscopy which is used to extract quantitative capacitance–voltage and conductance–voltage characteristics from HAR dielectric–semiconductor structures which would otherwise suffer from high gate leakage currents if tested using solid-state metal–insulator–semiconductor structures. High-temperature thermal oxidation to form a sacrificial oxide on RIE-fabricated Si MPs, followed by atomic layer deposition of 4 nm thick Al_2O_3 after removal of the sacrificial layer produces an interface trap density (D_{it}) as low as 1.5×10^{11} cm^{-2} eV^{-1} at the mid-gap energy of silicon. However, a greatly reduced mid-gap D_{it} (2×10^{11} cm^{-2} eV^{-1}) is possible even with a simple air annealing procedure having a maximum temperature of 400 °C.

1. Introduction

In recent years, nano- and microscale structure formation on semiconductor surfaces has become an extremely promising option for next-generation solar cells.[1,2] For example, nanotexturization decreases the surface reflectance of solar cells and enhances absorption of light.[3] Furthermore, the shortened carrier collection paths for electrons significantly reduce bulk recombination losses in nanostructure-based p-n junctions.[4] Previously, we showed 9.7% efficiency for radial junction Si micropillar (Si MP) arrays, with an optimized p-n junction configuration.[5] However, to date, nano/microstructured Si solar cells exhibit lower conversion efficiency compared to conventional cells due to enhanced surface recombination originating from their high surface-to-volume ratio.[6]

Many previous studies focus on surface passivation effects on Si-based nano/microwire solar cells by applying different surface treatment processes and capping layers.[7–10] In addition to the detailed passivation mechanisms for these surface treatments, methods to characterize the detailed nature of passivation effects in high-aspect-ratio (HAR) structures have been examined intensively. Due to the particular challenges for direct application of standard techniques for surface defect characterization to nanostructured surfaces, estimation of critical parameters such as the surface recombination velocity, minority carrier lifetime, and interface trap density from planar samples has been employed widely in such research.[9,11,12] In this study, we use a novel electrochemical impedance method that allows direct characterization of interface trap density in high-aspect-ratio structures; the advantage of this approach is that the nanostructure interface, which can differ significantly in morphology from that of planar structures, can be experimentally measured instead of estimated using a planar sample as a proxy.

Aluminum oxide, Al_2O_3, deposited by atomic layer deposition (ALD) has been demonstrated to inhibit minority carrier recombination on lightly doped n- and p-type as well as highly doped p^+-type silicon surfaces.[13–16] In practice, it is virtually impossible to avoid the presence of a layer of SiO_2 interposed between silicon and ALD-grown metal oxides and, indeed, a thin SiO_2 layer acts as an effective template for initiation of film deposition by ALD.[17–20] "Chemical passivation" (e.g., reduction of the density of dangling bonds on or near the Si surface) can be achieved by growth of SiO_2.[21] In addition to chemical passivation by SiO_2, a strong field-effect passivation is found to play a vital role in the performance enhancement achieved by coating silicon solar cells with Al_2O_3, and is consistent with the presence of a large negative fixed charge density near Al_2O_3/SiO_2 interfaces.[9,16,22,23] Industrial application of ALD-grown

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metal oxides in photovoltaics is in principle limited due to the relatively low deposition rates.[24,25] One should still note however, that the implementation of ultrathin Al_2O_3 has resulted in excellent surface passivation and thus it can be used in production.[26,27]

In order to achieve ideal surface passivation of nano/micropillars, critical challenges such as the existence of pinholes and surface defects must be addressed. It is also difficult to observe directly the passivation effect in wire array devices. For example, solid-state capacitance–voltage (C–V) measurement, well-established for quantifying the oxide/semiconductor interface trap density energy distribution, requires conformal coverage of a highly conductive gate metal over the sample in order to define the device area.[28,29] This is challenging for topologically complex HAR pillar samples. Contactless C–V measurements, such as COCOS,[30] are widely used for planar Si samples, but as mentioned recently by Pasanen et al.,[31] interface trap density determination for HAR surfaces (such as black Si) has not yet been demonstrated unambiguously.

Here, we report on ultrathin atomic layer deposited Al_2O_3 passivation of Si MPs using electrochemical impedance spectroscopy (EIS) to characterize interface trap densities. The application of ultrathin Al_2O_3 in solar cells requires careful chemical passivation in order to obtain low surface recombination velocities. We evaluate quantitatively the reduction in interface trap density associated with improved chemical passivation. Recently, Meng et al. have demonstrated the application of EIS for defect characterization in oxide–semiconductor nanostructures such as Si nanopyramids obtained by KOH etching of bulk silicon wafers.[32] We find that low interface trap density (D_{it}), indicative of effective chemical passivation, of silicon MPs prepared by reactive ion etching (RIE) can be achieved with a simple process combining pre-ALD wet-etching and annealing with a maximum process temperature of 400 °C. Such low-temperature passivation processes can be beneficial from the viewpoint of reducing thermal budgets in Si solar cell fabrication.

It is well known that the effective lifetime of minority carriers (τ_{eff}), which is often used to assess the quality of interface defect passivation, is determined by D_{it} and fixed charge density (Q_{ss}) values.[33,34] However, to the best of our knowledge, there is no experimental demonstration of this relationship in nano/microstructured silicon due to the great difficulty of performing D_{it} and Q_{ss} measurements with solid-state contacts to HAR devices. This work provides evidence of the trends in D_{it} and τ_{eff} and the specific contribution of interface trap reduction to chemical passivation for different surface treatments of HAR Si micropillars.

2. Results and Discussion

The p-type Si MPs were formed on a 500 µm thick Czochralski (CZ) grown Si (100) wafer by photolithographic patterning and deep RIE. The diameter, spacing, and length of the Si MPs were 5 µm, 10 µm, and 36 µm, respectively. **Figure 1**a shows a scanning electron microscopy (SEM) image of a Si MP sample used in this research. We performed all experiments on boron-doped p-Si MPs. However, the obtained results should also be relevant to radial/axial p-n junction Si MPs.

It is well known that the RIE Bosch process forms highly defective etched silicon surfaces. The RIE process leaves the pillar sidewalls with ripples due to the nature of the process sequence which cycles between etch and passivation phases.[35,36] Figure 1b shows the 30° tilted SEM image of single Si MP sidewall, where distinctive ripples can be observed. One way to reduce the surface roughness on the sidewalls is formation of a sacrificial oxide layer. Figure 1c shows the MP surface after oxide stripping.

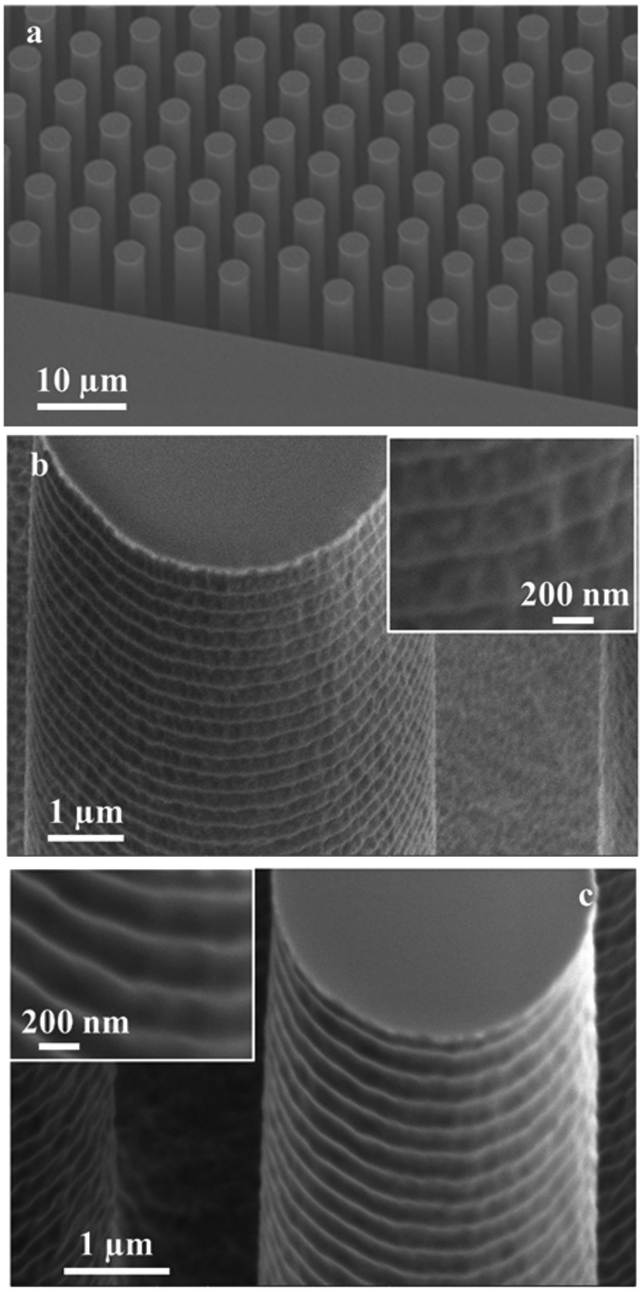

Figure 1. a) SEM images of the Si MPs array and b) the single Si MP sidewall surface after RIE process and c) after sacrificial oxide removal. SEM tilting angle is 30°. Insets: high-magnification SEM images of the ripples.

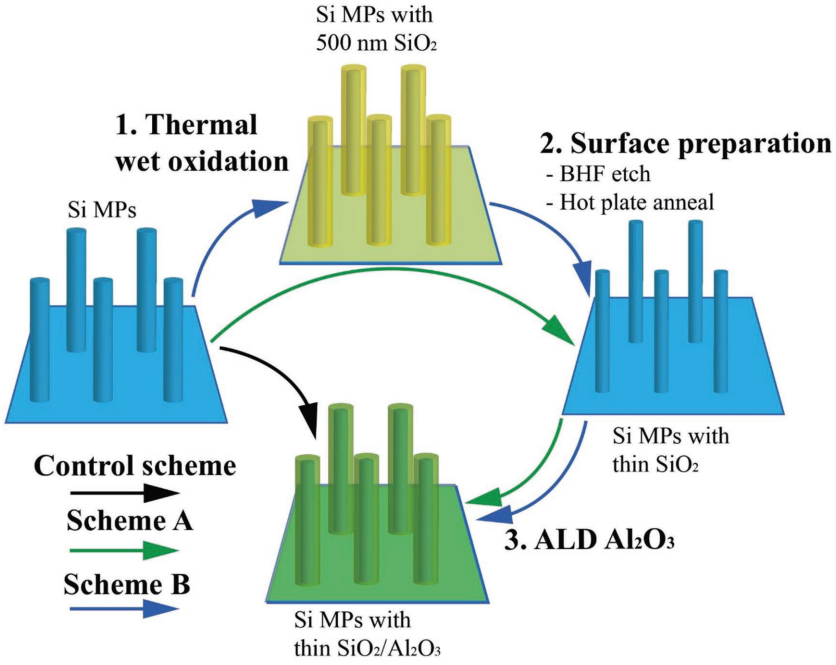

Figure 2. All passivation procedures for p-Si MPs: (1) formation of sacrificial thermal SiO_2 at 900 °C for 90 min; (2) BHF etch + hot plate anneal at 400 °C for 30 min; (3) 60 cycles ALD Al_2O_3.

To reduce the density of surface defects, we treated the silicon MPs using several different schemes. The control scheme did not include any surface pretreatment steps. Scheme A included a surface pretreatment as follows: 2 min BHF etching of the post-RIE native oxide-coated MPs followed by annealing in air on a hot plate at 400 °C for 30 min. Passivation scheme B had an additional thermal wet (water vapor) oxidation step for the formation of a sacrificial oxide layer in a tube furnace at 900 °C for 90 min before the surface pretreatment, which corresponds to a nominal SiO_2 thickness of 200 nm, as calibrated by oxidation of planar Si (100) wafers. Due to the much higher oxidation rate of the (110) orientation, the thermal wet oxide thickness formed on Si MPs was ≈500 nm.[37] The final step was identical for all three schemes and consisted of deposition of ≈4 nm of Al_2O_3 at 270 °C using 60 cycles of alternating trimethylaluminium (TMA) and H_2O precursor pulses. The pressure during ALD was ≈0.68 Torr, as maintained by dry N_2 flow, which is also used to purge the gas lines and chamber between ALD cycles. All passivation procedures are shown in **Figure 2**. After the ALD process, a back-contact to the silicon wafer was formed using an In-Ga eutectic. The active device area for EIS analysis was defined using standard two-component epoxy (Hysol 9460) and was in the range of 1–2 × 10^{-3} cm^2 as measured in an optical microscope.

Interface state density, D_{it}, values were extracted from the measured *C*–*V* and conductance–voltage (*g*–*V*) data using the full interface state model.[29] This method obtains a continuous distribution of interface traps as a function of their energy. To perform the calculation, the conventional single-energy Y equivalent circuit of a trap capacitance and two conductances (connecting to the conduction and valence bands) must be converted to a Δ equivalent circuit to facilitate integration of circuit elements over all trap energies.

First, we performed band alignment and carrier density versus applied bias simulations for the MOS structures. The simulations for the solid-state case can then be compared to the data from the EIS experiments. With a high ionic strength blocking electrolyte contact, the semiconductor undergoes inversion, depletion, and accumulation as its potential is increased versus that of the reference electrode, similar to the solid-state case when substrate bias is increased, due to the very low Debye length of the electrolyte, the large double layer capacitance, and the solution's high conductivity.[32] **Figure 3**a–c shows the band alignment of an $Al/Al_2O_3/SiO_2$/p-Si MOS structure in accumulation, flat band, and inversion regimes, respectively. The charge carrier densities, and therefore the capacitance, can be calculated as a function of gate voltage as it is swept from accumulation, where the surface charge density on the semiconductor is dominated by holes, to inversion, where it is dominated by electrons. The *C*–*V* curve of an ideal MOS structure has been calculated by taking the derivative of the total sheet charge density with respect to the bias voltage

$$C = \frac{dQ}{dV} \tag{1}$$

where *C* is the differential capacitance per unit area, *Q* is the sheet charge density per cm^2, and *V* is the applied bias. The simulated quasistatic *C*–*V* curve of the ideal p-type MOS capacitor structure is shown in Figure 3d. The inversion region (at positive gate bias) shows the predicted rise in capacitance under quasistatic conditions due to the formation of a thin inversion layer at the interface.

In order to provide solid-state *C*–*V* characterization as a reference, a control MOS structure with Al gate was prepared for MPs which underwent the control passivation scheme. Figure 3e illustrates the *C*–*V* characteristics of the MOS structure in the 1–800 kHz frequency range normalized to oxide capacitance (C_{ox}) at 1 kHz. The abnormally large capacitance dispersion in accumulation indicates high leakage current through the oxide. As explained below, this phenomenon can be attributed to a very rough Si surface as a result of the RIE process.

To improve surface passivation of the Si MPs, we applied surface treatment Scheme A, which includes wet etching of the native oxide and formation of a new oxide layer by baking the sample in air on a hot plate. It should be noted that below 600 °C, native oxide growth is approximately self-limited for growth times less than 3 h;[38] although, at elevated temperatures (400 °C in our case) the growth rate of native oxide occurs much faster than at room temperature. About 1 nm of native oxide was formed after hot plate baking according to ellipsometry. Chowdhury et al. recently investigated native silicon oxide and silicon nitride (SiN_x), deposited by plasma enhanced chemical

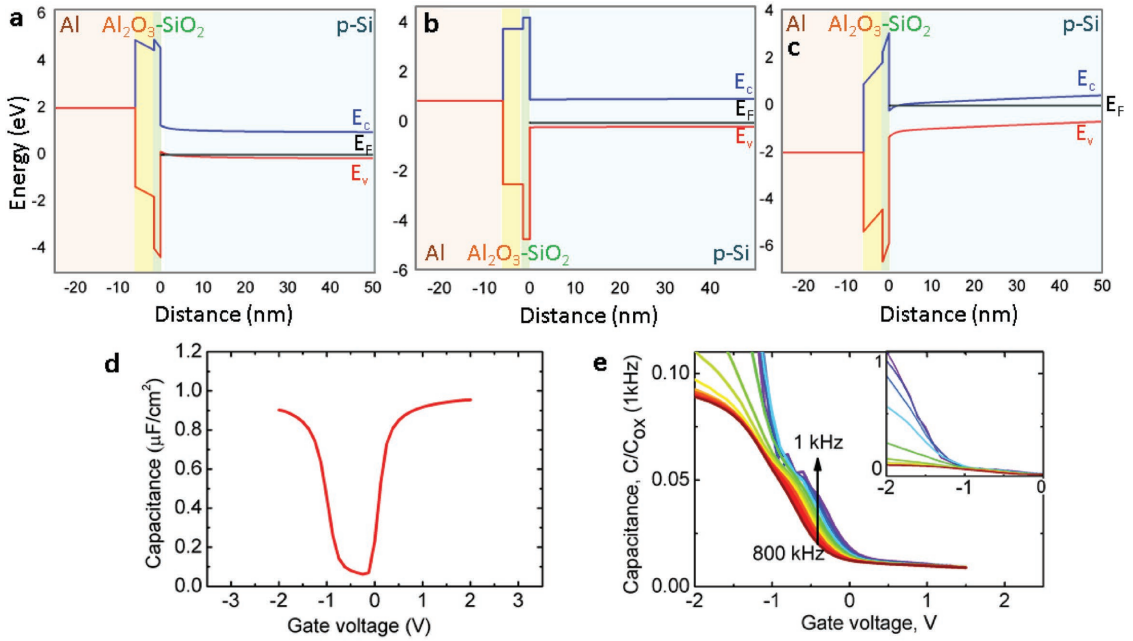

Figure 3. Band alignment of MOS structure $Al/Al_2O_3/SiO_2/p\text{-}Si$ in a) accumulation, b) flat band, and c) inversion modes; d) the simulated quasistatic *C–V* curve of the MOS structure; e) multifrequency solid-state *C–V* data from the $Al/Al_2O_3/p\text{-}Si$ MP sample. Inset represents the full capacitance range *C–V* characteristics.

vapor deposition, for surface defect passivation of c-Si.[39] ≈1 nm growth of native oxide was reported to result in a very low dangling bond defect density of 2×10^{10} cm^{-2} as calculated from excess carrier density dependent lifetime measurements using the dangling bond interface recombination model.[40] We took a similar approach for our passivation schemes. Scheme B included an additional step of wet oxidation to form a thick sacrificial oxide layer. Oxidation at high temperature is known to form oxide by consuming silicon from the substrate. The application of this step before etching and Al_2O_3 ALD can lead to improvements in the surface of Si MPs by reducing the sidewall roughness of MPs damaged by RIE, as shown in Figure 1b,c.

Figure 4 shows *C–V* characteristics of each passivation scheme in the 1–100 kHz frequency range extracted from EIS data. To simplify direct comparison of different passivation schemes, the capacitance was normalized to C_{ox} at 1 kHz, similar to the method of ref. [41]. Area-normalized *C–V* characteristics are shown in Figure S1 (Supporting Information). The capacitance is plotted versus substrate potential, which is opposite to the gate voltage in solid-state *C–V* measurements and simulations. The *C–V* plots show that, starting from inversion (at more negative substrate potentials), the capacitance is at a minimum value and begins to increase as the potential is increased toward depletion. Near depletion, we see a feature in the capacitance in all the measurements at ≈−1 V substrate potential and low frequencies. This feature is attributed to the capacitance associated with charging/discharging of interface traps as will be explained later.[28] Then, as the substrate potential is further increased to more positive substrate potentials, the capacitance reaches its maximum in accumulation.

As clearly seen from the *C–V* data, the curves have a significant frequency dispersion in accumulation. In solid-state data (see Figure 3e), this phenomenon is related to leakage current through the oxide layer due to pinholes caused by the scalloped surface of the etched MPs (Figure 1b).[35,36] The EIS method suppresses charge transfer current through the solid-liquid interface. Due to the absence of a dissolved redox couple, the electrolyte acts as a blocking layer for electronic carrier transport.[42] The dispersion in accumulation in the EIS method likely comes from the dependence of the double-layer capacitance on measurement frequency.[43] For HAR samples, this effect can be significant due to the large surface area. In accumulation, the effect of the double-layer capacitance being in series with the semiconductor–oxide system is maximized due to comparable values of these capacitances (see Figure S2, Supporting Information). However, in depletion/inversion, the effect is small and the interface trap density can be estimated from measured *C–V* and *g–V* data.

To compare the simulations with the EIS data, one should align the voltage scales with the vacuum level. A negative shift of 0.54 V was applied to the simulated *C–V* curve due to the difference in the work function of Al and the electrochemical potential of the Ag/AgCl (sat. KCl) reference electrode (4.1 and 4.64 eV vs vacuum, respectively).[44,45] The *C–V* curves are additionally shifted from the ideal *C–V* characteristic due to the presence of interface and bulk fixed charge. Quantum-mechanical simulations of the ideal *C–V* curve provide an estimate of the fixed charge areal density, Q_{ss}. This value, -9×10^{12} cm^{-2}, is larger in magnitude than typically observed in *C–V* measurements of $Si/SiO_2/Al_2O_3$, where negative interface fixed charge at the semiconductor–oxide interface is often partially compensated by positive bulk fixed charge in the oxide.[46] Observation of net negative fixed charge in these experiments is consistent with the ALD-grown oxide being very thin.[32,46]

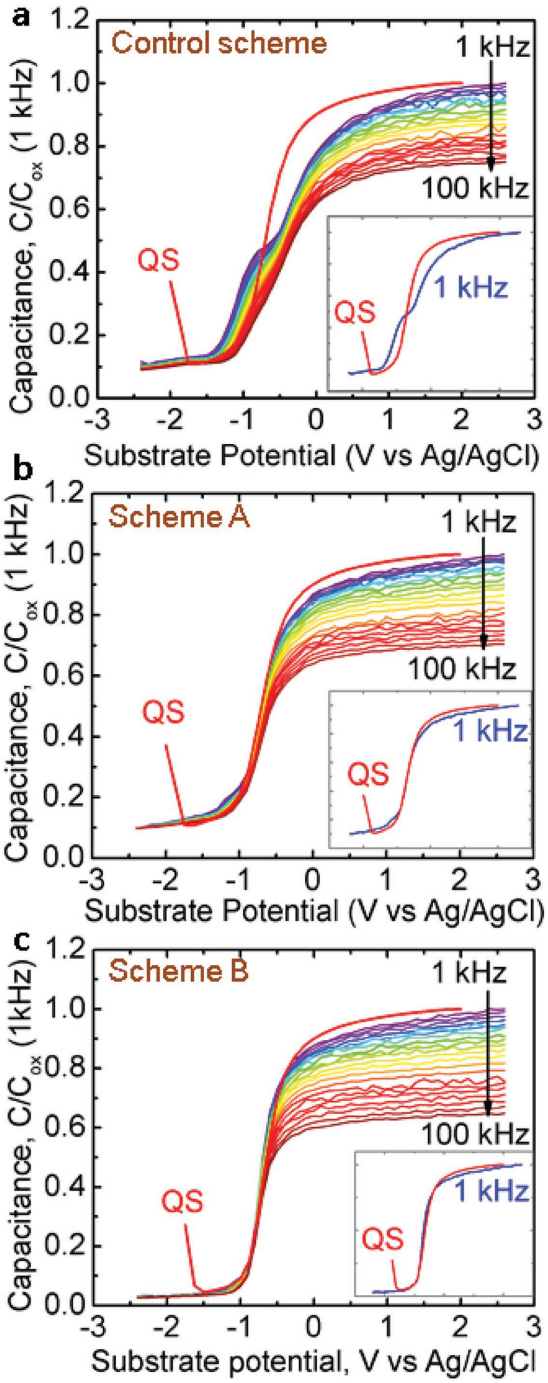

Figure 4. *C–V* curves extracted from EIS measurements of p-doped Si MPs with different passivation schemes: a) only 4 nm Al_2O_3 cap; b) scheme A with surface pretreatment and 4 nm Al_2O_3 cap; c) scheme B with etching 500 nm of previously formed sacrificial thermal silicon oxide, surface pretreatment, and 4 nm Al_2O_3 cap. Insets: 1 kHz *C–V* curve of each passivation scheme versus simulated quasistatic (QS) *C–V* curve (plus additional fixed charge).

We observe a frequency-dependent feature in the capacitance at ≈–1 V versus Ag/AgCl, consistent with the presence of interface traps (see Figure 4a).[32] These traps can be charged/discharged by applying a small AC voltage at different

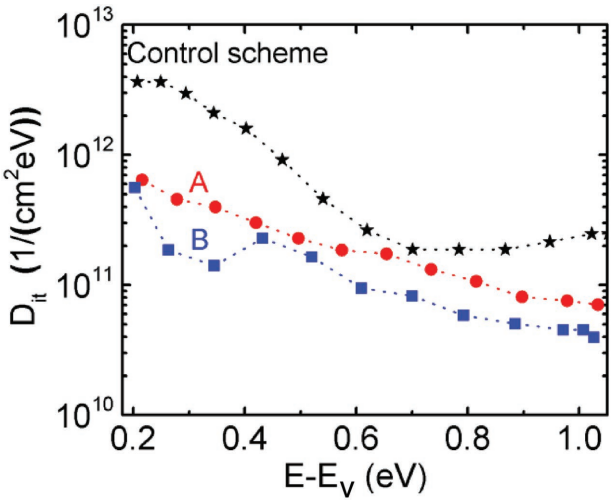

Figure 5. Extracted density of interface states (D_{it}) using the full interface method for three different passivation schemes: a) only 4 nm Al_2O_3 cap (black); b) surface pretreatment and 4 nm Al_2O_3 cap (red); c) etching 500 nm of previously formed thermal silicon oxide, surface pretreatment, and 4 nm Al_2O_3 cap (blue).

frequencies, leading to changes in the capacitance of the electrolyte–oxide–semiconductor system. Surface pretreatment can significantly decrease D_{it} (Figure 4b) by improving the Si/SiO_2 interface through formation of a native oxide of better quality compared to the air-exposed etched MPs. With an additional step of growth and removal of a high-temperature sacrificial thermal oxide, the interface trap density can be further suppressed (see Figure 4c). Thermal oxidation of the Si pillars, followed by BHF wet etching and reforming of a high-quality native oxide eliminates the majority of surface defects produced by the RIE process. The insets of Figure 4 show simulated QS and 1 kHz measured *C–V* data for each passivation scheme. An almost perfect match of the curves in the inset of Figure 4c confirms the improved passivation of oxide/silicon interface defects.

The interface state density can be estimated using the full interface state method.[29] The calculated distribution of interface states in the bandgap is plotted for all three passivation schemes of the p-Si pillars (**Figure 5**). The interface trap density at the mid-gap energy is lowered from 4.2×10^{11} to 2×10^{11} cm^{-2} eV^{-1} as a result of surface pretreatment and Al_2O_3 passivation and is further lowered to 1.5×10^{11} cm^{-2} eV^{-1} as a result of removal of the outermost 500 nm of the Si MPs by forming and etching the sacrificial thermal oxide prior to the surface pretreatment and Al_2O_3 passivation. It is well known that the main mechanism for recombination at semiconductor surfaces is electron–hole recombination at deep traps,[47,48] those producing energy levels located in the bandgap far ($\gg kT$) from the conduction and valence band edges. The interface state energy profiles in Figure 5 indicate that the passivation effects observed in these experiments are greater than that implied by the mid-gap D_{it} reduction from 4.2×10^{11} to 1.5×10^{11} cm^{-2} eV^{-1}. The reduction in D_{it} is even larger across most of the energy range from 0.3 to 0.8 eV above the valence band edge.

Furthermore, we performed quasi-steady-state photoconductance measurements (QSSPC) on Si MPs samples with different passivation schemes (see Figure S3, Supporting Information). The effective lifetime of minority carriers, τ_{eff}, is extracted from these measurements and compared with D_{it} values. A number of papers reported much lower τ_{eff} for HAR structures compared to planar samples with the same passivation method (µs vs ms).[11,49] This results from the fact that in high-quality bulk material, surface effects and enhanced high surface-to-volume structures dominate the minority carrier transport and, therefore, determine τ_{eff}. Moreover, passivation quality can be poor due to the deep and narrow geometry of HAR structures, which complicates uniform deposition of passivation layers. It is notable that the reduction of minority carrier concentration by the fixed charges of Al_2O_3 is the same for all passivation schemes and, as reported by Terlinden et al.,[22] in the case of thin oxide layers (only 4 nm in our case) chemical passivation plays a major role. Passivation scheme B resulted in a τ_{eff} of 4 µs, while the absence of a photoconductance signal was observed from the control sample. Finally, τ_{eff} below the detectable level (1 µs) was found for scheme A. Therefore, scheme B provides the best overall passivation, consistent with the D_{it} trend observed by EIS analysis of the interface trap density. It is worth noting that, in the case of radial p-n junction configuration, the diffusion length of minority carriers should be comparable to or larger than the radius of MPs for efficient carrier collection. This condition is achieved with the proposed passivation scheme.

Using passivation scheme B, we achieve a capacitance–voltage behavior consistent with a density of interface traps less than 2×10^{11} cm^{-2} eV^{-1} across almost the entire silicon bandgap. Moreover, even simple surface preparation by wet etching and low-temperature oxidation results in a substantial improvement in the chemical defect passivation of Al_2O_3-coated Si MPs. This result is significant as it shows the potential for achieving relatively electrically passive Si MPs surfaces with an inexpensive, low-thermal-budget process.

3. Conclusion

We studied surface passivation of RIE-formed Si MPs by different process schemes including thermal oxidation and ALD Al_2O_3. The *C–V* properties were characterized using the EIS method, allowing us to carry out measurements on high-leakage (scalloped surface) HAR structures. A passivation scheme with a high-temperature wet oxidation step for the formation of a sacrificial oxide layer produces the lowest interface trap density of 1.5×10^{11} cm^{-2} eV^{-1} at the mid-gap energy of silicon, resulting in an effective minority carrier lifetime of 4 µs in the silicon MPs. In addition, we found that a simple procedure including air annealing at 400 °C prior to ALD Al_2O_3 deposition reduces interface trap density across the silicon bandgap to almost as low a value as the sacrificial oxide process. With further optimization, this inexpensive and low-thermal-budget passivation scheme may be useful for fabrication of efficient silicon MP solar cells and photodetectors.

4. Experimental Section

Electrochemical Impedance Spectroscopy: Electrochemical impedance spectroscopy was performed on different samples to obtain the real and imaginary parts of the impedance from a BioLogic VSP potentiostat. A saturated aqueous solution of KCl was used as a conductive electrolyte, which replaces the metal gate used in a typical metal–oxide–semiconductor capacitor. Three electrode scheme consists of Ag/AgCl/saturated KCl (aq) as the reference electrode and a Pt wire counter electrode. EIS was recorded from 1 to 100 kHz at (–2.5; 2.5 V vs Ag/AgCl) substrate voltage range with an ac oscillation amplitude of 10 mV. To reduce instability during the measurements, waiting time of one full period of the applied ac perturbation before each new frequency and three measurements at each frequency were made. A simple equivalent circuit with parallel capacitance and resistance was used to calculate capacitance versus the applied bias on the sample.[32]

Simulations of the Band Alignments: Simulations of the band alignments of the structures and of the ideal *C–V* behavior of a p-type MOS capacitor were performed using the Next Nano software package.[50] Numerical simulations of the structure with Al gate as a visualization of the band alignment at the $Si/SiO_2/Al_2O_3$ interface with applied bias were provided. Due to the much larger diameter of MPs compared to the depletion width in p-Si (300 nm for 10^{16} cm^{-3} doping), simple 1D simulations correctly capture the physics. To simulate the band-bending at the semiconductor–oxide interface exactly, the 1D Schrödinger–Poisson equation was solved self-consistently. The following parameters were used: SiO_2 thickness of 1 nm, Al_2O_3 thickness of 4 nm, and doping concentration of p-type Si of 3×10^{16} cm^{-3}. A silicon dioxide layer was introduced in the simulations due to oxide formation between the Si surface and the deposited Al_2O_3 dielectric layer either during or prior to the ALD process. The bandgaps of amorphous Al_2O_3 and SiO_2 are taken as 6.1 and 8.9 eV, respectively.[51] The reported Schottky barrier at the Al/Al_2O_3 interface is 2.9 eV.[52]

MOS Device Fabrication: MOS structures for reference solid-state *C–V* measurements were fabricated on the silicon MPs using the control passivation scheme and a nominally 30 nm thick Al gate metal layer was e-beam evaporated through a shadow mask. Circular gates of diameter 250 µm were formed.

Quasi-Steady-State Photoconductance Measurements: QSSPC characterization was performed by means of a WCT-120TS photoconductance setup from Sinton Instruments. It consists of an inductive coil that converts the current produced by the excited carriers into a voltage signal which is coupled to the conductivity of the wafer.[53] The photoconductivity decay with the flash lamp intensity decay was measured. The minimum detectable lifetime is 1 µs.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

electrochemical impedance spectroscopy, micropillars, passivation, silicon

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