Mobility Degradation of 28-nm Bulk MOSFETs Irradiated to Ultrahigh Total Ionizing Doses

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***Abstract*—Using the *Y*–function method, this paper experimentally investigates the effects of total ionizing dose up to 1 Grad on the channel mobility of a commercial 28-nm bulk CMOS process.**

***Keywords*—Interface traps, mobility degradation, oxide-trapped charges, shallow trench isolation, total ionizing dose, 28-nm bulk MOSFETs, *Y* function**

I. INTRODUCTION

The total amount of energy absorbed by a MOSFET from incident ionizing radiation, measured by total ionizing dose (TID) using either a unit called rad or the SI unit called Gy (1 Gy=100 rad=1 J/kg), can build up an amount of trapped charges in oxides and activate hydrogen-passivated interface traps at silicon/oxide interfaces [1]. TID-induced oxide- and interface-trapped charges influence electrical characteristics of electronic devices [2]. For example, it gives rise to a drive current loss by increasing the absolute threshold voltage and/or reducing the effective channel mobility [3]. The innermost electronics of CERN's forthcoming high-luminosity Large Hadron Collider (HL-LHC) is anticipated to experience an unprecedented radiation level up to 1 Grad of TID and $10^{16}\mathrm{neutrons/cm^2}$ of hadron fluence over ten years of operation [4]. This might lead to device degradation and even failure [5]. With the perspective of using advanced CMOS technologies in the HL-LHC, we have been studying the radiation tolerance of a commercial 28-nm bulk CMOS process up to 1 Grad [3], [6]. Using the *Y*–function method [7], this paper experimentally investigates the effects of TID on the channel mobility in linear operation.

II. CHANNEL MOBILITY EXTRACTION

This work studies the drain-to-source current I_{DS} in strong inversion of linear operation at a small value of drain-to-source voltage ($V_{DS} = 0.01\,\mathrm{V}$). Using the drift-diffusion model for drain current $I_{DS} = W\mu_{eff}C_{ox}\left(V_{GB} - V_T\right)V_{DS}/L$ and the first-order model for mobility degradation $\mu_{eff} = \mu_0/[1 + \theta(V_{GB} - V_T)]$ gives the current-voltage expression:

$$I_{DS} = \frac{W}{L}\frac{\mu_0}{1+\theta(V_{GB}-V_T)}C_{ox}\left(V_{GB}-V_T\right)V_{DS}, \qquad (1)$$

where W and L are the effective channel width and length, respectively, μ_{eff} is the effective channel mobility, μ_0 is the low-field channel mobility, θ is the effective mobility degradation coefficient, V_{GB} is the gate-to-bulk voltage, V_T is the charge threshold voltage, and C_{ox} is the gate oxide capacitance per unit area. Differentiating I_{DS} versus V_{GB} for G_m and combining it with (1), we obtain the well-known Y function [7]:

$$\frac{I_{DS}}{\sqrt{G_m}} = \sqrt{\frac{W}{L}\mu_0 C_{ox} V_{DS}}\left(V_{GB}-V_T\right). \qquad (2)$$

In strong inversion, $I_{DS}/\sqrt{G_m}$ is independent of θ and proportional to V_{GB}, as evidenced by the $|I_{DS}|/\sqrt{G_m}$ versus $|V_{GB}|$ curves in Fig. 1a-b and Fig. 1e-f. V_T is defined as the $|V_{GB}|$–intercept of the linear extrapolation and μ_0 is deduced from the slope of the extrapolated line. At high TID levels, narrow-channel MOSFETs demonstrate a higher V_T shift and a more significant μ_0 reduction than wide-channel MOSFETs.

To get an accurate extraction of V_T, μ_0, and θ, this linear extrapolation has to be applied in a sufficient strong inversion region [7]. This can be checked by the occurrence of the $\theta(|V_{GB}|)$ plateau at high values of $|V_{GB}|$. Combining the derived G_m with (1) enables us to extract θ:

$$\theta = \left[\frac{I_{DS}}{G_m\left(V_{GB}-V_T\right)} - 1\right]\frac{1}{V_{GB}-V_T}. \qquad (3)$$

Fig. 1c-d and Fig. 1g-h confirm the $|V_{GB}|$ independence of θ in strong inversion. Due to the significant V_T shift at high TID levels, narrow-channel *p*MOSFETs have a reduced $|V_{GB}|$ range with the validity of the *Y*–function method. Furthermore, the corresponding θ tends to be zero, indicating a negligible influence of $|V_{GB}|$ on the μ_{eff} of narrow-channel *p*MOSFETs.

III. GIGARAD-TID EFFECTS ON CHANNEL MOBILITY

Fig. 2 plots the calculated μ_{eff} using the extracted V_T, μ_0, and θ versus $|V_{GB}| - V_T$. We observe a $|V_{GB}|$-induced mobility degradation, except for narrow-channel *p*MOSFETs that display a $|V_{GB}|$-independent μ_{eff} at high TID levels. This corresponds to their negligible θ at high TID levels. We also observe a higher μ_{eff} reduction for narrow-channel MOSFETs than wide-channel MOSFETs. Note that μ_0 corresponds to $|V_{GB}| - V_T = 0$. As expected, the low-field electron mobility is around three times the low-field hole mobility.

The μ_0 and V_T variation is plotted versus TID in Fig. 3. We see a limited influence on μ_0 ($< 20\%$) and V_T ($< 7\%$) of wide-channel MOSFETs even at ultrahigh TID levels. This indicates the improved radiation tolerance of the advanced gate stacks. However, narrow-channel MOSFETs undergo a significant μ_0 reduction up to 36% for *n*MOSFETs (Fig. 3a) and up to 73% for *p*MOSFETs (Fig. 3c). This is because narrow-channel MOSFETs are more sensitive to the TID-induced charge trapping related to the thick STI oxides. Near threshold, oxide-trapped charges near silicon/STI interfaces and trapped charges at silicon/STI interfaces act as Coulomb scattering centers that are believed to contribute to this significant mobility degradation. For narrow-channel *n*MOSFETs, the negative V_T shift (Fig. 3b) mitigates the effect of μ_0 reduction on the drive current. However, for narrow-channel *p*MOSFETs, oxide- and interface-trapped charges together increase V_T up to 36% (Fig. 3d) and degrade μ_0 up to 73% that considerably reduces the drive current and leads to a much worse situation.

IV. CONCLUSION

Using the *Y*–function method, we extract the channel mobility of commercial 28-nm bulk MOSFETs in strong inversion of linear operation before irradiation and at different TID levels. Extracted results confirm the enhanced radiation tolerance of wide-channel MOSFETs that is mostly due to the advanced

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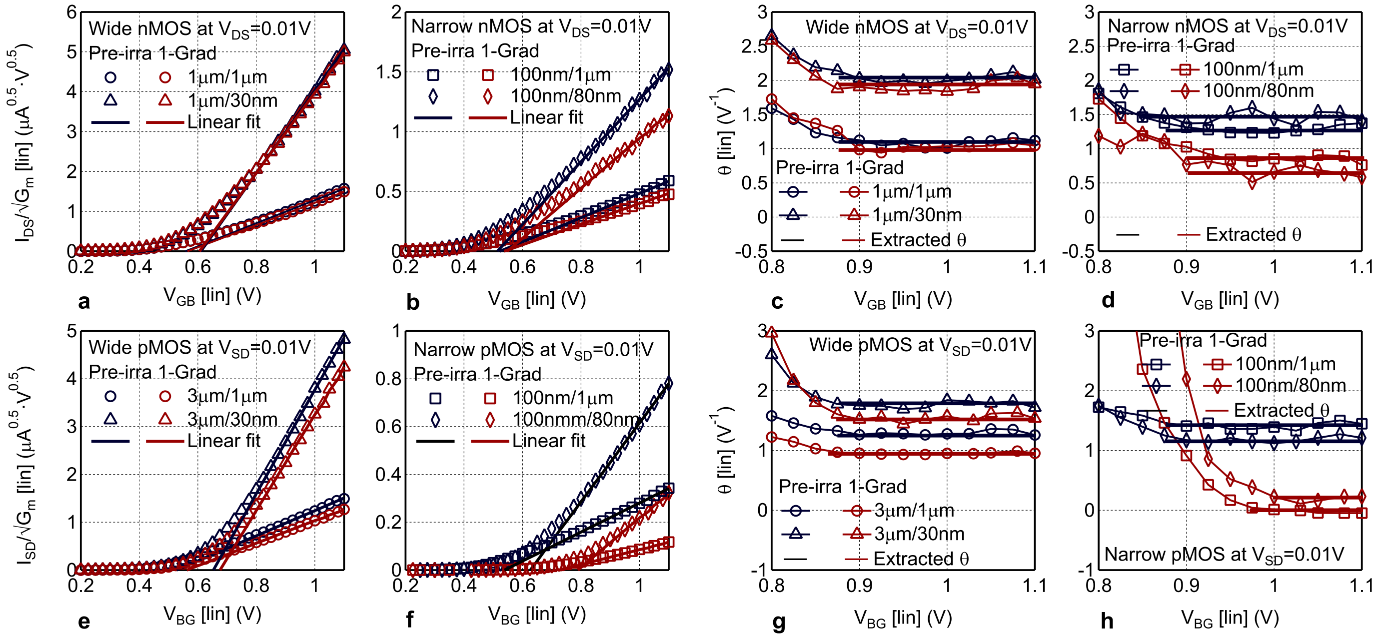

Fig. 1: Y–function $|I_{DS}|/\sqrt{G_m}$ (abef) and mobility degradation coefficient θ (cdgh) of n- (a-d) and pMOSFETs (e-h) versus gate-to-bulk voltage $|V_{GB}|$.

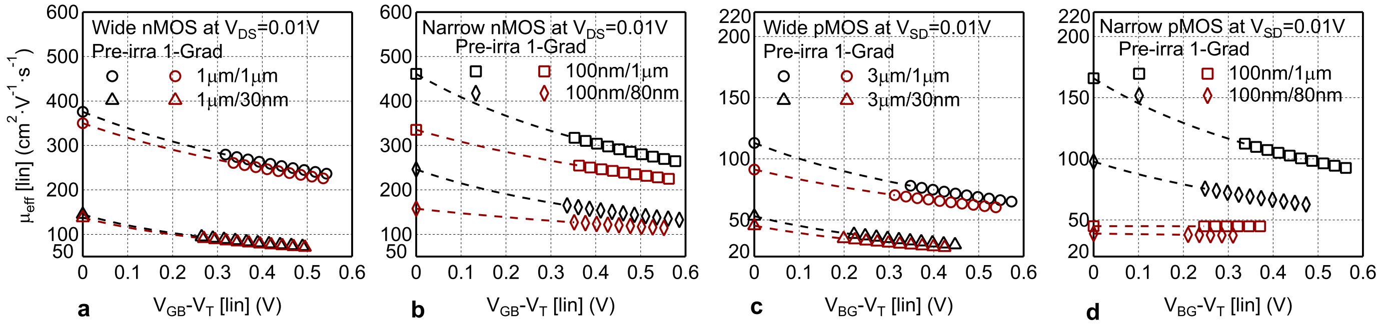

Fig. 2: Effective channel mobility μ_{eff} of n- (ab) and pMOSFETs (cd) versus overdrive voltage $|V_{GB}| - V_T$.

gate stacks in nanoscale CMOS technologies. Narrow-channel MOSFETs demonstrate a rather high mobility reduction that is attributed to the Coulomb scattering of the charge buildup related to the thick shallow trench isolation oxides.

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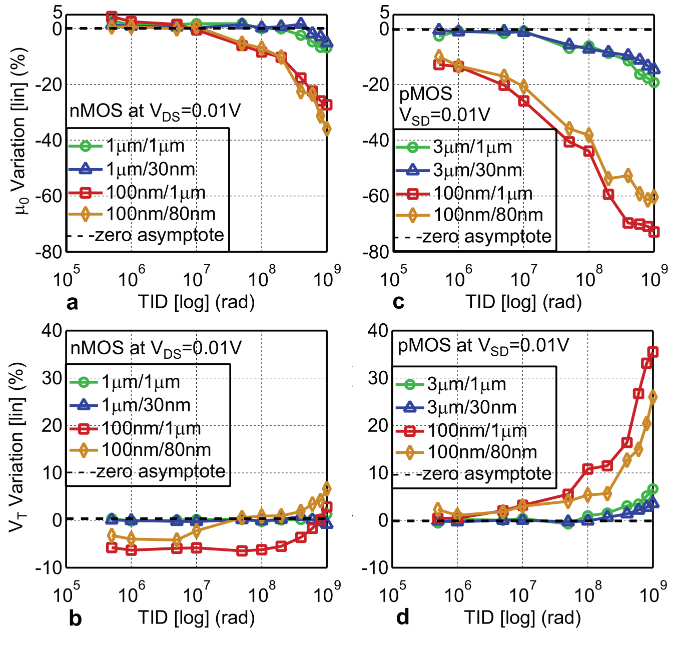

Fig. 3: Variation of low-field channel mobility μ_0 (ac) and threshold voltage V_T (bd) of n- (ab) and pMOSFETs (cd).