Implementing ultra-high-value floating tunable CMOS resistors

A. Tajalli, Y. Leblebici and E.J. Brauer

A compact high-value floating resistor utilising PMOS devices in the subthreshold region is introduced. A test chip has been fabricated in 0.18 μm CMOS technology to verify the proposed concept. This technique has been applied to design a reconfigurable sixth-order very-low-cutoff-frequency MOSFET-C filter.

Introduction: Integrated high-value resistors (HVR) are key elements in many applications. Compact HVRs can be applied for biasing purposes or for implementing very-low-frequency filters [1, 2]. In addition to achieving high resistance, usually it is necessary to have good tuning capability of the resistor value, thus the controllability of the HVR is another important design issue. In this Letter, a compact HVR is introduced that utilises only PMOS transistors operating in the subthreshold regime. The resistance is adjustable in a very wide range. This property makes this technique very suitable for ultra-low-power reconfigurable applications. A test chip has been fabricated in conventional 0.18 μm CMOS technology and characterised to verify this concept. The proposed HVR has been applied to implement a low-frequency MOSFET-C filter with a wide tuning range and a constant dynamic range (DR).

Proposed HVR structure: To implement very-large-value resistors utilising conventional MOS transistors biased in the triode region, very long channel devices are needed. Fig. 1 (inset) shows the proposed device in which the transistor is biased in the subthreshold regime [3, 4]. In this configuration, the bulk of the PMOS device (which is an isolated n-well) is connected to its drain. Thus, by increasing V_{SD}, the threshold voltage of this device is modified, and consequently, the drain current will increase. This dependence of the current on drain voltage results in a large and finite output conductance that can be expressed as follows, based on the EKV model [5]:

$$G_{SD} = (I_{SD}/nU_T)[n/(1 - \exp(-V_{SD}/U_t)) - 1] \quad (1)$$

where $U_t = kT/q$ is the thermal voltage, and n is the subthreshold slope factor of the proposed PMOS device. It can also be shown that, for zero voltage drop across the source-drain, the finite conductance (output resistance) of the device can be calculated as:

$$G_{SD0} = G_{SD}|_{V_{SD}=0}(I_0/U_T)\exp(V_{SG}/nU_t) \quad (2)$$

where $I_0 = 2n_p\mu C_{ox}(W/L_e)U_T^2\exp(-|V_{T0}|/nU_t)$ (μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, V_{T0} is the threshold voltage of PMOS device, W is the width of device, and L_e is the effective device length). G_{SD0} in (2) depends on V_{SG} and hence the value of this resistance can be adjusted through V_{SG}. Note that (1) and (2) are valid for $V_{SD} \geqslant 0$. When V_{SD} becomes negative, the device switches to moderate inversion and the current increases considerably.

Fig. 1 shows the measured I–V characteristics of the proposed PMOS device implemented in 0.18 μm technology. As this Figure shows, the device exhibits a very high resistivity for $V_{SD} > 0$ V as predicted by (1). For $V_{SD} < 0$ V the current increases considerably and the device shows a low output resistance. By keeping the source–gate voltage (V_{SG}) low (in the order of thermal voltage U_t), it is possible to obtain a very high value resistor while the device size can be very small (in the proposed test chip, the size of the test device is $W/L = 0.25/0.4$ μm). Based on these results, the proposed device can be utilised to implement very high value resistors (in the range of $\times 100$ MΩ) with very good control on the resistance value through V_{SG}. For V_{SD} larger than 0.5 V, the source-bulk p–n junction diode begins to conduct significant current and hence it limits the useful voltage headroom for utilising the device as a resistor.

Fig. 2 shows the implementation of a floating resistor with a symmetric I–V characteristic. In this circuit, M_1 and M_2 are two identical PMOS devices that realise a symmetric resistance with respect to the polarity of the voltage applied across its terminals. The total resistance seen at the output is $R_{eq} = R_{SD1} + R_{SD2}$ while M_3 biases the gate–source of both transistors. According to Fig. 1, when $\Delta V > 0$ V, then $R_{SD1} \ll R_{SD2}$ and hence $R_{eq} \simeq R_{SD2}$, and for $\Delta V < 0$ V, then $R_{SD2} \ll R_{SD1}$ and hence $R_{eq} \simeq R_{SD1}$. Fig. 3*a* shows the measured I–V characteristics of the proposed floating resistor. The resistance of the circuit, which varies between 100 kΩ and 1 GΩ, can be changed by adjusting the gate voltage of the PMOS devices. Fig. 3*b* shows the measured resistance of the proposed circuit versus $V_{SG} = V_M - V_B$. For low V_{SG} values, the devices M_1 and M_2 are in the subthreshold region and hence, based on (2), the equivalent resistance of the circuit is very high and can be adjusted over a wide range. When V_{SG} increases, the devices enter a moderate and then a strong inversion region and hence the resistivity and tuning range will decrease.

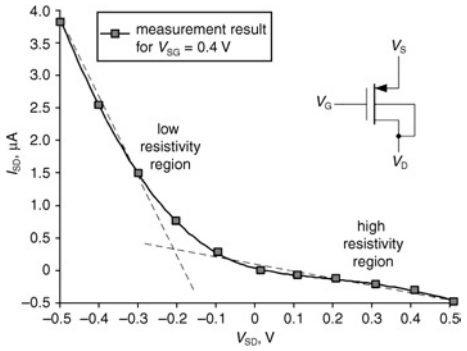

Fig. 1 *Measured I–V characteristics of bulk-drain connected PMOS device*

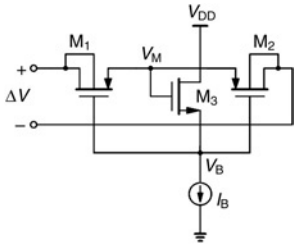

Fig. 2 *Configuration of proposed symmetric floating tunable resistor, consisting of two bulk-drain connected PMOS devices*

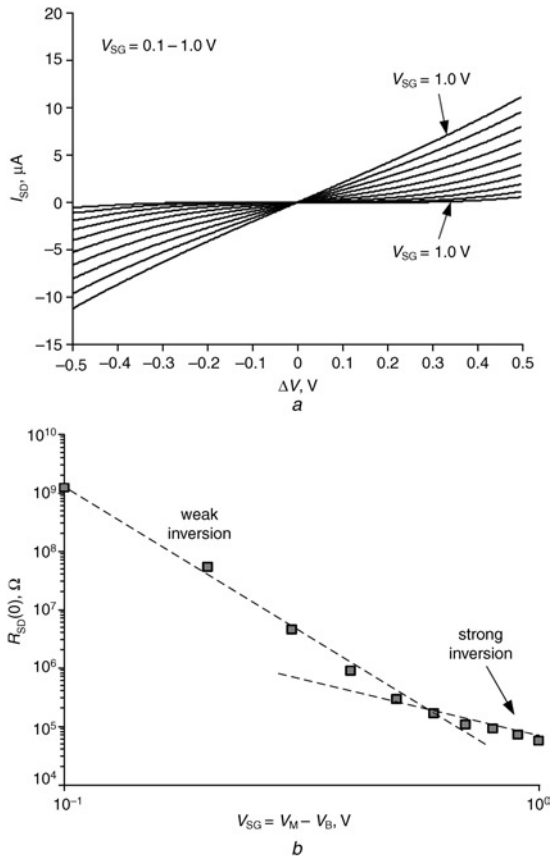

Fig. 3 *Measured characteristics*

a I–V characteristics of floating resistor for different bias voltages
b Variation of resistivity against V_{SG}

Application to filter design: The proposed compact and high resistivity circuit has been used to design a very-low-frequency sixth-order Butterworth MOSFET-C filter. A two-stage Miller compensated amplifier has been utilised for this purpose [6]. Fig. 4 shows the frequency response of this filter for different controlling current values (I_B in Fig. 2). Thanks to the wide tuning range of the resistors, the proposed filter can be applied in a very wide frequency range. In this example, the cutoff frequency of the filter can be adjusted from 3 Hz to 106 kHz without switching the filter capacitors and it is adjusted only by changing the value of resistors, via control current I_B. Based on (1) and (2), the linearity (or dependence of R_{SD} on V_{SD}) in the proposed resistor does not change by scaling the resistance value. Hence, it is expected that the linearity performance of the filter remains unchanged for different cutoff frequencies. Simulated total harmonic distortion (THD) shows less than 5 dB variation for different filter cutoff frequencies. Meanwhile, the total RMS (root mean square) noise of the filter is 260 μV_{rms} for the lowest cutoff frequency and changes by less than 12% for the entire tuning range thanks to the constant capacitor sizes. Based on these results, the proposed approach offers a very wide tuning range filter with an almost constant dynamic range (DR).

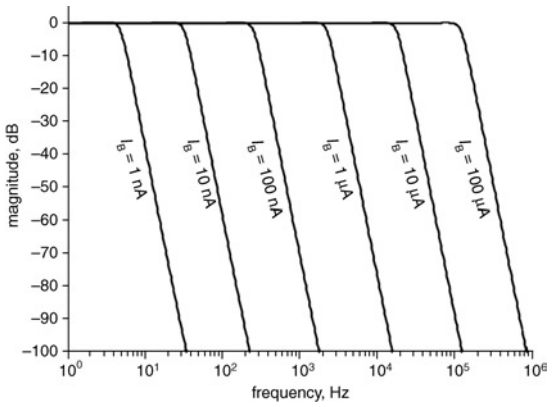

Fig. 4 *Frequency response of proposed sixth-order MOSFET-C filter controlled by I_B*

Conclusions: A very compact configuration for implementing very-high-value tunable floating resistors has been proposed. Biased in the subthreshold regime, two small-size PMOS devices with shorted bulk-drain terminals are used to implement the high-resistance element. Measurement results in conventional 0.18 µm CMOS technology confirm the proposed concept. Based on the proposed device, a very-wide-tuning-range constant dynamic range MOSFET-C filter has been designed and demonstrated.

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