

Hardware Implementation of Digital Signal Processing Algorithms for Programmable Epilepsy Control Systems

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To my parents, Manizhe & Mehdi ...

To my Sister, Niloufar ...

To epileptic patients ...

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Chapter 0

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Abstract

Epilepsy is a common chronic neurological disorder that causes recurring seizures and affects more than 50 million people worldwide. Implantable medical device (IMD)s are regarded as effective tools to cure patients who suffer from refractory epilepsy. Seizures of patients with intractable epilepsy can be controlled by neither currently available anti-seizure drugs nor resection surgery. In these cases, epilepsy control implants can reduce the frequency and severity of seizures. Furthermore, patients can use IMDs in conjunction with a reduced dosage of medication to prevent severe side effects.

A closed-loop epilepsy control implant applies electrical stimulation to specific brain tissues according to signal processing and seizure detection tasks conducted by an automatic seizure detector. Hardware implementation of signal processing algorithms is a challenging task to fulfill the stringent constraints of the implants in terms of power consumption, area occupation, hardware complexity and real-time operation.

System-level analysis of closed-loop seizure control implants is performed using the models of different components in Simulink software. The main properties of different components of the implant are modeled to simulate the operation of the implant. In addition, the temperature elevation of the implant, which highly impacts the safety and performance of the system in the long run, was investigated. The temperature elevation is controlled by the adjustment of stimulation parameters in order to maintain the temperature rise of the implant lower than 1°C.

A novel two-stage feature extraction method is developed in this thesis to offer accurate energy-efficient biomedical signal processing in the implant. The features available in the feature pool are divided into two groups, and extracted in the monitoring and detection stages. Extraction of the majority of the features is disabled during long inter-ictal periods which enables low-power consumption of the implant.

Intracranial electroencephalography (iEEG) signals are used to monitor and detect seizure events. iEEG signals are recorded by microelectrode arrays that consist of tens of electrodes. Signal processing applied on a large dimension of EEG signals is a crucial impediment for hardware-friendly and low-power seizure detection. A framework that contains a mutual electrode channel and feature dimension reduction technique is proposed to significantly

reduce the computation complexity of signal processing on hardware.

Moreover, seizure detection based on machine-learning techniques is studied in this thesis. Various types of machine learning techniques are reported in the literature while their hardware compatibility is not taken into account. Thus, the architecture of a Random Forest (RF) classifier is optimized in terms of classification accuracy and hardware complexity. The RF classifier with optimized hyperparameters is implemented on an Field-Programmable Gate Array (FPGA) to perform the seizure detection task.

In addition, the novel concept of programmable seizure detection is introduced for the first time in the literature. Programmable seizure detection enables a continuous interaction between users and implants. As a consequence, neurologists can adjust device's properties and the patients can play an important role in improving the effectiveness of their treatment. A 32-bit RISC processor compatible with implants is designed and implemented on an FPGA to realize the programmability function. Different therapy programs can be defined by neurologists and patients have the opportunity to switch between the available therapy options with respect to their current conditions and needs. Also, the RISC processor is used to generate a unique logical classification function to classify Intracranial Electroencephalography (iEEG) signals considering therapeutic targets and power consumption of the device.

Lastly, a digital one-shot charge balancing circuit is proposed which applies a hybrid charge balancing technique to ensure safe long-term operation of the implant. In this technique, charge balancing is realized using a combination of anodic pulse modulation and offset balance current injection. The designed digital charge balancer is implemented on a Cyclone IV Intel FPGA.

Key words: Epileptic seizure detection, Biomedical signal processing, FPGA implementation, RISC processor, Digital charge-balancing, Implantable seizure detector.

Résumé

L'épilepsie est une maladie neurologique chronique courante qui provoque des crises récurrentes et affecte plus de 50 millions de personnes dans le monde. Les IMDs sont considérés comme des outils efficaces pour soigner les patients souffrant d'épilepsie réfractaire. Les crises des patients atteints d'épilepsie réfractaire ne peuvent être contrôlées ni par les médicaments anti-épileptiques actuellement disponibles ni par la chirurgie de résection. Dans ces cas, les implants de contrôle de l'épilepsie peuvent réduire la fréquence et la gravité des crises. De plus, les patients peuvent utiliser les IMDs et une dose réduite de médicaments pour prévenir les effets secondaires graves.

Un implant de contrôle de l'épilepsie applique une stimulation électrique à des tissus cérébraux spécifiques en fonction du traitement des signaux et des tâches de détection de crises effectuées par un système automatique de détection de crises. L'implémentation matérielle des algorithmes de traitement de signal est une tâche difficile pour répondre aux contraintes strictes des implants en termes de consommation d'énergie, d'occupation de l'espace, de complexité matérielle et de fonctionnement en temps réel.

Une analyse au niveau du système des implants de contrôle de crise est réalisée en utilisant les modèles de différents composants dans le logiciel Simulink. Les principales propriétés des différents composants de l'implant sont modélisées pour imiter le fonctionnement de l'implant. De plus, la consommation d'énergie et l'élévation de la température de l'implant sont deux paramètres critiques qui ont un impact majeur sur la sécurité et les performances du système à long terme. Ces deux paramètres sont analysés et contrôlés par la modification des paramètres de stimulation afin de maintenir l'élévation de la température inférieure à 1°Celsius.

Une nouvelle méthode d'extraction de caractéristiques en deux étapes est proposée dans cette thèse pour permettre un traitement efficace en terme d'énergie des signaux biomédicaux dans l'implant. Les caractéristiques disponibles dans le pool de caractéristiques sont divisées en deux groupes et extraites lors des étapes de surveillance et de détection. L'extraction de la majorité des caractéristiques est désactivée pendant les périodes inter-ictales longues, ce qui permet une faible consommation d'énergie de l'implant.

Les signaux d'électroencéphalographie intracrânienne (iEEG) sont utilisés pour surveiller

et détecter les événements de crise. Les signaux iEEG sont enregistrés par des matrices de microélectrodes composées de dizaines d'électrodes. Le traitement de signal appliqué à une grande dimension de signaux EEG est un obstacle crucial pour une détection conviviale pour le matériel et à faible consommation d'énergie. Un cadre contenant un canal d'électrode mutuel et une technique de réduction de dimension de caractéristique est proposé pour réduire considérablement la complexité de calcul du traitement de signal sur le matériel.

De plus, la détection de crises basée sur des techniques d'apprentissage automatique est étudiée dans cette thèse. Divers types de techniques d'apprentissage automatique sont rapportés dans la littérature, mais leur compatibilité matérielle n'est pas prise en compte. Ainsi, l'implémentation FPGA de systèmes de détection de crises à l'aide de classificateurs Support Vector Machine (SVM) et RF est réalisée.

En outre, le concept novateur d'un dispositif de détection de crise programmable est introduit pour la première fois dans la littérature. La détection de crise programmable permet une interaction continue entre les utilisateurs et les implants. Par conséquent, les neurologues peuvent ajuster les propriétés de l'appareil et les patients peuvent jouer un rôle important dans l'efficacité de leur traitement. Un processeur RISC 32 bits compatible avec les implants est conçu et implémenté sur FPGA pour réaliser la fonctionnalité de programmation. Différents programmes thérapeutiques peuvent être définis par les neurologues et les patients ont la possibilité de passer entre les options thérapeutiques disponibles en fonction de leurs conditions et besoins actuels. De plus, le processeur RISC est utilisé pour générer une fonction de classification logique unique pour détecter les crises en tenant compte de l'objectif thérapeutique et de la consommation d'énergie de l'appareil.

Enfin, un circuit de rééquilibrage numérique de charge en cycle unique est proposé, qui applique une technique de rééquilibrage de charge hybride pour assurer le fonctionnement sûr à long terme de l'implant. Dans cette technique, le rééquilibrage de charge est réalisé en utilisant une combinaison de modulation d'impulsion anodique et d'injection de courant de rééquilibrage d'offset. Le rééquilibrage de charge numérique conçu est implémenté sur un FPGA Cyclone IV.

Mots clefs : Détection de crises épileptiques, Traitement des signaux biomédicaux, Implémentation FPGA, Processeur RISC, Équilibrage de charge numérique, Implant de détection de crises.

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Glossary

AC Alternating Current.

ADC Analog-to-Digital Converter.

AED Anti Epileptic Drugs.

AFE Analog Front-End.

ALU Arithmetic-Logic Unit.

ANN Artificial Neural Network.

ANT Anterior Nucleus of Thalamus.

ARM Advanced RISC Machine.

BCI Brain-Computer Interface.

BPS Bit Per Second.

C.E.R Channel Energy Ratio.

C.S Compressive Sensing.

CISC Complex Instruction Set Computer.

CNN Convolutional Neural Network.

CPU Central Processing Unit.

CWT Continuous Wavelet Transform.

DAC Digital-to-Analog Converter.

DAR Detection stage Activation Ratio.

DBS Deep Brain Stimulation.

DC Direct Current.

DSP Digital Signal Processing.

DWT Discrete Wavelet Transform.

EEG Electroencephalography.

EMD Empirical Mode Decomposition.

FDA Food Drug Administration.

FDP Feature Discriminating Parameter.

FFT Fast Fourier Transform.

FOM Figure-of-merit.

FPGA Field-Programmable Gate Array.

GPR General Purpose Register.

HFS High Frequency Stimulation.

iEEG Intracranial Electroencephalography.

IMD Implantable medical device.

IMFs Intrinsic Mode Functions.

KNN K-Nearest Neighbor.

LBP Local Binary Pattern.

LCF Logical Classification Function.

LFS Low Frequency Stimulation.

LNA Low-Noise Amplifier.

LPF Low-Pass Filter.

LSB Least-Significant Bit.

MCU Micro Controller Unit.

MDMR Maximum Discrimination Minimum Redundancy.

MIPS Microprocessor without Interlocked Pipeline Stages.

PC Program Counter.

PCA Principal Component Analysis.

PF Power Feedback.

PoR Power on Reset.

PSD Power Spectral Density.

RF Random Forest.

RISC Reduced Instruction Set Computer.

RNS Responsive Neurostimulation.

RTL Register-Transfer Level.

SAR Successive-Approximation.

SNR signal-to-noise ratio.

SVM Support Vector Machine.

SWEC Sleep-Wake-Epilepsy-Center.

UART Universal Asynchronous Receiver Transmitter.

VNS Vagus Nerve Stimulation.

1 Introduction

1.1 Epilepsy disorder

Epilepsy is a chronic non-communicable condition that affects the life quality of millions of people around the world. It causes recurrent and unprecedented seizures. Seizures are caused by bursts of electrical activity which temporarily affect the normal performance of the brain. Seizures may contribute to the involuntary movement of the body accompanied by the loss of consciousness, uncontrollable jerking and shaking, losing awareness, becoming stiff, passing out, or passing away [5]. Seizures vary from a brief lapse of attention to prolonged convulsions.

Various types of treatments have already been examined to entirely cure or tranquilize epileptic seizures. The main treatment is considered as using anti-epileptic drugs. Approximately 70% of epileptic patients can be properly treated using the available medications [6]. The remaining 30% of the patients continue to develop drug-resistant epilepsy. Thus, they are subjected to alternative treatments such as 1) removing a small part of the brain that causes seizure events, 2) ketogenic diet, and 3) using Implantable medical device (IMD)s.

IMDs are the intelligent healthcare systems that are attracting significant attention to help patients to overcome neurological disorders such as Epilepsy, Parkinson, Spinal cord injury, etc.

1.2 Brain electrical stimulation treatment for epilepsy

Brain electrical stimulation is a reversible and adjustable therapy for patients who suffer from refractory seizures. A pulse generator delivers current pulses with specific amplitudes to seizures focus via strip and depth electrodes. Strip electrodes are implanted on the cortex space, while, depth electrodes are placed deep into the brain tissue.

In general, brain electrical stimulation is performed by injecting current pulses at regular

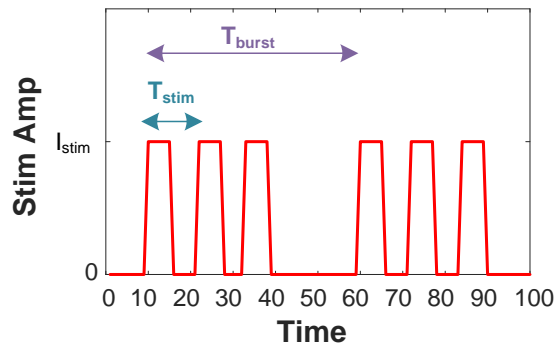


Figure 1.1: Current stimulation waveform example

intervals. Current pulses are categorized into monopolar and bipolar current pulses. In monopolar pulse injection, current pulses are conducted between the pulse generator and one electrode. In bipolar current pulse injection, currents are conducted between two electrodes. It should be noted that the efficacy of brain electrical stimulation mainly relies on stimulation settings, electrode placement structure, seizure focus, and triggering method. A sample current pulse waveform is depicted in Fig. 1.1. Short-term electrical pulses are delivered via electrodes in each stimulation burst. The stimulation amplitude, stimulation period and burst period are shown as I_{stim} , T_{stim} and T_{burst} .

Brain stimulation can contribute to **seizure suppression** and **seizure termination** which are described hereafter [7].

Studies have revealed that brain neuronal activities can be suppressed if the stimulation is conducted in specific stimulation locations under particular stimulation parameters [8]. Seizure suppression may be achieved by applying High Frequency Stimulation (HFS) and Low Frequency Stimulation (LFS). HFS desynchronizes impacts on focal large-scale networks, and it reduces the firing activities of neurons.

LFS has several impacts on neuronal firing activities. It demonstrates synchronization effects on different brain regions. Thus, it may suppress seizures when it targets the entorhinal cortex, amygdalo-hippocampus, and seizure onset zones [9].

All seizures terminate within a few minutes after seizure onsets through an intrinsic neuronal mechanism. During seizure episodes, neurons lose their potassium and other ionic ingredients which lead to seizure termination.

Seizure termination is realized by two methods [7].

1. Anti-epileptic drugs
2. Modulating brain functions by cortical electrical stimulation

Seizure termination mechanisms are explained at molecular and cellular levels. At molecular



Figure 1.2: (a) VNS therapy (b) FDA-approved VNS implant by LivaNova Inc (taken from [1])

level, HFS results in extra potassium accumulation that enhances the ability of neurons to restrain abnormal depolarization and conduction of neurons. At the cellular and network levels, neurostimulation modulates neurons' activities that result in the synchronization and desynchronization of large-scale networks.

1.3 Commercialized IMDs for Epilepsy

IMDs are called intelligent healthcare systems that are attracting significant attention to help patients to overcome neurological disorders such as Epilepsy, Parkinson, Spinal cord injury, etc. IMDs for epilepsy are regarded as a conjunctive treatment for people with refractory epilepsy who are not candidates for brain surgery.

Three methods have already received the approval from U.S. Food Drug Administration (FDA) for epilepsy treatment; 1) Vagus Nerve Stimulation (VNS), 2) Deep Brain Stimulation (DBS), and 3) Responsive Neurostimulation (RNS). The implants deliver electrical stimulation to the area of the brain involved in seizures in open-loop or closed-loop modes. The open-loop devices deliver electrical pulses regardless of the current brain activity. However, closed-loop devices apply electrical stimulation according to an automated seizure detection unit. The details of the currently available implants for epilepsy treatment are given hereafter.

1.3.1 Vagus Nerve Stimulation

The VNS therapy is an open-loop epilepsy control approach that is shown in Fig. 1.2.a. It is a form of treatment for epileptic patients whose seizures cannot be relaxed with currently available medications.

Vagus nerves are a pair of nerves that start in the brain and extend through the entire body. They carry messages between the brain and body. The VNS device by LivaNova Inc is shown in Fig .1.2.b [10]. It consists of a pulse generator, a handheld magnet, and a smartphone application to monitor the device properties. The pulse generator, which is placed under the

skin in the upper chest, sends mild and regular electrical pulses to the brain through the vagus nerve so as to modulate the brain activity that leads to seizures as depicted in Fig. 1.2.a.

The VNS therapy aims to decrease the number, length, and severity of seizures. The effectiveness of the VNS varies from subject to subject. It may reduce the intensity and length of seizures for approximately half of the people living with epilepsy [11]. It may also decrease the recovery time after each seizure event. But, it is unlikely to cancel the seizures completely.

The effects of this therapy do not appear quickly. Indeed, it takes up to two years to demonstrate positive effects on someone's seizures. Furthermore, VNS therapy is used alongside Anti Epileptic Drugs (AED)s. Therefore, it can contribute to reducing the medication dose after two years [11].

VNS therapy is prescribed when AEDs fail to control seizures, and the brain surgery is not acceptable. There are different types of implantable devices for epilepsy treatment and physicians will advise patients on the most suitable device.

The pulse generator is like a heart pacemaker that is implanted during a small operation. It is switched on within four weeks of it being implanted. It is programmed by a neurologist to define the length and amplitude of electrical stimulation. In general cases, it commences with a low level of amplitude which is gradually increased to the desired stimulation level. It is usually set at 30 seconds of stimulation every five minutes. The battery of the pulse generator can last up to ten years. Another similar surgical operation is required to replace the battery when it is drained.

VNS therapy has exhibited different side effects when the nerve is stimulated. Side effects are considered as a discomfort in the throat, a cough, etc. These side effects may not happen for all patients and they may reduce over time without any need to switch off the stimulator.

1.3.2 Deep Brain stimulation

DBS is another open-loop epilepsy treatment that delivers regular impulses to specific brain regions to suppress or terminate seizures as depicted in Fig. 1.3. It is a minimally-invasive surgical therapy using an IMD similar to a cardiac pacemaker. It is considered an add-on treatment for some neurological treatments including epilepsy.

In April 2018, Medtronic DBS therapy was granted U.S. FDA approval. It is proved that Medtronic DBS therapy is able to reduce the frequency of partial-onset seizures of patients 18 years of age and older who are resistant to at least three available epilepsy medications. The approval is given according to the SANTE (Stimulation of Anterior Nucleus of brain in Epilepsy) trial that shows a 75% median frequency reduction of seizures after seven years of implant surgery [2].

During DBS, a pacemaker, which is implanted in the chest, transmits electrical impulses to a deep area of the brain that is called the Anterior Nucleus of Thalamus (ANT) which is part of a

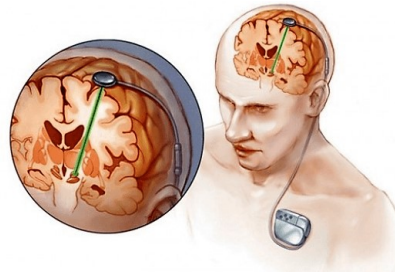


Figure 1.3: DBS therapy by a Medtronic device (taken from [2])

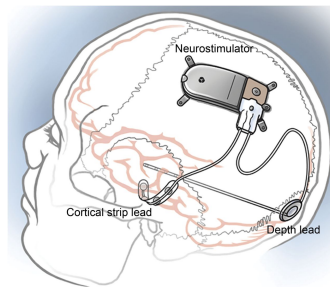


Figure 1.4: Responsive neurostimulation device (Taken from [3])

network involved in seizures. The Medtronic DBS device has been proven to be effective and safe for patients who have six or more seizures per month in the recent three months before surgery. Furthermore, DBS therapy has already been employed for other types of neurological disorders such as essential tremors and Parkinson's disease.

1.3.3 Responsive Neurostimulation

The RNS is considered as a breakthrough surgical approach to treat drug-resistant seizures. The neurostimulator is placed under the scalp within the skull as shown in Figure 1.4. The neurostimulator is connected to two electrodes. The electrodes can be placed on the surface of the brain or into the brain according to the neurologist's decision [3].

The RNS is a closed-loop approach in which the automatic seizure detection is performed by continuous monitoring of the brain's electrical activity. When a seizure-like pattern is detected, the device delivers a small amount of current to the brain. It helps to prevent, stop or shorten the seizures.

Epileptic patients with the following properties are candidates for the RNS.

- Adults with focal epilepsy
- Failing the treatment with at least two seizure medications
- Not candidate for resection surgery

The effectiveness of the RNS has been proved in clinical trials. More than half of the patients had 50% or fewer seizures compared to the presurgical period. The median seizure frequency reduction is reported as follows [3].

- **After a year:** 67% seizure reduction
- **After two years:** 75% seizure reduction
- **Within three to six years:** 82% seizure reduction

It is noteworthy that most of the patients claimed that their quality of life and life autonomy are considerably enhanced after using the RNS.

1.4 EEG/iEEG Signal Processing for Epileptic Seizure Detection

Although promising effects have already been observed by using the three aforementioned FDA-approved IMDs, they cannot cause significant seizure reduction and fast positive effects. The cause of this shortcoming largely refers to the seizure detection units employed in their implantable devices [3]. In the closed-loop brain stimulation, in which electrical stimulation is conducted with respect to learning the brain activity of the patient, the signal processing module plays a significant role in the overall performance of the device. IMDs employ basic seizure detection algorithms which have extremely low-power consumption to detect the onset of seizures. Using basic seizure detection algorithms may affect the overall performance of the device. Hence, a hardware-friendly algorithm is of paramount importance to make a balanced tradeoff between detection performance and power consumption.

Electroencephalography (EEG) is a powerful tool used so as to monitor and detect abnormalities in the human brain such as epileptic seizure. It is the recording of electrical activity in the brain that can be captured from the scalp or cerebral cortex (Intracranial Electroencephalography (iEEG)). EEG recordings reflect the cortical electrical activity. Two main characteristics of EEG signals that are used in digital signal processing modules are given hereunder.

EEG amplitude: The amplitude of EEG is quite low, in the range of microvolts to millivolts. As a consequence, amplification stages are required in recording channels. **EEG frequency:** Human EEG waveform mainly contains a frequency range of below 20 Hz. This frequency range includes delta, theta, alpha, and beta bands. A comparison between different EEG bands is given in Table 1.1 [12].

The iEEG signal of a sample patient from the Bern Inselspital dataset in four aforementioned frequency bands is depicted in Figure. 1.5. It can be observed that EEG signals of delta and theta bands contain the main information of the patient's brain activities. Frequency, voltage amplitude and morphology of EEG signals are widely used to elicit important information to accurately detect seizures [13].

The signal frequency refers to the rhythm of repetitive brain activities. The EEG waveform

Table 1.1: Human EEG bands properties

Band	Frequency(Hz)	Normal condition	Abnormal condition
Delta	< 4	Sleep	Sub-cortical lesion Diffuse lesion
Theta	4-8	Deeply relaxed Inward focused	focal sub-cortical lesion metabolic encephalography
Alpha	8-12	Relaxed Closing eyes	Coma
Beta	12-30	Stressed and anxious Focused	Benzodiazepines

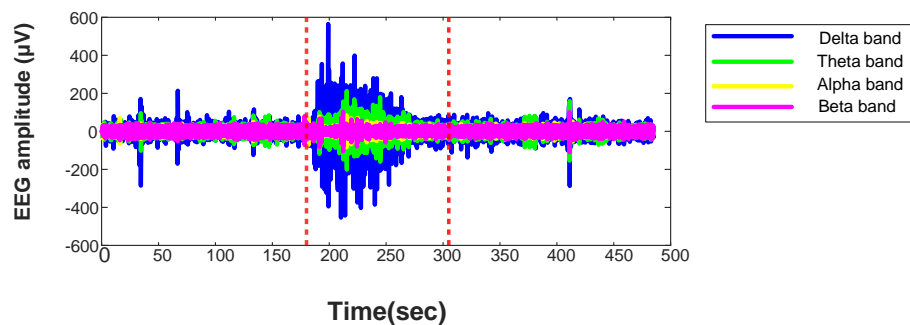


Figure 1.5: iEEG signal of a patient from the SWEC-ETHZ dataset in main EEG frequency bands

demonstrates rhythmic and arrhythmic frequency types. Rhythmic EEG signals are of constant frequency, which is unlikely to occur in epileptic patients. However, an arrhythmic EEG signal does not have a constant frequency and it varies over time.

The voltage amplitude of the EEG signal exhibits the average neuronal activities. The attenuation of EEG activity is tantamount to voltage reduction. It can be done with brain stimulation to block oncoming seizures. In addition, hyper-synchrony of the EEG signal means that there is a sudden increase in voltage amplitude and rhythm of EEG within a specific frequency band. Moreover, during EEG paroxysmal episodes, the EEG signal abruptly reaches a high value and returns to a lower level after a short time. [13].

Another important attribute of an EEG signal is signal morphology which refers to the signal shape. It is classified into monomorphic, polymorphic and transient EEG signals. A monomorphic EEG waveform has a dominant activity with a single frequency like the sinusoidal waveform. Furthermore, a polymorphic signal is composed of multiple frequencies originating from various brain activities. Lastly, a transient signal is an isolated waveform that is distinctly different from a normal background waveform like a short-duration spike.

1.5 Thesis Contribution and Organization

In this research, different signal processing algorithms are investigated to ensure precise epileptic seizure detection in IMDs. Programmability in seizure detection is a novel feature that can contribute to significant performance enhancement of IMDs. In addition, different active charge-balancing techniques are examined to guarantee the safe long-term operation of a closed-loop seizure control implant.

The main contribution of this research consists of proposing various digital signal processing, feature extraction, classification and programmability methods compatible with biomedical implantable devices.

The main challenge of accurate seizure detection is to find the best feature set for each subject. Moreover, the hardware complexity of signal processing algorithms should be taken into account for IMDs. Novel strategies are introduced to make a balanced tradeoff between hardware implementation compatibility and seizure detection accuracy. Several low-complexity time-domain features are studied in the feature pool of the signal processing block. A novel two-stage feature extractor is suggested to release the computation load of digital signal processing during long episodes of non-seizure states. The hardware implementation results proved the superiority of the novel technique over the state-of-the-art in terms of seizure detection parameters and power consumption. Besides, feature extraction in the frequency domain is examined using statistical features and the Discrete Wavelet Transform (DWT) function. The classification of features in the time and frequency domains is performed by hardware-friendly machine learning classifiers.

A significant computation complexity reduction in digital signal processing units is achieved by the proposed feature ranking and channel selection methods. Not only do these methods significantly decrease the computation load of the processor caused by a vast amount of recorded data, but it also improves seizure detection outcomes thanks to the elimination of non-informative data.

Another vital point of an epilepsy control system is to be adjustable over time with respect to patients' conditions evolution. For the first time in the literature, a 32-bit Reduced Instruction Set Computer (RISC) Micro Controller Unit (MCU) is designed in an application-specific manner for an IMD. Different therapy options are programmed on the RISC MCU to give some degree of freedom to patients to adjust the properties of the implant in terms of seizure detection.

Lastly, safe electrical stimulation of the brain so as to suppress or terminate forthcoming seizures are studied in this research. A charge-balancing circuit is an essential unit to ensure safe long-term electrical stimulation of tissue and control the accumulated charge on the electrode-tissue interface. An active charge-balancing method that incorporates anodic pulse modulation and offset current injection by using an ADC in a one-shot manner is proposed in this research.

The remainder of this thesis is organized as follows:

Chapter 2 explains the recent approaches regarding digital signal processing and machine-learning algorithms for biomedical applications. The state-of-the-art is illustrated in detail and the remaining issues and challenges are discussed.

Chapter 3 discusses the modeling of a closed-loop epileptic seizure control implant at system-level for the first time in the literature. All components of a wirelessly-powered seizure control implant are modeled using Simulink software and their critical parameters are studied. A controller unit is implemented in the proposed model to manage the temperature elevation caused by the implant. The model guarantees keeping the temperature rise under 1°C by dynamically adjusting the stimulation parameters.

Chapter 4 iEEG describes hardware implementation of various signal processing algorithms to be used in an implantable epileptic seizure detector. The tradeoff between hardware implementation complexity and seizure detection accuracy is explored in this chapter. Moreover, novel feature selection, channel selection, and computational complexity reduction technique are developed. Novel solutions regarding hardware implementation of machine-learning-based approaches for seizure detection are proposed.

Chapter 5 presents a novel concept of programmability in epileptic seizure detectors. The programmability feature enables constructive interactions between patients, neurologists and implants. The patients can adjust their therapy programs under permission of their neurologists to obtain specific therapeutic targets.

Chapter 6 discusses charge balancing in electrical neurostimulation. A digital charge-balancing processor is developed so as to minimize the power consumption of the charge-balancing system as well as improving the charge-balancing accuracy.

Chapter 7 summarizes the main conclusions of the dissertation and expresses the future directions towards the continuation of this research.

2 State-of-the-art

In this chapter, the recent advances and limitations of digital signal processing and safety of closed-loop IMD will be discussed. A large body of research has already been reported in the literature of signal processing on biomedical signals for wearable and implantable applications. Digital Signal Processing (DSP) approaches are categorized into time-domain, frequency-domain, time/frequency domain, and nonlinear methods. Making a wise compromise between hardware compatibility and algorithms performance is of paramount importance in wearable/implantable applications in which the lifetime of the device battery is directly influenced by the implemented signal processing algorithm [14].

2.1 Epileptic Seizure Detection Background

A large number of signal processing algorithms are already available in the literature of epileptic seizure detection. The most complicated challenge is to choose the optimized number and type of features to be extracted in feature extraction units of seizure detection systems. Furthermore, different kinds of machine-learning classification methods must be analyzed to ascertain a proper classifier in a subject-specific manner.

A typical seizure detection system comprises four main blocks; 1) Pre-processing, 2) Feature extraction, 3) Classification, and 4) Post-processing units, as illustrated in Figure. 2.1.

The pre-processing block is responsible for increasing the signal-to-noise ratio (SNR) of the input signal in conjunction with decreasing the computation cost for succeeding blocks of a seizure detector. Different filtering and compressive sensing techniques have been investigated to perform pre-processing tasks on biomedical signals. The second block is called feature extraction which mainly conducts signal processing algorithms in different domains. Statistical features, spectral entropy, and approximate entropy are extracted using time-domain signal processing techniques. Feature extraction in the frequency domain involves studying signal energy and power spectral densities in different frequency bands. To discriminate between non-ictal and ictal brain states of epileptic patients according to extracted features, thresholding and machine-learning classification techniques should be

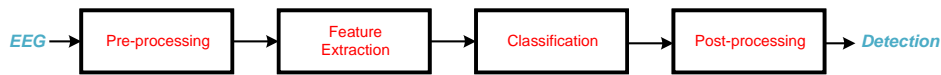


Figure 2.1: Seizure detection system block diagram

employed. [13]. Furthermore, the last block of a seizure detection system is a post-processing unit that aims to remove noise as well as smoothes classification outputs. The recently published papers, which focused on different units of seizure detection systems, are briefly introduced in the following.

2.1.1 Pre-processing Techniques Background

The pre-processing unit aims to remove input noise from recorded EEG and iEEG signals. Moreover, input dimension reduction is executed in this unit.

Input dimension reduction is achieved by compressing the large amount of input data acquired through tens of electrodes. The compressed channels may be an average of all electrode channels, a random sum of all channels or the output of common spatial filters [15, 16]. Input dimension reduction and electrode channel selection is highly beneficial when it comes to SNR improvement as well as computation complexity reduction for real-time low-power applications [17].

[18] improves computation efficiency by employing an automatic channel selection engine that consists of a supervised classifier. The extracted time and frequency domain features are fed to a Random Forest (RF) classifier to benefit from redundant data filtering, processing time reduction, and computation load reduction. It should be noted that [18] suffers from low sensitivity and high false alarm rates.

The Wavelet transform, Fourier transform, Notch filtering, Butterworth filtering, and empirical mode decomposition are regarded as common pre-processing techniques for noise removal from input signals [19, 20]. Noise reduction using different filters, Wavelet transform and Fourier transform may remarkably enhance the SNR of EEG signals which has a direct influence on seizure detection performed in the following blocks of the system.

Wavelets are small, localized, and oscillatory functions that contain the localized information of signals in both time and frequency domains. Wavelet transform is divided into two groups including Continuous Wavelet Transform (CWT) and DWT. The concept of noise removal by this method is to decompose signals into different frequency bands. Subsequently, a threshold is applied to the coefficients of different bands. Finally, the filtered signal is re-constructed using inverse wavelet transform.

In empirical mode decomposition, the signal is decomposed into finite numbers of Intrinsic Mode Functions (IMFs) to obtain noise reduction. IMFs are oscillatory functions that are defined to satisfy these two conditions.

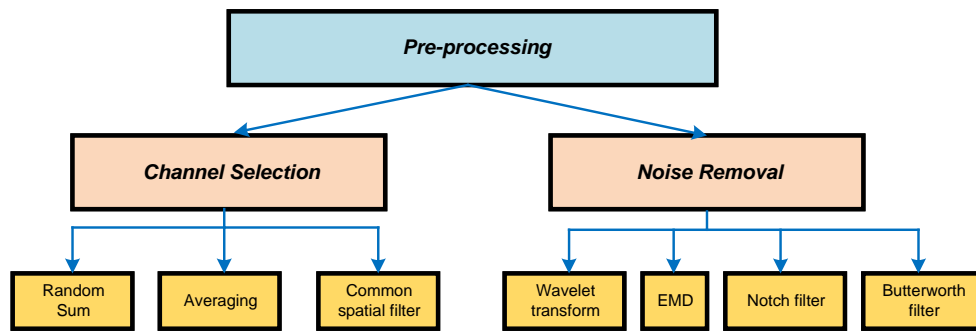


Figure 2.2: Pre-processing techniques chart

1. The number of extrema must be equal or differ at most one from the number of zero crossings in IMFs
2. At each point, the mean value of the envelope formed by the local maxima, and the mean value of the envelope formed by the local minima must be zero

Satisfying these criteria ensures that each IMF represents the oscillatory components within signals [21]. To enable filtering using Empirical mode decomposition, thresholds are applied to IMFs of the decomposed signal. Then, signal reconstruction is performed using filtered IMFs.

Band-pass filters such as Notch and Butterworth filters are implemented to remove dc noises from EEG/iEEG signals as well as limit the frequency band of interest. It is noteworthy that EEG signals have low-frequency characteristics in which the informative data is located in frequencies lower than 200Hz . The filter order and cutoff frequency are two major parameters that should be optimized in the design.

The summary of different pre-processing techniques is depicted in Figure. 2.2.

2.1.2 Feature Extraction Background

Recent advances in biomedical signal processing in time and frequency domains are described in the following.

[19] and [22] employs frequency domain techniques on the scalp and intracranial EEG signals, respectively. The results reveal that extracting features in the frequency domain contributes to greater performance using scalp EEG compared to iEEG.

The DWT is a powerful tool to examine signals in the time-frequency domain. Authors in [23] extract simple statistical features from DWT coefficients of EEG signals. The extracted features are given to a K-Nearest Neighbor (KNN) classifier. Some challenges are not addressed in this work such as memory constraints involving the implementation of KNN on hardware as well

as the selection of an optimized frequency band to reduce the classifier input dimension.

[24] exploits spectral features to predict forthcoming seizures from EEG and iEEG signals. It uses Fast Fourier Transform (FFT) to reduce the computation complexity compared to the state-of-the-art. It extracts spectral powers and their ratios in eight frequency bands including $\theta(4-8\text{ Hz})$, $\alpha(8-12\text{ Hz})$, $\beta(12-30\text{ Hz})$, $\gamma_1(30-50\text{ Hz})$, $\gamma_2(50-70\text{ Hz})$, $\gamma_3(70-90\text{ Hz})$, $\gamma_4(90-110\text{ Hz})$, $\gamma_5(110-128\text{ Hz})$ bands. Then, a subset of features is selected in a two-step manner using scatter matrix and branch & bound techniques. The drawback of this method relates to applying the FFT on EEG signals which are not a stationary waveform. In addition, FFT calculation requires more energy consumption compared to typical time-domain feature extraction techniques. Although the author declared achieving high sensitivity and low false positive detection rates, the detection delay is not reported which plays a pivotal part in seizure detection performance.

[25] includes both time-domain and frequency-domain features in its feature pool. Eleven mixed features are extracted based on auto-correlation features in the time domain, and spectral powers in the frequency domain. The classification of the features is carried out by an RF classifier. It obtains a relatively low seizure detection delay tested on EEG databases of Freiburg University Hospital. However, this algorithm lacks patient specificity and hardware implementation. Furthermore, the RF classifier used in this work is not optimized for implantable applications in terms of memory and logic constraints.

Plus, time-domain features are examined in [20], [26], [25], and [27]. Statistical time-domain features work well on both scalp and intracranial EEG signals. It should be noted that low-complexity time-domain features are highly practical only in the case that a patient-specific approach has been employed. Lacking patient specificity is a major disadvantage of the aforesaid papers.

Hjorth parameters are another time-domain features that include mobility and complexity metrics that are given in (2.1) and (2.2).

$$Mobility = \sqrt{\frac{Var(\frac{dX}{dt})}{Var(X)}} \quad (2.1)$$

$$Complexity = \sqrt{\frac{mobility(\frac{dX}{dt})}{mobility(X)}} \quad (2.2)$$

Where X is the input signal and Var is the variance function. The Mobility represents the pace of signal fluctuation; while complexity illustrates signal irregularities.

Authors in [28] utilize another aspect of time-domain feature extraction called symbolization. Time-domain iEEG signals are converted into a bit string that is called Local Binary Pattern (LBP). The LBP reflects the relational aspect between iEEG consecutive samples. The LBP of each sample is obtained with respect to the sign of temporal difference of the adjacent sample. It is worth noting that the LBP of length L is formed by concatenating the LBP of each sample with the bits of successive $L - 1$ samples [29]. [28] exhibits that LBPs are well-distributed over all possible codes during non-ictal states. Conversely, many possible LBP codes are missing during seizure occurrences, and a single LBP serves as a predominant code in the patient's histogram. As a result, the LBP symbolization method may be regarded as a useful tool for seizure detection. Although this method obtained high seizure detection performance for the majority of the tested patients, it demonstrates unacceptable seizure detection results on some specific patients since it relies only on a single feature. In addition, classification is performed using a Hyperdimensional computing technique that is not proven to be suitable for hardware implementation.

Authors in [30] try to reduce the dimension of the features in a patient-customized manner to not only reduce the response time, but also the power consumption of the system. They include time, frequency, time-frequency, and nonlinear features in the feature pool. Two nonlinear features including *Sample Entropy* and *Lyapunov Exponent* are extracted on the grounds that the EEG signal has been proven to have nonlinear dynamic characteristics. Subsequently, the features are ranked based on the minimum redundancy, maximum relevance approach. A Support Vector Machine (SVM) classifier discriminates between seizure and seizure-free states with 98.3% accuracy. Although this algorithm reaches a very low feature dimension of 1 and high detection accuracy, it still needs some improvements to deal with EEG signals captured by several electrodes.

Furthermore, [31] worked on feature and channel selection with a feature pool that is made up of uni-variant and bi-variant features. In bi-variant feature extraction, a narrow frequency band is selected for each patient for phase extraction. It demonstrates $\times 4.6$ dimension reduction to be compatible with implementation on low-power microprocessors.

[32] attempts to achieve significant dimension reduction using both channel selection and feature reduction. The authors extracted all spectral features from each channel and fed them to an RF classifier. Afterward, channel selection is carried out based on the number of times each channel contributes to the forest. In addition, the feature space is also mapped into a smaller space to reduce the overwhelming number of spectral features extracted from the selected channels. The feature mapping is performed according to t-distributed stochastic neighbor embedding which is a nonlinear dimension reduction technique [33].

2.2 Classification Background

Machine-learning-based classifiers are widely employed in various signal processing tasks including epileptic seizure detection. Particularly, the SVM, Convolutional Neural Network

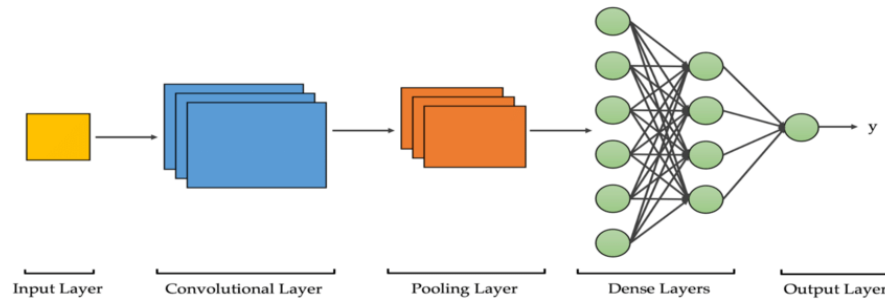


Figure 2.3: CNN architecture

(CNN), KNN, Artificial Neural Network (ANN), and RF classifiers have been commonly used in the literature of epilepsy analysis [34–36].

CNN is a powerful machine learning method for classification tasks with embedded feature extraction. The main attribute of a CNN classifier belongs to its convolutional layers which apply small filter kernels to input data to extract various features.

CNN is employed in [20, 37], and tested on scalp EEG signals. In addition, authors in [38] divide the iEEG signals into a binary detection group using a CNN. The figures demonstrate that the performance of CNNs on iEEG outweighs that of scalp EEG.

The architecture of a CNN classifier is illustrated in Figure. 2.3. A CNN has exhibited promising results in the seizure detection field due to its capability to extract patterns and features from raw EEG signals used for seizure detection. It consists of convolutional, pooling, and fully-connected layers. Different features are extracted in convolutional layers. The pooling layers are used for down sampling, and fully-connected layers are in charge of classification. The Early layers of a CNN extract simple features like spikes; while the deeper layers can capture more complicated features. Since a CNN is a deep-learning classification method, it demands several hours of EEG recording labels during the training phase.

It is notable to mention that the CNN weights and biases are optimized in the training phase through forward propagation. Then, the difference between predicted and actual labels is calculated and optimized using the back propagation techniques. The challenging point of using CNNs in an IMDs is the lack of balanced labels in available databases and the limitations regarding its hardware implementation.

A SVM classifier is another frequently used classifier that has already been examined on both scalp and intracranial EEG. A SVM is a supervised classification method used for binary classification. SVM is effective in high-dimensional feature spaces. It aims to maximize the margin between different classes of data. The margin is defined as the distance between the nearest data of each class and the hyperplane. This method is powerful tool in creating a robust classification boundary.

SVM classification can be effectively applied to non-stationary signals like EEG. Furthermore,

the SVM operates with approximately similar accuracy on both EEG and iEEG signals [39]. [40] employs radial-basis kernel SVMs with two feature types namely subpattern-based PCA and cross subpattern correlation-based Principal Component Analysis (PCA). [30, 41] use SVM classifiers connected to their feature extraction units. However, their seizure detection delays need to be improved for real-time applications.

[42] utilizes four frequently used machine learning-based classifiers including SVM, KNN, ANN, and Naive Bayes classifiers. The figures prove that the ANN contributes to the highest classification accuracy when 54-DWT wavelets are used for the feature extraction of predictors.

[43] expresses that the level of decomposition using 54-DWT wavelets plays a significant role in classification accuracy using SVM classifiers. [44] extracts statistical features from DWT coefficients. Moreover, KNN and Naive Bayes classifiers are used for classification tasks. The superiority of Naive Bayes classifiers has been shown in comparison with KNN classifiers.

Schematic diagrams of SVM, KNN, and ANN classifiers are depicted in Figure. 2.4. SVM classifier is made up of different weights and a bias value. It exhibits a robust performance in using a massive number of predictors and few training samples. Implementation of the SVM classifier is depicted in Figure. 2.4.a

The schematic of a KNN classifier is illustrated in Figure. 2.4.b. It is known as a non-parameteric, non-linear classifier. It works well when the training dataset is large. A KNN classifier follows an instance-based learning in which the model memorizes the entire training dataset instead of learning an explicit model during the training. In addition, KNN performs classification according to the majority voting among the K-nearest object available in the training dataset. Values of K may vary from three to ten in different articles. The main drawback of KNN classification is its memory-intensive architecture.

An ANN classifier consists of neurons and weights. Neurons form three layers; Input layer, hidden layer, and output layer as shown in Figure. 2.4.c. Each node in a layer is connected to multiple nodes of subsequent layers which forms a network of interconnected nodes. Hidden layers are in charge of feature extraction and the output layer generates class labels. ANNs have several hyperparameters such as number of layers, number of neurons, learning rate, etc. Fine tuning of this parameters are crucial to achieve an optimized design.

Recently, deep learning approaches are trying to target the seizure detection problem [45]. Authors in [46] extract spectral-domain features using FFT. A deep neural network based on multi-layer perceptrons are used to classify ictal and non-ictal states. It achieves 95% F_1 measure. Deep neural networks are highly beneficial to learn complex EEG patterns on the grounds that a clear mathematical model cannot be assigned to EEG patterns. The main shortcoming of deep learning techniques is that they require a large and balanced dataset to train the model. However, iEEG signals are extremely asymmetric and the ratio of non-ictal states to ictal states are quite large.

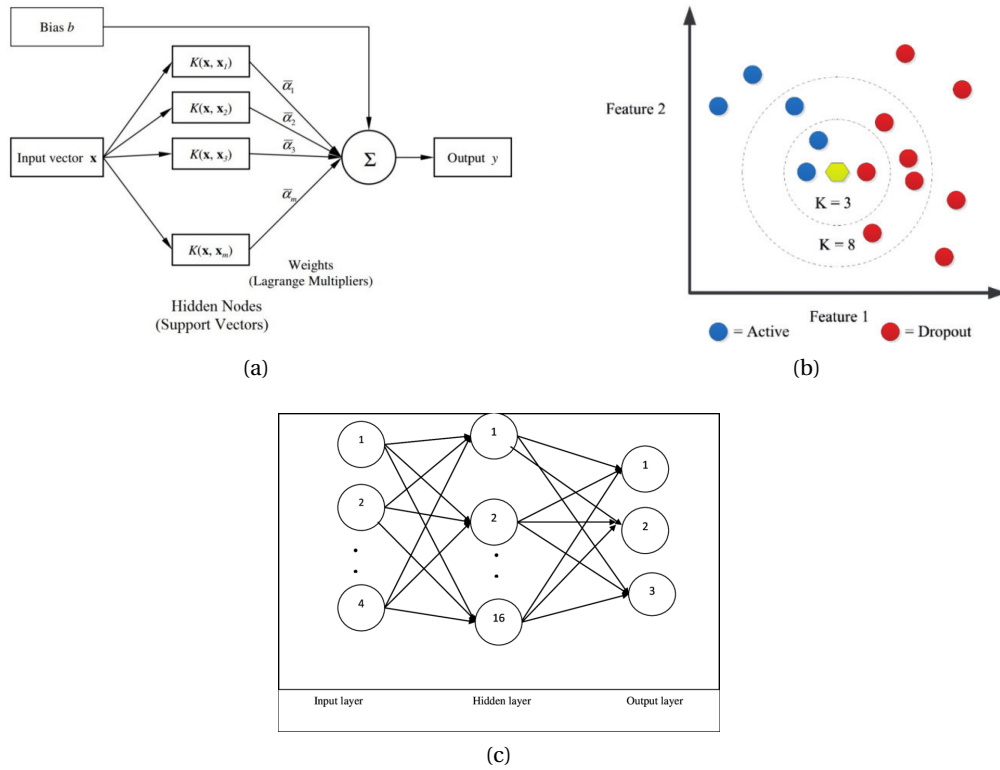


Figure 2.4: Architecture of the (a) SVM, (b) KNN, and (c) ANN classifiers

2.2.1 Post-Processing Background

Post-processing techniques are used in applications where the number of false positive detections must be maintained as low as possible [47]. Various methods have already been explored such as Poisson process random predictors [48], Kalman filters [49], and moving average filters [50].

In Kalman filtering, the history of classification is taken into account to reduce the effect of inconsistent classification output as well as unwanted output fluctuations that result in false detections. Prediction and measurement steps are the two main steps in the Kalman filtering technique. The Kalman gain is determined iteratively to make a relative importance between the prediction and the measurement steps of filtering.

In the moving average technique, the window size defines the number of data points that participate in the moving average calculation. This is typically an odd number to generate a symmetric distribution around the desired data point. Subsequently, the window will slide from the beginning to the end of the sequence, and the filtered signal is the average value of the data that are located inside the window of each data point.

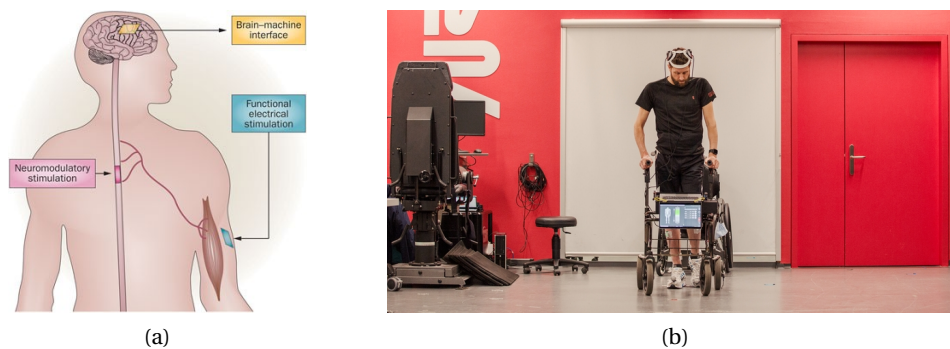


Figure 2.5: (a) Brain-computer interface, (b) a treated patient in Switzerland (taken from [4])

2.3 Electrical Stimulation and Charge Balancing Background

Closed-loop IMDs like the RNS require a safe electrical stimulator to deliver pulses upon seizure prediction or detection. Implantable neural stimulators are currently in use by many patients not only to treat neurological disorders such as Epilepsy, Parkinson and Alzheimer's diseases but also to restore paralyzed body functions. For instance, VNS is used for epilepsy, DBS for Parkinson, and functional electrical stimulation for body movement issues. Moreover, human sensory systems such as vision and auditory systems can be improved or restored by retinal and cochlear implants which apply electrical neural stimulation [51].

Brain-Computer Interface (BCI) devices have shown a striking potential to restore human motor functions [52]. The BCI establishes a constant link between movement intentions and the spinal cord to restore human mobility in a natural way shown in Figure. 2.5.a. Researchers in Switzerland have developed a wireless link between the brain and spinal cord to transform thoughts into motor actions which enables a patient to walk autonomously after spinal cord injury thanks to a link that is called the digital bridge depicted in Figure. 2.5.b. The digital bridge comprises two implants that are placed in the regions of the brain and spinal cord which control legs movements. It involves signal processing of EEG signals to decode movement intentions using adaptive artificial intelligence techniques. Another encouraging outcome is that remarkable sensory perception and motor skills are observed in the patients after switching off the digital bridge. It means that new neuronal pathways are generated in the patient's body after implanting the digital bridge [4].

Three sorts of neurostimulation are voltage-mode, current-mode, and charge-mode electrical stimulation. It should be noted that current-mode electrical stimulators enable better charge control over the other techniques since they operate relatively independent from electrode-tissue interface impedance variation. Moreover, current-mode electrical stimulation needs to cope with high voltage compliance requirements.

An important hurdle in neurostimulation is charge imbalances that are occurred on the electrode-tissue interface. It is worth noting that even remarkably accurate biphasic current

pulses cannot prevent residual potentials [53]. Charge imbalances may cause irreversible damage to both nerve tissues and implanted electrodes over long-term neurostimulation. In addition, the existence of residual potential may lead to the continuation of oxidation/reduction chemical reactions even after neurostimulation. Therefore, all neurostimulators must be accompanied by a safe charge-balancing circuit to persistently monitor the electrode potential.

Charge-balancing techniques are categorized into active and passive systems. While the charge balancing occurred according to the amount of residual potential in active charge-balancing systems, imbalances are canceled intermittently regardless of the interface potential in passive charge-balancing systems. The type of charge balancing technique strongly relies on the output current driver of the neurostimulator. Monopolar and bipolar output current drivers are used in the literature based on the stimulation site and purpose of stimulation. For example, in cochlear and retinal implants, microelectrode arrays, which contain several electrode channels, are utilized with monopolar output current driver. Thus, passive charge balancing techniques cannot be used due to stringent area requirements. However, passive charge balancing techniques are compatible with systems that use one or a few electrodes with bipolar output current drivers such the DBS used for Parkinson's disease.

[53] proposes a 24-channel charge-balanced neurostimulator employing preventive-detective charge-balancing control loops. In addition, Safe and unsafe thresholds are dynamically programmable to maintain the charge-balancing speed and precision under control. It incorporates a four-level comparator circuit to unravel a compromise between safety and power consumption. It also applies push/pull current pulse injection and anodic pulse modulation based on its detective and preventive control loops, consecutively.

A typical and simple charge-balancing method uses an AC-coupling capacitor in series with stimulation electrodes. It is capable of blocking unintended charge transfer to the interface during interpulse intervals. However, this method obligates a considerable voltage headroom for the stimulator current driver. This requirement contributes to employing a large off-chip capacitor or remarkably limiting the amplitude of stimulation currents [54].

A passive on-chip solution that is widely used in the literature is called electrode shorting which takes place after each biphasic stimulation phase before arriving subsequent pulses that is depicted in Figure. 2.6 [55–57]. A notable shortcoming of this method is the lack of control over the discharge rate when the electrodes are connected to a reference voltage. considering a fast discharge rate, a large discharge current depolarizes the cell membrane and prompts undesired action potential. The fast discharge rate takes place when the tissue impedance is too low. On the other hand, a slow discharge rate obliges to prolong the stimulation period which limits the maximum stimulation frequency. When the tissue impedance is large, a slow discharge rate occurs in which the entire residual charge is not released within a short interpulse delay.

Thus, some researchers have already attempted to integrate electrode shorting techniques

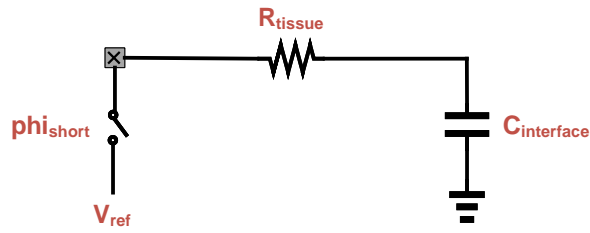
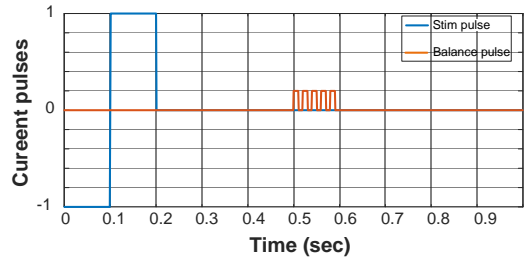
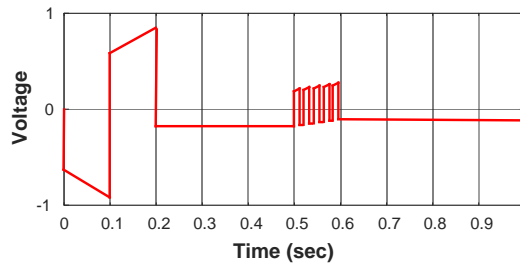


Figure 2.6: Simplified schematic of electrode shorting



(a)



(b)

Figure 2.7: (a) Current profile, and (b) voltage profile of charge-balanced current-mode stimulation

with some other approaches such as dynamic stimulation current matching [56, 58]. In these cases, only a proportion of residual potential is neutralized by electrode shorting without exposing brain tissues to possible damage risks.

Recently, active charge-balancing techniques are widely used in charge-balanced neurostimulators [59–62]. They responsively injected trains of pulses to a continuous measurement of electrodes’ residual potentials illustrated in Figure. 2.7. It is shown that the residual potential stays in an unsafe region. Thus, a train of high-frequency low-amplitude pulses are injected to return the residual potential within a safe range.

The polarity of the measured residual potential defines cathodic or anodic pulses to be injected during neutralization process. The imperfection of this method is the risk of unintended stimulation caused by charge-balancing pulses.

It is of paramount importance to select an appropriate threshold voltage in neurostimulation

applications. an appropriate threshold voltage should be a few times lower than the water oxidation/reduction voltage window [53]. [63, 64] consider common safe residual potential windows of 50 mV and 100 mV [63, 64].

Charge balancing circuits involve the safety-power dissipation tradeoff which is a quite challenging point in the design of an implantable neurostimulator. In other words, if the safe-region threshold is chosen very close to the reference voltage of electrodes, the charge-balancing system would be over-sensitive which leads to greater power consumption. On the contrary, a relaxed residual potential threshold may result in a higher risk of tissue and electrode damage. Consequently, [53] suggests a programmable threshold selection to fit different application requirements and electrodes' specifications. For instance, according to European standards, the maximum allowed DC-current leakage is 100 nA which translates to a few millivolts of residual potential thresholds [65].

The way of managing persistent imbalances is regarded as another important challenge needed to be addressed in this domain. Persistent imbalances are accumulated on electrodes after each stimulation phase. As a consequence, the long interpulse resting time is required to entirely cancel imbalances. Furthermore, the trains of pulses during interpulse delays may degrade the neurostimulation effectiveness in the long run.

Besides, adjusting the amplitude of anodic and cathodic pulses in the following stimulation phase according to the measured residual potential is regarded as another effective charge-balancing technique widely used in the literature [51, 66]. However, pulse amplitude modulation using analog techniques deals with imperfections such as using many off-chip components, dependency to Digital-to-Analog Converter (DAC) resolution, and the maximum stimulation current.

[67] employs a simple digital circuit consisting of D-latches, subtractors and comparators to responsively neutralize charge imbalances on electrodes. The charge neutralization is carried out in a current-mode electrical stimulator with an active charge balancing technique. Since cathodic pulses generate an action potential in the tissue, modification of cathodic pulse amplitude may affect the therapeutic goals [68]. Thus, anodic pulse modulation is conducted in [51] and [67].

Figure. 2.8 illustrates the anodic pulse modulation procedure. According to the voltage waveform shown in Figure. 2.8.a, the residual voltage with negative polarity occurs after the first stimulation phase. To compensate the charge imbalances with negative polarity, the amplitude of the anodic pulse is increased in the following stimulation phase as depicted in Figure. 2.8.b.

A circuit-level implementation of active charge balancing anodic pulse modulation is demonstrated in Figure. 2.9. The cathodic pulse amplitude is always kept constant in the anodic pulse modulation technique. During the cathodic phase, M_6 and M_8 conduct and current flows from E_1 to E_2 . In this case, SW_1 is off and SW_2 is on.

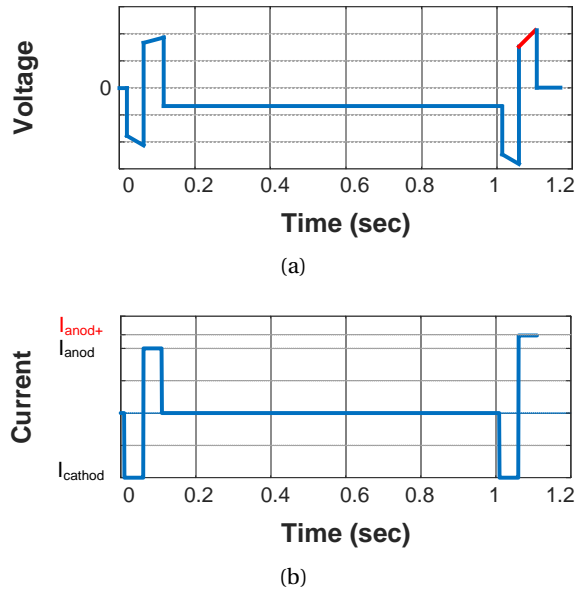


Figure 2.8: (a) Residual voltage ,and (b) Charge balancing current pulses

Anodic pulses flow from E_2 to E_1 when M_5 and M_7 conduct. If the residual potential polarity is positive, the amplitude of the anodic pulse in the subsequent stimulation phase should be reduced. Therefore, both switches will be turned off by control signals. With negative residual voltage polarity, the amplitude of anodic pulse is increased in the next phase. Hence, SW_1 and SW_2 are turned on and off, respectively.

The majority of charge balancing techniques carry out an iterative approach of modification to reach charge neutrality. [69] suggest a non-iterative charge balancing method based on real-time interface impedance estimations which guarantees no unwanted action potential generation. In conventional closed-loop charge imbalance cancellation methods, the charge balancer is activated when the electrode voltage exceeds a safe threshold. It dictates the continuous operation of an Analog-to-Digital Converter (ADC) that significantly increases the power consumption.

Translating the residual voltage to its equivalent charge requires interface impedance calculation that varies over time. [69] calculates interface impedance and adjusts the cathodic pulse width to cancel charge imbalances.

2.4 Summary and Conclusions

In this chapter, we have discussed the recent advances in closed-loop seizure control systems. These systems consist of various blocks in analog and digital domains. The focus of this chapter was on the advances in signal processing and neurostimulation techniques used in IMDs.

The last section of this chapter has explained the application of BCI devices to improve the quality of life of patients who suffer from neural and motor deficits by applying neurostimulation. Although different sorts of charge-balancing techniques have already been employed in the state-of-the-art, establishing a balanced tradeoff between safety, accuracy, and power consumption of charge balancers is still an open point. In this dissertation, we aim of suggesting a novel solution to strike a balanced tradeoff between the aforementioned points.

3 System-Level Overview on Epilepsy IMDs

3.1 Introduction and Motivations

In this chapter, all components of a closed-loop epilepsy control implant are introduced and modeled at the system level using Simulink software. The implant operates to suppress upcoming seizures by applying multi-channel electrical stimulation to the cortical area of patients.

The main motivation behind the system-level analysis and modeling of an epilepsy control implant is to demonstrate the main specifications of each component and the goals that we aim to achieve in the new design.

The System-level analysis of the implant is executed in four steps which are given in the following.

1. Modeling the essential parameters of each component
2. Defining the requirements and goals of the device
3. Extracting the adjustable parameter
4. Modifying the adjustable parameters to obtain a specific goal

An excellent closed-loop epilepsy control IMD should satisfy several standards and exhibit many properties such as low-noise high-resolution iEEG signal recording, accurate seizure detection with minimum delay, low power consumption, low area occupation, etc [70, 71].

The lifetime of an IMD is a significant property of the device that should be optimized as much as possible. Nowadays, commercial IMDs for epilepsy last between five to eight years [2, 10]. Thus, extra brain surgeries are still required which may endanger the health of the patients as well as impose hospitalization and excessive surgery costs. As a consequence, many patients who suffer from intractable epilepsy are still reluctant to accept this technology to improve

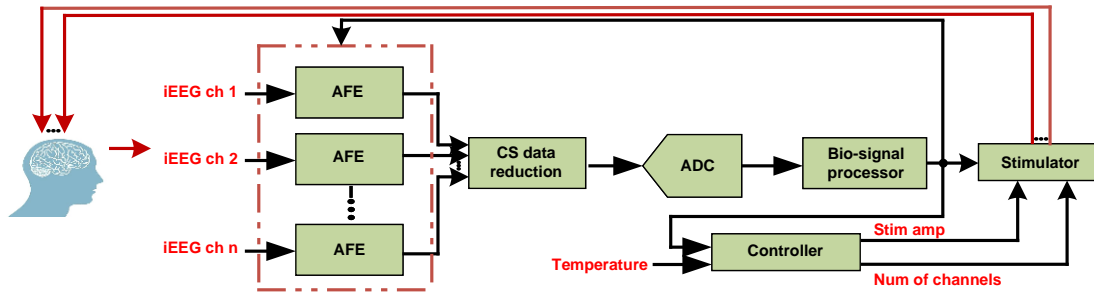


Figure 3.1: Block diagram of a closed-loop epilepsy control system

their life autonomy.

It is of paramount importance to design all components of an epilepsy control system in an energy-efficient mode to extend the life span of the device. Another challenging constraint is the maximum power budget that can be transferred through wireless power transmission systems. It should be noted that inductive links are commonly used in the literature of wireless power and data transmission of IMDs [71, 72].

Another important aspect of an IMD that is implanted in the cerebral cortex is the temperature elevation of the implant region caused by the power consumption of the implant. The temperature rise up to 1°C is generally accepted in the domain of cortical implants [70, 71]. Thus, the modification of different stimulation parameters is studied in this chapter to handle unwanted temperature rise of the brain which can jeopardize patients' lives.

A typical closed-loop epilepsy control system with wireless power and data transmission modules is made of several units that are shown in Figure. 3.1 and Figure. 3.2, respectively. The responsive epileptic seizure detection and suppression system is composed of several Analog Front-End (AFE) channels, a compressive data reduction system, an ADC, a biomedical signal processor, a controller, and several stimulation channels.

Moreover, the wireless power and data communication modules consist of an inductive link, ASK modulators, ASK demodulators, a rectifier, power control feedbacks, and a voltage regulator. The specifications of each unit are described in the following.

3.2 iEEG recording channels

The recording channels of the epilepsy control device consist of several AFEs, a Compressive Sensing (C.S) data reduction unit, and an ADC. The AFE of each channel is made of a Low-Noise Amplifier (LNA), a low-pass filter, a gain stage, and a sample & hold block shown in Figure. 3.3. The AFE has three main roles that are mentioned hereunder.

1. Amplification of weak neural signals

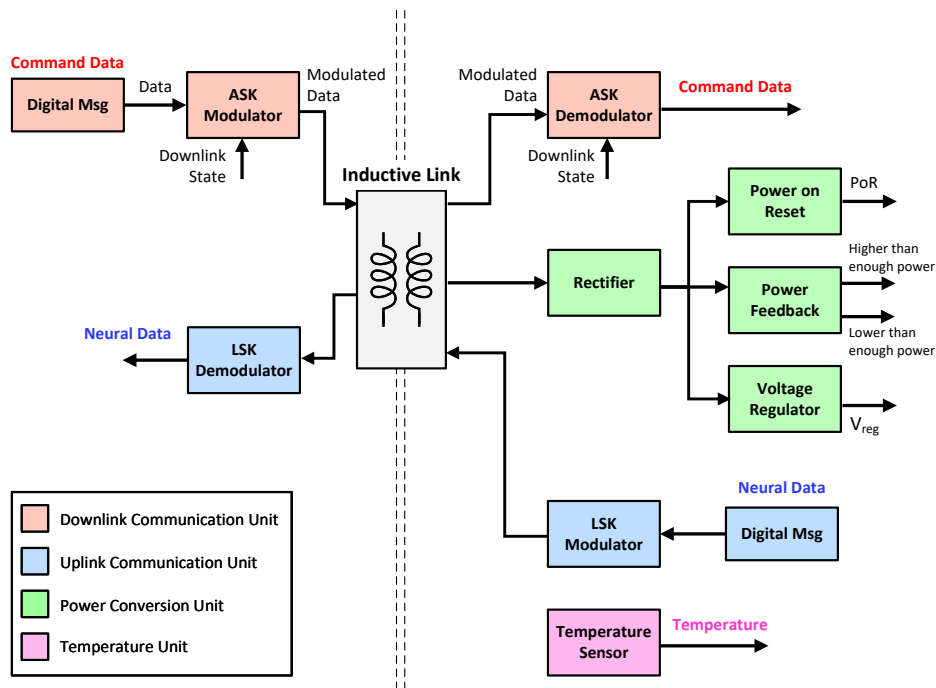


Figure 3.2: Block diagram of the wireless power and data transmission system

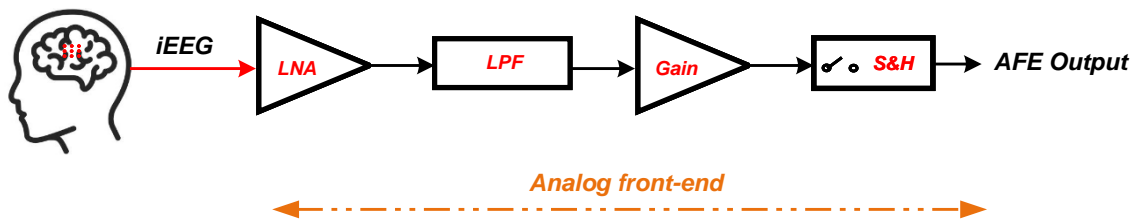


Figure 3.3: Elements of the AFE unit

2. limiting the frequency band to the band-of-interest
3. Rejecting the large DC offset

The first block of an AFE is the LNA. It amplifies the input iEEG signal within its pass-band frequency. Typical LNAs used in the state-of-the-art demonstrate the pass-band frequency of 10 Hz – 144 kHz. In addition, the typical LNA gain for the iEEG amplification is reported between 30 dB to 35 dB [71].

The LNA is modeled in Simulink using a transfer function and a gain block. The transfer function is used to imitate the band-pass characteristic of the LNA. The transfer function of a Butterworth band-pass filter is employed to enable the band-pass filtering of the LNA and the frequency response is shown in Figure. 3.4 . Furthermore, a gain block with the amplification value of 31.62 is utilized to provide an amplification of 30 dB for the LNA in Simulink which is compatible with the state-of-the-art LNA characteristics [28].

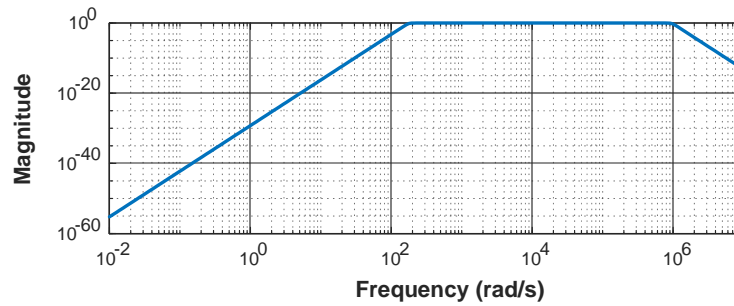
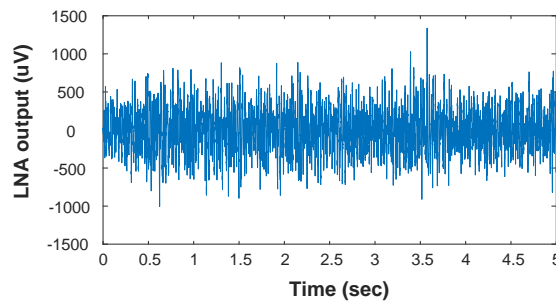
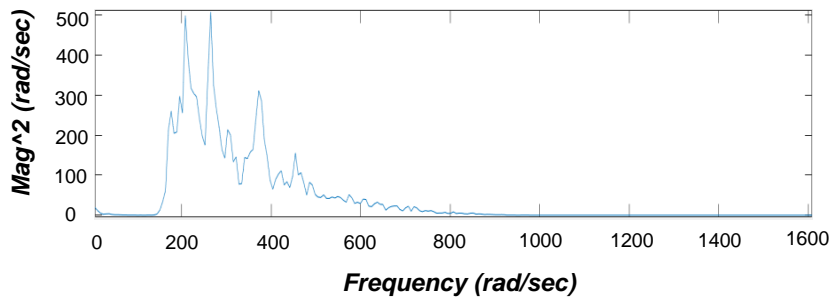


Figure 3.4: Frequency response of the LNA



(a)



(b)

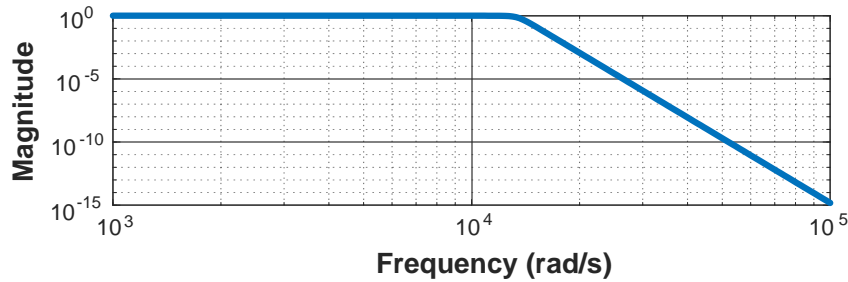
Figure 3.5: (a) LNA output in time domain, and (b) LNA output PSD

Figure 3.5.a illustrates the LNA output in the time domain. The iEEG data of a sample patient from the Bern University Hospital dataset is used for the simulation [73]. Moreover, the Power Spectral Density (PSD) of LNA output is shown in Figure 3.5.b., respectively. Figure 3.5 evidences that the LNA successfully rejects the large DC offset and amplifies the EEG in the frequency band of interest.

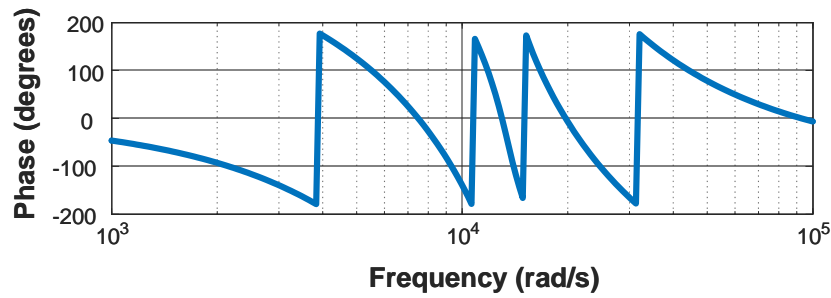
The next element of the AFE is a Low-Pass Filter (LPF) to limit the high cutoff frequency of the recorded iEEG. It offers many advantages thanks to the low-frequency inherent of the iEEG which has frequency components lower than 2 kHz [70, 71]. An analog Butterworth filter is designed to be included in the Simulink model. The properties of the filter are given in Table 3.1.

Table 3.1: Low-pass filter parameters

Filter type	Pass-band frequency	Stop-band frequency
Analog Butterworth	2 kHz	3 kHz
Filter order	Pass-band ripple	Stop-band ripple
17 th	0.5	50



(a)



(b)

Figure 3.6: (a) Magnitude response, and (b) Phase response of the LPF

The amplitude and phase plots of the designed Butterworth low-pass filter that are used in the Simulink is demonstrated in Figure. 3.6.

The LPF is followed by a gain stage shown in Figure. 3.3. the gain stage plays a decisive role in the AFE since the iEEG amplitude is extremely, low in the range of tens of microvolts. Therefore, an amplification of around 45 dB is required to strengthen the signal level to drive the following stages of the system. As previously mentioned, this amount of amplification cannot be fulfilled by the LNA stage because of noise requirements. Thus, the gain stage offers a 20 dB additional amplification that is implemented in Simulink.

The last element of the AFE unit is a sample & hold block. This block is essential in multi-channel recording IMDs since the output of each recording channel must be kept constant during the specific number of measurement cycles that is defined by the M parameter. The M parameter is defined in (3.1).

$$M = \frac{\text{Num of Total Electrode Channels}}{CR} \quad (3.1)$$

where the CR represents the compression ratio that is given in (3.2).

$$CR = \frac{\text{Num of Total Electrode Channels}}{\text{Num of Selected Channels}} \quad (3.2)$$

The EEG signals recorded from different channels are delivered to the compressive sensing data reduction block. 12 recording channels are included in this design and a maximum compression scenario is considered which results in a compression ratio equal to 12. The role of this unit is to reduce the dimension of the signal delivered to the ADC of the implant. Simulink implementation of the compressive sensing unit is executed using switches that are controlled by random binary number generators. It is important to mention that data dimension reduction offers several advantages that are described hereunder.

- Using a fewer number of ADCs
- Area and power consumption saving
- Computation cost reduction in the digital signal processing unit

An ADC is employed in the final stage of the iEEG recording system. The resolution and sampling frequency of the ADC are dictated by the number of bits used in the computation blocks of the digital signal processor. A 16-bit Successive-Approximation (SAR) ADC is frequently used in the literature [27]. The ADC is modeled by two components in Simulink that is expressed hereunder.

1. An ADC sample & hold block that is triggered by a pulse generator operating with 512 Hz frequency.
2. A 16-bit ADC quantizer

3.3 Biomedical Digital Signal Processor

The 16-bit digitized signal from the output of the ADC is delivered to the biomedical digital signal processor shown in Figure. 3.1. The digitized signal should be optimized to have enough resolution, and minimum noise to be suitable for further analysis in the DSP unit.

It is noteworthy that even with perfect signal recording and stimulation units, a closed-loop IMD cannot be effective if the biomedical DSP block is unable to detect seizures accurately with a minimum delay.

The biomedical DSP unit is in charge of extracting features and classifying them to swiftly differentiate between seizure-related and normal brain activities. Five widely used features are considered to be modeled in Simulink for the feature extraction task. 1) Coastline, 2) Energy, 3) Nonlinear energy, 4) Variance, and 5) Shannon entropy are the features that are introduced in (3.3)-(3.7).

$$Coastline(m) = \frac{1}{N-1} \times \sum_{i=2}^N |x(i) - x(i-1)| \quad (3.3)$$

$$Energy(m) = \frac{1}{N} \times \sum_{i=1}^N x(i)^2 \quad (3.4)$$

$$Nonlinear\ Energy(m) = \frac{1}{N-2} \times \sum_{i=2}^{N-1} x(i)^2 - x(i-1) \times x(i+1); \quad (3.5)$$

$$Variance(m) = \frac{1}{N} \times \sum_{i=1}^N (x(i) - \mu)^2 \quad (3.6)$$

$$Shannon\ Entropy(m) = \sum_{i=1}^N x(i)^2 \times \log_{10} x(i)^2 \quad (3.7)$$

Where (m) is the window number, (N) is the total number of samples in each window, (i) is the i^{th} sample of the window, and (μ) is the average value of the window.

As an illustration, the implementation of the energy feature is shown in Figure. 3.7. The squared value of each sample is generated by the product unit. Subsequently, the values are accumulated over a window length of 512 that is translated into a 1-sec window calculation.

The entire system model is demonstrated in Figure. 3.8. The digitized iEEG signal is given to the five feature extraction units. The features are extracted with 16-bit fixed-point signal processing techniques. Notably, a thresholding-based classification method is used in this work. Thus, the optimal thresholds are computed during training phases in a patient-specific way.

The result of all feature extractors must be analyzed together to determine the final detection label in the feature extraction techniques that employ multiple features with threshold crossing

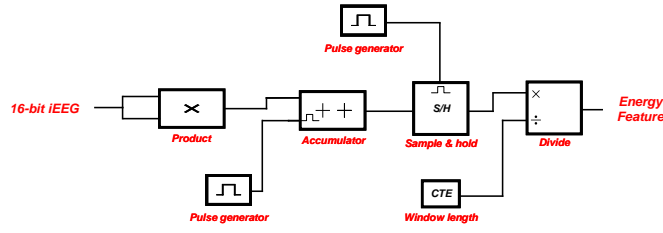


Figure 3.7: Simulink modeling of the energy feature extractor

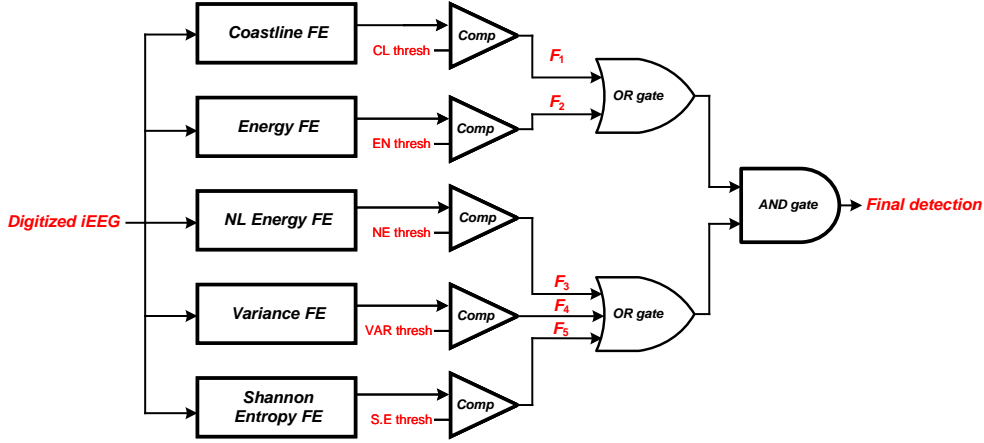


Figure 3.8: Simulink modeling of the biomedical signal processor

classification. Therefore, a function that combines logical *OR* and logical *AND* gates is chosen to make the final seizure detection decision. The seizure classification function is given in (3.8). The details regarding the constitution of logical classification functions are given in Chapter 4 and Chapter 5.

$$\text{Detection Function} = (F_1 + F_2) \cdot (F_3 + F_4 + F_5) \quad (3.8)$$

where $F_1 - F_5$ are seizure detection labels that are generated from each feature extraction unit shown in Figure. 3.8.

As a combination of logical *OR* and logical *AND* is employed, a tradeoff between true positive and false positive detections can be reached.

To evaluate the performance of the digital signal processor, the model is tested on five patients from the SWEC-ETHZ dataset that is publicly available from the Bern University Hospital epilepsy program [72]. The patients experience 33 short-term seizure periods and less than half of them are used in training phases.

The final detection signal of a sample patient (ID_2) is shown in Figure. 3.9. Two seizure events

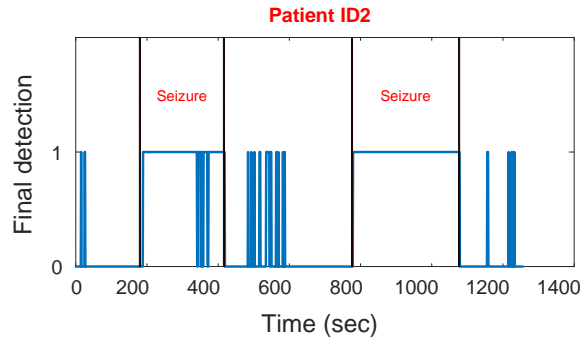
Figure 3.9: Patient ID_2 detection waveform

Table 3.2: Simulation results of the Simulink modeling

Patient	ID_1	ID_2	ID_3	ID_4	ID_5
Sensitivity (%)	83.33	100	100	100	100
Specificity (%)	91	94.58	87.5	98.5	90.28
Delay (sec)	7.8	7	6	12	8

are used in the test phase while the model is trained with the remaining two seizure events. The seizure duration is marked by red dotted lines. The first seizure starts at $t = 180 \text{ sec}$, and the last seizure ends 180 seconds before the end of the simulation. It is evident that the model is capable of detecting all two seizures quickly; however, it requires further improvements to reduce the number of false positive detections during the inter-ictal phases. The novel solutions to achieve this improvement are investigated in the next chapter of the thesis.

The simulation results of the biomedical signal processor are given in Table. 3.2. The model could reach 100% sensitivity for four patients, high specificity, and acceptable seizure detection delays for all five patients.

3.4 Wireless Power Communication

The concept of an inductive power transmission is to employ a pair of coils. Therefore, the magnetic field generated by the inductor brings about a voltage/current in the implant [74]. To model the inductive link used in wireless power and data transmission, a transfer function in conjunction with a capacitor that operates in the resonance mode is implemented.

The inductive link receives an Alternating Current (AC) voltage at the input and delivers it to a rectifier. The rectifier converts the AC voltage to an unregulated Direct Current (DC) voltage. In the circuit level, a rectifier consists of multiple MOSFET transistors that are modeled in Simulink in the form of switches with finite delays. Thus, the sinusoidal input signal of the rectifier is transformed into a DC voltage with some ripples and distortions in the output [70, 71].

The rectifier is followed by a voltage regulator to generate a stable ripple-free voltage. The voltage regulator unit is modeled in the Simulink as a transfer function with a negative feedback loop. To ensure reliable wireless power transmission, Power Feedback (PF) and Power on Reset (PoR) blocks are utilized.

The PF block indicates whether the received power is within a predefined acceptable range. It uses two bits to exhibit that the received power is higher or lower than enough power of the system.

In addition, the PoR uses a RESET bit to indicate that the power is sufficient to start a communication. The communication takes place in an uplink mode between the implant and an external unit to guarantee a steady power transmission to the implant.

The rectified and regulated voltages of the wireless power transmission unit are demonstrated in Figure 3.10. The amplitude of the regulated voltages is lower than the rectified voltage as shown in Figure 3.10.a. But, the voltage regulation is quite essential since the rectified voltage experiences ripples and fluctuations due to the load and signal amplitude modulation caused by data transmission using the same inductive link. These variations are rejected by the voltage regulator of the implant and a stable voltage is provided to be used as the implant power supply.

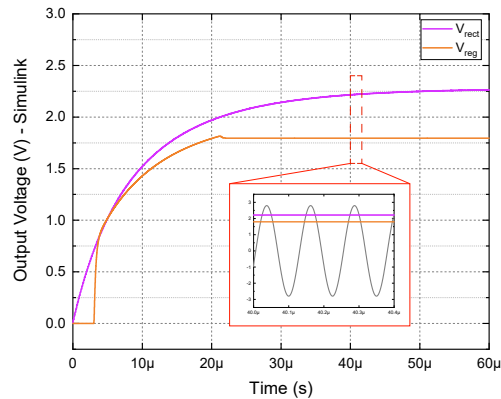
3.5 Multi-channel Charged-balanced Neurostimulator

In closed-loop seizure suppression devices, the seizure detector is followed by a neurostimulator. It has been proven that delivering mild responsive electrical pulses is effective to modulate the electrical activities of neurons and force them to behave in a normal way [75].

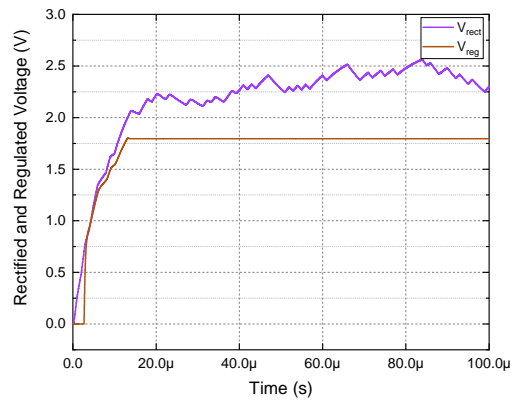
Various sorts of electrical stimulations have already been examined in the state-of-the-art to tackle different neurological disorders such as Alzheimer, epilepsy, and Parkinson's diseases. Neurostimulation can be applied in constant-current, constant-voltage, and constant-charge modes. The most frequently used form of stimulation is biphasic current-mode stimulation which is employed in this design. To model an ideal current-mode electrical stimulator, a current steering DAC is implemented in Simulink with the following specifications.

- **Bit resolution:** 5
- **Current amplitude resolution:** $31.25 \mu A$
- **Maximum stimulation current:** 1 mA
- **Stimulation frequency:** 1 kHz
- **Duty cycle:** 10%

The current-mode biphasic electrical stimulator is used since it exhibits the most accurate



(a)



(b)

Figure 3.10: Rectified and regulated voltages (a) without data communication, and (b) with data communication

charge-balancing profile. However, perfect matching between the anodic and cathodic pulses cannot avoid residual potential accumulation on the electrode-tissue interface. Hence, a charge balancer is modeled in Simulink to sustain the amount of residual imbalances below a safe window (window=40 mV) during the stimulation phases.

The anodic pulse amplitude charge modulation technique is utilized to cancel the charge imbalances. In this method, if the residual potential exceeds the 40 mV safe window, the charge balancer will be activated and modulate the anodic pulse amplitude of the following stimulation phase to compensate the charge accumulation on the electrodes.

Figure. 3.11 depicts the stimulation and residual potential signals during ten stimulation cycles. Figure. 3.11.b illustrates that the residual potential surpasses the safe window after the 4th and 6th stimulation periods. Therefore, the charge balancer is activated to modulate

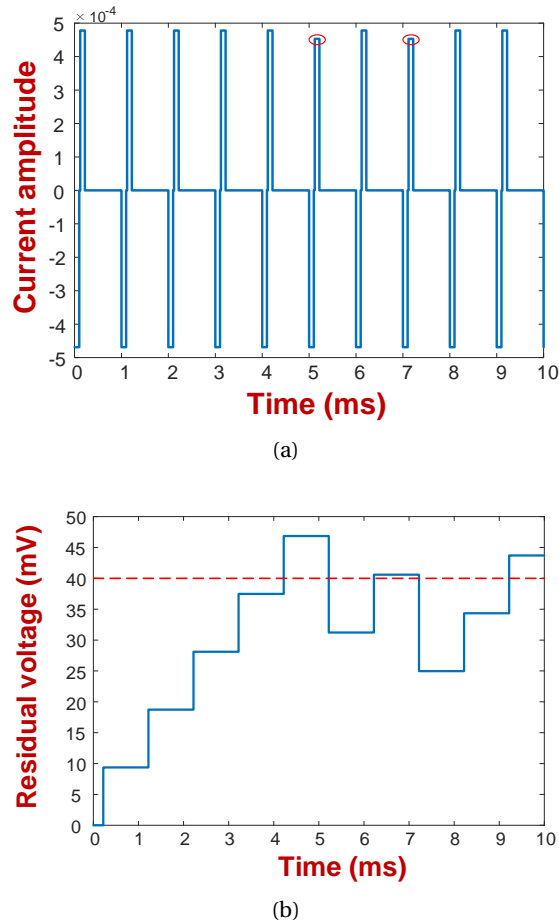


Figure 3.11: (a) Stimulation current pulses, and (b) Residual potential

the amplitude of anodic pulses in the following stimulation phases in order to neutralize the accumulated charges and ensure stimulation safety. A 100 mV residual potential would be accumulated on the electrodes after ten stimulation cycles without charge balancing.

3.5.1 Temperature Control of the Implant

All components of a closed-loop IMD for epilepsy control have been modeled and investigated using Simulink software. It allows us to perform several control tasks within the design to achieve different therapeutic or electronic design goals. The highest priority in the design of an IMD is the safety of patients. As a consequence, implants must be designed to fulfill strict power-budget constraints to avoid remarkable temperature rise in the brain tissue.

According to [70,76], the maximum allowed temperature elevation caused by the implant is 1°C . The controller block of the design attempts to limit the temperature rise below 1°C by adjusting the stimulation parameters. The number of stimulation channels and the amplitude of stimulation pulses in the cathodic and anodic phases are the major parameters that determine

the total power consumption of the implant. For instance, delivering 1 mA current pulses to a tissue with impedance of $1\text{ k}\Omega$ with 10% duty cycle results in 100 mW power consumption per channel.

The maximum stimulation current is 1 mA which is provided by a 5-bit current DAC. Therefore, the minimum stimulation current ($I_{stim-min}$) is $31.25\ \mu\text{A}$. As previously stated, the maximum number of stimulation channels is 12.

The temperature elevation of the implant depends on not only the device power consumption but also the size and location of the implant. A typical brain implant size with the dimension of $4 \times 4 \times 0.5\text{ mm}^3$ is considered in this model that is implanted in the brain's right lobe. In addition, the δ parameter is an important factor that links the power consumption of the implant to the corresponding temperature elevation depending on the device size and implant location. It is the slope of the power consumption that is plotted versus the device temperature. According to the model specifications, the δ parameter is equal to $\delta = 0.083\ \frac{\text{°C}}{\text{mW}}$.

Hence, if all stimulation channels are activated with minimum stimulation current, the temperature rise of the implant is $0.46\ \text{°C}$, which is within the allowed range. However, stimulating with the minimum stimulation current would not be effective for all patients. As a result, the stimulation current must be adjustable depending on the seizure severity and duration to realize specific therapeutic goals. The controller of the implant dynamically modifies the stimulation amplitude and the active number of stimulation channels to guarantee the safe operation of the device.

In order to demonstrate the effectiveness of the temperature control process, the model is tested on a random subject (ID5 from SWEC-ETHZ dataset) which has five seizure occurrences. The temperature elevation caused by the implant without and with the controller block is illustrated in Figure. 3.12.a. Furthermore, the number of active stimulation channels is shown in Figure. 3.12.b.

During the first two seizures, stimulation is conducted with the maximum number of stimulation channels ($N=12$), and the minimum stimulation current ($I_{stim} = I_{stim-min}$). The temperature rise during the seizure events is $0.46\ \text{°C}$. Thus, no parameter modification is required. The stimulator increases the stimulation current to $3 \times I_{stim-min}$ in the third and fourth seizure events. It is evident that without controlling tasks, the temperature rise of the implants surpasses the $1\ \text{°C}$ limit which may cause detrimental effects on the human brain. Thus, the controller reduces the active number of stimulation channels by deactivating three electrodes shown in Figure. 3.12.b. Subsequently, the stimulation amplitude is set to $5 \times I_{stim-min}$ during the last seizure of the patient. Without modification of the stimulation channels, the temperature elevation goes over $2\ \text{°C}$. As a consequence, the controller unit deactivates seven stimulation channels to decrease the temperature elevation to approximately $0.9\ \text{°C}$.

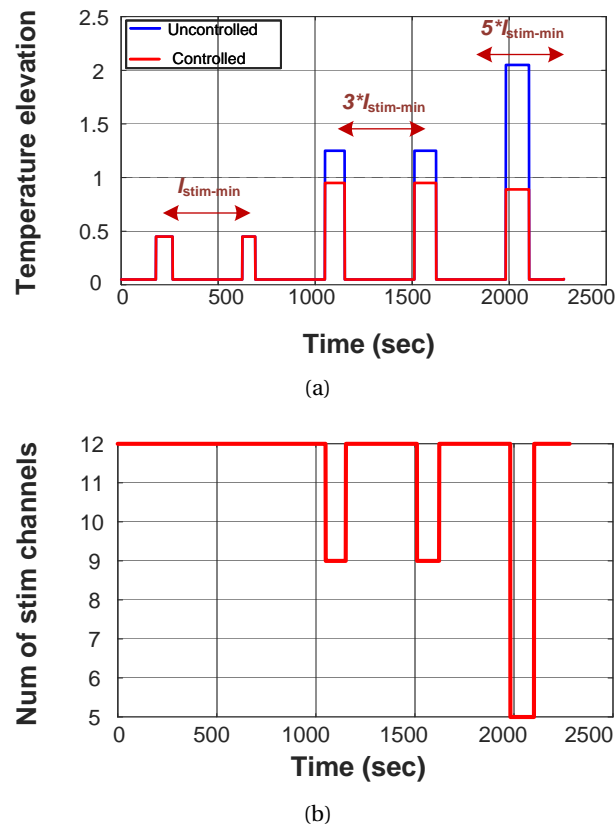


Figure 3.12: (a) Temperature elevation, and (b) Num of active stimulation channels

3.6 Summary and Conclusions

This chapter presented the model of a closed-loop epilepsy control implant at system level. A typical wirelessly-powered implant for close-loop epileptic seizure suppression is composed of recording channels, a digital signal processor, stimulation channels, wireless power and data transmission units, a temperature sensor, and a controller. All aforesaid units are modeled in Simulink and their operation is explained and demonstrated through the simulations. The crucial parameters of each component are determined that can be adjusted by an electronic engineer to obtain various design targets.

The AFE is capable of capturing extremely low-amplitude neural signals and delivering a clean and high-resolution iEEG signal to the DSP unit. The AFE provides a 50 dB amplification in frequencies lower than 2 kHz. Subsequently, 16-bit digital data is generated through analog to digital conversion.

The DSP extracts Coastline, Energy, Nonlinear Energy, Variance, and Shannon Entropy features. 1-sec window-based fixed-point signal processing and classification methods generate labels for all windows and activate the neural stimulator upon an upcoming seizure detection.

A 12-channel biphasic-current-mode electrical stimulator is utilized to deliver mild pulses to the brain region that involves the onset of seizures. The multi-channel constant current stimulator is equipped with a charge balancer to guarantee safe electrical stimulation in the long run by keeping the residual potential accumulation under control.

System-level modeling enables the designers to analyze and perform different control tasks. The temperature rise of the implant, which is a crucial safety parameter, was taken into account. The relation between stimulation parameters and temperature elevation of the implant was explained. Therefore, the implant controller dynamically modifies the stimulation parameters to continuously maintain the temperature elevation of the device below 1 °C.

4 Hardware-Friendly Digital Signal Processing

4.1 Introduction and Motivations

The digital signal processor is considered as the heart of IMDs for epilepsy treatment. It plays a significant role in the overall performance of the device. For instance, late seizure detection directly affects the electrical stimulation performance and makes it pointless for seizure cancellation. Although a large number of advanced signal processing techniques have already been developed to perform seizure detection, their adaptation to hardware implementation for implantable and wearable applications is not fully investigated.

The majority of the algorithms available in the literature can only be used for automatic real-time seizure detection as a software application to be installed on the computer of neurologists. Those techniques may replace the overwhelming duty of physicians to continuously monitor the brain activities of patients. Nevertheless, they are not compatible with portable and implantable applications in terms of area occupation, energy efficiency, and power dissipation.

In this chapter, various types of features in the time domain are extracted using hardware-friendly techniques. Furthermore, the extracted features are used to classify the ictal and non-ictal states of patients using thresholding as well as machine-learning methods. The structures of different feature extraction and classification methods are modified to make them suitable for hardware implementation.

Besides, an important challenge in feature extraction is the high dimensionality of the features required for accurate seizure detection. This chapter proposes novel techniques concerning feature ranking and dimension reduction to make a balanced tradeoff between hardware complexity and seizure detection performance.

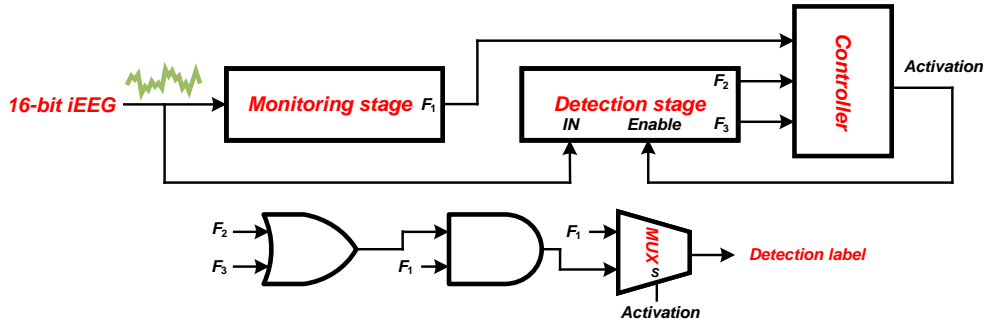


Figure 4.1: Block diagram of the two-stage feature extractor

In addition, advanced iEEG recording systems employ microelectrode arrays including tens of stripe, and grid electrodes. Although an extremely high recording resolution can be achieved, the dimension of the input signal is excessively high for digital signal processing. Hence, novel electrode channel selection techniques are proposed in this chapter.

Lastly, the architectures of different machine-learning classification approaches are studied and a RF classifier is optimized for hardware implementation in terms of logic usage and power dissipation. Moreover, the hardware compatibility of the suggested machine-learning-based technique is evaluated by the Field-Programmable Gate Array (FPGA) implementation to guarantee the low-power real-time operation of the design.

4.2 Energy-Efficient Feature Extraction

Relying on a single feature is not sufficient to detect the seizures of a large group of patients [14, 47] since the brain activities of different patients are quite diverse and a unique feature is unable to perform well on all brain signal types. Therefore, more than one feature must be included in the feature extraction unit to achieve acceptable results for a wide variety of subjects. However, the power budget limitation is another critical factor of implants that extract multiple features [77, 78].

A two-stage feature extraction system is proposed in this thesis which addresses the aforementioned challenges. In a two-stage feature extractor system, multiple features can be extracted in an energy-efficient manner. Moreover, the majority of the features are extracted in the second stage of the system that is deactivated during long inter-ictal periods.

The architecture of the two-stage feature extractor is depicted in Figure. 4.1. The first stage is called the monitoring stage which continuously extracts a feature with high seizure detection sensitivity. The second stage called the detection stage is temporarily activated by the controller to reduce false detections. when the second stage is deactivated, the seizure detection label is determined by the output of the monitoring stage. Otherwise, the logical gates and the multiplexer shown in Figure. 4.1 determine the seizure detection label.

To illustrate the performance of the novel two-stage feature extractor, three time-domain low-complexity features are chosen. The coastline, energy, and nonlinear energy features are described hereunder.

- The **coastline** feature represents the absolute difference between adjacent samples
- The **Energy** feature represents the squared value of the samples
- The **Nonlinear energy** feature represents the difference between the energy of the adjacent samples.

The **monitoring stage** of the proposed feature extractor continuously extracts the feature with the highest seizure detection sensitivity which is determined during the training phase. The feature used in this stage must exhibit a higher sensitivity compared to the other features to minimize the seizure detection delay. This feature is selected in a patient-specific training phase.

The **detection stage** extracts the majority of the features for a short time when the detection stage identifies an upcoming seizure event. Thus, the energy consumption of this stage does not significantly increase the power consumption of the digital signal processor. The main role of the detection stage is to minimize false positive detections. As a consequence, the thresholds of the features used in this stage are optimized to exhibit the minimum false positive detections. The controller units ascertain the activation duration of the detection stage.

It is noteworthy that a **post-processing** block is employed in both the monitoring and detection stages to filter the unwanted fluctuations of the output signal. A majority voting post-processing unit is utilized in this work. The length of the post-processing window is 3 seconds. The window length has a direct impact on the seizure detection delay. That is why a window with a minimum length is chosen in this work.

Figure .4.2 exhibits the post-processing procedure at Register-Transfer Level (RTL). The extracted feature (D_e) is compared with a threshold value and generates an early detection signal. The early detection signal is given to the post-processing majority voting with a 3-sec window length and generates the post-processed detection (D_{pp}).

The **controller** makes coordination between the monitoring and detection stages. It activates the detection stage for nine seconds when the monitoring stage detects an upcoming seizure. The duration of the detection stage activation is determined considering a tradeoff between seizure detection accuracy and energy consumption of the feature extractor.

The multiplexer shown in Figure. 4.1 determines the detection label of the two-stage system. The *SELECT* input of the multiplexer is connected to the controller output. Thus, when the second stage is deactivated, the detection label is the output of the first stage. Otherwise, the logical block which consists of logical OR and logical AND gates determines the detection

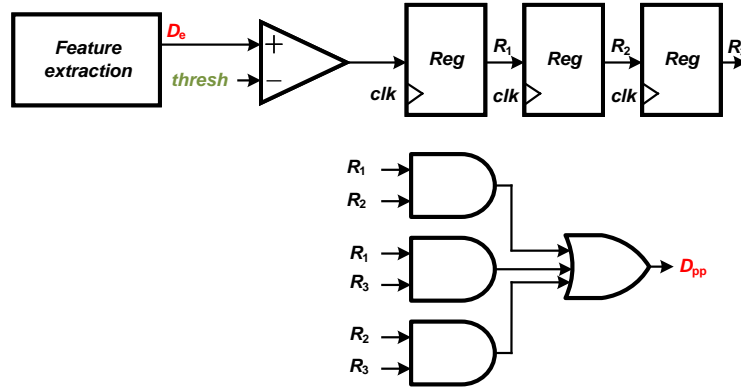


Figure 4.2: RTL view of the post-processing block

label. The logical function is given in (4.1).

$$Detection\ Function = F_1\ AND\ (F_2\ OR\ F_3) \quad (4.1)$$

(4.1) expresses that the detection signal of the first stage (F_1) is validated by at least a feature from the second stage to arise a detection flag. Thus, the detection function is capable of reducing the number of false positive detections which is of paramount importance in closed-loop IMDs.

4.3 SWEC-ETHZ Dataset

The dataset used throughout this thesis is the long-term and short-term datasets of the Sleep-Wake-Epilepsy-Center (SWEC)-ETHZ recorded in the University Department of Neurology in the Inselspital Bern [79]. The iEEG signals are recorded during the pre-surgical evaluations of medicament refractory patients. The dataset is publicly available and they are marked by an epileptologist to provide appropriate labels for the onset and termination of seizures during signal processing tasks. The long-term dataset contains the iEEG of 18 patients with 116 seizure events in the long-term recordings.

The brain activities of patients are captured by strip, grid, and depth electrodes. iEEG signals were sampled at 512 Hz and 1024 for different patients. Then, the analog-to-digital conversion is done by a 16-bit ADC. Two filters conduct post-processing tasks that are explained hereafter.

- A 4th order Butterworth filter applies a band-pass filtering to keep the iEEG signals within the frequency range of 0.5 Hz - 120 Hz.
- Backward & forward filtering is applied to the recorded signals to minimize the phase distortion that is highly important for the signals that are used in the frequency domain signal processing.

Table 4.1: Long-term SWEC-ETHZ dataset information

Patient	Num of electrodes	Recording hours	Num of seizures	Num of trained
ID1	88	293	2	1
ID2	66	235	2	1
ID3	64	158	4	2
ID4	32	41	4	2
ID5	128	110	8	3
ID6	32	146	4	2
ID7	75	69	8	4
ID8	61	144	4	2
ID9	48	41	23	11
ID10	32	42	17	8

Table 4.2: Short-term SWEC-ETHZ dataset information

Patient	Age	Num of electrodes	Avg Seiz (sec)	Num of seizures	Num of trained
ID1	46	47	37.8	13	6
ID2	48	42	267.5	4	2
ID3	32	62	98	2	1
ID4	19	42	223	4	2
ID5	31	54	37.8	10	5
ID6	31	64	15	4	2
ID7	36	36	98	2	1
ID8	23	61	121	3	1
ID9	49	92	79	6	3
ID10	24	47	71	13	6

After filtering in the digital domain, the data is stored at the frequency of 512 Hz. Table. 4.1 provides some information concerning the number of seizures, total hours of recording as well as data partitioning in training phases.

The details concerning the specifications of seizures for different patients are provided in Table. 4.2 [80].

4.4 Two-stage Feature Extraction Training Phase

The training phase of a two-stage automatic seizure detector offers valuable information concerning the importance of each feature. It is noteworthy that the training phase must be conducted in an unbiased way. Splitting the dataset into different groups is an important consideration to ensure that the model can learn from diverse and representative information.

To this aim, the dataset is divided into three groups that are given hereunder.

- **Training subset:** This partition of the dataset is used to train the model and define the hyperparameters.
- **Validation subset:** This partition of the dataset is used to optimize and tune the hyperparameters to reach the design's goals.
- **Test subset:** The test phase is used to conduct the final evaluation of the model and get the evaluation metrics such as precision, recall, F_{score} , and accuracy.

The minimum partition of data used in the training set must be carefully studied in the seizure detection system since seizure events are rare compared to non-seizure episodes. Therefore, a classifier that necessitates acquiring long hours of iEEG recordings during seizures may not work on patients who have a few short-term seizures in a month. Hence, this model is able to be trained using less than 50% of the dataset which is a big advantage over deep learning techniques that often need more than 80% of available data to use in the training phase.

Besides, the optimal thresholds of the features in the proposed two-stage system are computed in the training phase. Threshold calculation involves a tradeoff between the model's ability to correctly detect positive and negative labels. However, this tradeoff is regarded as an opportunity to enhance the system performance of the proposed model. The features that are used in the monitoring stage should be powerful enough to accurately detect the positive labels. The threshold of the feature in the monitoring stage is optimized to obtain the highest true positive detection rate.

On the other hand, the features in the detection stage should yield the minimum false positive detections to avoid unnecessary activation of the stimulator in closed-loop systems. The activation of the stimulator according to a false seizure detection not only has a destructive effects on the therapy but also increases the device power consumption and temperature elevation. Hence, the thresholds of features selected in the detection stage are optimized to minimize false positive detections during the training phase using the validation data subset.

The feature ranking is essential to properly assign features to the monitoring and detection stages. As a result, the accuracy of the features are computed using the validation data subset when the model is trained. The feature with the highest accuracy is selected for the monitoring stage, and the remaining two features are used in the detection stage. The feature ranking results of six patients from the SWEC-ETHZ database are demonstrated in Table. 4.3.

The importance of patient-specific feature extraction can be interpreted from Table. 4.3. It demonstrates that a single feature cannot yield the best performance on all tested patients. Hence, relying on a single feature extraction will fail to lead to high seizure detection results.

4.5 FPGA Implementation Results

The performance of the novel seizure detector with a two-stage feature extraction architecture

Table 4.3: Feature ranking results of the training phase

Patient ID	Feature ranks		
	Rank 1	Rank 2	Rank 3
1	Coastline	Nonlinear energy	Energy
2	Coastline	Nonlinear energy	Energy
3	Energy	Coastline	Nonlinear energy
4	Energy	Coastline	Nonlinear energy
5	Coastline	Energy	Nonlinear energy
6	Nonlinear energy	Energy	Coastline

Table 4.4: FPGA implementation details

Clock frequency	Num of registers	Memory bits	Dynamic power	Static power
512 Hz	955	175104	105 μ W	135 mW

is evaluated and tested on six patients with 120 hours of EEG recordings. The seizure detector is implemented on the Cyclone V FPGA of the ALTERA DE10-standard board. The hardware implementation parameters are given in Table. 4.4.

Several performance parameter metrics have been considered to evaluate seizure detectors in terms of accurate and timely seizure detection. The most important metrics that are commonly used in the literature are summarized hereafter.

- **Sensitivity:** It measures the proportion of the actual seizures that are correctly detected by the seizure detector. It is calculated as the number of true positive detections divided by the total number of actual seizures. The sensitivity calculation is given in (4.2).

$$Sensitivity = \frac{TP}{TP + FN} \quad (4.2)$$

- **Specificity:** It determines the rate of true negative detections. It measures the proportion of non-seizure samples that are correctly detected by the seizure detector. It is calculated as the number of true negative detections divided by the total number of actual non-seizure samples. The specificity calculation is given in (4.3).

$$Specificity = \frac{TN}{TN + FP} \quad (4.3)$$

- **Precision:** It represents the proportion of seizure detections that are correctly identified. It is computed as the number of true positive detections divided by the total number of positive detections. The precision calculation is given in (4.4).

$$Precision = \frac{TP}{TP + FP} \quad (4.4)$$

- **Negative predictive value:** It measures the proportion of non-seizure segments that are correctly identified by the seizure detector. It is computed as the number of true negative detections divided by the number of negative detections. The negative predictive value is given in (4.5).

$$NPV = \frac{TN}{TN + FN} \quad (4.5)$$

- **Accuracy:** It measures the ability of seizure detectors in correct detections of both positive and negative labels. It is calculated as the total number of true detections divided by the total number of segments. The accuracy parameter is given in (4.6).

$$Accuracy = \frac{TP + TN}{TP + TN + FP + FN} \quad (4.6)$$

- **F1-score:** It is the harmonic mean of the precision and sensitivity parameters. It can be highly useful in classification systems in which the number of positive and negative labels are imbalanced such as the epilepsy detection problem. The F1-score parameter is calculated in (4.7).

$$F1 - score = 2 \times \frac{Precision \times Sensitivity}{Precision + Sensitivity} \quad (4.7)$$

- **AUC-ROC:** The area under the curve of the receiver operating characteristics is an important parameter that determines the ability of the seizure detector to distinguish between seizure and non-seizure segments based on different detection thresholds. This metric is highly beneficial to evaluate the systems that require threshold optimization.
- **Detection delay:** The detection delay measures the time difference between the first positive label and the first marked seizure.

The two-stage seizure detector significantly decreases the energy consumption of the implantable seizure detector during long non-seizure periods by deactivating the features that are extracted in the detection stage. As a consequence, a new performance parameter metric is defined to demonstrate the superiority of two-stage seizure detectors over typical detectors. The new metric is called Detection stage Activation Ratio (DAR) which measures the time

Table 4.5: FPGA implementation details

	Method 1	Method 2	This work
Sensitivity	100%	100%	100%
Specificity	88.50%	94%	92.1%
Delay (sec)	5.7	12.9%	7.8%
DAR	n.a	1	0.272

proportion over which the detection stage is activated. The DAR is defined in (4.8).

$$DAR = \frac{t_{det}}{t_{sim}} \quad (4.8)$$

Where t_{det} is the time over which the detection stage is activated and t_{sim} is the total test phase duration. When ($DAR = 0$), the detection stage remains deactivated during the entire test process and the energy consumption of the seizure detector is minimum since only a single feature is extracted in the detection stage. On the other hand, when ($DAR = 1$), the detection stage continuously operates and the energy consumption reaches its maximum value by extracting all features continuously.

In the designed seizure detector, the coastline, energy, and nonlinear energy features are extracted using a two-stage topology. To visualize the advantages of the proposed design over the conventional seizure detection systems, the FPGA implementation result of the two-stage seizure detector is compared with two other methods that are explained hereunder.

- **Method 1:** Feature extraction using a single coastline feature
- **Method 2:** Feature extraction using three features in a conventional single stage topology

A seizure event of patient ID_1 is used for comparison purposes that is depicted in Figure 4.3.a. The seizure commences at $t = 100$ sec and it terminates at $t = 130$ sec. The proposed seizure detector exhibits less false alarm rate before the seizure onset compared to Method 1. Furthermore, the proposed design has a lower number of false positive detections before and after the seizure episode compared to Method 2.

The FPGA implementation results of the proposed seizure detector as well as two aforementioned models are summarized in Table 4.5 which includes the sensitivity, specificity, detection delay, and DAR metrics. All three methods could reach 100% sensitivity tested on six drug-resistant patients with long-term EEG recordings. Compared to Method 1 which employs only the coastline feature, the proposed method offers a higher specificity and lower false positive detections. In addition, this work exhibits remarkably lower detection delay compared to Method 2. Moreover, the proposed design achieves a very low DAR of 0.272. It conveys that the detection stage is activated only during 27% of the test period which is a highly practical approach for saving energy consumption for implantable applications.

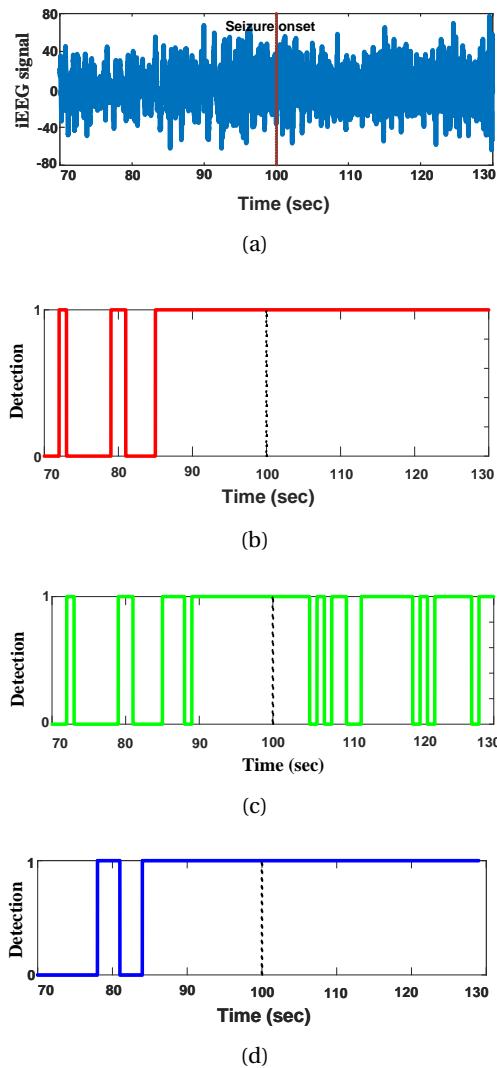


Figure 4.3: (a) iEEG signal of the patient ID1, (b) Method 1 detection, (c) Method 2 detection (d) The two-stage design detection

4.6 Feature Ranking and Selection

The feature ranking and selection is considered as a crucial step in the development of efficient hardware-compatible seizure detectors. EEG signals are complex and multi-dimension containing a wide variety of patterns with time-varying frequency components. As a result, different types of features are required to be extracted so as to yield acceptable seizure detections.

Thus, an efficient seizure detector includes multiple features in its feature pool. However, feature selection is necessary for portable and implantable applications since the number of resources and power budget is extremely limited. Patient-specific feature ranking and

selection methods offer a practical solution to these challenges.

In the feature ranking process, the most relevant and informative features are identified in a subject-specific manner. The feature ranking offers many advantages that are summarized hereafter.

- Data dimensionality reduction
- Computation efficiency improvement
- Over-fitting risk reduction
- Classification enhancement
- Enabling real-time operation
- Accelerating signal processing and enabling the clinical deployment

4.6.1 Conventional Feature Ranking Techniques

The information gain, relief algorithm, and recursive feature elimination are regarded as common approaches for the feature dimension reduction in the literature [81, 82]. These methods are briefly explained hereunder.

The **Information Gain** measures the reduction in the entropy of the signal when the raw input data is transformed into the extracted feature. The feature with the higher entropy reduction receives a higher information gain value and obtains a higher rank in the process. Therefore, the features are ranked based on their informative aspects.

The concept of feature ranking with the **relief algorithm** is to identify the quality of each attribute in distinguishing the samples that are so close to each other. The weights of the features are calculated according to two distance values. The first distance is called a *hit* which is the distance between the feature and the nearest feature in the same class. The second distance is called a *miss* which is the distance between the feature and the nearest feature in the opposite class. The features are sorted according to their discriminative abilities.

The **recursive feature elimination** technique is a machine-learning-based feature ranking algorithm [81]. In this method, the less relevant features are iteratively removed from the initial feature set to reach one of the following goals.

- The desired number of the features
- The desired performance metric threshold

The steps of feature ranking using the recursive feature elimination method are explained hereafter.

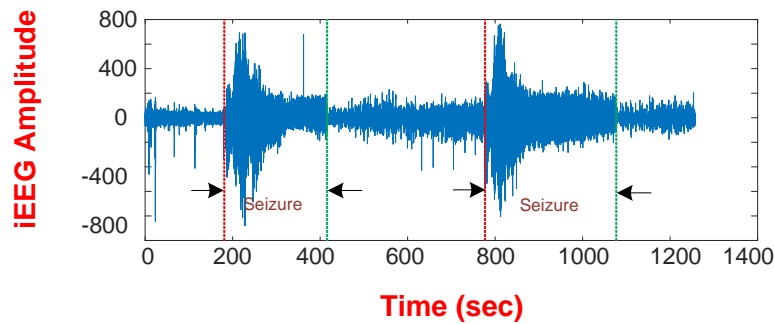


Figure 4.4: iEEG signal of a patient with two seizure events

1. The model is trained with all available features using a machine-learning classifier like SVM, RF, and decision trees.
2. The feature importances are computed according to the contribution of features in the model performance.
3. The feature with the least importance factor is eliminated from the feature set.
4. The model is retrained using the remaining features
5. Iteration until reaching the design target

4.6.2 Proposed Feature Ranking Algorithm

The proposed feature ranking algorithm is applied to a time-domain feature pool consisting of low-complexity features. 11 time-domain features including the coastline, energy, nonlinear energy, variance, minimum, maximum, root-mean-square, range, average, correlation, inter-quartile range form the feature pool of the seizure detector. To visualize the extracted features during seizure and non-seizure episodes, the iEEG of a sample patient with two seizure events is demonstrated in Figure. 4.4. The extracted features are categorized into amplitude-based features and amplitude-square-based features illustrated in Figure. 4.5 and Figure. 4.6, respectively. The signals plotted in red and blue denote the extracted features during seizure and non-seizure states, consecutively.

Figure. 4.5 and Figure. 4.6 disclose the fact that coastline, energy, and nonlinear energy features are more discriminative than the others for the seizure detection of the selected patient and it emphasizes the necessity of a patient-specific feature dimension reduction.

In this thesis, a two-step feature ranking algorithm is proposed to be employed in the two-stage feature extractor. The novel algorithm is called Maximum Discrimination Minimum Redundancy (MDMR) feature ranking [14]. The MDMR algorithm selects the most informative features which demonstrate the least redundancy with each other. The ranking is done in a two-step process using the Feature Discriminating Parameter (FDP) and *Mutual information*

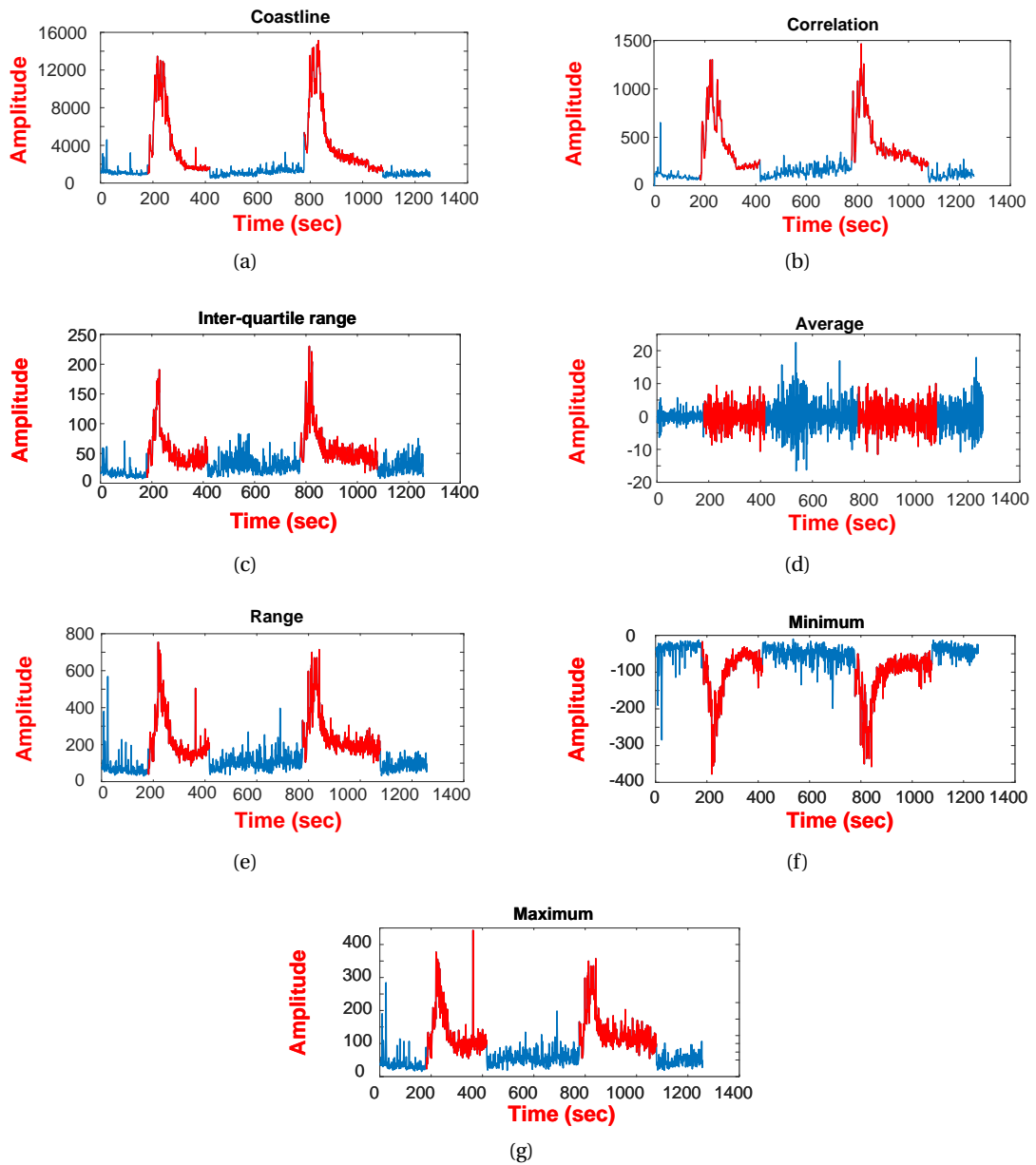


Figure 4.5: Extraction of amplitude-based features

measures. The FDP represents how well a feature discriminates between seizure and non-seizure episodes and it is defined in (4.9). Where F is the extracted feature, t_s is the duration of the seizure states, and t_{ns} is the duration of the normal states. The feature with the highest FDP has the largest average distance between seizure and non-seizure states.

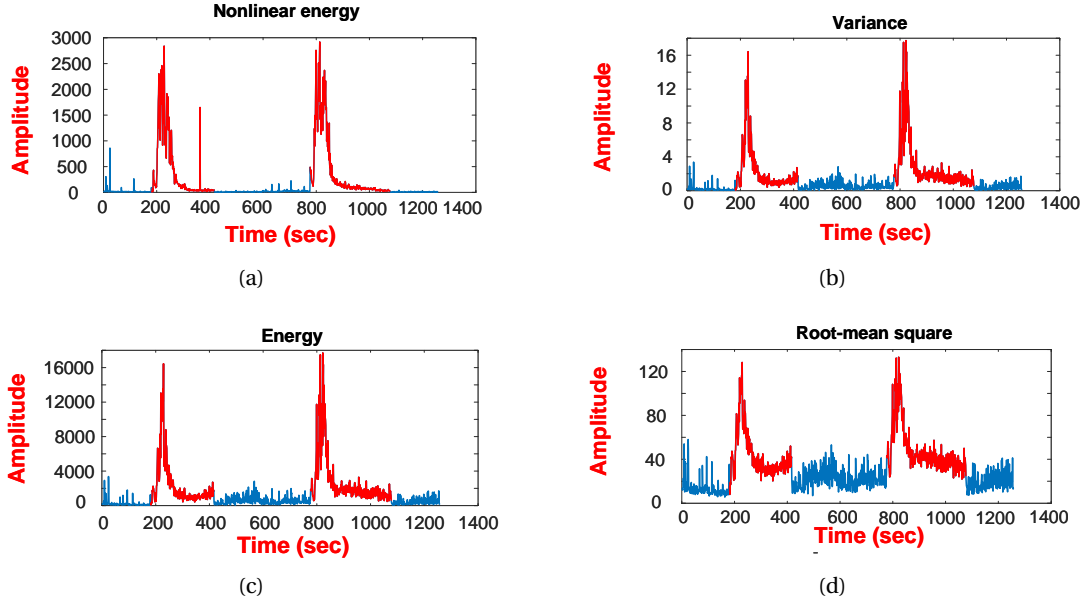


Figure 4.6: Extraction of amplitude-square-based features

$$FDP = \frac{\frac{\sum_{ts} F}{t_s}}{\frac{\sum_{ms} F}{t_{ms}}} \quad (4.9)$$

In addition, the mutual information is a measure that quantifies the level of dependency between two random variables. It is calculated as (4.10) [14].

$$M.I(F_1, F_2) = \sum \sum P(F_1, F_2) \times \log \frac{P(F_1, F_2)}{P(F_1) \times P(F_2)} \quad (4.10)$$

Where $P(F_1, F_2)$ is the joint probability mass function of two features and $P(F_1)$ is the marginal probability function. If two features exhibit a high mutual information, it means that they have a high correlation and one of them can be eliminated in order to reduce the redundancy.

The two-step MDMR ranking algorithm, which is applied on a two-stage feature extractor, is depicted in Figure .4.7. In the first step, the features are ranked with respect to their FDP values. Three features with the least FDP are filtered out, and the top 8-rank features are given to the second step. In the second step, the top two rank features obtained from the first step are assigned to the monitoring stage of the seizure detector. Subsequently, the mutual information of the remaining six features and the monitoring stage features are calculated. The two features that have the highest mutual information are removed from the feature set,

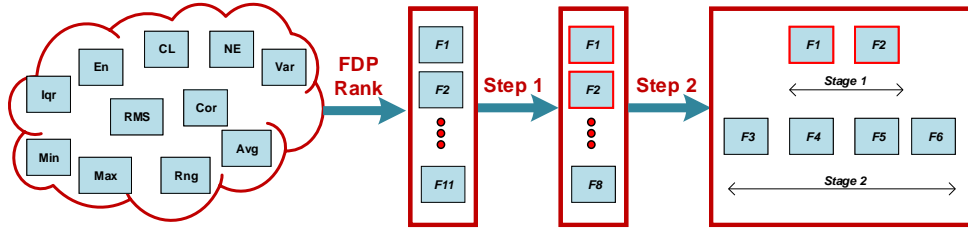


Figure 4.7: MDMR feature selection procedure

and the remaining four features are chosen for the detection stage. The **pseudo-code** of the MDMR feature ranking algorithm is given hereunder.

1. for $i=1:\text{num of features}$

$$F_i(s) = \frac{\sum_{t_s} F_i}{t_s}$$

$$F_i(ns) = \frac{\sum_{t_{ns}} F_i}{t_{ns}}$$

$$FDP(i) = \frac{F_i(s)}{F_i(ns)}$$
 end
2. FDP_rank \leftarrow sorting FDPs in descending order
3. Filtering out the FDP_rank(11), FDP_rank(10), FDP_rank(9)
4. Detection stage features \leftarrow FDP_rank(1) and FDP_rank(2)
5. for $j=3:8$

$$M.I(j) = M.I(1, \text{FDP_rank}(j))$$
 end
6. MI_rank \leftarrow sorting M.I ascending order
7. Detection stage features \leftarrow MI_rank (1), MI_rank(2), MI_rank(3), and MI_rank(4)
8. end

The proposed MDMR feature selection algorithm is tested on seven patients from the SWEC-ETHZ dataset and the results are given in Table. 4.6.

4.7 Electrode Channel Selection

Recording of iEEG signals typically involves a large number of electrode channels to provide sufficient spatial resolution. It is usually done by microelectrode arrays that contain approximately 100 electrodes. However, recording from several electrode channels contributes to computational challenges in conjunction with information overload.

Consequently, electrode selection is a crucial step in the development of an effective seizure

Table 4.6: Feature ranking results

Patient	Monitoring stage features		Detection stage features			
ID1	Energy	Nonlinear energy	Average	IQR	Max	Min
ID2	Coastline	Nonlinear energy	Cor	Variance	Max	Energy
ID3	Nonlinear energy	Variance	Energy	Cor	Min	Max
ID4	Energy	Average	IQR	Min	Range	Max
ID5	Nonlinear energy	Energy	Cor	Min	IQR	Range
ID6	Variance	Nonlinear energy	IQR	Correlation	Min	Range
ID7	Nonlinear energy	Min	Range	Max	Cor	RMS

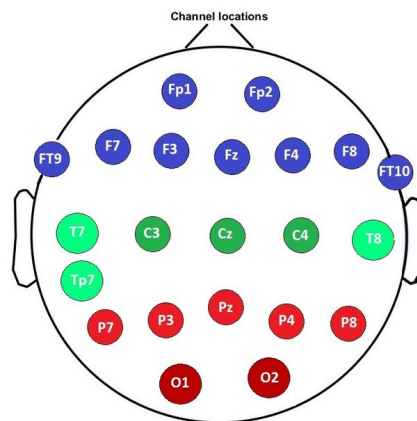


Figure 4.8: 10-20 electrode positioning system

detector. The electrode configuration must be optimized to capture relevant information. Channel selection techniques offer many benefits that are summarized hereunder.

- Data dimensionality reduction
- Computational burden reduction
- Real-time seizure detection
- SNR improvement

Different electrode positioning configurations have been used for EEG recording. The 10-20 electrode positioning system is a commonly used international standard for electrode positioning in EEG recordings. The configuration of the 10-20 system is shown in Figure. 4.8 [83].

The 10-20 term refers to the distances between the electrode placements. It means that the distances between the electrodes are 10% or 20% of the distances between front-back or right-left of the skull. The locations of the sample electrodes are described hereunder.

- F_{p1} and F_{p2} : Frontopolar locations; above the forehead.
- F_3 and F_4 : Frontal locations; along the hairline.
- C_3 and C_4 : Central locations; over the central part of the scalp.
- P_3 and P_4 : Parietal locations; toward the back of the head.
- O_1 and O_2 : Occipital locations; at the back of the head.

It should be noted that other electrode positioning systems like the 10-10 system are also available to capture EEG signals with higher spatial resolution and more electrodes.

Electrode channel selection can be conducted by machine learning techniques, spatial sampling, and manual methods according to the expert's knowledge. In the channel selection by machine learning techniques, a machine-learning-based classifier is trained using data from all electrodes. Afterward, according to the contribution of the electrodes to the model performance, the informative channels are distinguished and selected. In the spatial sampling technique, the cerebral cortex is divided into different regions and a spatially-distributed electrode configuration is achieved by the electrode selection. Moreover, an epileptologist can visually inspect the iEEG recordings and identify the most informative channels that demonstrate the minimum noise and artifacts. However, the manual method is quite overwhelming and time-consuming which must be replaced by new technologies and automatic approaches.

The PCA is a statistical data dimension reduction technique available in the literature. It reduces the amount of input data while preserving the most important information [84]. The PCA channel selection is carried out in four steps that are described hereunder.

- **Step 1:** The covariance of the multi-channel iEEG data is calculated. The covariance matrix provides insight into the relationship between different channels.
- **Step 2:** The PCA algorithm is applied to the covariance matrix and the eigenvectors and eigenvalues are computed. Eigenvectors demonstrate the principal components of the data and the eigenvalues reveal the importance of each principal component in the data variance.
- **Step 3:** N top-rank eigenvectors with the most eigenvalues are chosen.
- **Step 4:** The channels that contribute the most to the selected principal components are chosen.

The primary disadvantage of the PCA electrode channel selection is the significant loss in the temporal resolution of data if we need a remarkable data reduction rate. Thus, it may not be practical in the iEEG recording and processing for implantable applications.

In this work, we consider a channel selection technique based on the energy variation of channels during seizure events. The relation between the channel selection technique and the

features is a critical consideration. The energy of electrodes is chosen for channel selection on the grounds that the energy is associated with the squared amplitude of data and the features available in the feature pool are amplitude-based or amplitude-square-based features.

The channels are ranked according to their Channel Energy Ratio (C.E.R) that is defined in (4.11).

$$C.E.R(k) = \frac{\frac{\sum_{i=1}^{N_s} X(i)^2}{N_s}}{\frac{\sum_{i=1}^{N_n} X(i)^2}{N_n}} \quad (4.11)$$

Where K is the electrode number, $X(i)$ is i^{th} sample of data, N_s is the number of seizure samples, and N_n is the number of non-seizure samples. The channel with a high *C.E.R* exhibits a high energy variation which is regarded as an informative channel [14]. During the offline training phase, the *C.E.R* metrics of the electrode channels are computed and the number of selected channels are optimized. Therefore, the irrelevant channels are disregarded and the most discriminative channels are chosen.

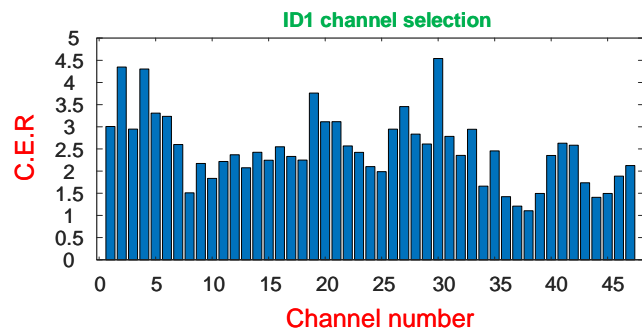
Figure. 4.9 depicts the *C.E.R* of the electrode channels of four patients from the SWEC-ETHZ dataset. It can be observed that some specific channels demonstrate a *C.E.R* much higher than the rest. For instance, electrode channel number 81 of patient ID_3 has a *C.E.R* over 45, while the *C.E.R* parameters of the majority of the channels are less than 15. Thus, this channel is highly sensitive to seizure events. In addition, the electrodes implanted in the specific regions of the brain are more informative than the others. So, a subject-customized channel selection is helpful to identify the exact cortical region related to the seizure events.

After ranking the electrodes based on the proposed approach, the number of the selected channels is determined in a patient-specific way during the training phase. Figure. 4.10 depicts the optimization of the selected channels for three patients from the dataset (ID_1 , ID_2 and ID_3). The optimized number of channels is obtained to realize the highest diagnostic accuracy. The optimized number of selected channels for the patients ID_1 , ID_2 and ID_3 are 10, 25, and 60, respectively.

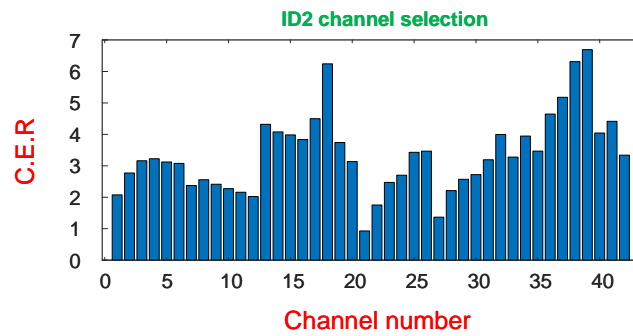
The **pseudo-code** of the proposed channel ranking algorithm is given hereunder.

1. for $i=1$:num of channels
 Calculating the energy of channel (i)
 end
2. for $j=1$:num of channels

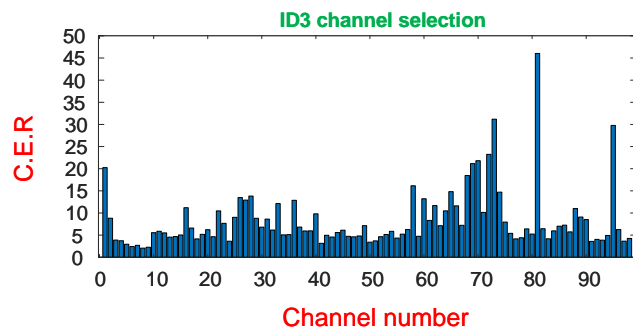
$$C.E.R(j) = \frac{\frac{\sum_{ts} Energy(channel:j)}{t_s}}{\frac{\sum_{ns} Energy(channel:j)}{t_{ns}}}$$



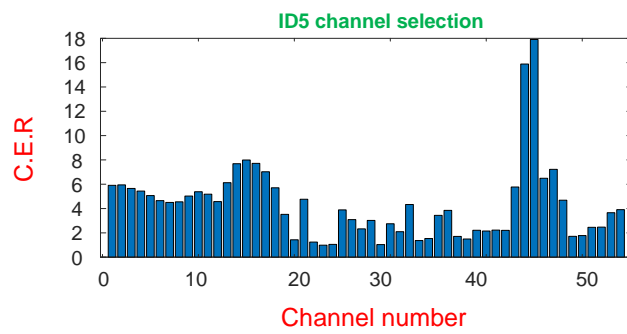
(a)



(b)



(c)



(d)

Figure 4.9: Channel energy ratio of patients (a) ID1, (b) ID2, (c) ID3, (d) ID4

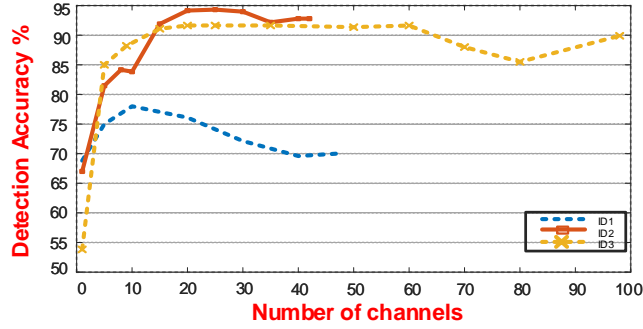


Figure 4.10: Channel selection optimization

- ```

end
3. Channle_rank <= sorting the C.E.R in descending order
4. for k=1: num of channels
 Accuracy calculation using the 1st rank to kth rank electrodes
end
5. Optimized num of channel = index(maximum(accuracy))
6. End

```

Figure. 4.10 reveals that the proposed input dimension reduction technique not only provides a considerable computational burden reduction, but it also enhances the detection accuracy compared to recording from all channels thanks to filtering out the non-informative electrodes. The number of electrodes used in data recording is dictated by the clinical setup according to the neurologist decision. That is why iEEG signals are captured via different number of electrodes.

The data reduction parameter quantifies the amount of input dimension reduction and it is given in (4.12).

$$Data\ reduction = \frac{Num\ of\ selected\ channels}{Num\ of\ total\ channels} \quad (4.12)$$

According to Figure. 4.10 and (4.12) the data reduction rate for the patients  $ID_1$ ,  $ID_2$  and  $ID_3$  are 78.2%, 40.5%, and 79.6%, respectively.

## 4.8 Hardware Implementation Experimental Results

In this section, a complete seizure detection system is formed by connecting the feature

extractor to the novel feature and channel selection units. The hardware implementations of the different blocks are illustrated in the following and the target hardware is a Cyclone V FPGA of the Terasic ALTERA DE-10-standard board. The digitized input iEEG with the 16-bit resolution is given to the seizure detector using Universal Asynchronous Receiver Transmitter (UART) serial data communication. A serial link is created between the PC and the NIOS II embedded processor of the FPGA. Thus, the data is transferred in 8-bit packets with a Baudrate of 115200.

The block diagram of the proposed seizure detector with subject-specific feature and channel selection is depicted in Figure. 4.11. The block diagram consists of the components in the training and test phases. The main motivations behind proposing this seizure detector are summarized hereafter.

- Deploying more than ten feature extraction accelerators that are personalized with respect to each patient's brain signals.
- Using an efficient feature ranking strategy
- Energy-efficient feature extraction
- Significant computational burden reduction

The training phase is carried out in an individualized manner and the outputs are tailored to each subject. It should be noted that less than half of the dataset is used in this phase to train the model. All features available in the feature pool are extracted from iEEG channels. The labeled dataset is used in the training phase and the optimized thresholds are computed in order to achieve the highest diagnostic accuracy. In addition, eleven features of the feature pool are ranked in a two-step way using the novel MDMR algorithm. Lastly, the C.E.R parameters of all electrodes are calculated and the channels' ranks are obtained. It is worth noting that the outputs of the training phase are delivered to the controller unit to be utilized in the test phase.

The data reduction, feature extractor, and controller units are implemented in the test phase. The data reduction unit selects the top-rank electrodes and filters out the irrelevant channels. Subsequently, a subset of features that includes six top-rank features are extracted in a power-efficient two-stage architecture. Finally, the controller block generates the final seizure detection label.

As an illustration, the hardware implementations of four features employed in the feature pool of the seizure detector are shown in Figure. 4.12 to Figure. 4.15. Figure. 4.12 demonstrates the extraction of the nonlinear energy feature which is computed based on (3.5) The 16-bit iEEG signal is delivered to three registers in a row. The first register is responsible for data sampling at the rate of  $clk = 512 Hz$  which is equal to the analog-to-digital conversion rate. The two following registers generate the delayed samples that are required for nonlinear energy calculation. Thereafter, two multipliers generate  $x(i)^2$  and  $x(i-1) \times x(i+1)$  signals.



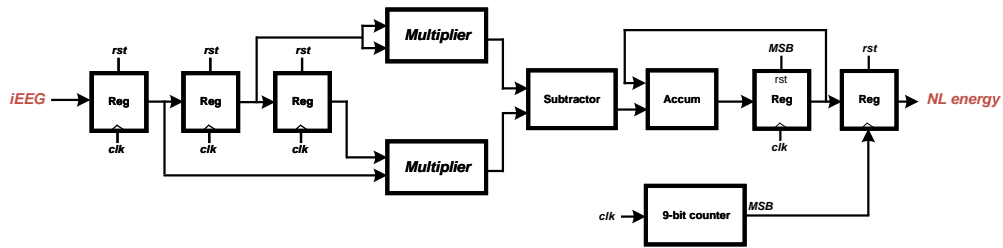


Figure 4.12: Hardware implementation of the nonlinear energy feature

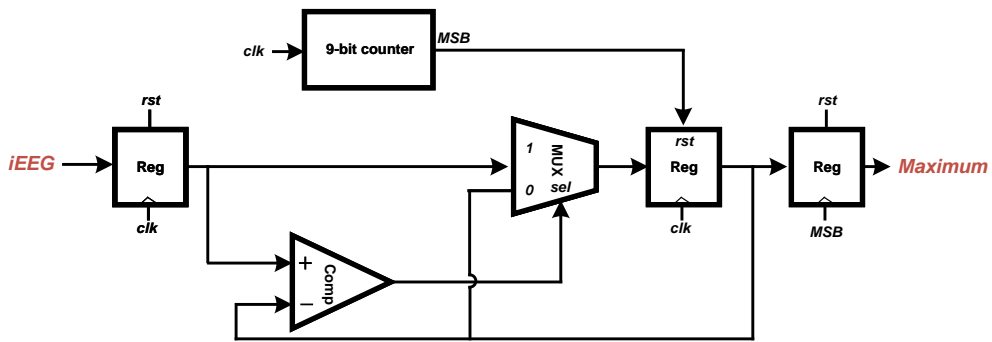


Figure 4.13: Hardware implementation of the Maximum feature

accumulated. An 8-bit right-shift block is used to divide the accumulated value by 512 and generates the average feature of the signal.

The controller unit of the seizure detector is shown in Figure. 4.11. It coordinates the operation of training and test phases and links them together. The RTL implementation of the controller is portrayed in Figure. 4.16. It receives the detection flags of the monitoring stage ( $P_1$  and  $P_2$ ). The logical *OR* gate checks whether a detection flag arrives from at least a feature from the monitoring stage. If a seizure event is detected by the monitoring stage, the controller keeps the activation signal high for nine seconds. When the activation flag arises, the feature extractors of the detection stage start working. The final detection label will be high if at least a feature from each detection stage confirms the seizure occurrence.

As previously mentioned, the hardware implementation is performed on an ALTERA CYCLONE V FPGA. The FPGA implementation details are given in Table .4.7. The design exhibits a low dynamic power of 490  $\mu$ W which is highly suitable for implantable devices with wireless power transmission systems.

The logic utilization breakdown of different feature extraction accelerators associated with the patient ID1 is given in Table. 4.8.

The top priority of the proposed two-stage feature extraction system is to conduct accurate seizure detection with a low feature dimension and energy consumption. Consequently, a new metric is defined in this thesis which indicates the feature dimension reduction level

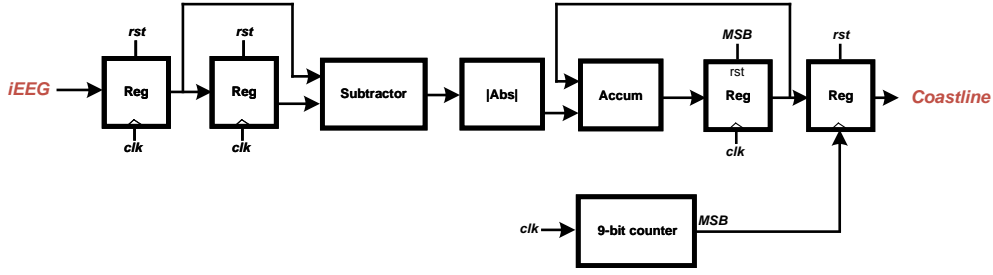


Figure 4.14: Hardware implementation of the coastline feature

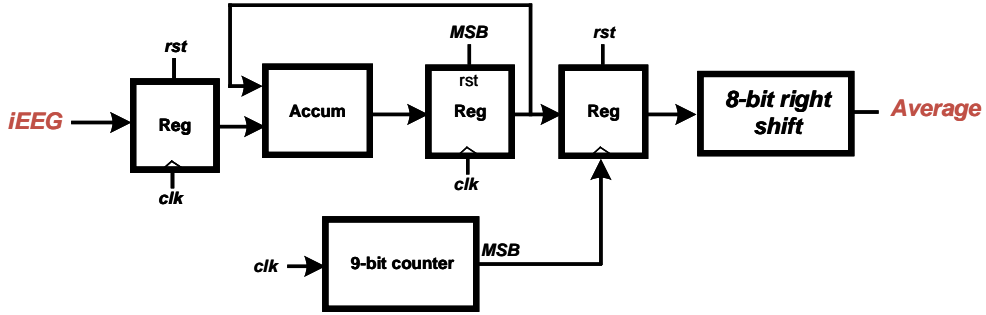


Figure 4.15: Hardware implementation of the Average feature

that is given in (4.13). The  $N_{eff}$  is the effective number of the features that are continuously extracted in the two-stage feature extraction topology.

$$N_{eff} = N_{s1} + N_{s2} \times \frac{t_{seizure}}{t_{tot}} \quad (4.13)$$

Where  $N_{s1}$  is the number of features in the monitoring stage,  $N_{s2}$  is the number of features in the detection stage, and  $t_{seizure}$  is the total duration of seizure events. The activation time and effective number of features for seven patients of the SWEC-ETHZ dataset are given in Table .4.9.

For instance, the activation time of patient ID1 is 24.5%. It denotes that the four feature extractors of the detection stage are activated only during 24.5% of the test time. Thus, the effective number of features is 2.98.

To evidence the superiority of the proposed feature selection and electrode channel selection algorithms, the experimental results of the proposed seizure detector are compared with two other models. In **Model 1**, the seizure detection is performed with the two-stage architecture and feature selection but without any channel selection. The input dimension is equal to the total number of recording electrodes.

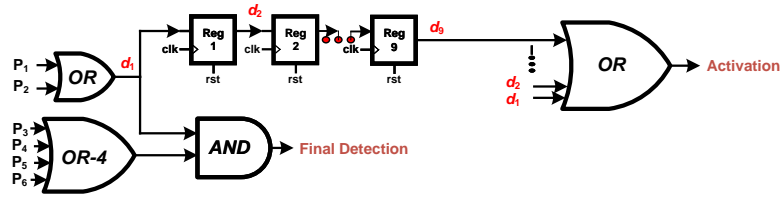


Figure 4.16: RTL implementation of the seizure detector controller

Table 4.7: FPGA details of the seizure detector with feature and channel selection

|                            |       |                          |         |
|----------------------------|-------|--------------------------|---------|
| <b>Operating frequency</b> | 4 kHz | <b>Total memory (kB)</b> | 6.92    |
| <b>Logic elements</b>      | 1856  | <b>Num of DSP blocks</b> | 5       |
| <b>Total registers</b>     | 3088  | <b>Dynamic power</b>     | 0.49 mW |

In **Model 2**, the feature ranking is conducted based on the MDMR method; however, the six top-rank features are extracted in one stage without using the proposed two-stage architecture. The test is conducted on a seizure event of the patient  $ID_1$  and the results are shown in Figure. 4.17.

The iEEG with a seizure event for patient  $ID_1$  is shown in Figure. 4.17.a. The seizure event starts at  $t = 180 \text{ sec}$  and it lasts for 72 seconds. Figure .4.17.b and Figure .4.17.d illustrate the FPGA implementations of model 1 and the proposed architecture, respectively. Comparison of two figures evidences that the 80% data dimension reduction done by the channel selection block does not degrade the detection quality. Furthermore, the detection result of the Model 2 is depicted in Figure. 4.17.c. Compared to model 2, the proposed design remarkably reduces the number of false positive detections while the effective number of extracted features is half of Model 2.

The proposed seizure detector is tested on both long-term and short-term dataset of the SWEC-ETHZ. The FPGA implementation results associated with the long-term dataset of five patients with 22 seizure events and more than 200 hours of data recordings are given in Table .4.10. It evidences the perfect sensitivity of 100% as well as great specificity for all five patients. The false alarm rate and the detection delay are also extremely low for all tested patients.

It is worth noting that several diagnostic metrics play roles in the overall performance of a seizure detector. Therefore, it is difficult to make a comparison between different designs available in the literature since most of the metrics have a complicated tradeoff with each other. Therefore, the critical seizure detection performance metrics must be considered together to evaluate the overall seizure detection performance. That is the motivation behind introducing a new Figure-of-merit (FOM) that is given in (4.14)

$$FOM_{SD} = \frac{\text{Sensitivity} \times \text{Specificity}}{\text{Delay} \times (1 - \text{Data reduction})} \quad (4.14)$$

Table 4.8: Logic utilization breakdown

| Module               | Extraction stage         | Logic utilization |
|----------------------|--------------------------|-------------------|
| Energy               | Monitoring               | 196               |
| Nonlinear energy     | Monitoring               | 188               |
| Average              | Detection                | 203               |
| Inter-quartile range | Detection stage          | 259               |
| Maximum              | Detection                | 193               |
| Range                | Detection                | 255               |
| Controller           | Monitoring and Detection | 163               |

Table 4.9: Effective number of features in the two-stage feature extractor

| Patient             | ID1  | ID2  | ID3  | ID4  | ID5  | ID6  | ID7  |
|---------------------|------|------|------|------|------|------|------|
| Activation time (%) | 24.5 | 24.9 | 17   | 28.8 | 38   | 21   | 15.7 |
| $N_{eff}$           | 2.98 | 3    | 2.67 | 3.15 | 3.52 | 2.84 | 2.63 |

The seizure detection figure-of-merit ( $FOM_{SD}$ ) incorporates the sensitivity, specificity, detection delay, and data reduction metrics. It is of paramount importance to aggregate all these parameters in a single metric to make a fair comparison between seizure detectors that are designed for wearable and implantable applications. These four metrics exhibit a challenging tradeoff in which improving one of them can intensively affect the remaining. Hence, if an improvement is achieved for a parameter in a design at the cost of sacrificing other crucial metrics, it will be reflected in the new  $FOM_{SD}$  parameter.

The proposed seizure detector is compared with recent works that are tested on the short-term iEEG of the SWEC-ETHZ dataset as well as CHB-MIT dataset. The comparison results are provided in Table. 4.11.

The proposed seizure detector achieves the perfect sensitivity of 100% as [47] and [85]. It also achieves a great sensitivity of 97.91% and a very low detection delay of 6.6 sec which outperforms the state-of-the-art. It should be noted that these results are obtained with 68% data reduction while the majority of the state-of-the-art are using all electrode channels for seizure detection and imposing an extreme computational load on processing units. Furthermore, the  $FOM_{SD}$  of this work is equal to 0.464 which is significantly better than the state-of-the-art. As a result, the proposed seizure detector with feature and channel selection techniques is highly practical for low-power resource-constraint implantable applications.

Apart from the aforementioned constructive effects of feature and electrode selections on seizure detection sensitivity, specificity and power consumption, the computational load of the seizure detector is also reduced. It contributes to faster signal processing and enables real-time applications. Thus, the proposed algorithm successfully reduces the computation time from 1551.2 sec to 7.64 sec tested on one-hour data using a Core i7 CPU [88].

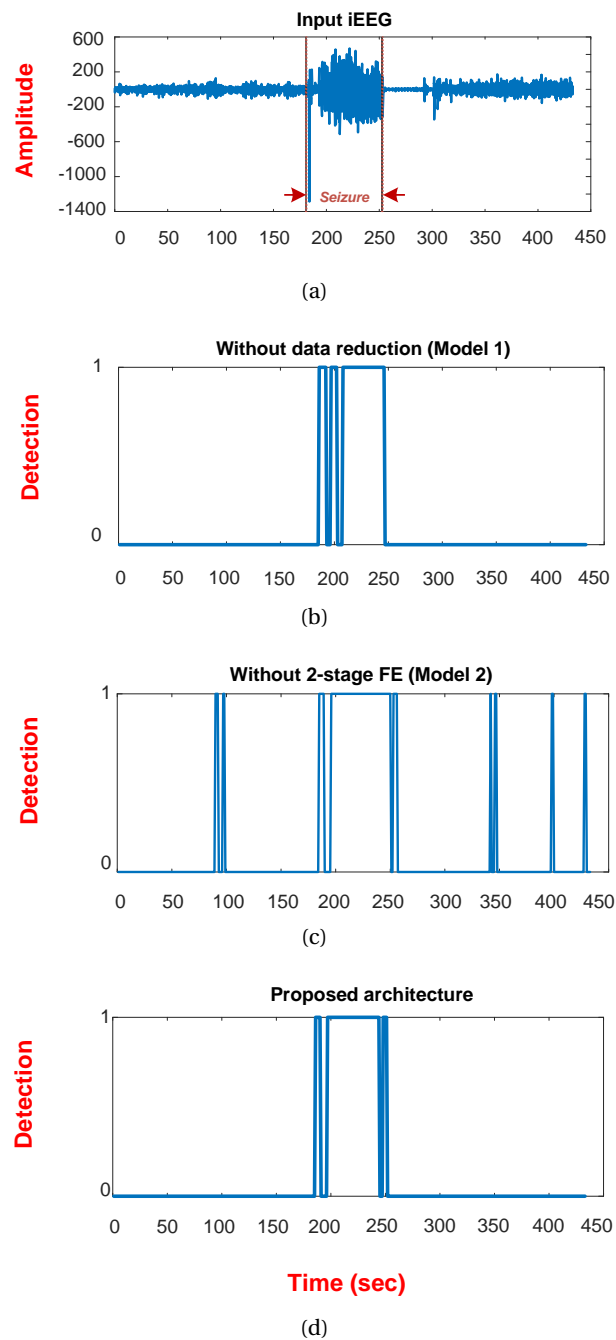


Figure 4.17: (a) iEEG signal with a seizure event, (b) Detection of Model 1, (c) Detection of Model 2, and (d) Detection of the proposed architecture

## 4.9 Computational Complexity Reduction

The computational complexity of DSP algorithms is considered as a crucial hindrance to transform the software-oriented algorithms to hardware-compatible DSP algorithms to be

Table 4.10: FPGA results on the long-term dataset

| Patient No.               | ID1    | ID2    | ID3    | ID4  | ID5   |
|---------------------------|--------|--------|--------|------|-------|
| <b>Sensitivity (%)</b>    | 100    | 100    | 100    | 100  | 100   |
| <b>Specificity %</b>      | 99.84% | 99.95% | 99.78% | 96%  | 98.2% |
| <b>False alarm/hour</b>   | 0.132  | 0.085  | 0.075  | 0.22 | 0.131 |
| <b>Delay (sec)</b>        | 3.8    | 21     | 5      | 6.5  | 4.8   |
| <b>Dynamic power (mW)</b> | 0.76   | 0.6    | 0.72   | 0.59 | 0.56  |

Table 4.11: Comparison with the state-of-the-art

|                                   | [73]   | [47]  | [70]   | [85] | [86]    | [87]    | This work |
|-----------------------------------|--------|-------|--------|------|---------|---------|-----------|
| <b>Dataset</b>                    | ETHZ   | ETHZ  | ETHZ   | ETHZ | CHB-MIT | CHB-MIT | ETHZ      |
| <b>Sensitivity</b>                | 95.21% | 100%  | 96.67% | 100% | 94.44%  | 95.51%  | 100%      |
| <b>Specificity</b>                | 94.54% | 88.5% | 92.4%  | -    | -       | 80.1%   | 97.91%    |
| <b>Delay (sec)</b>                | 15.8   | 7.8   | 8.2    | -    | -       | -       | 6.6       |
| <b>Data reduction</b>             | 0%     | 0%    | 0%     | 93%  | 0%      | 0%      | 68%       |
| <b>Hardware</b>                   | -      | FPGA  | -      | ASIC | FPGA    | FPGA    | FPGA      |
| <b>Power (<math>\mu W</math>)</b> | -      | 510   | -      | 13.6 | 2697.8  | 110     | 490       |
| <b>FoM</b>                        | 0.057  | 0.11  | 0.109  | -    | -       | -       | 0.464     |

used in portable seizure detectors. Applying computational complexity reduction techniques is an essential step in seizure detection when a complex DSP algorithm should be implemented on a hardware with low power budget.

Computational complexity reduction offers several merits in portable seizure detectors that are summarized hereunder.

1. Power consumption reduction
2. Processing time reduction
3. Real-time operation
4. Area occupation optimization
5. Logic and register usage optimization
6. Memory usage optimization

The concept of computational complexity reduction for portable seizure detectors originates from reducing the dimension of the features and electrode channels as much as possible while the detection performance is not adversely affected. Various feature selection and channel selection methods can be found in the literature of wearable/implantable seizure detectors [88–90]. Nonetheless, the feature selection and channel selection approaches do not operate coordinately and they are following totally different algorithms. It has been proven

that the coordination between channel dimension reduction and feature dimension reduction is required to achieve a remarkable computational complexity reduction in conjunction with diagnostic accuracy enhancement [17].

Authors in [89] employed both channel and feature selection approaches for computational complexity reduction. The mutual information is calculated and the channels are sorted based on that parameter. In addition, a supervised method of feature selection using the RF classifier and nonlinear SVM classifiers is employed. Indeed, the channel and feature selection methods used in [89] are not following the same criteria.

Authors in [90] achieved a significant input dimension reduction by reducing the channel dimension to 1. The computational complexity of [78] is still high in order to be adapted to portable seizure detectors since the feature dimension is high. The feature extraction is performed by converting the signal from time to frequency domain. Time to frequency domain conversion is done using Empirical Mode Decomposition (EMD) and DWT techniques. Four features are extracted from different frequency domains. Thus, the feature dimension reduction is not taken into account in [90].

[88] reduces the computational complexity by employing both channel and feature selection methods. The variance feature of each channel is computed during the offline training phases and the channels are ranked according to their variance features. Furthermore, the feature selection is conducted using the EMD technique. However, this work suffers from proper coordination between the feature and channel selection methods.

This thesis aims at proposing an advanced subject-customized channel and feature selection methods to achieve the maximum computational complexity reduction while the detection accuracy is preserved at a high level. This target can be reached by proposing a correlated technique for channel and feature selection. In the channel selection part, a criterion is applied to convert all electrode channels to a single compressed channel. Using a single compressed channel enables the maximum computational complexity reduction rate since the features are only extracted from a single compressed channel. In the feature selection part, we aim to include a variety of features in the feature pool and filter out more than 50% of the features using the feature selection algorithm. The main novelty of this approach is proposing a coherent feature and channel selection techniques which operate coordinately.

#### **4.9.1 Feature Dimension for Computational Complexity Reduction**

The number of features that are extracted in the digital signal processing unit of the seizure detector is a crucial factor in the computational complexity of the system. Nine statistical low-complexity time-domain features are included in the feature pool. 1) Line length, 2) Minimum, 3) Maximum, 4) Energy, 5) Nonlinear energy, 6) Variance, 7) Range, 8) Correlation, and 9) Average features.

As the iEEG is recorded via tens of electrodes, extracting all nine features from all electrode

channels imposes a huge computational burden on the signal processing unit that is extremely undesirable for portable seizure detectors. Thus, the goal of this section is to filter out more than 50% of the features in the feature pool in a patient-customized way and keep the four discriminating top features.

The feature ranking is carried out based on feature scores which demonstrate to what extent the features are discriminating when a seizure onset takes place. The features are categorized into amplitude-based features (Line length, Minimum, Maximum, Correlation, Average, and Range), and amplitude-square-based features (Energy, Nonlinear energy, Variance). The feature scores associated with amplitude-based and amplitude-square-based features are defined in (4.15) and (4.16), consecutively.

$$Feature\ score(i) = \frac{\frac{\sum_{t_{sz}} F_i}{t_{sz}}}{\frac{\sum_{t_n} F_i}{t_n}} \quad (4.15)$$

$$Feature\ score(j) = \sqrt{\frac{\frac{\sum_{t_{sz}} F_j}{t_{sz}}}{\frac{\sum_{t_n} F_j}{t_n}}} \quad (4.16)$$

Where  $F_i$  is the amplitude-based feature,  $F_j$  is the amplitude-square-based feature,  $t_{sz}$  is the seizure duration, and  $t_n$  is the non-ictal state duration. A feature with high a feature score is considered as an ideal candidate for the seizure detection task since it develops the most significant fluctuation upon seizure events. Thus, the features are ranked according to their corresponding feature scores and the top four-rank features are selected to be extracted in the test phase.

Furthermore, the proposed feature ranking algorithm enables an outstanding feature dimension reduction from nine to four which has a considerable effect on the computational complexity of the algorithm.

To demonstrate the computation complexity reduction offered by the proposed technique, the algorithm is tested on seven patients from the Bern University hospital database. Figure. 4.18 demonstrates the execution time of the feature extraction unit without and with the proposed feature dimension reduction technique.

The computation time reduction realized by the proposed feature dimension reduction technique is observable in Figure. 4.18. Execution time reduction enables real-time operation of wearable/implantable devices. Figure. 4.18 depicts different level of execution time reduction tested on different patients. The reason is that the feature subset selection is performed in a subject-customized way. Therefore, the complexity of available features in the feature subset determines execution time reduction.

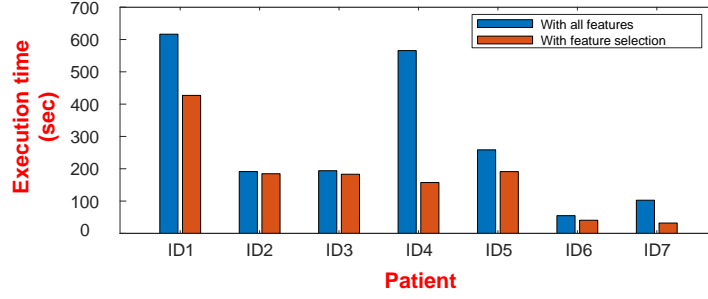


Figure 4.18: Effect of the feature selection on the code execution time

#### 4.9.2 Electrode Channel Dimension Reduction

Another important factor, which strongly influences the computational complexity of the seizure detector, is the dimension of the electrode channels. In general, high resolution recording systems consist of more than thirty electrode channels to provide sufficient spatial coverage of the cerebral cortex [80]. Furthermore, not only does the channel dimension reduction decrease the computational load, but it also ameliorates the seizure detection accuracy by eliminating the non-focal redundant channels.

The main focus of this section is to present a channel dimension reduction that is correlated to the feature dimension reduction unit. As a consequence, the channel ranking is performed based on the top four-rank features that are the outputs of the feature dimension reduction unit. A two-dimensional channel score is defined for each channel according to the top-four rank features. The channel scores indicate to what extent the channels are discriminating in extracting the top four-rank features. The channel score metric is calculated in (4.17).

$$Channel\ score(n, k) = \frac{\frac{\sum_{t_{sz}} F_k(n)}{t_{sz}}}{\frac{\sum_{t_n} F_k(n)}{t_n}} \quad (4.17)$$

Where (n) is the channel number, (k) is the feature index, and ( $F_k$ ) is the feature of the  $k^{th}$  top rank feature. There are four scores associated with each channel and the final score of a channel is computed by averaging all four values. As an illustration, the channel scores of the patient  $ID_1$  from the SWEC-ETHZ dataset are shown in Figure. 4.19.

The nonlinear energy, energy, variance, and average features obtained the highest feature scores during the feature ranking process of the patient  $ID_1$ . Figure. 4.19 shows that the features with the higher ranks are more powerful metrics to select the discriminating channels since the channel score differences are greater between informative and non-informative channels using the top-rank features. That is why proposing a channel selection method correlated to the feature ranking unit is of paramount importance.

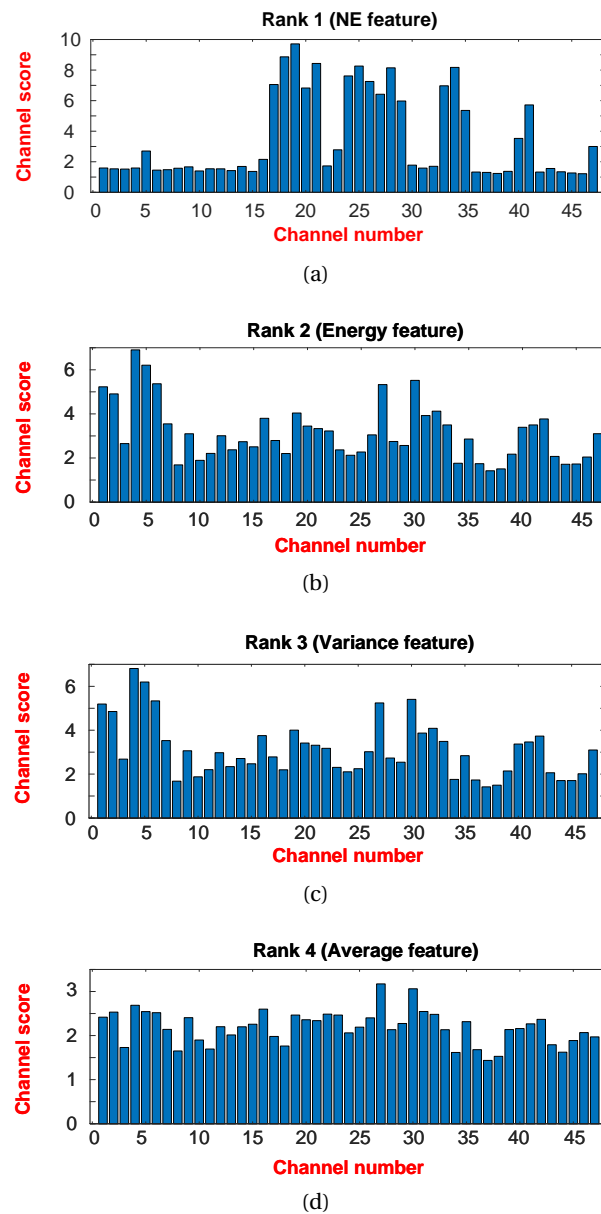


Figure 4.19: Channel scores of (a) the top-rank feature, (b) the second rank feature (c) the third rank feature, and (d) the fourth rank feature

Selection of the top-rank electrode channels is executed when they are ranked according to their channel scores. The optimized number of top rank channels which contribute to the highest detection accuracy is determined in a patient-specific way. Figure. 4.20 depicts the detection accuracy plot versus the number of selected channels.

The detection accuracy of three patients ( $ID_1$ ,  $ID_2$ , and  $ID_3$ ) versus the number of channels, which is selected from the top-rank channels, is shown in Figure. 4.20. It discloses the fact that using all electrode channels with a huge computational load does not always lead to better

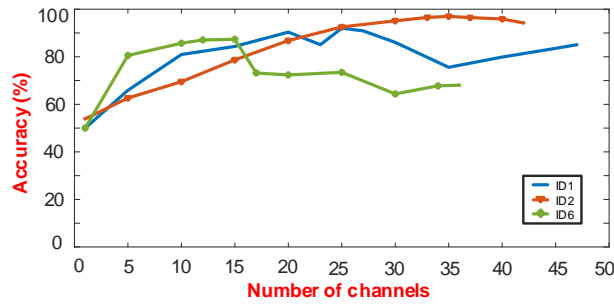


Figure 4.20: Detection accuracy with respect to the number of selected channels

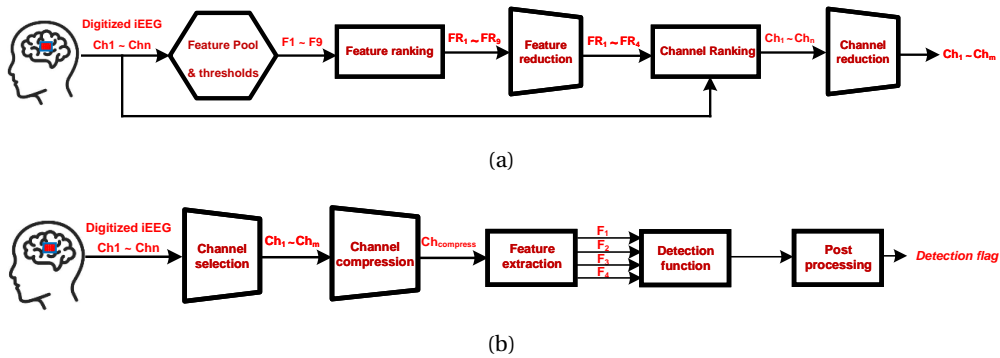


Figure 4.21: Block diagram of the seizure detector with reduced computational complexity

seizure detection. It also reveals that the highest detection accuracy occurs when the features are extracted from a fewer selected channels rather than all recording channels. Thus, the proposed channel ranking method is efficient enough to reduce the computational load in conjunction with accuracy improvement. To achieve the highest possible channel dimension reduction level, the selected channels are averaged and a single compressed channel of iEEG is delivered to the feature extraction unit.

### 4.9.3 Seizure detection with reduced feature and channel dimensions

Feature and channel dimension reduction techniques have been developed in the previous section. In this section, a complete seizure detection system is constituted by connecting the feature dimension reduction unit to the channel dimension reduction unit. The topology of the proposed system is shown in Figure. 4.21.

The training phase is shown in Figure. 4.21.a. All nine features and their corresponding thresholds are extracted in the feature pool. Then, the features are ranked based on the feature scores that are given in (4.15) and (4.16). The top four-rank features are chosen and delivered to the channel ranking unit. The channels are ranked according to the channel scores that are calculated in (4.17), and the top-rank channels are selected as shown in Figure. 4.20.

In the test phase, all electrodes channels are delivered to the channel selection unit and the

Table 4.12: Comparison with the state-of-the-art

|                  | Sensitivity (%) | Specificity (%) | Delay (sec) | <i>C.D</i> |
|------------------|-----------------|-----------------|-------------|------------|
| [80]             | 97.08           | 89.98           | 12.56       | 65.14      |
| [28]             | 94.03           | 88.84           | 13.4        | 65.14      |
| [47]             | 100             | 92.1            | 7.8         | 87.7       |
| [70]             | 96.66           | 92.37           | 8.1         | 223        |
| <b>This work</b> | 100             | 92.98           | 3.6         | 4          |

selected channels are averaged in the channel compression block. Subsequently, a single compressed channel of iEEG is delivered to the feature extractor. Four top-rank features are extracted. The detection function block employs a majority function to generate detection flags from the extracted features. Eventually, a 3-second post-processing block is utilized to smooth the detection flag signals and reduce the number of false positive detections.

A new metric that is called *Computational Dimension* (*C.D*) is defined in this thesis to make a comparison between the proposed design and the state-of-the-art in terms of computational dimension and complexity. The computational dimension metric is the product of the feature dimension and the channel dimension as given in (4.18).

$$C.D = \text{Feature dimension} \times \text{Channel dimension} \quad (4.18)$$

The computational dimension of this work is  $4 \times 1$  since the four top-rank features are extracted from a single compressed channel. The proposed low computational complexity seizure detector is tested on seven patients from the SWEC-ETHZ dataset to evaluate its seizure detection performance. Furthermore, the results are compared with the state-of-the-art that uses the same iEEG dataset. The comparison results are given in Table. 4.12.

Table. 4.12 reveals the outstanding performance of the presented seizure detector compared to the state-of-the-art. The design obtains an excellent sensitivity of 100% as [47] which is better than the rest. Also, the specificity, which represents the false alarm rate, is the best among the state-of-the-art. The detection delay is remarkably lower than the state-of-the-art. Notably, all these improvements are obtained when the feature and channel dimensions are considerably reduced. We reached a very low computational dimension of 4 which is remarkably lower than the computational dimension of the state-of-the-art.

## 4.10 Machine-Learning-Based Classification

In this section, epileptic seizure detection using the RF and SVM classifiers is studied. Low-complexity time-domain features are given as the input of the classifiers to find a high-performance classifier that is suitable for hardware implementation.

The SVM and RF classifiers are commonly used in the literature of seizure detection [91–95]. [91], [92] and [93] use the SVM classifier trained by time-domain features. Although they reach an acceptable specificity, their algorithms suffer from high seizure detection latency. Authors in [94] and [95] achieve a seizure detection latency improvement using an RF classifier.

The goal of this section is to implement a machine-learning-based seizure detection using RF and SVM classifiers which are trained by time domain features.

#### 4.10.1 Seizure detection by the RF classifier

The Random forest is an ensemble learning method that is an extension of the decision tree algorithm. A decision tree consists of several decision and leaf nodes. It is a hierarchical model that recursively splits data to form a tree-like structure. A decision is made in each node based on a feature threshold. In addition, leaf nodes represent the class labels of the trees [96].

The RF classifier incorporates several decision trees to form a robust classification model. The RF classification is performed in three steps that are described hereunder.

1. **Bootstrapped samples generation:** Bootstrap samples are subsets of the entire data which are randomly generated from the training data. Each bootstrap sample is used to train a decision tree of the random forest.
2. **Random feature selection:** A random subset of features is chosen to be used in each decision tree. It offers many advantages to the random forest classification since it introduces diversity and reduces the correlation between different trees in the ensemble model.
3. **Ensemble classification:** The final prediction of the random forest model relies on the majority voting between the prediction labels of the trees.

Compared to other classification methods, the RF classifier offers some advantages that are summarized hereafter.

- **High accuracy:** Multiple decision nodes are available in each tree. In addition, the predictions from more than one decision tree introduce variance and mitigate the overfitting.
- **Robustness to irregular data:** The majority voting is applied on the prediction label of all trees. Therefore, the effect of outliers on the final prediction label is considerably reduced.
- **Feature importance:** The RF classifier gives a metric that is called feature importance. It indicates to what extent a feature contributes to accurate predictions. It also reduces the dimensionality of the features.

The main drawback of the RF classification originates from its hardware implementation

Table 4.13: Classifiers comparison results

| Patient<br>Classifier | ID1  |      | ID2  |      | ID3  |      |
|-----------------------|------|------|------|------|------|------|
|                       | RF   | SVM  | RF   | SVM  | RF   | SVM  |
| <b>AUC</b>            | 0.88 | 0.15 | 0.98 | 0.92 | 0.96 | 0.87 |
| <b>Sensitivity</b>    | 1    | 1    | 1    | 1    | 1    | 1    |
| <b>Specificity</b>    | 0.94 | 0.95 | 0.94 | 0.89 | 0.96 | 0.99 |
| <b>Accuracy</b>       | 0.6  | 0.58 | 0.97 | 0.94 | 0.95 | 0.95 |
| <b>Delay (sec)</b>    | 3.3  | 12   | 0    | 0    | 3    | 4    |

compatibility. The hardware implementation of the RF classifier is quite memory-intensive and requires computational resources that are not compatible with implantable/wearable applications.

In this section, we aim to modify the hyperparameters of an RF classifier to make it suitable for the hardware implementation of low-power IMDs.

#### 4.10.2 FPGA Implementation of the RF Classifier

Time-domain features have already demonstrated the lowest hardware implementation complexity [14, 85]. A comparison between the RF and SVM classifiers is done to disclose which classifier can yield a better classification performance using time-domain features. Four metrics are considered for the comparison and tested on three patients from the SWEC-ETHZ dataset. The comparison results are given in Table. 4.13.

The comparison is done with respect to the area under the curve (AUC) of the receiver operating characteristics (ROC). This metric shows how a classifier is accurate versus the variation in the thresholds. The AUC of the RF classifier is better than the SVM for all three patients. Both classifiers obtain 100% sensitivity. Their specificities are close to each other while the detection delay of the RF classifier is better than the SVM.

Thus, the RF classifier is chosen for the hardware implementation due to its superiority over the SVM. The architecture of the RF classifier is depicted in Figure. 4.22. The classifier comprises (n) decision trees and the prediction labels are delivered to a majority function to generate the final prediction label.

The RF classifier involves two random aspects that are explained hereafter.

1. Each tree is trained with bootstrap samples which are randomly selected from the training data
2. A random subset of features is used in the splits of each tree

The out-of-bag samples are used in order to evaluate the performance of the RF classifier and optimize the hyperparameters. During the training phase, the classifier is trained using 11

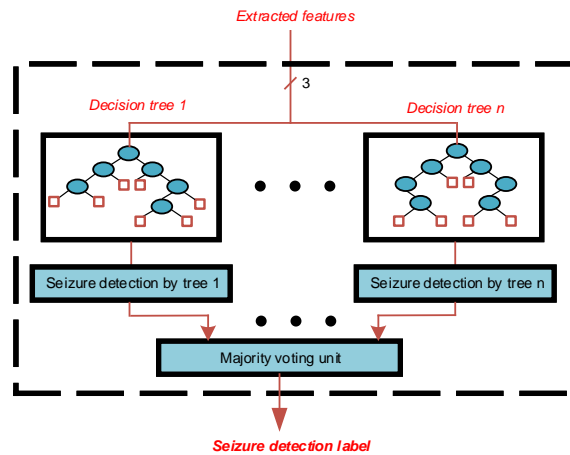


Figure 4.22: Topology of the RF classifier

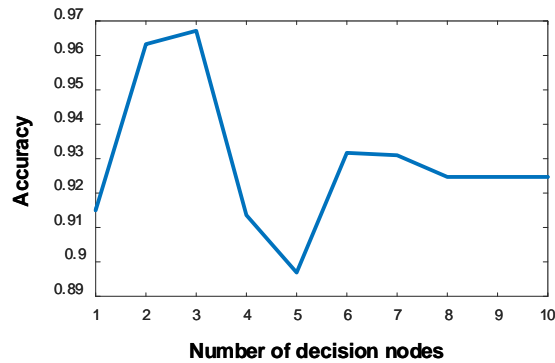


Figure 4.23: Decision nodes optimization

time-domain features. According to the feature's importance metric, the Coastline, Variance, and Range features are selected to avoid overfitting the model.

The number of trees and the depth of trees are two substantial hyperparameters that need to be optimized for hardware implementation. The depth of trees indicates the number of decision nodes in each tree. There is a tradeoff between detection accuracy and overfitting in finding the optimal number of decision nodes. If there are few decision nodes, the final prediction label is not accurate. On the other hand, using several decision nodes force the model to learn from irrelevant data and noises which degrades the accuracy. The optimization of the number of decision nodes is depicted in Figure. 4.23.

The optimal number of decision nodes is three according to Figure. 4.23. Increasing the number of decision nodes from one to three helps the model to understand the patterns better and leads to higher accuracy. As the number of nodes increases from three to five, the accuracy deteriorates because more detailed information is extracted that contributes to the overfitting. Moreover, the accuracy of the model is stabilized when the number of nodes surpasses six.

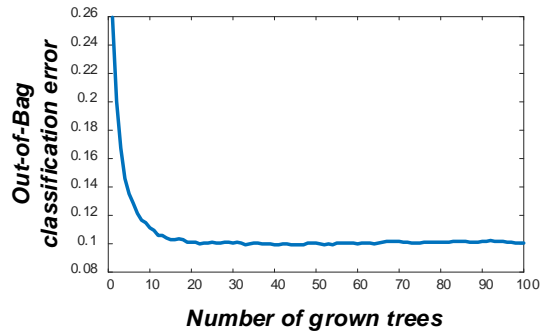


Figure 4.24: Number of trees optimization

Table 4.14: FPGA implementation of the RF classifier

|                            |      |                      |         |
|----------------------------|------|----------------------|---------|
| <b>Operating frequency</b> | 512  | <b>Memory (Kb)</b>   | 232.115 |
| <b>Logic elements</b>      | 1475 | <b>DSP blocks</b>    | 4       |
| <b>Num of Registers</b>    | 2297 | <b>Dynamic power</b> | 0.59 mW |

The number of trees in the ensemble should be high enough to provide sufficient accuracy. However, the hardware implementation of the classifier encounters resource constraints as the number of trees increases. The optimization of the number of trees in the ensemble is shown in Figure. 4.24.

It is evident that increasing the number of trees in the ensemble reduces the out-of-bag classification error. The optimal number of trees is 20 according to the Figure. 4.24. Nevertheless, a tradeoff exists between accuracy and hardware resources. Therefore, five decision trees are considered to be implemented on the hardware. 75% hardware resource saving is achieved by using five decision trees at the cost of increasing the classification error from 0.1 to 0.125 which is still within the acceptable range.

Thus, the optimization of the RF classifier results in extracting the coastline, variance and range features from five decision trees with a depth of three. The ROCs of the optimized RF classifier for three patients are illustrated in Figure. 4.25.

The seizure detector with machine-learning-based RF classifier is implemented on a CYCLONE V FPGA of Terasic DE10-standard board and tested on six patients from the SWEC-ETHZ dataset. The FPGA implementation parameters are given in Table. 4.14.

The experiment results of six patients are given in Table. 4.15. The model reaches 100% sensitivity tested on all six patients. A significant specificity of over 95% is reached for all patients. Moreover, the average power consumption of all patients is 0.59 mW which is low enough to be used in portable seizure detection applications.

The FPGA implementation results of six patients are compared with the state-of-the-art that have used the RF classifier for seizure detection. The comparison results are given in Table

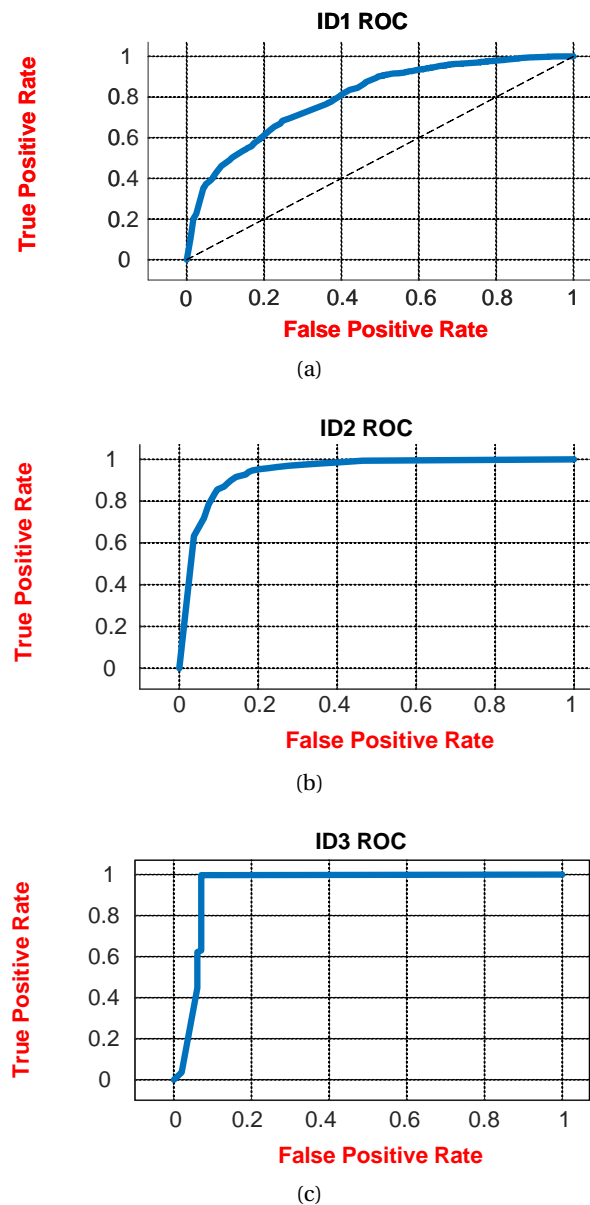


Figure 4.25: Receiver operating characteristics of patient (1) ID1, (2) ID2, and (3) ID3

.4.16

Compared to the state-of-the-art, this work reaches an excellent sensitivity as [95] which is better than [28]. In addition, this work outperforms the state-of-the-art in all other metrics including specificity, accuracy, and delay. It should be noted that the results of this work are experimental results of FPGA implementation while [28] and [95] report the software simulation results.

Table 4.15: FPGA implementation of the RF classifier

| Patient | Sensitivity % | Specificity % | Accuracy % | Delay (sec) | Power (mW) |
|---------|---------------|---------------|------------|-------------|------------|
| ID1     | 100           | 95.21         | 97.6       | 11          | 0.6        |
| ID2     | 100           | 98.61         | 99.31      | 0           | 0.58       |
| ID3     | 100           | 99.72         | 99.86      | 3           | 0.6        |
| ID4     | 100           | 95.14         | 97.57      | 5.5         | 0.61       |
| ID5     | 100           | 97.78         | 98.89      | 12          | 0.58       |
| ID6     | 100           | 97.5          | 98.75      | 2           | 0.59       |

Table 4.16: Comparison with the state-of-the-art using the RF classifier

|                    | [28]      | [95]  | <b>This work</b> |
|--------------------|-----------|-------|------------------|
| <b>Dataset</b>     | SWEC-ETHZ | [95]  | SWEC-ETHZ        |
| <b>Hardware</b>    | No        | No    | Yes (FPGA)       |
| <b>Sensitivity</b> | 94.94     | 100   | 100              |
| <b>Specificity</b> | 95.53     | 94.16 | 95.57            |
| <b>Accuracy</b>    | 95.24     | 97.08 | 97.78            |
| <b>Delay (sec)</b> | 15.09     | 17.03 | 6.1              |
| <b>Power (mW)</b>  | n.a       | n.a   | 0.59             |

## 4.11 Summary and Conclusions

In this chapter, the hardware implementations of various signal processing algorithms which are compatible with low-power implantable devices are discussed. Researchers have encountered several challenges concerning designing energy-efficient accurate seizure detectors for low-power implantable/wearable applications. This chapter proposed novel and effective solutions to address the following points.

1. Energy-efficient feature extraction
2. Feature ranking and selection
3. Electrode channel ranking and selection
4. Computational complexity of the algorithms for the real-time hardware implementation
5. Hardware implementation of machine-learning-based algorithms

We described the necessity of extracting various types of features to enable patient-specific accurate seizure detection. The crucial impediment of extracting multiple features is power consumption. A novel solution is proposed in this chapter in which the features are extracted using a two-stage architecture. In the proposed approach, only a small subset of features is continuously extracted in the monitoring stage. The detection stage of the seizure detector which extracts the majority of the features is temporarily activated by a controller upon seizure

detection of the monitoring stage. The hardware compatibility of the design is validated by the FPGA implementation. The design consumes a very low dynamic power of  $105 \mu W$  that is highly compatible with the implants. The DAR of the two-stage feature extractor is measured 0.272 which means that the majority of features are not extracted during 72.8% of the experiment which can contribute to considerable energy saving. The two-stage feature extractor achieves 100% sensitivity and 92.1% specificity.

A novel feature ranking algorithm that is called MDMR was suggested in this chapter. It can effectively identify the most discriminative channels according to the FDP and filter out the redundant non-informative channels based on the mutual information.

A novel patient-specific channel selection method was proposed in this chapter to enable energy-efficient digital signal processing on iEEG signals recorded from tens of electrodes. The proposed method ranks the channels based on the C.E.R metric. Furthermore, the seizure detector using the novel feature and channel ranking approaches was implemented on an FPGA which evidenced an excellent sensitivity of 100% with a low detection delay of 6.6 seconds. It demonstrated that the  $N_{eff}$  is equal to 2.98 while eleven features are included in the feature pool. Moreover, the  $FoM_{SD}$  of the design is 0.464 which is outstandingly better than the state-of-the-art. It proves the compatibility of the design for energy-efficient seizure detection implants.

The challenge of digital signal processing from high resolution iEEG signals was tackled in this chapter to reduce the computational complexity of the design. We develop a channel dimension reduction technique that is correlated to the feature dimension reduction unit. It was demonstrated that the coordination between channel and feature dimension reduction methods contributes to not only remarkable computational complexity reduction but also precise seizure detection. More than 50% of features are filtered out and the selected channels are compressed into a single channel. We achieved a  $C.D$  equal to 4 with a very low seizure detection latency of 3.6 sec which considerably outperforms the state-of-the-art.

Lastly, the challenge of hardware implementation of machine-learning-based classifiers for low-power resource-constraint implantable applications was successfully tackled. RF classifiers have demonstrated high seizure detection sensitivity in the literature. Nonetheless, their compatibility with portable applications was not examined in the recently published works. We designed an RF classifier with optimized hyperparameters for low-power implants. The number of trees in the ensemble as well as the number of splits in each tree was reduced to enable hardware implementation on the FPGA while the seizure detection performance was not affected. The FPGA implementation results revealed a power consumption of  $590 \mu W$  that is within the acceptable range for low-power implants. Furthermore, the seizure detection accuracy of the design is 97.78% which exhibits superiority over the recently published papers.



# 5 Programmable Seizure Detection with User Interactions

## 5.1 Introduction and Motivations

User interaction and programmability are two important factors that have not been considered in the literature on epileptic seizure detectors. Although available seizure detectors have demonstrated their capability to accurately detect seizures tested on tens of hours of iEEG data of patients, the patient's condition and their iEEG patterns evolve over time. Therefore, if an algorithm yields an acceptable seizure detection performance during the first year of using the implant, it may fail to preserve the same accuracy after two or three years. As a consequence, another brain surgery is needed to place a new device that is adapted to the current condition of the patient. That is highly unfavorable for epileptic patients since it involves the risk of undergoing another brain surgery as well as additional costs of the new implant and hospitalization [97].

Furthermore, the available seizure detectors lack interaction between patients and IMDs. This interaction is of paramount importance and offers several merits that are mentioned hereunder.

- **Patient safety:** A critical consideration in designing medical devices is to guarantee the safety of patients. If patients can adjust the settings of their medical devices according to their current activities, it can reduce the risk of uncontrollable seizures during activities that can endanger the patients' lives.
- **Patient empowerment:** Patients will feel more empowered if they understand the operation of their implant and dynamically interact with the device. In this case, patients are engaged in the therapy and their well-being will improve.

- **Real-time feedback:** Delivering real-time feedback is another advantage of the patient-implant interaction. For instance, adjusting stimulation parameters based on real-time feedback of patients will assist the device to reach the therapeutic goal.
- **Customization:** Customization of an implant settings according to patient interactions can alter the default parameters of an implant to make it suitable for the current needs and conditions of the patient.
- **Reducing anxiety:** Medical devices often evoke anxiety in patients. The anxiety stems from lack of patients knowledge related to device's functionalities. Interaction of patients with the implant can alleviate this concern.
- **Therapy compliance:** Patients are more likely to adhere to treatments when they have interaction with medical devices. Thus, they feel more responsible to play a constructive role in the proper operation of the medical device.

In this chapter, we shed light on two special aspects of programmability and user interaction in seizure detection. These two aspects can make a breakthrough in the performance improvement of ordinary seizure detectors. A 32-bit RISC microprocessor is designed to be used in the implant to enable the programmability attribute. Thus, the physician can define different seizure detection therapy programs for a specific patient. Each program could be useful under certain circumstances. Therefore, patients can constructively interact with the implant to determine the appropriate seizure detection therapy with respect to their daily activity or the severity of seizures.

A novel classification approach based on patient-specific logical classification functions is proposed in this chapter. The novel classification algorithm is highly compatible with the programmability attribute of the implant presented in this thesis. Therefore, the classification of the seizures will be performed according to the user's command which tailors the device to specific needs of patients.

## 5.2 Framework of a Programmable Seizure Detector

We introduce programmability as a special characteristic of seizure detectors in this thesis. It can enable physicians and patients to have continuous interactions with the implant. In this work, a 32-bit RISC microprocessor is employed with an instruction set that is tailored to the seizure detection application. Programmable seizure detection gives the opportunity to neurologists to alter therapy programs of patients without any need for hardware change and replacement surgery.

The topology of the proposed programmable seizure detector is illustrated in Figure. 5.1. The system comprises a 32-bit RISC processor, a feature extraction unit, a feature ranking unit, a feature selection unit, and a DSP core. Multiple time-domain features are extracted in the feature pool. Then, the most informative features are selected by a feature ranking strategy.

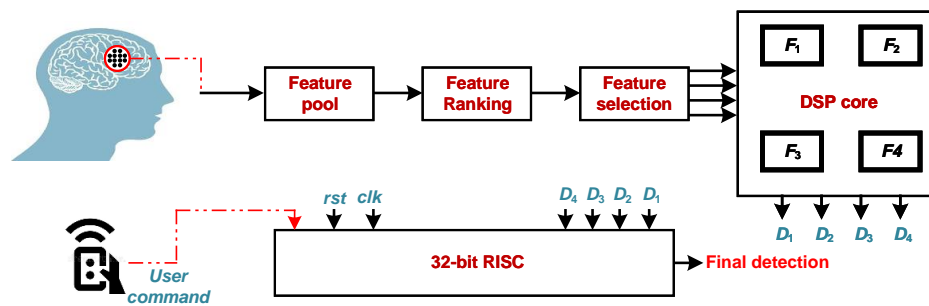


Figure 5.1: Block diagram of the programmable seizure detector

The selected features are extracted in the DSP core of the system. The outputs of the DSP unit are delivered to the 32-bit RISC microprocessor. The RISC executes the tasks that are already programmed by a neurologist. The outputs of the DSP core are analyzed according to therapy programs. More importantly, the patient can interact with the device and play a significant role in the seizure detection process. Patients can switch between different therapies and modify the seizure detection parameters under the permission of their physicians. The operation of different blocks in the programmable seizure detector is explained in the following.

### 5.3 RISC Microprocessor Design for Seizure Detection

The RISC is a type of microprocessor architecture that utilizes a compact and optimized set of instructions. It is an alternative to the Complex Instruction Set Computer (CISC). The RISC architectures are designed to prioritize efficiency and performance, making them well-suited for low-power application specific purposes. [98].

The instructions of the RISC perform less but the execution time is much faster. The RISC microprocessor emphasizes on simplicity and efficiency in its design. A small number of simple and well-defined instructions are included in the instruction set of the RISC. The instructions are executed in a single cycle. It is worth noting that the primary purpose of the RISC is to optimize the execution of instructions by minimizing the complexity of instructions as well as maximizing the speed of execution.

Key features of RISC processors are provided hereunder.

1. **Simple instructions:** The instruction set of RISC processors incorporates a small set of basic instructions.
2. **Load/store architecture:** Data are loaded from memory to registers to perform arithmetic and logical operations and the results are stored back to memory from the register file. It reduces the complexity of instruction execution.
3. **Single-cycle execution:** RISC aims to execute most of the instructions in a single cycle.

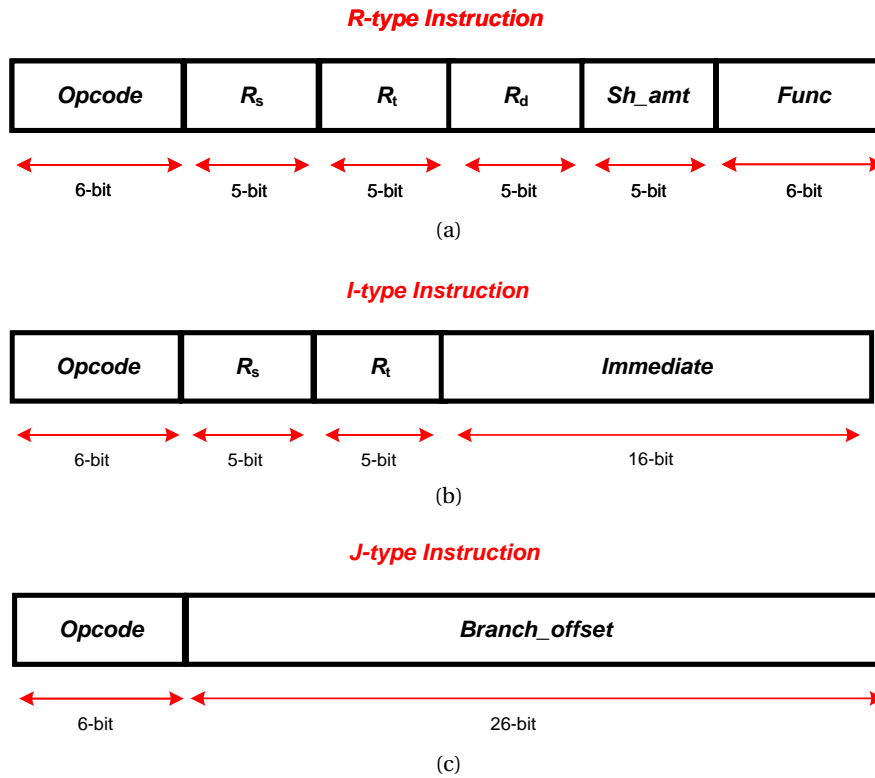


Figure 5.2: (a) R-Type instruction format, (b) I-Type instruction format, (c) J-Type instruction format

4. **Register usage:** Since the execution of instructions is simpler, the Central Processing Unit (CPU) uses less area. Therefore, more General Purpose Register (GPR)s can be employed to store frequently used data. It accelerates the execution process.
5. **Pipelining:** Many RISC architectures utilize the pipelining technique. In pipelining, the instructions are broken down into different stages which allows processing multiple instructions simultaneously. This technique improves the throughput of the processor.
6. **Reduced memory access:** More registers are used in RISC architectures compared to the CISC which reduces the need for frequent memory access. Hence, the speed of instruction execution is increased.

The Advanced RISC Machine (ARM) and Microprocessor without Interlocked Pipeline Stages (MIPS) are two examples of RISC architectures. MIPS-based RISC architectures are widely used because of their low power consumption and high-speed performance. In this thesis, we implement a 32-bit MIPS RISC architecture to be used as the microprocessor of the seizure detection system. It supports Register-type (R-type), Immediate-type (I-type), and Jump-type (J-type) instructions. The formats of these three instruction types are illustrated in Figure 5.2.

Figure 5.2.a shows the R-type instruction format of the 32-bit RISC architecture. The 6-bit

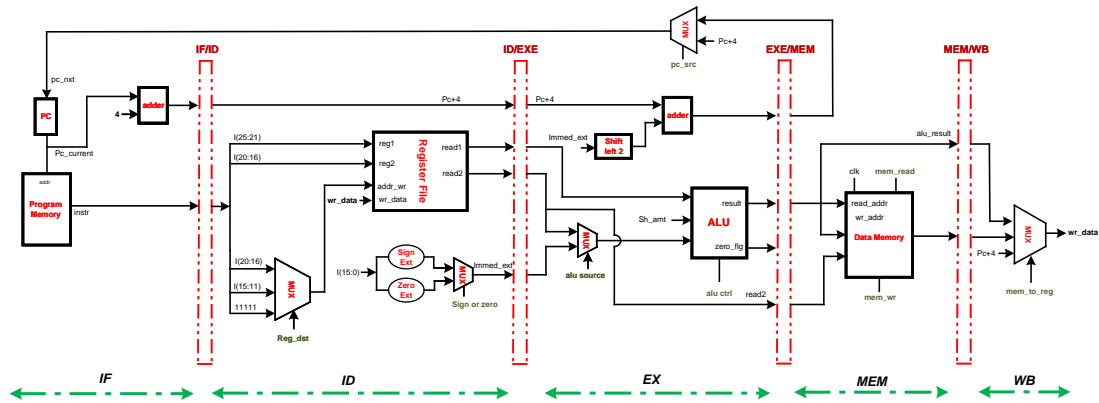


Figure 5.3: Five-stage RISC architecture

opcode field is the machine code representation of basic operations.  $r_s$  and  $r_t$  fields are the addresses of two operand registers. The 5-bit  $r_d$  field contains the address of the destination register.  $Sh_{amt}$  represents the amount of shift value using five bits suitable for 32-bit data length. The 6-bit function field determines the exact variant of the operation that is defined by the *Opcode* field.

Figure. 5.2.b shows the I-type instruction format. the type of operation is determined by the 6-bit *Opcode* field.  $r_s$  and  $r_t$  are the addresses of the operand and destination registers. The 16-bit immediate data is extended and converted to 32-bit data to be used in the Arithmetic-Logic Unit (ALU).

Figure. 5.2.c demonstrates the J-type instruction format. The *Opcode* indicates the variant of operation that is performed by the J-type instruction. The 26-bit *Branch offset* field is in charge of performing jump operations.

23 instructions are included in the instruction set of the RISC. The R-type, I-type, and J-type instructions are given in Table. 5.1.

### 5.3.1 RISC Implementation

The RISC microprocessor used for the implantable epileptic seizure detector follows the MIPS architecture with five pipeline stages [99]. The Harvard architecture is employed in the RISC microprocessor in which two separated memories are utilized for instructions and data. Moreover, the pipelining technique is used with five pipeline stages in order to increase the performance of the processor and improve the throughput. In the five-stage pipeline RISC, five instructions are processed concurrently. Five pipeline stages of the RISC are 1) Instruction fetch (IF), 2) Instruction decode (ID), 3) Execute (EX), 4) Memory (MEM), and 5) Write Back (WB) which are shown in Figure. 5.3. In the pipeline architecture, the output of each stage is stored in the registers of IF/ID, ID/EXE, EXE/MEM, and MEM/WB to be delivered to the next stage in the subsequent rising edge of the clock [100].

Table 5.1: Instruction list

| <b>R-type</b> | <b>Opcode</b> | $r_s$              | $r_t$ | $r_d$            | $Sh_{amt}$ | <b>Func</b>                                                                 | <b>Expression</b>                                                                   |
|---------------|---------------|--------------------|-------|------------------|------------|-----------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| NOP           | 000000        | -                  | -     | -                | -          | 000000                                                                      | No operation                                                                        |
| ADD           | 000000        | ✓                  | ✓     | ✓                | -          | 000001                                                                      | $R[r_d] \leftarrow R[r_s] + R[r_t]$                                                 |
| SUB           | 000000        | ✓                  | ✓     | ✓                | -          | 000010                                                                      | $R[r_d] \leftarrow R[r_s] - R[r_t]$                                                 |
| ADDu          | 000000        | ✓                  | ✓     | ✓                | -          | 000011                                                                      | Unsigned addition                                                                   |
| SUBu          | 000000        | ✓                  | ✓     | ✓                | -          | 000100                                                                      | Unsigned subtraction                                                                |
| AND           | 000000        | ✓                  | ✓     | ✓                | -          | 000101                                                                      | $R[r_d] \leftarrow R[r_s] \text{ AND } R[r_t]$                                      |
| OR            | 000000        | ✓                  | ✓     | ✓                | -          | 000110                                                                      | $R[r_d] \leftarrow R[r_s] \text{ OR } R[r_t]$                                       |
| XOR           | 000000        | ✓                  | ✓     | ✓                | -          | 000111                                                                      | $R[r_d] \leftarrow R[r_s] \text{ XOR } R[r_t]$                                      |
| NOT           | 000000        | ✓                  | -     | ✓                | -          | 001000                                                                      | $R[r_d] \leftarrow \text{NOT } R[r_s]$                                              |
| SLL           | 000000        | ✓                  | -     | ✓                | ✓          | 001001                                                                      | $R[r_d] \leftarrow R[r_s] \ll Sh_{amt}$                                             |
| SRL           | 000000        | ✓                  | -     | ✓                | ✓          | 001010                                                                      | $R[r_d] \leftarrow R[r_s] \gg Sh_{amt}$                                             |
| SLT           | 000000        | ✓                  | ✓     | ✓                | -          | 001011                                                                      | $R[r_d] \leftarrow '1' \text{ if } R[r_s] > R[r_t]$<br>else $R[r_d] \leftarrow '0'$ |
| <b>I-type</b> | <b>Opcode</b> | $r_s$              | $r_d$ | <b>Immediate</b> |            | <b>Expression</b>                                                           |                                                                                     |
| ADDi          | 100000        | ✓                  | ✓     | ✓                |            | $R[r_d] \leftarrow R[r_s] + \text{Immed}$                                   |                                                                                     |
| SUBi          | 100001        | ✓                  | ✓     | ✓                |            | $R[r_d] \leftarrow R[r_s] - \text{Immed}$                                   |                                                                                     |
| ANDi          | 100010        | ✓                  | ✓     | ✓                |            | $R[r_d] \leftarrow R[r_s] \text{ AND } \text{Immed}$                        |                                                                                     |
| Ori           | 100011        | ✓                  | ✓     | ✓                |            | $R[r_d] \leftarrow R[r_s] \text{ OR } \text{Immed}$                         |                                                                                     |
| LW            | 100100        | ✓                  | ✓     | ✓                |            | $R[r_d] \leftarrow \text{MEM}[R[r_s] + \text{Immed}]$                       |                                                                                     |
| SW            | 100100        | ✓                  | ✓     | ✓                |            | $R[r_d] \leftarrow \text{MEM}[R[r_s] + \text{Immed}]$                       |                                                                                     |
| SLTi          | 100101        | ✓                  | ✓     | ✓                |            | $R[r_d] \leftarrow 1 \text{ if } R[r_s] > \text{Immed}$                     |                                                                                     |
| BEQ           | 101100        | ✓                  | ✓     | ✓                |            | Branch if $R[r_s] = R[r_d]$                                                 |                                                                                     |
| BNQ           | 101101        | ✓                  | ✓     | ✓                |            | Branch if $R[r_s] \neq R[r_d]$                                              |                                                                                     |
| <b>J-type</b> | <b>Opcode</b> | <b>Jump offset</b> |       |                  |            | <b>Expression</b>                                                           |                                                                                     |
| J             | 101111        | ✓                  |       |                  |            | $pc \leftarrow \text{Jump offset extended}$                                 |                                                                                     |
| JAL           | 110000        | ✓                  |       |                  |            | $pc \leftarrow \text{Jump offset extended}$<br>$next\_pc \leftarrow pc + 4$ |                                                                                     |

The first pipeline stage is called instruction fetch. Two main components of this stage are the Program Counter (PC) and the program memory. The PC holds current instruction address to fetch from the instruction memory. An adder is employed to generate the address of next instruction that is (PC+4) if branches or jump operations do not occur. The program memory stores 32 instructions of four-byte width.

The second pipeline stage is the Instruction decode (ID). Instructions are made up of multiple segments which are shown in Figure. 5.2. In this stage, the segments are decoded and the processor differentiates between operands and opcode. The register file is the main module of this stage. It consists of 32 GPRs of 32-bit length. According to operands' addresses, two registers are read from the register file. Moreover, 16-bit immediate data that are decoded from instructions are extended to 32-bit data using sign-extension or zero-extension techniques. Two registers as well as the extended immediate data are given to registers of the next stage.

A key point to mention is that the control signals such as `reg_dst`, `sign`, `zero`, `alu_ctrl`, `mem_read`, `mem_write`, `pc_src`, and `mem_to_reg` are generated in the decode stage. Control signals are in charge of the following tasks.

- Ensure the correct operation of instructions.
- Determine the operation of the subsequent stages.
- Smooth operation of the pipeline
- Handling branch and jump operation

The third pipeline stage is the Execution stage (EXE). The ALU is the major module of this stage. The ALU performs arithmetic, logical, and shift operations. Two registers that are taken from the register file as well as the extended immediate data are the inputs of ALU. Three types of ALU operations that are considered for the proposed programmable seizure detector are explained hereafter.

- **Arithmetic operations:** Signed and unsigned adding and subtraction operations are performed in ALU.
- **Logical operations:** *AND*, *OR*, *XOR*, and *NOT* logical operations are conducted in ALU.
- **Shift operations:** Right shift and left shift operations are carried out in ALU.

Moreover, branch condition evaluation as well as jump target address calculation are also conducted in the EX stage of the RISC.

The fourth pipeline stage is the memory stage (MEM). The principal module of this stage is data memory. 32-bit data are stored in the data memory. This stage is responsible for memory-related operations such as load and store architectures.

The last pipeline stage is Write Back (WB). In this stage, a multiplexer receives the execution result of ALU and the data taken from the data memory. The output of this stage is written back to a register determined by the destination register field of instruction.

## 5.4 Seizure Detection with RISC

In this stage, the signal processing block is connected to the RISC microprocessor to enable programmable seizure detection. The connection of DSP unit to the RISC is shown in Figure. 5.1. Time-domain low-hardware complexity features that have demonstrated their seizure detection effectiveness in Chapter 4 are employed in the feature pool. The features are coastline, energy, nonlinear energy, variance, range, and correlation. As shown in Figure. 5.1, all features are extracted, ranked and a subset of features are selected.

Feature selection is conducted based on the F1-score. The F1-score is considered as an

Table 5.2: Feature ranking based on F1-score

| Patient | Rank 1           | Rank 2           | Rank 3           | Rank 4           |
|---------|------------------|------------------|------------------|------------------|
| ID1     | Coastline        | Nonlinear energy | Variance         | Range            |
| ID2     | Correlation      | Coastline        | Nonlinear energy | Range            |
| ID3     | Coastline        | Nonlinear energy | Correlation      | Range            |
| ID4     | Nonlinear energy | Coastline        | Variance         | Energy           |
| ID5     | Correlation      | Coastline        | Nonlinear energy | Energy           |
| ID6     | Correlation      | Coastline        | Variance         | Nonlinear energy |
| ID7     | Nonlinear energy | Coastline        | Correlation      | Energy           |
| ID8     | Nonlinear energy | Correlation      | Coastline        | Energy           |
| ID9     | Correlation      | Range            | Coastline        | Nonlinear energy |
| ID10    | Nonlinear energy | Coastline        | Range            | Correlation      |

appropriate feature ranking metric since the iEEG dataset of seizure detection is extremely unbalanced. The F1-score is a measure to evaluate both true positive and true negative detections. It is the harmonic mean of the precision and recall metrics introduced in (4.4) and (4.6). To assess the performance of feature ranking by F1-score, the algorithm is tested on 10 patients from the SWEC-ETHZ dataset. The results of feature ranking are given in Table. 5.2.

When the features are ranked according to the F1-score, a subset of features is selected which includes four top-rank features. The top-rank features are extracted in the DSP core. Subsequently, the seizure detection signals are obtained after threshold crossings and smoothing by a majority function with a 3-second window length. Thus, the DSP core outputs ( $D_1 - D_4$ ) are given to the RISC for further processing. The **pseudo-code** related to the training phase is given hereunder.

1. Extracting feature 1 to feature 6
2. Calculating the recall of feature 1 to feature 6
3. Calculating the precision of feature 1 to feature 6
4. Calculating the F1-score of feature 1 to feature 6
5. Ranking the features based on F1-score in a descending order
6. Eliminating two features with the lowest F1-score
7. Feature subset generation using the remaining four features

The **pseudo-code** regarding the test phase of signal processing is given as:

1. Feature extraction from the feature subset including four top-rank features
2. Comparing features with their corresponding thresholds

3. Generating early detection labels
4. Three-second majority function post-processing
5. Generating final detection labels ( $D_1 - D_4$ )

#### 5.4.1 RISC Therapy Programs

Programming the RISC processor realizes constructive interactions between the device and users. Users are epileptic patients as well as physicians. Interaction of neurologists is enabled by defining different therapy modes and programming the RISC processor with those therapies. The purpose of defining different therapy options is to fit seizure detection characteristics with current conditions of patients.

The main motivation behind proposing the programmable seizure detector is to adapt the implant performance to different daily activities of patients. It is required to modify seizure detection parameters during different daily activities of patients to enhance their safety, comfort, and quality of life.

Closed-loop IMDs apply electrical neurostimulation to cancel and decrease the severity of seizure occurrences. Nonetheless, this action involves some side effects that are described hereafter.

- Hoarseness and voice change
- Cough or throat irritation
- Tingling sensation
- Abdominal pain
- Headache
- Adverse cognitive effects
- Sleep disturbances

The proposed programmable seizure detector can be adjusted to match seizure detection settings to patients' conditions and daily activities. It should be noted that there is a tradeoff between detection latency and the number of false positive detections. Adjustment of these parameters according to the health condition of patients and their daily activities can be highly beneficial to improve their well-being.

For instance, when a patient gets sick, he prefers to have the minimum excessive neurostimulation which can intensify his headache or abdominal pain. It means that seizure detection must be done with maximum specificity and minimum false positive detections to prevent adverse impacts on the patient's health condition. In this case, seizure detection takes place

with more detection latency.

As previously mentioned, hoarseness and voice change are common side effects associated with neurostimulation. Thus, when a patient is making a speech in front of an audience, he prefers to avoid hoarseness caused by neurostimulation. In this case, the detector must inject the minimum current pulses during the stimulation phases.

In addition, during some specific activities like passing an exam and playing sports, patients may prefer to suppress upcoming seizures as soon as possible at the cost of experiencing more side effects caused by excessive neurostimulation.

Physicians can define different safe and effective therapies tailored to different situations of their patients thanks to the novel programmable seizure detector. Hence, patients have possibility to switch among the defined programs to dynamically fit the seizure detector specifications based on their current situations and needs. The communication between patients and implant is done by a handheld remote to transmit the user's commands to the RISC processor of the implant.

Furthermore, the positive effects of neurostimulation emerge after at least one year [10]. In this situation, therapy programs should be modified regarding the improved condition of patients. The proposed framework enables therapy change over time without any need for brain surgery related to the hardware change of the device.

To demonstrate the functionalities of the programmable seizure detector, three therapy modes are defined that are discussed hereafter.

1. **Therapy mode 1:** The goal is to obtain the fastest seizure detector.
2. **Therapy mode 2:** The goal is to make a tradeoff between seizure detection latency and false alarm rates.
3. **Therapy mode 3:** The goal is to achieve the minimum false positive detections.

Defining different therapy modes is realized using logical classification functions. The logical classification function is responsible to decide on the final seizure detection label when multiple feature extraction accelerators are available in the seizure detector.

A key point to mention is that applying logical *OR* to detection labels of feature extraction accelerators improves the sensitivity of detection at the cost of lowering the specificity. In addition, applying logical *AND* to detection labels of accelerators enhances the specificity and degrades the detection delay. As a consequence, classification functions of three therapy modes are given in (5.1), (5.2), and (5.3).

$$Function_{mode 1} = D_1 + D_2 + D_3 + D_4 \quad (5.1)$$

Table 5.3: RISC register file

|                       |            |        |        |            |            |                 |
|-----------------------|------------|--------|--------|------------|------------|-----------------|
| <b>Register No.</b>   | \$0        | \$1    | \$2    | \$3        | \$4        | \$5             |
| <b>Register Value</b> | reserved 0 | $D_1$  | $D_2$  | $D_3$      | $D_4$      | user command    |
| <b>Register No.</b>   | \$6        | \$7    | \$8    | \$9        | \$10       | \$11            |
| <b>Register Value</b> | 0x0000     | 0x0001 | 0x0002 | variable 1 | variable 2 | Final detection |

$$Function_{mode-2} = (D_1 + D_2) \cdot (D_3 + D_4) \tag{5.2}$$

$$Function_{mode-3} = D_1 \cdot D_2 \cdot D_3 \cdot D_4 \tag{5.3}$$

Where  $D_1 - D_4$  are early detection labels which are the output of the DSP core shown in Figure. 5.1. Fast detection program of therapy mode 1 is done using logical *OR* gates. The Tradeoff between specificity and detection latency is established by using a combination of logical *OR* and logical *AND* gates. The lowest false positive detection program of therapy mode 3 is performed by using logical *AND* gates.

One of the key attributes of a RISC processor is having a register file which incorporates 32 GPRs. According to the proposed seizure detection performance only 11 registers of the register file deal with seizure detection tasks that are provided in Table . 5.3.

\$0 is reserved by the compiler and always holds a zero value. The seizure detection labels of feature extractor accelerators are stored in \$1-\$4. \$5, \$6 and \$7 keep the constant values of 0, 1, and 2, respectively. They are used to check the branch conditions related to user commands. Two registers \$9 and \$10 are used to hold temporary variables associated with the computations of the RISC instructions. \$11 is used to store the final detection label. The other registers are unused and can be employed by other programs of the RISC.

The list of instructions and their corresponding assembly codes are given in Table .5.4. Instr 0 to instr 2 checks the user command and branch to their corresponding program lines. If the user chooses therapy mode 1, mode 2, or mode 3, the program counter branches to instructions 4, 12, and 20, respectively. Instructions 4-10 implement therapy mode 1, instructions 12-18 implement therapy mode 2, and instructions 20-26 implement therapy mode 3.

### 5.5 FPGA Implementation Results

Six feature extraction accelerators as well as the RISC processor are implemented on a Cyclone V FPGA of the Terasic DE-10 board to demonstrate the hardware compatibility in conjunction

Table 5.4: RISC instruction set list

| Instr No. | Assembly code      | Explanation                                                 |
|-----------|--------------------|-------------------------------------------------------------|
| 0         | BEQ \$5, \$6, 3    | Therapy mode 1: conditional branch to instr 4               |
| 1         | BEQ \$5, \$7, 10   | Therapy mode 2: conditional branch to instr 11              |
| 2         | BEQ \$5,\$8, 17    | Therapy mode 3: conditional branch to instr 18              |
| 3         | NOP                | No operation                                                |
| 4         | OR \$9,\$1,\$2     | Therapy mode 1: logical classification function             |
| 5         | OR \$10,\$3,\$4    | Therapy mode 1: logical classification function             |
| 6         | OR \$11,\$9,\$10   | Therapy mode 1: logical classification function             |
| 7         | SW \$11,1 (\$0)    | Storing the detection label to memory                       |
| 8         | BNQ \$5, \$6, 1    | Conditional branch to check user command                    |
| 9         | J 0                | Jump to instr 0                                             |
| 10        | J 4                | Jump to instr 4 to continue therapy mode 1                  |
| 11        | NOP                | No operation                                                |
| 12        | AND \$9,\$1, \$2   | Therapy mode 2: logical classification function calculation |
| 13        | AND \$9,\$3, \$4   | Therapy mode 2: logical classification function calculation |
| 14        | OR \$11,\$9, \$10  | Therapy mode 2: logical classification function calculation |
| 15        | SW \$11,1 (\$0)    | Storing the detection label to memory                       |
| 16        | BNQ \$5,\$7,1      | Conditional branch to check user command                    |
| 17        | J 12               | Jump to instr 12                                            |
| 18        | J 0                | Jump to instr 0                                             |
| 19        | NOP                | No operation                                                |
| 20        | AND \$9,\$1, \$2   | Therapy mode 3: logical classification function calculation |
| 21        | AND \$10,\$3, \$4  | Therapy mode 3: logical classification function calculation |
| 22        | AND \$11,\$9, \$10 | Therapy mode 3: logical classification function calculation |
| 23        | SW \$11,1 (\$0)    | Storing the detection label to memory                       |
| 24        | BNQ \$5,\$8,1      | Conditional branch to check user command                    |
| 25        | J 20               | Jump to instr 20                                            |
| 26        | J 0                | Jump to instr 0                                             |
| 27-31     | NOP                | No operation                                                |

with the dynamic power consumption of design. The programmable seizure detection algorithm is tested on the iEEG signals of 10 patients with intractable epilepsy from the SWEC-ETHZ database. The FPGA implementation parameters are given in Table. 5.5.

All 10 patients are tested with three aforementioned therapy programs. Switching between different therapy modes is done using the switches of the Terasic board to deliver user commands. Furthermore, iEEG signals of the patients are transmitted to the Nios II embedded processor of the FPGA through serial data communication. UART serial data transfer is used to deliver 16-bit iEEG signals through two packets of 8-bit width. The baudrate of communication is 115200 Bit Per Second (BPS) [97].

The test phases of all patients are carried out in a completely unbiased way in which the data

Table 5.5: Hardware implementation settings

| Logic utilization      | Num of registers | Memory bits   | DSP blocks   |
|------------------------|------------------|---------------|--------------|
| 2165                   | 3059             | 227200        | 5            |
| Accelerators frequency | RISC frequency   | Dynamic Power | Static power |
| 512 Hz                 | 50 MHz           | 0.78 mW       | 411.33 mW    |

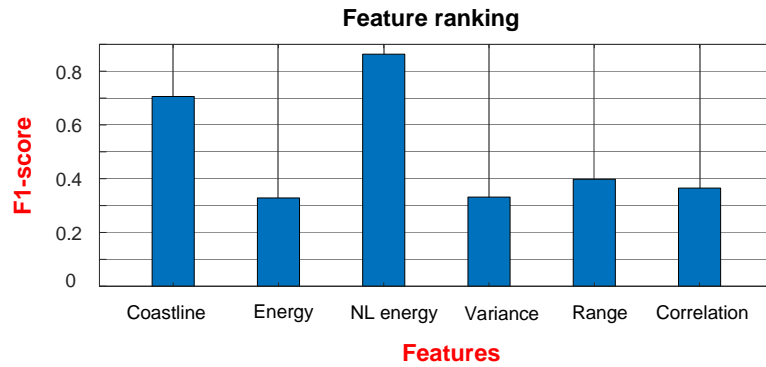


Figure 5.4: Training phase F1-scores

used for training the model is taken out from test data. Less than 50% of data is used for training the model which is a great advantage compared to common machine learning and deep learning systems [36, 97].

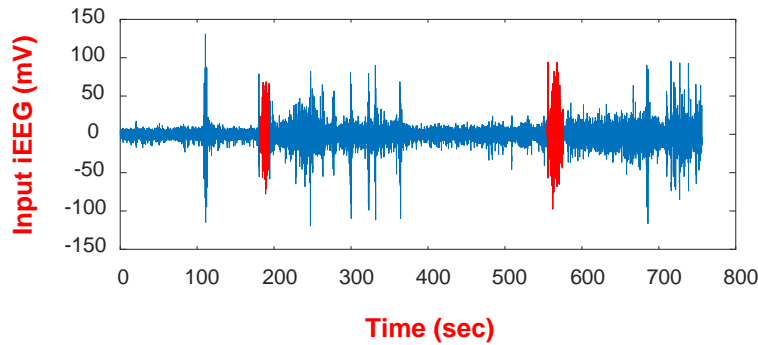
To visualize FPGA measurement results, the outputs of a random patient ( $ID_{10}$ ) are demonstrated in this section. F1-scores of the features that are used to train the model is depicted in Figure. 5.4. According to the F1-score plot, nonlinear energy, coastline, range, and correlation features are the selected subset of the feature pool for patient  $ID_{10}$ . Only these four features are extracted in the DSP core of system.

The iEEG used in the FPGA test phase is shown in Figure. The 5.5. iEEG contains two seizure events. The first seizure starts at  $t = 180 \text{ sec}$  and lasts for 13 seconds. The second seizure starts at  $t = 555 \text{ sec}$  and lasts for 21 seconds. The iEEG related to seizure events is depicted in red and normal-state iEEG is depicted in blue.

As previously mentioned, the feature selection unit chooses the top-four rank features. FPGA measurements of feature extractions in the DSP core are demonstrated in Figure. 5.6. The extracted features during seizure states are depicted in red.

The measurement results of three therapy programs on subject  $ID_{10}$  are demonstrated in Figure. 5.7. The seizures' duration are shown using red dashed lines.

Therapy mode 1 is depicted in Figure. 5.7.a. It uses (5.1) as the classification function which aims to minimize detection delay at the cost of more false positive detections. FPGA implementation results evidence that two seizures are rapidly detected with a detection latency

Figure 5.5: iEEG of patient  $ID_{10}$ 

of  $t=0.75$  sec. False positive detections are observable in pre-ictal and post-ictal states. The specificity, which is the representation of false positive detections, is 94.25% for patient  $ID_{10}$ .

Therapy mode 2 is shown in Figure. 5.7.b. It uses (5.2) as the classification function which aims to strike a balance between latency and specificity of detection. It is evident that the number of false positive detection is remarkably reduced at the cost of latency increment. The specificity improves from 94.25% to 99.17% at the expense of more latency from 0.75 sec to 6.25 sec that is still within an acceptable latency range.

Therapy mode 3 is illustrated in Figure. 5.7.c. It uses (5.3) as the classification function so as to maximize the specificity of detection. FPGA measurement results reveal that the number of false positive detections is extremely low which contribute to a great specificity of 99.72%.

The FPGA implementation results of 10 patients from the SWEC-ETHZ are given in Table. 5.6. The summary of FPGA results of 10 patients under three therapies is given in Table. 5.7. The proposed programmable seizure detector sheds new light on the application of RISC microprocessors in implantable seizure control devices. Table. 5.7 demonstrates that the maximum sensitivity of 100% and minimum detection latency of 9.95 seconds are reached using therapy mode 1. Moreover, the maximum specificity is obtained using therapy mode 3. It is noteworthy that therapy mode 2 establishes a balanced tradeoff between sensitivity, specificity, and detection delay parameters.

As mentioned in the beginning of this chapter, the key specification of the proposed seizure detector is the user interaction. Thus, this device is capable of exhibiting a maximum sensitivity of 100%, maximum specificity of 99.6%, and minimum detection delay of 9.95 sec if a patient properly switches between different therapy modes.

## 5.6 Programmability in Channel and Feature Selection

The goal of this section is to extend the programmability characteristic of the seizure detector. In the previous section, only logical classification functions were determined by the RISC

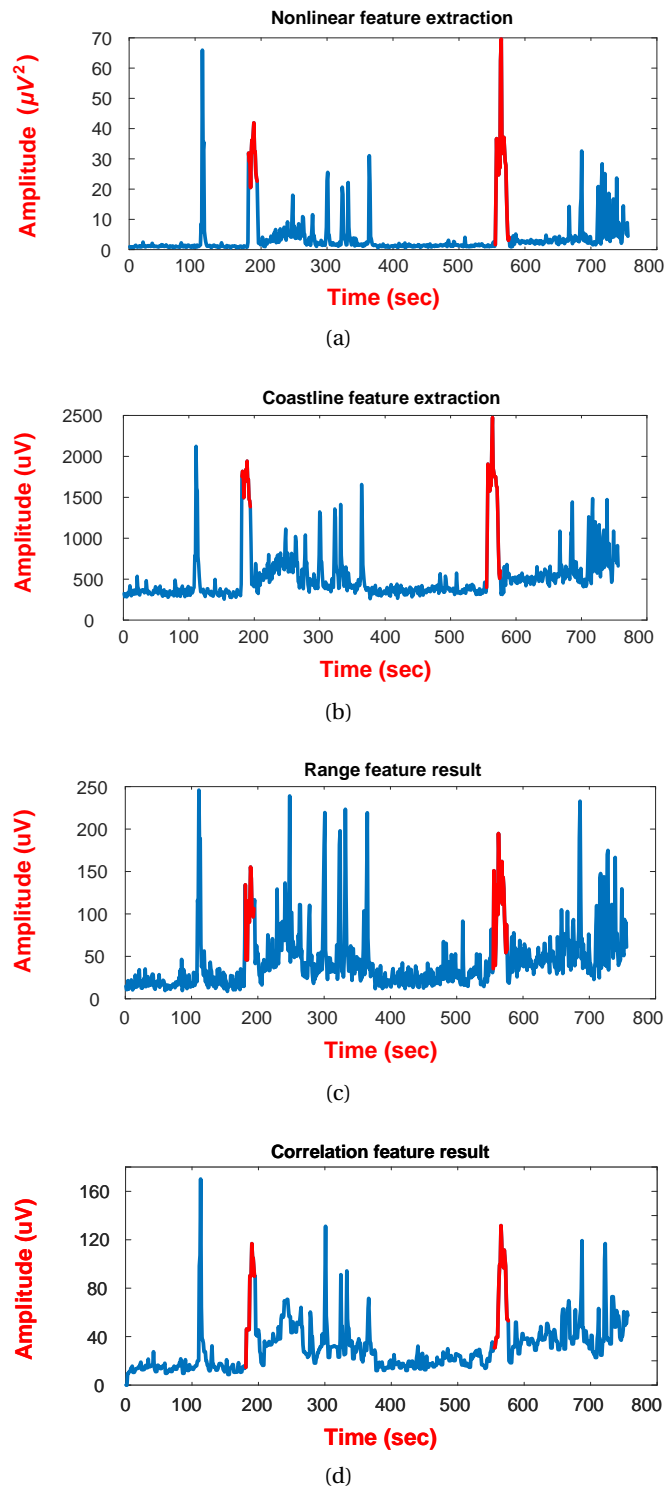


Figure 5.6: FPGA results of top-rank features of  $ID_{10}$  (a) nonlinear energy, (b) coastline, (c) range, and (d) correlation

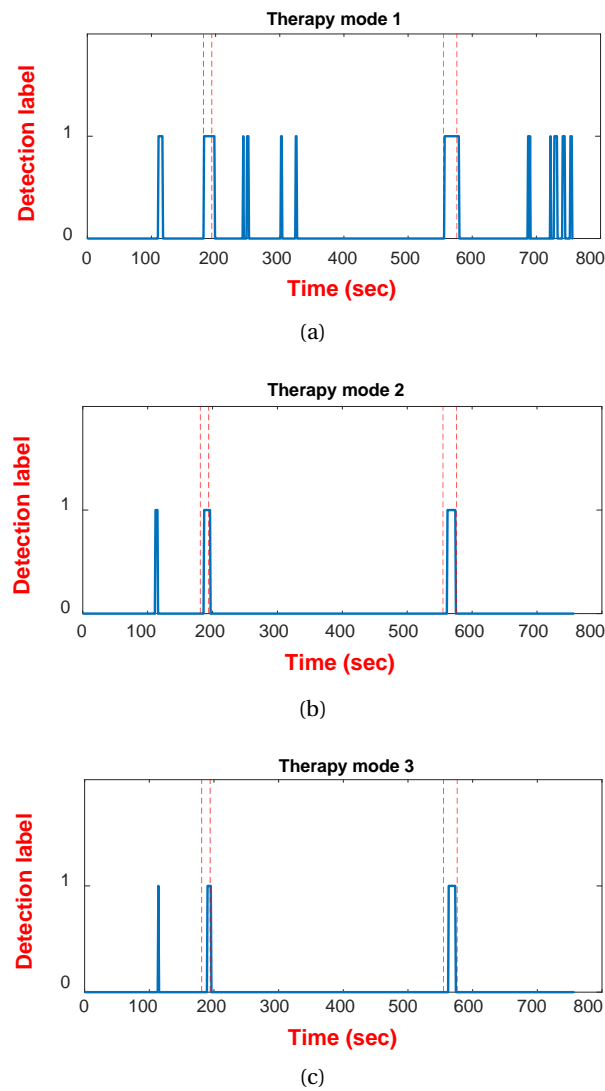


Figure 5.7: FPGS seizure detection results of (a) therapy mode 1, (b) therapy mode 2, (c) therapy mode 3

program and user commands. However, this section aims to generate not only programmable logical classification function but also programmable channel and feature selection. Furthermore, a robust algorithm for generation of advanced logical classification functions is presented.

The proposed programmable seizure detector can operate in different modes. Not only do operation modes depend on seizure detection performance but they also have an influence on the power consumption of the implant which is a critical design consideration.

The framework of the proposed seizure detector with programmable channel selection, feature selection and logical classification function is illustrated in Figure. 5.8.

Table 5.6: Detailed FPGA results of 10 patients

| Patient No. | Therapy | Sensitivity (%) | Specificity (%) | Latency (sec) | Power   |
|-------------|---------|-----------------|-----------------|---------------|---------|
| ID1         | Mode 1  | 100             | 87.5            | 4.08          | 0.79 mW |
|             | Mode 2  | 85.71           | 96.9            | 15            |         |
|             | Mode 3  | 71.4            | 99.05           | 17.3          |         |
| ID2         | Mode 1  | 100             | 97.78           | 3.3           | 0.79 mW |
|             | Mode 2  | 100             | 99.58           | 13.7          |         |
|             | Mode 3  | 100             | 100             | 22.2          |         |
| ID3         | Mode 1  | 100             | 93.44           | 3.6           | 0.76 mW |
|             | Mode 2  | 100             | 100             | 4.6           |         |
|             | Mode 3  | 100             | 100             | 29.7          |         |
| ID4         | Mode 1  | 100             | 98.9            | 21            | 0.79 mW |
|             | Mode 2  | 100             | 100             | 28            |         |
|             | Mode 3  | 100             | 100             | 28            |         |
| ID5         | Mode 1  | 100             | 97.78           | 3.3           | 0.76 mW |
|             | Mode 2  | 100             | 83.5            | 19.6          |         |
|             | Mode 3  | 100             | 91.17           | 26.32         |         |
| ID6         | Mode 1  | 100             | 98.33           | 7             | 0.79 mW |
|             | Mode 2  | 100             | 100             | 11.4          |         |
|             | Mode 3  | 100             | 100             | 31.6          |         |
| ID7         | Mode 1  | 100             | 91              | 2.5           | 0.78 mW |
|             | Mode 2  | 100             | 99.58           | 13.7          |         |
|             | Mode 3  | 100             | 100             | 22.2          |         |
| ID8         | Mode 1  | 100             | 85.6            | 2             | 0.76 mW |
|             | Mode 2  | 100             | 98.9            | 13            |         |
|             | Mode 3  | 100             | 100             | 13            |         |
| ID9         | Mode 1  | 100             | 90.42           | 25.3          | 0.78 mW |
|             | Mode 2  | 100             | 98.9            | 37.8          |         |
|             | Mode 3  | 100             | 99.9            | 39.4          |         |
| ID10        | Mode 1  | 100             | 94.72           | 0.753         | 0.78 mW |
|             | Mode 2  | 100             | 99.17           | 6.25          |         |
|             | Mode 3  | 100             | 99.72           | 8.25          |         |

Table 5.7: Summary results of the programmable seizure detector

| Therapy mode | Sensitivity (%) | Specificity (%) | Delay (sec) |
|--------------|-----------------|-----------------|-------------|
| Mode 1       | <b>100</b>      | 92.2            | <b>9.95</b> |
| Mode 2       | 98.6            | 98              | 16.9        |
| Mode 3       | 95.14           | <b>99.6</b>     | 23.26       |

Figure. 5.8 shows components used in the training phase. iEEG recordings of N channel are ranked based on the C.E.R given in (4.11). The channel ranks are outputs of the training phase that are delivered to the processing unit.

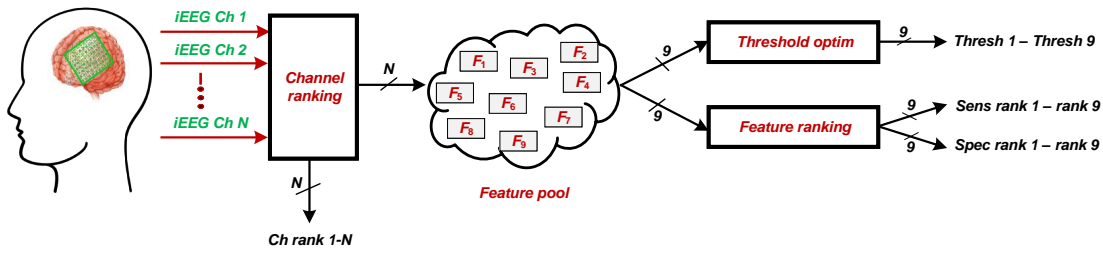


Figure 5.8: Training phase architecture of programmable seizure detector

Nine time-domain features are available in the feature pool (coastline, energy, nonlinear energy, variance, minimum, maximum, range, average, and correlation features). Threshold optimization is conducted in the training phase. The goal of this step is to find a proper threshold that guarantees at least 90% specificity. The **pseudo-code of threshold calculation** associated with a sample feature ( $F_x$ ) is given hereafter.

1. Extracting  $F_x$  from all windows of data
2. Finding the minimum amplitude of  $F_x$
3. Finding the maximum amplitude of  $F_x$
4.  $n=0$  (initial step number)
5. Step calculation:  $step = \frac{max-min}{100}$
6.  $threshold = min + n \times step$
7. Specification calculation using validation data
8. if (Specificity  $\geq 0.9$ ) then go to line 11
9.  $n=n+1$
10. Go to line 6
11. End

Feature ranking is also done in the training phase. In this section, the feature ranking is conducted in two ways and feature selection is completely dependent on the operation mode of the implant which is determined by patients' interactions through transmitting user commands. In the first feature ranking strategy, the features are ranked with respect to their capability of seizure detection with short latency. Thus, the sensitivity of each feature is calculated and a feature with a higher sensitivity obtains a higher rank.

In the second feature ranking strategy, the features are ranked based on their capability of generating the least false positive detections evaluated on the validation part of dataset. The

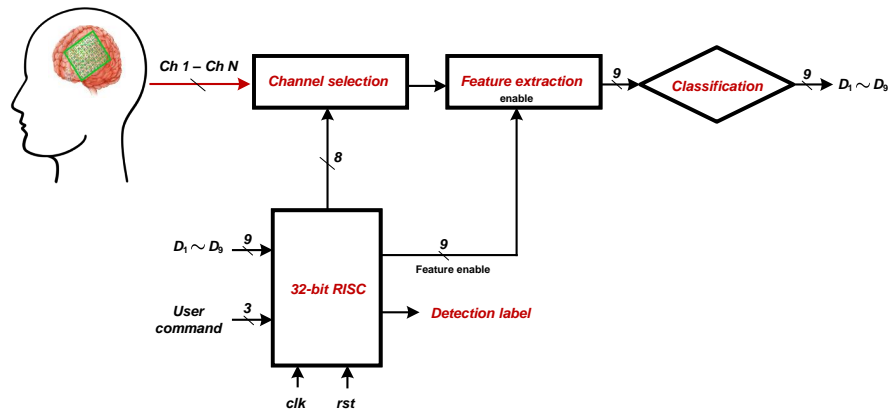


Figure 5.9: Test phase system topology

specificities of features are calculated and a feature with a higher specificity is placed in a higher rank.

The architecture of the test phase is illustrated in Figure. 5.9. The execution of this phase is influenced by user commands given by patients. All iEEG channels (N channels) are given to the channel selection unit. The RISC processor determines the number of selected channels according to user commands. The iEEG with reduced dimension is delivered to the feature extraction unit. The enable signal of each feature extraction accelerator is provided by the RISC based on user commands and operation modes of the device. Optimized thresholds computed in the training phase are used in the classification unit to generate early detection labels ( $D_1 - D_9$ ). Early detection labels are inputs of the RISC used in the classification functions. The microprocessor generates final detection labels according to the user command and its corresponding classification function.

The proposed architecture enables maximum user interactions in which patients can determine the number of extracted features, the number of recording channels, and the logical classification functions according to their needs under the permission of their neurologists. In addition, a novel method of classification function generation is proposed to realize high seizure detection performance under different operation modes.

Therapeutic goals and power consumption of the seizure detector are considered as the key parameters in defining the operation modes of the device. Thus, neurologists can program the RISC processor to define different therapy scenarios as well as enable different the power consumption options of the implant. Six operation modes are defined for the device that are given in table. 5.8.

The operation modes are defined based on therapeutic goals (Fast seizure detection and minimum false alarm rate), and power consumption level (low, medium and high) of the seizure detector. As a consequence, the number of selected features varies from 3 to 7 and the number of selected channels varies from 1 to 5 according to the RISC processor program

Table 5.8: Operation modes of the programmable seizure detector

| Op mode | Medical goal       | Power status | Num of features | Num of channels |
|---------|--------------------|--------------|-----------------|-----------------|
| 1       | Low latency        | Low          | 3               | 1               |
| 2       | Low latency        | Medium       | 5               | 3               |
| 3       | Low latency        | High         | 7               | 5               |
| 4       | Min false positive | Low          | 3               | 1               |
| 5       | Min false positive | Medium       | 5               | 3               |
| 6       | Min false positive | High         | 7               | 5               |

and user commands. Moreover, a unique logical classification function will be generated for each operation mode that is explained in the following. The Logical Classification Function (LCF) aims to strike a balance between sensitivity and specificity of seizure detection based on medical goals and power consumption status of the implant which are defined by user commands.

The pseudo-code related to LCF generation is given hereunder.

1.  $F_{sens} \leftarrow$  Ranking based on sensitivity
2.  $F_{spec} \leftarrow$  Ranking based on specificity
3. U.C  $\leftarrow$  user command (receiving a 3-bit user command)
4. if (U.C = "001") then
 
$$Num_{features} = 3, Num_{channels} = 1$$

$$LCF = (F_{sens}(1) \cdot F_{spec}(1)) + F_{sens}(1) \cdot F_{sens}(2)$$
5. else if (U.C = "010") then
 
$$Num_{features} = 5, Num_{channels} = 3$$

$$LCF = F_{sens}(1) \cdot (F_{spec}(1) + F_{spec}(2)) + (F_{sens}(2) \cdot F_{sens}(1)) + (F_{sens}(1) \cdot F_{sens}(2) \cdot F_{sens}(3))$$
6. else if (U.C = "011") then
 
$$Num_{features} = 7, Num_{channels} = 5$$

$$LCF = F_{sens}(1) \cdot (F_{spec}(1) + F_{spec}(2) + F_{spec}(3)) + F_{sens}(2) \cdot (F_{spec}(1) + F_{spec}(2)) + F_{sens}(3) \cdot F_{spec}(1) + (F_{sens}(1) \cdot (F_{sens}(2) \cdot (F_{sens}(3)))$$
7. else if (U.C = "100") then
 
$$Num_{features} = 3, Num_{channels} = 1$$

$$LCF = (F_{spec}(1) \cdot F_{sens}(1)) + F_{spec}(1) \cdot F_{spec}(2)$$
8. else if (U.C = "101") then
 
$$Num_{features} = 5, Num_{channels} = 3$$

$$LCF = F_{spec}(1) \cdot (F_{sens}(1) + F_{sens}(2)) + (F_{spec}(2) \cdot F_{spec}(1)) + (F_{spec}(1) \cdot F_{spec}(2) \cdot F_{spec}(3))$$
9. else if (U.C = "110") then

$$\begin{aligned}
 Num_{features} &= 7, Num_{channels} = 5 \\
 LCF &= F_{spec}(1) \cdot (F_{sens}(1) + F_{sens}(2) + F_{sens}(3)) + F_{spec}(2) \cdot (F_{sens}(1) + F_{sens}(2)) + \\
 &F_{spec}(3) \cdot F_{sens}(1) + (F_{spec}(1) \cdot F_{spec}(2) \cdot F_{spec}(3))
 \end{aligned}$$

10. end

In operation mode 1, the purpose is to achieve fast seizure detection with the lowest energy consumption. Therefore, only three features are extracted in the feature extraction unit from a single iEEG channel. Feature rankings based on both sensitivity and specificity metrics are used to define a feature subset. Since the medical goal of operation mode 1 is fast detection, the majority of features (two features) are selected according to their sensitivity ranks ( $X_1$  and  $X_2$ ) and the remaining feature is the feature with the highest specificity ( $Y_1$ ).

The LCF is generated to achieve the operation mode targets. In this operation mode, the importance of features with higher sensitivity ( $X_1$  and  $X_2$ ) is more than features with higher specificity ( $Y_1$ ). The logical classification function aims to establish a tradeoff between sensitivity and specificity of detection. The compromise can be constructed in two ways.

- Applying logical *AND* to a feature with high sensitivity and a feature with high specificity.
- Applying logical *AND* to all features in the feature subset that are selected based on their sensitivity ranks.

Hence, the logical classification function of operation mode 1 is generated in (5.4).

$$LCF_{mode-1} = X_1 \cdot Y_1 + X_1 \cdot X_2 \quad (5.4)$$

Where  $X_i$  and  $Y_i$  are the features with the  $i^{th}$  rank in the sensitivity ranking list and  $j^{th}$  in the specificity ranking list, respectively. The feature importance of  $X_1$  is more than  $X_2$ , and the importance  $X_2$  is more than  $Y_1$  according to their contribution in the LCF.

To clarify the functionality of the proposed programmable seizure detector, the results of a sample patient (patient  $ID_2$ ) are discussed in this section. The sensitivity and specificity ranking lists of patient  $ID_2$  are given in Table. 5.9.

The iEEG of Patient  $ID_2$  which contains two seizure events is shown in Figure. 5.10. The first seizure starts at  $t = 181$  sec and lasts for 236 seconds. The second seizure starts at  $t = 777$  sec and lasts for 301 seconds.

The seizure detection result of  $ID_2$  in operation mode 1 is demonstrated in Figure. 5.11. It performs fast seizure detection with a latency of 3.5 seconds. The specificity of this operation mode is 97.08%.

In operation mode 2, the medical goal is still fast seizure detection but the power consumption

Table 5.9: Sensitivity and specificity ranking list

| Rank | Sensitivity ranking | Specificity ranking |
|------|---------------------|---------------------|
| 1    | coastline           | nonlinear energy    |
| 2    | nonlinear energy    | correlation         |
| 3    | minimum             | coastline           |
| 4    | maximum             | energy              |
| 5    | range               | variance            |
| 6    | correlation         | maximum             |
| 7    | energy              | range               |
| 8    | variance            | minimum             |
| 9    | average             | average             |

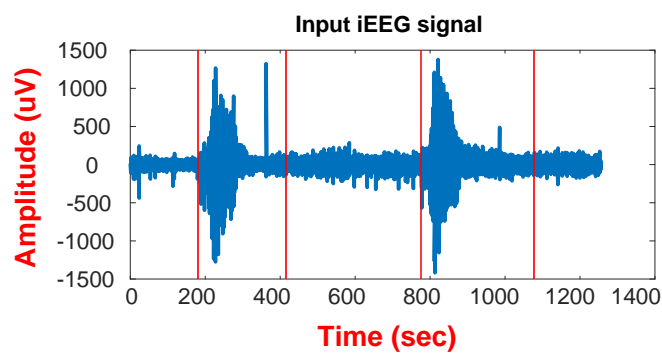


Figure 5.10: iEEG signal of patient ID2

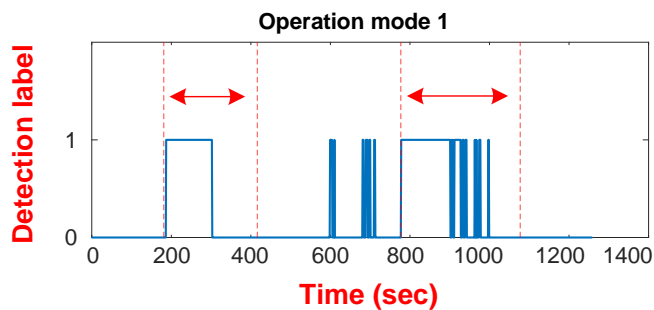


Figure 5.11: Seizure detection of ID2 under operation mode 1

of the seizure detector can be increased. More features can be extracted from more number of iEEG channels compared to operation mode 1. Therefore, the feature extraction unit extracts five features from top-three iEEG channels.

Since fast seizure detection is the medical goal of operation mode 2, the top three features of the sensitivity ranking list ( $X_1, X_2, X_3$ ) and the top two features of the specificity ranking list ( $Y_1, Y_2$ ) are included in the final feature subset. The importance of features from sensitivity list is higher than the features from the specificity ranking list. That is why these features exhibit more contribution in the LCF given in (5.5). It should be noted that a common feature cannot

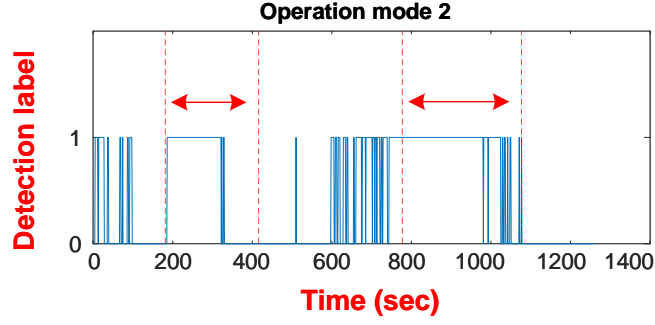


Figure 5.12: Seizure detection of ID2 under operation mode 2

be selected from both the sensitivity and specificity ranking lists. In this case, the next feature with a lower rank will replace the repetitive feature.

$$LCF_{mode-2} = X_1 \cdot (Y_1 + Y_2) + X_2 \cdot Y_1 + X_1 \cdot X_2 \cdot X_3 \quad (5.5)$$

The seizure detection result of  $ID_2$  is depicted in Figure. 5.12. We observe that seizure detection latency, which is the primary medical goal of this operation mode, is reduced from 3.5 seconds to 3 seconds. However, the number of false positive detections is increased and the specificity is decreased to 95.42%.

In operation mode 3, the medical goal is fast detection and power consumption status is high. Thus, the number of extracted features is increased from 5 to 7 and the number of selected channels is increased from 3 to 5 according to Table. 5.8. The majority of features in the final feature subset are taken from the sensitivity ranking list to achieve faster seizure detection ( $X_1 - X_4$ ). Three features are selected from the specificity ranking list ( $Y_1 - Y_3$ ). Features from the sensitivity list obtain more importance than the features from the specificity list. In addition, Features with a higher rank have more importance than features with a lower rank. Feature importances are reflected in the contribution of the features in the LCF. The LCF of operation mode 3 is given in (5.6).

$$LCF_{mode-3} = X_1 \cdot (Y_1 + Y_2 + Y_3) + X_2 \cdot (Y_1 + Y_2) + X_3 \cdot Y_1 + X_1 \cdot X_2 \cdot X_3 \cdot X_4 \quad (5.6)$$

The seizure detection result of operation mode 3 for patient  $ID_2$  is depicted in Figure. 5.13. The seizure detection delay is 3 seconds with a specificity of 87.8%. Although more features from more channels are extracted in operation 3, the detection delay is not improved compared to operation mode 2. In other words, consuming more energy by extracting more features from more electrode channels is not always tantamount to achieving faster seizure detection.

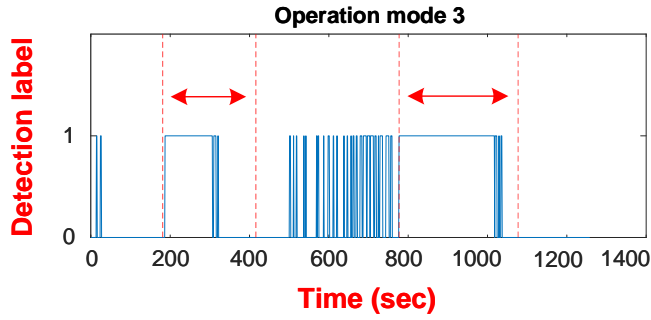


Figure 5.13: Seizure detection of ID2 under operation mode 3

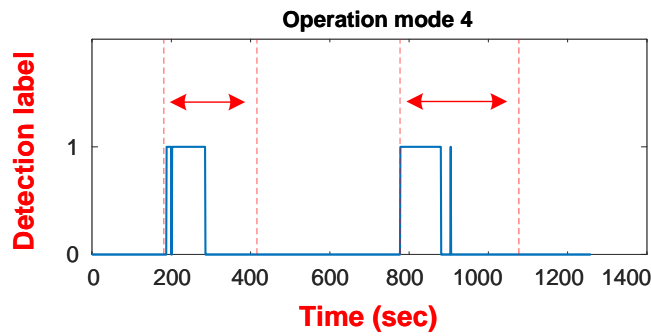


Figure 5.14: Seizure detection of ID2 under operation mode 4

In operation mode 4, the medical goal is to have minimum false positive detections and lowest power consumption. As a consequence, three features are extracted from a single iEEG channel. Since the medical target is to minimize false positive detections, the importance of features from the specificity ranking list gets higher than the importance of features from the sensitivity ranking list. Two features with the highest specificity ( $Y_1, Y_2$ ) and a feature with the highest sensitivity ( $X_1$ ) are used in the LCF. The LCF of operation mode 3 is given in (5.7).

$$LCF_{mode-3} = Y_1 \cdot X_1 + Y_1 \cdot Y_2 \quad (5.7)$$

The seizure detection result of patient  $ID_2$  in operation mode 3 is portrayed in Figure. 5.14. The seizure detector achieves 100% specificity and zero false detection which means that the medical goal is fully reached. The seizure detection latency is 4 seconds in this operation mode.

In operation mode 5, the medical goal is to have minimum false positive detection with a medium power consumption level. The number of features is increased from three to five and the number of selected channels is increased from one to three compared to operation mode 4. The majority of features (three features) are selected from the specificity ranking list

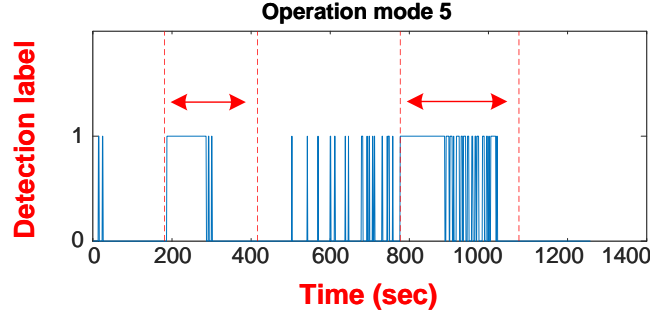


Figure 5.15: Seizure detection of ID2 under operation mode 5

and two other features are selected from the sensitivity ranking list. The logical classification function of operation mode 5 is given in (5.8).

$$LCF_{mode-5} = Y_1 \cdot (X_1 + X_2) + Y_2 \cdot X_1 + Y_1 \cdot Y_2 \cdot Y_3 \quad (5.8)$$

Seizure detection result of patient  $ID_2$  in operation mode 5 is depicted in Figure. 5.15.

We observe that the detection delay reduced from 4 seconds to 3 seconds at the expense of degrading the specificity from 100% to 95.7%.

In operation mode 6, the medical goal is to have minimum false positive detections with high power consumption. As a consequence, seven features are extracted from five iEEG channels. four features are taken from the specificity ranking list ( $Y_1 - Y_4$ ) and three features are selected from the sensitivity ranking list ( $X_1 - X_3$ ). The importance of the features from the specificity list is higher than the features of the sensitivity list because the medical target is to achieve a low false alarm rate. The LCF of operation mode 6 is given in (5.9).

$$LCF_{mode-6} = Y_1 \cdot (X_1 + X_2 + X_3) + Y_2 \cdot (X_1 + X_2) + Y_3 \cdot X_1 + Y_1 \cdot Y_2 \cdot Y_3 \cdot Y_4 \quad (5.9)$$

The seizure detection result of patient  $ID_2$  in operation mode 6 is illustrated in Figure. 5.16. It achieves a detection latency of 4 seconds and a specificity of 88.19%.

The seizure detection results associated with patient  $ID_2$  are summarized in Table .5.10. The programmable seizure detector tested on patient  $ID_2$  achieves perfect sensitivity of 100% in all operation modes. It also reaches perfect specificity of 100% in operation mode 4 and a short detection delay of 3 seconds in operation modes 2,3,5, and 6.

The proposed seizure detector with programmable feature selector, channel selector and logical classification function is tested on 10 patients from the SWEC-ETHZ dataset and

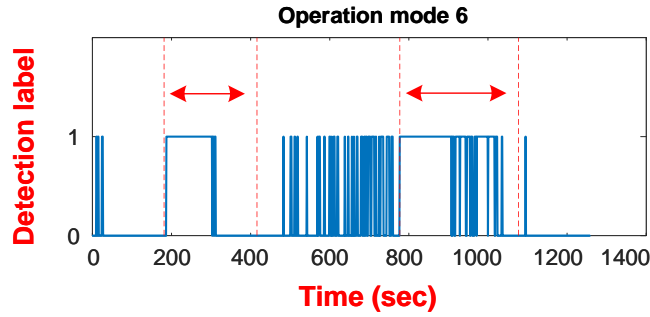


Figure 5.16: Seizure detection of ID2 under operation mode 6

Table 5.10: Results of ID2 in different operation modes

| Operation mode | Sensitivity % | Specificity % | Latency      |
|----------------|---------------|---------------|--------------|
| 1              | <b>100</b>    | 97.08         | 3.5 sec      |
| 2              | <b>100</b>    | 95.42         | <b>3 sec</b> |
| 3              | <b>100</b>    | 87.8%         | <b>3 sec</b> |
| 4              | <b>100</b>    | <b>100</b>    | 4 sec        |
| 5              | <b>100</b>    | 95.7          | <b>3 sec</b> |
| 6              | <b>100</b>    | 88.19         | <b>3 sec</b> |

Table 5.11: Comparison with the state-of-the-art

|                        | [73]'2018 | [28]'2020 | [14]'2022 | [97]'2023 | [101]'2021 | <b>This work</b> |
|------------------------|-----------|-----------|-----------|-----------|------------|------------------|
| <b>Dataset</b>         | ETHZ      | ETHZ      | ETHZ      | ETHZ      | ETHZ       | ETHZ             |
| <b>Sensitivity %</b>   | 99        | 97        | 100       | 100       | 97.1       | 100              |
| <b>Specificity%</b>    | 93.7      | 92.5      | 97.9      | 99.6      | 97         | 99.2             |
| <b>Latency (sec)</b>   | 14.9      | 14.3      | 6.6       | 9.95      | 8.46       | 3.2              |
| <b>Channel select</b>  | ×         | ×         | ✓         | ×         | ✓          | ✓                |
| <b>Feature select</b>  | ×         | ×         | ✓         | ✓         | ×          | ✓                |
| <b>Programmability</b> | ×         | ×         | ×         | ✓         | ×          | ✓                |
| <b><i>C.D</i></b>      | 65.14     | 65.14     | 11        | 221.6     | 12         | 1-35             |

the results are compared with recently published works that use the same database. The comparison results are given in Table. 5.11.

The proposed design reaches an excellent sensitivity of 100% as [14] and [97] which is better than [73], [28] and [101]. The specificity is 99.2% which outperforms [73], [28], [14] and [101]. The key achievement of the proposed seizure detector is fast detection with a very low latency of 3.2 seconds which outperforms all recently published works. It should be noted that the feature and channel selection method follows a novel programmability concept that involves user interactions. The computational dimension (*C.D*) of this work is also programmable and can be as low as 1 which is outstandingly better than the state-of-the-art.

## 5.7 Summary and Conclusions

In this chapter, the concept of programmability and user interaction in seizure detection was discussed for the first time in the literature. The challenging point is that patients' conditions evolve over time and if the seizure detection algorithms are not updated, they will fail to keep their effectiveness. In addition, seizure detection with user interactions can enhance the life quality of patients and reduce their anxiety concerning using IMDs.

To address the aforementioned challenges, a 32-bit RISC microprocessor is designed which supports R-type, I-type and J-type instructions. The instruction set of a MIPS-based RISC is customized to used in an implantable seizure detector. Three therapy modes were programmed on the RISC to realize fast detection, low false positive detection as well as a compromise between detection speed and false alarm rate.

Patients are enabled to have interaction with the programmable seizure detector by choosing therapy modes of the device that are defined by their neurologists. User interaction and giving real-time feedback to the device improves the effectiveness of therapy. Moreover, they can adjust seizure detection parameters according to their daily activities, severity and frequency of their seizures. The programmable seizure detector was implemented on an INTEL ALTERA CYCLONE V FPGA. It demonstrated a low power consumption of 0.78 mW, perfect sensitivity of 100%, high specificity of 99.6%, and detection delay of 9.95 seconds.

Besides, the programmability aspect was extended to feature selection and channel selection units. In this case, both the medical goals and power consumption of the implantable seizure detector can be adjusted by neurologists and patients. The number of selected features and number of selected channels vary from 3 to 7 and 1 to 5 according to the RISC program and user commands. Furthermore, a unique LCF was generated for each operation mode to realize specific therapy goals. The novel seizure detector with programmable feature and channel selection was assessed on 10 patients from the SWEC-ETHZ dataset and the results were compared to the state-of-the-art. It exhibits a sensitivity of 100%, a specificity of 99.2%, detection latency of 3.2 seconds with very low computational complexity between 1 to 35. The performance of the novel seizure detector outperforms the state-of-the-art.



# 6 Digital Charge Balancing for Neurostimulation

## 6.1 Introduction and Motivations

Neurostimulation is an essential part of a closed-loop epilepsy control device. Neurostimulation evokes action potentials in the brain tissue. As a consequence, the neural activity of the brain is modulated which can be helpful to cancel/suppress upcoming/detected seizures. Electrical neurostimulation methods are categorized into three groups that are explained hereunder [75].

### 1. Voltage-mode electrical stimulation

The principal parameter of voltage-mode stimulation is the amount of voltage that is applied across the target tissue. The amplitude of the voltage across the tissue determines the strength of the electrical field and the force exerted on ions within the tissue. The electrical field generation leads to cellular depolarization and nerve activation to enable neural activity modulation for seizure control.

### 2. Current-mode electrical stimulation

The main circuit parameter in current mode stimulation is the amount of current flowing through the tissue. The amount of current determines the amount of charge delivered to the tissue over time. The current injection leads to cellular depolarization and neural activity modulation.

### 3. Charge-mode electrical Stimulation

In charge-mode electrical stimulation, the key parameter is the amount of charge delivered to the tissue. Charge-mode stimulation adopts a bank of capacitors to deliver discrete packets of charges for neural excitation.

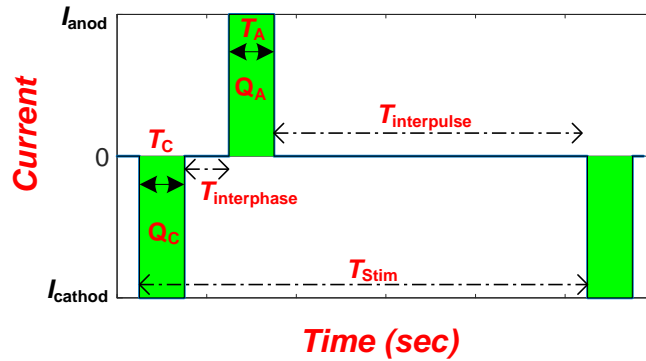


Figure 6.1: Timing diagram of biphasic current stimulation

Constant-current electrical stimulation is the most frequently-used mode of neurostimulation because of its accurate charge transfer profile, resiliency to interface impedance fluctuation, and compact implementation [53]. Although constant-current neurostimulation offers accurate charge transfer, it suffers from the lack of control over the residual voltage over electrode-electrolyte interface [102].

Constant-current electrical stimulators employ biphasic current pulses to achieve charge neutrality. Biphasic current stimulation waveforms are shown in Figure. 6.1.  $T_C$  and  $T_A$  are the periods of cathodic and anodic phases, consecutively.  $T_{interphase}$  is the delay between the cathodic and anodic phases.  $T_{interpulse}$  is the resting time between two consecutive stimulation cycles with the stimulation period of  $T_{stim}$ .

In biphasic current stimulation, a desired action potential is generated by injecting cathodic current pulses. Subsequently, anodic pulses are injected to release the injected charge and achieve charge neutrality. It is worth noting that inevitable charge imbalances will accumulate on electrodes even with perfect circuit matching and symmetric electronic design. The reason for the charge imbalance accumulation originates from some unavoidable device mismatches and interface impedance fluctuation [51, 103]. Therefore, the net delivered charge is not equal to zero and imbalance charge accumulation may lead to detrimental consequences over long-term neurostimulation.

The adverse effects of residual voltage accumulation on the electrode-tissue interface are discussed hereafter.

- **Tissue damage:** One of the most significant concerns associated with charge imbalances is tissue damage. Unbalanced charge delivery induces excessive chemical reactions and electrolysis which contributes to tissue damage.
- **Electrode corrosion:** Charge imbalances accumulation leads to the corrosion of electrodes over time. Electrode corrosion releases metal ions into the tissue which can cause tissue inflammation. Moreover, corroded electrodes may change the electrode impedance which affects stimulation efficacy.

- **Neural excitotoxicity:** Excessive charge accumulation due to a large amount of charge imbalances can overstimulate the neurons leading to neural excitotoxicity. Neural excitotoxicity worsens neurological symptoms and affects the effectiveness of electrical stimulation.
- **Electrode longevity:** Charge imbalances accelerate the degradation of electrodes and reduce the lifespan of the device. As a result, electrode longevity is shortened which necessitates an extra replacement surgery.
- **Treatment efficacy degradation:** If charge balance is not maintained during neurostimulation, the desired neural response may not be achieved.

Thus, a charge balancer plays a crucial role to ensure safe neurostimulation for long-term use of the device. Charge balancing techniques are divided into passive and active methods. Using DC-blocking capacitors and electrode shorting are common passive charge balancing methods that suffer from disadvantages such as stimulation frequency limitation and unintended stimulations.

In active charge-balancing techniques, the amount of residual voltage accumulated on electrode-electrolyte interface is continuously monitored. Subsequently, the charge neutralization process takes place based on the measured accumulated charge. Anodic pulse modulation and balance current injection are two widely used active charge balancing techniques. The main challenges of conventional active charge-balancing techniques are stated hereunder.

- The amount of charge that can be neutralized using existing analog techniques is limited. Thus, large imbalances may require multiple stimulation cycles to be entirely neutralized [51, 103].
- Available digital charge balancing techniques require continuous operation of an ADC leading to high power consumption.
- Offset current injection during entire interpulse resting intervals remarkably increases the power consumption of stimulators.

## 6.2 Charged-balanced Electrical Stimulation

Conventional neural stimulators are made up of a current DAC, an output current driver, and a level shifter. The framework of a charged-balanced current-mode electrical stimulator is depicted in Figure 6.2. The proposed digital charge balancing processor interferes with the stimulator DAC to control input digital codes, with the output current driver to manage balance current injection and with the electrode-electrolyte interface to sense the residual potential on the electrodes.

It should be noted that a model of the stimulator is used in this chapter to assess the performance of the proposed digital charge balancer. An output current driver is a principal

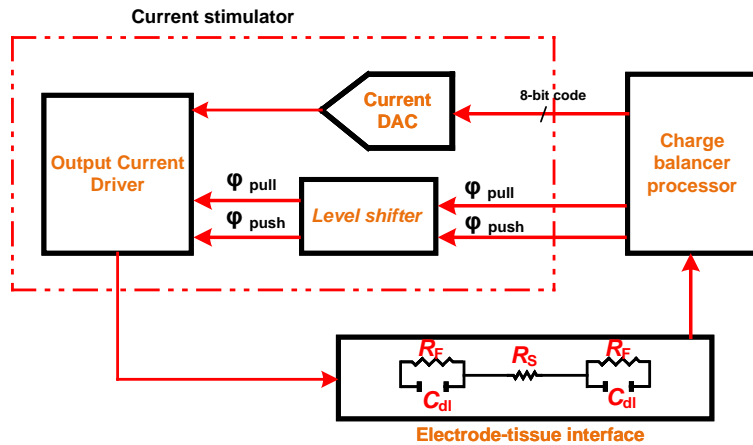


Figure 6.2: Topology of a charged-balanced electrical stimulator

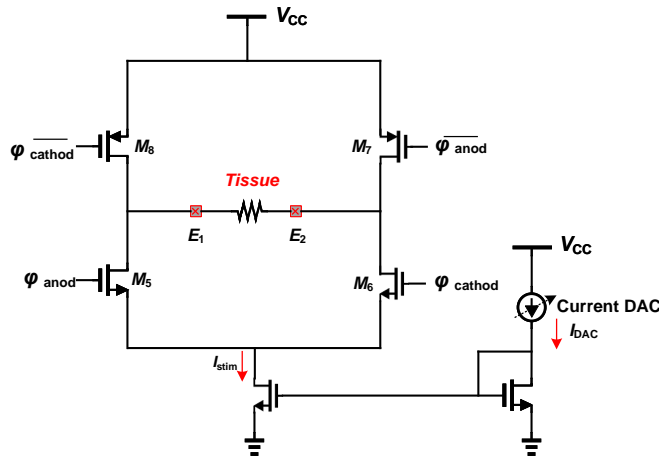


Figure 6.3: Simplified circuit-level implementation of the output current driver

component of a current-mode electrical stimulator. The simplified circuit-level implementation of an output current driver is shown in Figure. 6.3. The role of the output current driver is to deliver current pulses to the tissue through electrodes. This current can be delivered in a the cathodic phase, an anodic phase, or interpulse intervals for charge balancing.

Modern electrical stimulators exhibit high-voltage compliance greater than 12 volt [51]. The available techniques to implement high-voltage compliance electrical stimulators in the standard CMOS Technology are dynamic gate biasing and transistor stacking.

The level shifter is in charge of increasing the voltage level of digital control signals to be used in high-voltage compliant output current driver. For instance, the digital signal  $\varphi_{pull}$  is converted from 0 ~3.2 volt to 9.6 ~12.8 volt in [24] and the shifted signal is delivered to stack PMOS transistors.

The current-steering DAC plays a significant role in low-power charge-balancing systems. It

generates desired current pulses according to its input code. In this work, a current DAC with a maximum current of 1 mA and 8-bit resolution is modeled in the system. Therefore, the Least-Significant Bit (LSB) of the current DAC is calculated at 3.9  $\mu A$ .

The electrode-tissue model is illustrated in Figure. 6.2. It comprises a Faradaic resistance ( $R_F$ ), a double-layer capacitor ( $C_{dl}$ ), and a tissue resistance  $R_S$ .

The Faradaic resistance represents the impedance arising from electrochemical reactions. When an electrode is applied to a biological tissue, the current flows through the electrode and electrochemical reactions take place due to ions movement. This reaction contributes to the overall impedance of the electrode-electrolyte interface. Thus, the  $R_F$  represents the resistive component of this electrochemical reaction.

The double-layer capacitor represents capacitive effects due to the separation of charges at the electrode-tissue interface. The non-Faradaic process at the interface involves capacitive effects because of charge accumulation. The double-layer capacitor refers to a region of charge separation between the electrode surface and the electrolyte solution. This region has two layers called the Helmholtz and diffuse layers.

The tissue impedance is represented by the  $R_S$  component. The electrode-brain interface model depicted in Figure. 6.2 is a simplified interface model. [104] demonstrates the frequency dependency of BCIs. Indeed, the interface impedance varies in time and frequency. According to [104], the effect of this phenomena is more crucial in recording electrodes rather than stimulating electrodes since the charge injection removes biological materials accumulated on the electrodes.

[105] quantifies the electrode-tissue interface impedance using in-vitro and in-vivo measurements.  $R_f$  and  $C_{dl}$  are dependent to the stimulation frequency and their magnitudes are decreased as the stimulation frequency increases. However, the ratio of capacitive and faradaic charge transfer is still relatively constant. Moreover, increasing the current density reduces the  $R_f$  and increases the  $C_{dl}$ . [105] demonstrates that the  $R_f$  varies between 1  $k\Omega$  - 100  $k\Omega$ . In addition, the  $C_{dl}$  varies between 100 nF – 100  $\mu F$  in real-time based on frequency variation.

In this chapter, an interface model with  $R_s = 10 k\Omega$ ,  $R_f = 100 k\Omega$ , and  $R_s = 10 k\Omega$  is used. The focus of this chapter is to design a digital charge balancer that is described in the following section.

### 6.3 Digital One-Shot Active Charge Balancing

The primary goal of this section is to propose an accurate power-efficient charge-balancing system. Currently available charge-balancing circuits for current-mode electrical stimulators employ pulse modulation and balance current injection which suffer from the following points.

- **Drawbacks concerning offset current injection**

Offset current injection may lead to unintended tissue stimulation which affects the treatment efficacy. Unwanted stimulation caused by offset current injection is largely dependent on the amplitude of the balance current.

- **Drawbacks concerning current pulse modulation**

The accuracy of charge neutralization by anodic pulse modulation mainly relies on the DAC specifications such as maximum stimulation current and DAC resolution. As a consequence, precise charge balancing may not be achieved using conventional DACs available in the market.

We aim to strike a compromise between safety, accuracy, and power consumption by a hybrid method of charge neutralization. In the novel hybrid method, large persistent charge imbalances are neutralized using a combination of anodic pulse amplitude modulation and offset current injection techniques [75]. Furthermore, small charge imbalances are canceled by injecting a low-amplitude offset current for a short time during interpulse intervals.

A remarkable proportion of charge-balancing power consumption relates to the power consumption of the ADC. In this work, we propose a one-shot method of charge neutralization which means that the ADC takes a sample per stimulation cycle instead of continuously sampling compared to the state-of-the-art [53, 69]. Moreover, the activation time of the charge-balancing system is minimized using a novel dual-thresholding approach.

### 6.3.1 Residual Voltage Regions with a Dual-thresholding Technique

A challenging point in designing charge-balancing systems is to define a proper safe voltage threshold for residual potentials accumulated on the electrodes. Conventional charge-balancing systems use  $\pm 50\text{ mV}$  and  $\pm 100\text{ mV}$  residual voltage thresholds [51]. A crucial consideration concerning having a single threshold is the risk of returning to the unsafe region after each stimulation phase.

A dual-thresholding method associated with the hybrid charge balancing system is presented. In the dual-thresholding approach, a threshold is defined based on the anodic pulse modulation method ( $V_{th1}$ ), and a threshold is defined according to the offset current injection method ( $V_{th2}$ ). As a result, residual voltages are divided into five regions with respect to  $V_{th1}$  and  $V_{th2}$ . The operation regions are illustrated in Figure .6.4.

The charge-balancing processor assigns the measured residual voltage to a particular operation region according to its amplitude.  $R_{up}$  and  $R_{un}$  are two unsafe regions with positive residual voltage and negative residual voltage, respectively. Three regions ( $R_s$ ,  $R_{sp}$ , and  $R_{sn}$ ) are considered as the safe regions. The charge balancing conceptual diagram is demonstrated in Figure. 6.5.

The ADC samples the residual voltage after each anodic phase and the residual voltage ampli-

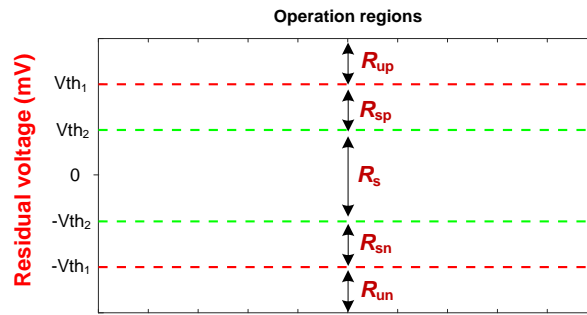


Figure 6.4: Operation regions of the charge balancer

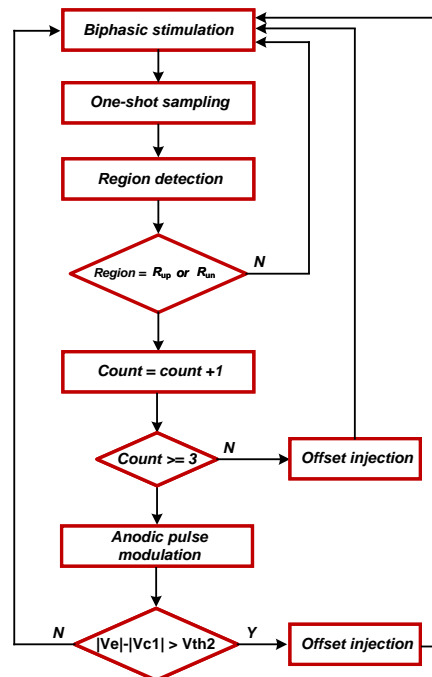


Figure 6.5: Charge-balancing flowchart

tude is delivered to the digital charge balancer. The charge balancing processor determines the operation region according to  $V_{th1}$  and  $V_{th2}$ . If the residual voltage is located in the  $R_{up}$  or  $R_{un}$  regions, the charge balancer will be activated.

The charge balancing processor evaluates whether the residual voltage is persistent or not using the *count* variable. When  $count \geq 3$ , it means that the residual voltage stays in an unsafe region for three consecutive stimulation periods. Then, a combination of anodic pulse modulation and balance current injection will neutralize the large persistent imbalances. The hybrid charge neutralization method takes place in two steps. First, the charge-balancing processor calculates the amount of required amplitude modulation to lower the residual voltage below  $|V_{th1}|$ . It brings the residual voltage to region  $R_{sp}$  and  $R_{sn}$ . Second, the charge balancing processor computes the duration of offset current injection to lower residual voltage

below  $|V_{th2}|$  and brings it back to the  $R_s$  region.

Anodic pulse modulation is only carried out when imbalances are persistent. As a result, large imbalances, which originate from a random process and they are observed in only a single stimulation phase, do not cause pulse modulation.

To compensate large non-persistent imbalances ( $count < 3$ ), a balance current injection with the maximum duration is performed to neutralize charge imbalances. In addition, if the residual voltage is in the  $R_s$ ,  $R_{sp}$ , or  $R_{sn}$  regions, the charge balancer is not activated which is highly beneficial for power saving.

### 6.3.2 Anodic Pulse Modulation

The anodic pulse amplitude is modulated to keep the net delivered charge close to zero in the anodic pulse modulation charge-balancing technique. The key advantage of anodic pulse modulation over other approaches is that it does not inject any additional pulse or DC-current during interpulse intervals. As a result, it does not increase the power consumption of the system due to additional current injection. The effectiveness of anodic pulse modulation charge balancing depends on the following factors:

1. **Maximum stimulation current**

The maximum stimulation current of 1 mA is considered for the DAC model.

2. **DAC resolution**

A DAC with an 8-bit resolution is considered

3. **Electrode type**

A platinum electrode model with a double-layer capacitor of 100 nF is considered.

The stimulation frequency and duty cycle are other critical factors that play roles in effectiveness of anodic pulse modulation. We consider a high stimulation frequency of 100 Hz with a 10% duty cycle. Consequently, the stimulation period is 10 ms with 500  $\mu$ s anodic and cathodic phases.

As mentioned in the previous section, the  $V_{th1}$  is defined based on the anodic pulse modulation. The  $V_{th1}$  is the minimum residual voltage that can be compensated by pulse amplitude modulation. The  $V_{th1}$  is calculated in (6.1).

$$V_{th1} = \frac{I_{LSB} \times t_{anod}}{C_{dl}} = \frac{3.9 \mu A \times 0.5 ms}{100 nF} = 20 mV \quad (6.1)$$

Where  $I_{LSB}$  is the least-significant bit current of the DAC which is equal to 3.9  $\mu$ A.  $T_{anod}$  is the duration of anodic pulse insertion which is 5 ms with a 10% duty cycle.

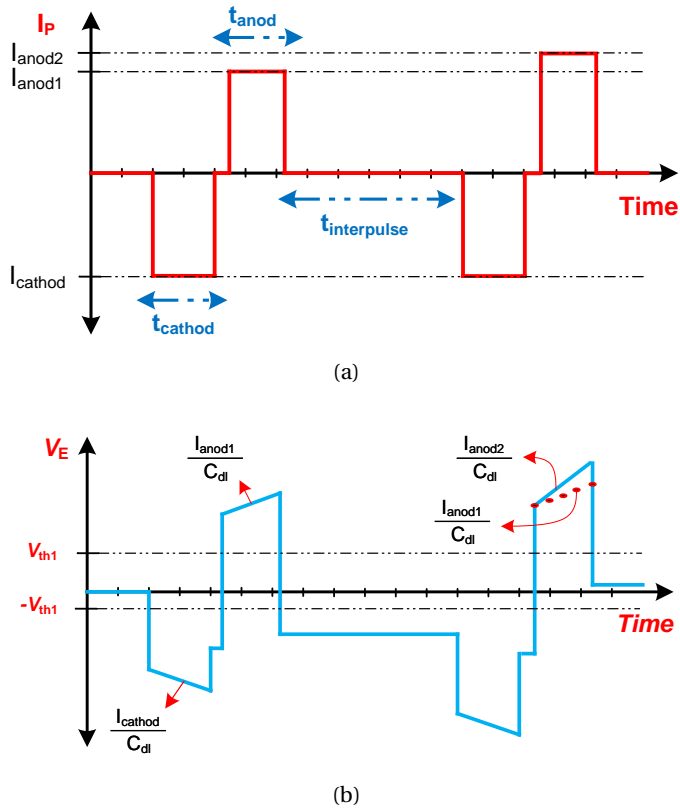


Figure 6.6: Anodic pulse amplitude modulation; (a) current profile, and (b) voltage profile

The concept of anodic pulse modulation is shown in Figure. 6.6. In the first stimulation phase, anodic and cathodic current pulses have the same amplitude ( $I_{anod1} = I_{cathod}$ ). Since the amplitude of current pulses is equal, the rate of electrode voltage decrement in the cathodic phase and electrode voltage increment in the anodic phase are the same. As shown in Figure. 6.6.b, the residual voltage after the first stimulation phase is lower than  $-V_{th1}$ . Thus, the charge balancing processor detects the operation region of the stimulator as  $R_{un}$ . In the following stimulation phase, the amplitude of the anodic pulse is increased to  $I_{anod2}$  to compensate the negative accumulated residual voltage of the previous stimulation phase. This current increment leads to a change in the slope of the electrode voltage waveform shown in Figure. 6.6.b. It is worth mentioning that the cathodic pulse amplitude will be chosen according to therapeutic goals and it is not influenced by the charge-balancing pulse modulation strategy.

Furthermore, the suggested pulse amplitude modulation technique is not affected by large charge imbalances that have random origins. That is why the charge balancing processor uses offset current injection for non-persistent large imbalances.

### 6.3.3 Offset Balance Current Injection

The purpose of offset balance current injection is to inject low-amplitude dc-current during

interpulse resting intervals to enable accurate charge neutralization. Two critical points involving offset current injection for charge balancing are offset current amplitude and duration of offset current injection which are explained hereunder.

- **Offset current amplitude:** The amplitude of the balance DC-current must be low enough to avoid unwanted stimulation and affecting treatment efficacy.  $1 \mu A$  offset current amplitude is considered for charge balancing.
- **Offset current duration:** A tradeoff exists between charge balancing accuracy and power consumption in defining offset current injection duration. In this work, 10% of the stimulation period is considered as the maximum duration of the balance current injection to reduce the power consumption as well as keep the charge balance accuracy equal to 10 mV.

As shown in the charge balancing flowchart, offset current injection is done in two conditions. These two conditions are illustrated in Figure. 6.7. In the first stimulation phase, the residual voltage is in the operation region of  $R_{un}$  and the charge balancing processor detects it as non-persistent residual voltage. Thus, the offset dc-current is injected for the maximum duration ( $t_{balance-max} = 1 ms$ ). In this case, the residual voltage is lowered within  $-V_{th1} < V_{res} < -V_{th2}$ .

In the second stimulation phase of Figure. 6.7, a combination of anodic pulse modulation and balance current injection is used for charge balancing. Anodic pulse modulation brings the residual voltage to the operation region of  $R_{sn}$ . Subsequently, a time-limited offset current injection brings the operation region to  $R_s$ .

The amplitude of  $V_{th2}$  is defined considering offset current injection.  $V_{th2}$  is regarded as the maximum amount of residual voltage that can be neutralized by offset current injection.  $V_{th2}$  is calculated in (6.2).

$$V_{th2} = \frac{I_{offset} \times 0.1 \times t_{stim}}{C_{dl}} = \frac{1 \mu A \times 0.1 \times 10 ms}{100 nF} = 10 mV \quad (6.2)$$

#### 6.3.4 FPGA implementation of the charge-balancing processor

The proposed digital charge-balancing processor is implemented on a Cyclone IV FPGA and measurement results are obtained using an Analog Discovery 2 device. The hardware implementation architecture is demonstrated in Figure. 6.8. The measured residual voltage is the input of the charge balancing processor. The charge balancer determines the region of residual voltage and delivers it to the processing unit of the charge balancer.

If the residual voltage is in the unsafe regions, charge balancing will be activated. In this case, the charge-balancing processor is in charge of generating  $\varphi_{pull}$ ,  $\varphi_{push}$ , and  $I_{anod-modul}$  signals. The  $\varphi_{pull}$  and  $\varphi_{push}$  signals control the timing of offset current injection with

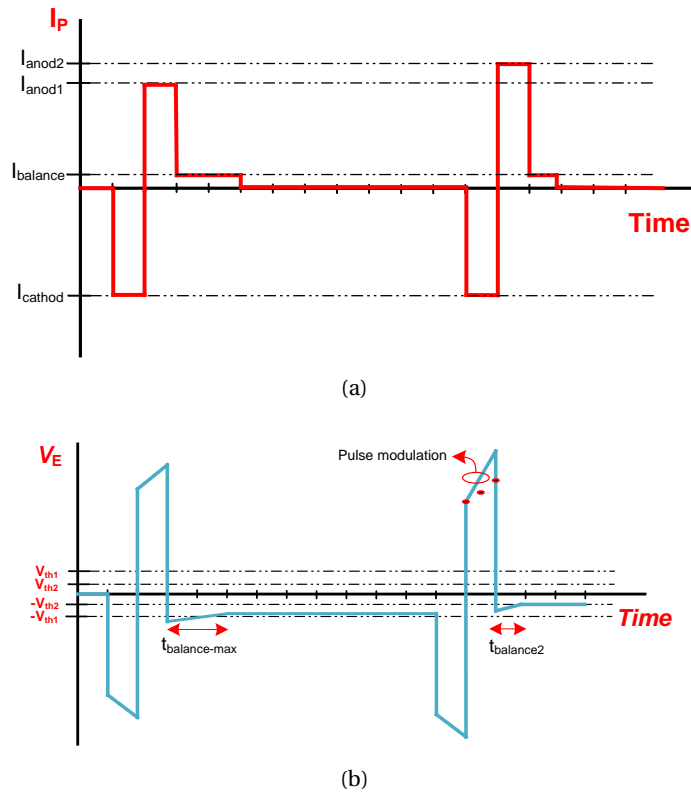


Figure 6.7: Offset balance current injection

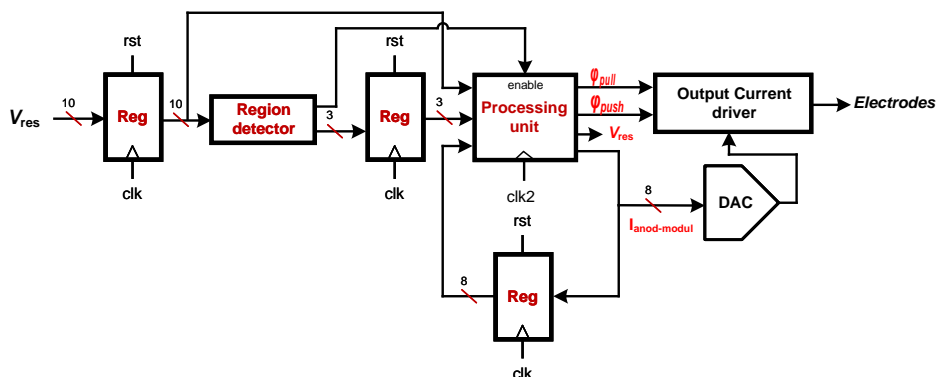


Figure 6.8: Hardware implementation architecture of the charge-balancing processor

negative and positive polarities, respectively. These control signals, which are generated by the processing unit of the digital charge balancer, are given to the output current driver to deliver dc-offset currents during interpulse resting intervals.

$I_{anod-modul}$  is an 8-bit width signal that performs anodic pulse modulation for charge balancing. This signal is delivered to an 8-bit current DAC to generate proper anodic pulses. The system uses two clock signals. The first clock ( $clk$ ) has a frequency of 100 Hz equal to the

Table 6.1: FPGA implementation parameters of the charge balancer

| Num of logic elements | Num of registers       | Processor frequency | Dynamic power |
|-----------------------|------------------------|---------------------|---------------|
| 2439                  | 1206                   | 1 MHz               | 0.76 mW       |
| Stimulation frequency | Electrode model        | Tissue impedance    | Memory bits   |
| 100 Hz                | 100 nF    1 M $\Omega$ | 10 K $\Omega$       | 27648         |

stimulation frequency. The clock signal of the processing unit ( $clk_2$ ) is 1 MHz. The FPGA implementation parameters are given in Table .6.1.

The measured FPGA implementation results are demonstrated in Figure. 6.9. The results of charge-balancing for 1 second with 100 cycles of stimulation are given. 15 mV offset residual voltage is manually added to each stimulation phase to verify the charge balancing performance to keep the residual voltage within the safe window. The initial amplitude of the anodic pulse is similar to the cathodic pulse amplitude which is  $100 \times I_{LSB}$ . The interface model presented in Section 6.2 is used to calculate the accumulated potential.

Figure. 6.9.a shows the amplitude of anodic pulses during 100 stimulation cycles. The charge imbalances cause changes in the anodic pulse amplitude. The anodic pulse amplitude settles at an amplitude of  $91 \times I_{LSB}$  at  $t=400$  ms. Since the polarity of the offset residual voltage in each stimulation phase is positive, anodic pulse modulation decreases the amplitude of the anodic phase to enable charge neutralization.

Figure. 6.9.b shows the  $\phi_{pull}$  control signal. when the  $\phi_{pull}$  signal is high, balance current with negative polarity is injected during interpulse intervals to reduce the residual voltage. We consider 10% of stimulation time as the maximum allowed time for offset current injection. However, Figure. 5.9.b reveals that the  $\phi_{pull}$  is high only for 53.2 ms during a 1-sec experiment which is highly beneficial to have an energy-efficient charge balancing. The charge-balancing processor consumes 0.76 mW which is compatible for low-power implantable applications.

Figure. 6.9.c illustrates the residual voltage computed by the charge balancing processor. It discloses that the proposed digital one-shot charge balancer is able to successfully maintain the residual voltage in the operation region of  $R_s$  in spite of applying a large offset residual voltage of 15 mV for each stimulation phase thanks to the hybrid digital charge balancing method. It is noteworthy that residual voltage of 1.5 V will accumulate after 100 cycles of stimulation without the charge balancer.

## 6.4 Summary and Conclusions

In this chapter, the necessity of charge balancing for safe long-term electrical stimulation in closed-loop epilepsy control implants was discussed. Neglecting small imbalances accumulated on electrodes in each stimulation phase will lead to adverse consequences such as tissue damage, electrode damage and, treatment efficacy degradation in the long run.

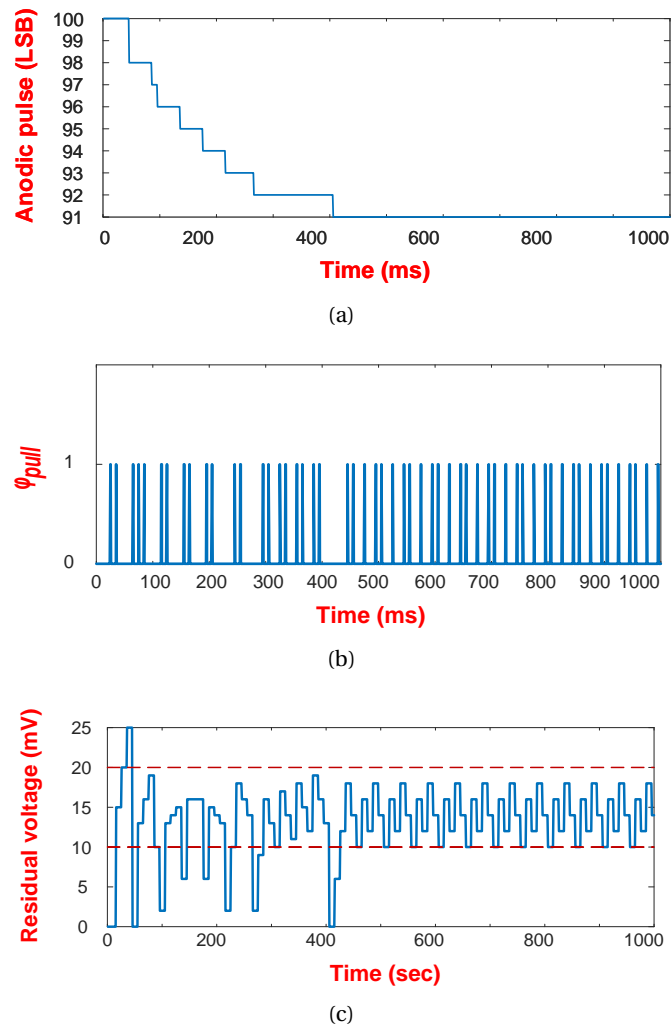


Figure 6.9: (a) Anodic pulse modulation, (b) Offset current control signal, and (c) Residual voltage after charge balancing

The shortcomings of currently available active charge-balancing techniques were described in this chapter. Recent charge-balancing systems follow adaptive algorithms for continuous monitoring of residual voltage. They mainly employ pulse modulation and offset current injection to neutralize the residual charges and keep the net delivered charge close to zero at the interface. However, anodic pulse modulation is not sufficient to cancel small imbalances. Furthermore, offset current injection during interpulse intervals involves unintended stimulation, more power consumption, and stimulation frequency limitation.

This chapter proposed a one-shot digital charge balancer using a hybrid method of anodic pulse modulation and balance current injection to strike a balance between safety, accuracy, and power consumption. Moreover, a novel dual-thresholding technique was presented to achieve energy-saving and charge-balancing accuracy simultaneously. In the dual-thresholding method, two thresholds were defined based on anodic pulse modulation

and offset current injection. The charge balancing is divided into five regions in which anodic pulse modulation is performed to neutralize large persistent imbalances and offset DC-current injection is employed to cancel small and non-persistent imbalances. The injection of offset balance current is limited to 10% of stimulation time to avoid excessive power consumption.

The proposed charge balancing processor was implemented on a Cyclone IV FPGA and measurement results disclosed the effectiveness of the presented algorithm to accurately maintain the residual voltage within the safe region by anodic pulse modulation as well as offset current injection during 5% of experiment time.

## 7 Conclusions and Future Work

The main objective of this thesis is to explore advanced digital signal processing and machine-learning approaches with low hardware implementation complexity well-suited for closed-loop epilepsy control implants. In this research, we propose novel techniques to establish a balanced tradeoff between seizure detection accuracy, seizure detection latency, hardware complexity of the algorithms, and power consumption. Furthermore, epileptic seizure detectors are followed by neurostimulators in closed-loop epilepsy control systems. In this dissertation, we explore active charge balancing methods to guarantee safe long-term operation of neurostimulation as well as minimize the power consumption of the charge balancing system.

**Chapter 3** discussed the system-level modeling of a closed-loop wirelessly-powered seizure control implant for the first time in the literature. Different components including LNA, LPF, gain stage, sample and hold, compressive sensing, ADC, bio-signal processor, stimulator, and controller were modeled using Simulink software. Important parameters of each component such as gain, bandwidth, number of features, number of recording channels, and number of stimulation channels were studied to achieve specific design goals. In particular, a controller unit was employed to manage the temperature elevation of the device. The model was tested on patients with different stimulation current amplitudes and 12 stimulation channels. The controller has successfully adjusted the number of stimulation channels according to the required stimulation amplitude and the temperature rise was maintained below 1°C limit.

**Publications:** The research presented in Chapter 3 resulted in two conference publications that are expressed hereunder.

1. The first model of implant focusing on seizure detection and temperature control was presented at the 2021 4th International Conference on Bio-Engineering for Smart Technologies (BioSMART). I received the BEST PAPER AWARD of the conference for this paper.

2. The second version of the implant model resulted in a conference paper presented at the 2022 IEEE Biomedical Circuits and Systems Conference (BioCAS). The main focus of this paper is on epileptic seizure detection using wireless data and power transmission.

In **Chapter 4**, a challenging tradeoff between seizure detection accuracy and hardware compatibility of seizure detectors was addressed. Advanced seizure detection algorithms mainly encounter limitations in the number of logic resources and power budget. The compromise between the number of extracted features in the DSP unit and energy consumption was fully studied in this chapter. We suggested a two-stage patient-specific seizure detection technique which extracts multiple features in an energy-efficient way. The two-stage feature extractor was implemented on an FPGA and tested on patients from the SWEC-ETHZ dataset. Accurate and low-power seizure detection was obtained by extracting three features in monitoring and detection stages in which the detection stage was activated during only 27.2% of the experiment time to enable energy efficiency.

Novel feature and channel selection algorithms were proposed to find an optimal patient-customized subset of features as well as the most informative electrode channels in Chapter 4. The novel MDMR algorithm can successfully select the most discriminating features with minimum redundancy from a feature pool. Furthermore, electrode recording channels were ranked and selected according to the C.E.R metric. The seizure detector with novel feature and channel selection algorithms is implemented on an Intel FPGA and tested on patients from the SWEC-ETHZ dataset. The FPGA implementation results of the proposed seizure detector evidenced higher specificity, lower detection delay and better  $FoM_{SD}$  compared to the state-of-the-art.

The computational complexity of seizure detectors plays a pivotal role in real-time low-power hardware implementation of signal processing algorithms. We proposed a novel correlated method of feature and channel selection not only to reduce the computational complexity but also to enhance the seizure detection performance. This work achieves a very low  $C.D$  of 4 which considerably outperforms the state-of-the-art in terms of computational complexity and execution time.

In the final section of Chapter 4, hardware implementation of seizure detectors using machine-learning classifiers was investigated. RF classifiers have demonstrated high seizure detection performance. The main disadvantage of the RF classifier is the large number of logic resources that is needed for hardware implementation. This thesis presented an effective solution to optimize the number of trees as well as the number of decision nodes. The hardware-friendly architecture of the RF classifier was used in a seizure detector and implemented on an Intel FPGA.

**Publications:** The research presented in Chapter 4 resulted in a journal publication and three conference publications.

1. The paper concerning the novel feature and channel selection algorithms was published

in IEEE Transactions on Biomedical Circuits and Systems journal (Volume: 16, Issue: 4, August 2022)

2. The novel two-stage energy-efficient seizure detector was presented at the 2021 43rd Annual International Conference of the IEEE Engineering in Medicine & Biology Society (EMBC).
3. The proposed computational complexity reduction technique for implantable seizure detectors was presented at the 2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS).
4. Low-power FPGA implementation of the seizure detector using RF classifier was presented at the 2022 IEEE-EMBS Conference on Biomedical Engineering and Sciences (IECBES). I received the BEST PAPER AWARD of the conference for this paper.

**Chapter 5** introduced the novel programmability function in seizure detection for the first time in the literature. A 32-bit MIPS-RISC processor with five pipeline stages is implemented on an FPGA to enable the programmability property. 23 instructions are included in the instruction set of the RISC architecture compatible with the seizure detection tasks and therapy programs. Three therapy options were programmed on the RISC. The key attribute of the presented programmable seizure detector is user interaction. The patients can dynamically switch between different therapy modes defined by their neurologists in order to adjust the seizure detection latency and false alarm rate. The design was implemented on an Intel FPGA and evaluated by 10 patients from the SWEC-ETHZ dataset.

Moreover, we extended the programmability property to the feature selection unit, channel selection unit, and logical classification function. Six different therapy programs were defined to enable patients to adjust not only the seizure detection parameters but also the power consumption mode of the seizure detector. Besides, we proposed a novel method of generating logical classification functions according to the therapy modes. The algorithm was tested on 10 patients from the SWEC-ETHZ dataset. The results revealed a perfect sensitivity of 100%, specificity of 99.2%, detection latency of 3.2 seconds, and a *C.D* between 1-35 which remarkably outperforms the state-of-the-art.

**Publication:** The research on programmable seizure detection resulted in a conference paper presented at the 2023 IEEE 14th Latin America Symposium on Circuits and Systems (LASCAS).

**Chapter 6** discussed active charge-balancing techniques for implantable neurostimulators. A charge-balancing processor was presented that enables a hybrid method of charge balancing using anodic pulse modulation and offset balance current injection. The proposed digital charge-balancing method established a balanced tradeoff between the power consumption, safety, and charge-balancing precision. We tackled the issue related to the high power consumption of using an ADC in adaptive charge-balancing algorithms by proposing the one-shot charge balancer. Moreover, the proposed dual-thresholding strategy categorizes the

residual voltages into five regions and makes a balanced tradeoff between the charge balancer power consumption and safety. The thresholds are defined based on anodic pulse modulation and offset current injections. The digital one-shot charge balancer was finally implemented on an Intel Cyclone IV FPGA.

**Publication:** The research on the digital charge-balancing processor resulted in a conference publication presented at the 2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME).

## 7.1 Future work

The study of digital signal processing on iEEG signals for epileptic seizure detection compatible with implantable medical devices can be continued and complemented in different ways. Some interesting topics for the continuation of this research are suggested in the following.

- This dissertation employs various types of time-domain features in the feature pool of the seizure detector. Different types of frequency and time-frequency features can be added to the feature pool to study their seizure detection compatibility.
- Using frequency-domain features in the feature pool of seizure detectors involves time-domain to frequency-domain signal conversion. The available frequency to time domain conversion algorithms require optimization in terms of energy consumption to be compatible with low-power seizure control implants.
- The RF classifier is the only machine-learning-based classifier that has been implemented in this dissertation. Optimizing the architecture of other classifiers such as Logistic regression, Decision trees, linear and nonlinear SVM, and ANN for low-power resource-constraint hardware implementation is an interesting field of research to complement this dissertation.
- An ensemble method of classification for seizure detection can be used as a continuation of this research. For this aim, an optimized classification method must be achieved for different feature types.
- Programmable seizure detection is a unique concept that is presented for the first time in this dissertation. It can be improved in many aspects to obtain different medical goals according to epileptologist decisions. In addition, the usability aspect of the device is of paramount importance to enable fast and effective interactions between patients and the implant.
- Security and data privacy are two important factors that must be taken into account in designing implantable seizure control devices with wireless power and data transmission as a continuation of this research.
- Finally, the programmability feature enabled by the RISC microprocessor can be ex-

tended to other components of the implant such as AFE recording channels and stimulator.

In summary, the research presented in this dissertation contributes to bridging the gap between the software design of advanced signal processing algorithms and the hardware realization of these algorithms, compatible with implantable biomedical devices. The proposed signal processing and machine-learning techniques can enhance not only the performance of devices used to notify patients of upcoming seizure events but also the performance of closed-loop seizure control implants. This research contributes to the improvement of various seizure detection parameters, such as latency, sensitivity, specificity, and accuracy, all of which greatly enhance the quality of life for patients. Moreover, I anticipate that the energy efficiency achieved by the proposed algorithms can significantly increase the lifespan of epilepsy control implants. As a result, patients can avoid frequent brain surgeries and hospitalizations.

We believe that this research paves the way for hardware implementation of more advanced signal processing, machine learning, and artificial intelligence algorithms in biomedical domain. These advancements will not only benefit epilepsy control implants but also other wearable or implantable devices used for various neurological disorders, such as Alzheimer's and Parkinson's diseases.



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# KEYVAN FARHANG RAZI

Digital/Mixed-signal IC Design Engineer

@ k.farhang.razi@gmail.com

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Renens, Switzerland

## EXPERTISE

- Low-power IC design
- Digital signal processing
- RISC microprocessor
- VHDL
- PCB design
- FPGA implementation
- RF IC design
- Arduino MCU
- C++

## SOFT SKILLS

Team-working

Multi-tasking

Group leader

Mentoring

## LANGUAGES

**English:** Advanced

**French:** Intermediate

**Persian:** Native

## SOFTWARES

Quartus

Questa Sim

Latex

Cadence

MATLAB

Altium

Simulink

SPICE

ADS

## ACHIEVEMENTS

**Best Paper Award:** IECBES  
2022 Conference, Malaysia

**Best Paper Award:** BioSMART  
2021 Conference, Paris, France

**2nd Rank of the University:**  
Master of Science education

## ABOUT ME

Creative and organized Electronics Engineer experienced in Digital/Mixed-signal IC design with high interest in hardware and FPGA implementation of digital signal processing algorithms.

## EDUCATION

### PhD - Electrical and Electronic Engineering | EPFL

Oct 2019 – Present

Lausanne, Switzerland

**Thesis:** Hardware implementation of digital signal processing algorithms for programmable epilepsy control system

### Master of Science - Electronics Integrated Circuits | Amirkabir University of Technology

Sep 2017 – Sep 2019

Tehran, Iran

**Thesis:** Design and Simulation of RF Energy Harvesting Circuit for Powering Sensors in Wireless Sensor Network

- **GPA:** 18.82/20

### Bachelor of Science - Electronics Engineering | Amirkabir University of Technology

2011 – 2016

Tehran, Iran

**Thesis:** Analysis and Simulation of an Opto-Electronic Mixer in RF Frequency Band

- **GPA of last two years** 17/20

## EXPERIENCES

### Researcher at Biomedical Microelectronic Systems Lab

2019–2023

EPFL, Switzerland

### Signal processing & FPGA project supervisor

2020–2023

BNMS Group, Switzerland

### Researcher at Radio-Frequency IC Lab

2017–2019

Amirkabir University of Technology, Iran

### Internship at VLSI Lab

Jul-Sep 2016

Amirkabir University of Technology, Iran

## SELECTED PROJECTS

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- Design of an automatic epileptic seizure detection system using time-domain feature extraction techniques
- FPGA implementation of a dynamic two-stage signal processing for low-power epilepsy implants
- Hardware Design of a 32-bit RISC Microcontroller for biomedical applications
- Designing and simulation of a comparator in 90nm CMOS Technology
- IEEG signal processing using time-frequency domain feature extraction in MATLAB
- Patient-specific time-domain feature extraction of six patients on Cyclone V FPGA
- Simulink system-level modeling of a closed-loop implantable epilepsy control device
- FPGA implementation of a programmable seizure detector with user interactions using a 32-bit MIPS-based RISC processor
- Design and simulating a fully differential two-stage OTA to be used in the front-end of an 8-bit pipelined A/D converter as a switched-capacitor sample and hold circuit in 90nm CMOS Technology
- Simulink modeling of the temperature elevation and power consumption of medical implantable devices
- Hardware implementation of a two-step feature ranking and selection algorithm using time-domain features
- Design a digital charge-balancing circuit for safe implantable electrical stimulation on Cyclone IV FPGA
- Developing an efficient data reduction technique for low-power resource-constraint biomedical implants
- FPGA implementation of a low-power accurate seizure detector with channel selection and feature ranking techniques
- Designing 12-bit analog to digital converter with Pipeline Architecture and 200 MS/s rate
- FPGA implementation of a low-power hardware-friendly Machine learning classifier for an implantable device
- Design and simulating a fully differential two-stage OTA to be used in the front-end of an 8-bit pipelined A/D converter as a switched-capacitor sample and hold circuit in 90nm CMOS Technology
- Designing and Simulating a zero-IF receiver which consists of LNA, Mixer and VCO in 90-nm CMOS Technology
- Designing an integrated HBT with improved and optimized structural parameters used in cascode configuration of an Opto-electronic mixer
- Designing a model of 12-bit Mid-rise quantizer with 100 MHz sampling frequency, linear and nonlinear input S/H circuits in MATLAB
- Designing a multi-stage feedback TIA with Butterworth response in 90 nm-CMOS Technology

## PUBLICATIONS

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1. Epileptic seizure detection with patient-specific feature and channel selection for low-power applications  
Journal Paper: (IEEE TBCAS, Jul 2022)
2. Programmable Seizure Detector Using a 32-bit RISC Processor for Implantable Medical Devices  
Conferecel Paper: (IEEE LASCAS, Feb 2023)
3. Digital One-Shot Charge-balancing Method for Implantable Current-Mode Electrical Stimulation  
Conference Paper: (IEEE PRIME 2023, June 2023)
4. A CMOS RF energy harvester with high PCE over a wide range of input power  
Journal Paper: (Springer Analog Integrated Circuits and Signal Processing, Aug 2022)
5. Hardware-Friendly Random Forest Classification of iEEG Signals for Implantable Seizure Detection  
Conference Paper: (IEEE IECBES, Dec 2022)
6. Computation Complexity Reduction Technique for Accurate Seizure Detection Implants  
Conference Paper: (IEEE ICECS, Dec 2022)
7. Modeling and Analysis of a Wirelessly Powered Closed-Loop Implant for Epilepsy  
Conference Paper: (IEEE BioCAS, Nov 2022)
8. System-level modeling of a safe autonomous closed-loop epileptic seizure control implant  
Conference Paper: (IEEE BioSMART, Dec 2021)
9. Two-stage hardware-friendly epileptic seizure detection method with a dynamic feature selection  
Conference Paper: (IEEE EMBC, Nov 2021)
10. Conversion Gain Improvement of InP/InGaAs HBT Opto-Electronic Mixer Using Nearly Gaussian Doping Profile and Linear Grading of Composition in Base Region  
Journal Paper: (SAP Electrical and Electronic Engineering, 2016)