# Improving Power-Delay Performance of Ultra-Low-Power Subthreshold SCL Circuits

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***Abstract*—This brief presents a technique for improving the power-delay performance of subthreshold source-coupled logic (SCL) circuits. Based on the proposed approach, a source-follower buffer stage is used at the output of each SCL stage. Analytical results confirmed by measurements in 0.18-$\mu$m CMOS technology show an improvement by a factor of as high as 2.4 in power-delay product (PDP). It is also shown that the proposed technique can be used for implementing subthreshold ultra-low power SCL logic gates with a better power and area efficiency, compared to the traditional SCL subthreshold circuits. An optimized approach is proposed to improve the power efficiency of ultra-low power STSCL library cells.**

***Index Terms*—Source-coupled logic (SCL), subthreshold SCL (STSCL), ultralow-power circuits, weak inversion SCL (WiSCL).**

## I. Introduction

THE demand for ultra-low power and low voltage integrated circuits is making the design of CMOS integrated circuits in the subthreshold/weak inversion region [1] increasingly attractive. Applications such as sensor networks, wearable battery-powered systems, and implantable circuits for biological applications require the implementation of circuits with very low power consumption as well as low sensitivity to the supply voltage and its variations [2]–[5].

It has already been shown that, by properly biasing CMOS logic circuits in the subthreshold regime, it is possible to achieve very low power consumption [6], [7]. However, the supply dependence of the maximum speed of operation $f_{\rm op}$ and power consumption $P_{\rm diss}$ of the CMOS logic circuits have made them very sensitive to supply voltage variations. Therefore, a precise supply voltage with low variation is required [8].

Due to their fully differential topology, source-coupled logic (SCL) circuits exhibit very low sensitivity to the supply voltage and its variations [9]. In addition, because of the differential topology of the SCL circuits, they inject less noise to the supply and substrate and hence exhibit less crosstalk. These properties make this topology very attractive for high-speed mixed-signal applications [10]. Some recent developments have shown that it is also possible to use this topology for ultralow-power applications [11]. Subthreshold SCL (STSCL) circuits can operate with a very low bias current per cell (down to a few picoamperes) and still provide low sensitivity to the supply voltage. The output drive capability of the STSCL gates, however, remains fairly limited, which also restricts their power-delay product (PDP) performance, as will be shown in the following. The restriction can easily be overcome using simple source-follower buffer (SFB) stages, without increasing the overall power dissipation.

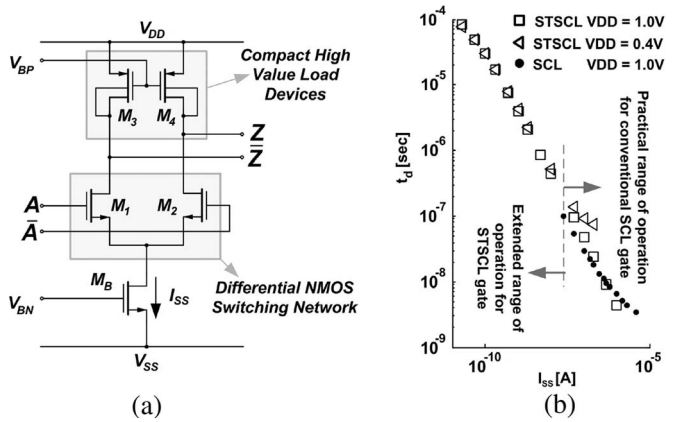


Fig. 1. (a) STSCL buffer (inverter) circuit schematic [11]. M1–M4 are biased in the subthreshold regime. (b) Measured gate delay of the STSCL gate ($V_{\rm DB} = 0$ V) for $V_{DD} = 0.4$ V and 1.0 V, in comparison to the gate delay of the conventional SCL topology, which uses PMOS load devices biased in the triode region ($V_{\rm SB} = 0$ V).

In this brief, after a brief overview of the STSCL circuits, some new techniques for improving their performance in terms of PDP will be described. Based on the proposed technique and using a structured approach, the possibility of implementing a low-power and low-area standard cell library will be investigated.

## II. STSCL Circuit Topology

### A. Overview

Fig. 1(a) shows the topology of an STSCL circuit [11]. In this topology, all transistors are biased in the subthreshold regime (except $M_B$, which can be in strong inversion). To have a successful switching event, the voltage swing at the input and output of this circuit should be more than $V_{\rm SW} > 4 \cdot n_n U_T$ [11], where $n_n$ is the subthreshold slope factor of the n-channel metal–oxide–semiconductor (NMOS) differential pair devices and $U_T = kT/q$ (where $k$ is Boltzmann's constant, $T$ is the junction temperature in kelvins, and $q$ denotes elementary charge). Satisfying this constraint, the circuit shown in Fig. 1(a)

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will also show enough gain for successful logic operation [11]. To provide the required voltage swing at very low tail bias current values $I_{SS}$, very high valued load resistances are required ($R_L = V_{\rm SW}/I_{SS}$). This load resistance should occupy a small area and exhibit good controllability to be able to adjust its resistivity with respect to the tail bias current. In Fig. 1(a), p-channel metal–oxide–semiconductor (PMOS) transistors with shorted drain–bulk terminals have been used to implement the proposed high-resistance load devices. For very low bias current values, the PMOS load transistors operate in the subthreshold regime. When the source–drain voltage of these devices is low ($V_{SD} < 100$ mV), they will be in the linear region. For higher source–drain voltages, the PMOS load devices will enter the saturation region. In this case, the threshold voltage depends on $V_{SD}$. Hence, the device exhibits lower output resistance, compared to the case when the source terminal is shorted to the bulk of the device. In this way, the linearity region of the load devices will increase. Using small-sized PMOS devices, this structure can be used to implement very high value resistances with a relatively high voltage swing at the output. A replica bias circuit can be used to control the resistance of the load devices and hence adjust the output voltage swing with respect to the tail bias current [11]. The replica bias circuit also reduces the sensitivity of the circuit to temperature and process corner variations by adjusting the load resistance accordingly.

Fig. 1(b) shows the measured delay of an STSCL gate for different tail bias currents and different supply voltages. As shown in the figure, the tail bias current of the gate can be reduced well below 1 nA, whereas the conventional SCL topology cannot be utilized for tail bias currents below 20 nA. Meanwhile, it can be seen that the supply voltage can be reduced from 1.0 to 400 mV, without degrading the gate delay or reducing the output swing.

### B. PDP Performance

In contrast to the CMOS gates, in which there is no static power consumption (neglecting the leakage current), each STSCL gate draws a constant bias current of $I_{SS}$ from the supply [Fig. 1(a)]. Therefore, the power consumption of each STSCL gate can be calculated by

$$P = V_{DD} I_{SS}. \tag{1}$$

Meanwhile, the time constant at the output node of each STSCL gate, i.e.,

$$\tau = R_L \cdot C_L \approx (V_{\rm SW}/I_{SS}) \cdot C_L \tag{2}$$

is the main speed-limiting factor in this topology. ($C_L$ is the total output loading capacitance.) Based on (2), one can choose the proper $I_{SS}$ value to be able to operate at the desired operating frequency. Regarding (1), it can be concluded that the power consumption is constant and independent of the operation frequency. Therefore, it is necessary to always operate the STSCL circuits at their maximum activity rates to achieve the maximum efficiency. Based on (1) and (2), the PDP of each gate can approximately be calculated using

$$\text{PDP} \approx \ln 2 \times V_{DD} V_{\rm SW} C_L \tag{3}$$

which is directly proportional to the supply voltage, the voltage swing at the output of the gate, and the total load capacitance. Load capacitance $C_L$ is partially due to the parasitic capacitances of the SCL gate itself, whereas the dominant part usually comes from the interconnection parasitic capacitances in a complex digital system. In the next section, a technique for reducing the PDP of SCL circuits biased in the subthreshold region will be presented.

## III. Performance Improvement Using SFBs

For implementing a complex digital system using STSCL topology, it is necessary to build a library of different logic functions (or cells) with different driving strengths, which can then be used in a top–down synthesis flow, followed by automated placement and routing [9]. To design different types of logic functions, it is possible to use a binary-decision-diagram configuration in the differential NMOS switching network [Fig. 1(a)]. Meanwhile, to construct logic cells with different driving strengths, the tail bias current of each cell and the size of the PMOS load devices must be scaled. This scaling needs to be proportional to the required driving strength, which will scale the power consumption and also the cell area proportional to the driving strength. Therefore, to achieve a larger driving strength, each cell will have to occupy more area that will reduce the power efficiency of the gate because of increased parasitic capacitances.

### A. Proposed Topology

To avoid scaling the area of each cell proportional to the driving strength, we are proposing the configuration shown in Fig. 2(a) [12]. Here, each STSCL gate uses a pair of simple SBFs, one at each of its two complementary outputs. The added output buffer will isolate the load capacitance from the core SCL gate. Since the output impedance of the SFB $(1/g_{m6,s})$ is very low, compared to the output impedance of the SCL gate $R_L$, an improvement in the total gate speed is expected. On the other hand, since the load capacitance is driven by the output buffer, it is sufficient to have different output buffer stages to achieve different driving strengths. This means that the core SCL gate does not need to be scaled and that the area and power consumption of this part will remain unchanged for different driving strengths. To scale the driving capability of the output buffer, it is necessary to scale the tail bias current of the output stage only [i.e., scaling $I_B$ in Fig. 2(a)]. Since the common-drain transistors are biased in the subthreshold, their sizes can be kept unchanged for different driving strengths, as will be explained in Section III-C. Therefore, the topology shown in Fig. 2(a) offers a more power- and area-efficient implementation of the STSCL gates for creating digital library cells.

### B. Performance Analysis

The output load capacitance seen by any gate in a complex design is generally due to the interconnections and can be as high as hundreds of femtofarads in the considered technology. In this case, using a simple buffer stage can considerably relax the power-delay tradeoff in the SCL circuits. As shown

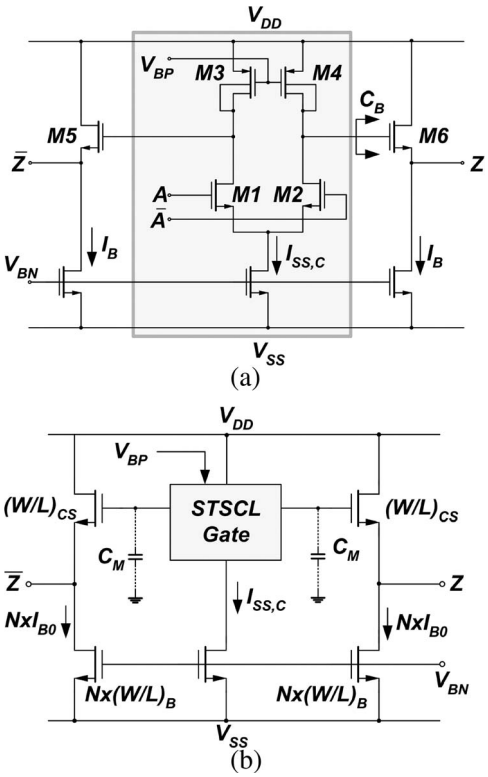


Fig. 2. (a) Generic STSCL gate uses an SFB at the output (STSCL-SFB) to improve the PDP of the gate. (b) Design of standard library cells with different driving strengths based on the STSCL-SFB topology. $C_M$ stands for the total parasitic capacitance seen by each output node of the STSCL core.

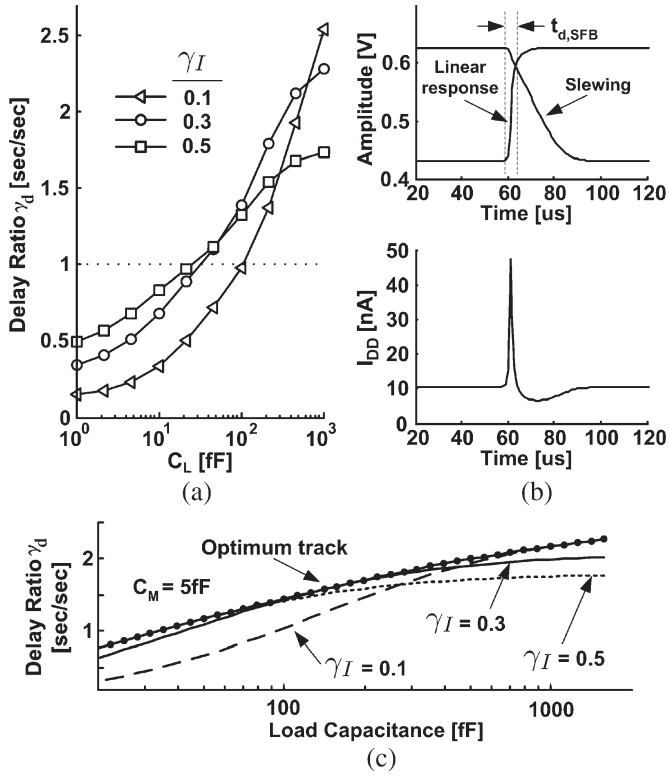


Fig. 3. (a) Total delay improvement using the SFB at the output of the STSCL circuit in equal total power consumption based on transistor-level simulations. Data points with a delay ratio of larger than unity represent delay improvement (reduction). (b) Transient simulation results: (Top) Output waveforms and (bottom) supply current for an STSCL-SFB topology ($I_{SS} = 10$ nA). (c) Delay reduction $\gamma_d$ for different $\gamma_I$ values, compared to the $\gamma_{d,\max}$ calculated based on (8).

in Fig. 2(a), in this case, the SCL core drives the parasitic capacitances due to M1–M3 and M2–M4, and the input capacitance of the buffer stage. Note that this capacitance is composed of the gate–drain overlap capacitance and the gate–source contribution of M5–M6; hence, it can be very low. Operating at very low bias currents, the size of the devices used in the SFB can be kept small, so the output stage would have a very small loading effect on the STSCL core. Therefore, the dominant time constant at the circuit topology shown in Fig. 2(a) is expected to be at the output node, i.e.,

$$\tau_{\rm SFB} \approx C_L/g_{m6,s} \tag{4}$$

which is valid for small signal variations. In a real case, when the output swing is on the order of several hundreds of millivolts, however, this equation will no longer be valid. Indeed, at each rising edge, more current will flow into the proposed common-source device. In this case, the time constant of the node would even be smaller than the value predicted in (4). On the other hand, for falling transitions, the common-source transistor will be turned off, and the only path for discharging the output node will be $I_B$ [Fig. 3(b)]. Therefore, the output will slow down with a slope of $I_B/C_L$. This means that the improvement predicted by (4) can be expected only at the rising edges. Neglecting the delay of the STSCL core and assuming typical conditions (e.g., $V_{\rm SW} = 200$ mV and room temperature), it can be shown that the slew mode will increase the total delay to

$$t_{d,\rm SFB} \approx 1.6\tau_{\rm SFB}. \tag{5}$$

Here, it is assumed that M5 and M6 will very quickly turn off at the falling edges. This assumption can be acceptable when the time constant at the output of the STSCL gate is much less than the time constant at the output of the SFB stage.

Including the delay of the STSCL core to the total delay and assuming that $t_{d,\rm STSCL-SFB} \approx t_{d,\rm STSCL} + t_{d,\rm SFB}$, it can be shown that the delay improvement (reduction) ratio is

$$\gamma_d = \frac{t_{d,\rm STSCL}}{t_{d,\rm STSCL-SFB}} \approx \frac{\ln 2 \cdot C_L R_{L1}}{\ln 2 \cdot C_M R_{L2} + 1.6 C_L/g_{m6,s}} \tag{6}$$

where $C_M$ is the total parasitic capacitance at the output of the SCL stage, as shown in Fig. 2(b); $R_{L1} = V_{\rm SW}/(I_{SS,C} + 2I_B)$ is the load resistance of a simple STSCL gate; and $R_{L2} = V_{\rm SW}/(I_{SS,C})$ is the load resistance of the SCL core in Fig. 2(a). Replacing $g_{m6,s} = I_B/(n_n U_T)$, then

$$\gamma_d = \frac{\gamma_I}{1+\gamma_I} \cdot \frac{1}{\gamma_C + \frac{3.2 n_n U_T}{\ln 2 \cdot V_{\rm SW}} \gamma_I} \tag{7}$$

in which $\gamma_C = C_M/C_L$ and $\gamma_I = I_{SS,C}/(2I_B)$ [see Fig. 2(a)]. Here, it is assumed that the total bias current in both topologies are equal, i.e., $I_{SS} = I_{SS,C} + 2I_B$. This equation also implies that, by properly choosing $\gamma_I$ with respect to $\gamma_C$, it is possible to achieve a balanced design for different load capacitance values. This property is especially useful for the design of digital library cell elements, as will be explained in Section III-C.

It is also interesting to notice that, for very large load capacitance values, the delay improvement factor can be as high as $\gamma_d \approx 2.25/(1+\gamma_I) \approx 2.25$. Therefore, using SFBs, it is possible to reduce the delay (or PDP) of the STSCL circuits by a factor of approximately 2.25 with the same amount of power.

Fig. 3(a) shows the total delay improvement using the SFB stage at the output of the STSCL gates, compared to the simple STSCL gate, under the assumption that both circuit solutions are dissipating the same amount of power. The comparison is shown for different load capacitances and different ratios of the bias currents between the core and buffers. For low load capacitances (less than 20 fF), the simple STSCL gate without the SFB stage shows smaller total delay. However, as the load capacitance increases, the topology shown in Fig. 2(a) exhibits less delay, compared to the simple STSCL gate. In complex digital systems, where the output load is dominated by interconnect capacitance, an improvement in the PDP by a factor of more than 2 can be observed. Fig. 3(b) shows the transient response of the circuit. While the proposed STSCL-SFB gate exhibits a considerable improvement in rising edges, the falling edge does not improve very much. This is mainly due to the fact that the source-follower stage very quickly turns off during the falling output transition. Consequently, the charge on the output capacitance will be discharging by the constant bias current of $I_B$. The estimated value of $t_{d,\mathrm{SFB}}$ in (5) is based on this behavior. This figure also shows that the supply current is no longer constant, whereas, in the simple STSCL, it is almost constant.

To keep the noise margin of the STSCL-SFB gates as high as that of the STSCL gates (which is about $NM = 130$ mV for $V_{\mathrm{SW}} = 200$ mV), it is necessary to increase the voltage swing $V_{\mathrm{SW}}$ of the core SCL gate in the STSCL-SFB topology. This is mainly for compensating the gain of the source-follower stage, which is less than unity. Since the gain of the source-follower stage is very close to unity, an increase in the range of about 10%–15% in the voltage swing is sufficient to compensate this effect. The other main issue is the mismatch between the gates and the replica bias circuit and the mismatch between the SFBs inside a cell. As discussed in [11], it is possible to control the mismatch effect among the gates and the replica bias circuit by proper sizing of devices and selection of a high-enough $V_{\mathrm{SW}}$. The size of the source-follower transistors needs to be large enough to make sure that the offset between them does not affect the proper logic operation of the gate. This can put a lower limit on the size of the devices and, hence, $C_B$ in Fig. 2(a). Minimizing $C_B$ helps to maximize the PDP improvement, as will be discussed later.

### C. Optimized Design

In a complex digital system, the parasitic capacitance due to the interconnections will be the dominant part of $C_L$, resulting in relatively high values, such as $C_L > 30$ fF. Therefore, the SFB stages can improve the PDP of the complex STSCL digital circuits by a factor of 2 or higher.

The choice of the output buffer topology also reflects a careful balance between circuit complexity and performance. Using a more complex output stage, more improvement can be achieved. For example, a push–pull output stage would reduce the sensitivity to the load capacitance even further. However, in this case, the circuit complexity would rapidly increase, and controlling the power consumption and voltage swing would be very difficult. Using a push–pull output stage can also increase the sensitivity to the supply voltage variations.

The simple SFB stage output buffer technique can simplify the design of library cells. Based on this approach, it is sufficient to design a single logic cell and provide the required driving strength by using different SFB stages, as shown in Fig. 2(b). Shown as an example in Fig. 2(b), a single STSCL Boolean gate, together with different SFB stages with different bias or driving capabilities, can provide the required specifications. Here, $I_{SS,C}$ can be kept constant for all the STSCL gates, whereas $N$ can be changed to achieve different driving capabilities. Since all the devices are biased in the subthreshold regime, it is sufficient to change the bias current in the SFB stage without changing the size of the source-follower devices (i.e., $W_{CS}$ and $L_{CS}$ can be kept constant) to implement different driving strengths. Therefore, the only required modification is changing the size of the tail bias transistors at the output buffer stage.

It is possible to use (7) to determine the proper bias current for the SFB stage with respect to load capacitance $C_L$. By solving $\partial\gamma_d/\partial\gamma_I = 0$, it can be shown that the optimum value for $\gamma_I$ for a given $\gamma_C$ is

$$\gamma_{I,\mathrm{opt}} = \sqrt{\ln 2 \cdot V_{\mathrm{SW}} \cdot \gamma_C/(3.2U_T)} \tag{8}$$

which indicates that, for larger load capacitances (i.e., a smaller $\gamma_C$), a smaller portion of the total current budget should be dissipated in the STSCL core (i.e., smaller $\gamma_I$ should be selected). Regarding (8), it can also be concluded that, to increase the driving capability of each gate by a factor of $S$, it is sufficient to keep the bias current of the core constant and increase the bias current of the SFB stage by a factor of $\sqrt{S}$, which is always smaller than $S$ for $S > 1$.

Defining $\alpha = 3.2U_T/(\ln 2 V_{\mathrm{SW}})$ and using (8), the maximum improvement that can be achieved is

$$\gamma_{d,\max} = 1/\left(\sqrt{\gamma_C} + \sqrt{\alpha}\right)^2. \tag{9}$$

Therefore, to have $\gamma_{d,\max} > 1$ (or a better performance for the STSCL-SFB configuration, compared to STSCL), then

$$C_L > C_M/\left(1 - \sqrt{\alpha}\right)^2. \tag{10}$$

Using the optimum value for $\gamma_I$ and using nominal values in the proposed design, it can be shown that the STSCL gates that are using the SFB show better performance for $C_L > 11C_M$. Using minimum-sized devices and a compact layout, it is possible to reduce the size of $C_B$ to only a few femtofarads. Therefore, using a careful design strategy, it is possible to have superior performance for load capacitances of as low as 30 fF using the STSCL-SFB topology. For $C_L < 11C_M \approx 30$ fF, a simple STSCL topology will exhibit a comparable or better performance. However, it is not possible to have a combine STSCL and STSCL-SFB gates in a design mainly because of the voltage drop on the source-follower stage. Since this limit (i.e., $C_L < 11C_M \approx 30$ fF) is very low, it is expected that, even in not very complex designs, the proposed topology provides considerable advantages from the power–speed points of view. Fig. 3(c) shows the delay reduction factor for different load

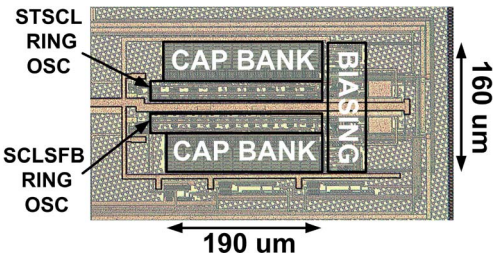


Fig. 4. Photomicrograph of the test chip implemented in 0.18-$\mu$m technology.

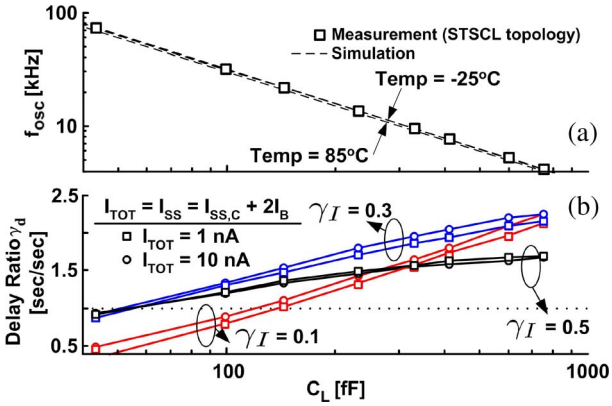


Fig. 5. (a) Measured oscillation frequency of the STSCL ring oscillator, in comparison to the simulation results at different temperatures. (b) Total delay improvement for a total bias current per stage of 1 and 10 nA. Each ring oscillator is composed of eight delay cells. Data points with a delay ratio of larger than unity represent delay improvement (reduction).

capacitance values and three different $\gamma_I$ values. To maximize the improvement, it is necessary to use different $\gamma_I$ values with respect to the load capacitance, as shown in (8). This figure also illustrates the maximum achievable improvement in different load capacitance values and corresponding $\gamma_{I,\mathrm{opt}}$.

## IV. Experimental Result

A test chip has been fabricated in a conventional digital 0.18-$\mu$m CMOS technology to verify the performance of the STSCL topology with and without SFBs in each stage. For this purpose, two ring oscillators have been implemented: one using simple STSCL multiplexer (MUX) gates configured as buffer stages and the other one using the same configuration, where each MUX gate is followed by an SFB. Each ring oscillator has a capacitor bank to be able to change the loading capacitance in all the intermediate nodes of the oscillator. In this way, it is possible to study the delay of cells for different capacitance load values. The chip photomicrograph is shown in Fig. 4.

The measured PDP for the ring oscillators depends on the load capacitance, and the results agree with the simulation results within $\pm 20\%$ accuracy. For a simple STSCL-based topology, the measured PDP is approximately 0.125 $\mathrm{J \cdot F^{-1}}$ or 0.7 fJ for $C_L = 6$ fF. The measured oscillation frequency is shown in Fig. 5(a). This figure also shows the simulated oscillation frequency for different temperatures. Due to the internal replica bias circuit, variations on the oscillation frequency due to the temperature variations can be kept very low.

Fig. 5(b) shows the measured delay ratio $\gamma_d$ for two ring oscillators for the total bias currents of 1 and 10 nA per stage (i.e., the total current consumptions of the ring oscillators are 8 and 80 nA, respectively). Both oscillators are connected to the same supply voltage and consume the same amount of power. In these measurements, $V_{DD} = 0.7$ V, $V_{\mathrm{SW}} = 0.2$ V, and the total power consumption (excluding the replica bias circuit) is 5.6 and 56 nW for $I_{SS} = 1$ nA and 10 nA, respectively. This figure shows the results for three different $\gamma_I$ values ($\gamma_I = 0.1, 0.3, 0.5$). It can be seen that the measured improvement in delay agrees well with the analysis result derived in Section III-B. The higher crossover point (where $\gamma_d = 1$) in Fig. 5(b), compared to the analysis, means that the $C_M$ value in practice is higher than the expected value. For supply voltages that are lower than 0.7 V, the gain of the amplifier used in the replica bias circuit starts to reduce; hence, there is less precise control on the output voltage swing in this case.

## V. Conclusion

It is shown that the PDP of the SCL circuits can be improved by utilizing an output SFB stage. A test chip has been implemented in 0.18-$\mu$m CMOS technology to verify the proposed concept. Based on the simulation and measurement results, improvement on the PDP of the circuit using output buffers can be as high as approximately a factor of 2.4. A structural approach for implementing digital library cells using STSCL topology has also been proposed.

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