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An area and power optimization technique for CMOS bandgap voltage references

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Abstract This article explores the main tradeoffs in design of power and area efficient bandgap voltage reference (BGR) circuits. A structural design methodology for optimizing the silicon area and power dissipation of CMOS BGRs will be introduced. For this purpose, basic equations of the bandgap circuit have been adapted such that can simply be applied in the optimization process. To improve the reliability of the designed circuit, the effect of amplifier offset has been also included in the optimization process. It is also shown that the minimum achievable power consumption and area are highly depending on the fabrication process parameters especially sheet resistivity of the available resistors in the technology and also the area of bipolar transistors. The proposed technique does not depend on a special process and can be applied for designing bandgap reference circuits with different topologies.

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1 Introduction

Design of low-power and small-area analog integrated circuits becomes more and more important especially in design of modern complex integrated circuits where several channels or systems are implemented on a single chip. However, due to the complex relationship between design parameters and design goals, developing an efficient methodology to simultaneously optimize the silicon area, power consumption, and circuit performance is not generally feasible. In this article, an effective methodology for optimizing the area and power dissipation of CMOS bandgap voltage reference (BGR) circuits will be described. Based on this methodology, a BGR circuit has been designed for a multi-channel voice-band CODEC chip. In this chip, each channel benefits a completely separate biasing circuit to reduce the cross-talk among the channels. Therefore, the power consumption and area of BGR and biasing circuits should be as small as possible.

To have an effective optimization methodology, basic equations of the bandgap core have been modified such that simply could be applied in optimization process. In addition to the area and power consumption, the effect of amplifier offset has also been included in the optimization process to result in a better circuit performance. As will be shown later, the minimum achievable area and power dissipation depends highly on the specifications of the available resistors in the fabrication process. Resistors with high sheet resistivity will result in less area and also less power dissipation. Meanwhile, the variation on the

absolute value of the output reference voltage depends on the process and temperature variations of the resistors and bipolar transistors. The proposed methodology does not depend on the process or supply voltage and can be applied to any CMOS BGR circuit topology.

Several techniques for implementing integrated reference voltage circuits could be found in the literature. Bandgap voltage reference circuits have been widely used due to their accuracy, reliability and compatibility with CMOS technologies [1–8]. The circuit topology introduced in [6] shows a high power supply rejection ration (PSRR) voltage reference circuit. This circuit topology (shown in Fig. 1) has been selected for the proposed application due to its simplicity, stability, and high PSRR [6]. In this topology, bias current, area ratio of the BJT transistors, and their bias current ratio are the main design parameters which can be used in optimization process.

Based on the proposed approach, a bandgap reference circuit has been implemented in a standard 0.5 μm CMOS technology. Simulation results show that the temperature coefficient of the proposed circuit is 15.6 ppm/°C with 9.4 mV standard deviation without any trimming. Furthermore, the whole circuit including the amplifier, draws only 160 μA from supply voltage and occupies 0.085 mm^2 silicon area.

In Sect. 2, the proposed design methodology will be presented. Circuit implementation and simulation results are discussed in Sect. 3 and conclusions will be explained in Sect. 4.

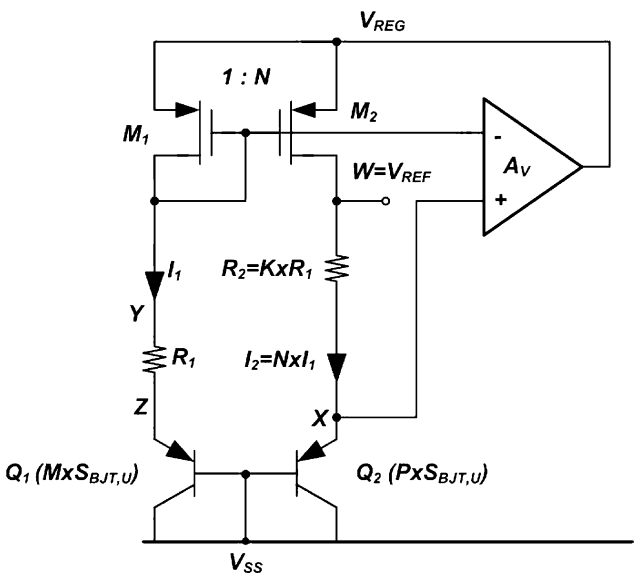

Fig. 1 The core of the bandgap reference circuit (BGR) [6]

2 Bandgap core design and optimization

2.1 BGR core operation

The core of a sample BGR circuit is shown in Fig. 1 [6]. In this topology, the amplifier forces the voltages at the nodes X and Y to be equal, and hence the output voltage will be:

$$V_{\mathrm{REF}} = V_{\mathrm{EB2}} + N \cdot K \cdot \ln\left(N \cdot \frac{M}{P}\right)\left(k \cdot \frac{T}{q}\right) + N \cdot K \cdot V_{\mathrm{OS}} \tag{1}$$

in which k is Boltzmann's constant, T is the temperature (in degree kelvin), and V_{OS} indicates the total equivalent input offset voltage of the amplifier A_{V}. Here, M and P are two positive integer numbers to explicitly indicate that Q_1 and Q_2 can be constructed only by putting unit BJT devices (with the area of $S_{\mathrm{BJT,U}}$) in parallel. These numbers will be also used later in the optimization process to distinguish between the different topologies. Meanwhile, N and K are indicating the ratio of the emitter bias current of the two BJT transistors and the ratio of the resistors, respectively. These two numbers should be rational numbers to be implementable in the proposed fabrication technology with a very good matching property.

By proper choosing the design parameters, the negative temperature dependence of the emitter-base junction (V_{EB2}) will be cancelled out by the second expression in (1) in a specified temperature of T_0. Based on (1), there are four design parameters in this topology: N, K, P, and M. In order to have a temperature independent output voltage (V_{REF}) in a desired temperature of T_0, the following equation should be satisfied by differentiating (1) versus T (neglecting the temperature variation of V_{OS}):

$$\left.\frac{\partial V_{\mathrm{EB2}}(T)}{\partial T}\right|_{T=T_0} = \delta_0 = -N \cdot K \cdot \ln\left(M \cdot \frac{N}{P}\right) \tag{2}$$

in which δ_0 is the temperature coefficient of the emitter-base voltage in T_0 (T_0 is the temperature in which $\partial V_{\mathrm{REF}}(T)/\partial T|_{T=T_0} = 0$). Meanwhile, according to (1), the amplifier offset appears at the output by the gain of

$$K_{\mathrm{OS}} = N \cdot K \tag{3}$$

Due to the random nature of the amplifier offset, this voltage (V_{OS}) can change the V_{REF} value unpredictably. Therefore, V_{OS} and K_{OS} both should be minimized as much as possible.

2.2 Bandgap core equations

To complete the design of BGR circuit, the value of δ_0 should be known. There are several articles describing the temperature characteristics of base-emitter junction [8–10].

Here, we need an expression including both temperature and bias current dependence of V_{EB} to use it in the optimization process. The basic equation of the base-emitter junction of a bipolar transistor is [8]:

$$V_{EB} = \left(k \cdot \frac{T}{q}\right) \cdot \ln\left(\frac{I_C}{I_S}\right) + r_b \cdot \frac{I_E}{(1+\beta)} \tag{4a}$$

$$V_{EB} = \left(k \cdot \frac{T}{q}\right) \cdot \ln\left(\left(\frac{I_E}{I_S}\right) \cdot \left(\frac{\beta}{(1+\beta)}\right)\right) + r_b \cdot \frac{I_E}{(1+\beta)} \tag{4b}$$

in which, β is the current gain of bipolar (BJT) transistor, r_b is the base resistance, and I_S is the reverse junction saturation current. Using a simplified expression for I_S, one can conclude that [8, 11]:

$$V_{EB}(T, I_E) \approx A + [B + C \cdot \log(I_E)] \cdot T + D \cdot T^2 \tag{5}$$

in which A, B, C, and D are four constant values depending on the bipolar device parameters. Here, I_E (emitter current) has been used instead of I_C (collector current) to have a better measure of I_1 and I_2 in Fig. 1. The temperature dependence of β has been also included in (5). SPICE simulations show that the amount of error in the estimated V_{EB} value in (5) compared to the accurate model is less than 1 mV for all corner cases [11]. In (5), I_E indicates the emitter current of a unit area BJT device which is available in the process (i.e., a bipolar device with the area $S_{BJT,U}$). Thus, in Fig. 1:

$$V_{EB1} = V_{EB}\left(T, \frac{I_1}{M}\right) \tag{6a}$$

$$V_{EB2} = V_{EB}\left(T, \frac{I_2}{P}\right) = V_{EB}\left(T, N \times \frac{I_1}{P}\right) \tag{6b}$$

The bias currents of I_1 and I_2 are both proportional to the absolute temperature (PTAT) value [4]. Indeed, since in Fig. 1 $V_X = V_Y$, then:

$$I_1 = \frac{I_2}{N} = \left[\left(\frac{1}{R_1}\right) \cdot \left(\frac{k}{q}\right) \cdot \ln\left(M \cdot \frac{N}{P}\right)\right] \times T = E \cdot T \tag{7}$$

It is also possible to include the temperature and voltage coefficients of R_1 (TC_{R1} and VC_{R1}) in (7). Now, Eqs. 5–7 could be used to satisfy the constraint of (2). Solving these equations renders the R_1 value [or more accurately $R_1(T_0)$] as the following:

$$R_1 = 10^G \tag{8}$$

where G can be expressed as:

$$G = \log\left[\left(\frac{N}{P}\right) \cdot \left(\frac{k}{q}\right) . \ln\left(N \cdot \frac{M}{P}\right)\right] + \frac{F}{C} + N \cdot K \cdot \frac{\ln\left(N \cdot \frac{M}{P}\right)}{C} \tag{9}$$

in which

$$F = B + C \cdot \log(e) + 2D \cdot T_0 + C \cdot \log(T_0) \tag{10}$$

As can be seen, F is a function of process parameters and T_0. In addition, G is a function of F, and design parameters N, P, M, and K. An important conclusion of Eqs. 8–10 is that the most crucial parameter that can affect the value of T_0 in different process corners, is the variation in absolute value of R_1. Indeed, the other parameters (such as N, M, P, and K or other process parameters presented by A, B, C, and D) do not change over the process corners or their variation is negligible whereas R_1 may change significantly (as high as ±20%). It means that according to (8), T_0 is approximately proportional to $\log(R_1)$ [i.e., $T_0 \propto \log(R_1)$]. Therefore, a resistance with the smallest possible variations over the process and temperature should be selected for this purpose. In addition, the voltage coefficient of R_1 (and R_2) has a negligible effect on T_0 if R_1 and R_2 have been perfectly matched, since V_{REF} relies only on the ratio of resistors as $K = R_2/R_1$. Inclusion of TC_{R1} and VC_{R1} in (9) results in a more complex expression for G and thus more accurate results. To obtain this equation, the term which is proportional to the r_b, i.e.:

$$r_b \cdot \frac{I_E}{(1+\beta)} \tag{11}$$

has been eliminated in (5). This expression indicates the voltage drop on r_b which creates an error on V_{REF} is proportional to the both temperature and bias current. Based on the transistor specifications in the proposed technology, the base spreading resistance of the transistors is 237 Ω (with a temperature coefficient of about 20 mΩ/°C) and the nominal value of β is about 7 (see Table 1). Hence, the total error in (5) resulting from (11) would be only 2 mV (for $I_E = 50\mu A$). According to (1) and (4a, 4b) this error voltage causes an equal DC shift on V_{EB} which could be embodied in (5) by adjusting the value of A. However, it is not simply possible to include the temperature variation of (11) in (5). Considering the temperature coefficient of r_b, the temperature variation of (11) would be 0.125 μV/°C. Therefore, compared to the temperature coefficient of the

Table 1 Technology parameters

Parameter	Value
BJT device (vertical PNP)	
β	7.1
I_S	1.11×10^{-9} (A)
r_b	237.09 (Ω)
TC of r_b	20 (mΩ/°C)
Emitter area	100 (μm^2)
Base area	784 (μm^2)
Resistor	
R_{SH}	33 (Ω)

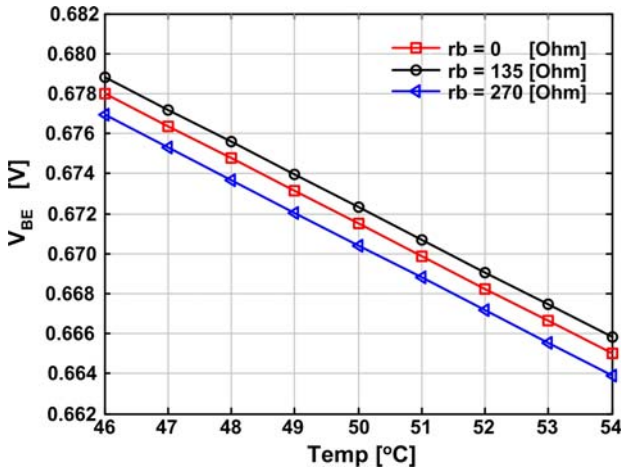

Fig. 2 V_{EB} versus temperature in $I_E = 50$ μA for $r_b = 0$, 135, and 270 Ω (temperature dependence of the r_b has been included). As can be seen the effect of r_b and its temperature dependence on V_{EB} is negligible. In this work: $T_0 = 50°C$, therefore, the simulation results around this temperature are shown

V_{EB} (which is more than 1.5 mV/°C), the effect of eliminating (11) in (5) would be negligible. Figure 2 shows the variation of V_{EB} for several different values of r_b (including its temperature coefficient). In this work $T_0 = 50°C$, therefore this plot shows the V_{EB} in a temperature range centered around this temperature. As can be seen, r_b does not affect very much the value of $\partial V_{EB}(T)/\partial T$, and hence it is sufficient to model its effect by a DC shift in V_{EB}.

2.3 Optimization process

Now, it is possible to use (8) in order to determine the circuit parameters and obtain an optimized area and power consumption for the bandgap circuit shown in Fig. 1 that have four circuit parameters namely N, M, P, and K.

Before starting the optimization process, it should be mentioned that the common centroid layout requirements limits the possible values for M and P (BJT area ratios) to some few integer pairs of numbers which leads to a good matching between Q_1 and Q_2. Based on this:

$$M + P \leq n^2 \tag{12}$$

where n is an integer number usually less than 5. Table 2 shows some possible numbers for M and P. Obviously, some of the values listed in Table 2 cannot be used practically and are shown only for comparison purpose.

The power dissipation of the bandgap core could be estimated simply by:

$$P_{diss} = V_{DD} \cdot I_1 \cdot (1 + N) \tag{13}$$

Meanwhile, the area of the resistors, BJT transistors, and current mirrors should be included in the area estimation.

Table 2 Possible area ratios for bjt transistors

Topology number	[P,M]
1	[1,8]
2	[4,4]
3	[4,5]
4	[5,4]
5	[4,12]
6	[12,13]
7	[1,24]
8	[5,20]
9	[9,16]
10	[8,17]
11	[4,21]
12	[13,12]
13	[20,5]
14	[16,9]
15	[12,4]
16	[17,8]
17	[21,4]

As will be shown later, the sizes of M_1 will be determined based on matching requirements of M_1:M_2 current mirror. Therefore, the area of the bandgap core (S_{tot}) can be determined approximately by:

$$S_{tot} \cong (M + P) \cdot S_{BJT \cdot U} + (1 + N) \cdot W_{M1} \cdot L_{M1} \cdot (1 + \theta) + (K + 1) \cdot \left(\frac{R_1}{R_{SH}}\right) \cdot W_R^2 \tag{14}$$

in which $S_{BJT,U}$ is the area of unit BJT device, W_{M1} and L_{M1} are the effective width and length of M_1 (in current mirror), R_{SH} is the sheet resistance of the resistors and W_R is the width of R_1 in bandgap core. Here, $\theta > 0$ is used to take into account the area headroom needed in drawing the layout of MOS transistors and hence have a better area approximation for the MOS devices. A good estimation for θ value can be extracted from the layout design rules.

The effect of amplifier offset (V_{OS}) at the output [as predicted in (1)] can be reduced by reducing the K_{OS}. Therefore, in addition to the silicon area and power consumption, the offset gain (K_{OS}) could be also embraced in the optimization process. As a result, the extracted circuit parameters render a reference voltage (V_{REF}) with low sensitivity to the amplifier offset.

In order to have a good assessment and determine the importance of each design parameter in optimization process, this Figure of Merit (FOM) can be introduced as:

$$FOM = \left[P_n^{\eta} \cdot S_n^{\rho} \cdot K_{OS,n}^{\lambda}\right]^{-1} \tag{15}$$

in which the index of n indicates that the parameters are normalized values, and η, ρ, and λ are used to reflect the importance of each design parameter. P, S, and K_{os} are indicating the power consumption, silicon area, and offset gain at the proposed circuit, respectively. Because of the importance of the Si area in our design compared to the power consumption, these coefficients selected: $\eta = \lambda = 1$ and $\rho = 2$.

Figure 3 shows the minimum achievable area of the proposed bandgap core for different values of power headroom (P_{diss}). To obtain this graph, area and power estimations besides Eq. 15 are estimated and optimized using a simple MATLAB script. In this figure, minimum achievable area is compared to one practical bandgap core whose area and power consumption were available and was fabricated at the same technology [12]. In equal power consumption, silicon area of the circuit reported in [12] is about 20% larger than the area of the circuit designed based on the proposed optimization methodology.

To optimize the circuit for maximum FOM defined in (15), the parameters K and N can be selected properly for different bipolar transistors area ratios [P,M] shown in Table 2. This operation is done by a simple MATLAB script. In this program for each value of [P, M, N, K], R_1 is calculated based on (8) (in a desired T_0). Then, I_1 is calculated from (7) and corresponding to that the values of K_{os}, P_{diss} and S are extracted from (3), (13) and (14), respectively. Then, corresponding to each [K_{os}, P_{diss}, S_{tot}], FOM is determined by (15). Finally, the values of [P, M, N, K] corresponding to the maximum FOM will be extracted. It is important to know that all the optimization process can be done in less than a minute using a simple MATLAB code.

Figure 4 shows the step-by-step flow diagram of the optimization methodology. Based on this flow graph, design methodology starts by extracting the necessary process parameters (such as R_{SH}, A, B, C, D, etc.) and then it will be followed based on design requirements (acceptable area, power and gain offset and importance of them respect to each other). Then the rest of steps indicated in this Section will be followed.

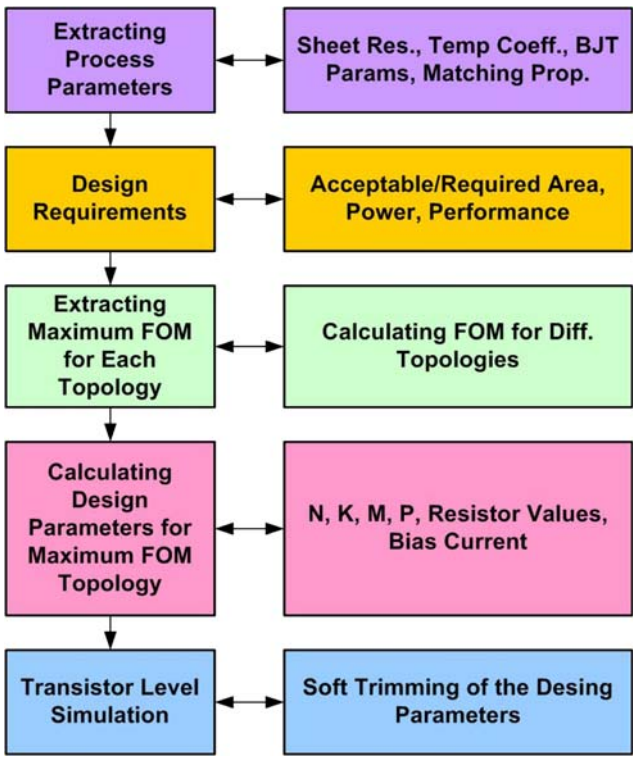

Fig. 4 Design flow diagram of the proposed optimization approach

Figure 5 shows the results of the optimization process for some of the topologies listed in Table 2. This has been

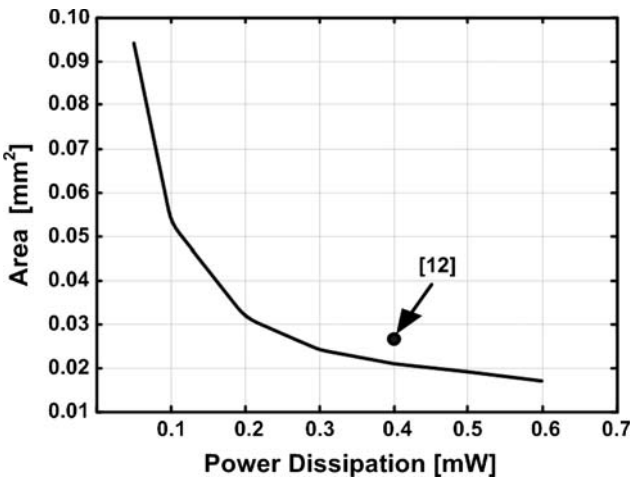

Fig. 3 Minimum possible area for bandgap core in a given power headroom of P_{diss}

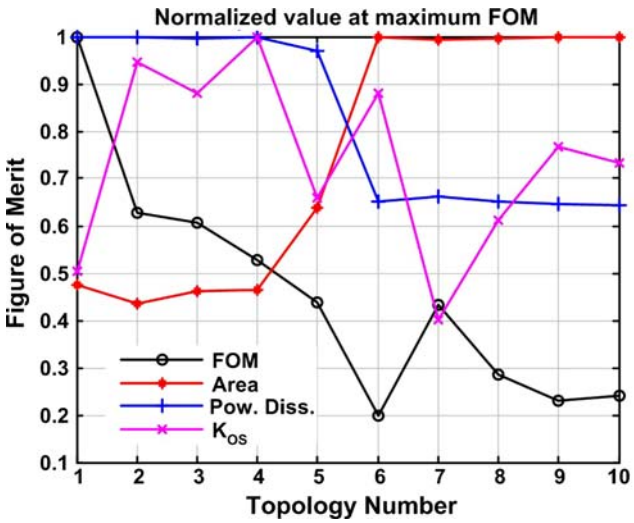

Fig. 5 Area, power, and offset gain (K_{OS}) of some topologies of the Table 2 when FOM of corresponding topology has been maximized

Table 3 Final design parameters after optimization ($T_0 = 50°C$)

Parameter	Value
M	8
P	1
N	4
K	1.67
R_1	8,350 (Ω)
L (length of pMOS current mirror devices)	4 (μm)
K_{OS}	6.68
Power dissipation	299 (μW)
Area	0.085 (mm^2)

done based on the model parameters of a 0.5 μm digital CMOS technology shown in Table 1. In this figure, for each topology the normalized area, powers, and K_{os} for maximum possible *FOM*, are also shown. Based on Fig. 5, the second topology of the Table 2 exhibits the minimum area, while the seventh topology has the smallest K_{os} value. Meanwhile, the first topology in this table shows the maximum value of FOM. For this reason, the first topology has been selected in this work. Here, the optimized values for N and K are 4 and 1.67, respectively. As shown in Table 3, the resulted value for R_1 is 8,350 Ω. R_1 and R_2 can be implemented as shown in Fig. 6(a). Since the sheet resistance of these resistors is 33 Ω/□ (see Table 1) the total area of these resistors will be dominant. To reduce the area, it is necessary to increase the power consumption.

The proposed design methodology is based on Eqs. 4a, 4b and 5 which are explaining basic operation of BJT transistors. Thus, it could be generalized for any other BGR topology. Using (4a, 4b) and (5), it is possible to calculate an equation similar to (8) for other topologies even with more complex structure and more design parameters such as the circuits shown in [13–15].

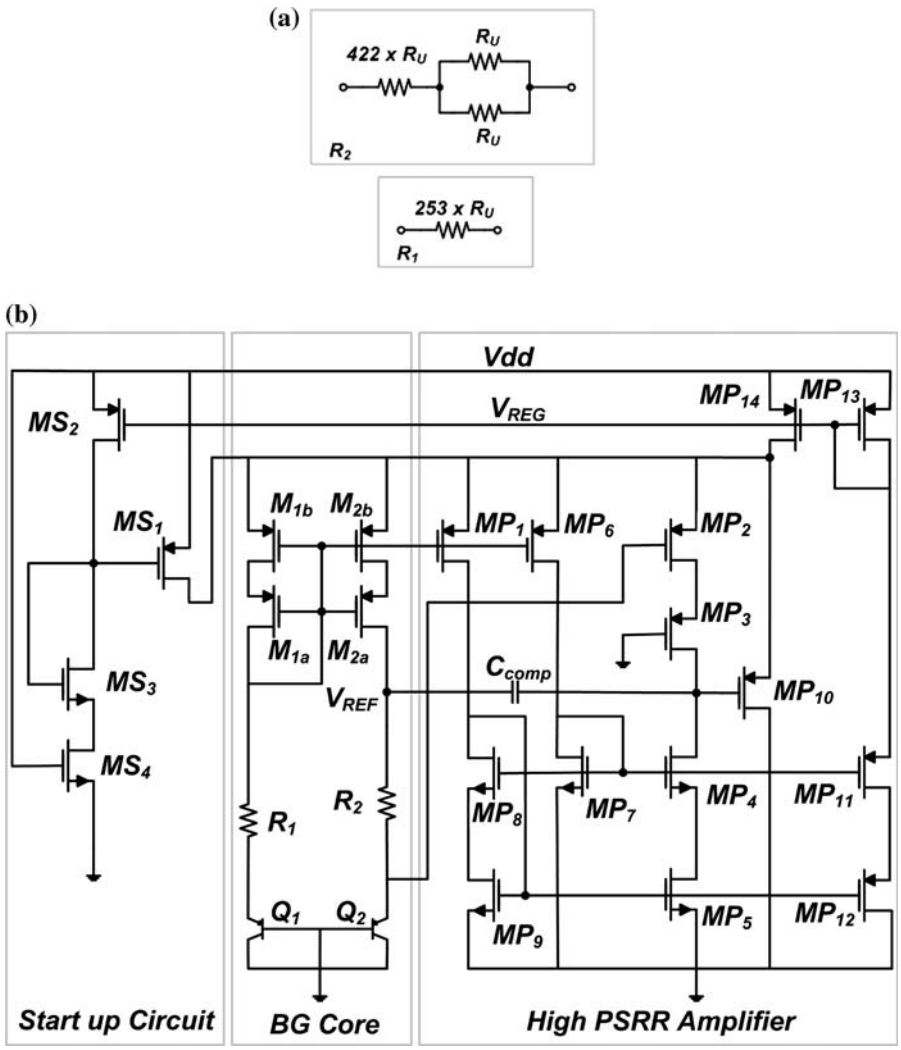

Fig. 6 **a** Implementing R_1 and R_2 to have the desired ratio. **b** Complete circuit of the proposed BGR

3 Bandgap voltage reference circuit

3.1 Device sizing

To minimize the amplifier offset or gain error in the current mirror, a careful sizing for MOS devices is required. Meanwhile, the gain and bandwidth of the amplifier A_V affect directly the PSR (power supply rejection) of the proposed BGR [13]. In this work, the topology of amplifier A_V is similar to the amplifier used in [6] [see Fig. 6(b)]. As shown in [6], because of using the bias current of the bandgap core as the bias current of A_V, power consumption of the A_V in Fig. 1 depends highly on the power (or bias current) of the bandgap core. Thus, minimizing the power dissipation in bandgap core leads to approximately the same result in A_V. Moreover, the offset of A_V depends on the area of this amplifier. Indeed, the size of transistors must be selected large enough to reduce its offset below an acceptable value.

Figure 7(a) shows the current mirror used in Fig. 1. In this figure, each transistor has been divided to two transistors such that $M1$b and $M2$b are in triode region, and $M1$a, and $M2$a are in saturation mode. This structure has larger effective channel length and also larger output impedance compared to a simple current mirror. In this current mirror, $M1$b and $M2$b are operating as two equal resistances in the source of $M1$a and $M2$a. Hence to have the desired current ratio:

$$\left[\frac{W_2/L_2}{W_1/L_1}\right]_{Ma,Mb} = N \tag{16}$$

Since both $M1$b and $M2$b have the same V_{GS} and V_{DS} ($V_{DS(M1b,M2b)} = V_{G(M1a,M2a)} + V_{GS(M1a,M2a)}$), the output impedance of current mirror would be more than a simple current mirror. Furthermore, since the voltage drop across the drain-source of $M1$b and $M2$b is small, the overdrive voltage of this structure is close to the overdrive voltage (V_{DSsat}) of a simple current mirror.

To determine the minimum acceptable transistor length in Fig. 7(a), temperature variations of V_{REF} in different current gain errors have been simulated [Fig. 7(b)]. As can be seen, the temperature variation of V_{REF} is approximately proportional to this error. Therefore, based on an acceptable error on V_{REF}, one can exploit the acceptable current gain error.

Figure 7(c) shows the result of Monte Carlo simulation indicating the maximum current gain error of the proposed current mirror [shown in Fig. 7(a)] versus transistor length. Therefore, Fig. 7(b) helps to determine the maximum acceptable gain error (for an acceptable temperature variation of V_{REF}), and Fig. 7(c) helps to choose a proper channel length for the transistors used in the current mirror. A similar approach could be followed in the amplifier design.

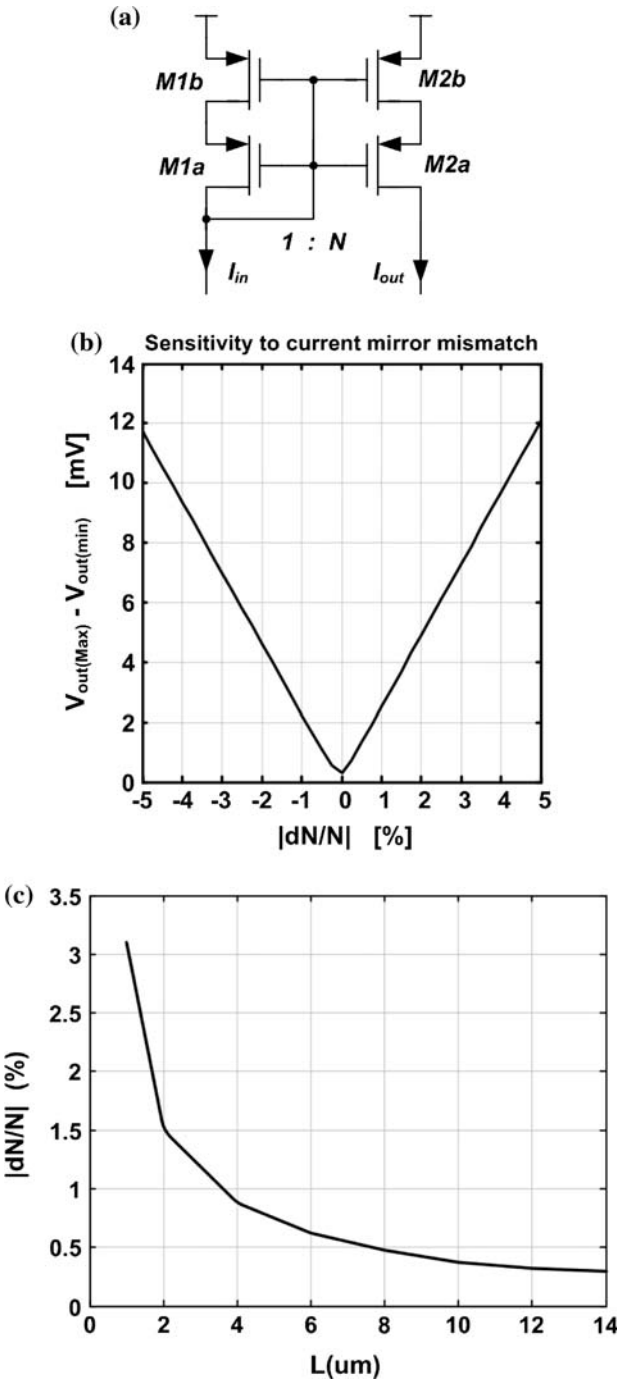

Fig. 7 **a** Current mirror, **b** the effect of current mirror gain error (dN/N) on V_{REF} extracted from Monte Carlo simulations, **c** absolute percentage of the gain error in current mirror (|dN/N|) versus transistor length (ideal value for N is 4 and $|dN/N| = |(N - N_{ideal})/N|$)

3.2 BGR circuit

In order to explore the practical aspect of the proposed optimization methodology, the proposed BGR has been designed in a conventional 0.5 μm CMOS technology.

Table 4 Simulation results

Parameter		Value
V_{DD}		5 ± 10 (%)
Temperature range		-20 to 140 (°C)
I_{DD} (total circuit)		160 (μA)
V_{REF} @ T_0	μ (V_{REF})	1.2411 (V)
In 100 Monte Carlo simulation	σ (V_{REF})	9.4 (mV)
ΔV_{REF} @ different corners	μ (ΔV_{REF})	3.1 (mV)
	σ (ΔV_{REF})	2.8 (mV)
	Max. (ΔV_{REF})	11.95 (mV)
PSR @ 2 MHz		59 (dB)
$TC = \left(V_{REF(Max)} - V_{REF(min)}\right)/\left(\Delta T \cdot V_{REF(nom.)}\right)$ @ TYPICAL corner [16]		15.6 (ppm/°C)

Table 3 shows the parameters for the optimized design. This table shows the proper value for transistor length that has been determined for less than 1% gain error in the current mirror, and also the expected values for power dissipation, area, and K_{os}.

Table 1 shows the technology parameters used in optimization process and Table 4 summarizes the simulation results of the complete BGR circuit achieved by 100 Monte-Carlo simulations in the temperature range of -20 to 140°C. In the proposed simulations, the variation of the parameters in different process corners has been also taken into account. The temperature coefficient of this circuit is 15.6 ppm/°C with a standard deviation of only 9.4 mV (with no trimming). As mentioned before, the main source of deviations in T_0 over process variations is due to the variation of absolute value of R_1 (see Fig. 1).

Figure 8 shows the result of a Monte Carlo simulation that can be helpful in determining the main factors affecting the temperature variations of V_{REF}. Figure 8(a) shows the error in K_{OS} arising from the mismatch between the various devices in circuit. Figure 8(b) plots the temperature variation of V_{REF}, i.e.,

$$\frac{\Delta V_{REF}}{V_{REF}} = \frac{\left(V_{REF,Max} - V_{REF,min}\right)}{V_{REF,Max}} \tag{17}$$

over -20 to 140°C compared to the corresponding $\Delta V_{REF}/V_{REF}$ value at the same temperature range but without any error on K_{OS} value, i.e., assuming $\Delta K_{OS} = 0$ (while $V_{OS} \neq 0$). Based on Fig. 8(b), both curves have approximately the same shape and in many samples the two curves have almost the same value. This means that in this design V_{OS} has the greatest effect on increasing the temperature variations at the output reference voltage, while errors on K and N values (or $K_{OS} = N \times K$) have much less effects. This result confirms that for lower temperature coefficient (TC) values on V_{REF}, both K_{OS} and V_{OS} (amplifier offset)

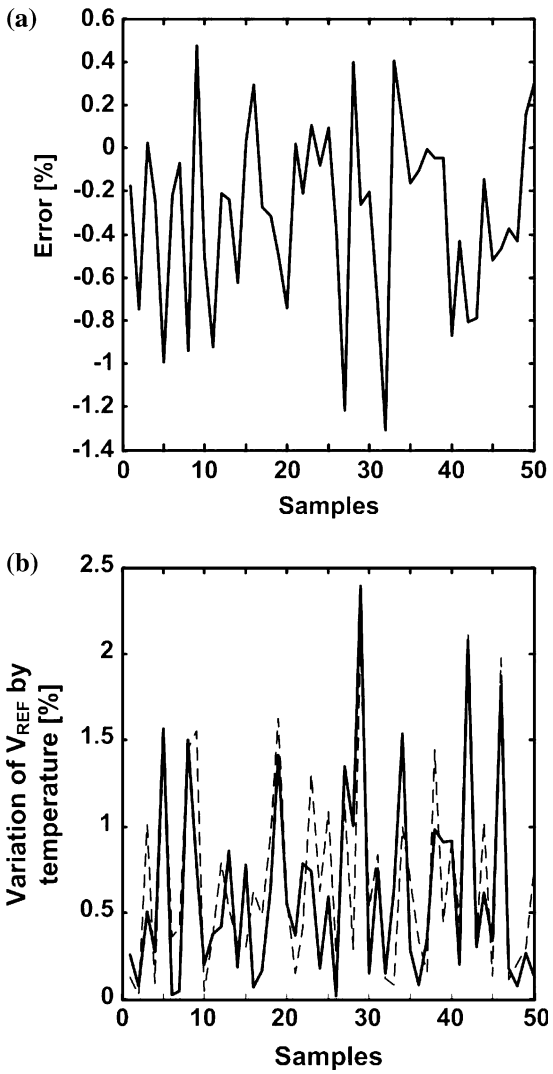

Fig. 8 Monte Carlo simulation results on **a** error in $K_{OS} = N \cdot K$ (ΔK_{OS}), **b** Total temperature variation of V_{REF} (*solid line*) compared to the corresponding ideal value of V_{REF} plus amplifier offset effect (*dashed line*)

should to be minimized. The former is determined by the circuit parameters and has been included in the FOM in (15) while the latter depends on the process specifications. A careful design and layout is required to reduce the amplifier offset. Large transistors with large V_{DSsat} (MOS saturation voltage) values can be helpful for this purpose.

Simulation results included in Table 4 shows that nominal value of V_{REF} is $\mu_{VREF} = 1.2411$ V with a standard deviation of $\sigma_{VREF} = 9.4$ mV [16]. For further reduction in the power dissipation, it is possible to use larger values for η in (15), although it will results in a larger area or more offset gain. Lack of resistors with high sheet resistance at the proposed digital CMOS process is the main barrier for further reduction of the power dissipation.

4 Conclusions

A structured design methodology for optimizing the area-power consumption of bandgap voltage reference circuits has been presented. In this approach, fundamental equations of the bandgap circuit based on process and circuit parameters were extracted. These equations besides the estimated area and power dissipation and the amplifier offset effect were used to determine the circuit parameters. Likewise, calculating the parameters in a very short time makes this method a useful approach to design an optimized bandgap circuit with the desired specifications.

The size of MOS transistors in the bandgap core and amplifier were chosen such that the mismatch effect has been reduced to an acceptable level. Based on the proposed approach, a bandgap voltage circuit has been implemented in a digital 0.5 μm CMOS technology. This circuit shows a temperature coefficient of 15.6 ppm/°C with a standard deviation of 9.4 mV and consuming 160 μA and silicon area of 0.085 mm^2.

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