

Ultra-low power subthreshold current-mode logic utilising PMOS load device

A. Tajalli, E. Vittoz, Y. Leblebici and E.J. Brauer

A novel approach for implementing MOS current-mode logic circuits that can operate with ultra-low bias currents is introduced. Measurements of test structures fabricated in 0.18 μm CMOS technology show that the proposed PMOS load device concept can be utilised successfully for bias currents as low as 1 nA, achieving sufficiently high gain (>3) over a wide frequency range.

Introduction: Current-mode logic (CML) circuits are widely used in many high-speed and high-performance applications [1]. The differential topology of CML circuits provides high immunity to supply noise and crosstalk, while reduced voltage swing at the output helps to operate the circuit in very high frequencies with low noise generation [1, 2]. These properties make the MOS CML (MCML) topology an attractive candidate for ultra-low power applications as well. This, however, usually requires that the circuit be biased in the subthreshold region, conducting a very low tail current and still producing a sufficiently large output swing. While several techniques for implementing CMOS logic circuits with transistors in the subthreshold regime and with very low power dissipation have been already introduced [3], the design of ultra-low power MCML circuits is yet an open research subject. This Letter introduces a new approach for implementing MCML circuits that can be applied to digital CMOS technologies.

Ultra-low power MCML topology: Fig. 1 shows an MCML buffer stage. The logic operation in this topology is performed in the current domain while the input source-coupled NMOS differential pair (M_1 and M_2) is switching a constant current between two branches. Thus, the inherent speed of the circuit can be high, and is mainly governed by the amount of tail current I_{SS} . The current is converted again to voltage output through the load resistors (R_L). The voltage swing at the output, i.e. $V_{sw} = R_L I_{SS}$, should be large enough to completely switch the current in the input transistors of the next stage, i.e. $V_{sw} > \sqrt{(2)V_{dsat}}$ (V_{dsat} is the drain-source overdrive voltage of input NMOS devices) when the device is biased in strong inversion and $V_{sw} > 4 \times nU_t$ when the device is biased in subthreshold where $U_t = kT/q$ is the thermal voltage and n is the subthreshold slope factor [4]. The main problem in a low-current MCML circuit is the realisation of very large, linear load resistors required for sufficient output swing. The load resistor should also be well controllable in order to adjust the output voltage swing to the desired value. In [4], the finite output resistance of the PMOS devices biased in the saturation (weak inversion) regime has been exploited to realise the desired large resistance for the design of subthreshold current-mode circuits. Here, we propose a novel load device biasing scheme in order to achieve large load resistivity with repeatable, good control on the resistance value.

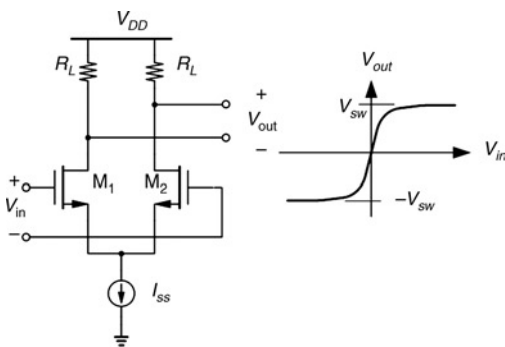


Fig. 1 MCML buffer stage and its DC transfer characteristics

A conventional PMOS device biased in the triode region would typically require a very large channel length to implement the large resistance, resulting in increased area and parasitic capacitance at the output. Fig. 2 (inset) shows the proposed connection of the load device that can be used as a high resistance element where the body (n -well) terminal is connected to drain. Based on the EKV model [5], the I-V characteristics of this device can be expressed as:

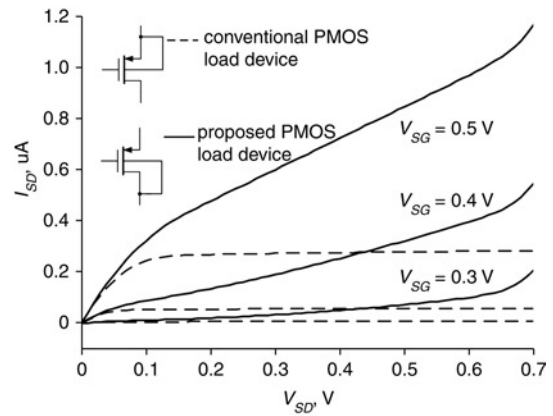


Fig. 2 I_{SD} - V_{SD} characteristics of proposed load device compared to conventional PMOS device

$$I_{SD} = I_{SD0} \exp(-V_{SD}/n_p U_t) [\exp(V_{SD}/U_t) - 1] \quad (1)$$

where $I_{SD0} = 2n_p \mu C_{ox} (W/L_e) U_t^2 \exp((V_{SG} - |V_{T0}|)/n_p U_t)$ (μ is the carrier mobility, C_{ox} the gate oxide capacitance per unit area, W the width of the device, V_{T0} the threshold voltage of PMOS device, n_p the subthreshold factor for PMOS device, and L_e the effective device length) [5]. This expression indicates that I_{SD} will increase with increasing V_{SD} in this configuration and the slope factor would be $(n-1)/n_p$. As shown in Fig. 2, the useful resistivity range of this device can be significantly extended into the saturation region, compared to the characteristics of a conventional PMOS load device.

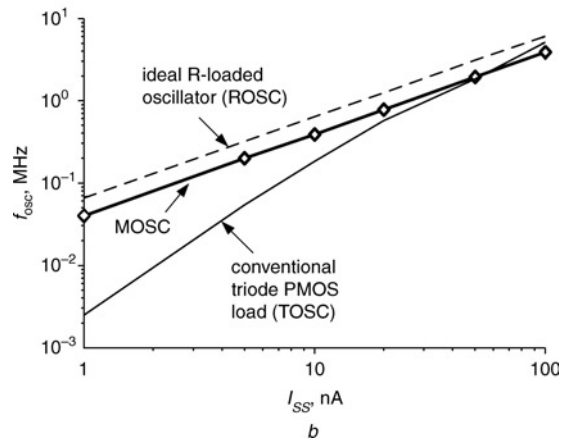
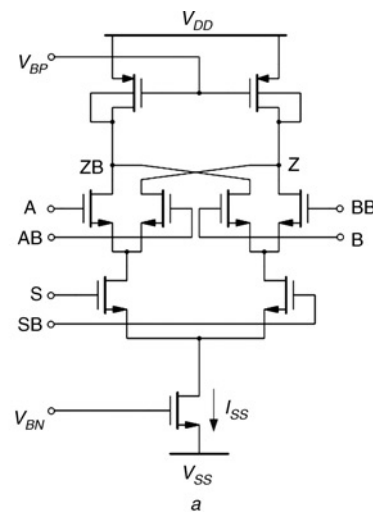


Fig. 3 Ring oscillator test circuit
 a MCML MUX gate utilising proposed load configuration
 b Oscillation frequency of five-stage ring oscillator using three different kinds of MCML gates as delay cells

Circuit performance: To explore the performance of the proposed circuit, a ring oscillator has been designed based on MCML AND gates as the delay cells using a conventional 0.18 μm CMOS technology. Fig 3a shows an MCML MUX circuit built using the proposed topology that has been configured as an AND gate to implement the proposed delay stage. The oscillation frequency of this circuit (called MOSC) has been compared to a CML-based oscillator using ideal resistors as the load (called ROSC and $R_L = V_{sw}/I_{SS}$) and also to an MCML-based oscillator using triode-mode PMOS load devices (called TOSC). In Fig. 3b, it can be seen that the operation frequency of the proposed MOSC is very close to the 'ideal' ROSC which in practice presents the upper limit of the achievable oscillation frequency. The main reason for the oscillation frequency reduction in MOSC compared to the ROSC is the parasitic capacitance of the reverse biased p - n junction between the n -well and the p -substrate. Compared to the TOSC, the proposed topology exhibits a slightly lower oscillation frequency for $I_{SS} > 100$ nA. However, for low bias currents, the MOSC circuit oscillates at frequencies much higher than TOSC. For $I_{SS} = 10$ nA for example, the oscillation frequency of the MOSC is 25 times higher than that of TOSC. The main reason for this difference is that the triode-mode PMOS load devices in TOSC must be scaled up to operate at very low bias current levels, increasing the parasitics significantly.

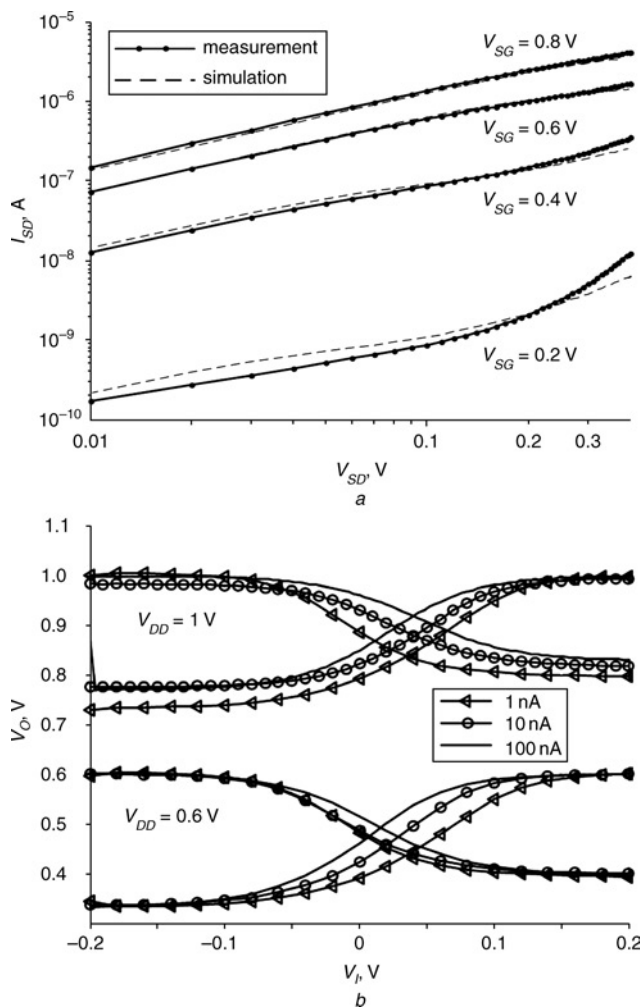


Fig. 4 Measurement results
 a I_{SD} against V_{SD} for proposed load device in compared to simulation results
 b Input-output DC characteristics for MCML buffer utilising proposed load device in different bias currents and supply voltages

Measurement results: A test chip has been fabricated in 0.18 μm CMOS technology, and it has been characterised extensively. Fig. 4a shows the measured I-V characteristics of the load PMOS device compared to the simulation results. The resulting I-V curve and especially the slope are well matched to the simulations. The DC transfer characteristics of an MCML buffer implemented based on the proposed topology has been measured with different bias currents and different supply voltages. Fig 4b shows the measured input-output characteristics for this buffer. The transfer characteristics of the circuits have been measured for three different bias currents and for two different supply voltage levels: 0.6 and 1.0 V.

It can be shown that the DC gain of this circuit is:

$$A_v \simeq n_p / (n_n(n_p - 1)) \quad (2)$$

Here, n_p and n_n are the subthreshold factors for PMOS and NMOS devices, respectively. As confirmed by measurement, the gain estimated by (2) is about 3.2. Also, it can be concluded from (2) that the circuit gain will improve by reducing the device slope factor. The power-delay-product (PDP) of the proposed gate is in the sub-fJ-range, and three to five times smaller than that of the conventional CMOS gates operating in the subthreshold regime, with the same supply voltage.

Conclusions: A novel technique for implementing ultra-low power MCML circuits has been presented. The proposed approach benefits from small size PMOS load devices realising very high value resistances. Analyses and silicon measurements prove the capabilities of the proposed technique for implementing circuits operating in the nA range. Further, it is possible to adjust the frequency of operation in a very wide range by adjusting the bias current and without resizing the devices. This feature makes the proposed technique very desirable for ultra-low power programmable applications.

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