

Ultra Low Power Subthreshold MOS Current Mode Logic Circuits Using a Novel Load Device Concept

Armin Tajalli, Eric Vittoz, Yusuf Leblebici

Microelectronic Systems Laboratory (LSM)
Ecole Polytechnique Fédérale de Lausanne (EPFL)
1015 Lausanne, Switzerland

E-mail: [armin.tajalli, eric.vittoz, yusuf.leblebici]@epfl.ch

Elizabeth J. Brauer

Department of Electrical Engineering
Northern Arizona University
Flagstaff, AZ 86011, USA

E-mail: elizabeth.brauer@nau.edu

Abstract— This article presents a novel and robust approach for implementing ultra-low power MOS current mode logic (MCML) circuits. To operate at very low bias currents, a simple and compact high resistance load device has been introduced. Operating in subthreshold regime, the circuit can be used in a very wide frequency range by adjusting the bias current without any need for resizing the devices. Measurements in 0.18 μm CMOS technology show that the proposed MCML circuit can be operated reliably with bias currents as low as 1 nA offering a significant improvement of the power-delay product compared to conventional CMOS gates. Simulations show that the proposed circuit exhibits faster response compared to the conventional MCML circuits with triode-mode PMOS load devices at low bias currents.

I. INTRODUCTION

Ultra low-power logic circuits with the capability of operating at relatively high frequencies are very desirable in many modern applications such as portable equipment or implanted biomedical systems [1]-[3]. The source-coupled logic (SCL) or current-mode logic (CML) topology has always been a very good candidate for implementing high-speed logic circuits [4]. In addition to the benefits of low signal swing and fast switching speed, they also show a very low sensitivity to supply and substrate noise due to their differential topology [4], [5]. However, the design of ultra low-power MCML-based circuits remains an important challenge. While several techniques for implementing CMOS logic circuits with transistors in the subthreshold regime and with very low power dissipation have been already introduced [1], the design of MCML circuits operating in subthreshold is yet an open research subject.

This paper introduces a new approach for implementing low-power MCML circuits that can be applied to digital CMOS technologies. Section II presents the novel load device and in Section III the performance of some basic circuits implemented based on the proposed technique are studied. Measurement results are presented in Section IV. Conclusions are presented in Section V.

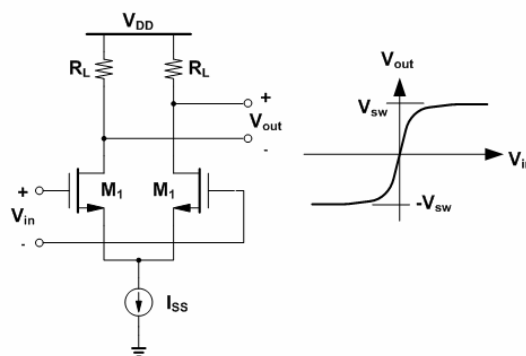


Figure 1. Basic MCML buffer stage and its DC transfer characteristics

II. PROPOSED TOPOLOGY

A. MCML Topology

Figure 1 shows a basic MCML buffer stage. With this circuit, the logic operation is performed in the current domain while the input source-coupled NMOS differential pair (M_1 and M_2) switches a constant current between two branches. Therefore, the inherent speed of the circuit can be high, and is mainly governed by the amount of tail current I_{SS} . The current is converted again to voltage output through the load resistors (R_L). The voltage swing at the output, i.e., $V_{sw} = R_L \cdot I_{SS}$, should be large enough to completely switch the current in the input transistors of the next stage. Based on this observation, the voltage swing should be larger than $\sqrt{2} \cdot V_{dsat}$ (V_{dsat} is the drain-source saturation voltage of input NMOS devices) when the device is biased in strong inversion [4] and larger than about $4 \times n \cdot U_t$ when the device is biased in subthreshold [6] where $U_t = kT/q$ is the thermal voltage and n is the subthreshold slope factor. The main problem in a low-current MCML circuit is the realization of very large load resistors required for a reasonable output swing. For example, a swing of $V_{sw} = 200$ mV with $I_{SS} = 10$ nA requires that $R_L = 20$ M Ω . This load resistor could be implemented by a very long PMOS

device which will increase the area and parasitic capacitance at the output. This resistor should be also well controllable to be able to adjust the output voltage swing to the desired value.

In [7], utilization of the finite output impedance of very short-channel PMOS load devices biased in saturation is proposed as means to achieve the desired large resistance. However, more studies are needed for exploring the matching properties of output impedance of MOS devices.

B. Load Device

The conventional PMOS load device is shown in Fig. 2(a) with the bulk terminal connected to VDD. The proposed load device configuration consists of a PMOS transistor where the bulk terminal (n-well) is connected to the drain (Fig. 2(b)). Due to the well-known dependence of the threshold voltage (V_{TH}) on the substrate potential, the drain current of this device keeps increasing with increasing V_{SD} . As shown in Fig. 3, this will result in a finite large equivalent resistance instead of almost infinite output impedance of conventional PMOS device.

Figure 2(c) shows the cross-section view of the proposed device including the two parasitic bipolar transistors which also contribute to the observed device behavior. Based on this figure and using EKV model [6], it is possible to describe the behavior of this device in more detail. Defining:

$$I_{SD0} = I_0 \cdot \exp(V_{SG}/n \cdot U_t) \quad (1)$$

then, based on EKV model, the drain current of the proposed PMOS device is

$$I_{SD} = I_{SD0} \cdot \exp(-V_{SD}/n \cdot U_t) \cdot [\exp(V_{SD}/U_t) - 1] \quad (2)$$

Figure 4 shows the I_{SD} versus V_{SD} for the proposed device. As can be seen, the simulated behavior of the device is very well described by (2) after adding a diode to simulate the effect of bipolars.

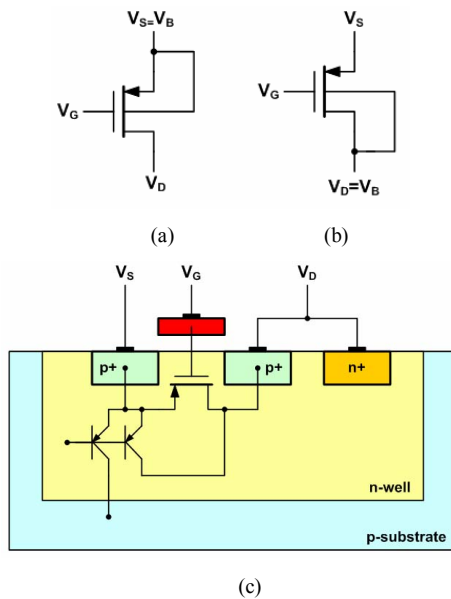


Figure 2. (a) Conventional and, (b) the proposed PMOS load configuration, (c) cross-section view of the proposed PMOS load device and parasitic elements

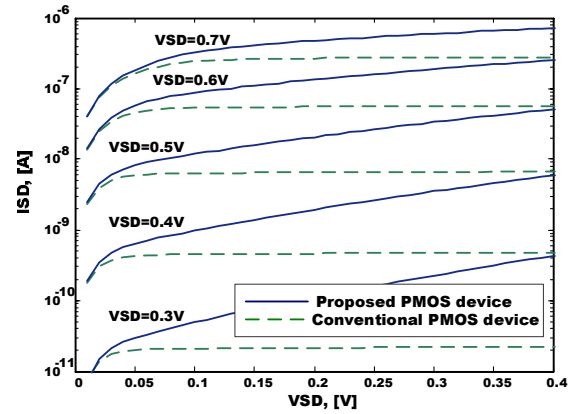


Figure 3. Simulated I-V characteristics for (a) simple PMOS device with bulk tied to the source, (b) proposed topology in which the bulk is connected to the drain ($W=250$ nm, $L=400$ nm)

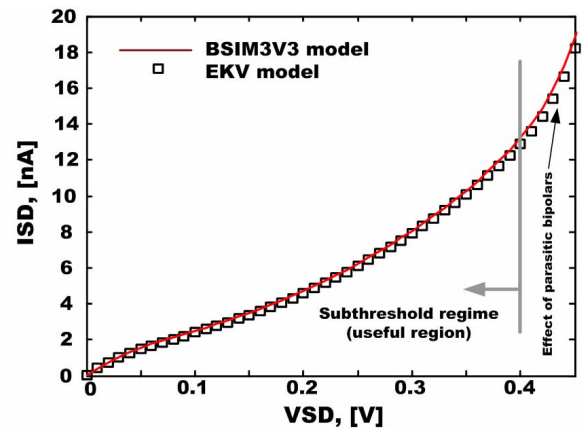


Figure 4. I_{SD} vs V_{SD} for the proposed PMOS device ($V_{SG}=300$ mV, $W=250$ nm, $L=400$ nm)

For $V_{SD} < 0.4$ V, the device is in normal subthreshold region while for larger V_{SD} values the PN junction of source-well becomes forward biased. Concerning the voltage swing needed to switch the input differential pair of an MCML circuit, the desired operation region would be $V_{SD} < 400$ mV (typically 200 mV).

III. CIRCUIT PERFORMANCE

To explore the performance of the proposed circuit, a ring oscillator has been designed based on MCML AND gates as the delay cells using a conventional $0.18 \mu\text{m}$ CMOS technology. Figure 5(a) shows a MCML MUX based on the proposed topology that has been configured as an AND gate to implement the proposed delay stage. The oscillation frequency of this circuit (called MOSC) has been compared to a CML-based oscillator using ideal resistors as the load (called ROSC and $R_L = V_{sw}/I_{SS}$) and also to a MCML-based oscillator using triode PMOS load devices (called TOSC). In this simulation, the parasitic capacitors due to the wiring have been also modeled to have a more realistic estimation. In all circuits, the output swing has been controlled carefully using a replica bias circuit [4]. Figure 5(b) shows the simulated waveforms of the proposed MCML AND gate used as the delay stage in ring

oscillator. As $G_{DS}(V_{SD} = 0) = I_{SD0}/U_i$ (based on (2)), the output nodes are pulled up to V_{DD} . In Fig. 6, it can be seen that the operation frequency of the proposed MOSC is very close to the “ideal” ROSC which in practice presents the upper limit of the achievable oscillation frequency. The main reason for the oscillation frequency reduction in MOSC compared to the ROSC is the parasitic capacitance of the reverse biased PN junction between the n-well and the p-substrate (Fig. 2(c)). Compared to the TOSC, the proposed topology shows a slightly smaller oscillation frequency for $I_{SS} > 100$ nA, However, for low bias currents, the MOSC circuit oscillates at frequencies much higher than TOSC. For $I_{SS} = 1.0$ nA, the oscillation frequency of the MOSC is 14 times higher than that of TOSC. The main reason for this difference is that the length of the triode-mode PMOS load devices in TOSC must be increased at very low bias current levels.

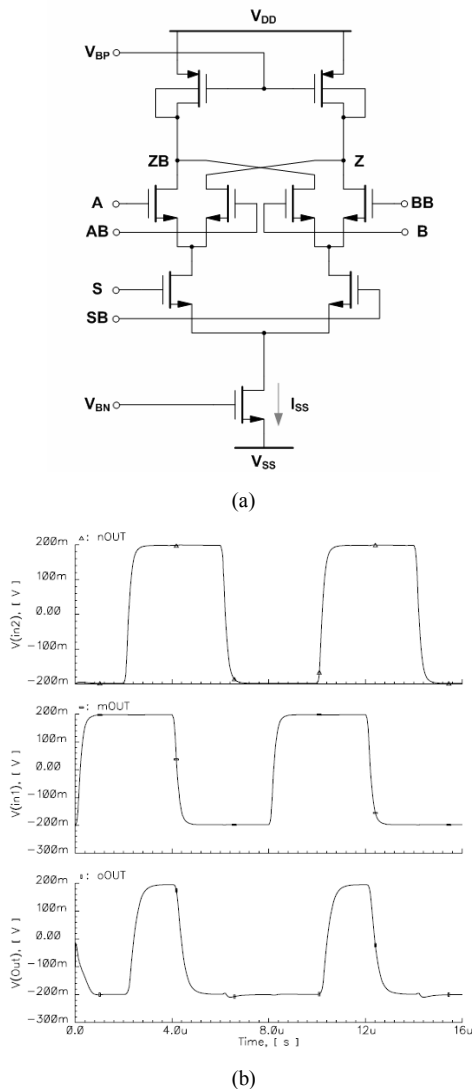


Figure 5. (a) MUX gate based on proposed topology, (b) transient response of the proposed MCML AND gate where the inputs are provided by MCML buffers ($V_{DD}=0.6$ V, $I_{SS}=10$ nA, FO=4)

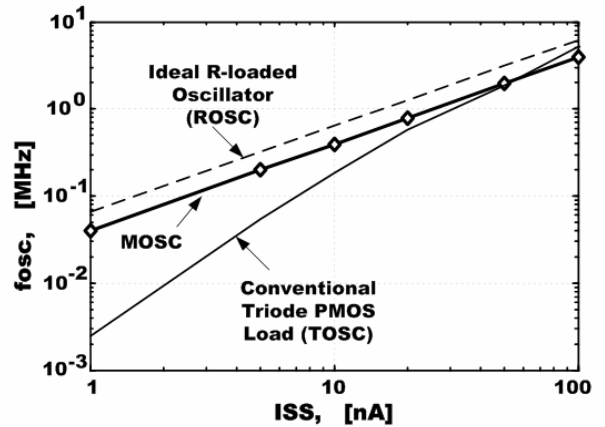


Figure 6. Comparing the oscillation frequency for a 5 stage ring oscillator simulated with the proposed PMOS load (MOSC), with the triode-mode PMOS load (TOSC), and with the ideal resistive load (ROSC). Here, the output swing is kept constant using a replica bias circuit [4].

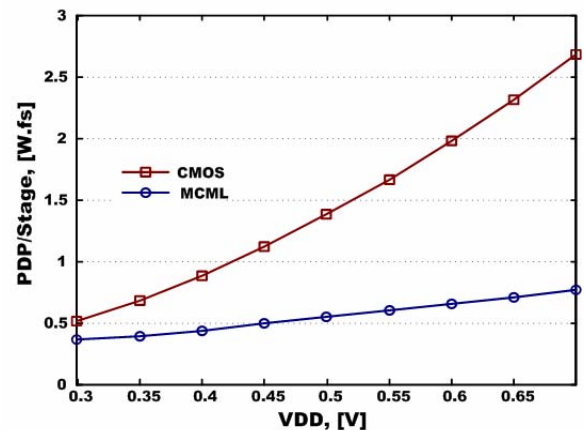


Figure 7. Simulated power-delay product for the proposed MCML circuit in comparison to the conventional CMOS gate, as a function of supply voltage

The other important point in Fig. 6 is that without any need to scale the sizes of devices, the circuit can operate over a very wide frequency range. This makes the proposed topology very suitable for programmable applications. Figure 7 compares the power-delay product (PDP) for the proposed MCML gates and CMOS gates from a typical $0.18 \mu\text{m}$ standard cell library, emphasizing the significant improvement of PDP that can be achieved with the proposed approach.

Simulation results for two different technologies (180 nm and 130 nm) have also shown that the benefits of this circuit topology are largely independent of technology.

IV. MEASUREMENT RESULTS

A test chip has been fabricated in $0.18 \mu\text{m}$ CMOS technology, and it has been characterized extensively. Figure 8 shows the measured I-V characteristics of the load PMOS device for 3 different test samples in comparison to the simulation results. The resulting I-V curve and especially the slope are well matched to the simulations.

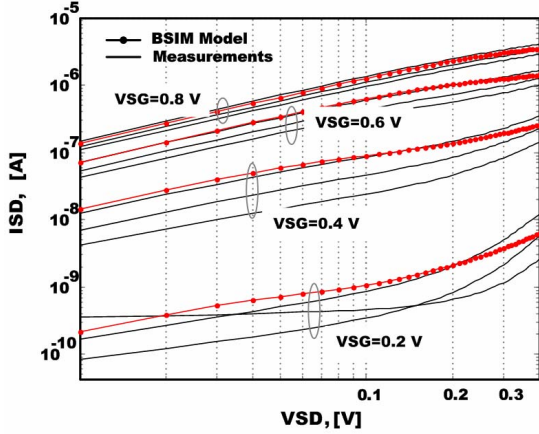


Figure 8. Measured I-V characteristics of the proposed PMOS load in comparison to simulation results ($W=250$ nm, $L=400$ nm). Each solid line represents a separate test sample.

Meanwhile, the DC transfer characteristics of a MCML buffer and a MCML full adder implemented based on the proposed topology have been measured with different bias currents and different supply voltages. Figures 9(a) and 9(b) show the measured input-output characteristics for these two cells. In these measurements, the output swing is kept constant, at $V_{sw} = 200$ mV. The transfer characteristics of the circuits have been measured for three different bias currents of 1, 10, 100, 1000 nA while the supply voltage has been reduced to 0.6 V.

In the proposed topology, the gain of each stage depends on the voltage swing V_{sw} . To calculate the voltage gain, the transconductance of the input differential pair can be expressed by:

$$g_m = \frac{I_{SS}}{2n \cdot U_t} \cdot \frac{1}{\cosh^2(\Delta V_i / (2 \cdot n \cdot U_t))} \quad (3)$$

(ΔV_i is the input differential voltage) and the G_{SD} of the load PMOS devices can be calculated from (2). Then it can be shown that the upper bound for differential gain of the circuit for $\Delta V_i = 0$ V would be:

$$A_v < n_p / (n_n \cdot (n_p - 1)) \quad (4)$$

where, n_p and n_n are the subthreshold factors for PMOS and NMOS devices, respectively. As confirmed by measurement, the gain estimated by (4) is about 3.2. Also, it can be concluded from (4) that the circuit gain will improve by reducing the device slope factor. This is helpful especially in deep submicron technologies where the slope factor moves toward one.

V. CONCLUSIONS

This paper presents a novel technique for implementing ultra low power MCML circuits. The proposed approach benefits from small size PMOS load devices to replace high value resistors. Analyses and silicon measurements prove the capabilities of the proposed technique for implementing circuits operating in the nA range. Further, it is possible to adapt the power consumption to the required frequency of

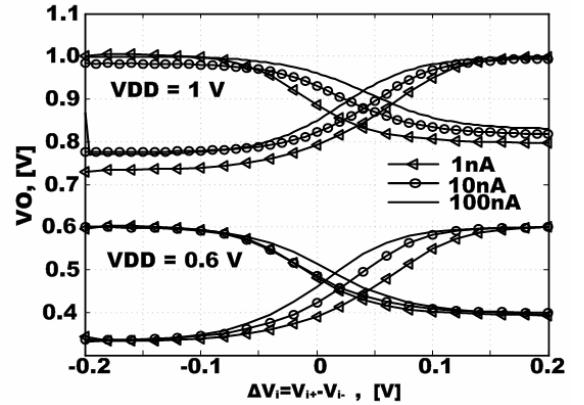
operation in a very wide range by adjusting the bias current and without resizing the devices. This makes this technique very desirable for ultra low-power programmable applications.

ACKNOWLEDGEMENT

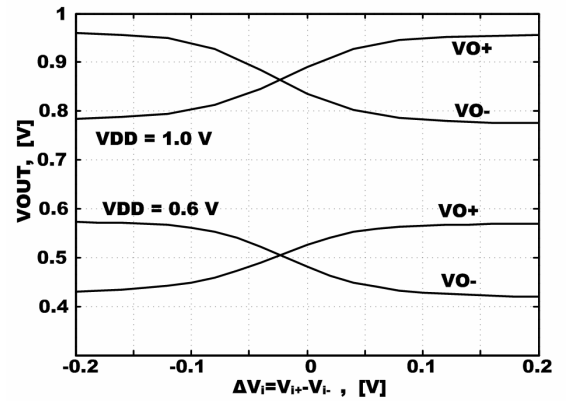
The authors would like to thank Z. Toprak Deniz for her valuable help in designing the test chip.

REFERENCES

- [1] H. Soeleman, K. Roy, and B. C. Paul, "Robust subthreshold logic for ultra-low power operation," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 1, pp. 90-99, Sep. 2001.
- [2] A. P. Chandrakasan et al., "Low-power CMOS digital design," *IEEE J. Solid State Circuits*, vol. 27, pp. 473-484, Apr. 1992.
- [3] M. Horowitz et al., "Low-power digital design," in *IEEE Int. Symp. Low Power Electron. Design*, 1994, p. 8-11.
- [4] B. Razavi, *Design of Integrated Circuits for Optical Communications*, McGraw-Hill, 2003.
- [5] J. M. Musicer, and J. Rabaey, "MOS current mode logic for low power, low noise CORDIC computation in mixed-signal environment," in *Proc. of Int. Symp. on Low Power Elect. and Des.*, pp.102-107, 2000.
- [6] C. Enz, and E. Vittoz, *Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design*, John Wiley and Sons Ltd, 2006.
- [7] F. Cannillo, and C. Toumazou, "Nano-power subthreshold current-mode logic in sub-100nm technologies," *IEE Electronics Letters*, vol. 41, no. 23, November 2005.



(a)



(b)

Figure 9. Measured DC transfer characteristics of (a) buffer [$V_{DD}=0.6, 1.0$ V, $I_{SS}=1, 10, 100, 1000$ nA], (b) full adder [$V_{DD}=0.6, 1.0$ V, $I_{SS}=100$ nA]