A Power-Efficient LVDS Driver Circuit in 0.18-µm CMOS Technology

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***Abstract*— This article presents a power-efficient and low-voltage CMOS output driver circuit based on low-voltage differential signaling (LVDS) standard. To reduce the ringing at the output of the proposed driver circuit and simultaneously keep the power consumption low, a new technique has been applied to control the output voltage slew. A pre-driver circuit is also utilized to have a very low total equivalent input capacitance of 50 fF. Designed in 0.18 µm CMOS technology, the entire output driver circuit including the input pre-driver, draws only 5.6 mA_{rms} while the output voltage swing is V_{OD} = 400 mV and the other specs are compliant with the LVDS requirements.**

I. INTRODUCTION

LVDS output drivers (ODs) play a very important role in chip-to-chip interconnections [1]. Demand for increasing the data transmission speed and the number of I/Os in modern applications, have made the design of high-performance and low-power ODs very desirable [2]-[4]. The main limiting factor for reducing the power dissipation in OD circuits is keeping the signal-to-noise ratio (SNR) on desired value. For this reason the voltage swing at the output must be kept large enough. Therefore, gradual reduction of supply voltage has made the design of OD circuits very challenging. While this circuit should drive a very large amount of current into the load in order to achieve the desired SNR, supply voltage reduction makes the current switching process very difficult.

This article describes the design of a low-voltage and power-efficient OD circuit in 0.18 µm CMOS technology based on LVDS requirements [1]. To keep the power dissipation n an acceptable level and simultaneously preserve the impedance matching, a new pre-emphasis technique has been proposed. To operate in such a low supply voltage, a pre-driver stage is applied also to control the voltage swing and also the common-mode voltage at the input of OD circuit very carefully.

The circuit topology of the proposed LVDS output driver is described in section II and simulation results will be explained in section III.

TABLE I. THE MAIN LVDS DRIVER REQUIREMENTS [1]

Parameter	Min.	Max.	Unit
V_{OD} (Differential voltage swing)	247	454	mV
V_{OS} (Common-mode voltage)	1.125	1.375	V
ΔV_{OD} (Acceptable mismatch on V_{OD})		50	mV
ΔV_{OS} (Acceptable mismatch on V_{OS})		50	mV
t_r, t_f (Rise and fall time)	0.26	1.2	ns

II. LVDS DRIVER CIRCUIT

A. Standard Requirements

Table I briefly describes the requirements of an output driver circuit based on LVDS standard. Regarding these requirements, it is very difficult to achieve the desired output voltage swing (V_{OD}) and output common-mode voltage (V_{OS}), while using a single 1.8 V supply voltage. Therefore, a very careful design strategy is required to satisfy all these specifications. Based on [1], the OD should be also able to drive an external differential 100 Ω termination resistor.

B. Driver Circuit

As a simple solution, an SCL (source-coupled logic) – based topology using load resistors can be applied as an output driver circuit. Although the impedance matching in this case is very good because of using internal load resistors, however, the power consumption would be high. The main reason for the high power consumption in this case is that the circuit should drive on-chip low-impedance load resistors in addition to the output termination resistor. Therefore, to keep the power consumption low, it is preferred to avoid internal termination resistors which double the power consumption. Switching both of the source and sink currents at the output stage helps more to reduce the total current consumption at the output stage. Figure 1 shows a sample LVDS output driver circuit, pre-driver buffers, and also practical connections and load model. In this work, a two-stage pre-driver buffer is applied to drive the large input capacitance of the OD stage.

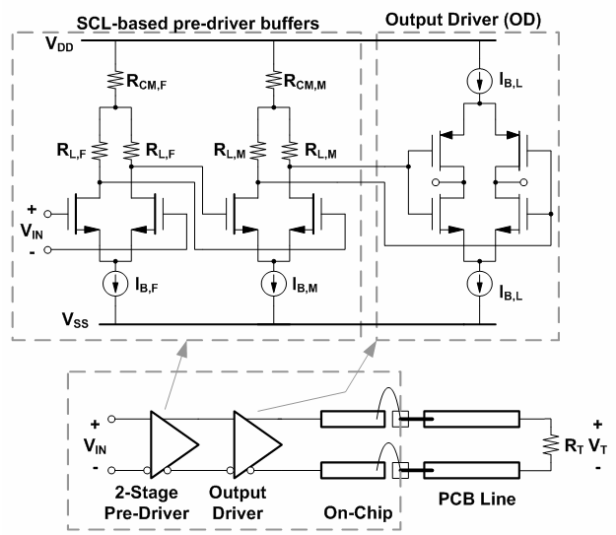

Figure 1. Input buffers, LVDS output driver (OD) stage, and practical loading (including on-chip and off-chip parasitic elements, and also termination)

These buffers also control the input common-mode (CM) voltage of the OD circuit very carefully. In this way, the transistors at the output stage (including tail current bias transistors) will remain in desired regime of operation for the whole switching process. To set the input common-mode voltage, a series resistance is added to each buffer stage as shown in Fig. 1 ($R_{CM,F}$ and $R_{CM,M}$).

In order to reduce the power-dissipation, internal termination resistors have not been applied and a new technique for controlling the output voltage slew has been proposed to compensate the impedance mismatch effect at the interfaces. While the required bias current at the OD depends on desired output voltage swing ($V_{sw,T}$) and also termination resistor (R_T) by: $I_{B,L} = V_{sw,T}/R_T$, the power consumption at the pre-driver stage highly depends on the input capacitance of the OD circuit. Hence, to reduce the total power consumption, the equivalent input capacitance of OD or in other words, the size of output switching transistors should be kept as small as possible. Based on Fig. 1, the total current drawn from the supply is:

$$I_{B,tot} = (I_{B,F} + I_{B,M}) + I_{B,L} \qquad (1)$$

in which $I_{B,F}$ and $I_{B,M}$ are the bias current of the first and second pre-driver stages (Fig. 1). It can be shown that these currents can be expressed approximately by:

$$I_{B,M} = \frac{V_{sw,M}}{R_{L,M}} = \frac{m_T}{T} \cdot \frac{L_{\min}^2}{V_{dsat}^2} \cdot \frac{V_{sw,M} \cdot V_{sw,T} \cdot \alpha \cdot C_{ox}}{R_T} \cdot \frac{k_N' + k_P'}{k_N' \cdot k_P'} \qquad (2)$$

$$I_{B,F} = \frac{V_{sw,F}}{R_{L,F}} = \frac{m_T}{T} \cdot \frac{L_{\min}^2}{V_{dsat}^2} \cdot \frac{V_{sw,F} \cdot I_{B,M} \cdot \beta \cdot C_{ox}}{k_N'} \qquad (3)$$

where V_{sw} indicates the voltage swing at the corresponding nodes, R_L is load resistance in each stage, T is the period of the input data or clock, V_{dsat} indicates the drain-source saturation voltage, $k' = \mu_{eff} C_{ox}$, the parameters α and β are added to take into account the effect of wiring or other parasitic capacitors ($\alpha, \beta \geq 1$), and $m_T = T/\tau$ ($\tau = R_L \cdot C_L$ is the time constant of the corresponding node).

To derive these equations, the settling time in each node is estimated and then the corresponding bias current is determined such that the time constant at the proposed node be m_T times smaller than T. Figure 2 shows the estimated total current consumption of the circuit shown in Fig. 1 based on (1)-(3). As can be seen in this figure, $I_{B,tot}$ depends highly on the desired voltage swing at the output as well as the speed of operation (through m_T and T). It means that to have a faster settling time at the internal nodes, the power consumption must be increased proportionally. In this work $T = 4$ ns and $m_T \approx 10$. Meanwhile, by choosing the minimum possible value for the output voltage swing, it is possible to reduce all the bias currents ($I_{B,F}$, $I_{B,M}$, and $I_{B,L}$) and hence reduce the power dissipation.

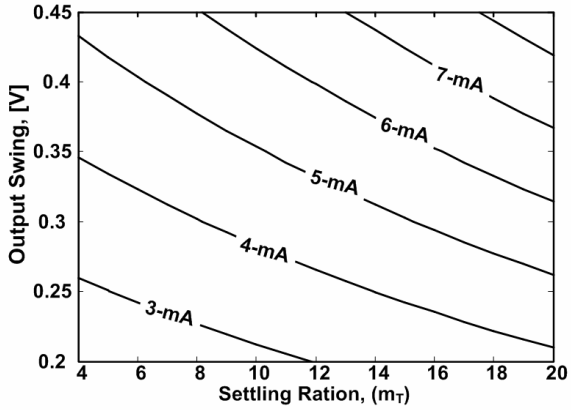

Figure 2. Estimated total current consumption of the whole driver circuit

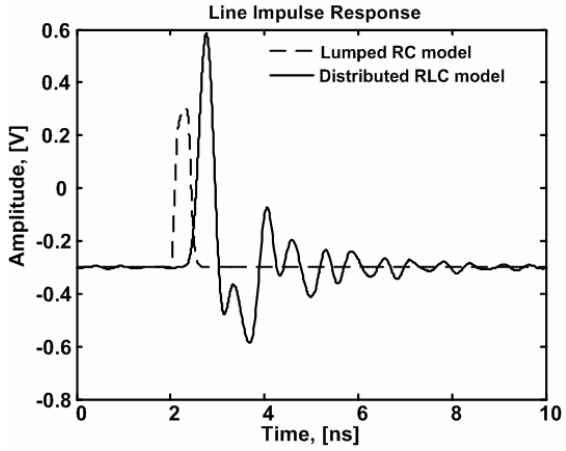

Figure 3. Line impulse response

C. Driver Step-Response

Because of several non-ideality effects like non-ideal transmission lines, unperfect termination, and pad parasitic effects, there are voltage spikes and also ringing on the output voltage. The impulse response of the proposed line is shown in Fig. 3. The pulse response in presence of line parasitic elements shows a large peaking followed by ringing [5]. To have an acceptable output waveform, it is possible to compensate this characteristic by pre-emphasis techniques. Because of the importance of power dissipation in the proposed application, a very low-power and simple compensation technique is intended.

Figure 4(a) shows the simplified topology of a differential driver and Fig. 4(b) introduces one possible remedy to control the output slew. Based on this technique, a part of current is delivered to the output by a delay through G_{m2} while the total driving current remains unchanged. Therefore:

$$G_m(s) = (G_{m1} + G_{m1}) \cdot \frac{1 + s \cdot R_P \cdot C_P \cdot G_{m1}/(G_{m1} + G_{m2})}{1 + s \cdot R_P \cdot C_P} \qquad (4)$$

Based on (4), the pole in the transfer function is smaller than the zero and so this topology has less transconductance in high frequencies (or equivalently in fast transitions) which helps to control the voltage slew.

The other possibility is shown in Fig. 4(c). In this topology, just the first part of the transconductance (i.e., G_{m1}) is driven by the input voltage V_{IN}, so the equivalent input capacitance would be smaller than in the previous approach and it makes the design of low-power pre-driver buffers much simpler. Based on this approach, the equivalent admittance of the cross-coupled transconductors at the output is:

$$Y_{eq}(s) = G_{m2} \cdot \frac{s \cdot C_A/G_{m2} - 1}{s \cdot R_A \cdot C_A + 1} \qquad (5)$$

Based on this, G_{m1} should be selected larger than G_{m2} to be sure that the circuit is stable. Figure 5 shows the driver circuit implemented based on Fig. 4(c). In this figure, M_{PDO} and M_{NDO} are implementing the G_{m1} and M_{PDX} while M_{NDX} are implementing the cross-coupled transconductors of G_{m2}. The total input capacitance of these transistors is large enough to implement the C_A. As shown in Fig. 6, the proposed OD shows a very smooth and fast settling time while driving the practical line. The whole circuit including the pre-driver stage benefits a fully differential topology which has a very good immunity to the power supply noise and produces very low current spikes on the power supply lines.

D. Common-Mode Feedback

Shown in Fig. 5, a simple common-mode feedback circuit has been applied to control the output CM value. Because of the large size of output transistors, stabilization of the CM loop is difficult. In the proposed circuit, R_C and C_C are used to compensate the loop frequency response. Meanwhile, the tail current PMOS transistor is divided to two transistors (M_{PBO} and M_{PCO}) to reduce the total CM feedback loop gain and also the total capacitance in node V_{CMFB}, and hence improving the stability.

Operating in a low supply voltage requires a very careful control on CM voltage and also voltage swing at the input of OD circuit. The input CM voltage of OD should be controlled such that both NMOS- and PMOS-side tail bias transistors stay in saturation region. For this reason, a separate CM feedback loop controls the CM voltage at the output of pre-driver stage (or input CM voltage of the OD) by controlling the current flow in $R_{CM,F}$ and $R_{CM,M}$ (in Fig. 1).

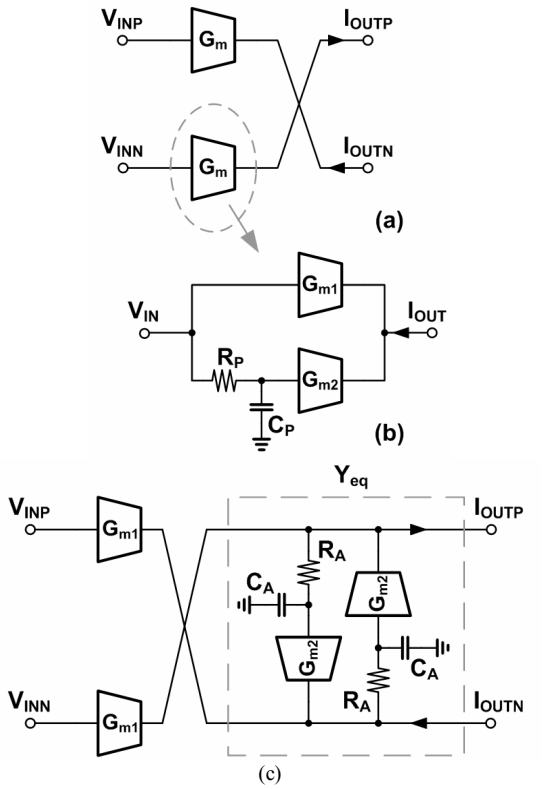

Figure 4. Compensating the step response of the OD

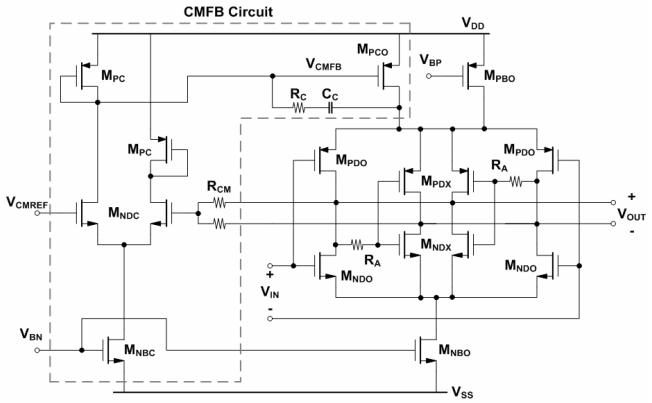

Figure 5. Proposed LVDS OD stage and the common-mode feedback circuit

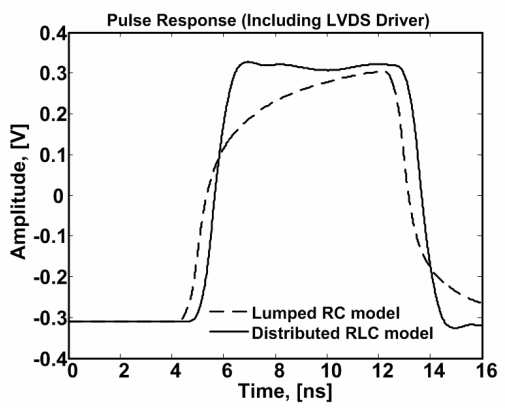

Figure 6. Simulated pulse response of the proposed LVDS driver with practical line model (filled line) in comparison to the ideal termination case (dashed line)

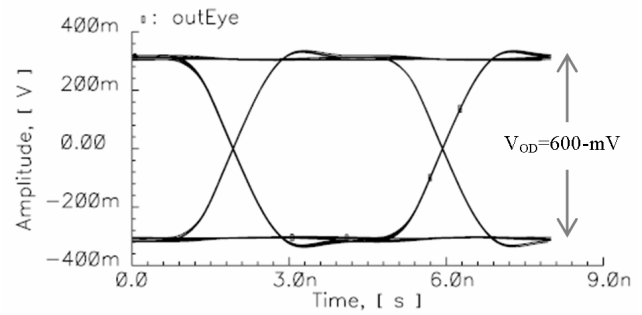

Figure 7. Simulated differential output signal eye diagram for a random input bit stream (V_{OD} = 600 mV_{pp}, slow corner, T=125°C)

III. Simulation Results

The proposed circuit has been designed in a conventional 0.18 µm CMOS technology. This circuit has been applied in a 250 MS/s analog-to-digital (ADC) data converter circuit and device sizes are optimized for this application.

Figure 7 shows the eye-diagram of the output signal for a random input bit stream. The output waveform shows a smooth transition with 1.1 ns rise and fall time. As shown in Fig. 8, cross-coupled switches at the output can result in a reduced total input capacitance of the OD circuit. This relaxes the power-speed tradeoff in pre-driver stage design.

The total input capacitance of the pre-driver buffer circuit is 50 fF (including the routing parasitic effect). Table 2 compares the proposed driver specifications with some other recently published reports. It can be seen that the proposed design methodology has resulted in a power-efficient LVDS driver while operating with a low supply voltage.

IV. Conclusion

In this article, a low-power LVDS driver for serial link applications has been developed. The proposed circuit includes input buffers to isolate the input digital circuits from the output part. A technique to reduce the input capacitance of the output LVDS driver stage and hence reducing the power consumption of the input buffers has been proposed. The whole circuit including input buffers draws 5.6 mA (4.0 mA) while driving a 100 Ω differential off-chip termination resistor in a swing of 400 mV (200 mV). A new pre-emphasis circuit is also suggested to improve the matching properties of the circuit. To our knowledge, this is significantly lower than the power dissipation of LVDS drivers presented earlier.

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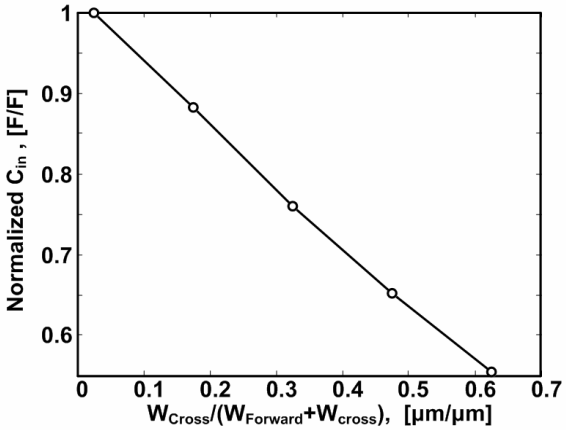

Figure 8. Input capacitance reduction in the OD stage by increasing the size of cross-coupled switches (M_{PDX} and M_{NDX}) respect to the size of M_{NDO} and M_{PDO} [see Fig. 5].

TABLE II. Comparison to the Other Works Reported in CMOS Technology

Ref.	Tech.	Supply [V]	V_{OD} [$mV_{pp,diff}$]	V_{OS} [V]	I_{DDrms} [mA_{rms}]
[5]	0.18 µm	1.8	200		13
[3]	0.35 µm	1.8			9
[4]	0.35 µm	3.3	100		10
[6]	0.18 µm	1.8	80		6.8
[7]	0.35 µm	3.3	320		5.5
This work	0.18 µm	1.8	400-800	1.2	4.0-5.6*

* Including the input buffer stages (pre-driver)