Introduction to the Special Issue on the IEEE 2002 Custom Integrated Circuits Conference

THIS Special Issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS is devoted to topics from the IEEE 2002 Custom Integrated Circuits Conference (CICC 2002). The selected papers reflect continuing trends toward higher levels of integration, lower power, and higher performance, along with the challenges in designing and verifying increasingly complex integrated circuits. The seventeen full papers are grouped into communications, analog, and digital systems papers. Five briefs conclude the issue.

The first four papers provide interesting insights into radio-frequency (RF) circuits and techniques. "Second-Order Intermodulation Mechanisms in CMOS Downconverters," by Manstretta *et al.*, covers a topic of fundamental importance for highly integrated transceivers. An in-depth discussion of the envelope distortion mechanisms is provided and the developed analytical models are supported by experimental results. The second paper, "Virtual Damping and Einstein Relation in Oscillators," by Ham and Hajimiri, introduces a new viewpoint on phase noise, starting from the fundamental physics of noise. The link between the new concepts and those more familiar to circuit designers is demonstrated by experiments. In the third paper, "Frequency-Independent Equivalent-Circuit Model for On-Chip Spiral Inductors," Cao *et al.* propose a 2Π ladder circuit to model spiral inductors. The equivalent circuit uses frequency-independent *RLC* elements, whose values can be analytically calculated based on the layout parameters. The region of model validity is proven to extend beyond the self-resonant frequency. Wireless LAN applications are currently drawing particular attention. In "A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18-μm CMOS," Cassan and Long propose a new low-noise amplifier (LNA) topology particularly suited for high-frequency operation. A low-loss feedback transformer is used to neutralize the gate–drain overlap capacitance of the input device. A differential implementation of the proposed circuit shows a 0.9-dB noise figure and $+0.9$-dBm IIP3 at 5.75 GHz while consuming 16 mW.

The next full paper, "An Adaptive PAM-4 5-Gb/s Backplane Transceiver in 0.25-μm CMOS," deals with a different subject: broad-band high-speed digital links. In this paper, Stonick *et al.* make use of multilevel signalling and self-adaptive equalization to enable 5-Gb/s communications across typical FR4 backplanes for distances up to 50 in. The device occupies 17 mm^2 and consumes 1 W.

The next nine papers focus on analog circuits. The first two of these papers concentrate on technology issues. In "Process and Circuit Design Interlock for Application-Dependent Scaling Tradeoffs and Optimization in the SoC Era," Diaz *et al.* describe well-known effects which are becoming of concern with the emergence of new technologies. Causes and remedies are reviewed, and a tighter collaboration between the process and circuit design is advocated. In "Understanding MOSFET Mismatch for Analog Design," Drennan and McAndrew focus on a novel technique to model device mismatch to gain new insight into its relation with technological variations.

Global clocks are generally implemented making heavy use of shielding and other techniques aimed at creating a well-defined return path. This structure makes it easier to analyze the reactive behavior of these nets. It is using the latter property that Huang *et al.* in "Loop-Based Interconnect Modeling and Optimization Approach for Multigigahertz Clock Network Design" propose a closed-form model for the loop resistance and inductance of global clocks.

The next three papers focus on analog-to-digital (A/D) converters. In "80-MHz Bandpass $\Delta\Sigma$ Modulators for Multimode Digital IF Receivers," Salo *et al.* present a bandpass Delta–Sigma modulator which works simultaneously as a downconverter and A/D converter. The two resonators of the modulator are implemented using a single operational amplifier, thus, reducing complexity and power dissipation. The selection of sampling frequencies and intermediate frequency (IF) results from a delicate balance between RF filtering, clock jitter, linearity, and other performance constraints. Next, Miller *et al.* in "A Multibit Sigma–Delta ADC for Multimode Receivers" propose a Sigma–Delta A/D converter with a high-resolution loop quantizer. The use of this type of quantizer is enabled by a dynamic element matching algorithm which minimizes any additional delay in the loop of the modulator. Finally, Uyttenhove *et al.* focus on techniques and tradeoffs employed in the design and validation of a state-of-the-art A/D converter in "Design Techniques and Implementation of an 8-bit 200-MS/s Interpolating/Averaging CMOS A/D Converter".

In the next paper, "An AI-Calibrated IF Filter: A Yield Enhancement Method with Area and Power Dissipation Reductions," Murakawa *et al.* show how to maximize yield while reducing the area of a Gm–C filter using a genetic algorithm. The technique has been demonstrated at a reasonable circuit complexity in the presence of significant technological variations.

TFT-LCD drivers are the focus of "A 402-Output TFT-LCD Driver IC With Power Control Based on the Number of Colors Selected," by Itakura *et al.*, who propose a technique to handle several color depths. The challenge is to allow several levels of power dissipation while tightly controlling phase and slew rate across a wide load range. The problem is solved by appropriate architectural decisions and proper buffer design.

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The final paper of the analog section deals with component design. In "Active-Feedback Frequency-Compensation Technique for Low-Power Multistage Amplifiers," Lee and Mok present a technique to decouple the constraints governing low- and high-frequency signal paths. The net effect is an improvement of slew rates while maintaining stability.

The next three papers focus on digital circuits and systems. The first, "A Reconfigurable System Featuring Dynamically Extensible Embedded Microprocessor, FPGA, and Customizable I/O," by Borgatti *et al.*, illustrates the applicability of embedded programmable logic in system design. The authors describe an image- and voice-processing integrated circuit which contains an SRAM-based embedded field-programmable gate array (FPGA). The embedded FPGA can be used to implement application-specific coprocessors and flexible I/O peripherals. The integrated circuit also contains a 32-bit extensible processor.

In the next paper, "A Single-Chip MPEG-2 Codec Based on Customizable Media Embedded Microprocessor," Ishiwata *et al.* describe an MPEG-2 MP@ML coder/decoder integrated circuit. The novel feature of this circuit is that it was designed using six microprocessors with the same instruction set, but different customization. The authors describe how this design methodology simplifies the design of large systems, yet provides excellent performance.

In the final paper of this section, "A Current-Based Reference-Generation Scheme for 1T-1C Ferroelectric Random-Access Memories," Siu *et al.* describe a novel structure for use in ferroelectric memories. Traditionally, ferroelectric memory cells require two transistors and two capacitors. By using a novel current-based reference circuit, however, smaller single-transistor single-capacitor memory cells can be employed.

This Special Issue concludes with five brief papers. The first two of these papers focus on communications. An interesting passive component suitable for large image-rejection applications is proposed by Frye *et al.* in "A 2-GHz Quadrature Hybrid Implemented in CMOS Technology." A coupled inductor pair and capacitor network replace resonant quarter-wavelength transmission-line elements to implement an integrated quadrature hybrid. Measurements show 65-dB image rejection and 4.7-dB noise figure at 2 GHz. In the second brief, "A Direct-Conversion Receiver for the 3G WCDMA Standard," Gharpurey *et al.* propose a SiGe BiCMOS solution that can fully satisfy the stringent WCDMA requirements. The receiver integrated circuit comprises an LNA, mixers, a variable-gain amplifier block, channel-select filters, and a frequency synthesizer. External components are limited to matching elements and band-select filters. The chip draws 46 mA from a 2.8-V supply.

The third brief paper, "A 2-V 23-μA 5.3-ppm/°C Curvature-Compensated CMOS Bandgap Voltage Reference," by Leung *et al.*, proposes techniques for compensating the temperature curvature of bandgaps to higher orders without affecting power dissipation. The fourth paper, "An Architecture for a Configurable Mixed-Signal Device," by Mar *et al.*, describes an integrated circuit containing programmable analog, digital, and clocking circuits, as well as a flash memory and a microcontroller. Finally, "Design and Performance Testing of a 2.29-GB/s Rijndael Processor," by Verbauwhede *et al.*, describes the design and performance of an Advanced Encryption Standard (AES) compliant encryption chip that delivers a throughput of 2.29 GB/s while consuming 56 mW of power in a 0.18-μm CMOS process. This integrated circuit implements the complete Rijndael algorithm, of which the AES standard is a subset.

We would like to thank the authors for their work in submitting and revising manuscripts; it has been gratifying to learn more about the advances first described at the CICC 2002. We also wish to express our deepest gratitude for the efforts of the reviewers. This Special Issue is only possible with their expert help.

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Dr. Wilton won the Douglas Colton Medal for Research Excellence for his research into FPGA memory architectures in 1998. In 2001, he received the Best Paper Award for a publication at the International Conference on Field-Programmable Logic. He is a Member of the Program Committee for the 2000–2003 IEEE Custom Integrated Circuits Conference and served as Chair of the Programmable-Logic Subcommittee for that conference in 2001 and 2002.