Introduction to the Special Issue on the IEEE 2003 Custom Integrated Circuits Conference

THIS Special Issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS is a selection of papers published in the 2003 IEEE Custom Integrated Circuits Conference. The papers of this selection reflect a continuing trend toward higher performance, lower cost, and further miniaturization. The 20 full papers are grouped into device modeling and radio-frequency papers, mixed-signal papers, and digital papers. Three brief papers conclude the issue.

The first two papers focus on MOSFET modeling techniques. In the first paper, entitled "SP: An Advanced Surface-Potential-Based Compact MOSFET Model," Gildenblat *et al.* describe the latest advances in surface-potential modeling techniques. The focus of this work is the relation between device physics and circuit simulation in the framework of a practical modeling environment. In the second paper, entitled "High-Frequency Characterization and Modeling of Distortion Behavior of MOSFETs for RF IC Design," Lee and Cheng's HF distortion characterization work indicates that the "low frequency limit" of a MOSFET is much higher than that of a comparable BJT, a useful observation for dealing with distortion behavior in RF IC design.

The next four papers discuss oscillators and quadrature local oscillator generation for a number of applications. In the first paper, "A Study of Injection Locking and Pulling in Oscillators," Razavi studies how the injection of periodic signals into an oscillator may result in locking and pulling phenomena. In the second paper, "Analysis and Design of Injection Locked LC Dividers for Quadrature Generation," Mazzanti *et al.* describe analytical expressions for locking range, quadrature accuracy, and phase noise for a class of divider topologies. In the third paper, entitled "A Subharmonically-Injected LC Delay Line Oscillator for 17-GHz Quadrature LO Generation," Ma and Long propose a delay line oscillator for simultaneous frequency multiplication and quadrature signal generation. The fourth paper by Temporiti *et al.*, entitled "A 700-kHz Bandwidth $\Sigma\Delta$ Fractional Synthesizer with Spurs Compensation and Linearization Techniques for WCDMA Applications," proposes a 2.1-GHz frequency synthesizer with 35-Hz resolution obtained thanks to a very large PLL bandwidth.

The next paper, entitled "A 4–91-GHz Traveling-Wave Amplifier in a Standard 0.12-μm SOI CMOS Microprocessor Technology," by Plouchart *et al.*, demonstrates a very high-bandwidth design implemented as a seven- and five-stage traveling-wave amplifier. The amplifiers operate at low voltage and exhibit a relatively low noise figure throughout the bandwidth.

The next two papers deal with data conversion. "Radio Frequency Digital-to-Analog Converter," by Luschas *et al.*, describes an RF narrow-band sigma-delta DAC designed to demonstrate a different DAC architecture where the DAC output is controlled by an oscillating waveform. The goal is to mitigate the troublesome switching distortion and clock jitter effects in high-speed DACs. In the next paper, entitled "A 1.8-V 67-mW 10-bit 100-MS/s Pipelined ADC Using Time-Shifted CDS Technique," Li and Moon discuss design of a pipelined ADC using a time-shifted correlated double sampling technique to reduce finite opamp gain error in order to achieve balanced performance for speed, power, and accuracy.

The next two papers focus on imager and display circuit design. In the first paper, "Amorphous Silicon Thin Film Transistor Circuit Integration for Organic LED Displays on Glass and Plastic," by Nathan *et al.*, the authors present a design of TFT drive circuits for active matrix organic light-emitting diode (OLED) displays, where the OLED layer was directly integrated on top of the TFT drive circuits. Next, Acosta-Serafini *et al.* propose a high dynamic range VGA sensor in the paper entitled "A 13″ VGA Linear Wide Dynamic Range CMOS Image Sensor Implementing a Predictive Multiple Sampling Algorithm With Overlapping Integration Intervals." The sensor's operation is based on a variable integration capacitance at the pixel level in combination with a feedback mechanism to extend saturation intensity levels.

The next paper, entitled "Statistical Leakage Current Reduction in High Leakage Environments using Locality of Block Activation in Time Domain," by Choi *et al.*, describes a new leakage current reduction methodology for realizing statistical leakage current reduction using a time locality of activation probability of a circuit block.

The next eight papers discuss digital design issues, in particular low power, content addressable memory (CAM), video compression, and SOI technology. The first two papers deal with low power reduction techniques in flip-flops and CAMs. "Standby Power Reduction Using Dynamic Voltage Scaling and Canary Flip-Flop Structures," by Calhoun and Chandrakasan, analyzes various flip-flop structures and proposes a closed-loop approach using canary flip-flops. Measurements reveal that this approach improves power by 40$\times$ in a 0.13-μm dual-V_T test chip, which in turn is 2$\times$ better than the open-loop approach. The next paper describes a novel pipelined scheme to reduce power consumption in "A Low-Power Content Addressable Memory (CAM) Using Pipelined Hierarchical Search Scheme," by Pagiamtzis and Sheikoleslami.

The third and fourth papers address issues related to clock/signal distribution. "Resonant Clocking Using Distributed Parasitic Capacitance," by Drake *et al.*, suggests ways of accelerating clock trees with local clock regeneration schemes. Drost *et al.* report results from wireless chip-to-chip communication experiments in their paper entitled "Proximity Communication."

Next, Hazucha *et al.* demonstrate a 10$\times$ improved reliability in SER tolerant latches in a test chip containing both standard

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and SER tolerant latches in the paper entitled "Measurements and Analysis of SER Tolerant Latch in 90-nm Dual-V_t CMOS Process." Garrett *et al.* present an architecture for 4×4 16QAM MIMO spherical decoder that achieves 38.8 Mb/s over a 5-MHz channel using only approximately 10 mm^2 in a 0.18-μm CMOS process in the paper "Silicon Complexity for Maximum Likelihood MIMO Detection Using Spherical Decoding."

The seventh paper, by Farjad-Rad *et al.*, entitled "A 33-mW 8-Gb/s CMOS Clock Multiplier and CDR for Highly Integrated I/Os," describes a compact non-LC low-power low-jitter 8-Gb/s CDR circuit using injection-locking for jitter suppression and phase interpolation in high-bandwidth SOC solutions. A mobile terminal for personal visual communication is gaining popularity and to realize an ultra-low-power and high-quality real-time MPEG4 video codec in the terminal, a highly efficient motion estimation process is essential. The next paper, by Miyama *et al.*, entitled "A Sub-mW MPEG-4 Motion Estimation Processor Core for Mobile Video Application," features a gradient search algorithm that reduces computational complexity to 15 MOPs.

This Special Issue concludes with three brief papers. "Analysis and Modeling of Bang-Bang Clock and Data Recovery Circuits," by Lee *et al.*, proposes a large-signal model for the characterization of jitter in bang-bang phase detectors. Partially depleted SOI (PD SOI) circuits possess inherent BJT leakage affecting the functionality of the circuit. Nanua and Blaauw address the PD SOI noise issues in a paper entitled "Noise Analysis Methodology for Partially Depleted SOI Circuits" and present a noise model to account for the floating body and the BJT effects. The final paper, by Prokop *et al.*, "An Eight-User UMTS Channel Unit Processor for 3GPP Base Station Applications," describes a multiuser W-CDMA baseband channel unit processor for cellular base-station applications that exceeds 3GPP performance requirements.

We would like to extend our thanks to the authors for their work in submitting and revising their manuscripts. Learning about novel work and advances of the art has been highly gratifying. We also wish to express our deepest gratitude to our reviewers for their efforts and dedication. This Special Issue would not have been possible without their expert advice.

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