

6.7. A CMOS Single Photon Avalanche Diode Array for 3D Imaging

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Time-of-flight (TOF) measurements using pulsed light beams for 3D imaging or profiling require either a costly mechanical device to scan the scene [1] or a short and highly energetic optical pulse to flood the scene with photons [2]. An alternative to these methods is the use of detector arrays based on single photon avalanche diodes (SPADs) operating in Geiger mode [3]. These devices accurately detect the arrival of a single photon and are therefore effective in computing TOF of extremely small bursts of optical power even when the source is uncollimated and diffused over a wide cone of light. Thus, SPAD arrays are indicated for 3D imaging of volumes of several cubic meters at sub-millimetric axial resolutions. This approach becomes attractive with the recent integration of SPAD arrays in standard CMOS technology [3].

In this paper, a system for fast and accurate evaluation of TOF with an 8x4 pixel array fabricated in 0.8 μ m CMOS technology is presented. The array is scalable and can be massively expanded without architectural changes. The sensor is also usable in a 2D mode with significant performance advantages over conventional CMOS imagers in terms of sensitivity and dynamic range.

Figure 6.7.1 shows the cross-section of the SPAD [3] and the read-out circuitry. The p+/n-well junction, where avalanche takes place, is surrounded by a guard ring designed to prevent edge breakdown. The pixel, whose layout is shown in the inset of Figure 6.7.2 consists of a circular SPAD, a quenching resistor R_{poly} in series between the cathode of the diode and VDD, and a comparator that transforms the Geiger voltage pulse at node A into a digital signal. V_{op} is used to bias the anode at -18.5V while VDD powers the remainder of the circuit. The breakdown voltage V_{bd} of the SPAD is 21V; thus the diode is biased with an excess voltage above breakdown V_e = |V_{op}| + VDD - V_{bd} = 2.5V. The comparator is implemented as a simple inverter with a threshold voltage of 3V.

When a photon reaches the avalanche region, a Geiger pulse is generated. The avalanche current discharges the parasitic capacitance at node A (Fig. 6.7.1), causing a voltage drop across R_{poly} from VDD to VDD - V_e, sufficient to switch the inverter and to stop the avalanche. The process of quenching the avalanche and recharging the parasitic capacitance at node A, thus switching the inverter to its original state, requires approximately 32ns. This time constant, known as dead time, determines the lowest possible time interval between detectable photons. The SPAD has a quantum efficiency η of about 10% at 635nm and is free of after-pulses. It exhibits a dark count rate (DCR) of about 50Hz and a time jitter of 50ps. Figure 6.7.3 shows the architecture of the 3D sensor. Since the output of a pixel is digital, the column readout circuitry requires no amplification, no analog processing, no sample-and-hold, and no A/D conversion before being routed outside the chip. The power dissipation of the sensor is less than 1mW.

The SPAD array is used in the electro-optical setup shown in Fig. 6.7.4. The distance between two points is computed by measuring the TOF τ of a light beam from source to target. A 635nm laser source, pulsed at repetition rate f_r = 50MHz with pulse width T_p =

100ps and peak power P_s = 40mW, is directed towards the target. The light beam was intentionally uncollimated to create a cone of diffused radiation that covers the entire scene. The detector array is placed behind a standard camera objective. A time histogram is captured for every SPAD independently but in a sequential manner due to the discrete setup.

Distance d is computed as d = ct/2, where c is the speed of light. In order to achieve a resolution R over distance d, one must resolve a TOF increment $\Delta\tau = 2R/c$. Note that $\Delta\tau$ must be equal or comparable to the time measurement uncertainty $\sigma(\tau)$ for the measurement to be meaningful. This setup shows an uncertainty of 268ps, mainly limited by the jitter of the external components. Therefore, to obtain sub-picosecond resolution, it is necessary to average over M measurements. The resolution scales with M^{-1/2}.

In the plot of Fig. 6.7.5 a histogram h_i(t) (centered around zero) is shown after M=10⁴ measurements. Due to the various skews introduced by the layout of the array and external discrete components, it is advantageous to compute two histograms for every pixel. The first h_i'(t) relates to the scene of interest, the second h_i'(t) to a reference, i.e., a background panel. Note that the reference image needs to be taken only once and is subsequently stored electronically. Instead of computing an absolute time, a TOF difference is evaluated. This procedure is accomplished by numerically computing the centroid of the cross-correlation function between h_i'(t) and h_i'(t). This method numerically simulates the presence of an optical copy of the source beam; consequently, a complex setup to generate such copy [1] is avoided.

The range finding performance of the 3D CMOS sensor is tested with M=10⁴. From the histograms, $\sigma(\tau)$ causes a theoretical uncertainty $\sigma(d) = 402\mu$ m. Fig. 6.7.5 shows a plot of measured vs. actual distance computed over a range of 15cm around 1m. The standard deviation was 618 μ m throughout the range. The probable cause of the mismatch in error is the finite time resolution of the counter, which results in histogram quantization noise. In Fig. 6.7.6 and Figure 6.7.7, two 3D images are extracted using the proposed algorithm. A sub-millimetric axial accuracy is obtained at a distance of 1m.

Future developments include the integration of a time-to-voltage converter or a fast counter per pixel, further miniaturization of the pixel, and a massive expansion of the array. Much higher lateral resolution and an optimized frame rate are expected. Based on the measured DCR, η , and dead time, a dynamic range of 88dB is estimated for 20ms integration time. This performance, coupled with the elimination of analog processing and A/D conversion, makes CMOS SPADs very attractive for ultra low power highly sensitive 2D sensors.

Acknowledgements:

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References:

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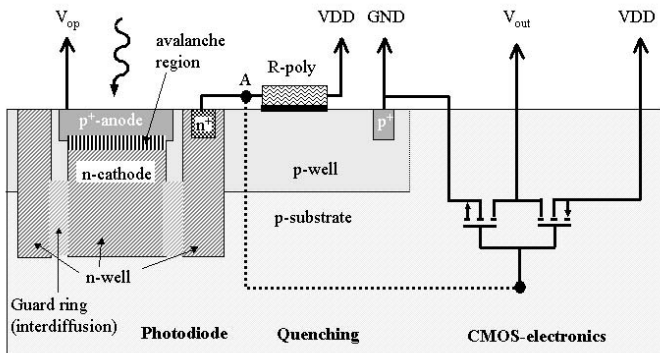


Figure 6.7.1: Pixel cross-section. The guard ring is obtained by interdiffusion of two n-wells with no changes to the CMOS fabrication process.

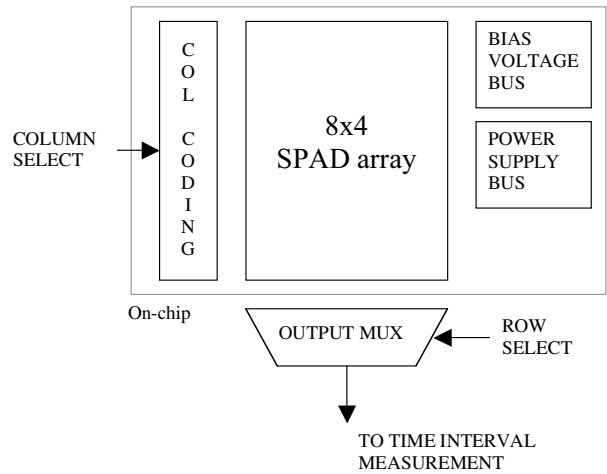


Figure 6.7.3: 3D Sensor architecture, including classic row and column selection circuits identical to conventional CMOS imagers.

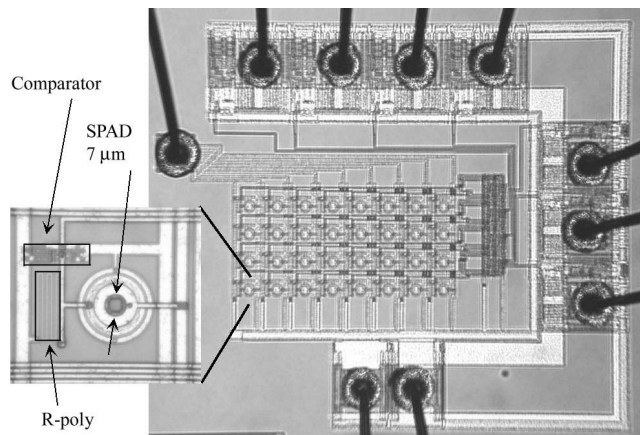


Figure 6.7.2: Chip photomicrograph with pixel inset.

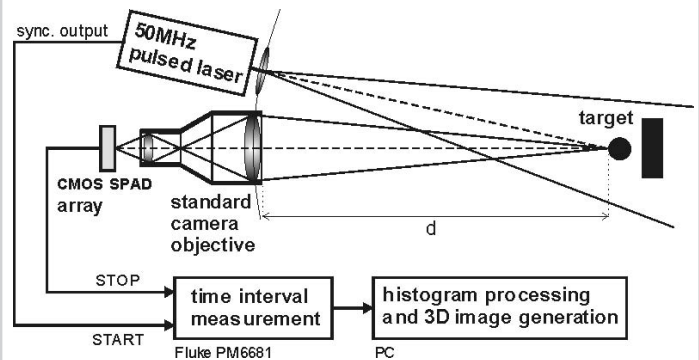


Figure 6.7.4: Camera set-up. The time elapsed between laser trigger (START) and SPAD response (STOP) is measured with a time resolution of 50ps and a jitter less than 150ps.

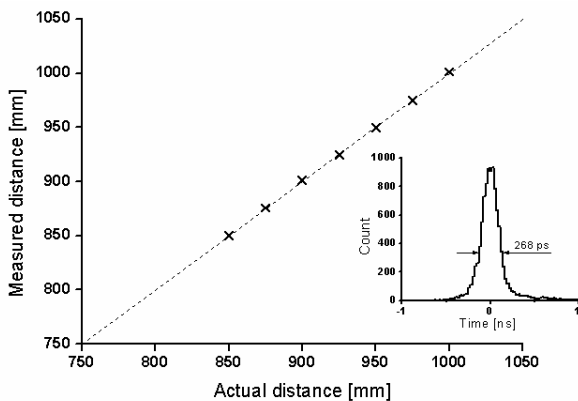


Figure 6.7.5: Plot of measured distance vs. actual distance. Inset: time arrival histogram centered around zero.

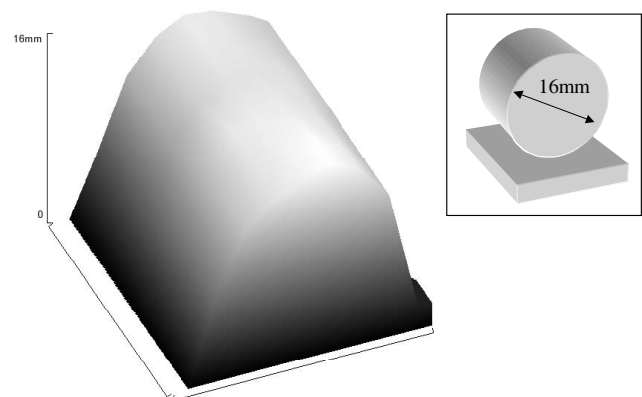


Figure 6.7.6: 3D surface of a cylinder.

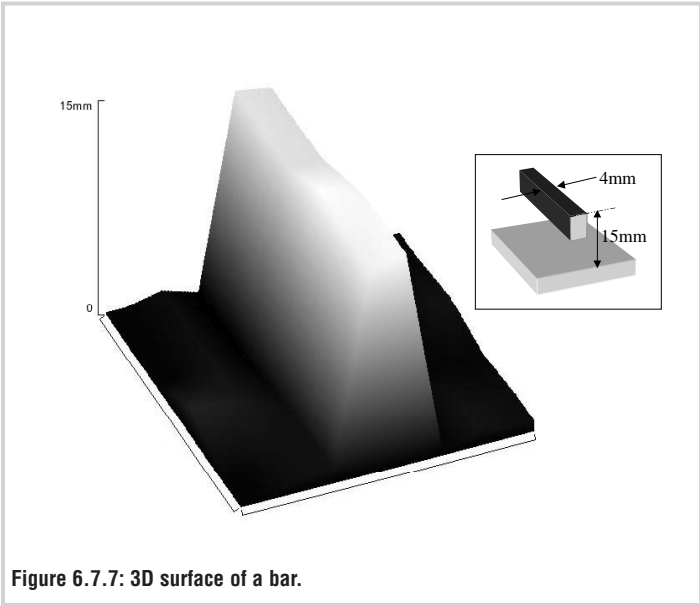


Figure 6.7.7: 3D surface of a bar.

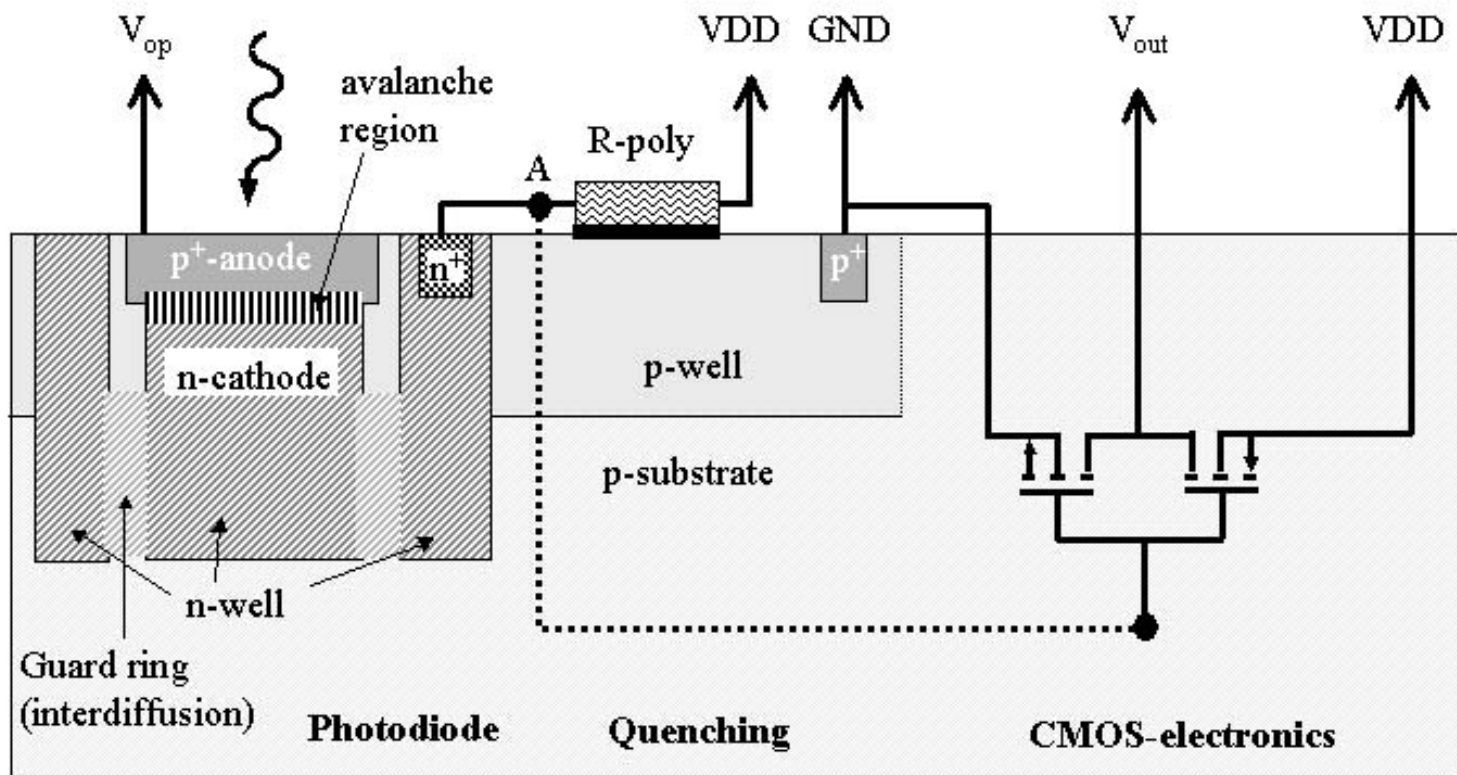


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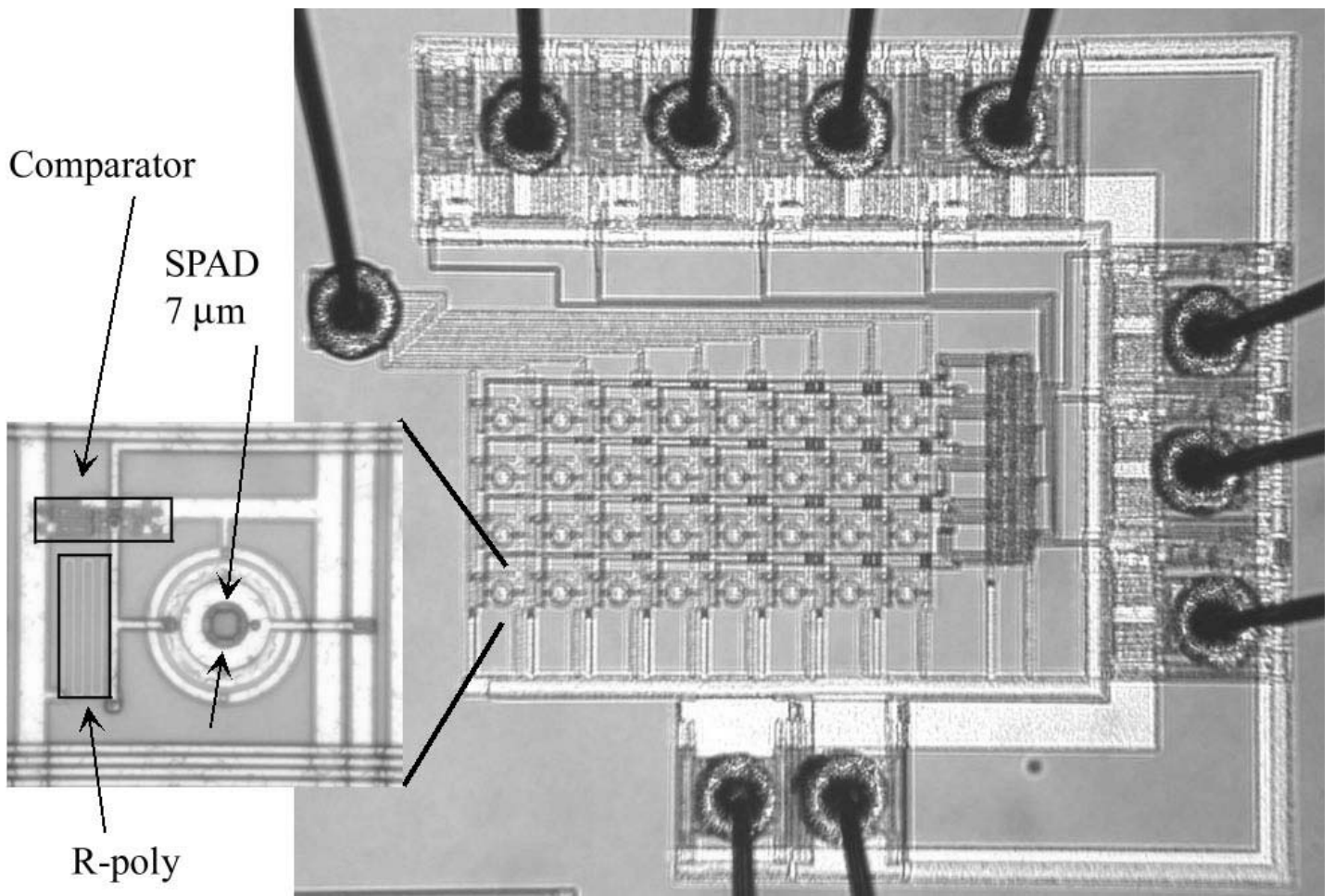


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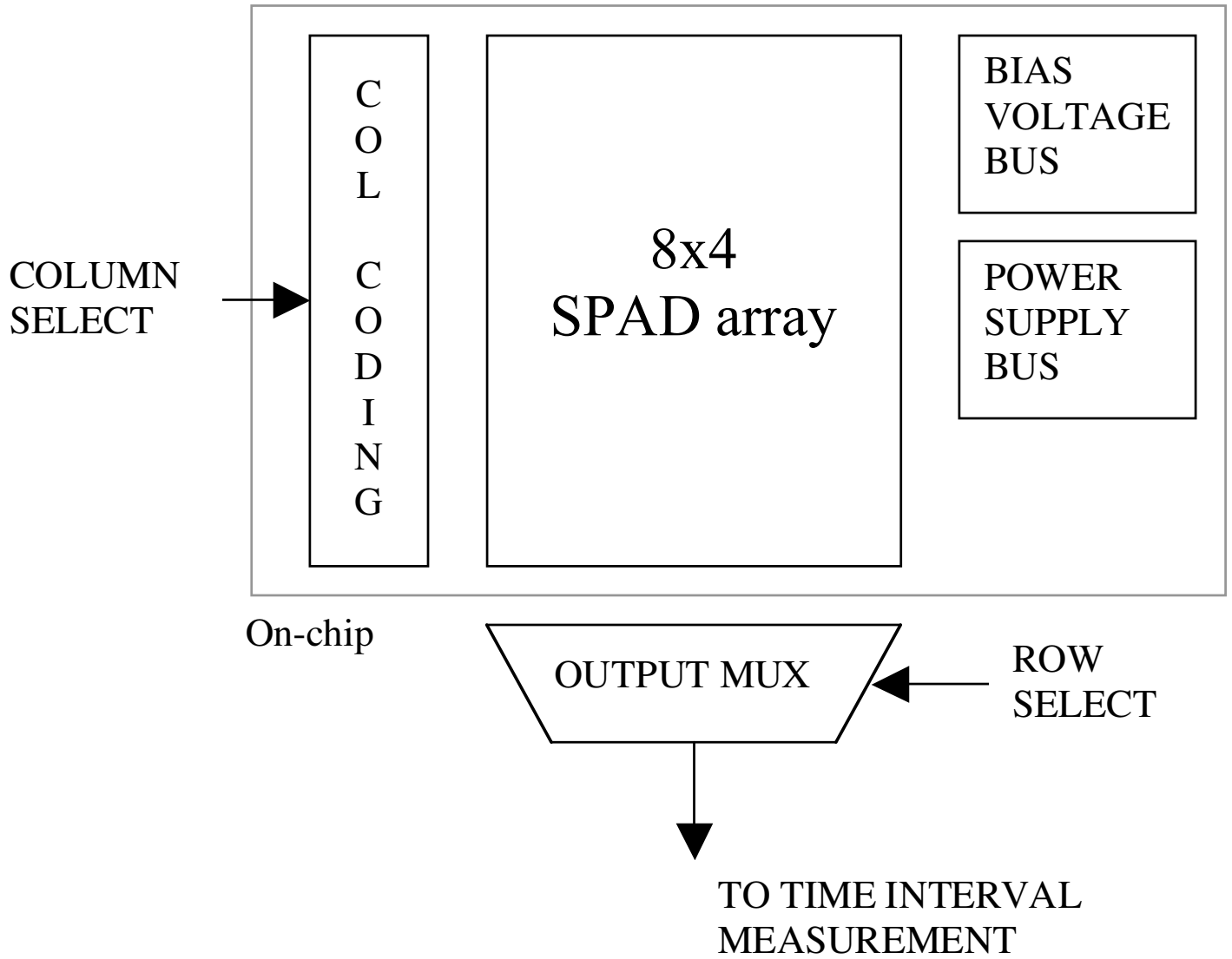


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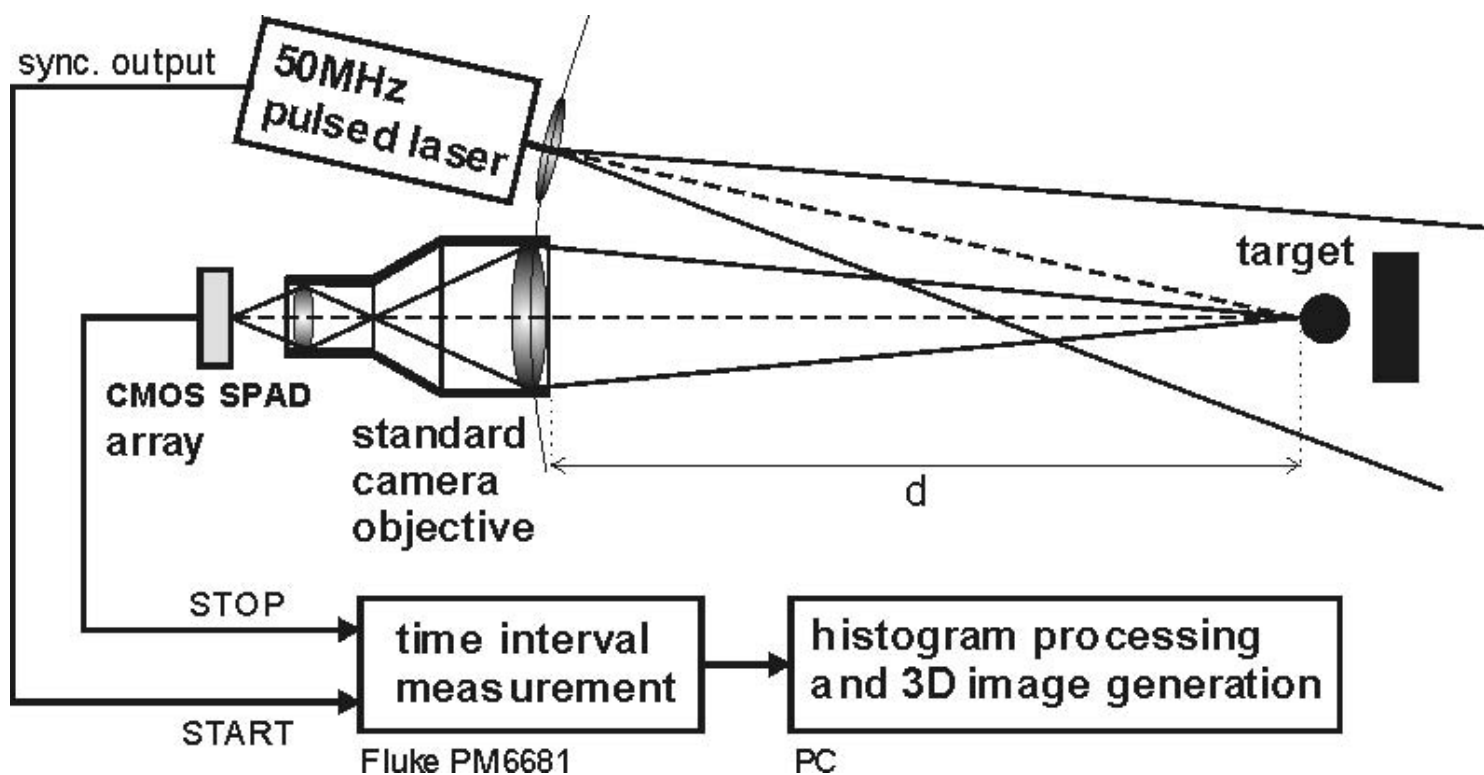


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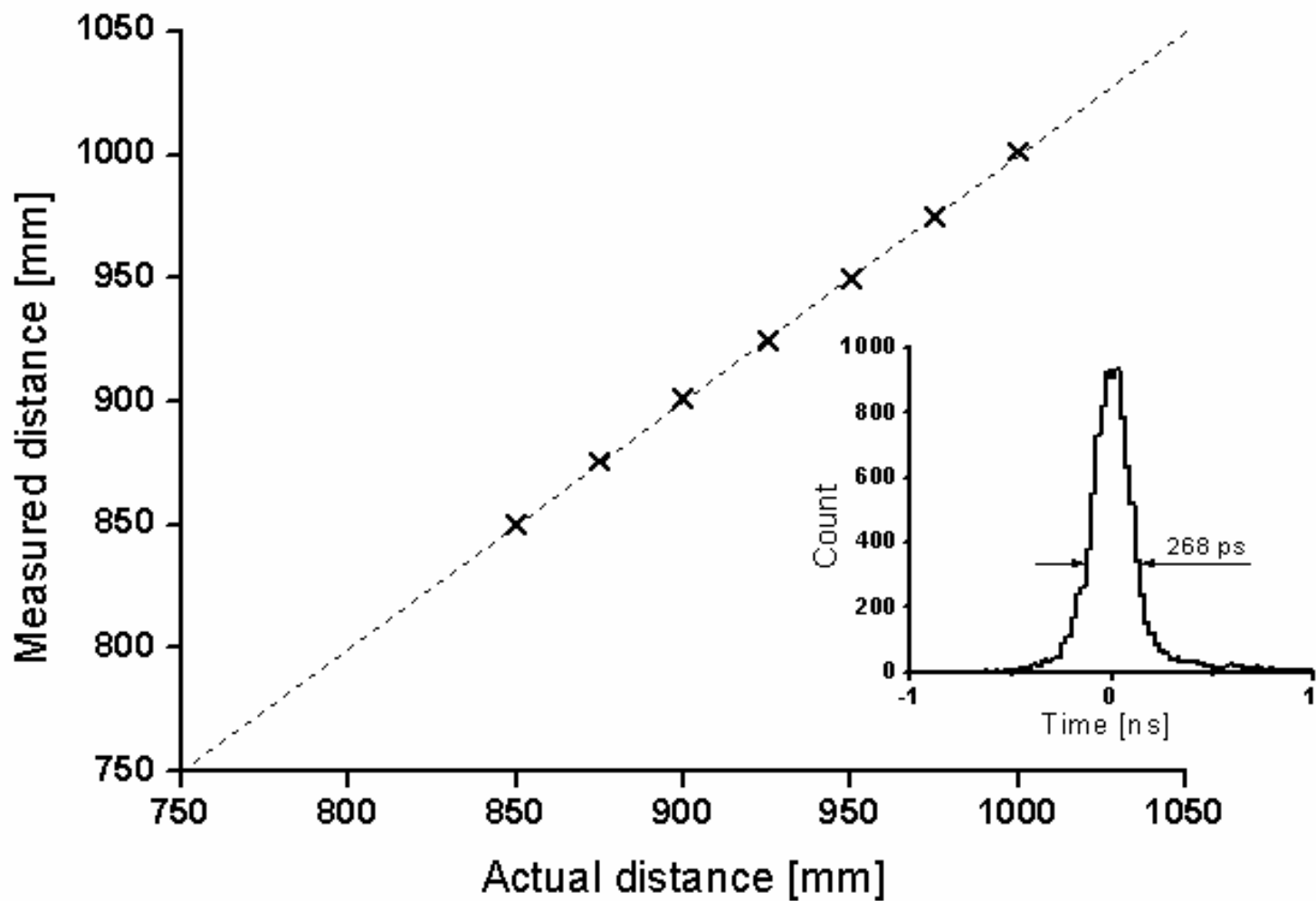


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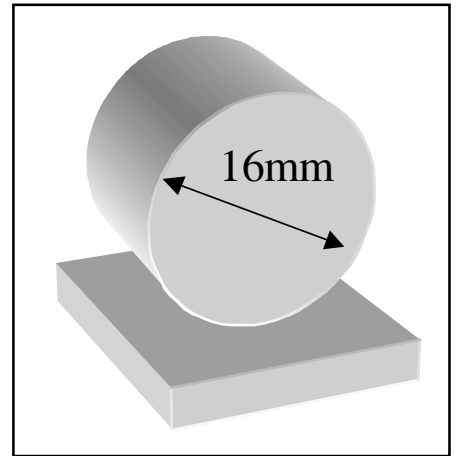
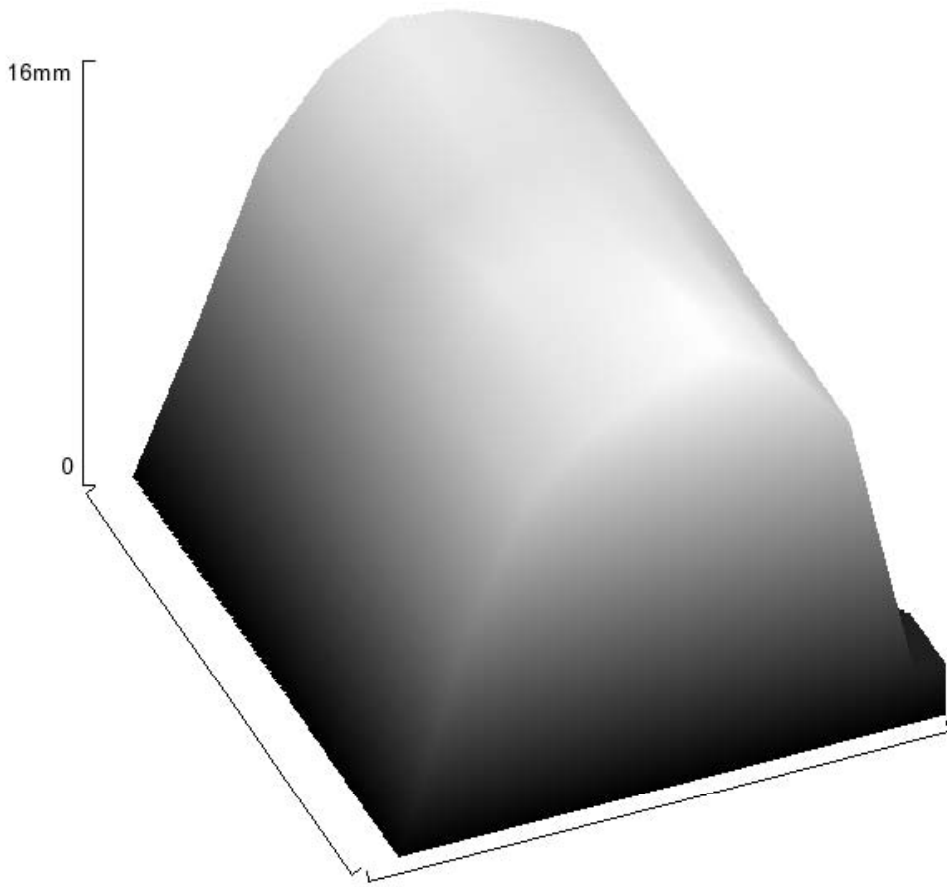


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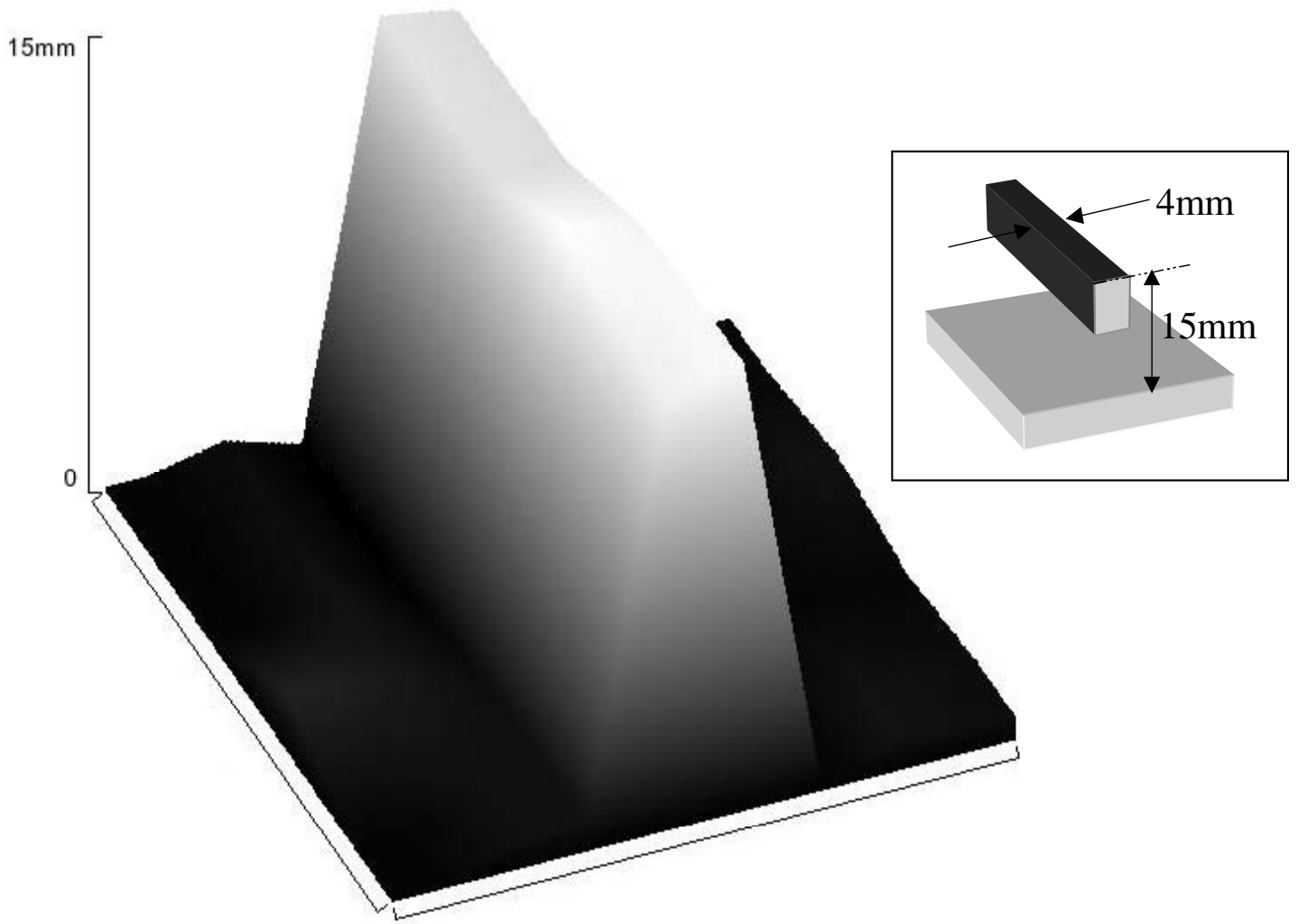


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