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Characterization of an integrated force sensor based on a MOS transistor for applications in scanning force microscopy

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Abstract

In this article an integrated force sensor based on a stress-sensing MOS transistor is introduced for applications in scanning force microscopy (SFM). The sensor configuration will be described, and theoretical and experimental investigations of the sensitivity will be presented. With the fabrication process, consisting of a standard CMOS process and post-processing (conventional silicon bulk micromachining), cantilevers with MOS transistors integrated at the base for deflection detection have been fabricated. The cantilevers typically have a spring constant of 1 N m^{-1}, are 400 to 950 μm in length and have a mechanical resonance frequency between 6.2 and 35 kHz. It is found that the stress sensitivity of the MOS transistor changes with the gate voltage, while being independent of the drain voltage. The cantilevers have successfully been used for SFM imaging in both contact mode and dynamic mode (tapping mode). These cantilevers together with integrated circuits are expected to be well suited for mass production because of their CMOS processing compatibility. © 1998 Elsevier Science S.A.

Keywords: Scanning force microscopy; Cantilevers; Force sensors; MOS transistors

1. Introduction

Modern force sensors for scanning force microscopy (SFM) are Si_3N_4 cantilevers, which are fabricated by a replica technique, SiO_2 or Si beams with tips prepared by anisotropic wet chemical or reactive ion etching. These levers are either brought into close proximity to the surface and, hence, bend slightly (contact mode), or they are approached to the surface while vibrating at their resonance frequency. The force gradient at the surface influences the resonance frequency, which is then sensed (dynamic mode or tapping mode). The mechanical requirements on the force sensors are a high resonance frequency (> 10 kHz) and a low spring constant (0.1–10 N m^{-1}). The deflection amplitude or vibration frequency of the lever is sensed either with an integrated stress sensor or by external means. Integrated force sensors are preferred for applications in ultra-high vacuum, or other special environments where direct access is hindered. They will also be needed for future instruments which will have several probes running in parallel. Piezoresistive [1,2] and piezoelectric [3–5] stress sensors are most commonly used at present.

We report on the implementation of a force sensor that is based on a MOS transistor. If its channel is subjected to stress, the carrier mobility changes, resulting in a changing source–drain current [6–9]. Similar to a piezoresistor, the MOS transistor is very compact and, hence, can easily be incorporated in the area of highest stress. In general, the piezoresistive coefficients of MOS transistors are as high as those of diffused piezoresistors [6–9] and one can expect the stress sensitivity to be the same as that of piezoresistors. However, since the channel of a MOS transistor is right at the surface and is very shallow, the sensitivity is expected to be improved in our application. Any transistor in a MOS integrated circuit can, basically, be applied as a stress sensor. Therefore, fabricating the force sensor can be a combination of a conventional CMOS process, which can be ordered at an external foundry without any extra steps (for example, implantation only for making piezoresistors), and post-processing for making the cantilevers. This is very attractive because not only sensors but also reliable amplifiers and signal processors can be fabricated on the same wafer.

A macro model of the MOS-type force sensor has been demonstrated by two of us [10]. In this article we shall

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describe the fabrication and testing of the integrated force sensor based on a MOS transistor. After a brief introduction into the theory of the sensor, the design concept and the fabrication of the sensor will be described. The sensor will be characterized by displacement sensitivity measurements. SFM images recorded with the force sensor are then introduced to show the performance of the force sensor.

2. Displacement sensitivity of the sensor

Fig. 1 depicts schematic drawings of our force sensor. A p-MOS transistor is designed at the base of the silicon cantilever. The cantilever is aligned with the ⟨110⟩ silicon crystal orientation of a (100) silicon wafer. The MOS transistor is positioned such that the direction of source–drain current flow is parallel to the cantilever, as shown in Fig. 1(a). In this case, we can take the longitudinal piezoresistive coefficient of the p-type inversion layer, which is higher than the transverse one. An applied force deflects the cantilever and the resulting stress in the material induces a change in the source–drain current I of the MOS transistor. The channel length of the transistor is short compared to the cantilever length and the channel width is designed to be as long as possible. The stress applied to the channel layer depends on the displacement at the cantilever end. For a small displacement ΔZ the mechanical stress σ is

$$\sigma = \frac{3Et}{2l^2}\Delta Z\beta \tag{1}$$

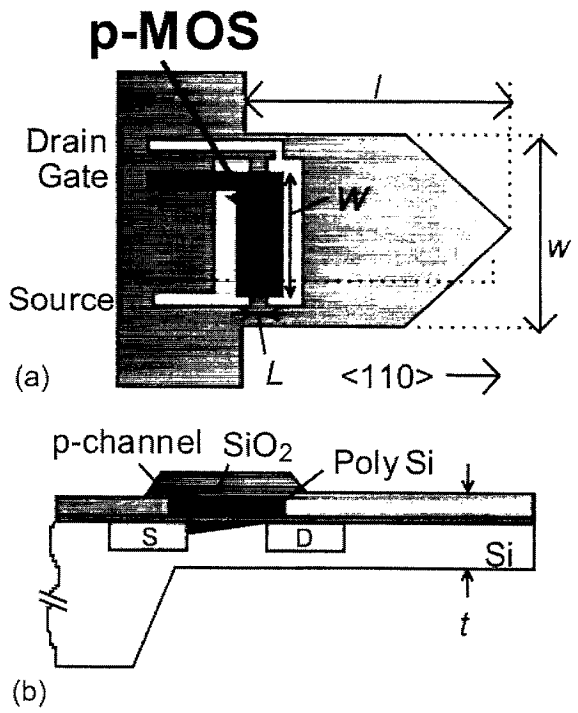

Fig. 1. Schematic of a p-MOS force sensor integrated in an SFM cantilever: top view (a) and cross-sectional view (b).

where E is Young's modulus of the beam material, l is the length of the cantilever, t is the thickness of the cantilever. The efficiency factor β is a number between 0 and 1, which takes into account that the channel layer (p-type inversion layer) is not at the surface of the cantilever (see Fig. 1(b)), where the stress is maximum. $\beta = 1$ when the channel layer is at the surface of the cantilever, and $\beta = 0$ when the channel layer is at the non-stressed centre plane in the cantilever. Since the thickness of the channel layer itself is small enough to be neglected, the value of β depends only on the thickness of the gate oxide, the gate polysilicon, the top oxide and the bulk silicon. For higher stress sensitivity, those layers on top of the silicon bulk should be as thin as possible.

The relative change in the source–drain current of a MOS transistor under stress is a function of the piezoresistive coefficient π of the p-inversion layer and the stress σ,

$$\frac{\Delta I}{I} = -\pi\sigma = -\pi\frac{3Et}{2l^2}\Delta Z\beta \tag{2}$$

In general, the piezoresistance coefficients of the MOS transistor depend on the gate voltage, the source–drain voltage and the temperature [6–9]. The longitudinal piezoresistive coefficient of a p-type inversion layer in the ⟨110⟩ direction of a (100) silicon wafer is $\pi = 6.8 \times 10^{-10}$ Pa^{-1} when the gate voltage is -5 V according to Ref. [9]. The values from other references [6–8] with the same gate voltage are within $\pm 10\%$ of this value.

3. Sensor design and fabrication

3.1. Design of the sensor

When designing a cantilever for SFM one goal is to achieve a specified spring constant, with the minimum detectable deflection being as small as possible. We designed four cantilevers with different dimensions, each having the same spring constant. The MOS transistors on the cantilevers have different channel widths and, therefore, different minimum detectable deflections can be expected. In Table 1, the dimensions of the cantilevers are summarized in addition to the size of the MOS transistors and the calculated $\Delta I/I$ per angstrom. For estimating the mechanical properties of the levers, it was assumed that the gate oxide, gate polysilicon and top oxide are thin enough to be neglected compared with the cantilever thickness. First, the spring constant k was determined to be $k = 1$ N m^{-1}. A low spring constant is preferred for our application. Next, the thickness of the cantilevers, which is a process parameter, was determined as $t = 4$ μm to account for our processing techniques. Finally, considering that the first resonance frequency should be higher than 10 kHz, the dimensions of the levers were determined. The first resonance frequency then turned out to be in the range 6.2 to 35.0 kHz. A channel length of 6 μm, which is short enough to be neglected compared with the shortest cantilever (400 μm), was chosen for the MOS transistors.

Table 1
Dimensions and mechanical properties of the SFM cantilevers with integrated p-MOS transistor

Cantilever (μm)	l	950	650	500	400
	w	316	102	46	24
	t	4	4	4	4
MOS (μm)	W	274	73	25	6
	L	6	6	6	6
Spring constant (N m^{-1})		1	1	1	1
Resonance frequency (Hz)		6.2k	13.3k	22.4k	35.0k
$\Delta I/I$ per 1 Å [a]		0.77e−7	1.64e−7	2.77e−7	4.33e−7

[a] Where $\pi = 6.8 \times 10^{-10}$ Pa^{-1}, $\beta = 1$.

3.2. Fabrication

4 inch n-type (100) 3–5 Ω cm silicon wafers were prepared for the device fabrication. Fig. 2 shows the schematic drawings of the process steps. The process was structured to making the electronics first and then microfabricating the cantilevers. 11 masks were used in total. The first part of the process was a standard LOCOS CMOS process with one exception: the polysilicon deposition for the gate followed the boron implantation for source and drain. This was necessary because on the same wafer there were some devices for another purpose which needed this unusual step. Gate oxide, gate polysilicon and top oxide are 800, 1200 and 3000 Å in thickness, respectively. The efficiency factor can, hence, be calculated to be $\beta = 0.85$. A thick LOCOS oxide layer was not grown on the area where cantilevers should be fabricated. The second part of the fabrication process followed the fabrication of the electronics (Fig. 2(a)). First, a part of the front surface is etched 7 μm deep by RIE while the electronics and the cantilevers are protected by resist (Fig. 2(b)). Next the silicon nitride on the wafer backside, which was already deposited during the LOCOS process, was patterned to act as a mask for KOH etching. By using a mechanical chuck the front surface was covered and the wafer was dipped into a KOH bath to form thin membranes (Fig. 2(c)). The membranes consisted of two parts with different thicknesses. The part where the cantilevers should be formed was 10 μm in thickness and the other part was 3 μm in thickness. The last step of the process was RIE etching of silicon from the backside. By this, cantilevers 4 μm in thickness were obtained (Fig. 2(d)). The back surface of the cantilever is smooth enough to reflect a laser light for external deflection detection. Fig. 3 depicts an optical microscope image of a chip showing four levers of different size. Note that the levers have not exactly the same size as those in Table 1 though they have the same configuration.

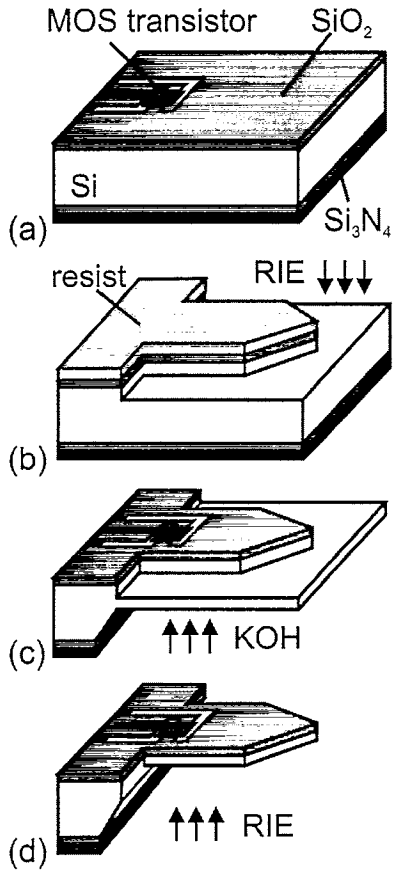

Fig. 2. Typical fabrication process of SFM cantilevers with integrated p-MOS transistor after the LOCOS CMOS was completed.

4. Characterization of the levers

In a first experiment the displacement sensitivity of the sensor was investigated. Fig. 4 shows a schematic drawing of the experimental set-up. A lever chip was mounted to a probe station in a shielded box. A small bimorph piezo-disk with a sharp needle was also mounted to a probe for deflecting the lever. Displacement of the needle had been previously calibrated by a confocal microscope. The needle was then brought into contact with the lever end, and a small deflection was induced to the lever. For the experiment, a sinusoidal wave with an amplitude of 1 μm peak-to-peak at 1 Hz was applied. While the lever was slowly vibrated in this manner, the source–drain current of the MOS transistor under various conditions was measured by a semiconductor parameter analyser (HP 4155A). From the amplitude of the sinusoidal signal superimposed on the large d.c. offset of the source–drain current, we evaluated $\Delta I/I$ per 1 μm for each lever.

First we investigated the relationships between $\Delta I/I$ and the gate voltage. The drain voltage was fixed at −0.5, −5

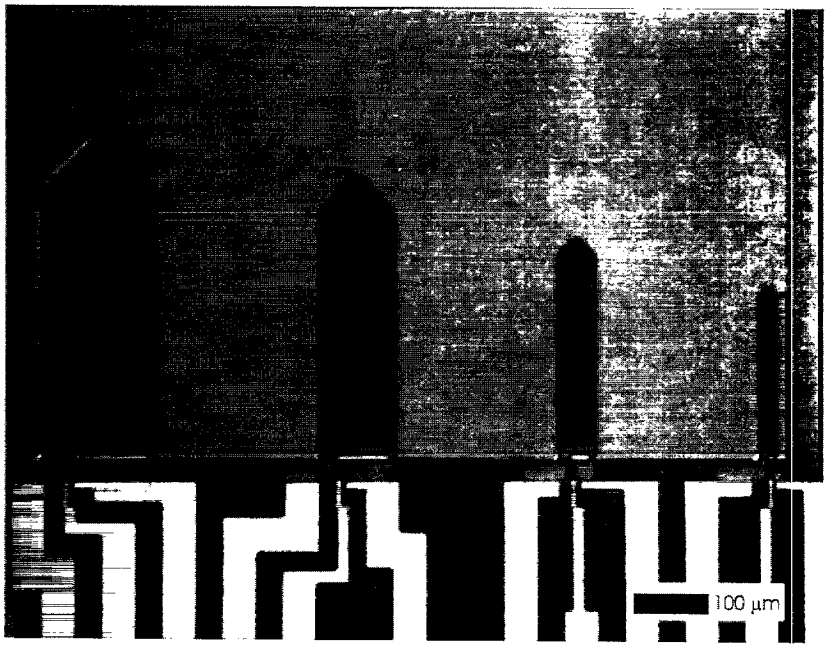

Fig. 3. Optical microscopy image of four SFM cantilevers with integrated p-MOS transistor at the base.

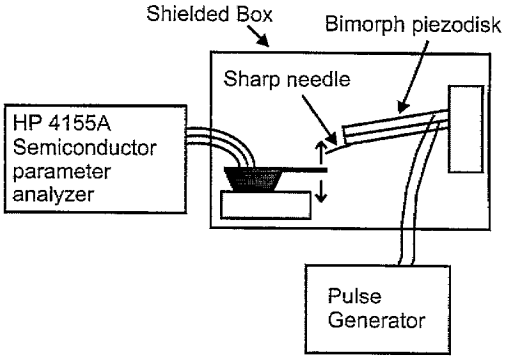

Fig. 4. Schematic of the experimental set-up for sensitivity measurement.

and -10 V while the gate voltage was varied from -1.5 to -10 V. These measurements were done for each MOS transistor having different channel widths. Fig. 5 shows a typical relationship between $\Delta I/I$ and gate voltage, and the current change as a function of gate voltage. From these curves it is obvious that the stress sensitivity is increasing with the gate voltage approaching a threshold voltage ($=-1.5$ V), where the source–drain current becomes very low. Especially for a gate voltage lower than -3 V, the increase of the stress sensitivity is very pronounced. This can be attributed to a change of the MOS transistor piezoresistance in the weak inversion regime, which is explained due to the stress-induced band-gap narrowing effect resulting in an increasing contribution of minority carriers [8,9]. This piezoresistance change can be associated with a change in the conductivity type [8,9]. The relationship between $\Delta I/I$ and the gate voltage in Fig. 5 is quite similar to the one in Ref. [9] if we take the opposite sign into account, where the experimental results are in good agreement with the simulation.

On the other hand, $\Delta I/I$ was almost independent of the drain voltage. Fig. 6 shows $\Delta I/I$ as a function of drain voltage. With a gate voltage fixed at -5 V, the drain voltage was varied from -0.5 to -7 V, where the MOS transistor was driven from the non-saturation region to the saturation region.

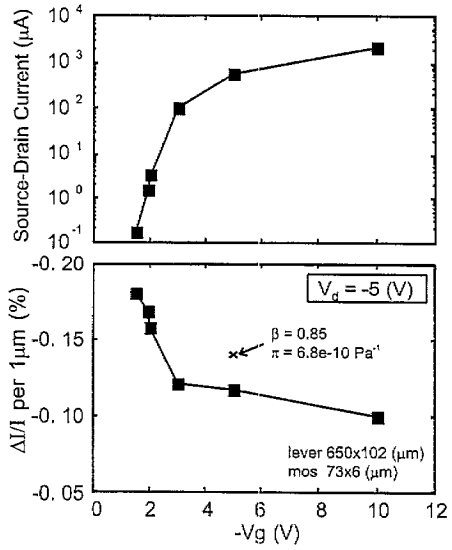

Fig. 5. Upper graph shows source–drain current vs. gate voltage. Lower graph shows $\Delta I/I$ per 1 μm vs. gate voltage.

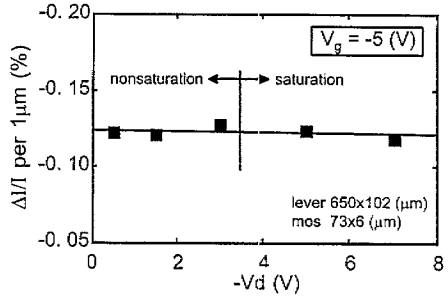

Fig. 6. $\Delta I/I$ per 1 μm vs. drain voltage.

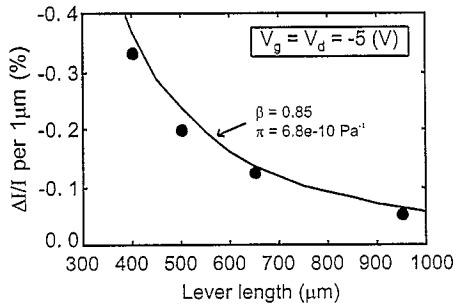

Fig. 7. $\Delta I/I$ per 1 μm vs. SFM cantilever length. The dots show the results obtained from the four levers. The solid line shows a calculation.

Although we performed the same measurement with different gate voltages (-0.5 and -10 V), $\Delta I/I$ was always independent of drain voltage.

In order to compare the stress sensitivity between the MOS transistors with different channel widths, we fixed both gate voltage and drain voltage at -5 V and measured $\Delta I/I$ of each transistor. If there is no difference between the MOS transistors in terms of the stress sensitivity, $\Delta I/I$ from each transistor should be proportional to the inverse of l^2 according to Eq. (2). Fig. 7 depicts a result of the measurement. The solid line shows a calculation obtained from Eq. (2) using $\beta = 0.85$, $E = 169$ GPa, $\pi = 6.8 \times 10^{-10}$ Pa^{-1} and $t = 4$ μm. The results of measurement are 10–20% lower than the calculation. Even if we consider a different piezoresistive coefficient that is within ± 10% of the value described above, the measured results are slightly lower than the calculation. This could be attributed to the fact that the lever end on the front surface does not align to the line formed by the KOH-etched (111) plane and the lever back surface. The base of the lever is hanging over by a few micrometres from the line and therefore the stress applied to the MOS transistor is smaller than the calculation.

It should be particularly noted that the power dissipations of the various MOS transistors are quite different at the same bias voltage because of the different channel widths. The biggest MOS transistor on the longest lever dissipated 11 mW when both gate and drain voltage were -5 V, while the power in the smallest one was only 0.23 mW. These values are drastically reduced with decreasing gate voltage under a constant drain voltage, where the sensitivity is much improved (see Fig. 5).

5. Imaging of sample with the levers

Imaging of various test structures was performed with the levers. We incorporated the levers in a conventional SFM (Nanoscope III). The current signal of the MOS transistor was converted to a voltage with a resistor and measured. Fig. 8(a) and (b) depicts SFM images of an Si grating recorded with one of the levers in contact and dynamic mode (tapping mode), respectively. The pit sizes are 5 μm × 5 μm and the depth is 180 nm. The edge of the lever was used as a probing 'tip'. We attribute the bluriness of the image of the

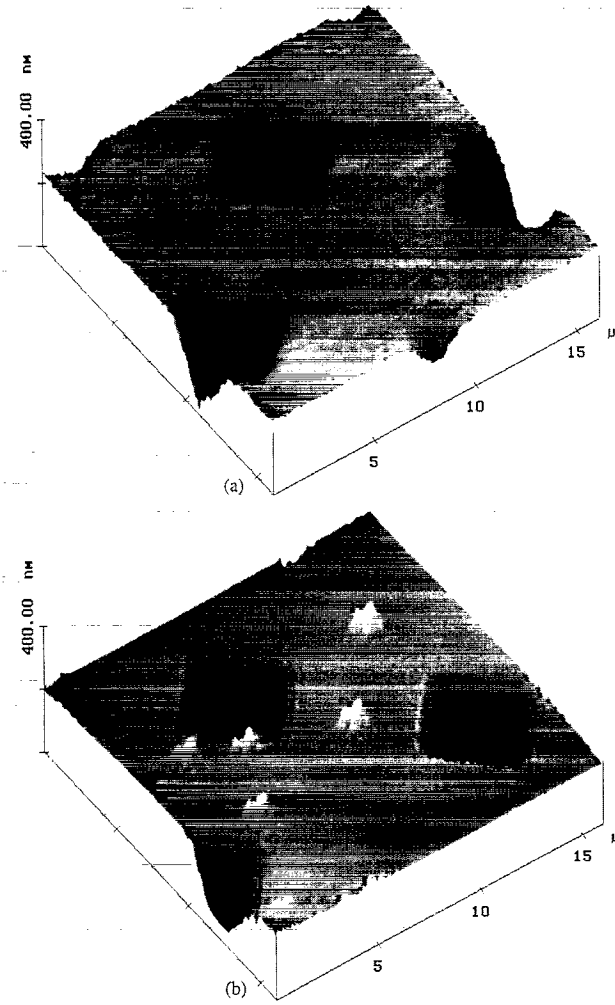

Fig. 8. SFM images of Si grating of 5 μm × 5 μm pits recorded in (a) contact mode and (b) dynamic mode (tapping mode). The pit is 180 nm in depth. The edge of the lever was used as a probing 'tip'.

pit edges to the ill-defined tip geometry. In order to increase the lateral resolution, a Pt tip has been deposited at the end of the cantilever. Fig. 9 shows an example of such a tip which was made by cracking an organometallic gas in a focused ion-beam machine. A gold-covered Si grating with a period of 1 μm was also investigated. Fig. 10 depicts the image recorded with the same lever in dynamic mode. The nominal amplitude of the lines is 15 nm.

6. Conclusions

In this article we have presented an integrated force sensor based on a MOS transistor for use in SFM. The sensor configuration was described and a theoretical and experimental investigation of the sensitivity was presented. A fabrication process consisting of a standard CMOS process and post-processing was introduced for making cantilevers with integrated deflection detection. It was found that the stress sensitivity was enhanced with decreasing gate voltage under a constant drain voltage. In contrast, the drain voltage did not

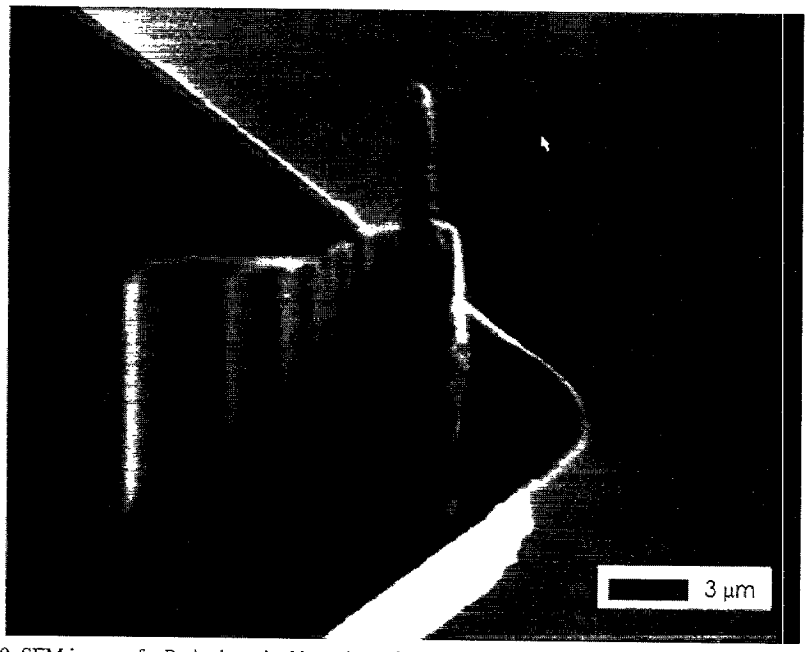

Fig. 9. SEM image of a Pt tip deposited by using a focused ion beam for cracking an organometallic gas.

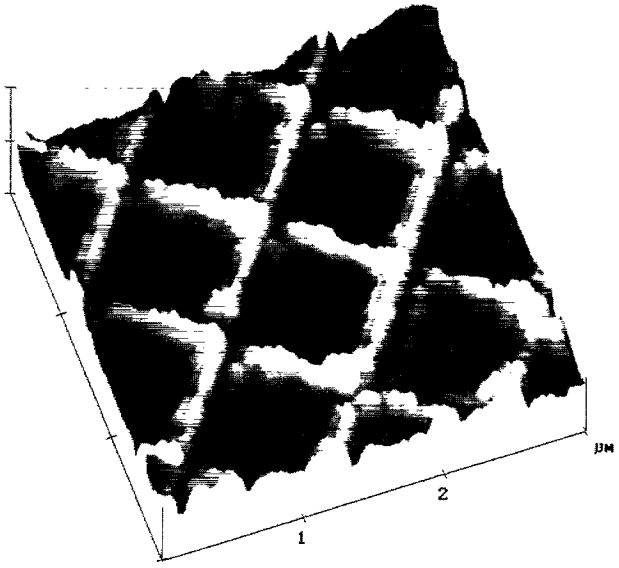

Fig. 10. A dynamic-mode image of a grating with a period of 1 μm. The height difference is 15 nm.

affect the sensitivity. The feasibility of SFM measurements with such levers in both contact mode and dynamic mode was demonstrated. Future improvements concern the mass production of integral tips at the free end of the cantilevers such that higher lateral resolution can be obtained.

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