LIMITING AMPLIFIERS FOR NEXT-GENERATION MULTI-CHANNEL OPTICAL I/O INTERFACES IN SoCs

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ABSTRACT

We present two fully differential limiting amplifiers with and without inductive peaking, designed and integrated in 0.18µm digital CMOS technology. The key design trade-offs, the importance of inductive coupling between neighboring channels, as well as the design of peaking inductors in a standard process are discussed. The amplifiers, which are intended for multichannel integrated optical receiver arrays, achieve a bandwidth of 4GHz and a gain of 32dB. The silicon area occupied by either amplifier is less than 0.5mm^2, while the area of the inductors can be further reduced.

1. INTRODUCTION

Technology scaling in successive generations of digital CMOS processes has led to increasing operating frequencies for the processor cores on the one hand, and to the emergence of multi-core processors on the other. In order to accommodate increasing data rates at the chip interface, alternative solutions to replace the synchronous bus paradigm must be developed. Electrical and optical serial interface solutions have been presented and major semiconductor companies are currently developing silicon-based lasers that could eventually be integrated [1]. Ultimately, full integration in a silicon CMOS-based manufacturing process is expected to result in very favorable cost/bit rate levels (Figure 1).

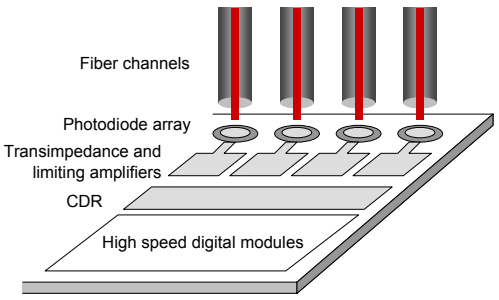

Fig. 1: Conceptual block diagram of an integrated multi-channel optical receiver for data communication

The design and fabrication of silicon SOI-based photodetector arrays with high quantum efficiency for 10 Gb/s data links have already been demonstrated [2], as well as the feasibility standard CMOS transimpedance amplifier array [3]. Obviously a microprocessor chip will contain many such optical input and outputs, which are not mandatorily synchronous. Inter-channel crosstalk of any nature may increase the bit error ratio (BER), be it due to substrate noise coupling, supply noise, capacitive or inductive coupling from close-by channels.

Considering a single channel receive chain (Figure 2), the transimpedance amplifier (TIA) converts the incoming photocurrent from the detector into a relatively small voltage. The realizable transimpedance gain does typically not exceed some kilo-ohms due to the inverse proportionality of the receiver bandwidth.

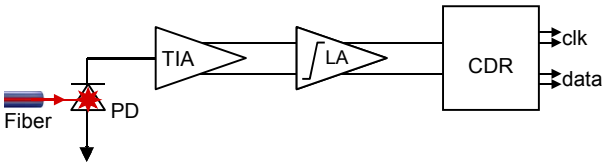

Fig. 2: Single channel fiber optic receiver diagram

The limiting amplifier (LA) boosts the transimpedance amplifier output voltage, which is typically a low-voltage differential signal, to a constant amplitude binary output. In this paper, we present design optimization strategies and trade-offs for high bandwidth limiting amplifiers and we compare the performance of an inductorless and an inductive-peaking limiting amplifier, both designed in a 0.18µm digital CMOS technology.

2. GAIN-BANDWIDTH TRADE-OFF FOR LIMITING AMPLIFIERS

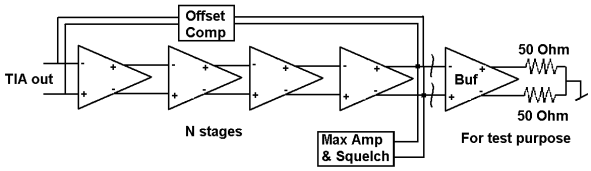

Fig. 3: Limiting amplifier block diagram

As shown in Figure 3, the limiting amplifier is composed of a cascade of N gain stages in open-loop configuration. Since each stage is built as a differential pair with resistive load (Figure 4), the only degree of freedom to improve the gain-band-

width trade-off is an increase of power consumption at the cost of higher input capacitance. Even this improvement is limited by the lower bound of the supply voltage as 1.6V.

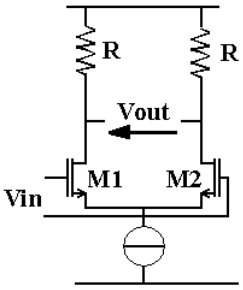

Fig. 4: Individual amplifier stage

This trade-off has been addressed in several papers with different approaches. As our primary goal is monolithic integration, only CMOS designs are mentioned here. Cherry-Hooper topologies [4] are very attractive for high gain, but suffer from decreasing supply voltages. The designs presented in [5] and [6] use high supply voltages to improve the achievable gain per stage, introducing reliability issues. The solution in [7] uses active inductors, which needs a high supply voltage, while [8] uses passive inductors, active feed-back and negative Miller capacitance. Magnetic coupling issues and area occupation of passive inductors will be discussed later.

3. INDUCTORLESS AMPLIFIER DESIGN

For robustness and large voltage headroom, we consider a cascade of resistively loaded differential pairs. Bandwidth and DC gain of such a cascade of N identical first-order amplifiers with identical cut-off frequencies f_{ci} are given by Equations 1 and 2.

$$BW = f_{ci} \cdot \sqrt{\sqrt[N]{2} - 1} \tag{1}$$

$$Av_{DC} = \prod_{i=1}^{N} Av_{DCi} = Av_{DCi}^{N} \quad \text{for identical } Av_{DCi} \tag{2}$$

Due to carrier velocity saturation in the differential pair, the resulting gain per stage is relatively small and does not allow for the use of bandwidth enhancement techniques like capacitive degeneration [9].

The bandwidth of each stage can be increased using the down-scaling technique proposed in [7]. If the stage (i+1) loading the stage (i) is scaled down by a factor h, the bandwidth of stage (i) achieved with an identical loading stage is multiplied by the same factor h. The drawback of this technique is the increase in input capacitance.

$$Av_{DC} = \left(\frac{g_{mu}}{2\pi \cdot BW} \cdot h \cdot \frac{1}{C_W \cdot (1 + \alpha \cdot h)} \cdot \sqrt{\sqrt[N]{2} - 1} \right)^N$$

$$\text{with } C_W = (C_{ox} \cdot L + C_{oxside} \cdot 2 + C_{overlap} \cdot Av_{DCi}) \tag{3}$$

$$\text{and } \alpha = \frac{C_J \cdot W_J + 2 \cdot C_{JSW}}{C_W}$$

An analytical expression of the DC gain, neglecting velocity saturation, allows its optimization while minimizing the input capacitance of the limiting amplifier. C_W and g_{mu} are the load capacitance and the transconductance normalized to a device width of 1µm, respectively. The gain is maximized through g_m/C_W by using minimum channel length devices and maximizing the current densities. It can also be shown that the results of the presented optimization still holds in presence of velocity saturation.

The complete expression cannot be solved analytically for Av_{DC}, but with a relatively small gain per stage, it can be shown that the Miller capacitance does not dominate the total load. An estimated value for the gain per stage is used and an error on this value will not dramatically affect the results obtained for the total gain.

In this flow, we first set the required bandwidth for the amplifier. Then we plot the achievable gain as a function of N and h (Figure 5). The horizontal plane shows the targeted gain and the intersection of both shapes gives the available solutions to the gain-bandwidth trade-off.

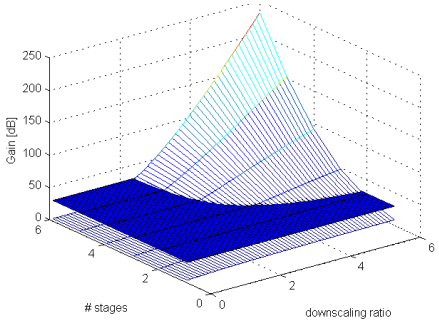

Fig. 5: Achievable gain as a function of (N,h) for a target bandwidth of 4.5GHz

Although downscaling is good for the overall noise performance, the penalties in the LA input capacitance may hurt the transimpedance amplifier design. It is preferable to achieve the required gain with a small number of amplifier stages and a larger downscaling ratio, than with a large number of stages (Figure 6). The area above the boundary curve corresponds to the (N,h) values for which the resulting gain exceeds the target value. The minimum input capacitance is obtained with four ampli-

fier stages and a downscaling factor of two.

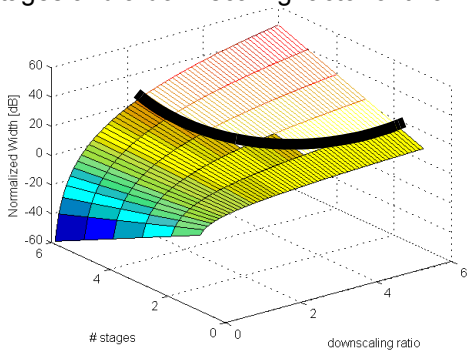

Fig. 6: Resulting normalized input capacitance of the limiting amplifier as a function of (N,h)

High gain requires low voltage drop on the current source I_0 to guarantee correct operation over all process corners and temperature variations. This results in large W/L ratios of the current sources, occupying considerable silicon area.

4. INDUCTIVE-PEAKING AMPLIFIER DESIGN

The large input capacitance of the limiting amplifier results in a large power consumption and chip area for the preceding transimpedance amplifier in the previous solution. In a second design, inductive peaking is used instead of downscaling to achieve the necessary bandwidth.

The required inductance value to partially cancel out the load capacitance was determined from simulation. A differential T-coil is used to maximize the benefits of the differential structure (Figure 7, [11]-[12]). The mutual inductance M of such a structure reduces the occupied chip area. The standard digital technology used for this design did not include any model parameters for spiral inductors. The effective parameters (self inductance L and mutual inductance k) have been simulated using ASITIC.

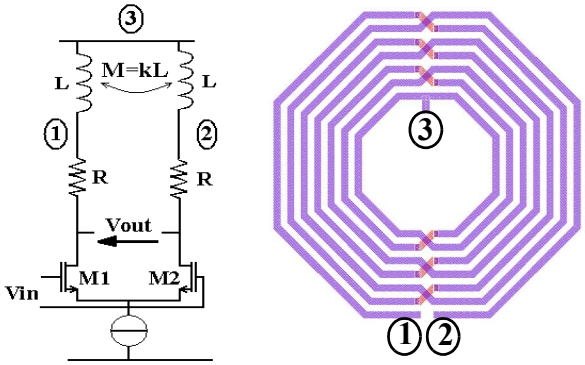

Fig. 7: Layout of the T-coil structure with terminals

Although the inductors are used in series with the load resistors and a high Q factor is not required, conservative geometric parameters are used. We should however be able to reduce the occupied chip area in future designs, using thinner wires and smaller core area, without neglecting the reduction of the self-resonant frequency. For this reason only the standard 0.9µm thick top metal layer was used.

Magnetic coupling should be a concern when targeting monolithic multichannel receivers using inductive peaking. Indeed, in the structure shown in Figure 7, the magnetic fields of both inductor parts add up, which explains the increased efficiency of these differential structures. Similarly, an external field applied to this differential inductor results in a differential signal appearing at its terminals.

5. SIMULATION RESULTS

As shown in Figure 8, the bandwidth of the amplifier with inductive peaking is slightly overdimensioned to compensate for weakly modeled Eddy current effects in the integrated inductors. The inductorless amplifier output swing exceeds the specification for the succeeding clock recovery input block by a factor of two. This has been corrected in the inductorless design, resulting in a drop in passband gain of 1.8dB.

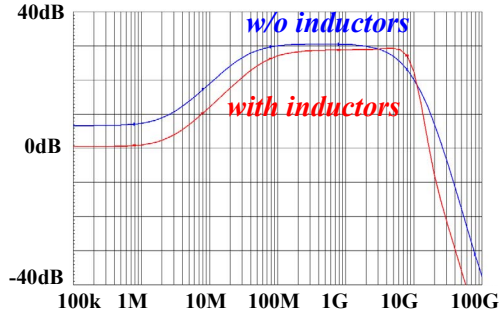

Fig. 8: Transfer function of both limiting amplifiers

The reduced gain at lower frequencies is due to the offset compensation mechanism. As the data encoding in short-distance communications guarantees a high transition density, only 2-3 decades of passband are required. The effects of inductive coupling from an active channel to a delayed “victim” channel is shown in Figure 9.

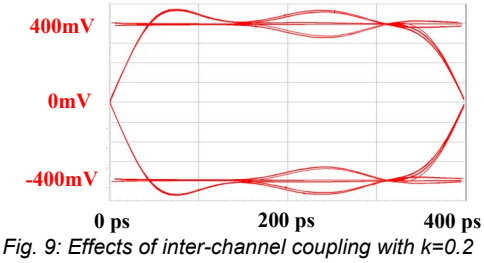

Fig. 9: Effects of inter-channel coupling with k=0.2

However, considerable eye closure at the amplifier output only appears with large mutual coupling coefficients (>0.1).

	LA w/o L	LA with L
Bandwidth [GHz]	> 3.7	> 4.5
DC Gain [dB]	> 25	> 23
Input Ref. Noise @ 1GHz [nV/sqrt(Hz)]	0.6	2.3
Load Capacitance to GND [fF]	2x 40	2x 40
Supply Current typ @ 25°C [mA]	60.0	7.5
Supply Voltage [V]	1.62-1.98	

Table 1: Simulation results for both limiting amplifiers

6. CHIP LAYOUT

Figure 10 and 11 respectively show the inductorless and inductive peaking limiting amplifiers with their respective drivers. Excluding the output driver stages, the inductorless LA occupies 0.4mm^2, while one LA with inductive peaking occupies 0.51mm^2.

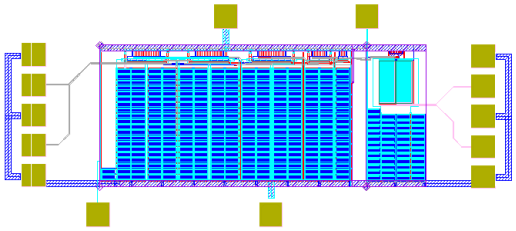

Fig. 10: Inductorless limiting amplifier layout (amplifier is 0.47mm x 0.84mm)

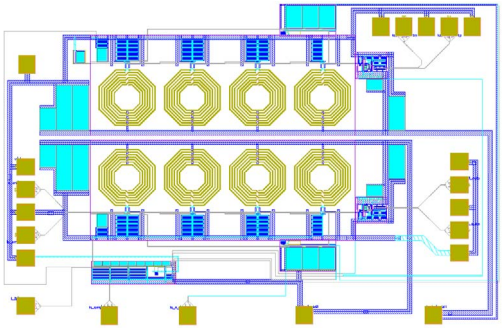

Fig. 11: Layout of two adjacent limiting amplifiers with inductive peaking (one amplifier is 0.44mm x 1.16mm)

7. MEASUREMENT RESULTS

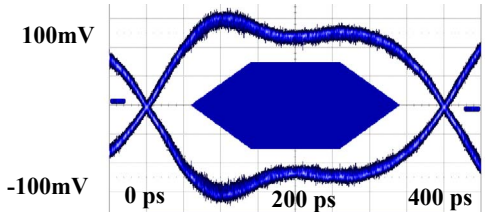

Fig. 12: Measured output of the inductorless LA

The wafer probed inductorless amplifier output is delivered by a 50Ω driver stage with a loss of ~10dB and a one decade passband, which therefor cannot handle PRBS data. The periodic sequence (Figure 12) at its output shows a swing of 200mV and operation at 2.5GHz. The inductive peaking amplifier benefits of an improved large bandwidth driver stage. Figure 13 shows perfect operation with a differential input of 20mV at 2.5 Gb/s.

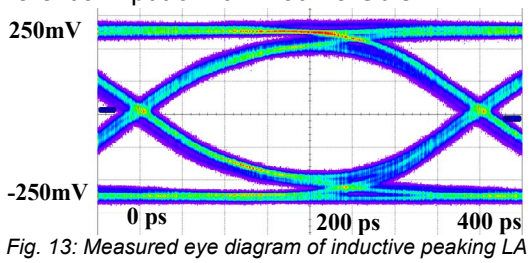

Fig. 13: Measured eye diagram of inductive peaking LA

Measurement of inductive coupling to the adjacent channel shows that for the case of large and near-by inductors, coupling effect must be considered. As smaller inductors have a lower quality factor and thus less coupling, careful placement of inductive peaking amplifiers should be sufficient to minimize crosstalk between neighboring channels.

8. CONCLUSION

We presented the trade-offs when designing multi-gigabit limiting amplifiers with and without passive inductors. The downscaling technique is analytically described and measurement results of the obtained design presented. Magnetic coupling issues in the case of adjacent limiting amplifiers with inductive peaking are presented.

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