SETMOS: A Novel True Hybrid SET- CMOS High Current Coulomb Blockade Oscillation Cell for Future Nano-Scale Analog ICs

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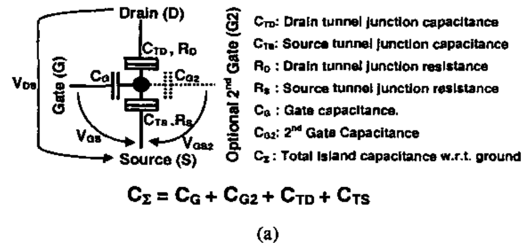
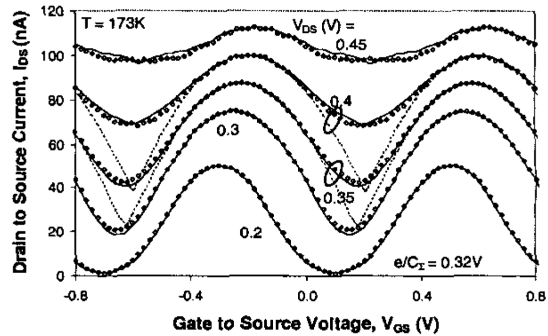
Introduction: Many recent studies [1-2] of nano-scale MOSFET and Single Electron Transistors (SET) suggest that these two solid-state devices are highly complementary: while CMOS advantages like *high-speed driving* and *voltage gain* cannot be matched by any proposed SET, SETs can potentially improve CMOS operation by virtue of their *ultra-low power* consumption [3] and *scalability*. Therefore, the combination of CMOS and SET could be promising solution for future nano-scale ICs. Since some programmable SET logic applications have been recently proposed and demonstrated [4], there is an acute need for true hybrid architectures for analog applications that could provide new functionalities, unachievable in pure CMOS technology. In this work, combining the virtues of both SET and CMOS devices, we propose a new hybrid elementary circuit cell, called SETMOS, which exhibits similar Coulomb Blockade oscillations as traditional Single Electron Transistor but offers much higher current driving capability. The proposed SETMOS cell acts, in fact, as an equivalent hybrid device with unique characteristics dictated by both its SET and MOSFET components. With realistic device parameters (corresponding to a 1-2nm island radius for the SET and the 65nm CMOS node [5] for the MOSFET), we use analytical SET model MIB to demonstrate its full new functionality in the *sub-ambient temperature range* (−150°C up to −100°C). The proposed SETMOS hybrid device not only substantially increases the drain-current capability of the traditional SETs, but also essentially exhibits a negative differential resistance (NDR) effect, which is unique compared to any other reported nano-scale NDR approaches, including pure SET circuits. Finally, for the first time, we present a *SET-MOS-NEMS* architecture with a second tunable SET gate capacitance, which *extends* the analog functionalities of the new SETMOS architecture.

Modeling Issues for Co-Design and Co-Simulation of SET/CMOS Hybrid Analog ICs: The use of SET as a candidate for hybridization with nano-scale-CMOS VLSI demands accurate analytical SET models instead of Monte Carlo (MC) simulation, Master Equation Method or Macro Modeling. Till date, all the SET analytical models [3,6] reported are valid for $|V_{DS}| < e/C_\Sigma$ [where C_Σ is the total island capacitance with respect to ground, see **Fig. 1(a)**], which is fairly practical for SET *digital* circuit design since the Coulomb Blockade region ceases to exist over $|V_{DS}| > e/C_\Sigma$ and the device is then handicapped for switching operation. By contrast, for SET-CMOS analog hybrid circuit design, a SET analytical model must remain valid over $|V_{DS}| > e/C_\Sigma$ due to two important practical requirements: (i) the use of constant current-biased SET (key architecture for designing SET analog cells), and, (ii) MOSFET biases may impose $|V_{DS}| > e/C_\Sigma$ to operate the SET. We propose the analog extension of our analytical SET model MIB [3], which also includes the capability of describing temperature behavior in the sub-ambient temperature range (up to −100°C). Specifically, the MIB model is analytically extended up to $|V_{DS}| \approx 1.5\ e/C_\Sigma$: in fact, for $|V_{DS}| > 1.5\ e/C_\Sigma$ SET characteristics becomes almost independent of V_{GS}. The proposed new model is embedded in professional circuit simulator SMARTSPICE [7] and verified against the simulated data from Monte Carlo simulator SIMON [8]. **Fig. 1(b)** reveals the accuracy of our analog SET model for a wide range (more than e/C_Σ) of values for V_{DS}. **Fig. 1(c)** demonstrates the accuracy of MIB model for a wide range of temperatures up to $T = e^2/(20k_BC_\Sigma)$[e.g., 185K for C_Σ= 0.5aF]. Note that the new analog SET model allows the analytical estimation of the sub-threshold slope (S) of SET: $S = d(V_{GS})/d(log_{10}I_{DS}) \approx (C_\Sigma k_BT)/(0.434eC_G)$. Also, with the proposed analog SET model, accurate co-simulation with MOSFET in both static and dynamic operations can be achieved in a SPICE simulation environment.



(a)



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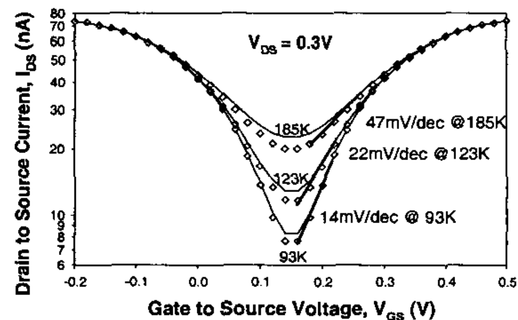

(c)

Figure 1: (a) Schematic of a basic SET device (b) Verification of MIB model for symmetric device with $C_G = 0.2aF$, $C_{TD} = C_{TS} = 0.15aF$ and $R_D = R_S = 1M\Omega$. Here symbols denote Monte Carlo simulation (SIMON), solid line represents MIB and dotted line represents MIB without $|V_{DS}| > e/C_\Sigma$ correction. (c) Validation of MIB and the Subthreshold Slope of the SET at T= 93K (p = 40), 123K (p = 30), 185K (p = 20) where $p = e^2/(k_BC_\Sigma T)$.

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SETMOS - High Current Coulomb-Blockade Oscillation Device: The new hybrid SETMOS cell architecture is depicted in **Fig. 2(a)**. The SET is biased by a constant current source and the drain terminal of the MOS serves as the output of the device [see **Fig. 2(a)**]. A unique characteristic of this hybrid circuit is that the output of the current biased SET (V_{DS1}) is a periodic (e/C_G) function of the input voltage (V_{GS}) [**Fig. 2(b)**], which *extends the Coulomb Blockade oscillation in the drain current of the MOSFET* such that higher current capability (~μA) output can be achieved [**Fig. 2(c)**].

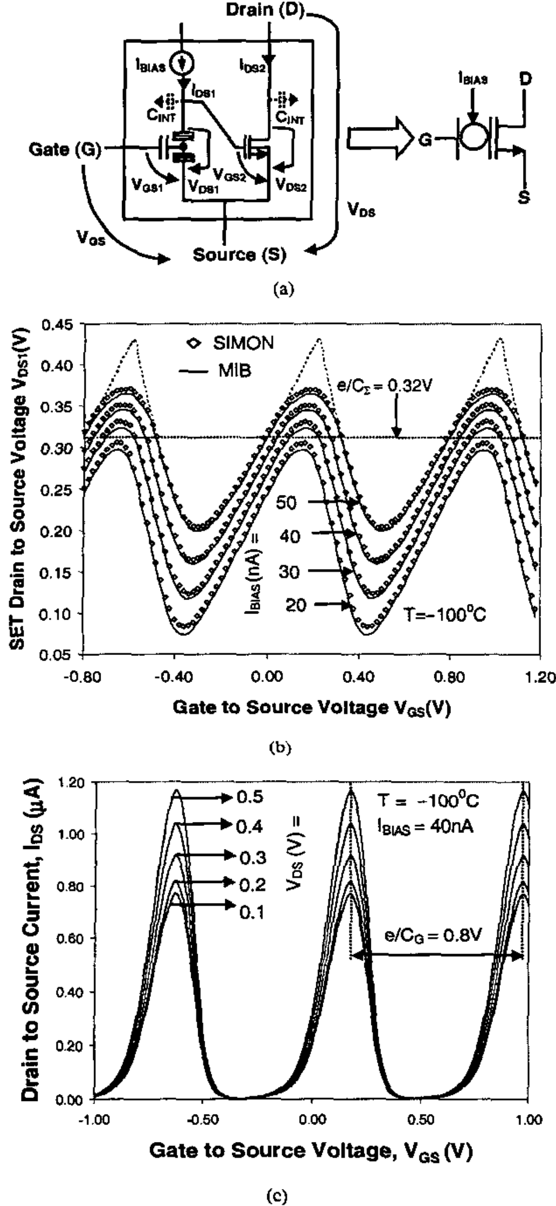


Figure 2: (a) Schematic and symbol of the proposed SETMOS device. Here C_{INT} represents the interconnect capacitance which is much bigger than the device capacitances of the SET (b) The periodic oscillation of drain to source voltage of the SET as a function of input voltage for different current biases as calculated by MIB and SIMON (dotted line represents MIB without $|V_{DS}|>e/C_\Sigma$ correction). The device parameters for the SET are same as Fig.1. (c) Characteristics of 'SETMOS' as obtained by SMARTSPICE simulation for the same SET device parameter. Here we have used BSIM parameters for 65nm node [5] for the MOS simulation.

The MOSFET is operated near its sub-threshold region in order to obtain effective Coulomb Blockade region, higher (exponential) sensitivity to V_{DS1} oscillation and low power dissipation. The characteristics of the SETMOS are demonstrated by the new model in sub-ambient temperature regime (near −100°C), where both SET and nano-MOSFET can properly operate with realistic parameters. There has recently been increased interest for CMOS ICs to be operated at these low temperatures for leakage power dissipation reduction [9]. The SET is assumed to have an island capacitance of ~0.5aF, reflecting an island radius of 1-2nm. The MOSFET has the parameters of L = 65nm, W = 100nm, T_{ox} = 1.7nm, V_{TH} = 0.32V. **Fig. 2(a)** depicts the new symbol used for SETMOS that can be finally assimilated with a hybrid SETMOS three-terminal device that *inherits Coulomb Blockade oscillations* and operates with *currents more that two decades higher* compared with a pure SET.

NDR Device and analog applications of SETMOS: By shorting the gate and drain of the SETMOS architecture one can use it as a unique NDR device, **[Fig. 3(a)]. Fig. 3(b)** explains the working principle of the SETMOS NDR and **Fig. 4** demonstrates a clear NDR region, as obtained by SMARTSPICE simulation. It is worth noting that *a MOS gate leakage current higher that SET current* [see inset of **Fig. 5(a)**] *could destroy the periodicity of the NDR device* and would cause the device to act as an ordinary resistor. The input conductance characteristics and temperature response of the SETMOS-NDR device are presented in **Fig. 5(a) and (b)**, these represent a significant improvement over the NDR device proposed by Heij et al.[10], which was based on a single electron box (SEB). **Fig. 6** reports a basic scheme to use the proposed circuit as a potential divider in order *to amplify analog signal* (via the NDR effect), which is a practical application of such hybrid CMOS-SET architecture. Gain values corresponding to the NDR region, [i.e., $A_v = 1/(1+Rg_{IN})>1$, see **Fig. 6**] up to 10 demonstrates that such a divider can be used as hybrid CMOS-SET amplifier. Note that similar gain values have not yet been achieved by pure SET [2, 3] architectures.

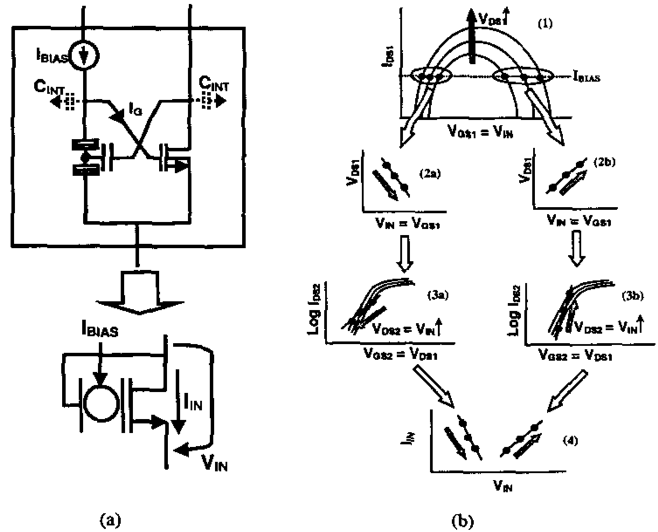


Figure 3:(a) Schematic of the application of SETMOS as NDR device. (b) working principle of the SETMOS-NDR device.

NEMS-SETMOS: Hybrid analog CMOS-SET cells such as SETMOS could directly benefit from the recent progress achieved in developing NEMS technology. With a suspended conductive layer using nano-air gap [11] of the order of some tens of nm, a tunable-gate SET device can be imagined and modeled. A possible layout and its gate capacitance characteristics are reported in **Fig.7.**

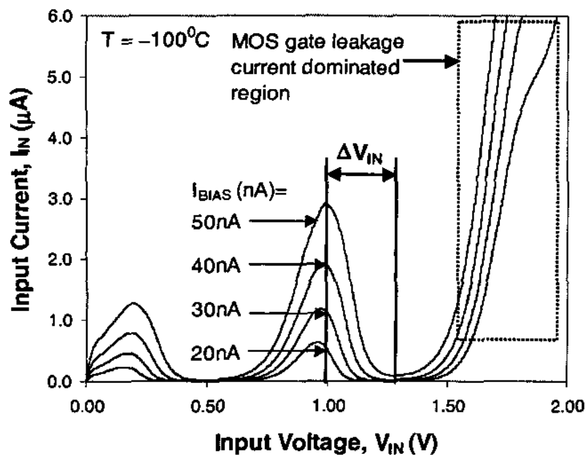


Figure 4: Characteristics of the NDR device as simulated by SMARTSPICE. ΔV_{IN} denotes the NDR regime.

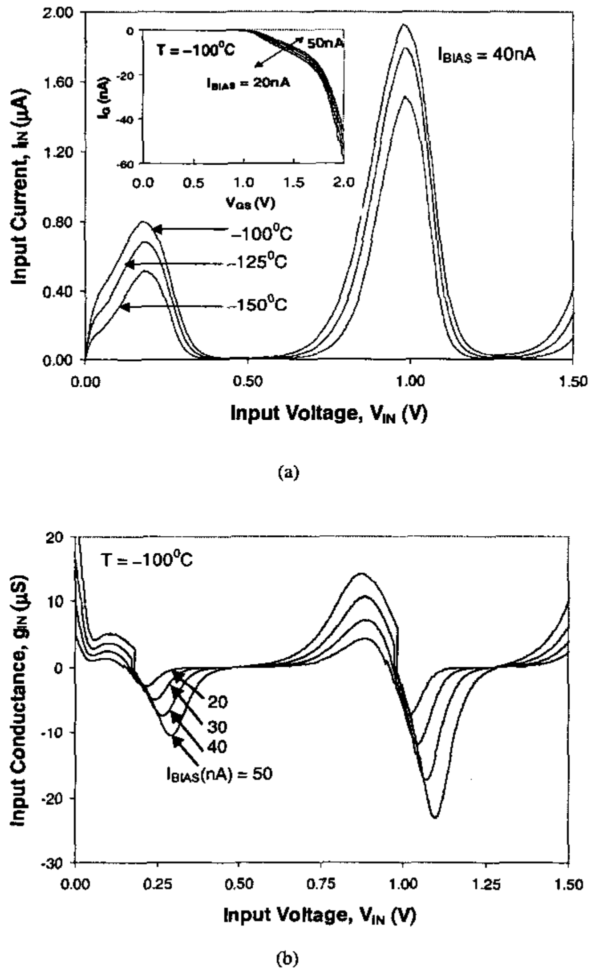


Figure 5: (a) Effect of temperature on SETMOS-NDR device [*inset:* MOS gate leakage current (I_G)] (b) input transconductance ($g_{IN} = dV_{IN}/dV_{OUT}$) as obtained from Fig. 4.

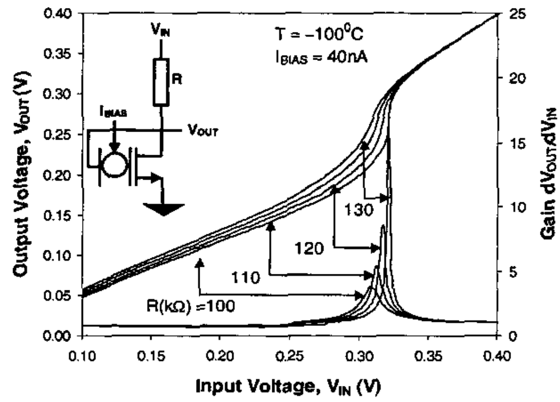


Figure 6: Application as a potential divider in order to achieve voltage gain.

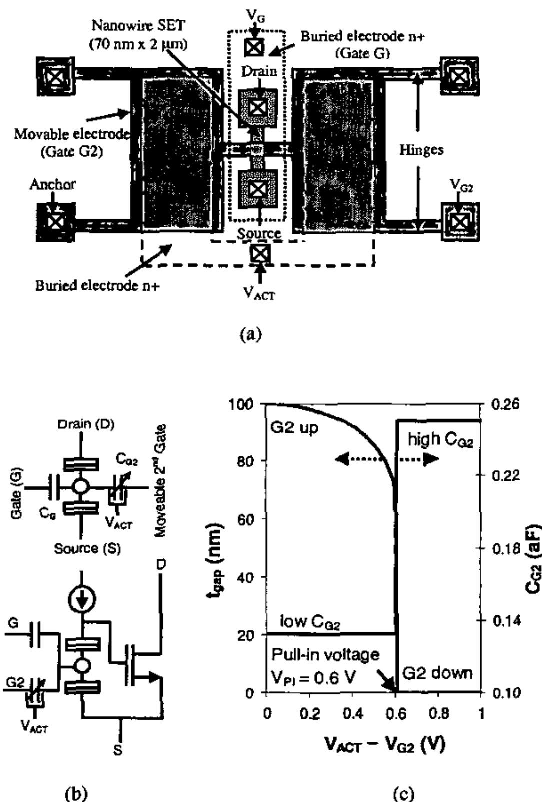


Figure 7: (a) Proposed layout for NEMS-SET device. The moveable metal electrode (*G2*) is electrostatically actuated by $V_{ACT} - V_{G2}$. A relatively high movable electrode surface (= 100 μm²), a small air gap (= 100 nm) and a low stiffness design (with elastic hinge coefficient, k = 1 N/m) are required for low-voltage (<1V) actuation. Circuits (b) show schematics of NEMS-SET device and NEMS-SETMOS, respectively. Plots (c) represent the displacement of the NEMS capacitor membrane (left axis) and corresponding C_{G2} variation (right axis) vs. actuation voltage, $V_{ACT} - V_{G2}$, for $V_{G2} = 0V$. In fact, the tuneable NEMS capacitor acts as a two-state capacitive switch (the n+ region underneath the movable membrane being covered with a 20nm thin oxide) with a pull-in voltage $V_{PI} = 0.6V$ (applied voltage at which the movable electrode snaps down).

By coupling a NEMS tunable capacitor model with our SET analog analytical model MIB and BSIM, we report for the first time, simulated electrical characteristics of hybrid NEMS-SET-MOS (**Fig. 8**), that couples electrical and mechanical characteristics at

nano-scale and suggest another novel functionality device: tunable-gate NEMS-SETMOS. Exploiting the fact that tuning of C_{G2} by external bias changes the C_Σ of the device, one can design novel threshold gate (hard limiter) as shown in **Fig. 9 (a)**. The proposed NEMS-SETMOS threshold gate can be realistically used to design high-density neural networks **[Fig. 9(b) and 10]** or a dense array of Analog-to-Digital flash converter (**Fig. 11**), which actually demand high-speed operation with low power consumption.

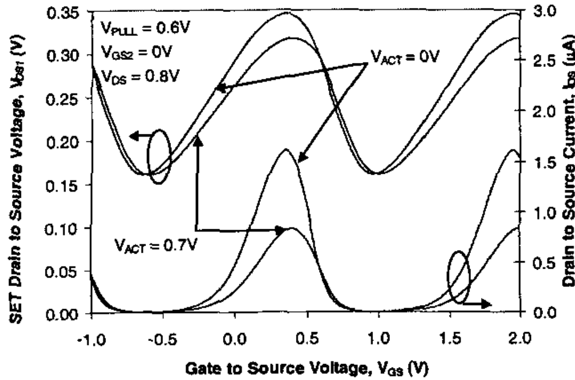
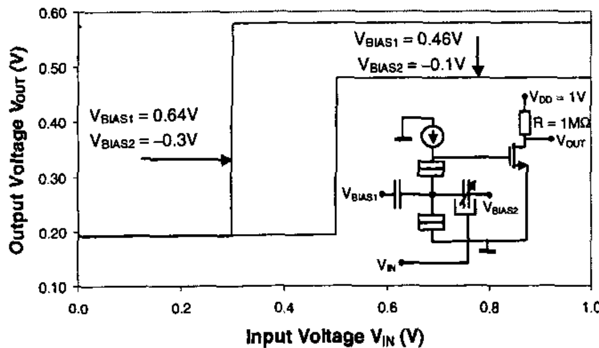
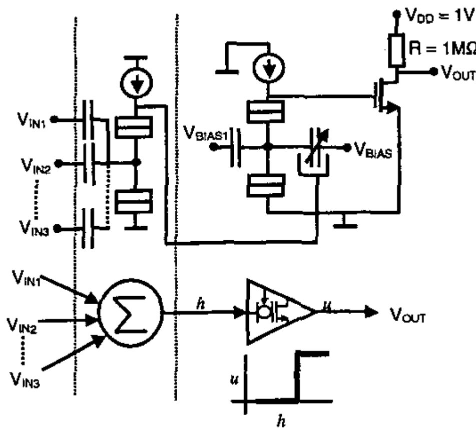


Figure 8: Characteristics of tunable gate NEMS-SETMOS device



(a)



(b)

Figure 9: (a) Application of NEMS-SETMOS as a threshold gate or a hard limiter (b) schematic of a CMOS-SET hybrid neuron cell by using the NEMS-SETMOS threshold gate.

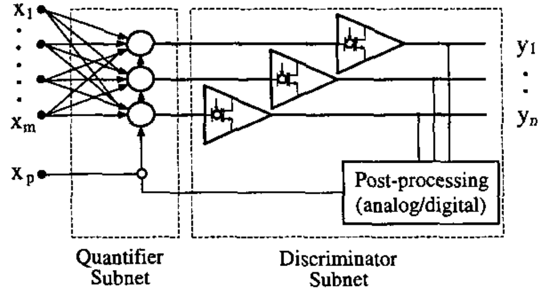


Figure 10: Schematic of the Hamming artificial neural network by using NEMS-SETMOS threshold gate [12]. Here x_is and y_is are input and output vectors respectively.

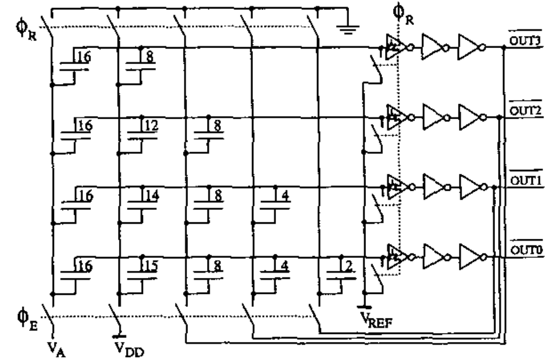


Figure 11: Application of NEMS-SETMOS threshold gate as Analog-to-Digital flash converter [13]. A very dense array design demands SET-CMOS hybrid circuit design instead of standard CMOS technology.

Conclusion: We have proposed and validated a true hybrid SET/CMOS device, called SETMOS, that is able to extend the Coulomb blockade oscillations of a SET transistor into the μA current range, corresponding to near sub-threshold operation region of a nanometer-scale MOSFET. New nano-scale analog applications, working at sub-ambient temperatures (−150°C up to −100°C), including a novel NDR circuit, amplifiers, and even NEMS-SETMOS circuit cells are uniquely supported by SETMOS.

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