TWISTED DIFFERENTIAL ON-CHIP INTERCONNECT ARCHITECTURE FOR INDUCTIVE/CAPACITIVE CROSSTALK NOISE CANCELLATION

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ABSTRACT

A simple generic interconnect architecture is presented to allow effective cancellation of inductive and capacitive noise in high-speed on-chip interconnect lines. The approach is based on the principle of constructing periodically twisted differential line pairs for parallel interconnect segments in order to eliminate the mutual coupling influences. Detailed 3-D simulations show that a crosstalk noise reduction of up to 60 dB is achievable with this approach.

1. INTRODUCTION

With continued scaling of device features and interconnect dimensions down to deep-sub-micron and nanometer range, interconnects are becoming the limiting factor for performance and reliability in many system-on-chip (SoC) designs. Since the overall chip dimensions continue to increase with increasing system complexity, interconnects - especially the long-distance connections between various system blocks on chip - tend to get longer. At the same time, wire width and wire separation continue to drop while their cross-sectional area is scaled down at a slower rate to prevent resistance values increase dramatically. This ongoing trend of controlling the RC delay, combined with the faster rise/fall times and longer wires, makes the inductive part of the wire impedance become comparable to its resistive part [1]. Thus, inductive effects, and more specifically, mutual inductive coupling between neighboring wires, become non-negligible in recent VDSM technologies. In this paper, we explore inductive coupling effects between neighboring parallel wires using a simple, physically-based equivalent circuit model, and we propose simple generic interconnect architecture to reduce cross-talk noise due to capacitive and inductive coupling between the interconnects. The proposed differential design and twisted-pair layout strategy is shown to reduce the observed cross-talk noise by about 60 dB in certain cases. This approach could prove to be a very suitable solution for the design of long high-speed bus lines that link various system sub-blocks on chip, achieving very low, predictable delays and noise levels even at very high switching speeds.

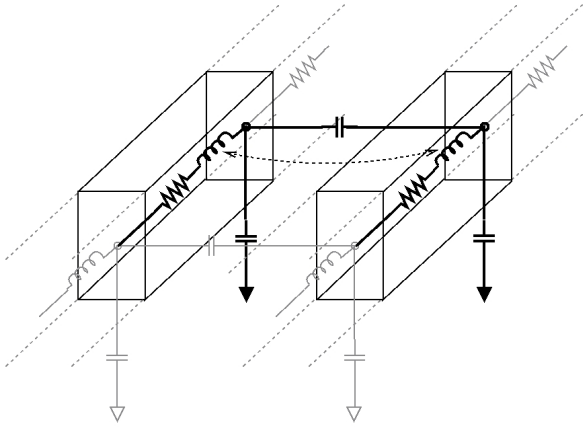

Figure 1: RLCM model of an interconnect segment, showing inductive and capacitive coupling between two parallel lines.

2. ON-CHIP INTERCONNECTS

The classical approach for modelling on-chip interconnects is based on the assumption that the wire loads are mainly capacitive and lumped. In most cases, however, the load conditions imposed on the interconnection line are far from being simple. The line, itself a three-dimensional structure in metal (aluminium wires and tungsten vias), usually has a non-negligible resistance in addition to its capacitance. The (length/width) ratio of the wire usually dictates that the parameters are distributed, making the interconnect a true transmission line. Also, an interconnect is rarely isolated from other influences. In realistic conditions, the interconnection line is in very close proximity to a number of other lines, either on the same level or on different levels. The capacitive/inductive coupling and the signal interference between neighboring lines should also be taken into consideration for an accurate estimation of delay.

In general, if the time of flight across the interconnection line (as determined by the speed of light) is much shorter than the signal rise/fall times, then the wire can be modelled as a capacitive load, or as a lumped or distributed RC network. If the interconnection lines are sufficiently long and the rise times of the signal waveforms are comparable to the time of flight across the line, then the inductance also becomes important, and the interconnection lines must be modelled as transmission lines.

Figure 1 shows the simplified cross-section of two parallel interconnect lines, together with one segment of the distributed RLCM network that represents the resistive/capacitive/inductive loads as well as the capacitive and inductive coupling between the lines (also called the PEEC model, [2]).

The inductive effects mainly manifest themselves as the overshooting and undershooting of the signal edges, switching noise due to Ldi/dt voltage drop, and the long-range coupling. However, most of the techniques which have been used in order to reduce noise on wires, like shielding, increasing metal-to-metal spacing and etc., are more suitable for countering capacitive effects.

The capacitive coupling and the resulting capacitive crosstalk noise between neighboring wires are relatively well studied and understood. The capacitive cross-talk noise can be easily reduced by introducing a shield between the aggressor line and the victim line, because electric fields are terminated on the neighboring metallic nodes. However, the same is not necessarily true for the magnetic fields, which may extend well beyond the aggressor nodes. Therefore, the definition of the return path is very critical in determining the inductance of a wire. In the following, we demonstrate how the capacitive noise and the inductive noise can be suppressed significantly by applying a simple, repetitive interconnect pattern (structure) at the layout level.

3. INDUCTIVE COUPLING BASICS

Our first assumption is that we use two parallel traces for each signal line; driven in true differential mode: while one of the input nodes of the line is making a low-to-high transition, its complementary input node is making a high-to-low transition. Clearly, it requires gates (or line drivers) with two complementary outputs and also, differential receivers.

Using low-voltage swing differential signaling already offers a range of advantages: faster circuits, less crosstalk susceptibility, reduced power consumption and reduced electromagnetic interference (EMI). All these benefits are mainly due to the fact that the differential driver needs to drive a load only to a few hundreds of millivolts, compared to a few volts depending on the technology used. Therefore, differential drivers are much smaller compared to single-ended drivers, which results in smaller change of current in time, followed by significant reduction of inductive noise [3]. Still, the use of full differential signaling is not capable of eliminating the inductive crosstalk between lines.

To allow a perfect cancellation of coupled magnetic and electric field components between two parallel adjacent lines, we consider using twisted differential line (TDL). The benefits of using twisted lines on printed circuit boards (PCB) are already studied and well-known [4]. Twisted line interconnect architectures have been proposed earlier for on-chip connections as well [4][5], but the systematic application of this structure together with full-differential signaling has not been studied or analyzed yet.

To start the theoretical modeling, first consider an interconnect segment (a) with a current i_a, and the magnetic field generated by this wire segment (aggressor loop, Figure 2).

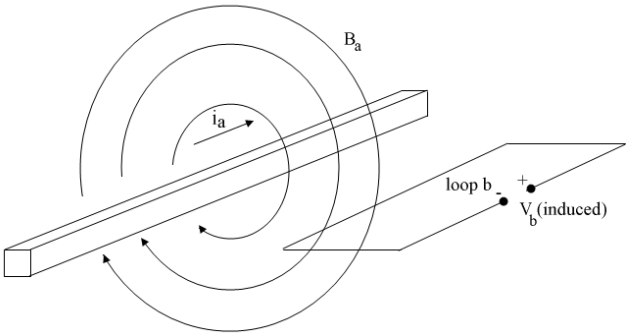

Figure 2: Magnetic field generated by the aggressor line influencing the victim loop.

The strength of the magnetic field generated by the aggressor loop is proportional to the current i_a. The direction of the magnetic field is determined by the direction of the current i_a [7].

$$\oint \overrightarrow{B_a}\,\overrightarrow{dl} = \mu \int_S \overrightarrow{j_a}\,\overrightarrow{dS}$$

The the magnetic flux Φ in loop (b) caused by (a) can be calculated using the following:

$$\Phi a = \int_{area\,of\,loop\,b} \overrightarrow{B_a}\,\overrightarrow{dS}$$

The voltage induced in loop b is defined as the time derivative of the magnetic flux that is caused by the current in (a).

$$\Rightarrow \quad V_b(induced) = \frac{d}{dt} \int_{area\,of\,loop\,b} \overrightarrow{B_a}\,\overrightarrow{dS}$$

4. ANALYSIS OF THE TDL STRUCTURE

Now, assume that two adjacent differential signal lines are formed as shown in the Figure 3. In this figure, the length of lines between two twisting sections is assumed to be much larger than the distance between the differential pairs.

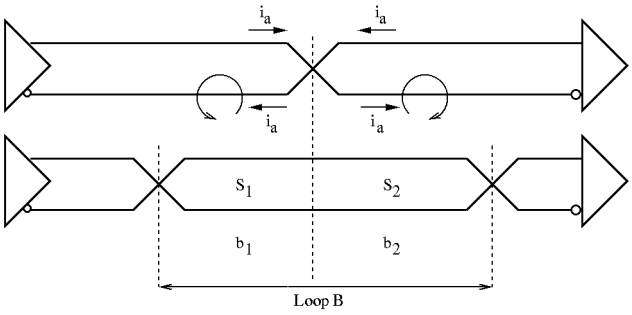

Figure 3: Offset twisted differential line arrangement used in coupling field analysis.

To calculate the total voltage induced by the aggressor line (a) on the victim loop (b), we can divide the surface of the loop (b) into two equal parts (b_1 and b_2), each with the same surface ($S_1 = S_2$).

$$V_b(induced) = \frac{d}{dt}\left(\int_{loop1} \overrightarrow{B_1} d\overrightarrow{S_1} + \int_{loop2} \overrightarrow{B_2} d\overrightarrow{S_2}\right)$$

Since the fields B_1 and B_2 are generated by the same current magnitude (i_a) but with opposite polarity, their strength (magnitude) is equal. Hence:

$$V_b(induced) = \frac{d}{dt}\left(\int_{loop1} \overrightarrow{B_1} d\overrightarrow{S_1} - \int_{loop1} \overrightarrow{B_1} d\overrightarrow{S_1}\right) = 0$$

This means that the amount of induced voltages on the victim loop will cancel out each other for any two adjacent twisted sections, as shown in Figure 3.

Also note that in the proposed arrangement (offset twisted differential line), there is no fundamental difference between the aggressor and the victim line - i.e., the roles are completely reversible, and the cancelling effect would be observed in that case, as well.

Now, the phenomenon of inductive crosstalk noise cancellation can also be described by using equivalent lumped circuit elements for the two differential lines. To simplify the view, only the partial inductance elements are shown. Each line segment is modeled by two equal partial inductances [2][3], as shown below in Figure 4. Note the current directions in each branch and the dots indicating the direction of inductive coupling.

Note that the polarity of the voltage induced by one inductor (L) on an adjacent inductor is determined by the relative location of the dots and by the current directions. At the same time, the magnitude of the induced voltage is determined by the amount of mutual inductance (M) between two adjacent line segments.

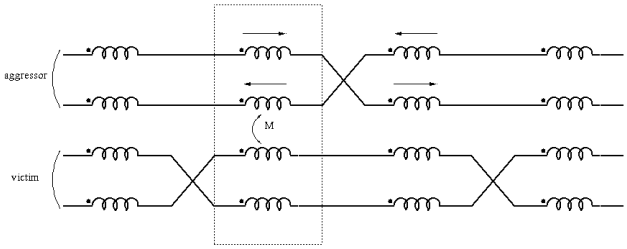

Figure 4: Lumped circuit element model of two TDL segments, showing only inductive elements for simplicity.

It can be seen that the voltage induced by each partial inductor will be cancelled out by the voltage (same magnitude, reverse polarity) induced on the neighboring segment. Also note that this is true for all line segments (even for those located further apart) and not just the closest ones. Furthermore, it can be shown easily that the offset TDL structure is similarly effective for the cancellation of capacitive coupling between the adjacent line pairs.

5. SIMULATION RESULTS

To demonstrate the effectiveness of the proposed approach, a series of detailed transient simulations were made assuming a TDL segment with a length of $500\mu m$, with line width of $0.6\mu m$, line separation of $0.6\mu m$ and metal height of $925nm$. It is assumed that the line pair is periodically twisted at an interval length of $10\mu m$. The twisted line segments were modeled using the full PEEC model (as shown in Figure 1), including partial resistance, capacitance, inductance as well as coupling capacitance and mutual inductance values calculated by the 3-D extraction package OEA-NETAN (METAL/HENRY) [8]. In all simulations, the aggressor is driven by a signal with rise/fall time of 100ps, while the victim line input is kept at a constant DC level (not left floating). The voltage fluctuation at the output end of the victim line, terminated with a capacitive load, is measured as the crosstalk noise voltage.

Figure 5 shows the crosstalk noise voltage on a single-ended victim line subjected to the same conditions, compared to the noise on a TDL. The noise level on the TDL victim remains significantly lower than that on the single-ended victim line. To make a fair comparison, the crosstalk noise on a straight full-differential line pair is shown in Figure 6, in comparison to the noise on the TDL, with the same conditions and using the same geometry. It can be seen clearly here as well that the TDL approach results in dramatically lower crosstalk noise. Under certain conditions, the reduction of crosstalk noise can be in the order of 60 dB.

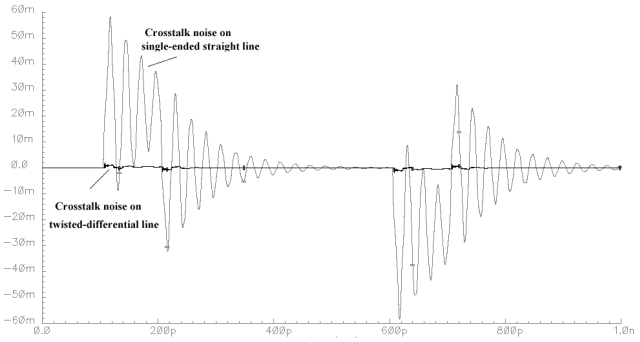

Figure 5: Simulation results for comparison of single-ended straight line vs. TDL.

It was also determined that the additional via resistance that are associated with the TDL structure do not significantly influence the results.

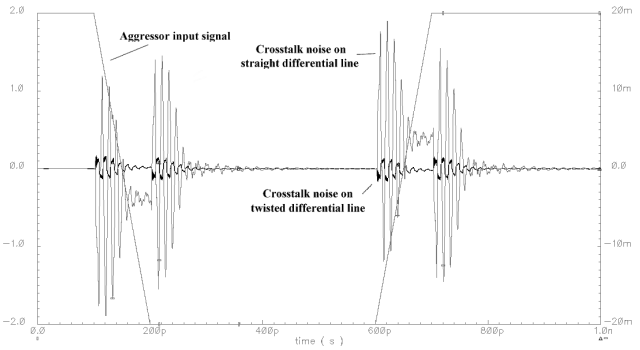

Figure 6: PEEC-based model simulation results, TDL vs. straight-differential line.

Finally, the noise performance of the TDL structure was simulated using the full 3-D extraction/simulation package OEA-NETAN [8], which confirms the theoretical model expectations and the simulations made using the PEEC-based model (Figure 7).

6. CONCLUSIONS

In this paper, we present a fully differential, offset twisted interconnect structure that is capable of reducing the crosstalk noise between adjacent line pairs by as much as 60 dB. The effectiveness of the proposed interconnect architecture is demonstrated with detailed simulation results. This approach could be applied very early and efficiently to construct highly noise-tolerant, on-chip high-speed bus structures for SoC.

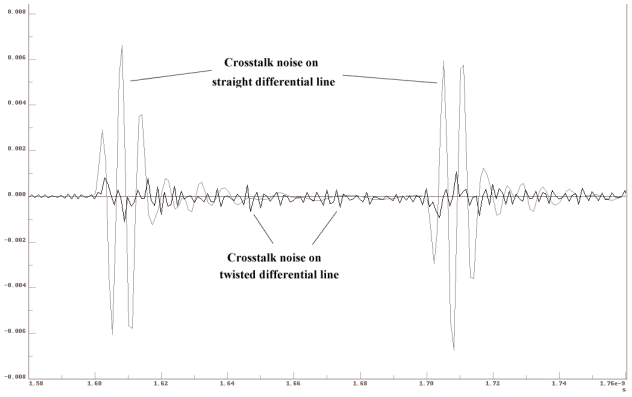

Figure 7: 3-D simulation results for TDL vs. straight differential line comparison.

7. REFERENCES

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