SYMMETRICAL MULTILEVEL CONVERTERS WITH TWO QUADRANT DC-DC FEEDING

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Preface

About four and a half years ago, I started my diploma project in the field of multilevel converters in the Industrial Electronics Laboratory (LEI) of the Federal Institute of Technology in Lausanne (EPFL). The Laboratory was headed by Prof. Bühler, while Prof. Rufer was his assistant Professor.
After my excellent four-month experience in the laboratory doing my diploma project, I obtained my Masters degree as an Electrical Engineer from the Swiss Federal Institute of Technology (ETHZ) in Zürich. I was motivated to stay in Lausanne to do further research in this promising field. So Prof. Rufer gave me the chance to stay in the LEI for further research activities on multilevel converters. Meanwhile, Prof. Rufer had become the head of the LEI. After three and a half years, from 1996 to 2000, my work on the multilevel converters advanced and many publications on the topic were written. The result of this project is the thesis presented here, a project that has been done in collaboration with a competent industrial society, namely ADtranz, recently bought by Bombardier.

I would like to thank Mr. Prof Rufer for his excellent aid throughout my research work, for his availability and open-mindedness for new research ideas, and in particular I want to mention his outstanding social competence.

From the Industrial Electronics Laboratory I would like to thank Mr. Gilbert Renggli, always responsible for the excellent working conditions in the laboratory. My thanks also goes to all the assistants of the LEI for their support and for the good atmosphere they contributed to the lab. I do not want to forget to thank the diploma students Minh T. Nguyen and Adrian Schaller who participated actively in this research project, and of course Christian Briguet, who started his diploma project on the same topic together with me.

Special thanks must be attributed to my industrial partner ADtranz, namely Mr. Stefan Umbricht and Mr. Michael Steiner for the collaboration and the variety of ideas they brought into my work. It was very stimulating for my thesis to work together with the people who are looking for new applications for industrial products.

I would also like to thank my family, especially my mother, for their constant support. Last but not least my thanks go to all my friends from the international community of Lausanne, who in many different ways actively or passively took part in the realization of my work or in inspiring me to create new ideas.

Nikolaus Schibli

Abstract

In the technology sector of power electronics and control, the multilevel converter technology is still a rather new research area, but the application possibilities in the field of power drives and energy will demand more solutions with this promising technology. In the future, more converter systems will be realized with the multilevel topology. Up to now, multilevel converters have only been used in very particular applications, mainly due to the high costs and complexity of the multilevel converter system. The high costs are due to the fact that the latest technology on semiconductors, magnetic material for inductor and transformer cores and control system technology had to be used.
But nowadays new developments in the fields of power semiconductors such as the IGBT, IGCT and perhaps in the future SiC switches as well as improvements of the performance of magnetic cores used in medium frequency transformers will favor the multilevel converters for many other application fields. It can be noted that the industrial trend is moving away from heavy and bulky passive components towards power converter systems using more and more semiconductor elements controlled by powerful processor systems integrating intelligent multi-task control algorithms.

The presented work is a contribution to the large field of multilevel converters. It shows a certain kind of multilevel converter in a single phase and a three-phase configuration, called the series-connected four-quadrant converters (SCFQ). The two specialities of the presented converter type are a) that all the multilevel converter steps are fed by an identical DC voltage and b) that every multilevel converter step is realized with an individual AC-DC converter or four-quadrant converter. This type of multilevel converter is called multilevel converter with symmetrical feeding.
In this work, a general theoretical development has been done for the use of this multilevel converter type. A special type of DC-DC converter is presented, in order to feed the individual four-quadrant converters of the multilevel converter with a constant DC voltage. All the developments and methods used are based on mathematical expressions. Various simulations using the latest software simulation tools are accomplished and are used to study different cases. The feasibility of the developments is underlined with a series of experimental results with all types of the used converters, which have been realized in the framework of this thesis.

The main application for the multilevel converter presented in this work is the front-end power converter in locomotives. Instead of using a heavy low-frequency transformer to reduce the high-voltage from the catenary to a supportable voltage for the semiconductors, a multilevel converter concept is used. The multilevel converter is directly coupled to the catenary. There are many advantages compared to the existing solutions. In the same context, a novel solution of a multilevel converter has been developed for a locomotive usable on different power lines. The converter allows not only the operation on the high AC voltage power line (15kV), but also can be coupled to a medium-voltage DC power line(3kV). Three different configuration types of the locomotive converter have been developed and tested in a complex simulation environment. Besides the locomotive application, there are many more interesting applications for the symmetrical multilevel converter, e. g. in the fields of energy transmission (FACTS, static VAR compensators, electronic high-voltage transformers, etc.) and industrial drives. But certainly in the fu-

ture with the availability of cheap semiconductors adapted to the needs of the multilevel converter, even more applications in lower power fields will be realized.

Résumé

Dans le domaine de l'électronique de puissance et des systémes de réglage, les convertisseurs multiniveaux sont un secteur de recherche relativement récente. Les possibilités d'application de cette technique dans le domaine des entraînements électriques et de la conversion statique de l'énergie électrique sont nombreuses, cependant elles demandent encore beaucoup de développements et d'optimisations pour être appliquées industriellement. A l'avenir il aura de plus en plus de systèmes de conversion statique qui vont utiliser les onduleurs multiniveaux. Jusqu'à aujourd'hui, les solutions industrielles des convertisseurs réalisés avec des niveaux multiples sont plutôt rares, et on les trouve dans des applications plutôt exotiques. Ceci est causé par le fait que le nombre de composants nécessaires comme les semi-conducteurs de puissance est élevé, et les processeurs de signaux puissants inévitables. Les solutions réelles ont toujours été handicapées par le prix élevé qui en résultait.
Mais les derniers développements dans le domaine des semi-conducteurs de puissance comme par exemple les IGBT, IGCT et à l'avenir les SiC (Silicium Carbide), mais aussi les derniers matériaux utilisés pour fabriquer des noyaux magnétiques vont faire avancer la technologie des onduleurs multiniveaux d'une manière décisive pour certaines applications. Dans l'industrie, la tendance et est de plus en plus de renoncer aux composants passifs emcombrants et lourds, comme les transformateurs et les filtres, et d'utiliser de plus en plus des convertisseurs qui ont un nombre élevé de semi-conducteurs, et qui sont commandés et réglés par des systèmes de processeurs puissants, intégrant des algorithmes de réglage sophistiqués.

La thèse présentée est une contribution au domaine vaste des onduleurs multiniveaux. Une variante particulière de l'onduleur multiniveaux est présentée, dans une configuration monophasée et triphasée. Cette variante est appelée convertisseurs à quatre quadrants reliées en série (SCFQ). Les deux particularités de l'onduleur présenté sont premièrement le fait que toutes les cellules de l'onduleur multiniveaux sont alimentées avec une tension continue identique, et deuxièmement que toutes les cellules sont réalisées avec des convertisseurs à quatre quadrants autonomes. Ce type de convertisseur à niveaux multiples est aussi nommé onduleur multiniveaux avec alimentation à tension continue symétrique, ou plus simplement onduleur multiniveaux symétrique.
Dans le cadre de ce travail, une théorie générale est établie pour ce type d'onduleurs. Un convertisseur continu-continu spécial est présenté, et qui est nécessaire pour imposer les niveaux de tension de chaque cellule élémentaire constituant le convertisseur multiniveaux. Tous les développements et méthodes sont documentés avec des équations mathématiques. Avec des logiciels modernes, adaptés au domaine de l'électronique de puissance, de nombreuses simulations des systémes ont été faites pour tester les différentes applications. La faisabilité des circuits des convertisseurs a été soulignée par une série de mesures sur les maquettes à puissance réduite. Les maquettes de chacun des convertisseurs ont été développées et réalisées dans le cadre de cette thèse.

L'application principale de l'onduleur multiniveaux proposée correspond au convertisseur d'entrée (AC-DC) pour une locomotive, afin de coupler cette dernière avec la caténaire. Au lieu de réduire la tension alternative élevée de la caténaire avec un transformateur à basse fréquence, encombrant et lourd, un redresseur-onduleur multiniveaux

sera directement couplé à la caténaire. Ceci est necéssaire pour amener la tension au niveau de celle des semi-conducteurs. Dans le même contexte, une solution configurable originale permet de définir une nouvelle solution pour des locomotives multicourants, c'est à dire qui peuvent fonctionner aussi bien sur une caténaire à tension alternative à tension élevée (15kV), que sur une alimentation continue à tension moyenne (3kV). L'onduleur multiniveaux présente des nombreux avantages pour ce genre d'applications. Trois configurations différentes d'un convertisseur de puissance pour locomotive basées sur le principe des multiniveaux sont étudiés et simulés dans un environnement de simulation complexe. Mais à côté des applications pour le circuit d'entrée de la locomotive, il y a beaucoup d'autres domaines d'applications pour l'onduleur multiniveaux symétrique. Parmi ces domaines j'aimerais mentionner le domaine du transport et de la distribution d'énergie électrique (FACTS, Compensateurs Statiques de Puissance Réactive, transformateurs de haute tension électroniques, etc.) et le domaine des entraînements industrielles. Mais à l'avenir certainement, avec la disponibilité de semi-conducteurs bon marchés et adaptés aux besoins des onduleurs multiniveaux, il y aura beaucoup plus d'applications, notamment dans la domaine de basse puissance, où les avantages d'une meilleure définition de la tension de sortie est exigée.

Zusammenfassung

Auf dem Gebiet der Leistungselektronik und Regelungstechnik ist die Mehrstufenwechselrichter-Technik eine relativ neue Forschungsrichtung. Die Anwendungsmöglichkeiten im Energie- und Antriebssektor sind gross. Noch viele Entwicklungen und Optimierungen in der Mehrstufen-Wechselrichtertechnologie werden aber gemacht, um daraus industrielle Produkte zu erzielen. In der Zukunft wird man die Mehrstufen-Wechselrichtertechnik sicher mehr einsetzen. Zum heutigen Zeitpunkt sind Mehrstufen-Wechselrichter selten in Produkten genutzt und kommen teils in eher exotischen Applikationen zum Einsatz. Dies ist insbesondere bedingt durch die Tatsache, dass die Anforderungen an die notwendigen Komponenten wie Halbleiter und Prozessrechner sehr hoch und deswegen sehr teuer sind. Man greift dabei auf die neueste Technologie zurück.
Doch die Neuentwicklungen im Gebiet der Leistungshalbleiter wie beispielsweise die IGBT, IGCT und in Zukunft auch die SiC-Halbleiter, aber auch die neuesten Materialien für Magnetkerne werden dem Mehrstufen-Wechselrichter einen entscheidenden Auftrieb für verschiedene Applikationen geben. Der Trend in der Industrie führt immer mehr weg von den schweren und grossen passiven Bauelementen zu neuen Stromrichtertopologien, die immer mehr Silizium-Schaltelemente aufweisen und mittels moderner Prozessortechnologie komplexe Steuer- und Regelalgorithmen ausführen.

Die hier vorgestellte Arbeit ist ein Beitrag zum weiten Forschungsgebiet der Mehrstufen-Wechselrichter. Eine spezielle Variante des Mehrstufen-Wechselrichters wird gezeigt, in der einphasigen aber auch in der dreiphasigen Konfiguration, genannt die in Serie geschaltenen Vierquadrantensteller (SCFQ). Die beiden Eigenheiten des hier vorgeschlagenen Mehrstufen-Wechselrichtertyps sind erstens, dass alle Stufen des Wechselrichters mit einer äquivalenten DC Spannung versorgt werden und zweitens, dass alle Stufen aus einem elementaren Vierquadrantensteller bestehen. Dieser Typ von Mehrstufen-Wechselrichter nennt man auch Mehrstufen-Wechselrichter mit symmetrischer DC Speisung oder kurz symmetrischer Mehrstufen-Wechselrichter.
Eine allgemeine Theorie wurde für diesen Wechselrichtertyp aufgestellt. Ein spezieller DC-DC Steller wird vorgestellt, welcher für die Speisung der Vierquadrantensteller verantwortlich sind. Dieser DC-DC Steller liefert eine konstant geregelte DC Spannung. Auf aktueller Simulationssoftware wurden viele Simulationen gemacht, um die verschiedenen Anwendungsfälle zu testen. Die Machbarkeit der untersuchten Schaltungen wurde mit einer Serie von Messresultaten untermauert. Die Messungen wurden mithilfe von Konvertern gemacht, die im Rahmen dieser Arbeit hergestellt wurden.

Die Hauptanwendung des hier vorgeschlagenen Mehrstufen-Wechselrichters ist die Netzankopplungs-Leistungskonverter für Lokomotiven. Anstatt mit einem schweren Niederfrequenztransformator die hohe Spannung des Bahnnetzes herunterzusetzen, um eine brauchbare tiefere Spannung für die Halbleiter zu erhalten, wird ein Mehrstufenwechselrichter eingesetzt. Dies ist in Hinblick auf die heutigen Trends zur Leichtbauweise ein entscheidender Vorteil. Der Wechselrichter ist nun direkt mit dem Bahnnetz gekoppelt. Der Mehrstufenwechselrichter bietet für dieses Anwendungsgebiet einige entscheidende Vorteile. Im Rahmen dieser Anwendung wurde eine spezielle Variante entwickelt, der konfigurable Mehrstufen-Wechselrichter. Dieser erlaubt es der Lokomotive, sich an ein Hochspannungs-AC-Netz (15kV) zu koppeln, aber auch der Betrieb an einem

Mittelspannungs-DC-Netz (3kV) ist möglich. Drei Konfigurationsvarianten wurden entwickelt und in einer vollständigen Simulationsumgebung simuliert. Neben dem Anwendungsgebiet für die Lokomotiven gibt es aber viele andere Anwendungsmöglichkeiten für den symmetrischen Mehrstufen-Wechselrichter. Ich möchte dabei das Gebiet der Energieverteilung ansprechen (FACTS, Blindleistungskompensatoren, elektronische Hochspannungstransformatoren, etc.) und industrielle Antriebe. Jedenfalls werden in Zukunft billigere Halbleiterschaltelemente erhältlich sein, welche an die Bedürfnisse der Mehrstufenwechselrichter angepasst sind. Dann werden noch mehr Anwendungen realisierbar, auch im tieferen Leistungsbereich.

Contents

Chapter 1

Introduction

Up to now, multilevel converters have been applied in some very specialized fields of power electronics, such as broadcast amplifiers [1] and fast supplies used in plasma physics [2]. Nowadays many new applications are possible. This is due to the availability and low price of high speed semiconductor devices [3], able to switch several kilovolts. The use of more semiconductor devices instead of heavy passive components [4] like transformers and inductors are a general trend observed in the fields of power electronics. New magnetic material for transformers enable developments for medium power transformers with medium switching frequency.
Applications in high power traction systems are of special interest for instance the $16\frac{2}{3}$Hz, 15kV single-phase system in the German, Austrian and Swiss railways. The present drive solution uses a heavy low-frequency transformer to reduce the input voltage and a classical bi-directional converter connected to the DC link. The low quality of the converter output voltage has the consequence that low frequency filters must be used, taking a lot of space and causing additional weight. The proposed single-phased multilevel-converter (ML-converter) topology replaces the heavy transformer due to the direct coupling to the catenary and allows a reduction of all filtering elements. But not only the traction application is an interesting field for the multilevel converter topology.
This work focuses on a special type of the multilevel converter topology, called series-connected four-quadrant converters (SCFQ) [5] [6] [7]. Each four-quadrant converter of the SCFQ multilevel converter is fed by an identical DC voltage. This kind of feeding for multilevel converter is called symmetrical feeding. To create the symmetrical feeding of a multilevel converter, many types of feeding methods are discussed, but the emphasis is on feeding by a DC-DC converter. It allows a two-quadrant operation, having always a positive voltage, but the current can be positive or negative. The thesis consists of six chapters. They have the following contents:

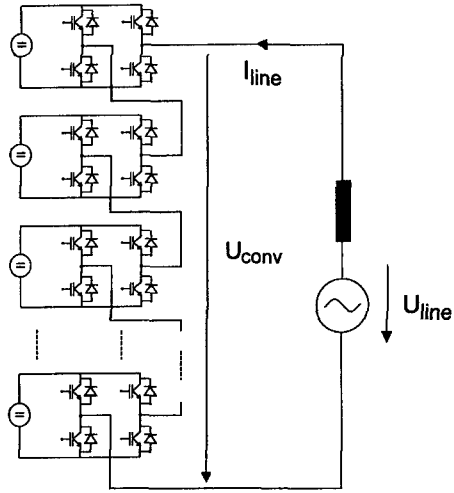

Figure 1.1: The multilevel converter with symmetrical DC feeding

Chapter 2 (At this point I want to remind the reader that this introduction is the first chapter) talks about the SCFQ multilevel converter. The SCFQ is compared with two other existing multilevel types. Different feeding methods for the four-quadrant converters are discussed, like the feeding from three-phase and single-phase AC voltage power lines and from DC links by using DC-DC converters. Two modulation methods (step modulation and PWM modulation) are defined and optimized for the multilevel converter. For the control of a multilevel converter, a novel control scheme has been developed. The control by a monophasor referenced to a rotating coordinate system. Of course all the developments have been tested on a laboratory prototype. More of this can be seen on page 7.

Chapter 3 presents the SCFQ multilevel converter in a three-phase configuration. Two special features for this converter must be mentioned: Firstly, the converter can generate higher voltages than the semiconductor blocking voltage and thus can be used to supply high-power industrial drives. Secondly, the converter voltage quality is much better than the quality from traditional converters. This advantage can be used to drive motors that need a superior voltage quality or motor with very low inductance. For this new converter type, a special vector modulation is presented, allowing a minimization of switching losses. The developements have been tested on a prototype driving an induction motor. Chapter three starts at page 59.

Chapter 4 shows the examined DC-DC converter topology. For the feeding of the four-quadrant converters in the SCFQ-configuration from a DC-link, a special type of hard-switched DC-DC converter with galvanic insulation is presented. The DC-DC converter has a controlled output voltage and is able to operate in two quadrants: The output voltage is always positive, while the current can be reversible. New modulation and control methods have been studied for this DC-DC converter, in operation with a

SCFQ multilevel converter. The modulation and control methods are validated on an experimental prototype, to be seen on page 99.

Chapter 5 informs about multilevel converter systems used for the particular application as a front-end AC-DC converter in locomotives. The main idea is to replace the heavy low-frequency transformer and to reduce all passive filtering elements. These new application possibilities present many advantages compared to the classical solution. Three different types of front-end converters have been developed and tested on a complex simulation environment. This chapter starts at page 173.

Chapter 2

Single phase multilevel converter

Single phase multilevel converters can be used in several applications. The first application, where multilevel converters were used in a high power field, were power supplies for broadcast transmitters. The broadcast transmitters need a very high voltage (for instance 60kV with an instantaneous power of about 10MW), which could not be generated by classical solid-state converter topologies. This is due to the fact that the voltage blocking capability of semiconductors is limited. Also the supplies do need a very good voltage definition in order to allow a transmission with little noise. The voltage has to be controlled very precisely and needs fast $\frac{du}{dt}$ slopes. These special specifications for a power converter made the multilevel converter unavoidable for this application. Some other application fields followed, like voltage sources for accelerators used in plasma physics. These applications fields are rather exotic and the typical clients did not fear high costs for that kind of solutions. Nowadays, thanks to the availability of cheap and faster high-power semiconductors, more and more applications can be found, where the multilevel converter can replace a classical solution. The main features of the single-phase multilevel design are:

- The use of solid-state power switches like power MOSFETS, IGBT (Insulated gate bipolar transistor) or IGCT (Integrated gate commutated thyristor)
- Totally controllable output voltage, generation of medium-frequency output waveforms with high power (20kHz fundamental AC frequency at 10MW). Thanks to adapted modulation schemes the resulting output switching frequency is a multiple of the switching frequency of each semiconductor
- All low-frequency elements like frequency filters, transformers and inductors can be avoided or reduced in size. This allows the reduction of weight and space. In many cases this is an important point to avoid high system costs.
- The high voltage quality combined with a powerful DSP processor for the control and modulation allows efficient active filtering applications or static VAR compensation. Powerful control performance can be implemented

The main drawback of the multilevel converter is especially the high complexity of such a system. Many switches are needed, the systems reliability depends on the quality of the semiconductors. The chapter shows three basic single-phase multilevel converters and the modulation methods for those topologies.

2.1 Introduction

The basic principle of multilevel converters is a series-connection of a certain number n of DC voltage sources U_{dc2}. These independent DC voltage sources can now be turned on and off, in order to achieve a resulting multilevel voltage U_{conv} with a maximal number of steps n. This resulting voltage cannot be any kind of voltage, it will always be a multiple of an independent DC voltage U_{dc2}. So if a particular voltage waveform has to be generated (for instance a sine wave), the sinewave will not be perfect, it will be a quantization of the desired waveform with the quantization step U_{dc2}.

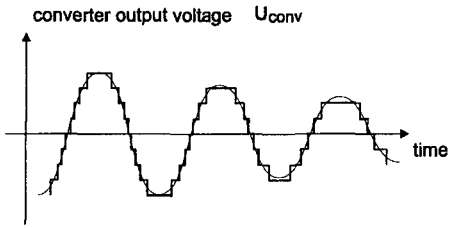

Figure 2.1: Typical waveform from a multilevel converter

In the Figure (2.1) it can be seen, that a reference function is quantified by a discrete voltage waveform with a certain number of steps. So the converter output waveform is expressed by Equation (2.1):

$$U_{conv} = \sum_{i=1}^{n} U_{dc2(i)} \tag{2.1}$$

The output voltage is the sum of the partial DC voltages, which are turned-on. In this thesis, only the symmetrical multilevel converters are considered. The multilevel converters with assymmetrical feeding are presented in [8] and [9] and are not discussed in this work. A symmetrical multilevel converter is defined by the fact that all feeding DC voltages are equivalent:

$$U_{dc2} = U_{dc2(i)} \qquad i = [1, 2, .., n] \tag{2.2}$$

The maximal voltage, which can be generated by a symmetrical multilevel converter, is:

$$U_{conv(max)} = n \cdot U_{dc2} \tag{2.3}$$

while n gives the number of steps used. A multilevel converter needs a certain number of DC voltage sources. Not in all the cases these have to be galvanically separated. Figure (2.2) shows an example of a ML-converter using sources connected in series.

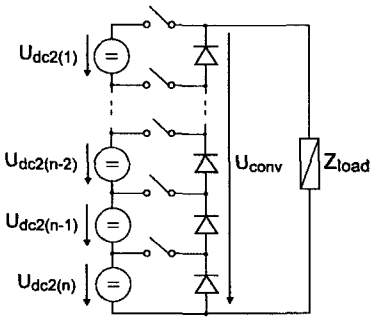

Figure 2.2: Basic structure using a ladder of voltage sources

An other typical multilevel converter structure can be realized by using a set of galvanically separated voltage sources. These voltage sources can afterwards either be turned-on or turned-off in order to generate the converter output voltage U_{conv}.

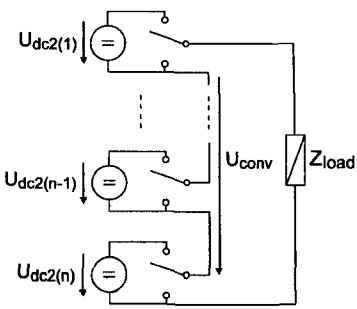

Figure 2.3: Basic structure using a number of independent voltage sources

The main drawback of this structure is the fact that there is no possibility to generate a negative voltage, therefore real AC voltage generation is not possible. If the load needs an AC voltage, it is possible to put a large decoupling capacitor into the load circuit. This capacitor would be charged to the average value of the converter voltage. In this way, the load will see an AC voltage. The next topology presents a ML-converter which is able to generate real AC voltages:

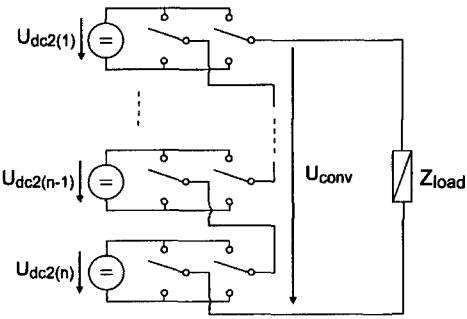

Figure 2.4: Basic structure using a number of voltage sources with full-bridges

This topology needs the same number of voltage sources, but it can generate actively the positive half-period of the converter voltage U_{conv} with up to n steps, and can generate the negative half-period as well. The implementation of such a converter is done with four switches per DC source, in a so called full-bridge configuration or four-quadrant converter. The middle points of each half-bridge in the full-bridge configuration is interconnected in series with the neighbor full-bridge converter. This topology is the so called series-connected four-quadrant converter (SCFQ) multilevel converter.

2.2 Schematics of single-phase multilevel converters

The first schematic proposed for the realization of a single-phase multilevel converter is the series-connected four-quadrant converter topology (SCFQ) as shown in Figure (2.4). The topology is quite simple and consists of four-quadrant converters (also called full-bridge converters). The four-quadrant converters are fed by a constant DC source on its DC side. So each four-quadrant converter can generate a positive or a negative voltage step, but also the zero voltage.

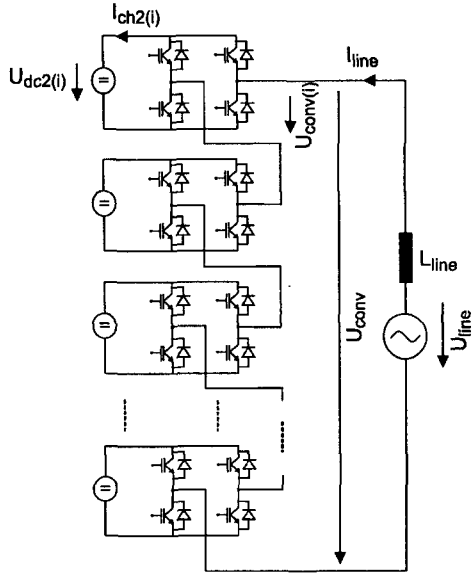

Figure 2.5: Single-phase multilevel converter realized by the series-connection of four-quadrant converters (SCFQ)

The AC side of the four-quadrant converters are afterwards connected in series over the AC side as shown in Figure (2.5). All the DC sources are galvanically insulated of each other. This allows a free operation of the switches of the four-quadrant converters. The features of this topology are listed below:

- The DC voltages for the feeding of four-quadrant converters have to be all generated separately and with a galvanic separation. This can be done either by low-frequency transformers from an AC line, but also from a DC source with isolating DC-DC converters. The topology needs a complex feeding setup, but there will not be any voltage fluctuation between the DC voltages.

- The topology is perfectly symmetrical, there are always two semiconductor voltage drops per 4Q-converter, regardless to the generated output voltage. By using an adapted modulation scheme, all the voltage sources are loaded symmetrically.

- Another advantage to be lined out is the lack of high-voltage elements on the DC side of the ML-converter. No high-voltage capacitors are needed with this topology, the high voltage is perfectly shared over a large number of steps. The high-voltage capability of this converter is limited only by the isolation transformer to generate the DC voltages

The SCFQ-topology presents many advantages for traction applications and is examined thoroughly in this thesis.

A second method to realize a multilevel converter consists in the principle of the imbricated cells. The basic schematic is given in the Figure (2.6). This topology is described in details in the publications [10], [11] and [12]. The switches are arranged in two pairs (s_{11}, s_{21}) and (s_{12}, s_{22}). Like in the case of using an half-bridge converter, the switch pair (s_{11}, s_{21}) and (s_{12}, s_{22}) have to be in a complementary state. A blanking time must be respected (Comparable to the blanking time used for half-bridge commutation) in order to avoid a short-circuit of the feeding voltage.

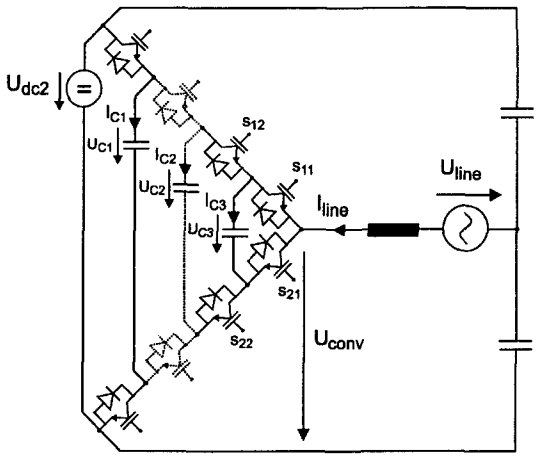

Figure 2.6: Single-phase multilevel converter realized by imbricated cells

The main goal of this converter topology is to use only one DC supply voltage U_{dc2}. All the other voltages $U_{C(n)}$ will not be active, there shall only be a capacitor instead of a DC feeding voltage source. The idea is to pre-charge the capacitors at the partial voltage values:

$$U_{c(k)} = \frac{n-k}{n} \cdot U_{dc2} \qquad k = [1, 2, .., n-1] \tag{2.4}$$

The voltages on the capacitors shall afterwards be maintained by an adapted modulation scheme. The modulation scheme must guarantee that the capacitor input current and output current have always the same average value. By doing this, the capacitor voltages will not fluctuate. This must be guaranteed even for low frequencies, when a variable speed drive is used. But the implementation of such a modulation strategy is not a trivial problem and has been a research activity in the framework of the project [11]. Each capacitor is connected between two pairs of switches, for instance $C3$ for the pair (s_{11}, s_{21}). The current in this capacitor can now be either I_{line}, $-I_{line}$ or zero. Thus, the voltage on the capacitors is stable if:

$$\frac{d}{dt}\overline{U}_{c(k)} = \int_O^T I_{c(k)} dt = 0 \tag{2.5}$$

The Figure (2.7) shows the working principle of the imbricated cells converter. The converter has only four switching elements and is capable to generate three different voltage levels, if $U_c = 0.5 \cdot U_{dc2}$.

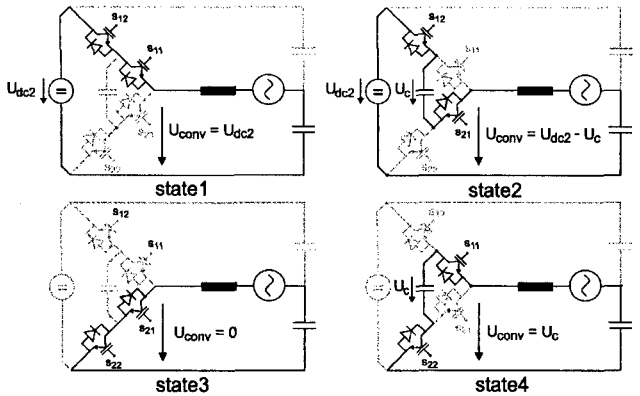

Figure 2.7: Commutation sequence of a two-level imbricated cells converter

The typical modulation sequence is *state*1 – *state*2 – *state*3 – *state*4. During a modulation cycle, the current in the capacitor can be positive, negative and zero. In the two states 2 and 4, the current of the capacitor I_C will be equal to the load current I_{line}. In *state*2, the line current I_{line} will be a positive charging current of C. In *state*4, the current is inverted and so will be negative. The output voltage will be the same value, if the following equation is valid:

$$U_c = \frac{1}{2} \cdot U_{dc2} \tag{2.6}$$

In the other two states, the current through the capacitor is equal to zero. In a PWM modulation strategy, it must be alternatively changed between *state*2 and *state*4. If the duration of these two states is the same, the capacitor voltage will remain constant. This allows the operation with low frequency currents or even with DC current sources as a load. In a chopper mode, where the multilevel converter acts like a DC-DC converter towards another voltage source decoupled by an inductance, the voltages on the capacitors will be symmetrized automatically. For instance, if the following relation is valid:

$$U_c = \frac{1}{4} \cdot U_{dc2} \tag{2.7}$$

and the voltage source on the load side is assumed being zero, the load current generated in the *state*2 will be higher than the load current generated in *state*4. This means that the capacitor C will be more charged in the *state*2 than discharged in the *state*4. This effect will cause an natural symmetrization of all the capacitor voltages.

Anyway the impedance of the load L_{line} has a big influence on the natural equalization of the capacitor voltages. In some cases a filter for each capacitor C has been used to

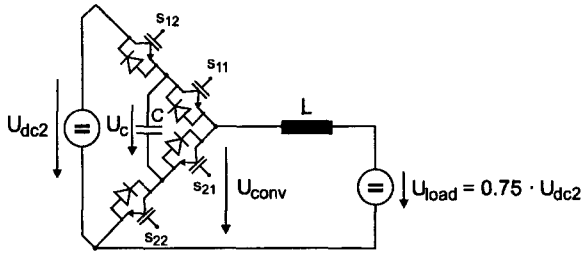

Figure 2.8: Imbircated cells ML-converter working as a chopper

get rid of the switching frequency and the harmonics. For AC drives with high line impedances, the symmetrization problem of the voltage is not easily solved, some active symmetrization techniques have to be used.

The third realization of the multilevel converter presented in this overview is the topology with the diode clamping of the neutral points. The basic topology was presented the first time in [13]. Multilevel NPC converters are proposed in [14]. This topology is well-known for three-phase applications, where three different voltage levels per phase voltage can be generated. In this example, the topology is given for a single-phased implementation in a multilevel structure.

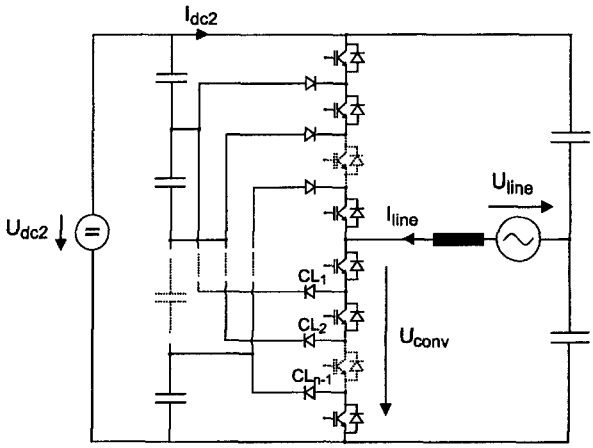

Figure 2.9: Single-phase multilevel converter realized by clamping all the neutral points by diodes

This topology has some problems which have to be solved before implementing a solution. It is considered that the topology is fed by only one voltage source U_{dc2}. All

the other partial voltages are generated by a ladder of equal capacitors. This setup can be seen in Figure (2.10). If this converter topology is used to feed variable-speed drives, the line current I_{line} can be very low frequency, it can even be a DC current. By looking on the switching sequences given in Figure (2.10), it can be seen that the multilevel converter will not generate an AC voltage for a while, but a DC voltage like a chopper. This can be achieved by changing constantly between the two converter *state2* and *state3*. In this way, the capacitors C_3 and C_4 will be constantly discharged by the line current I_{line}. The line current I_{line} is seen each time as discharging capacitor current for the capacitor C_3 or C_4, depending on the chosen state. The conclusion for this effect is that for low-frequency drives, these capacitors have to be very big. But a DC current is not tolerable, otherwise the capacitors must be infinitely big. If instead of capacitors controlled voltage sources could be used, the problem is solved, but the system is much more expensive and complex.

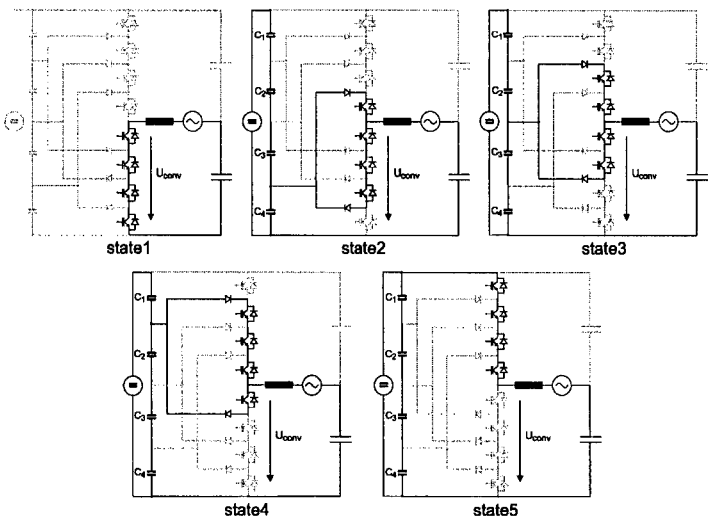

Figure 2.10: Switching sequence with a five-level NPC mulitlevel topology

Another observation on this topology can be made on the clamping diodes CL_1 to CL_{n-1}. While the lowest clamping diode CL_{n-1} will only have to block a voltage equal to U_{dc2}, the highest clamping diode CL_1 will have to block the voltage $(n-1) \cdot U_{dc2}$. So actually, only the semiconductor switches with its anti-parallel diodes will share the same voltage. If there are many steps, the highest clamping diode will have to block a very high voltage (up to 70kV), comparing to the lowest one. Diodes with high-blocking voltage do exist, but there on-state characteristics will cause large losses (high on-state voltage). The NPC multilevel solution remains only usable if the number of steps is limited.

2.3 Feeding of the multilevel cells

2.3.1 Feeding from DC voltage source

Due to the nature of the SCFQ multilevel converter, the converter cells have to be fed by an individual DC voltage, which usually has to be isolated from ground by at least the maximal generated voltage of the multilevel converter. The multilevel converter output voltage composes its voltage from the individual DC voltages. If these are not galvanically separated there would be immediately a short-circuit. In some applications, these independent DC voltages are naturally at disposition. There are installations, where a several number of photovoltaic cells, DC current motors in power generation mode, fuel cells, etc. have to be converted into a three-phase voltage system. Often this is done to put their power into an existing power grid of 50Hz/60Hz. By using a multilevel structure it can even be possible to avoid the grid transformer, because the ideal voltage can be reached and there is only a decoupling inductance needed.
But there are many cases, where only one DC voltage is available. Typically in many locomotives and other mobile systems only one DC link can be found to feed the motor converter. In these cases, the DC voltage has to be generated by a number of DC-DC converters. The DC-DC converters can be realized using a medium-frequency (8-12kHz) or high-frequency (40-100kHz) transformers with high-voltage isolation, in order to reduce the weight. The needed winding ratio between the primary and the secondary side will be $w_r = 1$. In the most applications, the medium-frequency transformer would be ideal because the weight gain is considerably high while the losses are not to important. A typical DC-DC converter, which is well studied and could be used for a multilevel converter is the series-loaded series-resonant DC-DC converter [15]. Its operation mode consists of the alternate closing of a pair of transistors $T1$, $T2$, $T3$ and $T4$. The excitation of the resonant LC circuit with the series-connected passive elements L_{R1}, C_R and L_{R2} will generate a resonant current. The switches are controlled in a way that they always turn-on when the resonant current passes through zero. The detailed description of the modulation methods can be found in [16] and [17].

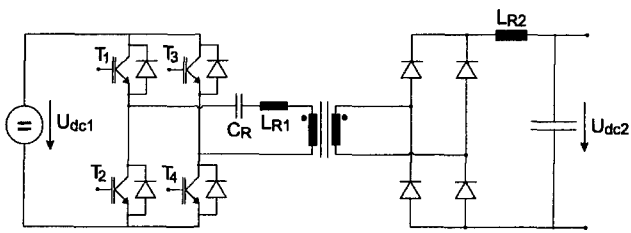

Figure 2.11: Single-quadrant operated DC-DC converter for resonant current operation

This DC-DC converter is usually used with rather high switching frequencies (around 50kHz) might be suitable for many applications and does not generate much losses. Many other resonant DC-DC topologies can be used for the feeding of the four-quadrant converters, an example is [18] and [19]. Every four-quadrant converter has to be equipped with one of those converters. The next Figure (2.12) shows a setup, where there is only

one converter on the primary side with n transformers. This feeding topology can be used, if the overall system power can be handled by one single four-quadrant converter, using a medium or high frequency to feed the power transformers.

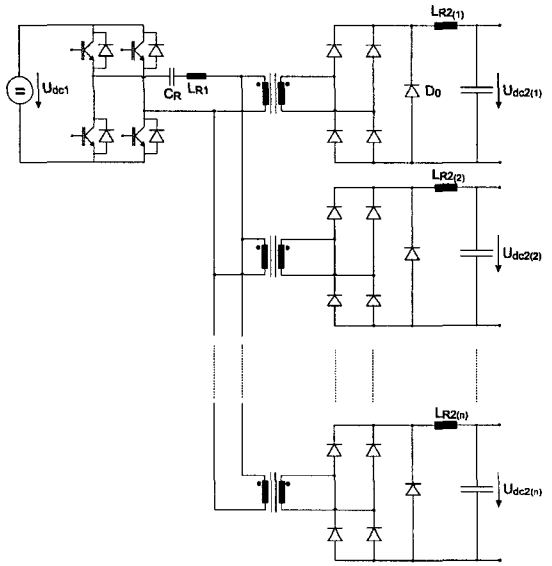

Figure 2.12: Series-connected resonant DC-DC converters with additional clamping diode

The additional clamping diode D_0 is introduced to provide a free-wheeling operation with only one voltage drop over the semiconductors and thus reduces on-state losses. These topologies unfortunately do not allow the possibility of reversing the power direction. So the multilevel converter can not work in power recuperation mode. A resonant DC-DC converter topology for the feeding of ML-converters is presented in the next Figure (2.13), also shown in [16].

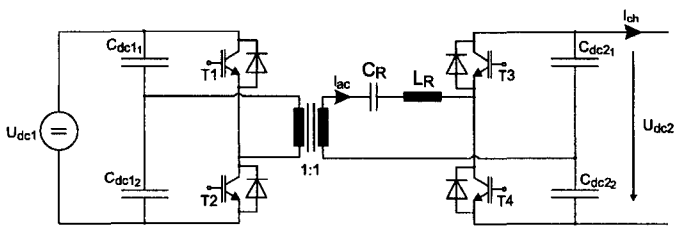

Figure 2.13: Resonant DC-DC converter for two-quadrant operation

This half-bridge DC-DC converter topology can be used for ML-converters, where the

power must flow in both directions. It is capable to transfer the energy in the two ways. The load current I_{ch2} can be positive or negative, which allows a two-quadrant operation. The switches $T1$ and $T3$ are switched on and off in alternatively with the switches $T2$ and $T4$. The resonant circuit L_R, C_R is designed in the way that the resonant frequency is the same as the switching frequency f_p of the DC-DC converter.

$$f_p = \frac{1}{2\pi\sqrt{L_R C_R}} \tag{2.8}$$

Two AC voltages are generated on the resonant LC circuit. The difference between the two voltages U_{dc1} and U_{dc2} will so be applied to this LC circuit and a resonant current is generated. The input and output capacitors are connected as a bridge with middle point used as the AC terminal. They must be chosen much bigger than the resonant capacitor. This avoids parasitic oscillation. This half-bridge configuration with only four semiconductors allows a reduction of the on-state losses by only having one semiconductor voltage drop over a current path. Another advantage is the lack of a DC current through the transformer, due to the termination of the AC link in the middle point of the capacitor bridges.

$$C_{dc2_1}, C_{dc2_2} >> C_R \tag{2.9}$$

The current I_{ac} will be sinusoidal with a frequency f_p, if Equation (2.8) is respected. This topology is useful, if the input and the output voltage is the same (or the voltage level is adapted by the winding ratio of the transformer). Unfortunately, the duty cycle of the generated AC voltages on the transformer and the LC circuit has to be controlled in order to avoid a saturation of the transformer [20].

The DC-DC converter proposed and studied in details in this thesis is proposed in chapter 4, page 99. This DC-DC converter allows not only a two-quadrant operation (bi-directional load current), but also a fully controllable DC output voltage. The controlled output voltage is in this way completely decoupled from the input voltage. Furthermore, modulation methods are proposed for reduced losses without the use of resonant topologies.

2.3.2 Feeding from low-frequency AC voltage grids 50Hz/60Hz

If a low-frequency AC source (single- or three-phased) can be used for the feeding and weight as well as volume of the setup are not a problem, the supplying can easily been done by a low frequency transformer with the needed number of secondary turns, shown in [1], [2], [21] and [22]. The voltages on the secondary side of the transformer are rectified by a rectifier bridge or another power converter into a DC voltage. The first figure shows a simple way to do the feeding by single-phase diode bridges to rectify single-phased voltages. Of course the rectifier bridge only allows an energy flow in one direction.

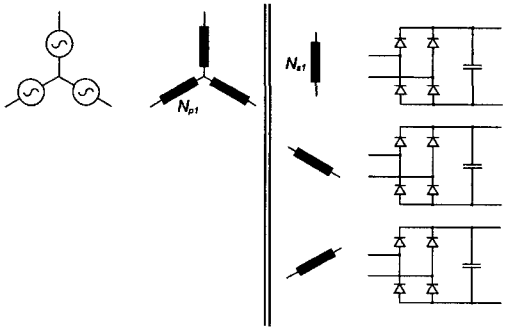

Figure 2.14: Multilevel converter feeding by single-phase diode bridges

If all the phases have to be charged symmetrically, the number of multilevel cells has to be a multiple of three. Otherwise, a three-phase rectifier for each multilevel cell has to be used. In this way there is no problem of symmetrical power sharing, independent of the number of multilevel cells. This is shown in Figure (2.15).

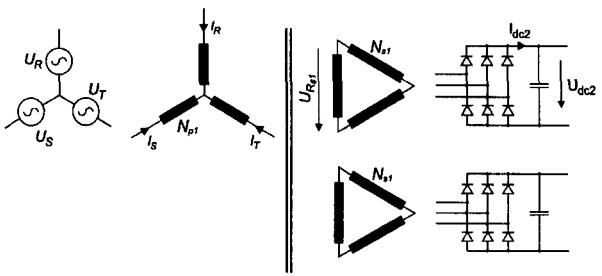

Figure 2.15: Multilevel converter feeding by three-phase diode bridges

In any case it is recommended to use the three-phase rectifier bridge. The single-phase rectifier generates each half-period a current peak. This current peak is non-sinusoidal waveform and can of course be found on both sides of the transformer. On the primary side the feeding network will be disturbed, while on the capacitor on the output of the rectifier bridge is charged by these current peaks. The ripple on the voltage U_{dc2} of the DC capacitor will twice the line frequency f_{line}, mostly 100Hz. If now the three-phase rectifier is used, the current peaks occurred by a diode half-bridge occur at 100Hz for each phase. Due to the fact that there are three phases, there will be a oscillation of 300Hz on the capacitors at load. So by using the three-phase rectifier, smaller capacitors can be chosen for the same voltage ripple on U_{dc2}. The rectifier bridges at least generate AC currents with no DC component on the primary side, but there is much low-order harmonic content. The proposed solutions with the rectifier bridges can be improved. The disadvantage of this solution is still the poor current quality by having non-sinusoidal

peak currents on the line side. The improved transformer topology must fulfill the two following points:

- The current taken from the grid on the primary side are must of course be sinusoidal, resulting a good power quality. If the currents cannot be sinusoidal, there should be at least an harmonic cancellation of low-order harmonics.

- On the other hand, the multilevel converter needs a high number of galvanically insulated ideal DC voltages sources. The desired voltage is achieved by adapting the winding ratio of the transformer coils.

If the currents are of poor quality, there are two main disadvantages: Firstly the primary side of the transformer does need a low-frequency filter so that the converter feeding system introduces fewer harmonics into the grid. The simulation shows insufficient current quality for high-power transformers. Secondly the transformer has to be designed for more power than is actually demanded from the power converter, in order to handle the peak currents. Otherwise there would be saturation effects causing excessive losses. So the basic idea is to use several secondary coils, each of them generating a phase-shift between the phase of the voltage and the current.

The proposed transformer circuit is using a special transformer winding configuration on the secondary side, taking advantage of the possibility to generate phase-shifted voltages on the secondary side of the transformer [21]: By having phase-shifted current demands from every rectifier bridge on the secondary side, the overall primary current has less harmonic content due to harmonic cancellation. The superposed current of the primary side has a more sinusoidal shape. The feeding topology below shows a solution, if the number of multilevel converter cells are a multiple of 2:

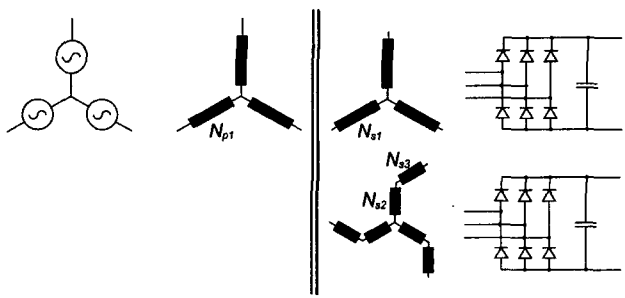

Figure 2.16: Multilevel converter fed by 12-pulse polyphase transformer

The upper coil in the star configuration does not generate any phase shift comparing to the primary side. But the lower one with the special middle-point connection generates a phase-shift of 30°. This generates two pairs of phase-shifted current peaks. For the whole transformer, there are twelve current peaks. That is why the transformer is called

12-pulse polyphase transformer. More details on these transformer types with simulations are given in Appendix B.

2.4 Modulation methods

There are several different methods to modulate a classical single-phase voltage-source inverter. Each of them can also be implemented on a multilevel converter. This is obvious, because the ML-converter consists of a series-connection of independent four-quadrant converters. The aim of the modulation is to generate a voltage output of the multilevel converter which follows as accurate as possible a referential function $k \cdot V_{ref}$, also called set value. Usually, this set value is sinusoidal. V_{ref} represents the sinusoidal function with the amplitude boundaries $[-1, 1]$. k is the modulation degree and is something like an weight factor for the reference function. The modulation should also work even if the referential function is not sinusoidal. This is an important fact if a active harmonic filter has to be implemented, or if the multilevel converter works on power lines, where the AC voltage is not sinusoidal at all. The ideal modulation method for a ML-converter can be described as follows:

- Easy implementation as processor algorithm or as digital state machine
- Very short delay time from the generated reference function to the switching signals
- Symmetrical distribution of the losses on all the switches and symmetrical power consumption from the feeding DC source
- Reduction of the switching losses to a minimum
- Very low harmonic content in the generated voltage

Of course, not every modulation method can present all the advantages at once. Depending on the application and the setup of the converter, it has to be decided which method has to be implemented. Two methods have been compared and tested.

2.4.1 Step modulation

A simple method to do the modulation is to approximate the desired output voltage by certain number of steps, shown in [23] and [7]. This is exactly the principle of an AD-converter: A reference function is quantified into a set of discrete values. Exactly this principle can be used for the multilevel converter. The output voltage will correspond to the number of four-quadrant converters generating a voltage (either positive, negative or zero): It can be said that the output voltage is:

$$U_{conv} = U_{dc2} \cdot \sum_{j=1}^{n} S_j \tag{2.10}$$

S_j represents the quantification functions, U_{dc2} is the supply voltage of the four-quadrant converters. To generate the quantification functions, a reference function is simply compared in parallel to a number of threshold values. After the comparison the switching patterns are generated. The value of these thresholds are at the arithmetic mean value between two voltage steps. So for each of the n full-bridge converters there must be a comparator. The Figure (2.17) shows the principle of operation:

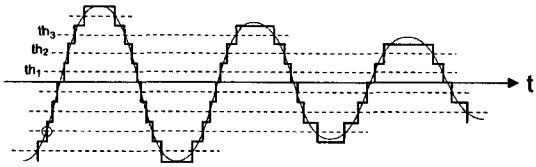

Figure 2.17: Typical waveform generated by the step modulation

The next Figure (2.18) shows an analog implementation of this modulation method. The Figure represents the schematics of a flash AD-converter. For each of the n steps, there is a comparator. The threshold values are generated by a resistance ladder or by constant voltages sources with the adequate values.

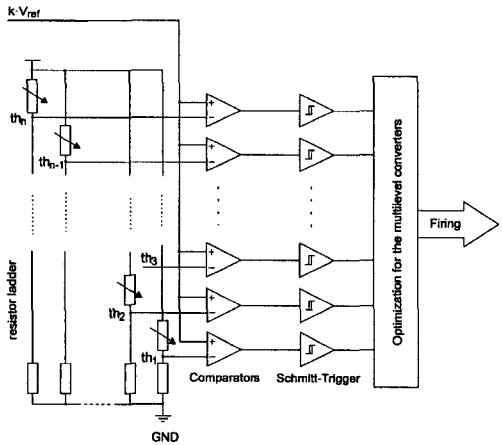

Figure 2.18: Principle of the modulator for the step modulation

The same principle is used for a digital implementation. The only disadvantage of the digital implementation is the resolution of the modulator: If the chosen resolution is $res = 8Bit$, there are 256 steps where the threshold values can be set. For an equal distribution of the threshold values, the Equation (2.11) must be respected:

$$mod\left(\frac{res}{2n}\right) = 0 \tag{2.11}$$

For instance, in the case of a $n = 12$ step multilevel converter, the are no equal distributed threshold values. To avoid a non-equal distribution of these values, it is advised to use a modulator resolution of 12 or 16 Bit.
In Figure (2.18) it can be seen that the switching signals must be optimized for the multilevel converter. The following algorithms can be followed to symmetrize losses of the multilevel converter. The first method is self-explaining with Figure (2.19). The method

consists of a simple turn-on and turn-off in series from one four-quadrant converter (4Q-converter) to the other.

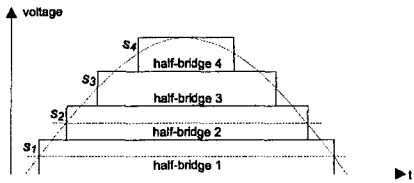

Figure 2.19: Principle of the modulator for the step modulation

This modulation optimization is simple, it only has to be ensured that there is never a negative voltage from a 4Q-converter that is cancelling a positive voltage. If it is considered that the current is in phase with the multilevel converter voltage, it can be seen that the first half-bridge is conducting the most of the time the full current. So the RMS of the current seen by each 4Q-converter is different. On the other hand, the switching losses are the smallest for the first 4Q-converter, it has only to switch a small current at 12.5% of the full current. This means that the losses are not shared equally on all the individual converters. The following Table (2.1) gives an overview of unsymmetrical distribution of the losses:

Half-bridge	Conduction losses	Commutation losses	Total losses	Percentage
1	132.6W	0.6W	133.2W	0.27%
2	126.3W	1.3W	127.6W	0.25%
3	108.7W	2.1W	110.8W	0.22%
4	69.1W	3W	72.1W	0.14%

Table 2.1: Step modulation losses A

The example given in this table is concerning a ML-converter with $n = 4$ steps, a fundamental frequency of 50Hz, with the overall power of 50kVA (625V/80A). Of course the step modulation method generates hardly any switching losses at low frequencies (50Hz). But it has to be considered that the converter is feeding high-speed motors with fundamental frequencies above 500Hz. To avoid the non-equal power share, a step modulator is used with load sharing, as described in [2] and [24]. The Figure (2.20) shows the principle.

To compare this method with the precedent version, the losses have been calculated and compared. The Table (2.2) shows the results. It can be seen that the RMS current for each cell is better distributed, but in this case the switching losses are worse distributed.

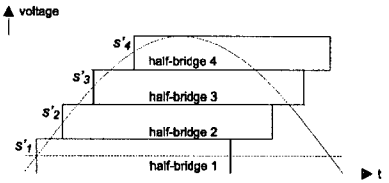

Figure 2.20: Load sharing

Half-bridge	Conduction losses	Commutation losses	Total losses	Percentage
1	100.6W	1.5W	102.1W	0.2%
2	117.6W	1.7W	119.3W	0.24%
3	117.6W	1.9W	119.5W	0.24%
4	100.6W	2W	102.6W	0.2%

Table 2.2: Step modulation losses B

Due to the high turn-on losses with a high current, the fourth half-bridge takes an important part of the switching losses. This causes a superior stress in the recovery diode of the first element. The circuit of the multilevel converter was given in Figure (2.5). If the frequency of the generated voltage is risen, the commutation losses will become very important. To distribute the power losses equally over all cells, the third method proposes a rotating switch pattern after each period of the fundamental sine-wave. Due to the high thermal capacity of the converter, the losses will be perfectly shared. The principle is shown in Figure (2.21).

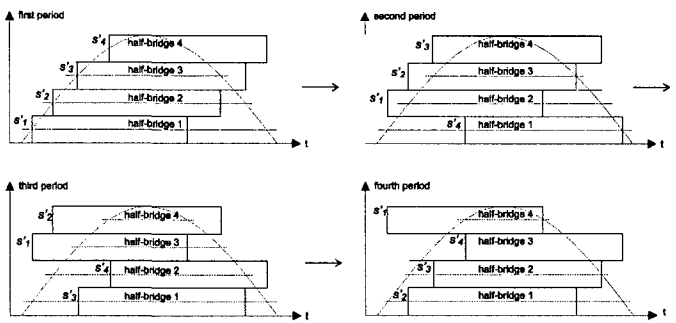

Figure 2.21: Rotating commutation patterns each period

If the modulation is executed with the full modulation degree, all the 4Q-converters are used. The upper 4Q-converter (modulation function s_n) is related with the lowest one (modulation function s_1). The function s_{n-1} will be correlated with s_2, etc. If the

rotation	$s_1, .., s_{\frac{n}{2}}$	$s_n, .., s_{\frac{n}{2}+1}$	$s'_1, .., s'_{\frac{n}{2}}$	$s'_n, .., s'_{\frac{n}{2}+1}$
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Table 2.3: Rotation logic table

number of steps n is not an even number, the middle step function $s_{\frac{n}{2}+1}$ will not be changed. The next Figure (2.22) illustrated the multilevel converter, where only three steps are active. The middle step 2 is not changed.

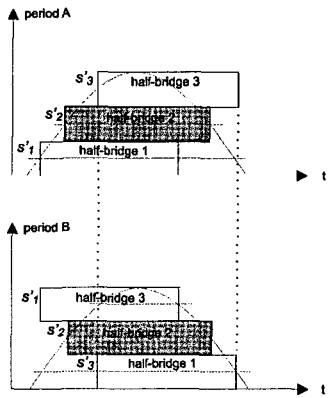

Figure 2.22: The middle step is not changed

The sequential analysis of the commutation signals allows the generation of a logic for this optimization. For this reason, the truth table with the state "rotation" has to be considered. The state rotation must be stored in a flip-flop.

The algorithm below will execute a rotation of the switch patterns. The input are the original switch signals s_1 to s_n.

```
for i = 1 to round(n/2)

s'(i)       =!rotation*s(i) + rotation*s(n-i+1)
s'(n-i+1)   =!rotation*s(n-i+1) + rotation*s(i)

end(for)
```

The next step is to introduce a second rotation of the already symmetrized modulation functions s'_1 to s'_n. This function must be done by a counter, which starts at zero, when

the first period is passed. Each period, the counter increments until the number n of 4Q-converters is passed. This function does not depend on the fact that the number n of 4Q-converters is even or odd. To execute this algorithm, it is important to have a digital signal giving an impulse each time the period changes.

```
repeat

read(impulse)

    if impulse = 1 then period := period + 1 end(if)

    if (period > n) then period := 0 end(if)

        for i = 1 to n
        s'(i) = s'(mod((j+period)/n))
        end(for)

until (end modulation)
```

The next steps concerning the step modulation are talking about the generated harmonics and the transfer function of the step modulation. The aim is to express an analytical transfer function and calculate the ideal angles of step modulation. There are three different usable methods to optimize the harmonics:

- The width of the steps are all equal, and the height of the steps is varied (this would demand a variable DC supply voltage)
- The height of every step is equal (fed by a constant DC voltage source) but the width is variable
- Both, width and height can be optimized

In is not in the interest of the multilevel converter principle to vary the feeding DC voltages $U_{dc2(i)}$. This is implementable with a voltage-controlled DC-DC converter, but the control performance of the output voltage of a DC-DC converter is limited. It depends especially on the output capacitor of the DC-DC converter. Details on the voltage-controlled DC-DC converter can be found in Chapter 4. To have a mathematical base, the fourrier series are developed of a ML-converter with n 4Q-converters. The Figure (2.23) shows the variable parameters.

The mathematical development can be seen in Appendix A.1. The next Expression (2.12) gives all the harmonics in relation with a timebase t and a fundamental frequency ω_{line}:

$$U_{conv}(t) = \frac{4U_{dc2(i)}}{\pi} \sum_{j=odd}^{\infty} \sum_{k=1}^{n} cos(j \cdot \varphi_{(k)}) \frac{sin(j\omega_{line}t)}{j} \tag{2.12}$$

The amplitude of a harmonic with the frequency $p \cdot n$ is given by (2.13):

$$\hat{U}_{harm(p)} = \frac{4U_{dc2(i)}}{\pi} \sum_{j=1}^{n} \frac{cos(j \cdot \varphi_{(k)})}{j} \tag{2.13}$$

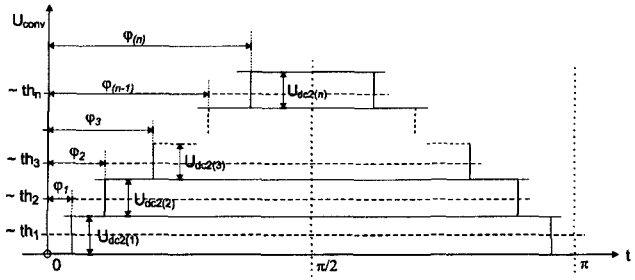

Figure 2.23: Generalized step modulation waveform

Depending on the modulation degree k, a certain number of steps of the n steps are activated. The modulation degree k is defined as follows for the multilevel step modulation:

$$k = 1 \Longleftrightarrow \widehat{U}_{conv} = n \cdot U_{dc2(i)} \tag{2.14}$$

So over-modulation means that the modulation functions amplitude is higher than the maximal number of steps. By an equation it has to be found out how many steps are active, depending on the modulation degree k, the number of steps n. The threshold values $th_{1,2,..,n}$ are considered to be at equal distance.

$$th_{(1,2,..,n)} = \pm\frac{1}{2n} \pm (i-1) \cdot \frac{1}{n} \qquad i = [1\,..\,n] \tag{2.15}$$

The threshold values are always in pairs with a positive and a negative one. There are $2n$ threshold values. The number of active steps is given by the value n_{step} and is defined in the Equation (2.16):

$$n_{step} = round(k \cdot n) \tag{2.16}$$

The firing angles are calculated after knowing how many steps are active. The Equation (2.17) shows the computing of these angles.

$$\varphi_{(i)} = \arcsin\left(\frac{th_{(i)}}{k}\right) \qquad i = [1\,..\,n_{step}] \tag{2.17}$$

If the Equation (2.16) is not used or the threshold values are not distributed with equal distances, there is an easy way to find out if the calculated angle is valid or not:

$$Im\left[\arcsin\left(\frac{th_{(i)}}{k}\right)\right] = 0 \qquad i = [1\,..\,n_{step}] \tag{2.18}$$

The easiest way to reduce the harmonics is of course to take an important number of steps. But in the most applications a ideal value between the number of steps and the tolerated harmonics have to be found. The idea is to see if the equal distance between the threshold values for the comparator in Figure (2.18) is the ideal method. To verify this, the following procedure has been followed:

- The firing angles (corresponding to a threshold value) are varied in small steps around the values given by the equal distribution of the steps
- Calculation of the THD value of the given sine-wave
- Find the minimal THD value to find the ideal firing angles

The THD (total harmonic distortion) is a value expressing the energy of all the harmonics in comparison with the fundamental sine wave. All the calculations have been done with a modulation degree of $k = 1$. The definition is given in Equation (2.19):

$$THD[\%] = 100 \cdot \sqrt{\frac{\hat{U}_{conv}^2 + \sum_i \hat{U}_{harm(i)}^2}{\hat{U}_{conv}^2} - 1} \tag{2.19}$$

$\hat{U}_{conv}$ is the amplitude of the output voltage of ML-converter (the amplitude of the fundamental sine wave), while $\hat{U}_{harm(i)}$ are the amplitudes of the harmonics of the same voltage. A numerical analysis have been done as described above. Two angles have been optimized for a multilevel converter using $n = 2$ full-bridge converters. To reduce the complexity of the analysis, only the harmonics to the $i = 250$ order have been taken into account. In any case, the harmonics of a higher order have a negligible influence. The result of this optimization is shown in Figure (2.24).

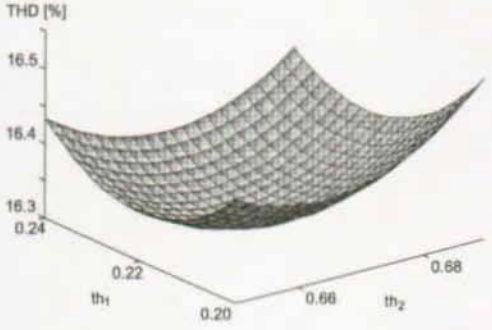

Figure 2.24: Optimal firing angles for a n=2 ML-converter

It is surprising to see that the optimal angles are not on the thresholds on the equal distance $arcsin(\varphi_{1,2}) = 0.25, 0.75$, but below these values. This can be explained by the fact that the THD becomes much better as soon as there are two steps active instead of one. The next Table (2.4) shows the optimal THD firing angles for different multilevel converters (ML converters):

The FFT of the step modulation voltage has been calculated. It can be seen that the step modulation has low-order harmonics which could be filtered. The simulation is done for a ML-converter with $n = 8$ steps.

If the step modulation is used in a closed-loop control system, there is another problem to resolve. The transfer-function of a step modulator is not linear in the small-signal

Nr. of steps	Threshold	Firing angles [deg]	THD [%]	SNR [dB]
2	$th_1 = 0.394$	$\varphi_1 = 23.2^o$	28.86%	10.7dB
4	$th_1 = 0.210$	$\varphi_1 = 12.12^o$	16.32%	15.8dB
	$th_2 = 0.645$	$\varphi_2 = 40.17^o$		
8	$th_1 = 0.125$	$\varphi_1 = 7.18^o$	8.83%	21.1dB
	$th_2 = 0.365$	$\varphi_2 = 21.41^o$		
	$th_3 = 0.600$	$\varphi_3 = 36.87^o$		
	$th_4 = 0.835$	$\varphi_4 = 56.62^o$		
12	$th_1 = 0.087$	$\varphi_1 = 4.97^o$	5.87%	24.61dB
	$th_2 = 0.247$	$\varphi_2 = 14.28^o$		
	$th_3 = 0.410$	$\varphi_3 = 24.21^o$		
	$th_4 = 0.570$	$\varphi_4 = 34.75^o$		
	$th_5 = 0.733$	$\varphi_5 = 47.17^o$		
	$th_6 = 0.893$	$\varphi_6 = 63.30^o$		

Table 2.4: Optimal firing angles

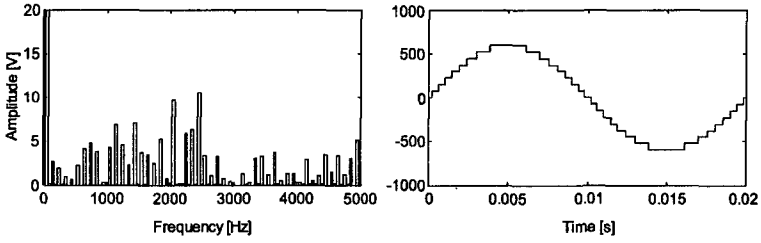

Figure 2.25: FFT of the step modulation voltage

response. If the modulation factor varies around the threshold values, there is a strongly non-linear behavior. This behavior can be explained by the sudden activation of a additional step. If the modulation degree is very high and there are a lot of steps, linearity of the change from on step to the next one is better than in the region of the low-modulation degree.

Figure (2.26) shows the non-linear transfer function. The linear graph represents the ideal linear behavior of the modulation method. If the modulation degree is below the value τ_{offset}, there is no action on the modulator side.

$$\tau_{offset} = \frac{1}{2n} \tag{2.20}$$

If the number of steps is very high (e.g. $n = 10, 12$), this might not be a severe problem. But if the number is small, it is better to compensate this non-linear behavior, especially the offset effect. From Equation (2.16), it is known how many steps are active at the moment. In the next Equation (2.22), the transfer function of the fundamental sine wave in function of the modulation degree is represented.

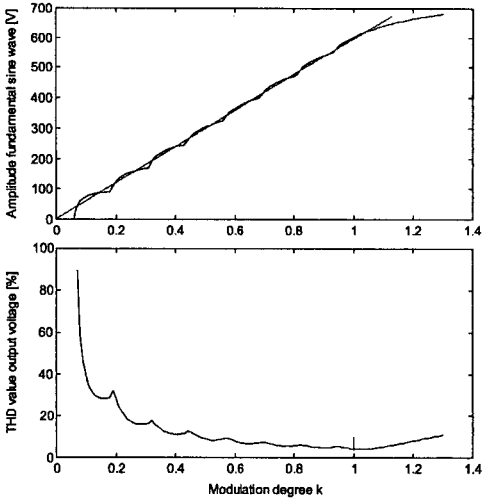

Figure 2.26: Nonlinear behavior of the step modulation

$$\begin{aligned} \widehat{U}_{conv} &= f(U_{dc2}, n, k) \\ \widehat{U}_{conv} &= \frac{4U_{dc2}}{\pi} \sum_{i=1}^{n_{step}} cos\left(\arcsin\left[\frac{1+2(i-1)}{2nk}\right]\right) \qquad (\tau_{offset} < |k| < \infty) \\ \widehat{U}_{conv} &= 0 \qquad (0 < |k| < \tau_{offset}) \end{aligned} \tag{2.21}$$

The interval of validity has to be respected. n_{step} is calculated with Equation (2.16). If the modulation degree k is smaller than the smallest threshold value, the modulator shows no action. The desired transfer function with a new value for the modulation k' should be:

$$\begin{aligned} \widehat{U}_{conv} &= f(U_{dc2}, n, k') \\ \widehat{U}_{conv} &= n \cdot U_{dc2} \cdot k' \qquad \left(0 < |k'| < \frac{4}{\pi}\right) \end{aligned} \tag{2.22}$$

The maximal achievable value for the amplitude of the fundamental sine wave is given when all the steps are turned-on at the angle $\varphi = 0$, so is a rectangular block. The value is:

$$\widehat{U}_{conv(max)} = \frac{4U_{dc2}n}{\pi} \tag{2.23}$$

In this way, the step modulation would have a linear behavior (towards the fundamental sine wave) in the whole range. As shown in Figure (2.26), it is not recommended

to use modulation degrees above 1. The optimal THD value is found at $k = 1$. An inverse function has to be found for the linearization:

$$\hat{U}_{conv} = f(U_{dc2}, n, k'(n,k)) \tag{2.24}$$

The function k' in dependence of n and k is computed and represented in Equation (2.25):

$$k' = \frac{4}{\pi n} \sum_{i=1}^{n_{step}} cos\left(\arcsin\left[\frac{1+2(i-1)}{2nk}\right]\right) \qquad \left(\frac{1}{2n} < |k| < \infty\right) \tag{2.25}$$

This Equation (2.25) has to be resolved by k in order to have the inverse function for the compensation of non-linearity. Unfortunately, the analytical reverse function can only be calculated if $n = 1$.

$$k = \frac{1}{2n \sin\left(\arccos\left[\frac{\pi n k'}{4}\right]\right)} \tag{2.26}$$

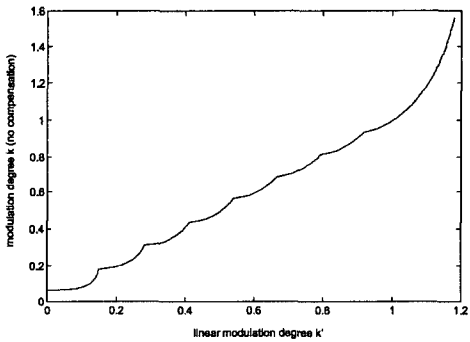

Figure 2.27: Compensation function to generate modulation degree k

For values of n superior to 1, the function must be evaluated numerically, as shown in Figure (2.27). The values can be put down in a look-up table. Anyway, the look-up table solution is more convenient, due to the fact that an algorithm implementation needs much computation power per sampling period.

2.4.2 PWM modulation

The most common modulation method, the pulse width modulation or simply PWM, can also be used for the multilevel converter. To use the PWM modulation method, a certain number of carrier functions (also called auxiliary modulation signals) are needed. All of them are compared with the same reference function $k \cdot V_{ref}$. The carrier functions are normally symmetrical triangular functions, with the same slope in the rising and descending part. In some applications saw-tooth signals are implemented as carrier functions, but this is not discussed in this thesis. The use of the PWM is simple: An carrier

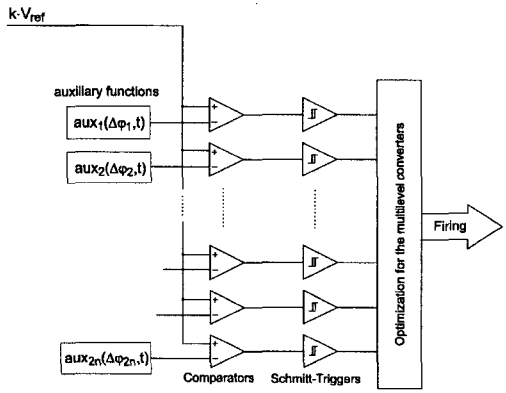

Figure 2.28: Principle of the modulator for the PWM modulation

function is always continuously compared with the set value $k \cdot V_{ref}$: If the set value is smaller than the carrier function, the output of a simple half-bridge would be a negative voltage. If the set value is higher, the half-bridge will generate a positive voltage.

Figure (2.28) shows a schematics of the implementation of the PWM method. So for each half-bridge converter in the multilevel system, an carrier signal is needed.

$$n_{aux} = 2 \cdot n \tag{2.27}$$

In some applications it is desired that every 4Q-converter of the ML-converter is modulated with a different set value. Every 4Q-converter sees a sine wave set value with the same amplitude, but all of them with a small phase shift. This method is only used in particular cases where the power flow for each 4Q-converter must be controlled separately, to be seen in Section 5.1.1, page 194.

Modulation by horizontally shifted carrier signals HSCS

There are two different methods that can be used to create the carrier modulation functions. The first method is called horizontally shifted carrier signals (Method HSCS). All the carrier functions are phase shifted for this modulation method. The frequency f_s of the carrier signals is in any case higher than the frequency f_{line} of the set value, so the frequency of the converter output voltage. So each half-bridge is modulated by a triangular signal with a different phase angle. Figure (2.29) illustrates the modulation method.

For the proposed converter with $n = 4$ steps, 8 carrier signals are needed. A carrier signal for the generation of the positive voltages (aux_i) is represented and a carrier signal for the negative voltage (aux_{n+i}). The carrier signals are in this way indexed from 1 to $2n$. If the modulation degree is equal to $k = 1$, the reference voltage $k \cdot V_{ref}$ will be a sine wave moving within the interval $[-1, 1]$. The definition of the modulation degree k is given in Equation (2.14). It is the same definition for step and PWM modulation method. All the carrier signals for the generation of the positive output voltage have to

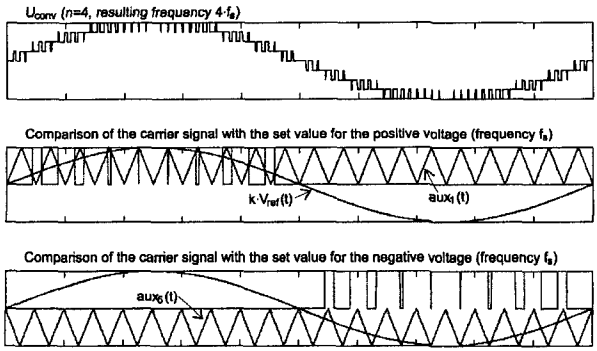

Figure 2.29: Horizontally shifted carrier signals HSCS

be between the interval $[0, 1]$. For the generation of the negative sine wave of the output voltage, the interval is between $[-1, 0]$. This vertical distribution of the carrier signals has a very positive effect for the PWM modulation:

- There is never an voltage cancellation of a positive voltage step by an negative voltage. This effect would generate losses without any power transfer and has to be avoided if the losses shall be kept low.
- Due to the fact that each step of the multilevel converter has the same sliding average value, the switching and conduction losses are automatically equally shared over all voltage steps. This allows the construction of equal cooling facilities for every module.
- No further optimization of the switching signals is required, the signals can directly be used by the converter

The carrier functions can be described mathematically by the following Equation (2.28):

$$aux_i(t) = \begin{cases} \frac{1}{2}\left(1 + \frac{2}{\pi}\arcsin\left[\sin(2\pi f_s t + \Delta\varphi_i)\right]\right) & i = [1, 2, .. n] \\ \frac{1}{2}\left(-1 + \frac{2}{\pi}\arcsin\left[\sin(2\pi f_s t + \Delta\varphi_{i+1-n})\right]\right) & i = [n+1, .. 2n] \end{cases} \tag{2.28}$$

By an equal distribution of all the phase angles over the 360^o, a reduction of the voltage and current harmonics can be observed: The phase angles are chosen as follows:

$$\Delta\varphi_i = \frac{360}{n} \cdot (i-1) \qquad i = [1, 2, .., n] \tag{2.29}$$

So there are n different phase shift values. The resulting switching frequency on the voltage generated by the PWM modulation with the horizontal shift method (HSCS) is:

$$f_{res(HSCS)} = n \cdot f_s \tag{2.30}$$

Modulation by vertically shifted carrier signals (VSCS)

Instead of shifting positive and negative triangular signals by a phase angle, each of the carrier signals per half-bridge can also be shifted vertically, this means the amplitude and offset of the carrier signal depends on the number of steps. But all the triangular carrier signals have got the same amplitude and phase.

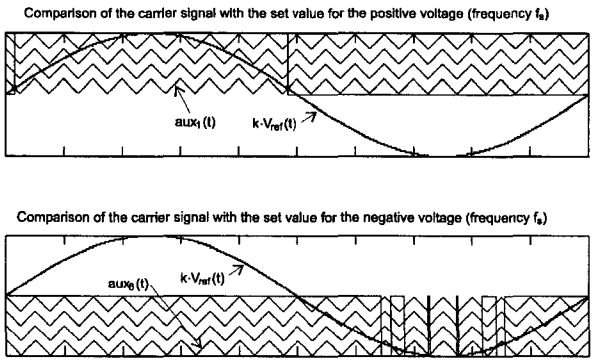

Figure 2.30: Vertically shifted carrier signals (VSCS)

This modulation method is easy to implement (with all the synchronous carrier signals), but presents some disadvantages:

- The voltage cancellation problem is resolved
- Each 4Q-converter has a different RMS voltage value. The upper steps only have a small duty cycle, while the lower steps are turned-on nearly the whole period. This causes unsymmetrical share of losses

If this method is used, an switching optimization has to be implemented in order to share the losses symmetrically. A algorithm is shown in Appendix A.2 where an optimization is done for the a general multilevel voltage. The carrier functions for the VSCS method is given by the Equation (2.31).

$$aux_i(t) = \begin{cases} \frac{1}{2n}\left(\frac{2i-1}{8} + \frac{2}{\pi}\arcsin\left[\sin(2\pi f_s t)\right]\right) & i = [1, 2, .. n] \\ \frac{1}{2n}\left(-\frac{2(i-n)-1}{8} + \frac{2}{\pi}\arcsin\left[\sin(2\pi f_s t)\right]\right) & i = [n, n+1, .. 2n] \end{cases} \tag{2.31}$$

It can bee seen, that there is only a vertical shift (y-axis) and no phase shift angle. But due to the fact that the carrier signals are not phase-shifted, there is no multiplication of the switching frequency. The output voltage of the multilevel converter has the same switching frequency as the carrier signals:

$$f_{res(VSCS)} = f_s \tag{2.32}$$

Harmonics generated by PWM

Another interesting point is the evaluation of the harmonics generated by the PWM. The Figure (2.31) shows a quarter of a period in a PWM modulated multilevel converter. A fourier series expression for this generalized function will be found.

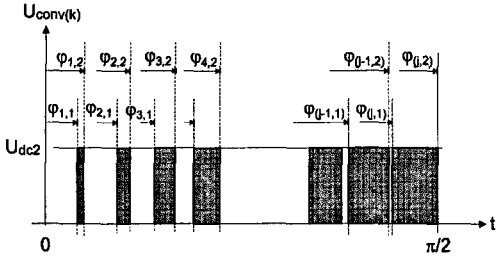

Figure 2.31: Computation of the turn-off and turn-on angles

For this matter, the fourier series of every generated impulse has to be added up. This is done by decomposing the ML-converter in individual 4Q-converters. Each 4Q-converter uses one carrier signal (for the positive part of the sine wave), so there are n sets of turn-on and turn-off angles. In the Figure (2.31), the parameter $\varphi_{(j,k)}$ has the index j, which indicates the impulse number (the number depends on the switching frequency), while k belongs to the carrier function which generated the waveform. Always a pair with a even and a odd number belongs to the same carrier function: The odd numbers are the turn-on angle, while the even numbers represent the turn-off angle. The set $[1, 2]$ belongs to the first carrier function, $[3, 4]$ to the next one and it goes up to $[2n-1, 2n]$ for the last carrier function.
The Equation (2.33) is the fourier evaluation of the converter voltage given in Figure (2.31). To use this equation, the switching frequency f_s should be an entire multiple of the fundamental frequency f_{line}:

$$U_{conv}(t) = \frac{4U_{dc2}}{\pi} \sum_{i=odd}^{\infty} \sum_{j=1}^{\frac{f_s}{2f_{line}}} \left(\left[\frac{-cos(it)}{i} \right]_{\varphi_{(j,1)}}^{\varphi_{(j,2)}}, .., \left[\frac{-cos(it)}{i} \right]_{\varphi_{(j,2n-1)}}^{\varphi_{(j,2n)}} \right) \tag{2.33}$$

The number of steps is also summed, so the following Equation can be found, expressing the output voltage waveform as a fourrier series:

$$U_{conv}(t) = \frac{4U_{dc2}}{\pi} \sum_{i=odd}^{\infty} \sum_{j=1}^{\frac{f_s}{2f_{line}}} \sum_{k=1}^{n} \left((-1)^{k+1} \cdot \cos(i\varphi_{(j,k)}) \right) \cdot \frac{\sin(i\omega t)}{i} \tag{2.34}$$

The variable i represents the order of the harmonic. The next Equation shows the amplitude of a harmonic $U_{harm(p)}$ of the order p:

$$U_{harm(p)} = \frac{4U_{dc2}}{\pi} \sum_{j=1}^{\frac{f_s}{2f_{line}}} \sum_{k=1}^{n} \left((-1)^{k+1} \cdot \frac{\cos(p \cdot \varphi_{(j,k)})}{p} \right) \tag{2.35}$$

The next to Figures (2.32) and (2.33) show a simulation of a multilevel converter using $n = 8$ steps, including the FFT analysis of the voltage. The HSCS method was used. In the first simulation, the switching frequency is 250Hz, so the resulting frequency f_{result} is 2kHz. In the second simulation, the switching frequency is doubled.

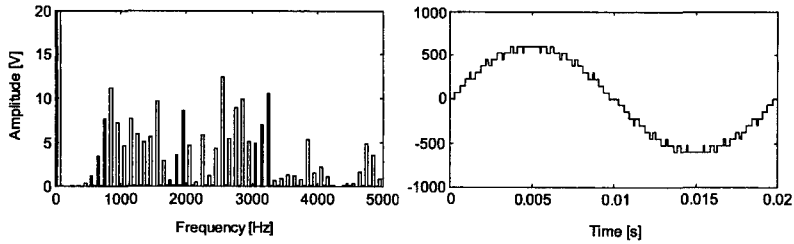

Figure 2.32: PWM simulation with f_s=250Hz

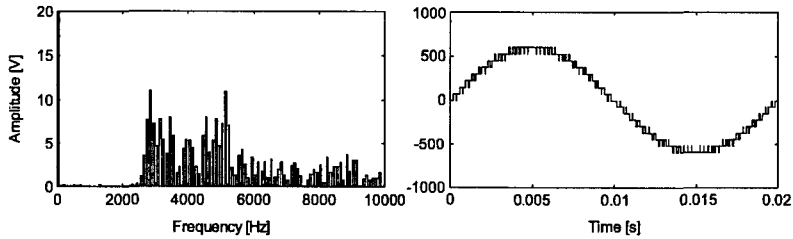

Figure 2.33: PWM simulation with f_s=500Hz

In the PWM modulation, there are no low-frequency harmonics, as can be seen in the simulations. The first harmonics are grouped around the resulting switching frequency, and the next package can be found at the every entire multiple of the resulting switching frequency. This is a important advantage over the step modulation.

2.5 Control methods

There are many usable methods to control the single-phase multilevel converter. There are two points to be noted for the implementation of a multilevel controller, especially if the controller structure is compared with a controller for a conventional single-phase converter without multiple steps:

- If the multilevel converter consists of a high number of steps n, the converter voltage U_{conv} will be of a very good quality and can be considered as a sinusoidal voltage, especially by comparing with a classical converter. This allows to use the converter voltage as a feedback value for a state-space controller.
- If the step modulation is used in a multilevel converter, the non-linearity of this modulation method has to be compensated (see in chapter 2.4.1). This is particularly important if the number of steps n is low. A fast controller system will otherwise try to compensate the non-linearity, which will cause additional switching.

In the following sections, two different controller methods are proposed: A state-space controller using a classical PI-controller scheme and a controller using a rotating coordinate system, called the monophasor controller.

2.5.1 State space controller

Several methods have been proposed to control the line current I_{line} by acting on the voltage of a multilevel controller U_{conv}. A typical implementation of a state-space controller is described in [25], page 95. This implementation shows many interesting features of a state-space controller. The chosen states of the controller are the converter voltage U_{conv} and line current I_{line}. The converter voltage is considered as a non-measurable value, while the line voltage U_{line} is considered to be the perturbation value of the system. This method uses an observer to create a mathematical value of the non-measured states. A PLL must generate the sine-wave used for the current set value. The feedback values of the states are designed to create a predictive set value for the current.
The most efficient state-space controller is described in [26]. This method uses the well-known trigonometric relations between all three electrical values U_{conv}, U_{line} and the current I_{line}. In this way, the set value for the ML-converter is anticipated. The controller is only responsible for slight corrections of the line current I_{line}. The controller is easily implemented and can be easily combined with other controllers, as shown in the multilevel systems Chapter 5. The method [26] has been implemented in the simulations shown in Section 5.1.1 on page 188 and the system is showing considerable performance. For more information please refer to the mentioned chapter.

2.5.2 Control by monophasors referenced to a rotating coordinate system

A general view of a typical single-phase converter system using a multilevel converter is shown in Figure (2.34). The controlled output value is the current I_{line}, it is measured and compared to the set value $I_{line(set)}$. The controller in (1) generates a sinusoidal

set value $k' \cdot V'_{ref}$. This modulation function enters block (3), where the line current is directly derived from the trigonometric relations between U_{line}, U_{conv} and I_{line}, shown in the Figure (2.37). To do this, a PLL or an observer (3) has to generate a sinewave (in phase with the line voltage U_{line}) and a cosine-wave (in phase with the voltage drop ΔU on the line inductance). This is described in [26] and in the Chapter 5.1.1 starting at page 183.

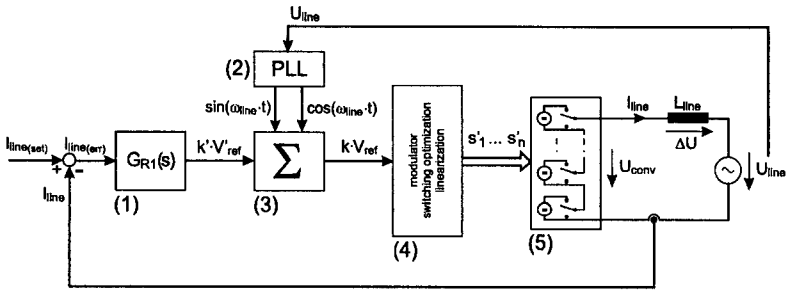

Figure 2.34: A general view of a typical single-phase converter controller

After the feed-forward of those values, the modulation function $k \cdot V_{ref}$ results. In the function block (4), the switching signals s'_1 to s'_n are generated from the modulation function $k \cdot V_{ref}$. The nonlinear behavior of the modulation method is compensated (see Section 2.4.1) and the switching signals are optimized for the ML-converter. At last, the ML-converter (5) generated the output voltage U_{conv}. This control method has been tested in Chapter 5. The control of the current I_{line} in this system, the multilevel converter always demands a relatively fast controller system: All the values are rapidly changing with the time. For instance, the converter voltage U_{conv}, line voltage U_{line} and the line current I_{line} are all sinusoidal or have another time-dependent waveform. In order to avoid a controller using sinusoidal values for the error (line current error), set value (line current set value) and controller output (modulation function), a different method has to be used, using the monophasors in a rotating coordinate system. An overview of this control method is given in Figure (2.35).

Instead of a controller G_{R1}, the function block (1) with the monophasor controller is taken. The method uses monophasors in a complex plane, which are afterwards referenced to a rotating coordinate system. The rotating coordinate system turns with the line frequency $2\pi f_{line}$. By doing this coordinate transformation, the controlled values are no time-dependent functions anymore. Especially in this case, where the line current I_{line} should be controlled to a perfect sine-wave, method seems ideal. If the controlled line current I_{line} is not supposed to be sinusoidal, the method is not ideal, because the controller will not see only the DC-component of the values. An overview of the method is itemized below:

- First, the monophasors in the coordinate system (Im, Re) for the time-dependent values have to be generated. The most interesting value is the current I_{line}, which has to be controlled. The result is a vector $\underline{I}_{line}$

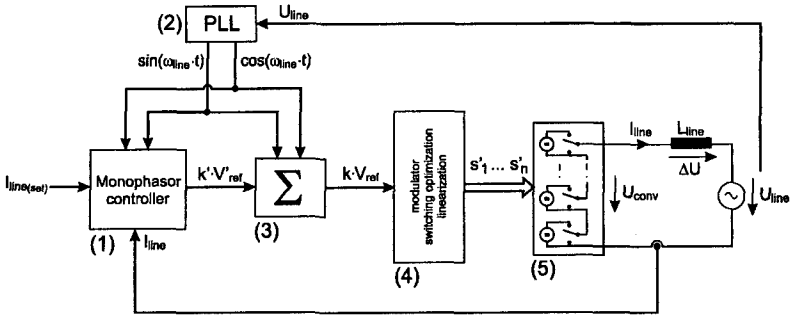

Figure 2.35: Control by using the monophasors

- The measured line voltage U_{line} must be in phase with a reference function $sin(2\pi f_{line}t)$. From the measured voltage U_{line} a phase-locked loop (PLL) or an observer generates the function $sin(2\pi f_{line}t)$. At the same time a cosine-function $cos(2\pi f_{line}t)$ is generated, with a phase shift of 90^o compared to the sine-wave.

- A rotating coordinate system (α, β) is defined, rotating in the complex phasor plane in phase with the monophasor $\underline{U}_{line}$. The rotating frequency is the line frequency $2\pi f_{line}$, the coordinate system is composed of two axes α and β. The two axes are orthogonal, this means α turns with the generated function $sin(2\pi f_{line}t)$, while β turns with $cos(2\pi f_{line}t)$.

- At last, the monophasor of the line current is referred to the rotating coordinate system. The result are two DC components of the current (I^r_α, I^r_β), described in a vector $\underline{I}^r$.

The Figure (2.37) shows the monophasors of a single-phase multilevel converter. The method has a certain similarity with the transformation of the three-phased, time-dependent values to the phasor values, used in three-phase motor control [27], page 151 and [28], page 100, and is also described in Chapter 3. In this report, the monophasor is defined as a vector $\underline{U}$ rotating with a constant frequency $2\pi f_{line}$ in the complex plane. In the case where the coordinate system (α, β) and the vector $\underline{U}$ are in phase, the real part $Re(\underline{U})$ of the vector $\underline{U}$ is the existing, time-dependent value, which has a sinusoidal waveform. The imaginary part $Im(\underline{U})$ is a non-existing value, which is only useful for the control. Of course it is also a sinusoidal value.

Transformation and control of the monophasor in a rotating coordinate system

In this section the principle of the controller for the current is explained. The Figure (2.36) shows the block schematic of the system with transformation, controller and re-transformation.

The measured line current I_{line} is the input to the converter system, as been seen in (2.35). For a single-phase converter the line current I_{line} can be defined as a vector $\underline{I}_{line}$

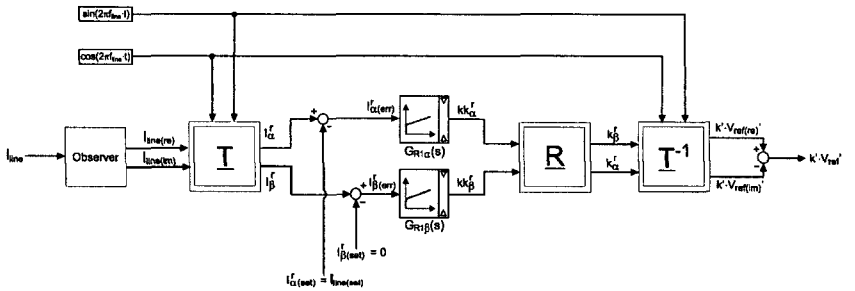

Figure 2.36: Schematics of the monophasor controller

in the complex plane (Re, Im). This vector is called monophasor.

$$\underline{I}_{line} = \begin{bmatrix} I_{line(re)} \\ I_{line(im)} \end{bmatrix} \tag{2.36}$$

If the current is controlled at $cos\varphi = 1$, the real part $I_{line(re)}$ is the amplitude of the line current I_{line}. Otherwise the two components of the vector $\underline{I}_{line}$ have to be generated. In the Equation (2.39), the current is assumed without a DC component, with a phase-shift α_c towards the line voltage U_{line}:

$$I_{line(re)} = \hat{I}_{line} \cdot sin(2\pi f_{line} t + \alpha_c) \tag{2.37}$$

$$I_{line(im)} = \hat{I}_{line} \cdot cos(2\pi f_{line} t + \alpha_c) \tag{2.38}$$

$$\hat{I}_{line} = \sqrt{I^2_{line(re)} + I^2_{linc(im)}} \tag{2.39}$$

The two components are generated through a state observer, described on page 44. A general situation showing the monophasors of the line current I_{line} and the line voltage U_{line} can be seen in the phasor diagram presented in Figure (2.37).

The transformation of the current from the fixed coordinate system (Re, Im) to the rotating coordinate system (α, β) is done by a matrix operation:

$$\underline{I}^r = \underline{T} \cdot \underline{I}_{line} \tag{2.40}$$

This operation is visualized in the Figure (2.36). The matrix contains the following information:

$$\underline{T} = \begin{bmatrix} sin(2\pi f_{line} t) & cos(2\pi f_{line} t) \\ cos(2\pi f_{line} t) & -sin(2\pi f_{line} t) \end{bmatrix} \tag{2.41}$$

If the matrix $\underline{T}$ is implemented in a controller system, it needs the two time-dependent functions $sin(2\pi f_{line} t)$ and $sin(2\pi f_{line} t)$, which must be generated by a PLL or an observer. After this transformation, two DC values for the current $\underline{I}^r$ are obtained, as to

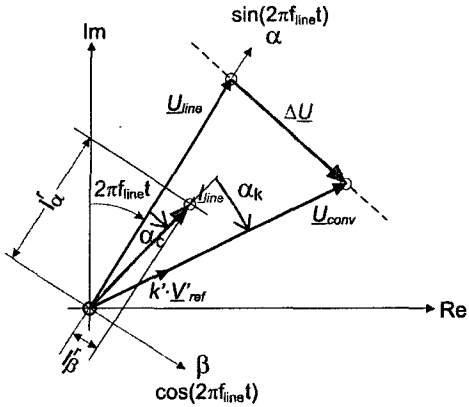

Figure 2.37: Turning coordinate system to generate the monophasors

be seen in the Figure (2.36). The vector of this current in the rotating coordinate system (α, β) is given with Equation (2.42):

$$\underline{I}^r = \begin{bmatrix} I^r_\alpha \\ I^r_\beta \end{bmatrix} \tag{2.42}$$

These two current components are DC values, which represent the measured line current $I_{line}(t)$. A current error is generated from a current set value $\underline{I}^r_{set}$:

$$\underline{I}^r_{err} = \underline{I}^r - \underline{I}^r_{set} \tag{2.43}$$

If the current must be in phase with the line voltage, of course the β-part of the current must be zero, while the α-part represents the line current amplitude:

$$I^r_{\alpha(set)} = \hat{I}_{line} \tag{2.44}$$

$$I^r_{\beta(set)} = 0 \tag{2.45}$$

The two components of the error vector $\underline{I}^r_{err}$ are entering a classical PI-controller. An implementation of a PI controller is shown in Figure (5.16), page 192. The outputs kk^r_α and kk^r_β of the PI-controllers have afterwards to be turned by 90° clockwise in the complex phasor plane: The controller $G_{R1\alpha}$ has as an output the modulation degree kk^r_β, while the controller $G_{R1\beta}$ generates the modulation degree kk^r_α. The reason for this can easily be explained by looking at the phasor diagram shown in Figure (2.37): If the amplitude of the current I_{line} is not big enough (α-direction), the modulation function $k' \cdot V'_{ref}$ must be risen in the β-direction. The β-direction is the direction of $\Delta\underline{U}$, which generates the current amplitude. This direction cannot change the phase of the current I_{line}. A change on the α-direction on the modulation function $k' \cdot V'_{ref}$ will cause a phase-shift on the current without causing a change in the amplitude. So the controller output

vector is $\underline{kk}^r$. This vector must be rotated by 90^o clockwise to receive the vector for the modulation $\underline{k}^r$. Both vectors are oriented to the rotating coordinate system (α, β):

$$\underline{k}^r = \begin{bmatrix} k^r_\alpha \\ k^r_\beta \end{bmatrix} = \underline{R} \cdot \underline{kk}^r = \underline{R} \cdot \begin{bmatrix} kk^r_\alpha \\ kk^r_\beta \end{bmatrix} \tag{2.46}$$

The matrix for the rotation is:

$$\underline{R} = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix} \tag{2.47}$$

The modulation function is defined as a vector $\underline{V}'_{ref}$. This is a monophasor in the complex plane (Re, Im). The components of the vector are given below:

$$\underline{V}'_{ref} = \begin{bmatrix} V'_{ref(re)} \\ V'_{ref(im)} \end{bmatrix} \tag{2.48}$$

And the definition of the real and imaginary parts for sinusoidal waveforms:

$$k' \cdot V'_{ref(re)} = k' \cdot sin(2\pi f_{line} t + \alpha_k + \alpha_c) \tag{2.49}$$

$$k' \cdot V'_{ref(im)} = k' \cdot cos(2\pi f_{line} t + \alpha_k + \alpha_c) \tag{2.50}$$

The modulation function V'_{ref} must be composed after a re-transformation in the fixed coordinate system. The inverse transformation matrix $\underline{T}^{-1}$ is needed.

$$k' \cdot \underline{V}'_{ref} = \underline{T}^{-1} \cdot \underline{k}^r \tag{2.51}$$

The matrix is defined in Equation (2.52). The inverse matrix $\underline{T}^{-1}$ is the same as the original matrix $\underline{T}$

$$\underline{T}^{-1} = \underline{T} = \begin{bmatrix} sin(2\pi f_{line} t) & cos(2\pi f_{line} t) \\ cos(2\pi f_{line} t) & -sin(2\pi f_{line} t) \end{bmatrix} \tag{2.52}$$

Due to the behavior of the observer to generate the imaginary and real part of the current, proposed in the Section on page 44, the modulation function for the modulator is not just the real part of the vector $\underline{V}'_{ref}$, but the difference between the real part and the imaginary part, to be seen in Equation (2.53):

$$V'_{ref} = V'_{ref(re)} - V'_{ref(im)} \tag{2.53}$$

This composition can be seen in the schematic of the Figure (2.36). Combined with the modulation degree k', the final composition Equation is:

$$k' \cdot V'_{ref} = k' \left[V'_{ref(re)} - V'_{ref(im)} \right] \tag{2.54}$$

The explication for this composition is given with the following development: If the line current I_{line} has a DC component $I_{line(DC)}$, the monophasor controller can eliminate this component. For this, the transformation to the rotating coordinate system (α, β)

and the re-transformation has to be looked at. A line current is given without any time-dependent part:

$$I_{line}(t) = I_{line(DC)} \tag{2.55}$$

The observer described in Section 2.5.2 is generating the imaginary part. But due to the integral behavior and the initial conditions of the observer, the imaginary part will remain zero:

$$\underline{I}_{line} = \begin{bmatrix} I_{line(DC)} \\ 0 \end{bmatrix} \tag{2.56}$$

After the transformation to the rotating coordinate system (α, β) and a simplification of the trigonometric relations according to [29], page 67, it results:

$$\underline{I}^r = \begin{bmatrix} I_{line(DC)} \cdot sin(2\pi f_{line} t) \\ I_{line(DC)} \cdot cos(2\pi f_{line} t) \end{bmatrix} \tag{2.57}$$

The DC current is represented in the plane (α, β) as a oscillating current with the frequency f_{line}, and the amplitude $I_{line(DC)}$. The set values $\underline{I}^r_{set}$ are constant, so the controllers $G_{R1\alpha}$ and $G_{R1\beta}$ will generate two sinusoidal values from the difference between the set value and the measured current. All other transient responses are not considered. After a rotation of the vector by 90^o by the matrix $\underline{R}$ it can be found:

$$\underline{k}^r = \begin{bmatrix} -k' \cdot cos(2\pi f_{line} t) \\ k' \cdot sin(2\pi f_{line} t) \end{bmatrix} \tag{2.58}$$

These two values are re-transformed to the plane (Re, Im) and after an algebraic simplification it results:

$$k' \cdot \underline{V}'_{ref} = \begin{bmatrix} 0 \\ -k' \end{bmatrix} \tag{2.59}$$

While the real part of the vector $k' \cdot \underline{V}'_{ref}$ is containing all information needed to generate a sinusoidal set value for the modulation function $k' \cdot V'_{ref}$, the imaginary part only will have the information to compensate the DC component of the line current, but as a negative value. This DC component has to be compensated. This is why the modulation function $k' \cdot V'_{ref}$ is generated by a difference between the two vector components of $k' \cdot \underline{V}'_{ref}$. This can be seen in Figure (2.36). This effect is especially due to the behavior of the proposed observer, in which the imaginary part of the current $\underline{I}_{line}$ has no DC component.

Observator to generate the imaginary part of the monophasor

The observer is used to generate the imaginary part of the current $\underline{I}_{line}$. This non-existing value $I_{line(im)}$ is phase-shifted by 90^o comparing to the real part I_{line}, shown in Figure (2.37). A general introduction to the observers can be found in [30], page 275, or in [31], page 90. The observer can be described by the following state-space Equation, using the state vector $\underline{x}_w$:

$$\dot{\underline{x}}_w = \underline{A}_w \cdot \underline{x}_w + \underline{g} \cdot I_{line} \tag{2.60}$$

$$I_{line(re)} = \underline{c}^T \cdot \underline{x}_w \tag{2.61}$$

$$I_{line(im)} = \underline{h}^T \cdot \underline{x}_w \tag{2.62}$$

The parameter matrix and the vectors of the state-space Equation are:

$$\underline{A}_w = \begin{bmatrix} -g_1 & -2\pi f_{line} \\ 2\pi f_{line} - g_2 & 0 \end{bmatrix} \tag{2.63}$$

$$\underline{g} = \begin{bmatrix} g_1 \\ g_2 \end{bmatrix} \tag{2.64}$$

$$\underline{c}^T = [1 \quad 0] \tag{2.65}$$

$$\underline{h}^T = [0 \quad -1] \tag{2.66}$$

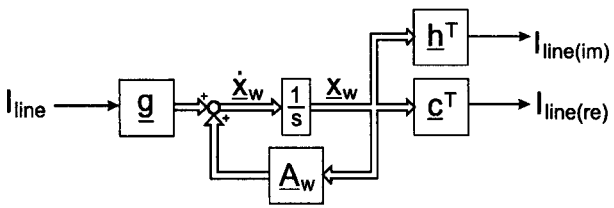

Figure 2.38: Observer to generate the complex current values

The two unknown parameters is the feedback vector $\underline{g}$ to the two states. To compute these parameters, the poles of the system can be chosen. For this aim, the transfer function of the open loop system is calculated, and then the poles of the denominator are placed, by using the two undefined parameters g_1 and g_2. The polynomial of the denominator is:

$$p_{observ} = det(s\underline{I} - \underline{A}_w + \underline{g}\underline{c}^T) = s^2 + s2g_1 - 2\omega_{line}g_2 + \omega_{line}^2 \tag{2.67}$$

The characteristic polynomial p_{observ} of the observer can be represented in the following form:

$$p_{observ} = (s - s_1) \cdot (s - s_2) \tag{2.68}$$

For an optimal stability and control performance, the poles s_1 and s_2 are placed in the manner that they are a pair of conjugal-complex value with a negative real part:

$$s_{1,2} = -\sigma \pm j \cdot \omega_{res} \tag{2.69}$$

σ is the dominant attenuation factor and ω_{res} is the natural resonance frequency of the observer. By comparing the parameters of the Equation (2.69) with the Equation (2.67), the following parameters can be found for $\underline{g}$:

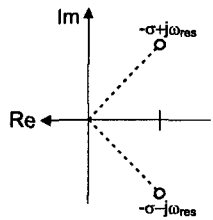

Figure 2.39: Placement of the poles of the observer

$$g_1 = \sigma \tag{2.70}$$

$$g_2 = \frac{\omega_{line}^2 - \sigma^2 - \omega_{res}^2}{2\omega_{line}} \tag{2.71}$$

The numerical value for the attenuation shall be ten times faster than the line frequency:

$$\sigma = 10 \cdot 2\pi f_{line} \tag{2.72}$$

$$\omega_{res} = 10 \cdot 2\pi f_{line} \tag{2.73}$$

The initial conditions for the state vector of the observer are also important. The best is to start the control when the imaginary and real part of the states are defined. The converter starts to control when the line voltage U_{line} passes through zero and is rising. The following initial conditions can be found:

$$\underline{x}_w(U_{line} = 0) = \begin{bmatrix} 0 \\ -\hat{I}_{line} \end{bmatrix} \tag{2.74}$$

A simulation shows the current monophasor referenced to the rotating coordinate system (α, β). The current is phase-shifted compared to the reference coordinate system.

In the first simulation, a current with a DC component of 20A is taken. The current amplitude is 283A. As said before, the imaginary part of the line current $\underline{I}_{line}$ does not contain any DC component. The two parameters referenced to (α, β) are shown in red: The oscillating part of I_α^r is in phase with the reference function $sin(2\pi f_{line} t)$, while I_β^r is in phase with $cos(2\pi f_{line} t)$. After the re-transformation of the controller output values, the DC component compensation can be seen on the imaginary part of the modulation function $k' \cdot \underline{V}'_{ref}$

In the second simulation, a non-sinusoidal current has been chosen with a flattened peak value. In the Figure (2.40), the current is in the colour blue. The reference function $sin(2\pi f_{line} t)$ is multiplied with the current amplitude and is shown with the dashed line. The flat parts are seen as bumps on the current I_α^r. The controller is in this way able to react and will correct the non-sinusoidal parts of the current.

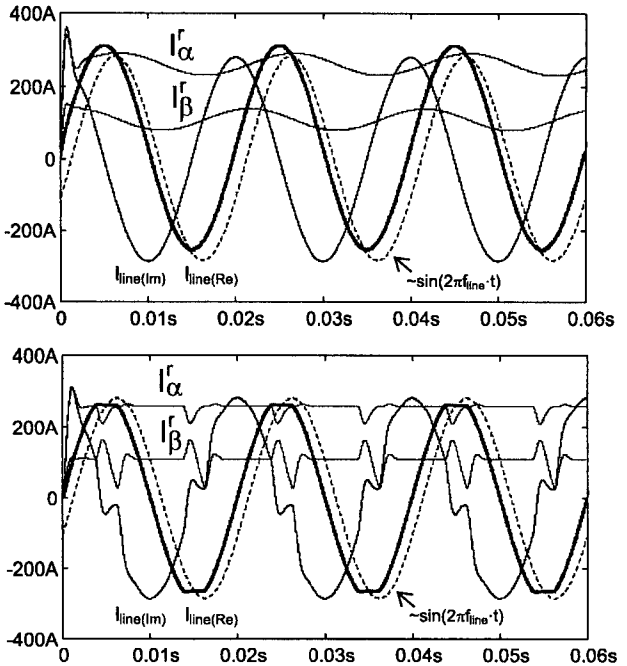

Figure 2.40: Simulation of the observer with a current $\alpha_c \neq 0$

Overview over the entire control system

The entire control system as described before has been implemented. The schematics of the simulated controller is shown in Figure (2.41). The implementation has been done in MATLAB/SIMULINK. The two controllers $G_{R1\alpha}$ and $G_{R2\beta}$ are standard PI controllers. The parameters are computed by using the meplat criteria, shown in [30], page 322. The meplat criteria optimizes the performance of the controller on changes of the set value, but has not for influences on the perturbation value. But due to the fact that all perturbation values are directly introduced to the set value $k' \cdot V'_{ref}$, and the controller is implemented in the rotating coordinate system, where all values are DC values, there is no visible perturbation for the controller. That's why the meplat criteria is ideal. An overview of the controller system is shown in (2.41).

The controller parameters for the two line current controllers $G_{R1\alpha}(s)$ and $G_{R2\beta}$ are PI controller, which generate after re-transformation a sinusoidal modulation function $k' \cdot V'_{ref}$. The final set value $k \cdot V_{ref}$ is a linear combination of the line current U_{line}, the cosine function generated with the PLL circuit representing the phase of the voltage drop ΔU over the line inductance L_{line} and of course the set value $k' \cdot V'_{ref}$ coming from the monophasor controller block. For more details, please refer to the systems chapter, 5.1.1. The transfer function transferring the output value of the controller to a physical value

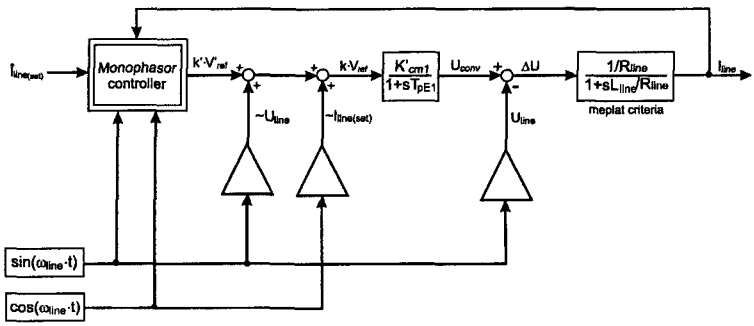

Figure 2.41: Overall schematics of the multilevel controller using the monophasors

is named $G_{cm1}(s)$ and is composed of an amplification factor and a small time delay:

$$G_{cm1}(s) = \frac{K'_{cm1}}{1 + sT_{pE1}} \tag{2.75}$$

The amplification factor from the modulation degree to the multilevel converter voltage can be found in Equation (5.36) and the small time constant of the system is composed of:

$$T_{pE1} = \frac{T_{sample}}{2} + T_{cm2} + T_{r2} \tag{2.76}$$

The calculation of T_{cm2} can be found in Equation (5.38). The system that has to be controller is called $G_{Sa1}(s)$. This transfer function has a behavior as a PT_1-element, in order to design the controller parameters by the meplat criteria. The PT_1-element is defined in [31].

$$G_{Sa1}(s) = \frac{\frac{1}{R_{line}}}{1 + s\frac{L_{line}}{R_{line}}} = \frac{K_{s1}}{1 + sT_{11}} \tag{2.77}$$

The two time constants are computed by the meplat criteria:

$$T_{n1} = T_{11} \tag{2.78}$$
$$T_{i1} = 2K'_{cm1}K_{s1}T_{pE1} \tag{2.79}$$

And the amplification parameters K_{p1}, K_{i1} of the controllers $G_{R1\alpha}$ and $G_{R1\beta}$ are given with the Equations (5.44) in the Section 5.1.1.

A multilevel converter system has been simulated with these parameters to show the performance of the monophasor controller. The first simulation done is a step response

n	10	Number of converter steps
$\overline{U}_{dc2(set)}$	$2.8kV$	DC feeding voltage U_{dc2}
P_{mot}	$3MW$	Motor power, maximal value
U_{line}	$15kV$	Effective line voltage
f_{line}	50Hz	Line frequency
L_{line}	$25\mu H$	Line inductance
R_{line}	$100m\Omega$	Line resistance
T_{sample}	$200\mu s$	Sampling time
f_s	50Hz	Switching frequency 4Q
$\tau_{blank(4Q)}$	$3\mu s$	Blanking time 4Q
$T_{\tau 2}$	$65\mu s$	Measurement delay

Table 2.5: Numerical values for the simulated system

on the set value, the line current amplitude $I_{line(set)}$. The step is done from 50% of the possible line current to 100%, in the moment when the current is on the maximal value of the sine wave. The current reaches its steady-state after 15ms, but without any significant overshooting or generation of high-frequency harmonics.

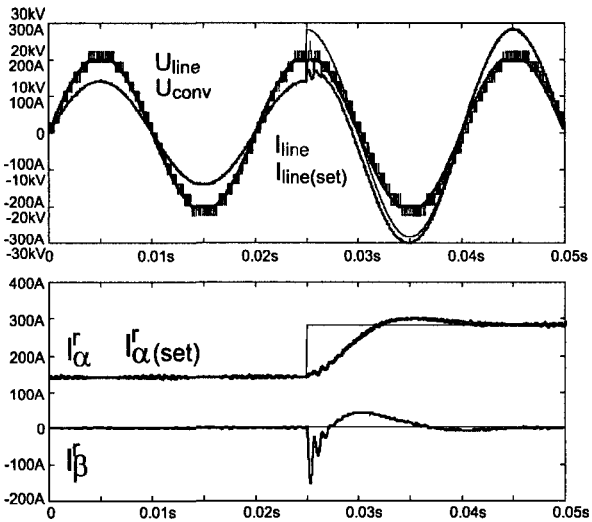

Figure 2.42: Change of current set value using monophasor controller

The following Table (2.5) shows the simulation parameters:

The Figure (2.43) shows the two current vector components $I_{line(re)}$ and $I_{line(im)}$ in a XY-plot. This graph reminds the reader of the three-phase motor current representations, used for the vector control. The current is following an inner circle until the current set value is changed by the factor 2.

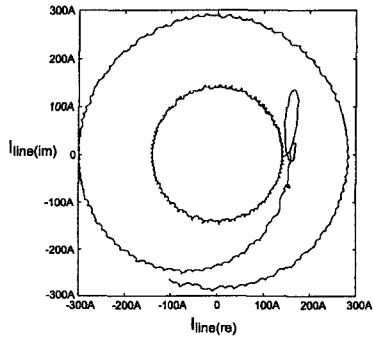

Figure 2.43: Single phase current represented as a phasor

To show the excellent performance of the controller system towards the perturbation value, which is the line voltage U_{line}, the line voltage amplitude is risen from $\sqrt{2} \cdot 12kV$ to $\sqrt{2} \cdot 16.5kV$. Once again this is done in the worst case, where the current is maximal. The simulations presented in Figure (2.44) show no change on the current, this can be seen on the sinusoidal current I_{line} but also on the vector representation I_{α}^{r}, oriented to the rotating coordinate system.

The monophasor controller method does not present the same dynamic performance like the controller systems presented in the Chapter 5. But the line current I_{line} is compared with a perfect sine-wave in a two-component vector space, representing all necessary information on the current like the phase-angle, the amplitude and the harmonics. This allows to implement a controller compensating most of the harmonics and the DC-component by using only one controller. Unfortunately, the implementation needs some processing power for the transformations and the implementation of the observer.

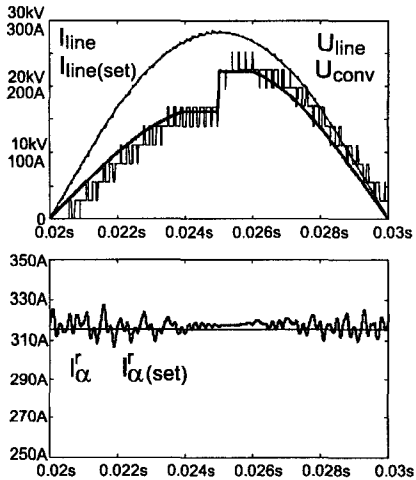

Figure 2.44: Change of line voltage (perturbation value) using monophasor controller

2.6 Experimental results on a 500W prototype

To test the modulation methods and the control principles, a prototype has been assembled in the laboratory. The basic element of the experimental setup is shown in Figure (2.45). The four-quadrant converter on the right side of the image consists of power MOSFET switches without any snubber circuit. The DC feeding voltages $U_{dc2(i)}$ are generated over a transformer, which is coupled to a 50Hz network and a rectifier bridge. If there is no load on the AC side of the 4Q-converter, the DC voltages $U_{dc2(i)}$ are about 50V. A chopper is integrated to tolerate negative load current $I_{ch2(i)}$.
The AC side of the 4Q-converters are connected in series, building a SCFQ converter. Altogether, there are $n = 4$ of those power modules in series. This converter group is connected to a 50Hz AC source U_{line} throughout a decoupling inductor L_{line}. This setup was already shown in Figure (2.5). The system parameters are given in the Table (2.6)

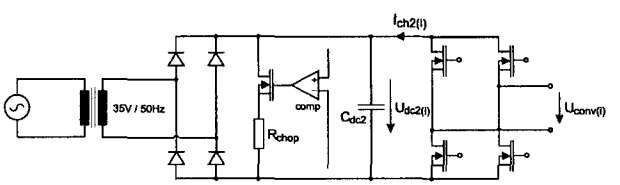

Figure 2.45: Realized multilevel converter step module with MOSFETS

A chopper circuit integrated in the 4Q-converter feeding part allows a generative current in the line. If the current entering to the DC capacitor $I_{ch2(i)}$ is positive (comparing

Parameter	Symbol	Value
Number of steps	n	4
DC power supply	$U_{dc2(i)}$	50V
Sampling time	T_{sample}	$250\mu s$
Measurement delay	T_{r2}	$75\mu s$
Switching frequency PWM	f_p	1kHz
Power MOSFET	$U_{ce(max)}$, $I_{c(max)}$	200V,5A
Max. DC current	$I_{ch2_{max}}$	2A
Inductive load	L_{line}	$170mH$
Resistive part	R_{line}	2Ω
Chopper resistance	R_{chop}	12Ω
Line voltage	U_{line}	90V / 50Hz
Nominal current	I_{line}	$1A$

Table 2.6: The parameters of the realized single phase converter

to the given sign value), the capacitor is charged. The diode rectifier bridge does not allow a current in this direction. In this case, the chopper is used. The power MOSFET switch works in a hysteresis mode: It is turned-on when the voltage $U_{dc2(i)}$ is 20% higher than its nominal value. In this way, the capacitor is discharged over the chopper inductor. Once the voltage $U_{dc2(i)}$ has reached again its nominal value, the MOSFET is turned-off again. The power resistor of the chopper is chosen by respecting the following Equation (2.80) on page 52:

$$R_{chop} < \frac{U_{dc2(max)}}{2 \cdot I_{ch2(max)}} \tag{2.80}$$

In this way, the capacitor is always discharged very quickly, even if a high current I_{ch2} is coming in.

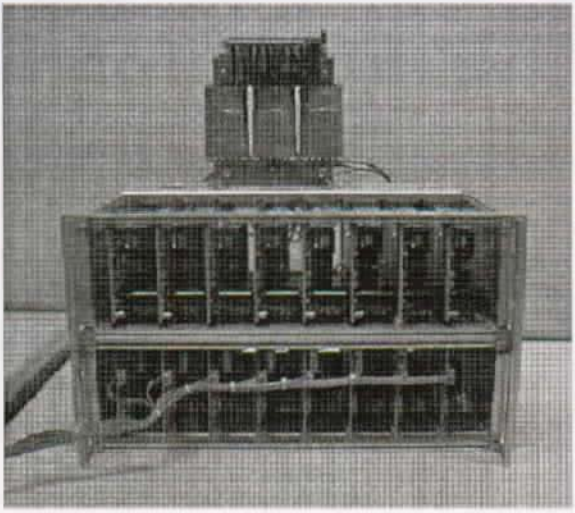

Figure 2.46: The realized single-phase multilevel converter

The photo (2.46) shows the laboratory implementation. On the top of the rack a three-phase transformer with the orange colored isolation can be seen, used to generate the individual DC voltages $U_{dc2(i)}$ for the feeding of the 4Q-converters. The upper eight boards in the slots are the feeding elements with rectifier and chopper. The lower cards are the 4Q-converters. The bunch of flat cables going to the left are needed for the firing signals controlling the power MOSFET. In the same time, the cables are transmitting the measured values for the line current I_{line}. The cables are connected to a PC. The PC is equipped with an AD-converter board for the measured signals and a gate array board, in which the modulators are implemented.
The first experimental results have been done with the step modulation. Figure (2.47) show the multilevel converter a nominal line current of $I_{line} = 1A$. A state-space controller according to Section 5.1.1 has been implemented. The modulator uses the principle of the rotating commutation patterns in order to distribute the losses equally, as described in Section 2.4.1. The current I_{line} is kept in phase with the line voltage U_{line}. The decoupling inductor is relatively big ($L_{line} = 170mH$). That is why on the measurements of the current no distortion can be seen.

The same measurement has been done with a generative current in Figure (2.48): The line current I_{line} has a 180° phase-shift comparing to the line-voltage U_{line}. Due to the hysteresis characteristics of the chopper, the DC-voltages $U_{dc2(i)}$ are higher (about 60V) than in the simulation in Figure (2.47) (about 50V). The voltage U_{line} has been generated over a transformer from the ordinary 50Hz domestic network. The voltage is not perfectly sinusoidal, the peak of the waveform is flattened.

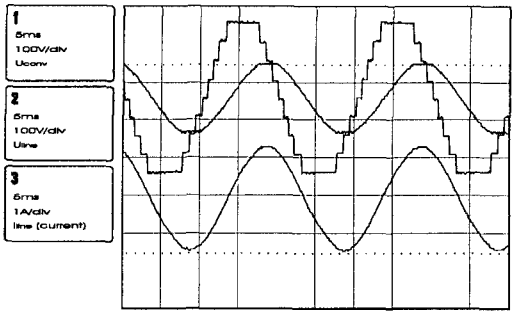

Figure 2.47: Measurements with the step modulation in the motor mode

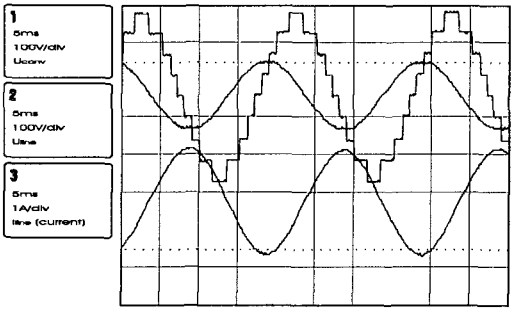

Figure 2.48: Measurements with the step modulation in the generator mode

For the next two experiments, a PWM modulation scheme has been implemented, using the VSCS method, already described in Section 2.4.2. The resulting switching frequency is rather high 8kHz and due to the use of a high line inductance I_{line}, the current waveform seems to be perfectly sinusoidal. The experiments in Figure (2.49) shows the multilevel converter values with a motor current consumption.

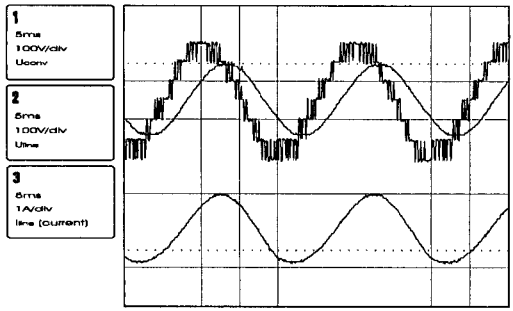

Figure 2.49: Measurements with the PWM modulation in the motor mode

The same measurements are done in Figure (2.50), but this time with a generative current. It has to be remarked that the DC voltages $U_{dc2(i)}$ are 20% bigger than in the measurement in Figure (2.50).

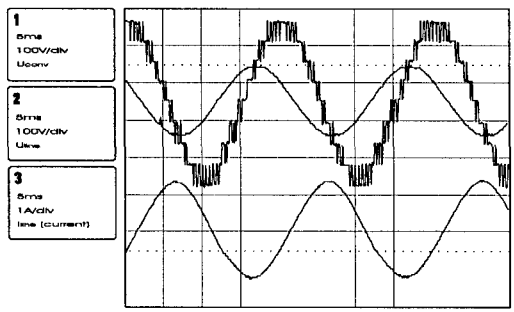

Figure 2.50: Measurements with the PWM modulation in the generator mode

An FFT analysis has been done on the converter voltage U_{conv}, in order to confirm the simulated results presented in the Figure (2.33). Two FFT graphs are shown in Figure (2.51), one with the full modulation degree $k = 1$, the other one with the modulation degree $k = 0.5$. The switching frequency harmonics with their high-order harmonics can be seen, at the frequencies 8kHz, 16kHz and 24kHz. At 16kHz, the PWM modulation harmonics are divided in two groups of harmonics. No FFT has been done on the currents, because of the high noise level no harmonics could be identified.

A measurement has also been done of the single-phase ML-system using the monophasor controller, presented in Figure (2.52). The line current I_{line} referenced to the rotating coordinate system with the two DC components I_α^r and I_β^r can be seen. As shown before in the Section 2.5.2, the controller controls only DC values. The current component I_β^r must be controlled to zero in order to achieve a current with $cos\varphi = 1$. I_α^r is equivalent to the amplitude of I_{line}. The controller shows a step response of the set value $I_{\alpha(set)}^r$.

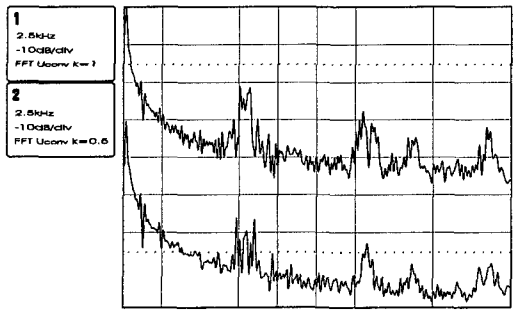

Figure 2.51: FFT of the generated converter voltage U_{conv} in the PWM modulation method

The converter is working in the motor mode, and when the current passes through zero, the sign value is changed to put the converter in the generative mode.

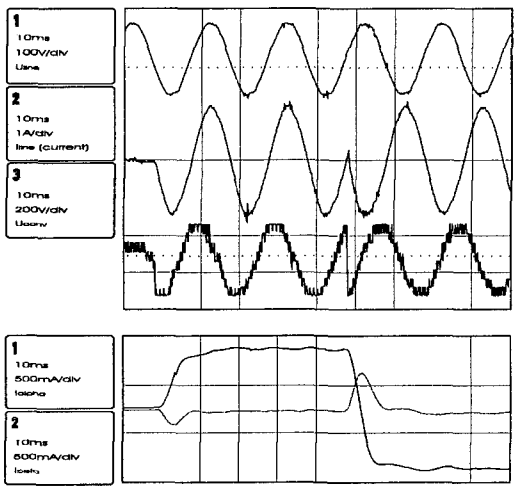

Figure 2.52: Experimental result of the monophasor controller method

Conclusions

The general concept of the single phase multilevel converter with the series connected four-quadrant converters (SCFQ) is explained. The SCFQ type is compared with two other multilevel converter concepts. Many of the known DC feeding techniques for the four-quadrant converters are compared. The step modulation method and PWM modulation method have been developed and optimized for this kind of converter type. A novel single-phase control principle is proposed. The alternative values are transformed to a rotating coordinate system, where the time-dependent waveforms are seen as DC values. This method is not as fast as a state-space controller, but shows good performance to eliminate line current harmonics with only two PI-controllers. All the developments have been simulated and tested on a reduced power prototype.

Chapter 3

Three phase multilevel converter

3.1 Introduction

In this thesis, a three-phase multilevel converter is presented. A general multilevel topology is discussed, consisting of the series connection of the four-quadrant converters. Depending on the application, there are many similar topologies of the multilevel converter, which can all be derived from the general topology [16]. The presented topology can be used for several applications, where the classical voltage-source inverters like the three-phase converter with six IGBT switches or the NPC converter are not useable. Of course the multilevel converter presents not only advantages towards the classical solutions, especially the high complexity and with this the higher costs are the main disadvantages of the multilevel solution. Two typical application fields are distinguished.

3.2 Multilevel vs. traditional methods

3.2.1 High-voltage generation

Three-phase voltage-source drives with or without variable frequency are usually driven by classical three-phase converters or NPC converters. If high currents (>2kA) are demanded, the switches used in these converters (usually GTO or IGCT) are set on parallel, in order to obtain a multiple of the current passing through a single switch. The voltage applied to the motor will always remain the same and will be limited to the semiconductor blocking voltage. If a high voltage has to be applied to the motor, the voltage has to be risen on the AC side by a transformer. A true-series connection of the semiconductor is a very difficult problem. The voltage-sharing problem on each semiconductor has yet not been resolved and has never been implemented on an industrial drive. But the use of an additional transformer adds new costs to the system and introduces new problems to the system such as additional losses, stray inductance and capacitors. The side effects have to be compensated by the control system.

By using a multilevel converter as proposed in this thesis, the a very high voltage can be applied to the motor. The series-connection of the four-quadrant converters allows to achieve a multiple of the blocking voltage, without any problems of the voltage-sharing on the true-series connection. So the demanded power is shared equally on a number of four quadrant converters.

3.2.2 High-quality voltage generation

The converters used for motor drives have furthermore the disadvantage of poor voltage and current qualities. The semiconductor switches are usually commutated at low frequencies such as 100Hz up to 500Hz. To improve the voltage quality, the switching frequency has to be risen and so will cause more switching losses. In the present high-power drive solutions, a switching frequency filter is introduced between the converter and the motor. This filter allows to obtain sufficient voltage and current quality, but adds a new, expensive component to the system. Furthermore the filter will add more resonant poles to the entire system, the system transfer function becomes a higher order. These poles can be compensated by the control algorithm [30], but will introduce some limitations and a reduction of control performance, especially in the dynamic variable-speed application.
A three-phase multilevel converter consists of four-quadrant converters, which can all be switched independently. This advantage can be used in order to generate AC voltage of much higher quality. The use of independent phase-shifted triangular carrier signals for each half-bridge converter allows a much higher resulting switching frequency on the motor voltages. The effective switching frequency f_s remains low, while the resulting frequency is a multiple of this switching frequency. The converter system can so avoid a complicated filter setup and can directly be connected to the motor. Furthermore, the switching is distributed to a big number of smaller switches. If it can be considered that the switching losses increase exponentially with the choice of bigger semiconductors, the multilevel converter scheme will generate fewer switching losses than a comparable classical type, and even generating a far better voltage quality, seen in Table (3.2.3).

The disadvantage of the three-phase multilevel converter is the more or less complicated setup with many switches. This does not only raise the costs, but it also can lower the systems reliability. Each additional electronic switch has its reliability and its MTTF failure time. For the same reliability as a classical system, more reliable switches are needed.

3.2.3 Feeding of the multilevel converter cells

Depending on the type of three-phase converter used, different voltage feeding sources must be provided. The most simple feeding as a single DC source. A single source is used for the classical three-phase voltage converter, using 6 power switches. For the multilevel converter, many isolated DC power sources must be provided. Different types of feeding strategies are already presented in Section 2.3, for all kinds of sources. A very interesting feeding method was presented in [21], using a polyphase transformer. The following Table (3.2.3) shows an comparative overview between the classical converter, the NPC converter type [13] and the here presented multilevel on the symmetrical fed SCFQ principle. The explication for the number of phasor points seen in the Table (3:2.3) is shown later this chapter.

	classical	NPC	multilevel n=2	multilevel n=3
Number of DC power supplies	1	1	6	9
DC supply voltage	U_{dc2}	$2 \cdot U_{dc2}$	U_{dc2}	U_{dc2}
type of DC source	single DC	DC with neutral point	6 floating DC	9 floating DC
switch blocking voltage	U_{dc2}	U_{dc2}	U_{dc2}	U_{dc2}
Maximal amplitude line voltage	U_{dc2}	$2 \cdot U_{dc2}$	$2 \cdot U_{dc2}$	$3 \cdot U_{dc2}$
Maximal amplitude line-line voltage				
Number of switches	6	12	24	36
Number of diodes	6	18	24	36
THD line-line voltage	64.7%	39.5%	16.7%	9.8%
Number of phasor points	7	19	61	127

Table 3.1: Comparison of four different converter topologies

3.2.4 Applications

High-voltage high-power industrial drives

A typical application for the multilevel converter is the high-voltage industrial drive. Due to the addition of several independent voltages, automatically a high voltage can be achieved. By putting some four-quadrant converters in parallel, also the current can be multiplied by the number of cells in use. The industrial drive takes automatically the advantage of the high resolution of the voltage, which allows currents of higher qualities. This topology is actually an approach for a modular three-phase multilevel converter, where any desired power can be delivered.

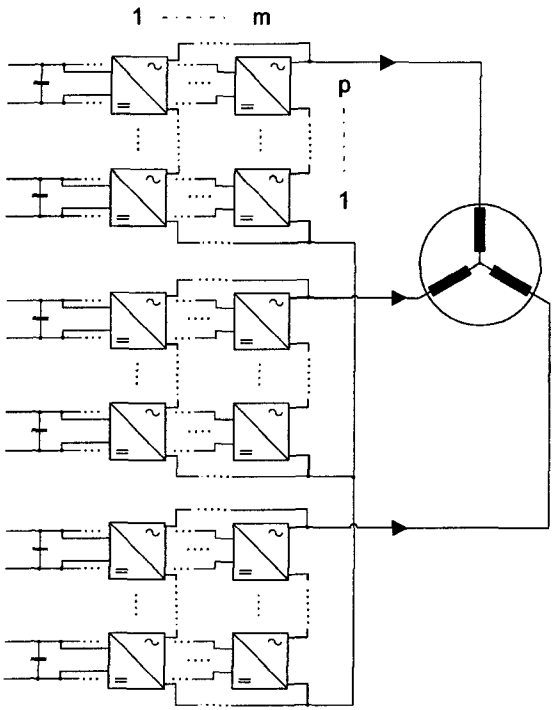

Figure 3.1: Modular three-phase multilevel converters

High-speed drives for ironless motors

In some applications, an excellent voltage quality is demanded. A good voltage quality can be achieved by using switching frequency filters or by a using special three-phase

power transformer with changeable configuration. The multilevel converter can solve this problem without any additional passive components. So the system can reduce the costs and saves a lot of space. A typical application is a drive topology to feed ironless motors, turning at very high speed (200'000 rpm). A ironless motor can for instance consists of a hallbach magnetical array. This is a motor setup designed for very high speeds, but the feeding voltage has to be of excellent quality due the weak inductance values of the phase windings.

3.3 Describing equations of the converter

In this chapter, all the equations are given in order to design an entire three-phase multilevel converter. The four-quadrant converters of the multilevel converter are considered to be fed by independent DC-DC converters. The next figure shows this converter with all possible electrical values:

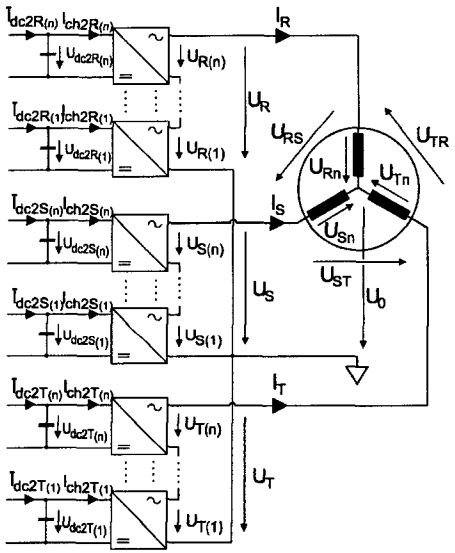

Figure 3.2: Three-phase multilevel converter system

Each phase of the multilevel converter consists of an single-phase multilevel structure. There are three times n four-quadrant converters fed by n DC-DC converters. For each four-quadrant converter, there is a feeding capacitor $C_{dc2R,S,T}$. The phase voltage is the sum of all the four-quadrant AC voltages.

$$U_R = \sum_{i=1}^{n} U_{R(i)} \tag{3.1}$$

$$U_S = \sum_{i=1}^{n} U_{S(i)} \tag{3.2}$$

$$U_T = \sum_{i=1}^{n} U_{T(i)} \tag{3.3}$$

The AC voltage generated by the four-quadrant converter depends on the DC voltage of the feeding $U_{dc2R,S,T}$, the modulation degrees $k_{R,S,T}$, the frequency of the modulation signal and the blanking time $\tau_{blank(4Q)}$. It is assumed that the modulation signal is sinusoidal.

$$U_{R_{(n)}} = U_{dc2R_{(n)}} \sin(2\pi f_{mod} t + \varphi_R) \cdot (k_R - \tau_{blank(4Q)} f_s) \tag{3.4}$$
$$U_{S_{(n)}} = U_{dc2S_{(n)}} \sin(2\pi f_{mod} t + \varphi_S) \cdot (k_S - \tau_{blank(4Q)} f_s) \tag{3.5}$$
$$U_{T_{(n)}} = U_{dc2T_{(n)}} \sin(2\pi f_{mod} t + \varphi_T) \cdot (k_T - \tau_{blank(4Q)} f_s) \tag{3.6}$$

The four-quadrant converters of one phase are usually modulated by the same function (A sinusoidal signal). A three-phase multilevel converter, where each four-quadrant converter has its own modulation signal is not discussed in this thesis. The currents on the DC side of the four-quadrant converter are given by the next expression:

$$\overline{I}_{ch2R_{(n)}} = I_R(t) \cdot \sin(2\pi f_{mod} t + \varphi_R) \cdot (k_R - \tau_{blank(4Q)} f_s) \tag{3.7}$$
$$\overline{I}_{ch2S_{(n)}} = I_S(t) \cdot \sin(2\pi f_{mod} t + \varphi_S) \cdot (k_S - \tau_{blank(4Q)} f_s) \tag{3.8}$$
$$\overline{I}_{ch2T_{(n)}} = I_T(t) \cdot \sin(2\pi f_{mod} t + \varphi_T) \cdot (k_T - \tau_{blank(4Q)} f_s) \tag{3.9}$$

This expression gives an average value of the current and does not depend on the modulation method . The only input given from the modulation method is the modulation degree $k_{R,S,T}$ and the fact that the modulation function is sinusoidal. In this thesis, only the symmetrical multilevel converter is looked at (all DC voltages are identical):

$$U_{dc2} = U_{dc2R_{(i)}} = U_{dc2S_{(i)}} = U_{dc2T_{(i)}} \qquad \forall i \qquad 1 < i < n \tag{3.10}$$

If multilevel converter has to be understood better, a normalized voltage vector $\underline{u}$ is defined, which can be represented in the three-dimensional space.

$$\underline{u} = (u_R, u_S, u_T) = \left(\frac{U_R}{U_{dc2}}, \frac{U_S}{U_{dc2}}, \frac{U_T}{U_{dc2}}, \right) \tag{3.11}$$

Each phase of the multilevel converter with n steps generates $n_{voltage}$ different voltage steps:

$$n_{voltage} = 2n + 1 \tag{3.12}$$

So typically one phase of the multilevel converter with $n = 2$ four-quadrant converters can generate the voltages $2U_{dc2}$, U_{dc2}, 0, $-U_{dc2}$ and $-2U_{dc2}$. The phases R,S and T are each considered as the axes of a three-dimensional, orthogonal coordinate system x, y, and z. For each possible voltage vector, a reference point in the three-dimensional coordinate system can be set. The grid in the three-dimensional coordinate system consists of many voltage vector points:

$$3^{n_{voltage}}\Big|_{n_{voltage}=5} = 125 \tag{3.13}$$

The next Figure (3.3) visualizes the grid in the three-dimensional system.

This three-dimensional grid contains a lot of information that can be used. If somebody looks at this grid from the direction of the vector $\underline{n} = (1, 1, 1)$, there are only 61 points which can be seen. Many of the 125 vector points are now hidden behind other points. These visible vector points correspond to the phasor vector points.

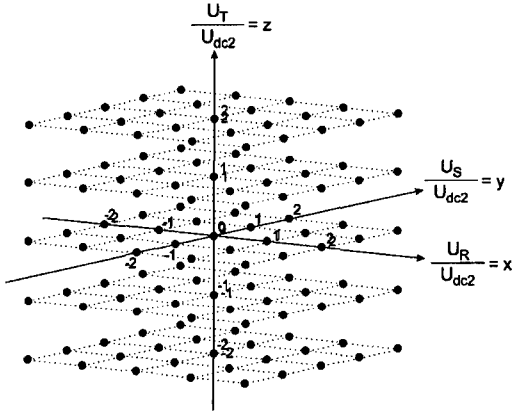

Figure 3.3: Three-dimensional coordinate system showing 125 vector points

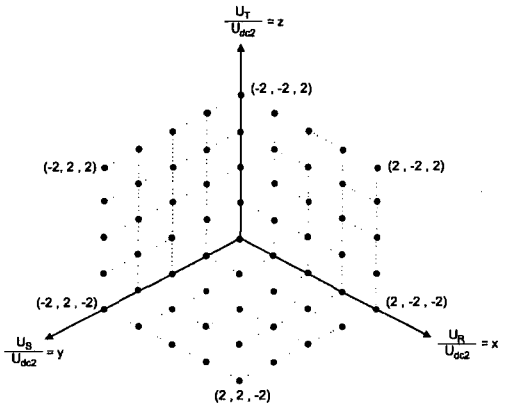

Figure 3.4: 61 vector points seen from the view angle (1,1,1)

The phasor vector points in a two-dimensional coordinate system are visualized, but still the three-dimensional coordinates can be seen. By solving the well-known Equations (3.14) and (3.15), the voltage vector coordinates (u_R, u_S, u_T) are transformed to the phasor points (u^s_α, u^s_β).

$$u^s_\alpha = \frac{U^s_\alpha}{U_{dc2}} = \frac{2u_R - u_S - u_T}{3} \tag{3.14}$$

$$u^s_\beta = \frac{U^s_\beta}{U_{dc2}} = \frac{u_S - u_T}{\sqrt{3}} \tag{3.15}$$

The two-dimensional coordinate axes are visualized in Figure (3.5):

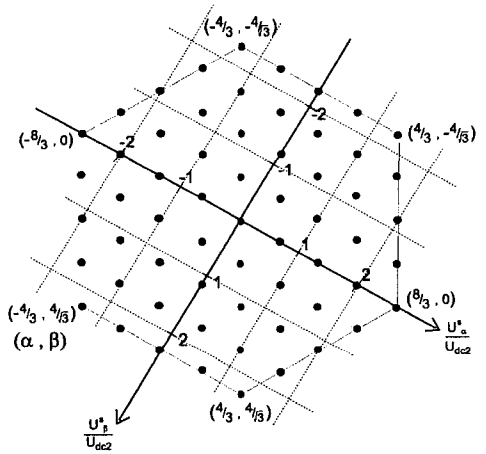

Figure 3.5: 61 phasor points in the coordinate system (u_α^s, u_β^s)

The number of visible points depends on the number of multilevel steps. Equation (3.16) gives the number of points:

$$n_{phasor} = 1 + 6 \cdot \sum_{i=odd}^{2n-1} (2i+1) \tag{3.16}$$

So there are several phasor points (u_α^s, u_β^s) , which can be represented by a multiple of voltage vector points (u_R, u_S, u_T). The most typical example is the zero voltage phasor point, which can be represented by five different voltage vectors. This is shown in Table (3.2)

$\frac{U_R}{U_{dc2}}$	$\frac{U_S}{U_{dc2}}$	$\frac{U_T}{U_{dc2}}$	$\frac{U_\alpha^s}{U_{dc2}}$	$\frac{U_\beta^s}{U_{dc2}}$
2	2	2		
1	1	1		
0	0	0	0	0
-1	-1	-1		
-2	-2	-2		

Table 3.2: Zero voltage phasor with 5 different voltage vector points

If all three phase voltages increase or decrease the voltage by one voltage together, the phasor voltage has the same value, as to be seen in the Equations (3.14) and (3.15). This can be repeated, until one position of the voltage vector exceeds the maximal boundaries

$(\pm n, \pm n, \pm n)$. So the number of possible voltage vectors for a defined voltage vector point is n_s:

$$n_s = n_{voltage} - (max(u_R, u_S, u_T) - min(u_R, u_S, u_T)) \tag{3.17}$$

If all phasor points are classified by number of existing voltage vector solutions, it can be seen that the points can be grouped in hexagons. The hexagons shall be indexed by the number n_h. The smaller the hexagon index number is, the more switching redundancy there is. So for the inner hexagon $n_h = 0$, which is actually only one point, there are five different possibilities n_s to generate the phasor vector $(0, 0)$.

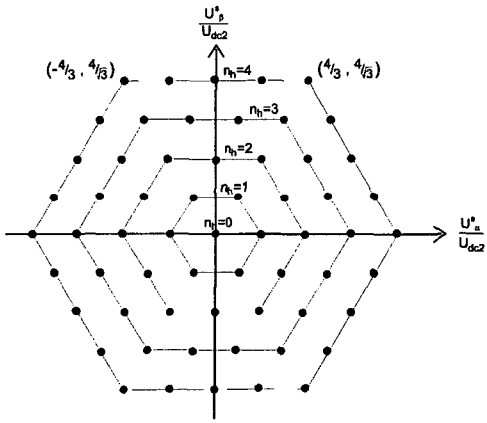

Figure 3.6: The phasor points are classified in hexagons

The grid with the $n_{voltage}{}^3$ different vector points contains more information. By using the Equations (3.14) and (3.15), from three variables (u_R, u_S, u_T) only two new parameters are calculated. There is one degree of liberty. The missing parameter is the neutral point voltage, calculated as follows:

$$u_0 = \frac{1}{3}(u_R + u_S + u_T) \tag{3.18}$$

If the angle of view on the grid is modified, the neutral point voltage u_0 can be viewed. If a voltage vector point is chosen, the belonging neutral-point voltage u_0 corresponds to the distance from the chosen vector point to an orthogonal surface to the vector $\underline{n} = (1, 1, 1)$. This surface is given by the Equation (3.19):

$$u_R + u_S + u_T = 0 \tag{3.19}$$

The next Figure (3.7) visualizes the normalized neutral point voltage u_0

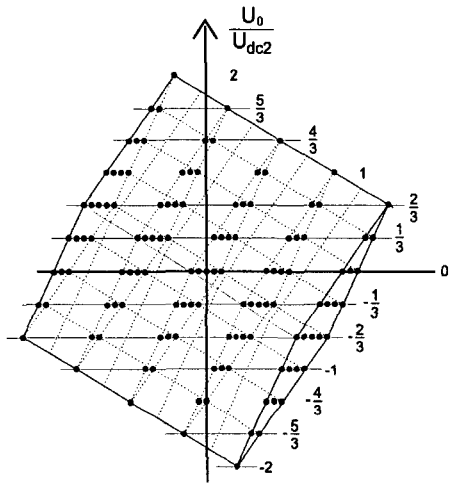

Figure 3.7: Visualization of the neutral point voltage

The neutral point vector is always parallel to the direction $\underline{n} = (1, 1, 1)$. To see the neutral point vector without any distortion, the grid has to be viewed from a vector lying in a plane going through (0,0,0) and orthogonal to $\underline{n} = (1, 1, 1)$.

3.4 Modulation methods

For the multilevel converter, different modulation methods can be used to drive an induction motor or another three-phase load. Three different methods have been studied, tested and compared. Each of them have different advantages, depending on the application type.

3.4.1 PWM modulation

The first modulation method, which is described, is the PWM modulation. For one four-quadrant converter, consisting of four semiconductor switches with the anti-parallel diode, two carrier signals are needed. The carrier signals with horizontal phase shift are already defined with Equation (2.28). One half-bridge is responsible for generating the positive voltage an the other one for the negative part of the AC voltage. For the phase R of the multilevel converter, there are n steps, each with 2 triangles. The phase angles used are given by the following Equation:

$$\Delta\varphi_{R(i)} = \frac{360^o}{2n} \cdot i \tag{3.20}$$

The next two Equations show the phase shift for the other two phases of the converter:

$$\Delta\varphi_{S(i)} = \frac{360^o}{2n} \cdot i + \frac{360^o}{3n} \tag{3.21}$$

$$\Delta\varphi_{T(i)} = \frac{360^o}{2n} \cdot i + \frac{360^o}{6n} \tag{3.22}$$

This is a simple PWM method for the three phase multilevel converter. More sophisticated PWM modulation methods have been presented in [32] for a classical three phase converter. The chosen carrier signals are not triangular waveforms, but have a saw-tooth waveform. There is only a phase-shift of the carriers between each half-bridge of one phase, but between the phases the same carriers without phase-shift are found. Special over-modulation strategies are implemented to linearize the modulation.
Independent on the PWM modulation strategy chosen, it has to be assured that there is never a situation where one half-bridge voltage cancels another one. This means for that one half-bridge is generating a positive voltage, while the other half-bridge generates a negative voltage. On the AC side of one phase of the converter, this would generate no voltage, but the current will still run trough both full-quadrant converters. In this way, the DC feeding part delivers two times a equivalent power causing additional switching and conduction losses. On the AC side, the power will circulate from one half-bridge to the other half-bridge. But the output power on the AC side will remain zero (Described in the chapter of the single-phase converter, page 33).
This can be avoided by using not only horizontal-shifted (this means phase-shifted carriers, to be seen in Section 2.4.2) triangular carrier signals. The carriers are also distributed vertically over the range $[0, 1]$ for the generation of the positive voltage steps and over the range $[-1, 0]$ for the negative ones.

3.4.2 Step modulation

The step modulation for the three-phase multilevel converter does not need any further explanations compared to the single-phase version of this modulation type. The same principle can be use, it just has to be expanded to three independent phases. Details are given in Section 2.4.1.

3.4.3 Vector modulation

For the classical converter consisting of six power semiconductors, a special modulation method called the vector modulation or online modulation was proposed. This type of modulation presents some advantages comparing to the two other modulation types. This method has been presented the first time in [33]. The vector modulation is especially suited to be implemented in a fast processor with real time modulation and vector control at the same time.
To perform the vector modulation, the phasor voltage plane has to be considered. A reference voltage in form of a phasor vector $\underline{u}_{ref}$ has to be generated in the phasor plane (α, β). This vector is normalized to the DC feeding voltage U_{dc2}.

$$\underline{u}_{ref} = \begin{bmatrix} \frac{U_{ref_x}}{U_{dc2}} \\ \frac{U_{ref_y}}{U_{dc2}} \end{bmatrix} = \begin{bmatrix} u_{ref_x} \\ u_{ref_y} \end{bmatrix} \tag{3.23}$$

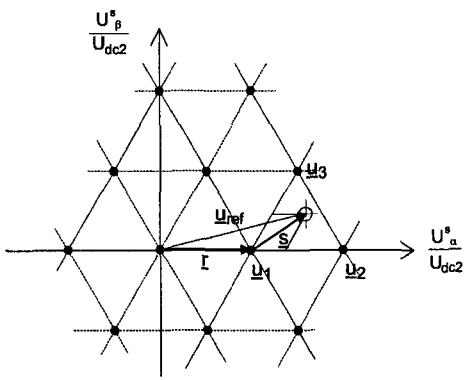

Figure 3.8: Decomposition of the reference vector in two smaller ones

At the same time, the entire phasor plane has to be divided into triangles, as to be seen in the Figure (3.8). The reference vector $\underline{u}_{ref}$ has to be decomposed into two new vectors: A part $\underline{r}$ of the vector pointing to a corner of the triangle, and a part $\underline{s}$ going from the corner point to the reference vector:

$$\underline{u}_{ref} = \underline{r} + \underline{s} \tag{3.24}$$

The vector $\underline{s}$ will now be decomposed in two components $\underline{a}$ and $\underline{b}$, which are lying on the sides of the triangle. The vector $\underline{s}$ is a linear combination of the two new vectors $\underline{a}$ and $\underline{b}$:

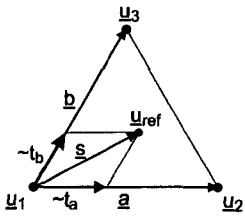

Figure 3.9: Vector decomposition inside the triangle

The Equation (3.25) below gives the decomposition:

$$\underline{s} = t_a\underline{a} + t_b\underline{b} = t_a \begin{bmatrix} a_x \\ a_y \end{bmatrix} + t_b \begin{bmatrix} b_x \\ b_y \end{bmatrix} \tag{3.25}$$

Vector $\underline{s}$ is the vector going from vector point $\underline{u}_1$ to the point $\underline{u}_{ref}$:

$$\underline{s} = \begin{bmatrix} s_x \\ s_y \end{bmatrix} = \underline{u}_{ref} - \underline{u}_1 = \begin{bmatrix} u_{ref_x} - u_{1_x} \\ u_{ref_y} - u_{1_y} \end{bmatrix} \tag{3.26}$$

The two time coefficients t_a and t_b are calculated by the projection parallel to the triangle sides. According to Equations (3.27) and (3.28) the time values are:

$$t_b = \frac{s_x a_y - s_y a_x}{b_x a_y - b_y a_x} \tag{3.27}$$

$$t_a = \frac{s_x b_y - s_y b_x}{a_x b_y - a_y b_x} \tag{3.28}$$

The idea of the vector modulation is to represent the vector $\underline{u}_{ref}$ by the three points of the triangle. The vector points are the corners of the reference triangle. The two variables t_a and t_b represent the relative time values to modulate the vector $\underline{u}_{ref}$. In accordance to Figure (3.9), t_a is proportional to the time, where $\underline{u}_2$ is applied and t_b is the time for the vector $\underline{u}_3$. These time values are normalized between [0..1] and have to be adapted to the sampling frequency of the modulator:

$$T_a = t_a \cdot T_{sample} \tag{3.29}$$

$$T_b = t_b \cdot T_{sample} \tag{3.30}$$

If these two times are subtracted from the sampling time, the remaining time T_c results:

$$T_c = T_{sample} - T_a - T_b \tag{3.31}$$

During the remaining time T_c, the reference vector will be put to the phasor vector $\underline{u}_1$. So the rotating reference vector in the complex phasor plane can be reconstructed by a sequence of three voltage points:

$$\underline{u}_{ref} = \frac{1}{T_{sample}}(T_a \cdot \underline{u}_2 + T_b \cdot \underline{u}_3 + T_c \cdot \underline{u}_1) \tag{3.32}$$

Each sampling period, the three time values are recalculated. By averaging the voltage vector over each time period, the result will be exactly the vector $\underline{u}_{ref}$.

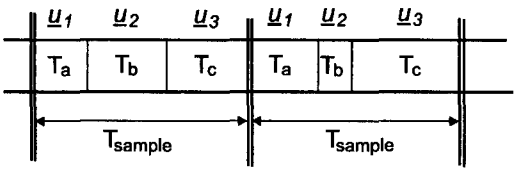

Figure 3.10: Time sequence over two sampling periods

Finding the three points of the reference triangle

As to be seen in the Figure (3.8) the reference vector is pointed into a defined triangle, called the reference triangle. Three different points define this triangle, each point is corresponding to a three-phase output voltage vector. An algorithm has been established to define the triangle with the three vector points.

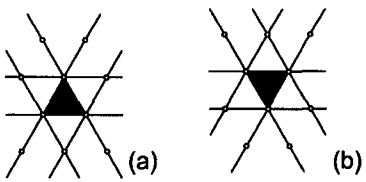

Figure 3.11: Six different lines are defining the triangle

As to be seen in the Figure (3.11), there are six lines describing the triangle. These lines have to be specified by the basic linear Equation (3.33). First the horizontal lines are determined.

$$y = a \cdot x + b \tag{3.33}$$

For the horizontal lines, the coefficient a is trivially:

$$a^h_{u,l} = 0 \tag{3.34}$$

The upper index h is representative for horizontal line, the lower indexes l, u are representing the lower and upper line. For the lower line, the coefficient b is:

$$b^h_l = u_{ref_y} - \left(u_{ref_y} \bmod \frac{1}{\sqrt{3}} \right) \tag{3.35}$$

And the coefficient b for the upper line is:

$$b^h_u = b^h_l + \frac{1}{\sqrt{3}} \tag{3.36}$$

The rising lines, represented by the upper index r, the following coefficients can be found:

$$\begin{aligned} a^r_{u,l} &= \sqrt{3} \\ b^r_l &= u_{ref_y} - \sqrt{3} \cdot u_{ref_x} - \left[\left(u_{ref_y} - \sqrt{3} \cdot u_{ref_x} \right) \bmod \left(\frac{2}{\sqrt{3}} \right) \right] \\ b^r_u &= b^r_l + \frac{2}{\sqrt{3}} \end{aligned} \tag{3.37}$$

And at last, the falling lines (index f) have the coefficients:

$$\begin{aligned} a^f_{u,l} &= -\sqrt{3} \\ b^f_l &= u_{ref_y} + \sqrt{3} \cdot u_{ref_x} - \left[\left(u_{ref_y} + \sqrt{3} \cdot u_{ref_x} \right) \bmod \left(\frac{2}{\sqrt{3}} \right) \right] \\ b^f_u &= b^f_l + \frac{2}{\sqrt{3}} \end{aligned} \tag{3.38}$$

If all these lines are crossed and the crossing points are calculated, six points will be found. Only three of these points are defining the reference triangle. There are two orientation possibilities, both shown in Figure (3.11). To classify whether the triangle is in situation (a) or in situation (b), the following procedure has to be followed:
The higher rising line y^r_u has to be crossed with the higher horizontal line y^h_u. Then the upper falling line y^f_u will be crossed with the same horizontal line y^h_u. If the two points are the same, then the triangle is oriented like in (a) of Figure (3.11), if the two points are different, the triangle is oriented like (b) in Figure (3.11). By using this information, all the three points of the desired triangle can be calculated.
The modulation index has to be defined for this modulation method. The modulation vector $\underline{u}_{ref}$ is limited to a certain amplitude for this application. It never goes into over-modulation. The maximal modulation degree is defined by the phasor touching the middle of the line of the hexagon border. It is the longest possible vector, which never leaves the boundary of the outer hexagon in Equation (3.39):

$$\hat{\underline{u}}_{ref} = max\left(\sqrt{{u_{ref_x}}^2 + {u_{ref_y}}^2} \right) = \frac{n_{voltage} - 1}{\sqrt{3}} \tag{3.39}$$

Overmodulation methods were already discussed in [34] and [35] for classical converters and have not been tested in this paper. The same methods could be used for the multilevel converter. The definition of the modulation degree k for the reference vector $\underline{u}_{ref}$ is:

$$k = \frac{n_{voltage} - 1}{\sqrt{3}} \cdot \frac{1}{\sqrt{u^2_{ref_x} + u^2_{ref_y}}} \tag{3.40}$$

For the case where $n = 2$, the maximal value for $\underline{u}_{ref}$ is $\frac{4}{\sqrt{3}}$, while the modulation degree would be $k = 1$.

Optimized switching to minimize the number of voltage switching

By implementing the vector modulation, there is a possibility to minimize the number of voltage commutations per sampling period. Two specialities of the three-phase ML-converter can be used:

- Many of the phasor points (U_α^s, U_β^s) can be generated by a set of different voltage vectors (u_R, u_S, u_T), as to be seen in Section 3.3. This redundancy can be used to reduce the number of switching events per period.
- In each sampling period, three different voltage vectors $\underline{u}_1$, $\underline{u}_2$ and $\underline{u}_3$ are switched. The temporal order, seen in Figure (3.10) in which these voltages are applied, is free and can be used for the switching optimization.

In each sampling period, three points $\underline{u}_1$, $\underline{u}_2$ and $\underline{u}_3$ of the reference triangle will be chosen. In order to reduce switching losses, this time sequence is optimized together with the redundant switching patterns for the phasor. Theoretically this can be done by comparing all the possible solutions. But this can take a lot of processing time. So the following algorithm is presented, which will optimize the voltage switching to a minimum. The difference vector between two points is expressed by Equation (3.41):

$$\Delta\underline{u} = (\Delta u_R, \Delta u_S, \Delta u_T) = (u_{Rnew} - u_{Rlast}, u_{Snew} - u_{Slast}, u_{Tnew} - u_{Tlast}) \quad (3.41)$$

The following Equation expresses the number of switched voltage levels when changing from one vector point $\underline{u}_{last}$ to the next one $\underline{u}_{new}$:

$$n_c = abs(u_{Rlast} - u_{Rnew}) + abs(u_{Slast} - u_{Snew}) + abs(u_{Tlast} - u_{Tnew}) \quad (3.42)$$

The aim is to minimize the number of commutations n_c:

$$n_{c_{min}} = min\,(abs(\Delta u_R) + abs(\Delta u_S) + abs(\Delta u_T)) \quad (3.43)$$

In the Section 3.3 it could be seen, that some of the phasor vectors can be represented by a set of voltage vectors. By adding or subtracting a constant to a voltage vector, the same phasor results:

$$\underline{u}_{new} = (u_{Rnew}, u_{Snew}, u_{Tnew}) \equiv (u_{Rnew}+k_n-k_c, u_{Snew}+k_n-k_c, u_{Tnew}+k_n-k_c) \quad (3.44)$$

The vector $(u_{Rlast}, u_{Slast}, u_{Tlast})$ is already applied to the load from the past sampling period and cannot be changed to optimize the switching. But the voltage vector position of $\underline{u}_{new}$ can still be chosen. The fewest voltage switching is done if the next Equation (3.45) is respected:

$$n_{c_{min}} = min\,(|\underline{u}_{last} - \underline{u}_{new}|) \quad (3.45)$$

Equation (3.45) means that the geometrical distance in the three dimensional coordinate system $(x = u_R, y = u_S, z = u_T)$ between the new voltage vector $\underline{u}_{new}$ and the last one $\underline{u}_{last}$ has to be minimized. The proposed algorithm can only work, if the neutral point voltage is not modulated or fixed to a constant value. In this way the redundancy

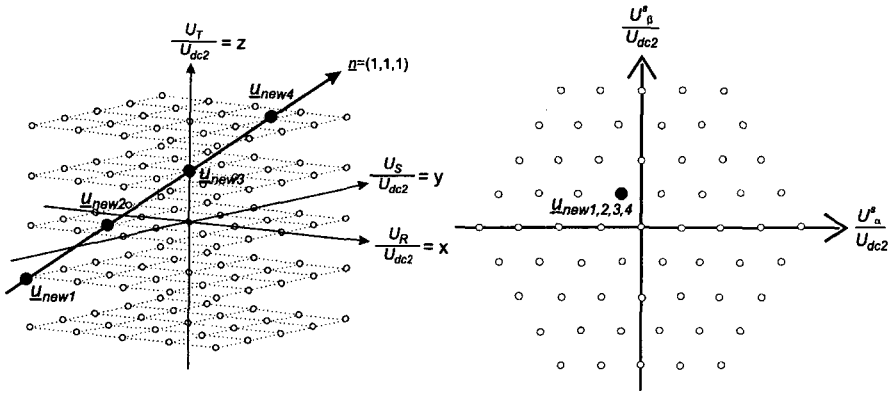

Figure 3.12: One phasor point represented by 4 voltage vectors

of phasor points can be used. The final goal is to execute the fewest possible voltage commutations.
The first step is to identify the three possible voltage vectors $\underline{u}_1$, $\underline{u}_2$ and $\underline{u}_3$ from the triangle of interest. After using the algorithm to identify the three phasor points of the triangle, three voltage vectors $\underline{u}_1$, $\underline{u}_2$ and $\underline{u}_3$ can be calculated. The detected phasor point (U^s_α, U^s_β) has now to be converted to a voltage vector point (u_R, u_S, u_T). This can be done either by implementing a look-up table or by using the Equations (3.14), (3.15) and (3.18). For this cause, the normalized neutral point voltage u_0 has to be set to zero. By setting the neutral-point voltage to zero, it is possible that the voltage vector found is not composed of entire numbers. In this case it cannot be generated by the multilevel converter. This fact can be seen in Figure (3.7), where only 19 different voltage vector points generate $u_0 = 0$. But for the algorithm this does not make any problems. It is known, that all the points on the vector $\underline{n} = (1, 1, 1)$ generate the same phasor point. So three vectors are defined, which are pointed in the direction $\underline{n} = (1, 1, 1)$ and go through the three points $\underline{u}_1$, $\underline{u}_2$ and $\underline{u}_3$.

$$\underline{r}_1 = \underline{u}_1 + l_1\underline{n} = \begin{cases} x = u_{R1} + l_1 \\ y = u_{S1} + l_1 \\ z = u_{T1} + l_1 \end{cases} \tag{3.46}$$

The two other lines are:

$$\underline{r}_2 = \underline{u}_2 + l_2\underline{n} \tag{3.47}$$

$$\underline{r}_3 = \underline{u}_3 + l_3\underline{n} \tag{3.48}$$

The vector $\underline{u}_n$ represents the voltage vector point (u_{Rn}, u_{Sn}, u_{Tn}) from the chosen triangle, while l_n represents a distance in direction $\underline{n} = (1, 1, 1)$.
The voltage vector point, which is geometrically the closest to $\underline{u}_{last}$, has to be found. So this new vector voltage point must be on a surface (or has to be as close as possible to

a surface) going through the last applied vector point u_{last} and is orthogonal to n. The Equation for this surface is given below:

$$0 = x + y + z - u_{Rlast} - u_{Slast} - u_{Tlast} \tag{3.49}$$

By cutting the surface in Equation (3.49) with the three vectors in Equation (3.46) and (3.48), the three nearest points to the vector u_{last} are found.

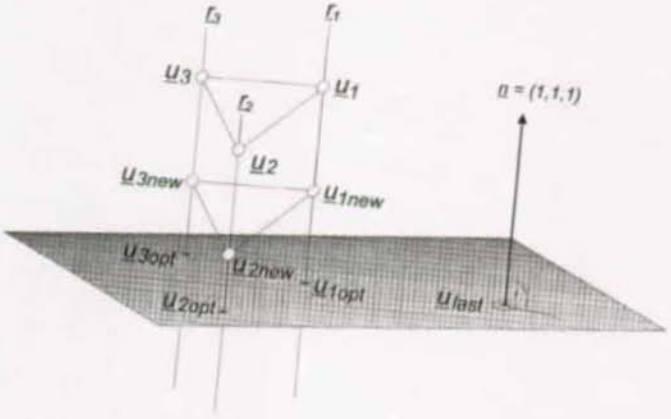

Figure 3.13: Searching the nearest points from the last voltage vector u_{last}

By introducing the Equations (3.46) (3.48) into the surface Equation (3.49), the vectors r_n will cut the surface and three values l_1, l_2 and l_3 will be found. By reintroducing l_1, l_2 and l_3 into the Equations (3.46) (3.48), the closest points to the vector u_{last} are found. But these points have to be an entire number, so that the multilevel converter can generate the voltage. This is done by rounding all three values to the next entire number:

$$k_{n1,2,3} = round(l_{1,2,3}) \tag{3.50}$$

This parameter has to be introduced into the Equation (3.44). The first three vectors u_{1new}, u_{2new} and u_{3new} are found. Now it has to be found out, whether the generated voltage vector is produceable by the ML-converter or if it is outside of the grid. The correction parameter for this is $k_{c1,2,3}$. If the calculated vector is an existing one, the correction parameter is:

$$k_{c1,2,3} = 0 \tag{3.51}$$

If the generated voltages are higher than the number of full-bridges per phase, the point will be outside of the grid. The voltage can obviously not be generated. The voltage vector has to be corrected by:

$$k_{c1,2,3} = max(u_{1new,2new,3new}) - \frac{n_{voltage} - 1}{2} \tag{3.52}$$

For instance if the vector $\underline{u}_{1new}$ is $(3,1,1)$ and the ML-converter consists of two four-quadrant converters per phase, so the correction factor k_{c_1} is $3-2=1$. The new vector $\underline{u}_{1new}$ will be $(2,0,0)$.
To find the final voltage vector, k_n and k_c have to be introduced in (3.44). The last point in the algorithm is to find out, which voltage from the three new voltages $\underline{u}_{1new}$, $\underline{u}_{2new}$ and $\underline{u}_{3new}$ is selected first in the sampling period. The voltage vector to be applied at first is the one with the shortest distance to $\underline{u}_{last}$. The last one is the one with the longest distance. The distances are calculated by the Equation set (3.53):

$$\begin{aligned} d_{1new} &= |\underline{u}_{last} - \underline{u}_{1new}| \\ &= \sqrt{(u_{Rlast} - u_{R1new})^2 + (u_{Slast} - u_{S1new})^2 + (u_{Tlast} - u_{T1new})^2} \\ d_{2new} &= |\underline{u}_{last} - \underline{u}_{2new}| \\ &= \sqrt{(u_{Rlast} - u_{R2new})^2 + (u_{Slast} - u_{S2new})^2 + (u_{Tlast} - u_{T2new})^2} \\ d_{3new} &= |\underline{u}_{last} - \underline{u}_{3new}| \\ &= \sqrt{(u_{Rlast} - u_{R3new})^2 + (u_{Slast} - u_{S3new})^2 + (u_{Tlast} - u_{T3new})^2} \end{aligned} \tag{3.53}$$

The voltage $\underline{u}_{new}$ with the shortest distance d to $\underline{u}_{last}$ will now be applied first. The next voltage is the one with the intermediary distance to $\underline{u}_{last}$, and the last one is the point which has the largest distance. By following this algorithm, the fewest possible voltage switching is done.

Optimized switching to minimize the switched power

Instead of optimizing the voltage switching, the switched power can be optimized. The aim is to guarantee that in each period the fewest possible power is switched. With other words, the difference between the sum of the power of one switching event to the next one shall be minimized. The method is based on the same principles shown in the method before, but now the converter phase voltage is additionally multiplied by the according phase current. In each sampling period, the normalized voltage grid $\underline{u} = (u_R, u_S, u_T)$ is multiplied by the present current values $\underline{I} = (I_R, I_S, I_T)$, which can be measured by the system. The current values can also be normalized $\underline{i} = (i_R, i_S, i_T)$ and then be multiplied by the normalized voltage. The normalization of the voltage values although is necessary in order to get entire values. So the new, three-dimensional grid is composed of the axes:

$$\underline{p} = (p_R, p_S, p_T) = (u_R \cdot I_R, u_S \cdot I_S, u_T \cdot I_T) \qquad [A] \tag{3.54}$$

The voltage values are entire numbers (converter voltages), while the current values are continuous. So the new power grid consists of vector points in amperes $[A]$, which do not consist of entire numbers. In the same time, the distances of the points in direction x,y and z are not the same anymore. This due to the fact that all the three currents I_R, I_S and I_T have rarely the same value. The grid is visualized by the following images:

Figure (3.14) show all the 125 possible power vector points. The three used currents for this example are: $I_R = 6[A]$, $I_S = 1[A]$ and $I_T = -7[A]$, while the DC voltage step U_{dc2} is set at 200V. It can be seen that any movement in the direction $z = T$ will switch seven times more power that in direction $y = S$. By looking at the grid from the

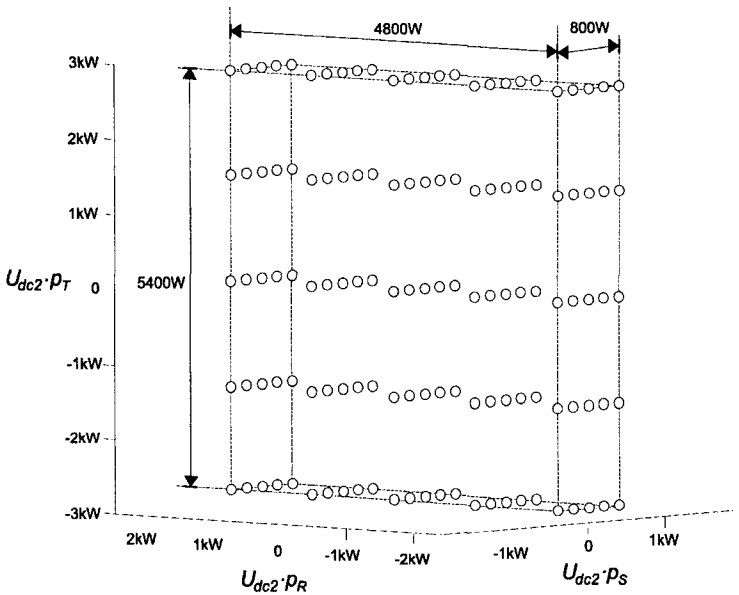

Figure 3.14: All possible power vector points on grid

direction $\underline{n}_{power} = (I_R, I_S, I_T)$ the phasor representation of the grid can be viewed. In Figure (3.15), still the three orthogonal axes R, S and T are displayed.

The Figure (3.16) shows the grid with the phasor axes defined with the Equation (3.55):

$$(P^s_\alpha, P^s_\beta) = (p^s_\alpha \cdot U_{dc2}, p^s_\beta \cdot U_{dc2}) \qquad [W] \tag{3.55}$$

This phasor points are defined by the following Equation set:

$$p^s_\alpha = \frac{P^s_\alpha}{U_{dc2}} = \frac{2p_R - p_S - p_T}{3} \tag{3.56}$$

$$p^s_\beta = \frac{P^s_\beta}{U_{dc2}} = \frac{p_S - p_T}{\sqrt{3}} \tag{3.57}$$

By representing the grid in the direction $\underline{n}_{power}$, again only 61 points can be seen.

The losses of a semiconductor are depending more or less linearly on the switched current and voltage. This has been shown in several publications like [36]. A base to compute the losses is given in Appendix A.7. That is why this method could reduce the switching losses to a minimal value.

$$E_{turn-on,turn-off} \sim U_{ce} I_c \tag{3.58}$$

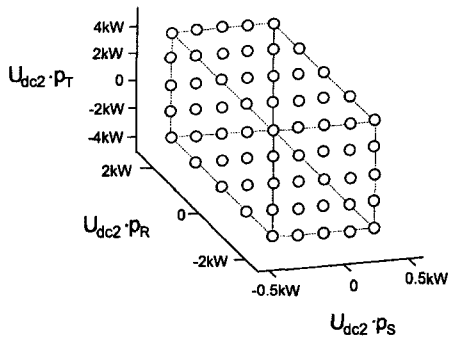

Figure 3.15: Power vector grid with visible 61 points viewed from the vector $\underline{n}_{power}$

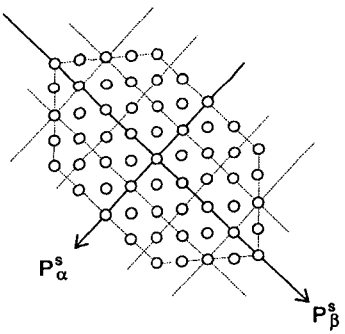

Figure 3.16: Power vector grid viewed from $\underline{n}_{power}$ with the axes (P^s_α, P^s_β)

The difference vector between the last selected power point and the next point is given by equation;

$$\Delta\underline{p} = (\Delta p_R, \Delta p_S, \Delta p_T) = (p_{Rnew} - p_{Rlast}, p_{Snew} - p_{Slast}, p_{Tnew} - p_{Tlast}) \quad (3.59)$$

It has to be remarked that the current is always changing, while the voltage steps are always constant. So each sampling period, the last power vector $\underline{p}_{last}$ has to be recalculated. From the last sampling period to the next one the current may have changed. The next Equation expresses the basic idea to switch the least possible power:

$$\Delta p_{c_{min}} = min(abs(\Delta p_R) + abs(\Delta p_S) + abs(\Delta p_T)) \quad (3.60)$$

As to be seen in the past chapter, the shortest distance from the last power vector $\underline{p}_{last}$ to the next possible vector point $\underline{p}_{new}$ has to be found. For the modulation method, the rotating vector will be the voltage vector $\underline{u}_{ref}$ and not a power reference vector. The first step in the algorithm consists of identifying the three new voltage vector points

$\underline{u}_1$, $\underline{u}_2$ and $\underline{u}_3$. Once the reference triangle is detected, the voltage vector is multiplied with the current in order to get the present power vector.

$$\underline{p}_n = \underline{i} \cdot \underline{u}_n \qquad \forall n = 1, 2, 3 \tag{3.61}$$

In this way the optimization is not only done with the switched voltage. The current in each phase is respected and the switched power is optimized. It is known that all the power vector points on the vector $\underline{n}_{power}$ will represent the same power vector point (P^s_α, P^s_β). But in the power grid, this vector is not the vector $\underline{n} = (1, 1, 1)$, because of the multiplication of the voltage with the current. The direction is:

$$\underline{n}_{power} = \underline{n} \cdot \underline{I} = (I_R, I_S, I_T) \tag{3.62}$$

So the lines defining all possible power points are given by the following equation set:

$$\underline{r}_1 = \underline{p}_1 + l_1 \underline{n}_{power} = \begin{bmatrix} x = p_{R1} + l_1 \cdot I_R \\ y = p_{S1} + l_1 \cdot I_S \\ z = p_{T1} + l_1 \cdot I_T \end{bmatrix} \tag{3.63}$$

The two other lines are:

$$\underline{r}_2 = \underline{p}_2 + l_2 \underline{n}_{power} \tag{3.64}$$

$$\underline{r}_3 = \underline{p}_3 + l_3 \underline{n}_{power} \tag{3.65}$$

The vector p_n represents the power vector point (p_{Rn}, p_{Sn}, p_{Tn}) with $n = 1, 2$ or 3 from the selected triangle. l_n represents a distance in the direction $\underline{n}_{power} = (I_R, I_S, I_T)$. The power vector point, which is the closest possible to $\underline{p}_{last}$ has to be found: The same principle is used as described in Section 3.4.3, page 77: A surface has to be defined which is crossing the last power vector point $\underline{p}_{last}$ and is orthogonal to $\underline{n}_{power} = (I_R, I_S, I_T)$. The Equation of the surface is given in (3.66):

$$0 = I_R \cdot x + I_S \cdot y + I_T \cdot z - p_{Rlast} - p_{Slast} - p_{Tlast} \tag{3.66}$$

By cutting the surface in Equation (3.66) with the three vectors in the Equations (3.63), (3.64) and (3.65), the three closest points from the last power vector $\underline{p}_{last}$ are found. As to be seen before, the line Equations (3.63), (3.64) and (3.65) are now introduced into the surface Equation (3.66). The parameters l_1, l_2 and l_3 found in this operation are reintroduced into Equation (3.63), (3.64) and (3.65). By calculating the values, the three optimal power vector points (p_R, p_S, p_T) are found. In many cases, the vector points found cannot be generated, because of the discrete number of steps. So the next possible vector point has to be found. In the vector switching optimization it was only necessary to round the given value to the next entire number.

In the power switching optimization, all the possible points on the vectors $\underline{r}_1$, $\underline{r}_2$ and $\underline{r}_3$ have to be checked in order to find the nearest point. They can either be calculated or can be taken from a look-up table. Fortunately, all the points are lying on the same line, so it is only necessary to check the distance from one coordinate (for instance the

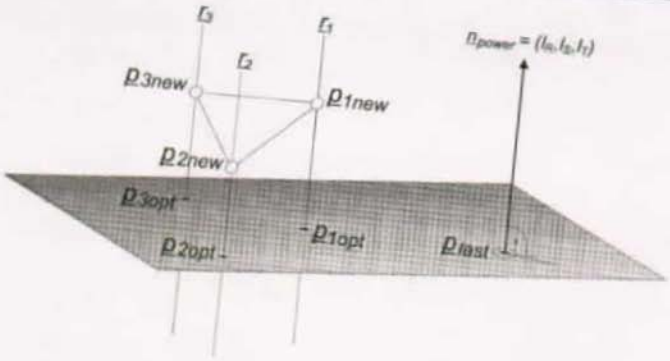

Figure 3.17: Calculating the optimal power vector points

x-coordinate). By using the next Equation, the parameter l_1 of the vector Equation (3.63) can be found.

$$l_1 = \min\left(\left|(p_{1R_{opt}} - p_{1R_{new\perp i}})\right|\right) \qquad \forall i \tag{3.67}$$

The same has to be done for the parameter l_2 and l_3 of the Equations (3.64) and (3.65). By introducing the values l_1, l_2 and l_3 with the values p_{1opt}, p_{2opt} and p_{3opt} into (3.63), (3.64) and (3.65), the new power points are found. They are certainly on the power grid, but also they will be as closest possible. Now the power values have to be calculated into the equivalent voltage vector values in order to proceed the modulation:

$$u_{new} = \begin{bmatrix} \frac{p_{R_{new}}}{I_N} \\ \frac{p_{S_{new}}}{I_S} \\ \frac{p_{T_{new}}}{I_T} \end{bmatrix} \tag{3.68}$$

The voltage u_{new} is not the vector point with the shortest distance u_{last}, but the fewest power will be switched by choosing this point as the next applied power point.

Resymmetrization of the switching and conduction losses

The two algorithms described before generate a voltage vector consisting of three vector positions (u_R, u_S, u_T). But the vector does not give any information, which of the four-quadrant converters will really generate the phase voltage. In the case of a multilevel converter with n=3 steps, the voltage vector $u_R = 2$ can be generated by three different switching patterns:

In fact there are even more possibilities to generate $u_R = 2$, but the cases, where one voltage cancels another are not considered. All partial voltages u_R, are either all positive or all negative, and never a combination of positive and negative voltages. The redundancy can be used to distribute the switching and conduction losses equally to each four-quadrant converter.

The algorithm visualized in Figure (3.18) looks at the sequence of the values of the phase voltage u_R. If there is a rising voltage, one of the three partial voltages is risen.

$U_{R_{(1)}}$	$U_{R_{(2)}}$	$U_{R_{(3)}}$	U_R
0	1	1	2
1	1	0	2
1	0	1	2

Table 3.3: The phase voltage composed of three four-quadrant converter voltages

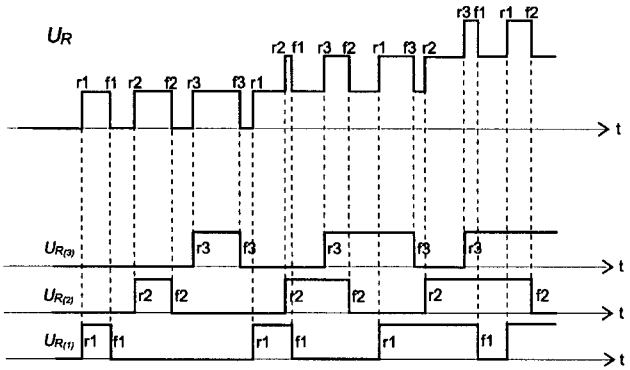

Figure 3.18: Separation of the phase voltage into the partial converter voltages u_{R_i}

The next time when u_R is risen, the next partial voltage is risen. The same algorithm is applied to the falling voltages of u_R. The algorithm is presented in the Appendix A.2. By applying this algorithm to all the three phase voltages, the losses in commutation and conduction are shared equally by each four-quadrant converter. The results of this optimization can be viewed in the next Figure (3.19):

On the left hand side of the Figure (3.19), the non-symmetrical distribution of the commutations can be seen. During most of the time of the period, the voltage $U_{R_{(1)}}$ remains positive and the current is flowing through the four-quadrant converter. The other voltage $U_{R_{(2)}}$ starts to switch when $U_{R_{(1)}} = 1$, and thus takes the important part of the switching losses. On the right side the voltage switching is symmetrically shared on the two multilevel steps with the help of the algorithm.

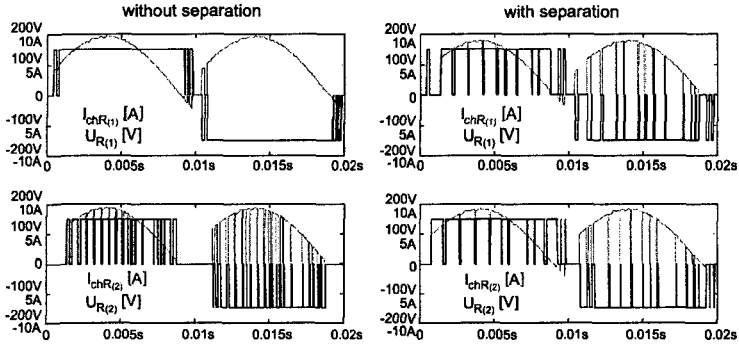

Figure 3.19: Simulation with separated and unseparated phase voltages u_R

	PWM	step	vector
k	1	1.2	1
U_{dc2}	150	150	150
f_s	1kHz	-	-
T_{sample}	$250\mu s$	$250\mu s$	$250\mu s$
-2	-2	-2	

Table 3.4: Simulation parameters for the comparison

3.5 Comparison of the three modulation methods

A three-phase multilevel converter consisting of $n = 2$ four-quadrant converters per phase was used to simulate different waveforms. All the parameters of the simulation results are given in the Table below:

The first set of simulations compares the phase voltages generated by the three different modulation methods, where already some interesting observations can be done:

The PWM phase voltage is can be recognized by the regular voltage impulses, becoming more and more wide. The step modulation consists of blocks with only few switching, while the vector modulation method shows irregular pulse lengths, reminding at hysteresis band modulated signal.

On the phase-neutral point voltage the multilevel effect can already be observed: The use of phase-shifted carrier signals in the case of the PWM modulation allows the generation of 15 different steps on the phase-neutral point voltage. By using the step modulation, some intermediate steps are missing: Only 11 different voltage steps are generated. If the motor is in the star configuration, this voltage generates the currents. The next image shows the phase-phase voltages of the multilevel converter.

The phase-phase voltage is responsible for the current generation, when the motor phases are in the triangle configuration. For all the three modulation methods, there are $4n + 1 = 9$ different voltage steps.

On the Figure (3.23) a very interesting effect can be observed: In the case of the PWM modulation and the step modulation, the neutral point voltage is defined by the

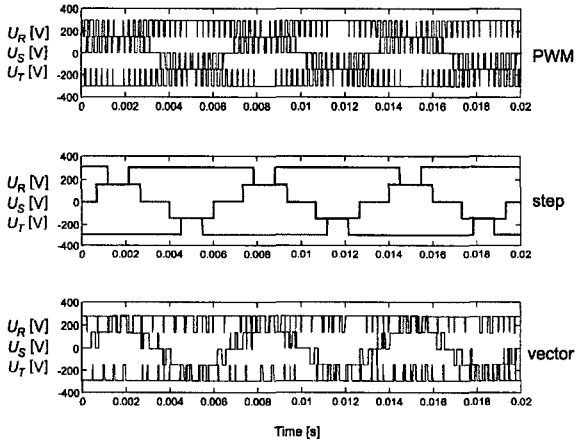

Figure 3.20: Simulation of the phase voltages with the three modulation methods

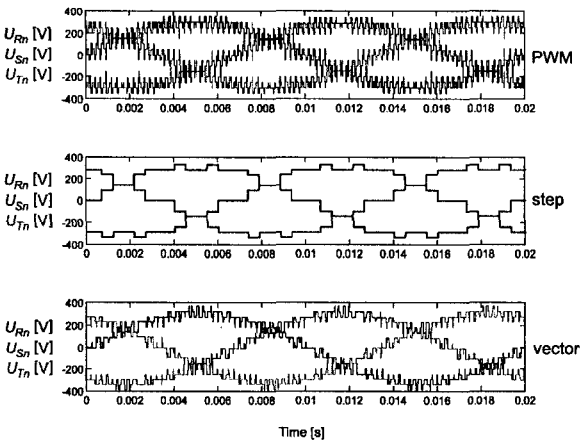

Figure 3.21: Simulation of the phase-neutral point voltages

three phase voltages, given by the well known Equation (3.18). So the neutral point voltage only uses three different voltage steps in both cases. This is different for the vector modulation: This modulation is done by using the complex phasors, so there is still a degree of liberty to choose the neutral point voltage. By executing the algorithm to minimize the switching losses, the neutral point voltage jumps over many possible positions (7 steps). But as to be seen on the projection in Figure (3.7), 13 positions are possible. In general it can be said that there are at all $6n + 1$ possible voltage values for

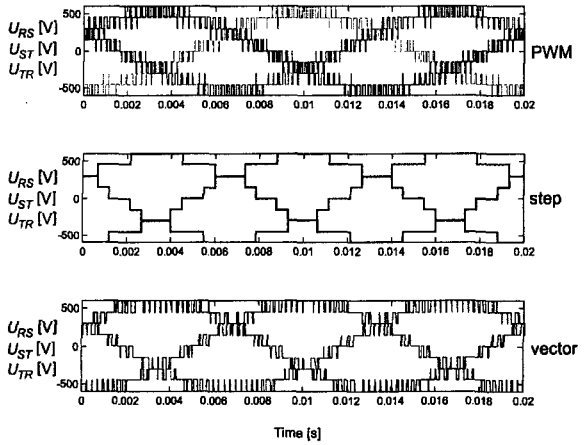

Figure 3.22: Simulation of the phase-phase voltage

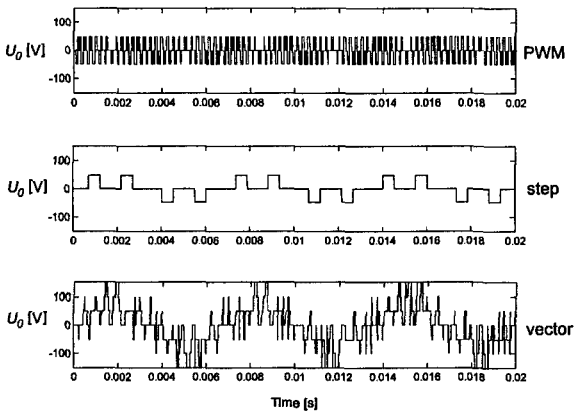

Figure 3.23: Simulation of the voltage from the neutral point to ground

U_o. The possible voltage steps are given in Equation (3.69):

$$U_o = j \cdot \frac{U_{dc2}}{3} \qquad j = [-3n, -3n+1, .., 3n-1, 3n] \tag{3.69}$$

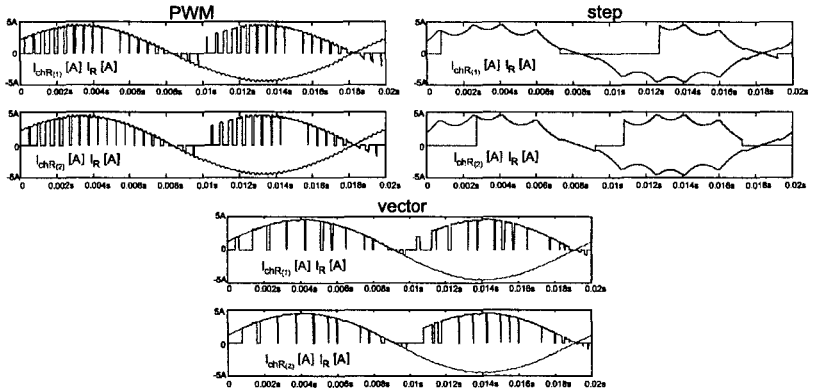

Figure 3.24: Comparison of the DC load currents

The simulation shown in Figure (3.24) show the DC currents on the DC side of the four-quadrant converters. This simulation gives an idea, what kind of DC source must feed the capacitors.

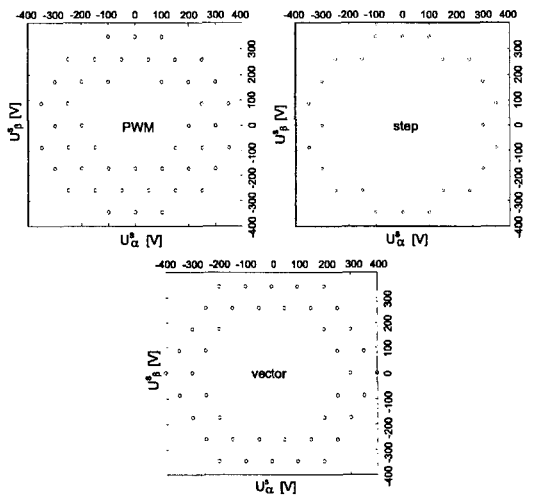

Figure 3.25: Simulation results of the voltage phasor points

The next Figure shows the three different voltage phasor patterns generated by the modulation methods. In the PWM modulation method it can be seen that on the outer hexagon, there are six voltage vector points missing. Even by using an over-modulation, these points cannot be reached. The vector points are also spread over three different

hexagons. The vector modulation uses all the possible outer vector points due to the vector-oriented modulation scheme. The points are only spread over 2 hexagons (these are the hexagons where the reference vector has passed through). The step modulation method of course does not select as much voltage vectors as the two other methods. The cornerpoints of the outer hexagon as well cannot be reached by the step modulation method. The next Figure gives a comparison of the harmonic content of the phase-phase voltages.

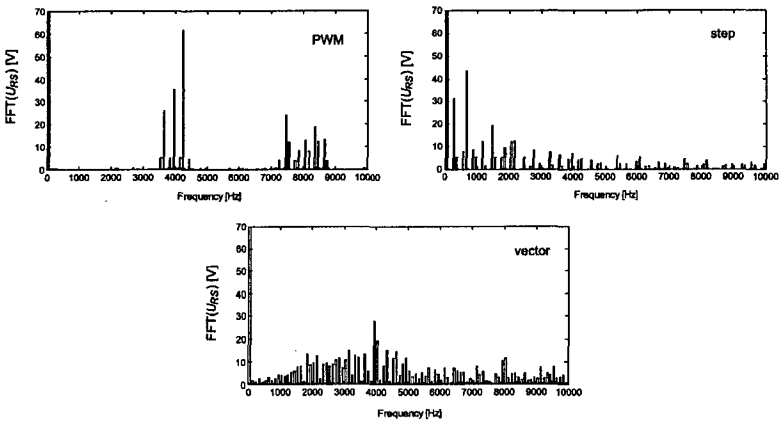

Figure 3.26: Comparison of the FFT of all the phase-phase voltages

The PWM modulation with the phase-shifted carrier signals show the typical repetition of the resulting harmonic of 2n times the basic switching frequency (Each half bridge has its own carrier signal). The harmonics are repeated at $4nf_s$, $6nf_s$ etc. The concentration of the switching harmonics on determined frequency bands makes the PWM ideal for applications, where a switching frequency filter is used to avoid the current ripple.
The step modulation contains especially low-order harmonics, due to the very few switching done per period. With such low-order harmonics normally a filter is used. The filter needs quite big elements (inductors, capacitors) and so will cost certainly more than a filter for the PWM modulation.
The vector modulation is the only modulation method where the harmonic contents are distributed over all the frequency range. The harmonics are stochastically distributed, so there is no dominant frequency. The highest harmonic peak is the sampling frequency of 4kHz, but the peak is not dominant. The vector modulation is an ideal modulation method, if there is no possibility to use a filter (weight constrains, volume, etc.). To give a better overview on the distortion of the voltage, a comparison table in function of the modulation degree is presented:

The Figure (3.27) shows the total harmonic distortion of the normalized phase voltage. It is interesting to see that by using different modulation degrees, the best modulation method in regard to THD changes. If the modulation degree is very low, the best values are found using the vector modulation. In the middle range, the PWM method is the best. For the step modulation a local minima can be observed, at the modulation degree

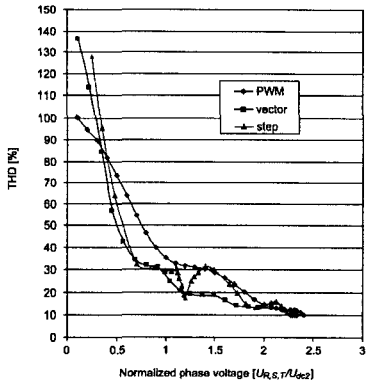

Figure 3.27: Representation of the THD value in function of the modulation degree

$k = 1.25$. This is just before the second step is activated.
The motor currents are also simulated. Particularly interesting is the representation of the current as a phasor.

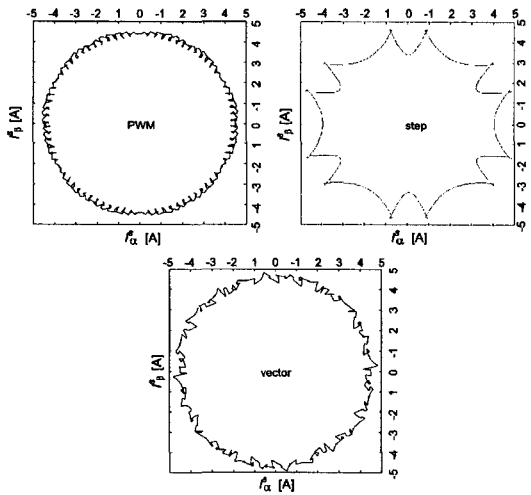

Figure 3.28: Simulation of the motor currents in the phasor plane

It can be easily seen that the current of the step modulation is of poor quality. This simulation is done while the multilevel converter is directly coupled to the motor, so there is no filter. The PWM current phasor shows a regular current oscillation, due to the fixed switching frequency. The vector modulation current has a non-deterministic

behavior. It is not possible to identify a switching frequency.

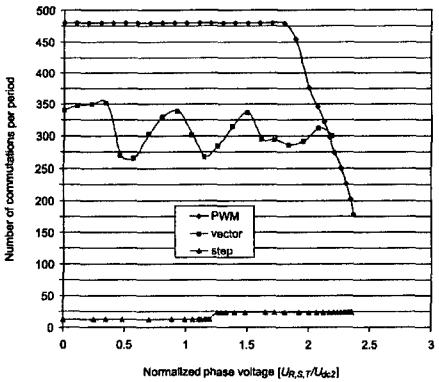

Figure 3.29: Comparison of the number of switching

The last simulation in Figure (3.29) concerns a comparison between the number of power semiconductor commutation per period. The PWM modulation method is compared with the optimized switching method of the vector modulation, using the minimized voltage switching, as been described in Section 3.4.3. The fundamental frequency of the motor is $f_{mod} = 50\text{Hz}$. The switching frequency of the PWM modulation (per half-bridge) is $f_s = 1\text{kHz}$, while the sampling period for the vector modulation is $T_{sample} = \frac{1}{4kHz}$. This gives a comparable voltage and current quality. It can be seen that the optimized vector modulation performs less switching events over nearly the whole range of the defined modulation degree. The PWM scheme performs always the same numbers of switching events per period, only when it is in over-modulation, there is less switching. Of course the step modulation does only very few switching.

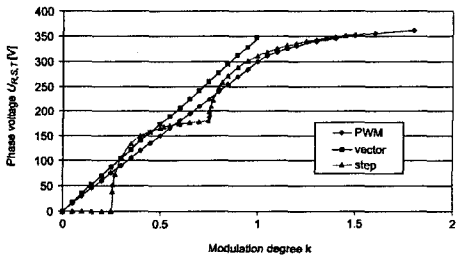

Figure 3.30: Comparison of the linearity between modulation degree and phase voltage

The computed graphs in Figure (3.30) show the amplitude of the phase-phase voltages of the multilevel converter in dependence of the modulation degree k, of course without any compensation of the non-linearity (step modulation). It can be seen that only the

vector modulation method is linear over the entire defined modulation degree. The PWM method is non-linear, if no over-modulation strategy is used. By using an adequate over-modulation strategy, also the PWM modulation becomes linear over the whole range of the modulation degree.

3.6 Experimental results on a 10kW prototype

For the test and verification of all the modulation circuits described in the chapter above, a reduced power prototype has been realized in the laboratory. The multilevel converter consists of $n = 2$ four-quadrant converters per phase. The schematics of the converter is given in Figure (3.2). The same type with $n = 4$ has been shown already in Section 2.6 for a single phase application. The parameters for the experimental results are given in the Table (3.5):

Parameter	Symbol	Value
DC power supply	U_{dc2}	150V
Sampling time	T_{sample}	$250\mu s$
Switching frequency PWM	f_s	1kHz
Power IGBT	$U_{ce_{max}}, I_{c_{max}}$	1200V,50A
Max. DC current	$I_{dc1_{max}}$	10A
DC capacitor	C_{dc2}	$9 \cdot 220\mu F$
Induction motor PWM and step	Frequency	$120Hz/3600rpm$
Lenze DFVARS080	nominal current	$9.1A$
	nominal voltage	$390V$ star
	power factor	$cos\varphi = 0.8$
Induction motor vector	Frequency	50Hz / 1500rpm
ABB QU100L4 AT	nominal current	4.9A
	nominal voltage	$390V$ star
	power factor	$cos\varphi = 0.84$

Table 3.5: Motors used for the experimental results

The four-quadrant converter consists of two half-bridge IGBT modules from FUJI used together with the appropriate FUJI IGBT drivers. The feeding is done by a simple single-phased rectifier. On the 50Hz AC side between the rectifier and the secondary transformer coils, there is a triac circuit. The triacs firing angle is variable in order to variate the DC feeding voltage. With the variation of this angle DC voltages between 50V and 200V can be generated. On the DC side of the rectifier there is a chopper circuit. The chopper consists of a power MOSFET with an power resistor of 20Ω in series-connection. This circuit allows the dissipation of energy, if the motor is braking or running as a generator. The control algorithms have been implemented on a PC using C code on the DOS operating system level. The modulator (carrier triangular signals and timing) have been generated by a gate array logic card connected to the PC. For the measurements a 12 bit AD-converter has been used. Normal vector control algorithms are executed in the sampling time of about $250\mu s$ with all the measurements and the modulator output.

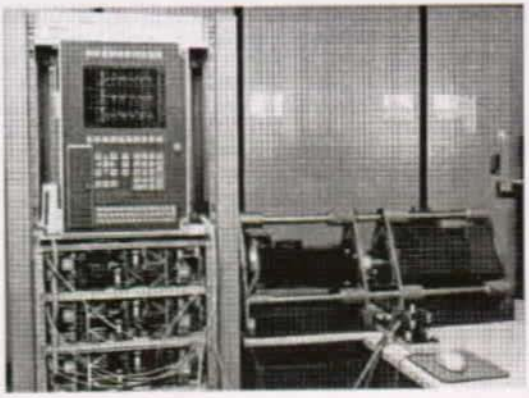

Figure 3.31: The realized three-phase multilevel converter

The PC was furthermore equipped by a resolver to digital converter for a high-precision measurement of the motor speed. This setup allowed the test of different modulation schemes and a vector control for the induction motor speed. The next Figure (3.32) shows a overview of the schematics of the supply circuit:

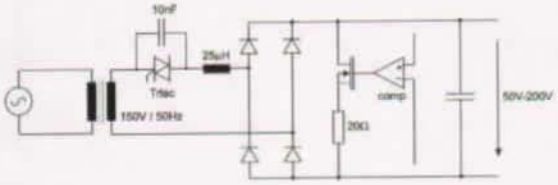

Figure 3.32: Power supply of the 4Q-converters for the experiments

The first Figure (3.33) of the experimental results shows the induction motor driven by the multilevel converter. A motor with a relatively low main inductance has been chosen in order to use the advantage of the multilevel converter. The frequency of the triangular carrier signal for the modulation is chosen at 1kHz (switching frequency of the half-bridge). So the resulting frequency seen on voltages and current is 4kHz. It can be seen that the phase voltage consists of 5 different voltage levels, while the phase-phase voltage is composed from 9 voltage levels.

The current phasors have been measured and compared (Figure (3.34)). The inner line shows the current obtained with a classical converter using 6 IGBT switches. In this way the enhancement of the current quality is shown. The resulting switching frequency is multiplied by the factor 4.

The same measurements were done on exactly the same configuration using the step modulation. The Figure (3.35) shows the graphs with the step modulation. The step modulation has also been tested on the same motor as the PWM modulation.

The step modulation is the most efficient modulation method concerning the losses. But the method lacks of current quality. The driven motor was directly coupled and there was no current filter. It is interesting to see the voltage-waveform of the neutral-point voltage. The fundamental frequency is 120Hz. The Figure (3.36) shows the multilevel converter current once again compared to the classical converter. While the ML-current is still tolerable for a filterless drive system, the current of the classical converter must definitely be filtered.

The same multilevel converter has been used to implement the vector modulation. Instead of using the low-inductance motor rotating 3600rpm a different induction motor has been used, rotating at 1500rpm (50Hz). This has been done in order to have more sampling events during a period. All the algorithms have been implemented on the same PC. If the generated voltage has the frequency of 120Hz and the sampling time is $250\mu s$, there are only 32 sampling events per period. If the reference vector turns between the two outer hexagons of the complex phasor plane, it passed by 42 triangles. So if the

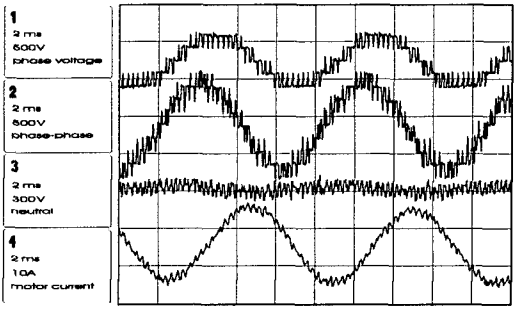

Figure 3.33: Measurements of the PWM modulation driving an induction motor

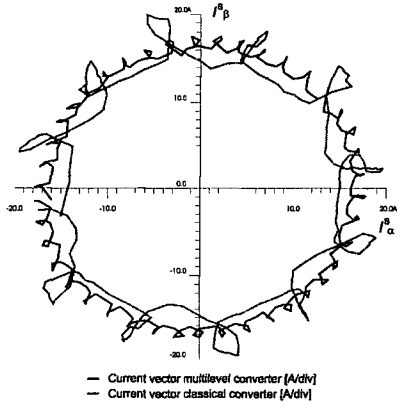

Figure 3.34: PWM motor currents in the phasor plane

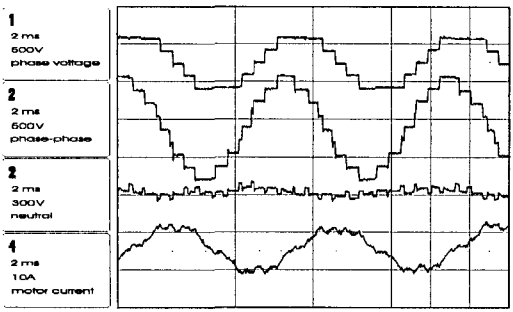

Figure 3.35: Measurements of the step modulation

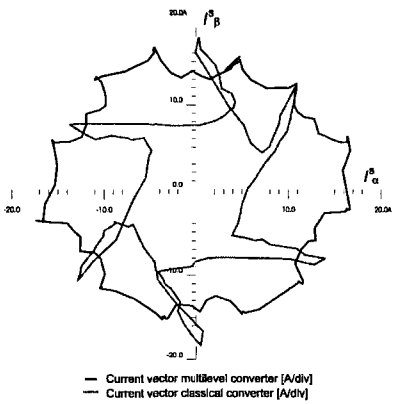

Figure 3.36: Step modulation motor currents in the phasor plane

reference vector is rotating at full modulation degree (passing in region of the outer hexagons), it will jump over some of the triangles. To avoid this, there should be at least the same number of sampling events as triangles in the outer region.
To achieve this, either the sampling time must be smaller (faster processor, faster AD-conversion), or the motor speed must be reduced. Due to the fact that the algorithms are quite complex, it is not very easy to increase significantly the sampling frequency. This is why the a motor for 50Hz feeding has been chosen. The Figure (3.38) shows phase and phase-phase voltage. Once again the non-deterministic switching frequency can be observed.

A very interesting effect can be observed when the modulation degree is reduced: The phase voltage is not a sinusoidal value, while the current-generating phase-phase voltage is sinusoidal. This fact is a result of the active optimization of the switching losses: If the modulation degree is not $k = 1$, there are always several ways to generate a phase-phase voltage. The voltage switching has been implemented in the experimental setup and is

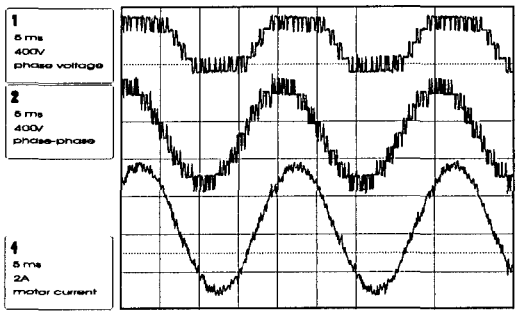

Figure 3.37: Measurements of the vector modulation, full modulation degree

tested on the induction motor. If the modulation degree is high, it is not possible to use the redundant switching patterns (the reference vector is moving on the outer hexagon). The next Figure (3.38) shows the optimized switching. A modulation degree of $k = 0.6$ has been used.

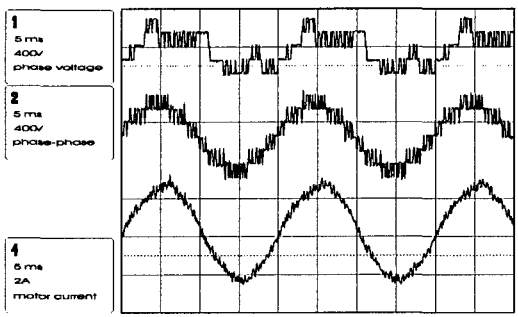

Figure 3.38: Measurements of the vector modulation, reduced modulation degree

Together with the vector modulation, a vector control has been implemented. The control of flux and speed is done by using two PI controllers. The speed is directly measured from the motor by the resolver to digital measurement card and is afterwards compared with the sign value of speed. The flux cannot be measured from the used motor. An observer for the flux is used, estimating the value of the flux. The output of those two PI-controllers are giving the sign values for the two currents I_α and I_β, responsible to generate the motor flux and torque. The current controllers are also realized with two PI-controllers. For the comparison with the real current values of the motor, two of the motor currents are measured and are transformed by the Equations for the coordinate transformation found in [27] to the two phasor currents I_α and I_β. So the rotating coordinate system is referenced to the rotor flux. The output of these two controllers are giving the sign values of the stator voltages. The values are re-transformed into the

fixed coordinate system. The resulting two voltage components are the two coordinate components of the reference vector $\underline{u}_{ref}$. So this reference vector can directly be used for the vector modulator. The reference vector is the idealized voltage applied to the motor, generated by the multilevel converter.

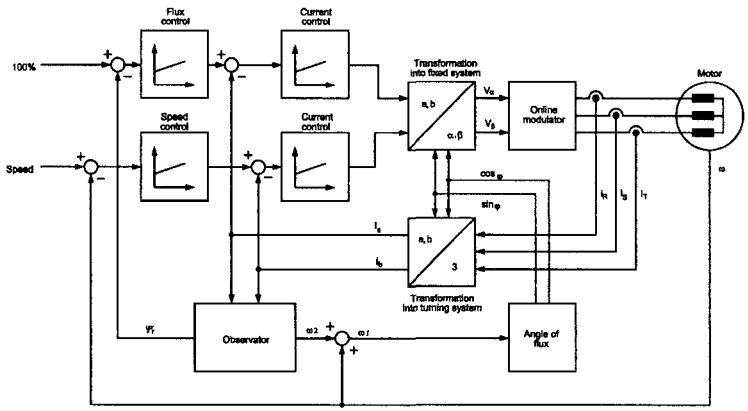

Figure 3.39: Schematics of the implemented speed controller

The model of the induction motor is a conventional model taken from [28] and first was used on a simulation model. After some tests the vector control has been implemented on the PC in a real-time environment. Figure (3.40) shows a test done with the induction motor. The motor starts up and accelerates up to 1200rpm. Afterwards the set value for the speed is changed to 600rpm, which forces the multilevel converter to go into a generative mode to slow down the motor. The torque-generating current I_β becomes negative to slow down the motor immediately. A DC current motor has been used as load for the motor.

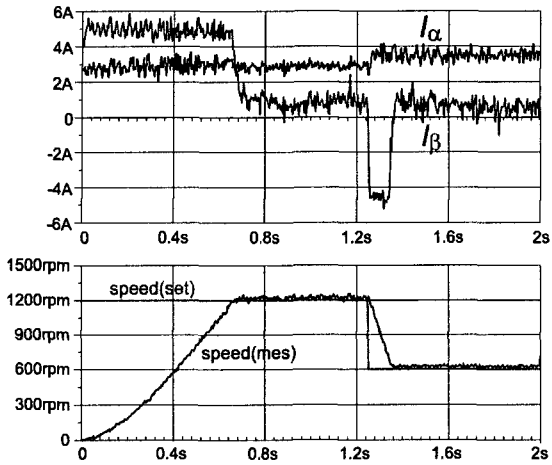

Figure 3.40: Performance test of the vector control with vector modulator

Conclusions

The results achieved with the realized prototype are showing that there is a important potential for the three-phase multilevel converter in several application fields. The high quality voltage vector definition combined with a special vector modulation principle with optimized switching can be especially used for high-power industrial drives. Passive components like switching frequency filters can be reduced in weight and size and thus allow to implement powerful vector control algorithms for speed and torque. All the developed modulation methods have been tested by simulation and have also been implemented on a reduced power prototype. The publication [7] done on this work was awarded by the IEEE Power Electronics Society (PELS) as the best publication on power electronics in the year 1999 (PELS transactions prize paper awards).

Chapter 4

Voltage controlled DC-DC converter

4.1 Introduction

The proposed multilevel converter topology requires individual DC-DC converters for the feeding of each four-quadrant converter. The primary function is to provide a galvanic insulation of each supply voltage, to be seen in [5] and [23]. One supply voltage feeds an individual AC-DC converter of the multilevel converter chain. Therefore the DC-DC converter also has to be foreseen for a bi-directional energy exchange. The feeding by the proposed DC-DC converter also allows a high reduction of the system weight. Instead of providing the galvanic separation by low-frequency transformers, the galvanic insulation is done by using a medium-frequency transformer, working in the frequency range between 5 and 20kHz. The medium-frequency converters are much lighter than low-frequency transformers for the same power.
An other important point is the controllability of the DC-DC converter: Due to the pulsing current and also the perturbations on the AC voltage line, a voltage control has to be implemented to achieve an efficient separation of the AC line from the DC link. The Figure (4.1) shows a schematic of a DC-DC converter, containing all different parts:

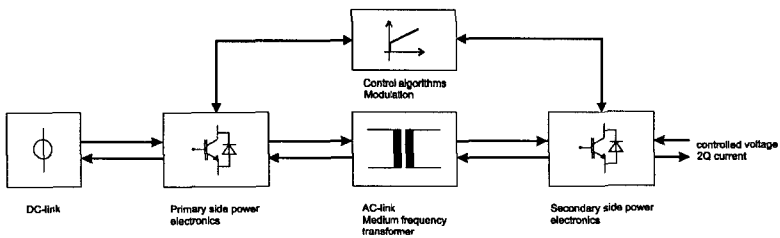

Figure 4.1: The full-bridge DC-DC converter

This report will propose two possible implementations of a DC-DC converter controlling the secondary side voltage. In this case, all perturbations on the primary side (DC link) will not be transferred to the secondary side (individual four-quadrant converters, usually realized as a full-bridge converter). This requires voltage measuring and a control algorithm that can be implemented on a microprocessor. The DC-DC converter will be

used in a two-quadrant operation with a positive output voltage and a bi-directional current. On the other hand, trap circuits for filtering can be avoided on the secondary side, then it will be entirely decoupled from all low frequency voltage ripples on the primary.

4.2 Controlled two quadrant DC-DC converter

The proposed DC-DC converter consists of two full-bridge converters. An intermediary circuit is found between the two AC sides of the full-bridges, composed by a medium frequency transformer, an inductance and two capacitors in series. This intermediary circuit is called the AC link. The Figure (4.2) shows the schematics of the DC-DC converter used. The full-bridges can apply a positive, negative or zero voltage to the intermediary circuit on both sides of the medium-frequency AC link.

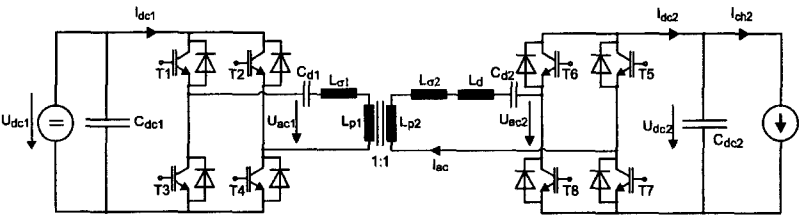

Figure 4.2: The full-bridge DC-DC converter

The main difference between the conventional DC-DC converters can be found in the series-connected inductance L_d in the AC link:

- In conventional DC-DC converters, the series-inductance in the AC-link has to be as small as possible. The AC voltages U_{ac1} and U_{ac2} have to be in phase and the inductance is needed to create a resonant current [15] and [20]. The series capacitor is adapted to achieve a resonant frequency close to the switching frequency. Some examples are shown in Section 2.3.1, page 16 . There is no additional inductance and even the natural stray inductance of the AC link must be reduced to a maximum (around $1\mu H$). This DC-DC converter types do not allow a voltage-controlled operation.

- The proposed DC-DC converter needs a relatively large series inductor. The inductor is needed to be able to create a voltage difference from the primary AC voltage U_{ac1} to the secondary AC voltage U_{ac2}. This allows a determined current generation, which allows the control of the output voltage. The proposed DC-DC converter needs a very high voltage insulation. High-voltage insulation transformers usually have high stray inductances, so naturally already a high stray inductance is present.

The proposed DC-DC converter has an additional inductor L_d and two capacitors C_{d1}, C_{d2} on both sides of the transformer. These elements are in series in the AC link. The resonant frequency of this LC-circuit is much smaller than the switching frequency. This AC link of the proposed DC-DC converter is shown in the Figure (4.3) below:

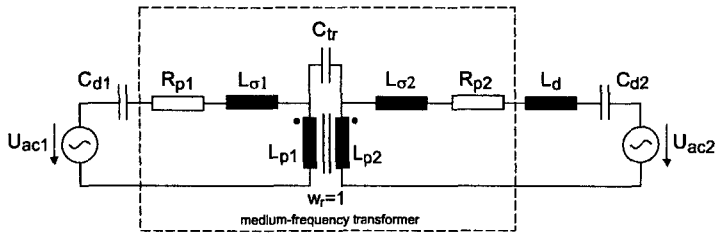

Figure 4.3: AC link with all elements of the DC-DC converter

Primary and secondary winding resistance	R_{p1}, R_{p2}
Primary and secondary stray inductance	$L_{\sigma 1}$, $L_{\sigma 2}$
Principle inductance	$L_p = L_{p1} = L_{p2}$
Coupling capacitor primary-secondary side	C_{tr}
Winding ratio	w_r

Table 4.1: Medium frequency transformer parameters

The medium frequency transformer used in this AC link consists of the elements shown in Table (4.1), which can be measured or calculated from the transformer design. More details concerning the medium-frequency transformer can be found in Section 4.3 at page 151.

The other three elements, namely the current DC component capacitors C_{d1}, C_{d2} and the decoupling inductance L_d are additional elements of the AC-link. The capacitors are chosen relatively large in order to compensate any DC current created by the two 4Q-converters. The capacitors of the series connection can be seen as single capacitor:

$$C_d = \frac{C_{d1} C_{d2}}{C_{d1} + C_{d2}} \tag{4.1}$$

The impedance of the capacitor $Z = \frac{1}{\omega_p C_d}$ is very small and so this effect can be neglected. Also the resistances of the transformer winding are very small (around $100m\Omega$). After this simplification, the new equivalent scheme is presented in Figure (4.4):

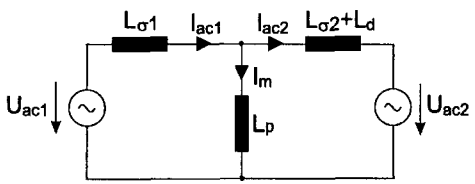

Figure 4.4: The full-bridge DC-DC converter

In this simplified equivalent scheme of the AC-link, only the inductive elements are remaining. The transformer winding ratio used for the medium-frequency transformer is

always $w_r = 1$. So the two main inductances can be put together $L_p = L_{p1} = L_{p2}$ to simplify the equivalent scheme. In this transformer design, the main transformer inductance is much larger than the sum of all series-connected inductors, shown in Equation (4.2):

$$L_p \gg L_{\sigma 1} + L_{\sigma 2} + L_d \tag{4.2}$$

Usually the medium-frequency transformer has a principle inductance of about $1 - 5mH$, while the sum of the stray inductances with the additional inductance L_d is smaller than $100\mu H$.

$$L_{\sigma tot} = L_{\sigma 1} + L_{\sigma 2} + L_d \tag{4.3}$$

The decoupling inductance is often split in two equal parts to be placed on both sides of the transformer. So it can be found:

$$L_{d1} = L_{d2} = \frac{L_d}{2} \tag{4.4}$$

After this last simplification, the equivalent scheme is reduced to a decoupling inductor $L_{\sigma tot}$ between two AC voltages U_{ac1} and U_{ac2}. This equivalent scheme is shown in (4.5).

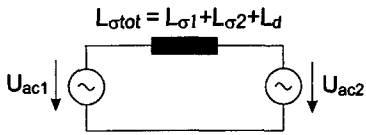

Figure 4.5: The full-bridge DC-DC converter

By considering the schematic (4.5) as the AC link, the working principle of the DC-DC converter can be easily explained: If the two voltages U_{ac1} and U_{ac2} are exactly the same waveform, there is no current in the AC link and thus no power transfer. As soon as the two voltages are different, for instance by giving a phase-shift between the two voltages U_{ac1} and U_{ac2}, an AC link current I_{ac} is generated. The current I_{ac} is of course a pure AC current due to the big capacitors C_{d1} and C_{d2}. But the switching of the 4Q-converters will transform this AC current on both DC sides of the converter to a DC current, namely on the secondary DC side to the current $I_{dc2}(t)$. The AC current I_{ac} and of course the DC current on the secondary side I_{dc2} can be defined by the difference voltage between the two voltages U_{ac1} and U_{ac2}, which is lying across the decoupling inductance $L_{\sigma tot}$.
In particular, it can be said that the stray inductances of the intermediary circuit do not cause any problems. It is even advantageous to have a high stray inductance, so that the external inductance L_d can be taken smaller. More details on the transformer design can be found in Section 4.3. Figure (4.6) shows the possible variations of the voltages U_{ac1} and U_{ac2}. Each 4Q-converter on both sides of the AC link is able to generate a positive, a negative and the zero-voltage. By respecting a fixed switching frequency of the DC-DC converter f_p, the parameters of the modulation to variate U_{ac1} and U_{ac2} are defined in Table (4.2).

Phase shift between U_{ac1} and U_{ac2}	δ
Zero-voltage width U_{ac1}	Ω_{d1}
Zero-voltage width U_{ac2}	Ω_{d2}

Table 4.2: Modulation parameters for the DC-DC converter

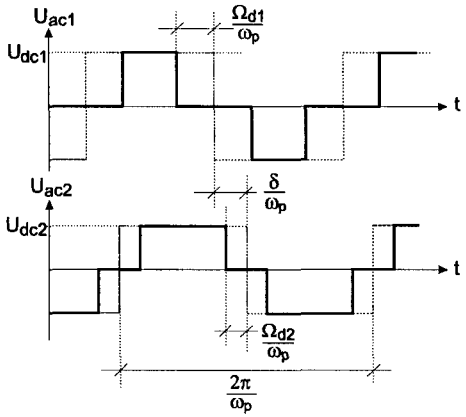

Figure 4.6: The voltage waveforms U_{ac1}, U_{ac2} depending on the modulation parameters δ, Ω_{d1} and Ω_{d2}

The final aim is to control the output voltage of the DC-DC converter, namely U_{dc2}. If the equivalent scheme of the DC-DC converter in Figure (4.2) is looked at, it can be seen that the voltage U_{dc2} is changed by the difference between the two currents $\overline{I}_{dc2}$ and I_{ch2}. The output voltage U_{dc2} is controlled by a DC-DC converter modulator generating a current I_{dc2} entering the output capacitor C_{dc2}, which must be equal to the load current I_{ch2}. The current going into the output capacitor will be zero and so the voltage U_{dc2} is stabilized. The current $\overline{I}_{dc2}$ is the DC component of the current I_{dc2} and can be determined by the two DC voltages U_{dc1} and U_{dc2} and all the three modulation parameters. Figure (4.7) shows the schematic of this function.

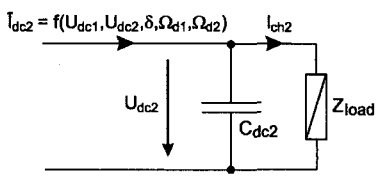

Figure 4.7: Stabilization principle of the output voltage U_{dc2}

The most important Equation is the transfer function of the DC-DC converter: In

particular the current I_{dc2} charging the capacitor C_{dc2} in function of the parameters U_{dc1}, U_{dc2} has to be determined, as shown in the Figure (4.7). Also the influence of all the passive components, especially the resulting decoupling inductance $L_{\sigma tot}$, are interesting to know. The mathematical evaluations for these equations can be found in Appendix A.3. The final expression for the power transfer on the secondary side is:

$$P_{dc2} = \overline{I}_{dc2} \cdot U_{dc2} = \frac{4U_{dc1}U_{dc2}sin(\delta)cos(\Omega_{d1})cos(\Omega_{d2})}{\pi^3 f_p L_{\sigma tot}} \tag{4.5}$$

The current $\overline{I}_{dc2}$ is the DC part of the DC-DC converter current I_{dc2}. Equation (4.6) gives the reactive power for the primary and secondary side.

$$Q_{ac1} = \frac{4[{U_{dc1}}^2 cos^2(\Omega_{d1}) - U_{dc1}U_{dc2}cos(\delta)cos(\Omega_{d1})cos(\Omega_{d2})]}{\pi^3 f_p L_{\sigma tot}} \tag{4.6}$$

$$Q_{ac2} = -Q_{ac1} \tag{4.7}$$

The ideal case is, when the reactive power is always equal to zero. This is only possible if the decoupling inductance is close to zero. The ratio reactive power to the active power gives an idea on the losses of the whole DC-DC converter. The more reactive power there is, the less efficiency has the converter.

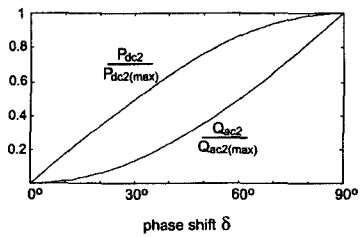

Figure 4.8: Reactive power and active power in function of δ

The Figure (4.8) shows the reactive and active power as a function of the phase-shift δ, when Ω_{d1} and Ω_{d2} are equal to zero. It is better not to operate the DC-DC converter with high phase-shift values due to the high reactive part of the power. The parameters limiting the power flow are the switching frequency and the decoupling inductance. For higher switching frequencies smaller inductance have to be taken for the same power transfer. The parameters Ω_{d1} and Ω_{d2} are defined as follows:

$$0 \leq \Omega_{d1}, \Omega_{d2} \leq \frac{\pi}{2} \tag{4.8}$$

Maximal power flow is reached with Ω_{d1} and $\Omega_{d2} = 0$. These parameters have no influence on the sign of the power flow, but they can vary the reactive power.

4.2.1 Modulation and control with the rectangular mode

The first method described is already shown in [16] and [37]. It describes a classical method to implement a voltage controlled DC-DC converter. For the multilevel feeding, all design parameters and a voltage controller system have been developed using the rectangular modulation method. The method is easy to implement and shows excellent control performance, but the overall efficiency is not sufficient.
The modulation of the rectangular mode can be described as follows: The power semiconductors of the primary side full-bridge (T1-T4) are commutated to generate a rectangular voltage U_{ac1}, always with a duty cycle of 50%. The full-bridge on the secondary side (T5-T8) is also switched to generate a rectangular voltage U_{ac2}, but with the possibility to have a phase shift δ between U_{ac1} and U_{ac2}. The phase shift δ is generated by changing the duty cycle of the secondary full-bridge at one period and is responsible for the power transfer: By causing a differential voltage ΔU on the inductor of the intermediary circuit, a AC current I_{ac} is generated.

Advantages:
- Highest power transfer possible with the given converter
- Symmetrical share of the losses on all switches
- Usable if the input voltages are not very different (20% variation)
- Power transfer is possible also if one of the voltages is zero
- Current I_{dc2} does not depend on the output voltage U_{dc2}

Disadvantages:
- 8 commutations of IGBTs have to be performed
- Negative current on the DC-side reduces the power transfer, in this way the efficiency is reduced
- High losses caused by reactive power when the input voltages are different and no power is transferred ($\delta = 0$, $U_{dc1} \neq U_{dc2}$)

The Figure (4.9) represents the voltage waveforms on the intermediary circuit. The IGBTs T1 and T2 are turned-on with the positive half-wave of U_{ac1}, the IGBTs T3 and T4 are consequently turned-on for the generation of the negative half-wave.

Mathematical description of the rectangular mode

Rectangular mode by monophasor representation

In order to find a mathematical description of the rectangular modulation method, the phasor representation of the electrical values in the complex plane (Re, Im) are taken. Of course only the fundamental sine wave of the values are considered. By definition of the rectangular mode, two of the modulation parameters are always equal to zero.

$$\Omega_{d1}, \Omega_{d2} = 0 \tag{4.9}$$

In spite of the desactivation of the parameters Ω_{d1} and Ω_{d2}, the parameter δ can control actively the power flow. It is limited by definition to the following interval:

$$\delta_{Pmin,rec} = 0 \tag{4.10}$$

$$\delta_{Pmax,rec} = \pm\frac{\pi}{2} \tag{4.11}$$

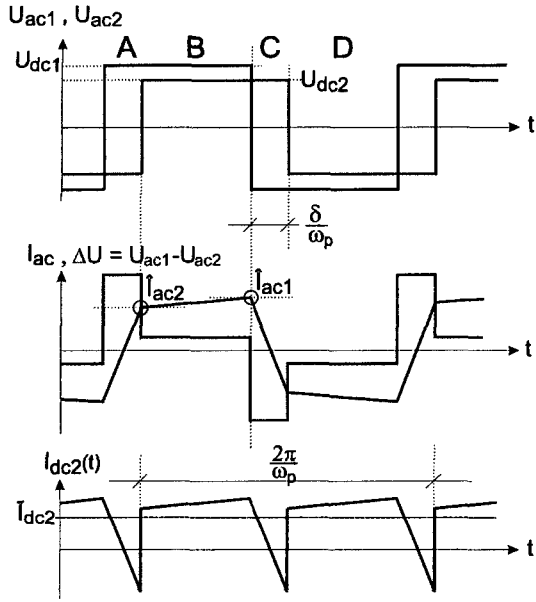

Figure 4.9: Voltage and current waveforms for the rectangular mode

If δ is put to zero, there is no power flow. A negative δ changes the sign of the power flow, which means that the power is transferred from the secondary side P_{dc2} to the primary side P_{dc1}. The transferred power is given with the Equation (4.12).

$$P_{dc2} = \overline{I}_{dc2} \cdot U_{dc2} = \frac{4U_{dc1}U_{dc2}sin(\delta)}{\pi^3 f_p L_{\sigma tot}} \tag{4.12}$$

The peak current is the amplitude of $\underline{I}_s$ and was already calculated in the appendix Equation (A.21). Equation (4.13) shows the AC current. The parameters Ω_{d1} and Ω_{d2} are set to zero.

$$\widehat{I}_s = \frac{2\sqrt{{U_{dc1}}^2 + {U_{dc2}}^2 - 2U_{dc1}U_{dc2}cos(\delta)}}{\pi^2 f_p L_{\sigma tot}} \tag{4.13}$$

The current from the load can be calculated also, if the electrical values U_{dc1} and U_{dc2} are measured. Of course the parameters f_p and $L_{\sigma tot}$ have to be known. The load current I_{ch2} must have the same value as the average value converter output current $\overline{I}_{dc2}$. So it can be found:

$$I_{ch2} = \frac{4U_{dc1}sin(\delta)}{\pi^3 f_p L_{\sigma tot}} \tag{4.14}$$

The prediction of δ used for the controller is given by the next Equation (4.15). The electrical values U_{dc1}, U_{dc2} and the load current I_{ch2} are measured. A phase shift δ is predicted allowing the generation of a current $\overline{I}_{dc2}$ equal to I_{ch2}.

$$\delta = arcsin\left(\frac{I_{ch2}\pi^3 f_p L_{\sigma tot}}{4U_{dc1}}\right) \tag{4.15}$$

The condition, when it is not possible to generate $\overline{I}_{dc2}$ equal to I_{ch2} is given by Equation (4.16):

$$I_{ch2} \leq \frac{4U_{dc1}}{\pi^3 f_p L_{\sigma tot}} \tag{4.16}$$

It is very interesting to see that the current $\overline{I}_{dc2}$ (in Equation (4.14)) and of course also the prediction of δ (in Equation (4.15)) is not depending on the output voltage U_{dc2}.

Rectangular mode based on the time axis

Another way to describe the transfer function of the DC-DC converter is by analyzing the current given in the time-axis. The currents are linear. By generating an average value over a switching period it can be found:

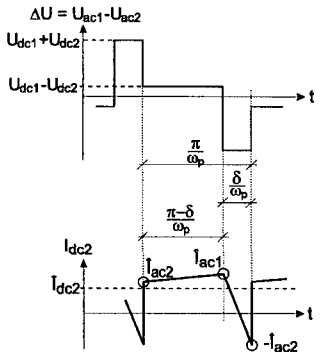

Figure 4.10: AC link current and voltage drop ΔU

$$\overline{I}_{dc2} = \frac{1}{\pi}\left[\int_0^{\pi-\delta} \frac{\hat{I}_{ac1} - \hat{I}_{ac2}}{\pi - \delta}t + \hat{I}_{ac2}dt + \int_0^{\delta} \frac{-\hat{I}_{ac1} - \hat{I}_{ac2}}{\delta}t + \hat{I}_{ac1}dt\right] \tag{4.17}$$

The two peak currents $\hat{I}_{ac1}$ and $\hat{I}_{ac2}$ are also the turn-off currents in this modulation method. The expression for the primary side current turn-off value is:

$$\hat{I}_{ac1} = \frac{U_{dc1}\pi + U_{dc2}(2|\delta| - \pi)}{4\pi f_p L_{\sigma tot}} \tag{4.18}$$

and for the secondary side:

$$\hat{I}_{ac2} = \frac{U_{dc1}(2|\delta| - \pi) + U_{dc2}\pi}{4\pi f_p L_{\sigma tot}} \tag{4.19}$$

By solving Equation (4.20) and replacing the turn-off currents with the Equations (4.18) and (4.19), the transfer function of the DC-DC converter can be found:

$$\overline{I}_{dc2} = sgn(\delta)\frac{U_{dc1}|\delta|(\pi - |\delta|)}{2\pi^2 f_p L_{\sigma tot}} \tag{4.20}$$

The power transferred by the DC-DC converter in the rectangular modulation method is:

$$P_{dc2} = U_{dc2} \cdot \overline{I}_{dc2} = sgn(\delta)\frac{U_{dc1}U_{dc2}|\delta|(\pi - |\delta|)}{2\pi^2 f_p L_{\sigma tot}} \tag{4.21}$$

The maximal power of the DC-DC converter in the rectangular mode is found when the phase-shift is $\delta = \frac{\pi}{2}$. This can be proven by deriving the Equation (4.19) and setting the resulting equation to zero.

$$\delta = sgn(I_{ch2})\frac{\pi}{2}\frac{U_{dc1} - \sqrt{U_{dc1}^2 - 8U_{dc1}L_{\sigma tot}f_p|I_{ch2}|}}{U_{dc1}} \tag{4.22}$$

The maximal tolerated load current I_{ch2} is equal to the maximal DC-DC converter current:

$$I_{ch2} \leq \frac{U_{dc1}}{8L_\sigma f_p} \tag{4.23}$$

Once again, it is interesting to see that the Equations (4.20) and (4.22) do not depend on the output voltage U_{dc2}. This means that even if the output voltage is zero, a current $\overline{I}_{dc2}$ can be generated to load the capacitor C_{dc2}.

Computing of the converter components

The components of the DC-DC converter given in Figure (4.2) have to be computed in a way to respect the power transfer capabilities. All the Equations are computed with the mathematical descriptions based on the time axis seen on page 107, because they represent the DC-DC converter behavior more precisely. The most important component is the decoupling inductance L_d. The maximal possible power depends on the inductance. Based on Equation (4.21) it can be found:

$$L_d = \frac{U_{dc1}\delta_{max}(\pi - \delta_{max})}{2\pi^2 f_p \hat{I}_{ch2}} - L_{\sigma 1} - L_{\sigma 2} \tag{4.24}$$

The maximal value for δ is $\frac{\pi}{2}$. But it is better to take a value for δ_{max} smaller than $\frac{\pi}{2}$, about $\frac{\pi}{3}$. This allows the DC-DC converter to create less reactive power (and thus is more efficient), the decoupling inductance can be chosen smaller and the transfer function of

the converter is nearly linear. The linearity is an advantage for the control system. The inductance L_d can be split in two equivalent parts and be put on both sides of the AC link. The maximal load current $\hat{I}_{ch2}$ depends on the application.
The next parameter is the maximal current value $\hat{I}_{ac}$ in the inductor L_d to avoid saturation of the inductor. If the inductor L_d goes into saturation, the current will rise immediately like in a short-circuit and the semiconductors will be destroyed. If there is a partial saturation (The current I_{ac} will be too high and will cause a DC current which will oscillate with the resonant current), the LC circuit oscillation can be activated, with L_d and C_d as resonant elements.

$$\hat{I}_{ac} = \begin{cases} \hat{I}_{ac1} + I_{margin} & U_{dc1} > U_{dc2} \\ \hat{I}_{ac2} + I_{margin} & U_{dc1} \leq U_{dc2} \end{cases} \tag{4.25}$$

The security margin current should be about 20% to 30% more than the maximal AC link current $\hat{I}_{ac}$.
The next component of the DC-DC converter is the decoupling capacitor C_d. The resonant frequency f_{LC} caused by the series-connection of C_d and L_d must be much smaller than the switching frequency f_p:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_{\sigma tot}C_d}} \leq 5 \cdot f_p \tag{4.26}$$

So the capacitor is given by the following Equation:

$$C_d = \frac{1}{4\pi^2 f_{LC}^2 L_{\sigma tot}} \tag{4.27}$$

Although the capacitor C_d is very big, there will be a small voltage oscillation on the decoupling capacitors C_d. It is important to know the maximal possible amplitude in order to choose the right capacitor value.

$$U_{Cd_{max}} = \frac{1}{C_d}\int_0^{\frac{\delta_{max}}{4\pi f_p}} \frac{4\pi f_p \hat{I}_{ac}}{\delta_{max}} t dt = \frac{\hat{I}_{ac}\delta_{max}}{8\pi f_p C_d} \tag{4.28}$$

To avoid a DC current on both sides of the DC-DC converter, the capacitor must be split into two partial capacitors C_{d1} and C_{d2}:

$$C_{d1} = C_{d2} = 2C_d \tag{4.29}$$

$$U_{Cd1_{max}} = U_{Cd2_{max}} = \frac{1}{2}U_{Cd_{max}} \tag{4.30}$$

The last parameter that has to be computed for the DC-DC converter is the output capacitor, which allows to stabilize the voltage U_{dc2}. A big capacitor allows to control a stable voltage with only few ripple, but any change of the set value will require a long transient time. If the capacitor is small, the ripple will be bigger, but the dynamic performance of the controlled voltage towards set value changes will be better. A proposal for the capacitor value is given in Equation (4.31).

$$C_{dc2} = 50 \cdot \frac{\hat{I}_{ch2}}{U_{dc2} f_p} \tag{4.31}$$

Anyway the voltage ripple depends also on the controller system performance (small time constant) and on the chosen control strategy. More on this topic can be found in Section 5.1.2.

Modulation of the rectangular mode

There are four commutation states of the power switches in order to achieve the rectangular modulation method. The Table (4.3) below shows the sequence of four different states of the modulator. A fifth state is added for the zero-power transfer or of course for the case where the DC-DC converter is not active. The states A, B, C and D are referred to the letters given in Figure (4.9).

State	T1	T2	T3	T4	T5	T6	T7	T8	U_{ac1}	U_{ac2}	Duration
A	1	0	0	1	1	0	0	1	$+U_{dc1}$	$-U_{dc2}$	τ_A
B	1	0	0	1	0	1	1	0	$+U_{dc1}$	$+U_{dc2}$	τ_B
C	0	1	1	0	0	1	1	0	$-U_{dc1}$	$+U_{dc2}$	τ_A
D	0	1	1	0	1	0	0	1	$-U_{dc1}$	$-U_{dc2}$	τ_B
E	0	0	0	0	0	0	0	0	0	0	-

Table 4.3: Commutation sequence of the switches for the rectangular mode

The parameters τ_A and τ_B are angles which are calculated as follows:

$$\tau_A = \delta \tag{4.32}$$

$$\tau_B = \pi - \delta \tag{4.33}$$

This values are calculated into time values by using the following Equation:

$$T_{A,..,D} = \frac{\tau_{A,..,D}}{2\pi f_p} \tag{4.34}$$

If the power is transferred from the primary side to the secondary side, the sequence of the modulation is (A,B,C,D). In the case where the transferred power is negative, this means the current $\overline{I}_{dc2}$ must be negative, the modulation sequence is reversed (D,C,B,A). Changes of the modulation states times are usually done in the states A or C, but this is not very important to be respected. The highest possible switching frequency for this modulation method is limited by the chosen blanking time of the semiconductor switches:

$$f_{p(max)} = \frac{1}{2\tau_{blank}} \tag{4.35}$$

A state-machine as an implementation method for the rectangular modulation is shown below. A counter represented by the time t is reset each time when new state is active.

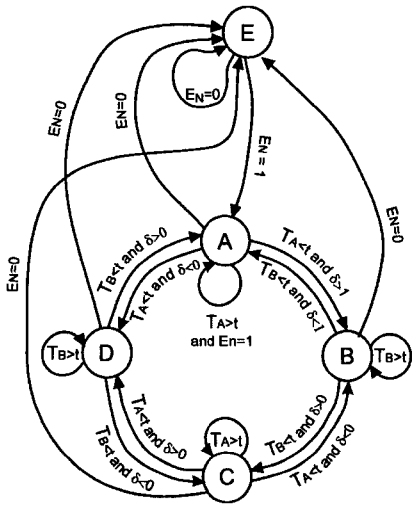

Figure 4.11: State machine for the rectangular current modulation

The following Figure (4.12) shows the efficiency for two different power switch technologies. The numerical values are taken for a DC-DC converter with a nominal power of 300kW. The losses for the SiC power semiconductor are estimated. The detailed numerical values and the computation principle of the losses is given in Appendix A.7. The transformer losses are not taken into account in this computing. The efficiency for small phase-shifts of δ is very poor, when the two voltages U_{dc1} and U_{dc2} are not the same. The highest efficiency is found at the transition from case I to case II. This is due to the fact that the current I_{ac} crosses zero, when one of pair of semiconductors do the turn-off. The two cases are described in the commutation paragraph at page 112. The parameters for this computation is found in the Table (4.4):

U_{dc1}	2100V
U_{dc2}	2800V
$L_{\sigma tot}$	100μH
$P_{dc2_{(max)}}$	914kW

Table 4.4: Parameters to compute the efficiency

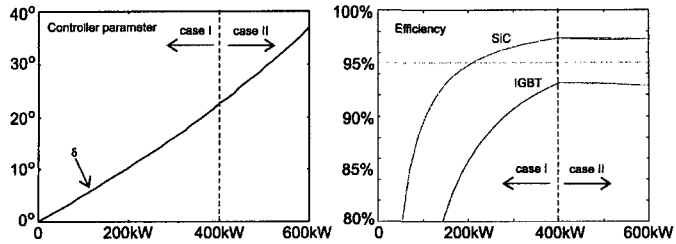

Figure 4.12: Efficiency and modulation parameters in function of transferred power

Commutations of the rectangular mode

The rectangular modulation method interacts only on the AC voltages U_{ac1} and U_{ac2}, regardless to the situation of the current I_{ac}. In order to analyze the losses generated by the proposed DC-DC converter, two different cases have to be distinguished, concerning the current I_{ac}. The Figure (4.13) show the two different current situations:

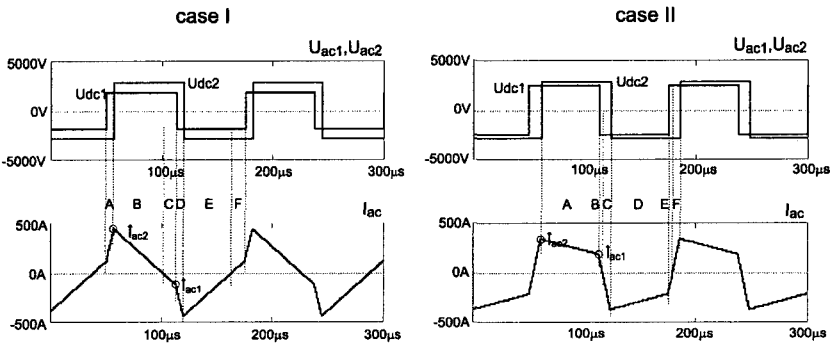

Figure 4.13: The two different modulation situations

In the case where the two voltages U_{dc1} and U_{dc2} are different, there is a situation where the current I_{ac} changes its sign value during the commutation states B and D. If the current is staying positive in the states B and D, the converter will only generate turn-off losses. This means a converter can be designed using an appropriate turn-off snubber on all the switches. But if the current I_{ac} crosses the zero-current line and changes its sign value, the converter will generate as well turn-on as turn-off losses. A snubber design seems more difficult. The limit condition, where the current I_{ac} goes through zero while the modulator changes from modulation state B to C or D to A is given in the Equation (4.38).

$$\delta = \frac{\pi}{2}\left(1 - \frac{U_{dc1}}{U_{dc2}}\right) \tag{4.36}$$

Case I: Modulation with turn-on and turn-off losses There are four switching events where losses are generated. The modulation sequence is indexed in the six steps A, B, C, D , E and F, the according voltage and current situations can be seen in the situation schematics in Figure (4.14) and in the waveform Figure (4.13). These waveform situations should not be confused with the modulation states shown in Figure (4.9). The four switching events are the transitions AB, DE, CD and FA. The condition for δ, where the current is going to change the sign value is given in the Equation below:

$$\delta \geq \frac{\pi}{2}\left(1 - \frac{U_{dc1}}{U_{dc2}}\right) \tag{4.37}$$

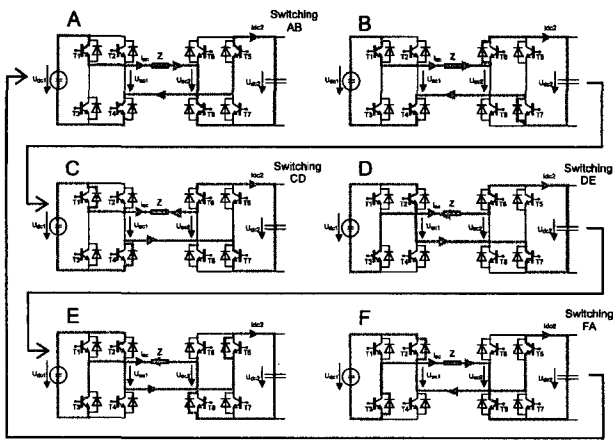

Figure 4.14: Case I with turn-on and turn-off losses

The next Table (4.5) shows all the commutation events of the converter. The capital letter T is used for the semiconductor switch (MOSFET, IGBT) while the letter D is representing the anti-parallel diodes of each switch. It is interesting to see that the turn-on losses are generated on that side of the DC-DC converter, where the DC voltage is smaller. In the represented case it is the primary side. Every switch is involved in the commutation cycle. The used semiconductor switches must be fast (commutation times T_{on} and T_{off} less than $1\mu s$ for a 50kW power converter working at $f_p = 20$kHz. Especially the anti-parallel diodes have to be fast so that they commutate very quickly, when the opposite power switch of the half-bridge is turned-off. This phenomenon is shown in three steps in the Figure (4.15)

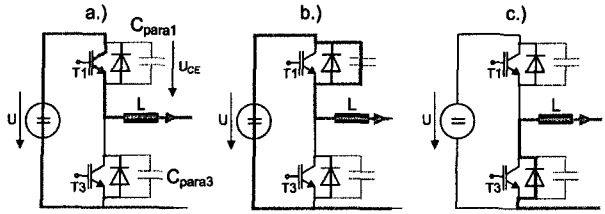

Figure 4.15: Diode commutation in a half-bridge

If the commutation of the diodes is too slow, there will be additional turn-on losses caused by the switches in parallel with the diodes. This effect can be avoided if the parasitic capacitor C_{para1}, C_{para3} across each power switch is as small as possible.

Transition	Commutation	Seminconductor	U	I
AB	Turn-off T5, T8	Switch	U_{dc2}	$\hat{I}_{ac2}$
	Turn-on D5, D8	Diode	U_{dc2}	$\hat{I}_{ac2}$
CD	Turn-on T2, T3	Switch	U_{dc1}	$\hat{I}_{ac1}$
DE	Turn-off T6, T7	Switch	U_{dc2}	$\hat{I}_{ac2}$
	Turn-on D6, D7	Diode	U_{dc2}	$\hat{I}_{ac2}$
FA	Turn-on T1, T4	Switch	U_{dc1}	$\hat{I}_{ac1}$

Table 4.5: Commutation event in the case I of the rectangular mode

Case II: Modulation without any turn-on losses If the current does not change its sign value, the current will remain always in the power switches and will not change to the opposite side diode of the half-bridge like in the case I. That is why there will be only turn-off losses. This makes a snubber design easier. The condition for δ to stay in the case II is shown in Equation (4.38):

$$\delta < \frac{\pi}{2}\left(1 - \frac{U_{dc1}}{U_{dc2}}\right) \tag{4.38}$$

In this Equation it can be seen that if the two DC voltages are equal, the DC-DC converter always operates in the case II. The current situation in the switches is shown in Figure (4.16).

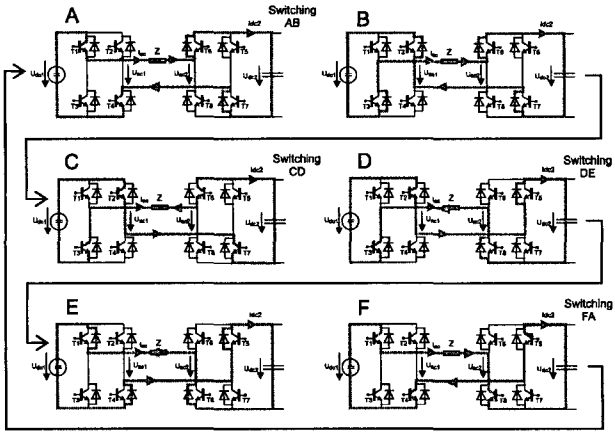

Figure 4.16: Case II without turn-on losses

The Table below shows the commutation events. Every switch is involved doing one turn-off per period, and every diode does one turn-on. If the two DC voltages are the same, the losses are distributed perfectly. The side of the DC-DC converter, which has the smaller DC voltage will also have the smaller turn-off current $\hat{I}_{ac1}$ and $\hat{I}_{ac2}$.

Transition	Commutation	Seminconductor	U	I
AB	Turn-off T1, T4	Switch	U_{dc1}	$\hat{I}_{ac1}$
	Turn-on D2, D3	Diode	U_{dc1}	$\hat{I}_{ac1}$
CD	Turn-off T6, T7	Switch	U_{dc2}	$\hat{I}_{ac2}$
	Turn-on D5, D8	Diode	U_{dc2}	$\hat{I}_{ac2}$
DE	Turn-off T2, T3	Switch	U_{dc1}	$\hat{I}_{ac1}$
	Turn-on D1, D4	Diode	U_{dc1}	$\hat{I}_{ac1}$
FA	Turn-off T5, T8	Switch	U_{dc2}	$\hat{I}_{ac2}$
	Turn-on D6, D7	Diode	U_{dc2}	$\hat{I}_{ac2}$

Table 4.6: Commutation event in the case II of the rectangular mode

Control of the DC-DC converter using rectangular mode

The output voltage U_{dc2} of the DC-DC converter has to be controlled. The control system has been designed using a pseudo-continuous model. Only one PI-controller element as shown in (5.16) is used. The input of the controller is the voltage error $U_{dc2(err)}$:

$$U_{dc2(err)} = U_{dc2(set)} - U_{dc2} \tag{4.39}$$

The output of the controller is the only actively variable parameter, the phase shift δ. The phase shift value is the input of the next function block, called the function block

$G_{cm5}(s)$. This block contains the small time constants of the system and is described in Equation (4.41). The block must represent the action of the current $\overline{I}_{dc2}$, when the parameter δ is changed. Each δ will generate a current $\overline{I}_{dc2}$, with a certain proportional factor described with K_{cm5} and a certain time delay T_{pE5}

$$G_{cm5}(s) = \frac{K_{cm5}}{1 + sT_{pE5}} \tag{4.40}$$

The amplification factor of the transfer function K_{cm5} is the result of the Equation below:

$$K_{cm5} = \frac{\overline{I}_{dc2}}{\delta} \tag{4.41}$$

By using the Equation (4.20) to resolve the Equation (4.41), it can be seen that the amplification is depending on the two parameters U_{dc1} and on the input parameter δ. This means that this transfer function is not linear. The transfer function is shown in the Figure (4.17), in dependence of the two parameters.

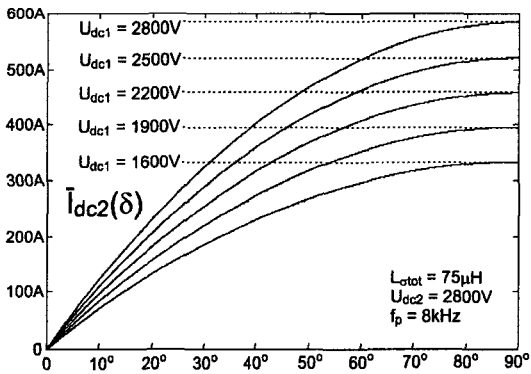

Figure 4.17: Transfer function of $\overline{I}_{dc2}$ depending on δ

If the input voltage of the DC-DC converter U_{dc1} does only vary slightly (around 10%) and the maximal phase shift value δ_{max} is limited to a reduced value, the transfer function is nearly linear. By choosing an operating point in order to simplify the control algorithm, a value for K_{cm5} can be found.

$$K_{cm5} = \frac{U_{dc1(nom)}(\pi - \delta_{nom})}{2\pi^2 f_p L_{\sigma tot}} \tag{4.42}$$

The nominal value for δ can be found by solving the Equation (4.21) for δ by replacing the power P_{dc2} with the nominal power. The small time constant T_{pE5} contains all system delays like the sampling time, the measurement delay of the processor system and the modulation. A small time constant T_{pE5} makes the controller powerful, because

the controller will be able to react faster on set value changes and perturbations. The parameter is composed as follows:

$$T_{pE5} = \frac{1}{2}T_{sample} + T_{cm5} + T_{r5} \tag{4.43}$$

T_{sample} is the sampling time of the processor system. The time delay T_{cm5} is the delay time caused by the modulator. This is defined in [38] and has the following value:

$$T_{cm5} = \frac{1}{2f_p} \tag{4.44}$$

The value T_{r5} contains the remaining delay times like the measurement delay from the AD-converters and the signal filtering plus the delay caused by the computing of the control algorithm. This time constant T_{r5} is normally smaller than the sampling time. Finally the transfer function of the system has to be defined, called $G_{S5}(s)$. The output voltage U_{dc2} is generated through an integration of the current flowing into the capacitor C_{dc2}. Of course the current entering the capacitor is the difference between the current generated by the DC-DC converter $\overline{I}_{dc2}$. The transfer function for the system is:

$$G_{S5}(s) = \frac{1}{sT_{I5}} = \frac{1}{sC_{dc2}} \tag{4.45}$$

If the output capacitor of the controller system is an electrolytic capacitor, a non-negligible current represented by a resistance R in parallel with the capacitor decharges the capacitor. The output voltage is mostly measured by a resistor bridge in parallel with the capacitor. This is why the system transfer function can also be described by a PT_1-element. The transfer function is:

$$G_{S5}(s) = \frac{K_{s5}}{1 + sT_{15}} = \frac{R}{1 + sRC_{dc2}} \tag{4.46}$$

The entire control system is represented in the Figure (4.18). The three elements controller, signal transfer function and the system transfer function are easily identified. The controller generates a preliminary value δ_1. The most important part of the controller system is the direct introduction of the perturbation value, represented as the function block $f_{\delta 2}$. It generates δ_2 and this value is a result of the current I_{ch2} and the supply voltage U_{dc1}. The current I_{ch2} is considered as the first perturbation value of the system, while the voltage U_{dc1} is the second perturbation value of the system. In each sampling period, the necessary value for δ_2 is calculated by the function block $f_{\delta 2}$. The function block $f_{\delta 2}$ contains the Equation (4.22).

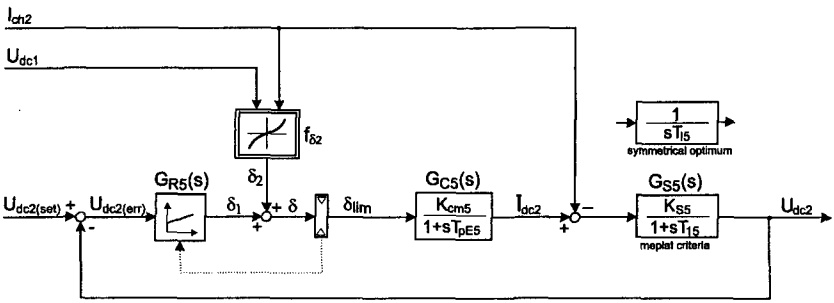

Figure 4.18: Controller schematics to control the output voltage U_{dc2}

The calculation of δ_2 allows the controller to produce a current $\bar{I}_{dc2}$, which is exactly the load current I_{ch2}. Thanks to the direct introduction of both perturbation values I_{ch2} and U_{dc1}, the necessary current is generated before the controller needs to react. There is only a small delay due to T_{pE5}, which cannot be avoided. The controller only needs to interact when the set value $U_{dc2(set)}$ is changed or if there is a voltage drift on the output capacitor. This method enhanced the controller system performance significantly.
The last step in the description of the controller system is the design of the controller parameters. The controller amplification factors are the two values K_{i5} and K_{p5}. The symmetrical optimum is used to design these two parameters, seen in [30] and [28]. It is an ideal method if the system behavior is integral and if the system needs a strong stability against perturbation influence. But the method is not ideal if the system must show an excellent performance towards set value changes. In reality, a DC-DC converter for a multilevel converter feeding will only rarely change the set value. The two time constant of the controller are:

$$T_{n5} = 4 \cdot T_{pE5} \tag{4.47}$$

$$T_{i5} = \frac{8 K_{cm5} {T_{pE5}}^2}{T_{I5}} \tag{4.48}$$

The amplification parameters resulting from the symmetrical optimum method are:

$$K_{i5} = \frac{T_{sample}}{T_{i5}} \tag{4.49}$$

$$K_{p5} = \frac{T_{n5} - \frac{T_{sample}}{2}}{T_{i5}} \tag{4.50}$$

The final parameters for the controller $G_{R5)}$ are the values given in (4.50), but divided through the factor 3. The direct introduction of the perturbation value allows to implement the controller with amplification factors for K_{i5} and K_{p5}.

$$K_{i5} = \frac{1}{3} K_{i5} \tag{4.51}$$

$$K_{p5} = \frac{1}{3} K_{p5} \tag{4.52}$$

The last improvement on the controller parameters is done regarding changes in the set value, especially when starting up a DC-DC converter or when feeding a 4Q-converter of the multilevel converter dynamically with variable voltage U_{dc2}. When the output capacitor U_{dc2} is charged to reach the set value, a big error will be integrated by the controllers integral state. The integrated error can cause a voltage overshoot with a voltage oscillation. This can introduce harmonics to a 4Q-converter. So when the error is big, the integral amplification factor K_{i5} is set to a smaller value than the nominal value given in (4.52). The values for K_{i5} depending on the error $U_{dc2(err)}$ are given below:

$$K_{i5} = \begin{cases} K_{i5} & |U_{dc2(err)}| < 2\% \\ \frac{K_{i5}}{2} & 2\% < |U_{dc2(err)}| < 4\% \\ \frac{K_{i5}}{5} & 4\% < |U_{dc2(err)}| \end{cases} \tag{4.53}$$

The experience has shown that the use of this adaptive value for the integration amplification K_{i5} improves the performance of the control system towards the changes of the set value.

A simulation of this control method has been implemented on MATLAB/SIMULINK. The DC-DC converter was simulated using the following parameters:

U_{dc1}	50VDC + 15VAC/$33\frac{1}{3}$ Hz	Feeding voltage
$L_{\sigma_{tot}}$	160μH	Decoupling inductance
C_{dc2}	680μF	Output capacitor
δ_{nom}	30°	Nominal value δ
f_p	19.5kHz	switching frequency
$C_{d1} = C_{d2}$	200μF	Decoupling capacitor
T_{sample}	200μs	Sampling frequency
$T_{\tau 5}$	80μs	Small time constants

Table 4.7: Numerical values for the simulated DC-DC converter

The DC link voltage U_{dc1} is a DC voltage with a superposed oscillation with an amplitude of 15V and a frequency of $33\frac{1}{3}$Hz. It can be seen in the simulation that when the DC feeding voltage is at a minimum and the load current I_{ch2} is maximal, the converter controller already saturates with $\delta = 90°$. This is why there must be enough power transfer margin when choosing the decoupling inductance. The behavior of the system towards the perturbation values U_{dc1}, I_{ch2} is excellent due to the prediction of the value δ.

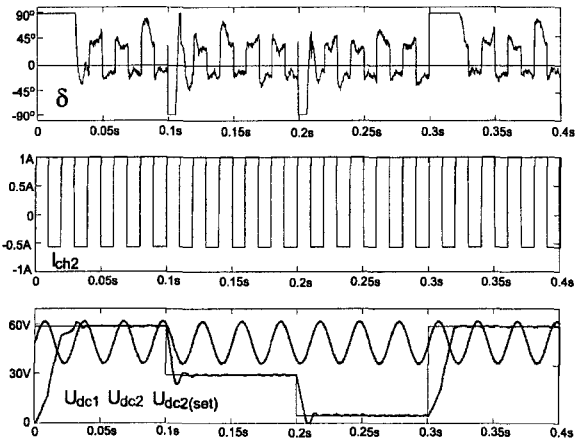

Figure 4.19: Simulated DC-DC converter with changes of the set value $U_{dc2(set)}$

4.2.2 Modulation and control with the combined triangular and trapezoidal current mode

The combined triangular and trapezoidal current modulation method is a modulation principle allowing the control of the output voltage U_{dc2}. It is a hard-switched method. The AC current circulating in the AC link with the medium-frequency transformer will follow a predefined waveform: The current will have either a trapezoidal or a triangular waveform, by respecting a special set of modulator timings. This will force the current through zero, in order to achieve zero-current switching for half of the commutation events. Compared to the rectangular current mode, this method allows a high reduction of the semiconductor turn-off losses. The two modulation methods are describe in the following two sections:

The trapezoidal current mode

The two AC voltages are modified in the impulse length Ω_{d1}, Ω_{d2} and the phase shift δ in order to achieve zero-current switching on each side of the DC-DC converter. By turning on U_{dc1} to the intermediary circuit the current ramps from zero to the value $\hat{I}_{ac2}$. Then the voltage U_{dc2} is switched to the intermediary circuit. The current goes down to $\hat{I}_{ac1}$. Then U_{dc1} is switched off the circuit, so that the current drops to zero. At this moment, the voltage U_{dc2} is switched off. To enhance efficiency, the next current integration is made as fast as possible. At least the modulator has to wait a blanking time period τ_{blank} before starting the next ramping. This blanking time is defined by the speed of the IGBT switches and is typically between 2μs and 7μs.
So the period with zero current (period D and H) are always as long as the blanking time τ_{blank}. The important disadvantage is that this modulation method cannot be used if one of the voltages is zero. This means that the secondary side capacitor cannot be charged by this modulation method if the voltage across is zero.

Advantages:
- High power transfer possible
- Usable for different and equal input voltages U_{dc1} and U_{dc2}
- High efficiency (4 turn-offs on the power semiconductors)
- Triangular mode is a special case of the trapezoidal mode

Disadvantages:
- Unsymmetrical share of the losses on the half-bridge if the two voltages are not equal
- Not useable if one of the DC voltages is small or close to zero (No power transfer possible)
- Complicated control and modulation algorithm

The intermediary circuit current is not measured. By knowing the exact value for the blanking time τ_{blank}, the switching frequency f_p and the decoupling inductance $L_{\sigma tot}$, the current will always be turned off in the zero-crossing. If the transformer is designed correctly, there is no problem with saturation effects caused by an oscillating magnetizing current I_m.

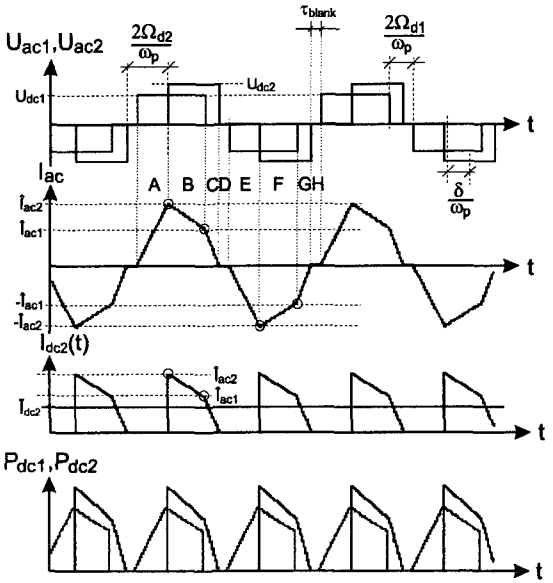

Figure 4.20: Voltage and current waveforms for the trapezoidal mode

Mathematical description of the modulation

The trapezoidal mode works within an upper and lower power limit. The operating point for the lowest and highest possible power transfer has to be found. The variable parameter is the phase-shift δ. The other parameters depend on δ and can afterwards be calculated. Two different cases have to be distinguished:

Case I: the input voltage is lower than the output voltage

The mathematical condition for the first case is given with the Equation (4.54)

$$U_{dc1} \leq U_{dc2} \tag{4.54}$$

The start value for δ can be found by using the Equation (4.55)

$$\delta_{Pmin,trap} = \pm\frac{\pi(1-2\tau_{blank}f_p)}{2}\left[1-\frac{U_{dc1}}{U_{dc2}}\right] \tag{4.55}$$

The highest possible power transfer is found by making the derive of the power transfer by delta and setting the resulting expression to zero. It can be seen that it is not allowed to put $U_{dc2}=0$. So $\delta_{Pmax,trap}$ is computed by:

$$\delta_{Pmax,trap} = \pm\frac{\pi(1-2\tau_{blank}f_p)}{2}\left[\frac{{U_{dc1}}^2+{U_{dc2}}^2}{{U_{dc1}}^2+U_{dc1}U_{dc2}+{U_{dc2}}^2}\right] \tag{4.56}$$

So δ must be varied within the period given with Equation (4.55) and (4.56). The two other parameters are:

$$\Omega_{d1} = \frac{\pi(U_{dc1} - U_{dc2}) + 2U_{dc2}(|\delta| + 2\pi\tau_{blank}f_p)}{2(U_{dc1} + U_{dc2})} \tag{4.57}$$

$$\Omega_{d2} = |\delta| - \Omega_{d1} + 2\pi\tau_{blank}f_p \tag{4.58}$$

The transferred power is given by the Expression (4.59):

$$\begin{aligned} P_{dc2} &= sgn(\delta)\frac{U_{dc2}(\pi - |\delta| - \Omega_{d1} - \Omega_{d2})\left[U_{dc2}(|\delta| - \Omega_{d2} + \Omega_{d1}) + U_{dc1}(|\delta| - \Omega_{d1} + \Omega_{d2})\right]}{4L_{\sigma tot}\pi^2 f_p} \\ &\quad + sgn(\delta)\frac{{U_{dc2}}^2(|\delta| - \Omega_{d2} + \Omega_{d1})^2}{4L_{\sigma tot}\pi^2 f_p} \end{aligned} \tag{4.59}$$

The turn-off currents are then calculated with:

$$\hat{I}_{ac1} = \frac{U_{dc2}(|\delta| - \Omega_{d2} + \Omega_{d1})}{2L_{\sigma tot}\pi f_p} \tag{4.60}$$

$$\hat{I}_{ac2} = \frac{U_{dc1}(|\delta| - \Omega_{d1} + \Omega_{d2})}{2L_{\sigma tot}\pi f_p} \tag{4.61}$$

The voltage controller for the DC-DC converter needs a prediction of δ. By measuring I_{ch2}, U_{dc1} and U_{dc2} the desired δ will be predicted. The current $\overline{I}_{dc2}$ cannot be measured. But I_{ch2} can be measured (load current) and should anyway be equal to the DC component of $\overline{I}_{dc2}$. When all the modulation parameters are known, the current $\overline{I}_{dc2}$ and is given in the equation below:

$$\begin{aligned} \overline{I}_{dc2} &= sgn(\delta)\frac{(\pi - |\delta| - \Omega_{d1} - \Omega_{d2})\left[U_{dc2}(|\delta| - \Omega_{d2} + \Omega_{d1}) + U_{dc1}(|\delta| - \Omega_{d1} + \Omega_{d2})\right]}{4L_{\sigma tot}\pi^2 f_p} \\ &\quad + sgn(\delta)\frac{U_{dc2}(|\delta| - \Omega_{d2} + \Omega_{d1})^2}{4L_{\sigma tot}\pi^2 f_p} \end{aligned} \tag{4.62}$$

The Equation set for the δ-prediction is given in (4.63), (4.64) and (4.65) At first, three expressions have to be calculated, which are afterwards introduced to the final Equation (4.66):

$$ex_1 = {U_{dc1}}^2 + {U_{dc2}}^2 \tag{4.63}$$

$$ex_2 = {U_{dc1}}^2 + U_{dc1}U_{dc2} + {U_{dc2}}^2 \tag{4.64}$$

$$ex_3 = {U_{dc1}}^2 U_{dc2} \tag{4.65}$$

and finally:

$$\delta = sgn(I_{ch2})\pi\left(\frac{ex_1(1-2\tau_{blank}f_p)}{2ex_2} - \frac{(U_{dc1}+U_{dc2})\sqrt{ex_3(4{f_p}^2{\tau_{blank}}^2+1)-4f_p(|I_{ch2}|L_{\sigma tot}ex_2+\tau_{blank}ex_3)}}{2\sqrt{U_{dc1}}ex_2}\right) \quad (4.66)$$

If δ is imaginary, the trapezoidal mode is not possible for the three measured values I_{ch2}, U_{dc1} and U_{dc2}. This means it is not possible to generate a current I_{dc2} equal to I_{ch2}. Expressed in an equations, the condition is:

$$4f_p(I_{ch2}L_{\sigma tot}ex_2+\tau_{blank}ex_3+ex_3)+ex_3 < 4{f_p}^2{\tau_{blank}}^2ex_3 \quad (4.67)$$

And of course δ cannot be imaginary:

$$Im(\delta) = 0 \quad (4.68)$$

The maximal possible power transfer is given by Equation (4.69). The expression is found by making the derivative of the power transfer by delta and setting the resulting expression to zero. This equation can be used for the design of the size for the decoupling inductance. The inductance is the passive component limiting the power transfer.

$$P_{dc2_{(trap,max)}} = \frac{{U_{dc1}}^2{U_{dc2}}^2(1-2\tau_{blank}f_p)^2}{4f_pL_{\sigma tot}({U_{dc1}}^2+U_{dc1}U_{dc2}+{U_{dc2}}^2)} \quad (4.69)$$

The minimal power transfer of the trapezoidal mode is the maximal power transfer of the triangular mode.

Case II: Input voltage is higher than output voltage

The mathematical condition for the first case is given with the Equation (4.70):

$$U_{dc1} > U_{dc2} \quad (4.70)$$

The start value for δ can be found by the Equation (4.71). U_{dc1} and U_{dc2} are swapped in this expression comparing to the Equation (4.55).

$$\delta_{Pmin} = \pm\frac{\pi(1-2\tau_{blank}f_p)}{2}\left[1-\frac{U_{dc2}}{U_{dc1}}\right] \quad (4.71)$$

The upper boundary for δ is found in Equation (4.56). It stays the same for both cases. So $P_{dc2_{trap,max}}$ is also achieved with this value of δ.

$$\Omega_{d1} = |\delta| - \Omega_{d2} + 2\pi\tau_{blank}f_p \quad (4.72)$$

$$\Omega_{d2} = \frac{\pi(U_{dc2}-U_{dc1})+2U_{dc1}(|\delta|+2\pi\tau_{blank}f_p)}{2(U_{dc1}+U_{dc2})} \quad (4.73)$$

The transferred power P_{dc2} is expressed by the same Equation (4.69) for both modes. It only has to be respected that the modulation parameters Ω_{d1} and Ω_{d2} have changed. Also the turn-off currents and the maximal possible power transfer are then calculated by the same equations by using the new parameters.

The triangular current mode

The triangular current mode can be seen as a special case of the trapezoidal mode. The period C and G of the trapezoidal mode are not used, because the current is already zero at the end of the periods B and E. The current is ramped in order to achieve zero-current switching on one full-bridge. This modulation method is only possible, if the two input voltages U_{dc1} and U_{dc2} are different. But if one of the two voltages is equal to zero, this method cannot be used. By doing it this way, large capacitor charging currents can be prevented. The blanking times of the IGBT switches have to be respected. This time τ_{blank} determines the shortest possible duration of the periods D and H of the modulation. The maximal power transfer is achieved, when the periods D and H have got the length of the blanking time.

Advantages:
- Lowest switching losses for all hard-switching methods
- Only two turn-offs per period of switching
- Ideal modulation method if the two voltages U_{dc1} and U_{dc2} are different
- Triangular mode is a special case of the trapezoidal mode

Disadvantages:
- Turn-offs are always performed by the same two switches
- Inefficient use of the period for power transfer, so limited power transfer possible
- The triangular mode is not possible if one of the two DC voltages is zero
- Complicated modulation and control algorithm (combination with the trapezoidal mode)

Mathematical description of the modulation

The given parameters are the two voltages (measured by voltage probes) and the system parameters like the switching frequency f_p, the blanking time τ_{blank} and the decoupling inductance $L_{\sigma tot}$. At first, the parameters for the modulation have to be found. The variable parameter is again δ. The other parameters depend on δ and can be calculated afterwards. Again the two different cases have to be distinguished:

Case I: the input voltage is lower than the output voltage

The mathematical condition for the first case is of course the same like in the trapezoidal mode:

$$U_{dc1} \leq U_{dc2} \tag{4.74}$$

δ is now chosen. If δ is zero, there is no power transfer. So to start, δ is to be set at 0^o. The higher δ is, the more power is transferred. There is an angle $\delta_{Pmax,tri}$ for the maximal power transfer with the triangular current mode, given by Equation (4.76):

$$\delta_{Pmin,tri} = 0 \tag{4.75}$$

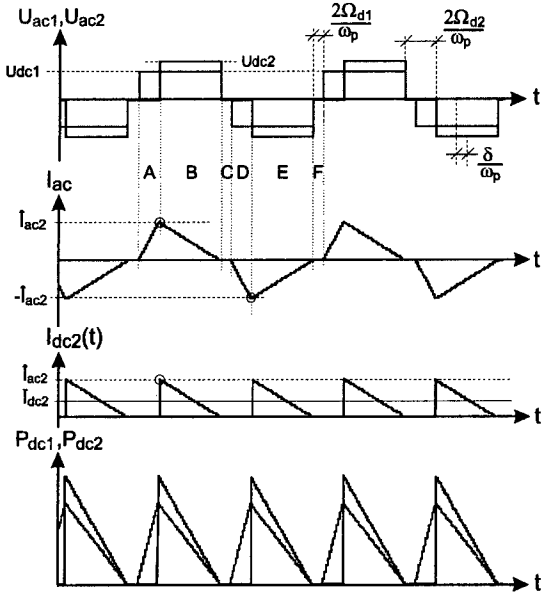

Figure 4.21: Voltage and current waveforms for the triangular mode

$$\delta_{Pmax,tri} = \pm\frac{\pi(1-2\tau_{blank}f_p)}{2}\left[1-\frac{U_{dc1}}{U_{dc2}}\right] \tag{4.76}$$

For a positive power flow, the sign of δ is positive, otherwise negative. It can be seen that U_{dc2} cannot be zero. After having chosen δ, the other two parameters are calculated as follows:

$$\Omega_{d1} = \frac{\pi}{2} - \frac{|\delta|U_{dc2}}{U_{dc2}-U_{dc1}} \tag{4.77}$$

$$\Omega_{d2} = |\delta| + \Omega_{d1} \tag{4.78}$$

So the transferred power is given by the expression:

$$P_{dc2} = \frac{U_{dc1}U_{dc2}\delta(\pi-2\Omega_{d2})}{2\pi^2 L_{\sigma tot}f_p} \tag{4.79}$$

And the turn-off current is computed with:

$$\widehat{I}_{ac2} = \frac{U_{dc1}|\delta|}{\pi L_{\sigma tot}f_p} \tag{4.80}$$

Also for the triangular mode, the controller for the DC-DC converter needs a prediction of δ based on the measured voltages U_{dc1}, U_{dc1} and I_{ch2}. I_{ch2} is the current required

from the load, in this case from a four-quadrant inverter of the multilevel structure. The desired δ will be predicted. The other two modulation parameters are calculated afterwards by Equation (4.77) and (4.78). The Equation for the δ-prediction is given below:

$$\delta = sgn(I_{ch2}) \frac{\pi \sqrt{|I_{ch2}| L_{\sigma tot} f_p (U_{dc2} - U_{dc1})}}{U_{dc1}} \tag{4.81}$$

If δ has an imaginary component, the triangular mode is not possible for the three measured values I_{ch2}, U_{dc1} and U_{dc2}. Like in the trapezoidal mode, this relation is expressed with the following equation:

$$32 f_p |I_{ch2}| L_{\sigma tot} (U_{dc2} - U_{dc1}) + (U_{dc1} - U_{dc2})^2 > 0 \tag{4.82}$$

For the controller it is important, whether the triangular or the trapezoidal current mode has to be used. This must be decided based on the required and measurable power in Equation (4.83)

$$P_{dc2} = I_{ch2} \cdot U_{dc2} \tag{4.83}$$

The maximal power transfer for the triangular mode is given with:

$$P_{dc2_{(tri,max)}} = \frac{{U_{dc1}}^2 (1 - 2\tau_{blank} f_p)^2 (U_{dc2} - U_{dc1})}{4 L_{\sigma tot} f_p U_{dc2}} \tag{4.84}$$

By comparing Equation (4.84) with the actual power demanded (4.83), it can be decided which modulation method has to be used.

Case II: the input voltage is higher than the output voltage

The next equation defines the second case:

$$U_{dc1} > U_{dc2} \tag{4.85}$$

δ is now chosen. For zero power transfer, δ is to be set at 0^o. There is an angle $\delta_{Pmax,tri}$ for the maximal power transfer with the triangular mode, given by Equation (4.87):

$$\delta_{Pmin,tri} = 0 \tag{4.86}$$

$$\delta_{Pmax,tri} = \pm \frac{\pi (1 - 2\tau_{blank} f_p)}{2} \left[1 - \frac{U_{dc2}}{U_{dc1}} \right] \tag{4.87}$$

For a positive power flow, the sign of δ is positive, otherwise negative. It can be seen that U_{dc2} cannot be zero. Physically no power can be transferred, which causes a division by zero. After having chosen δ, the other two parameters are calculated as follows:

$$\Omega_{d1} = |\delta| + \Omega_{d2} \tag{4.88}$$

$$\Omega_{d2} = \frac{\pi}{2} + \frac{|\delta| U_{dc1}}{U_{dc2} - U_{dc1}} \tag{4.89}$$

In contradiction to the trapezoidal mode, the power transfer equation has changed. The transferred power is now given by the following expression:

$$P_{dc2} = \frac{U_{dc1}U_{dc2}\delta(\pi - 2\Omega_{d1})}{2\pi^2 L_{\sigma tot} f_p} \tag{4.90}$$

Also for the triangular mode, the controller for the DC-DC converter needs a prediction of δ. The desired δ will be predicted. The other two parameters are calculated afterwards by Equation (4.88) and (4.89). The Equation for the δ-prediction is given below:

$$\delta = sgn(I_{ch2})\frac{\pi\sqrt{|I_{ch2}|L_{\sigma tot}f_p(U_{dc1} - U_{dc2})}}{\sqrt{U_{dc1}U_{dc2}}} \tag{4.91}$$

If δ has an imaginary component, the triangular mode is not possible for the three measured values I_{ch2}, U_{dc1} and U_{dc2}. Once again this means that the DC-DC converter cannot generate a current $\overline{I}_{dc2}$ equal to the required current I_{ch2}. Expressed in a equation, the condition is:

$$32f_p|I_{ch2}|L_{\sigma tot}(U_{dc1} - U_{dc2}) + (U_{dc2} - U_{dc1})^2 > 0 \tag{4.92}$$

For the controller it is important, whether the triangular or the trapezoidal current mode has to be used. The maximal power transfer of the triangular mode in this case is given with:

$$P_{dc2_{(tri,max)}} = \frac{{U_{dc2}}^2(1 - 2\tau_{blank}f_p)^2(U_{dc1} - U_{dc2})}{4f_p L_{\sigma tot}U_{dc1}} \tag{4.93}$$

By comparing Equation (4.93) with the actual power demanded, it can be decided which modulation method has to be used.

Computing of the components for the combined trapezoidal and triangular mode

As described before, the converter can operate in a combined mode using the triangular and the trapezoidal current modulation. For low power transfers, the triangular mode is used, while for the high power transfers, the trapezoidal mode is employed. All the components for the DC-DC converter can be designed exactly in the same manner as in the Section 4.2.1, page 108, with exception of the decoupling inductor L_d. L_d must be designed by respecting the maximal possible power transfer of the trapezoidal mode, already shown in Equation (4.56). The decoupling inductor is:

$$L_d = \frac{{U_{dc1(nom)}}^2 U_{dc2(nom)}(1 - 2\tau_{blank}f_p)^2}{4f_p\widehat{I}_{ch2}(U_{dc1}^2 + U_{dc1}U_{dc2} + U_{dc2}^2)} - L_{\sigma 1} - L_{\sigma 2} \tag{4.94}$$

The inductor must in any case be chosen smaller that the value received in (4.94), in order to have enough security margin for the power transfer. In this modulation method, the inductor depends also on the blanking time τ_{blank}. The voltages are nominal values and not the minimal values. The maximal current for the inductor $\widehat{I}_{ac}$ as well as all the capacitor values for C_{dc2} and C_d can be calculated like in the rectangular mode.

Modulation using combined trapezoidal and triangular mode

If the DC-DC converter has to transfer a desired power P_{dc2}, it has to be decided if the triangular or the trapezoidal current mode has to be used. Of course the modulator must choose the method which causes the lowest losses for this situation. The losses of the most power semiconductors depend nearly linearly on the switched current [36]. So the idea is to prove that the next Equation (4.95) is always valid:

$$\hat{I}_{ac2_{tri}} < \hat{I}_{ac1_{trap}} + \hat{I}_{ac2_{trap}} \tag{4.95}$$

This Expression says that the sum of the two turned-off currents in the trapezoidal mode will always be bigger than the current turned-off in the triangular mode. To do this comparison, the trapezoidal mode has not been limited to the case where the two periods D and H are equal to the blanking time τ_{blank}:

$$D, H \geq \tau_{blank} \tag{4.96}$$

The transmitted power $P_{dc2_{tri}}$ of a triangular mode modulation is set equal to a power $P_{dc2_{trap}}$ of the trapezoidal mode, with the only condition that the two DC voltages U_{dc1} and U_{dc2} are not changed for the both modulation methods. All modulation parameters are eliminated and the Equation is resolved for the variable $\hat{I}_{ac2_{tri}}$. For two different voltage conditions the following Equation is found:

$$\hat{I}^2_{ac2_{tri}} U_{dc2} = \hat{I}^2_{ac2_{trap}} U_{dc2} - \hat{I}^2_{ac1_{trap}} U_{dc1} \qquad U_{dc2} \geq U_{dc1} \tag{4.97}$$

$$\hat{I}^2_{ac2_{tri}} U_{dc1} = \hat{I}^2_{ac2_{trap}} U_{dc1} - \hat{I}^2_{ac1_{trap}} U_{dc2} \qquad U_{dc2} < U_{dc1} \tag{4.98}$$

The currents $\hat{I}_{ac1}$, $\hat{I}_{ac2}$ and the two voltages U_{dc1} and U_{dc2} are by definition always positive. After some steps of mathematical evaluation, it can be found:

$$\hat{I}_{ac2_{tri}} < \hat{I}_{ac2_{trap}} + \sqrt{\frac{U_{dc1}}{U_{dc2}}} \hat{I}_{ac1_{trap}} \qquad U_{dc2} \geq U_{dc1} \tag{4.99}$$

$$\hat{I}_{ac2_{tri}} < \hat{I}_{ac1_{trap}} + \sqrt{\frac{U_{dc2}}{U_{dc1}}} \hat{I}_{ac2_{trap}} \qquad U_{dc2} < U_{dc1} \tag{4.100}$$

Due to the conditions on the voltages U_{dc1} and U_{dc2}, the coefficient in the root is always smaller than 1. This means that the Equation (4.95) is valid for all the cases. By relying on the fact that the losses depend linear on the switched current, the triangular mode must always be preferred to the trapezoidal mode, if the losses must be minimized. For the trapezoidal current mode, as described in the section before, an iterative algorithm has been used to calculate the sum of the converter losses in dependent on two modulation parameters δ and Ω_{d1}. The computing includes switching and conduction losses, but does not contain transformer losses. More details on the numerical values used are given in Appendix A.7. In any case, the parameter Ω_{d2} depends on the two other modulation parameters. The triangular modulation method can be seen as special case of the trapezoidal modulation method. The conditions respected for the two modulation methods were the following:

$$\delta \leq \Omega_{d1} + \Omega_{d2} \quad (4.101)$$
$$\Omega_{d1} \leq \delta + \Omega_{d2} \quad (4.102)$$
$$\Omega_{d2} \leq \delta + \Omega_{d1} \quad (4.103)$$
$$\delta \leq \pi - \Omega_{d1} - \Omega_{d2} \quad (4.104)$$

If these conditions are respected, the AC link current I_{ac} is crossing exactly two times zero, when there is a switching event (This means when one of the AC voltages U_{ac1} or U_{ac2} changes its value). This is the basic definition of the combined triangular/trapezoidal mode.

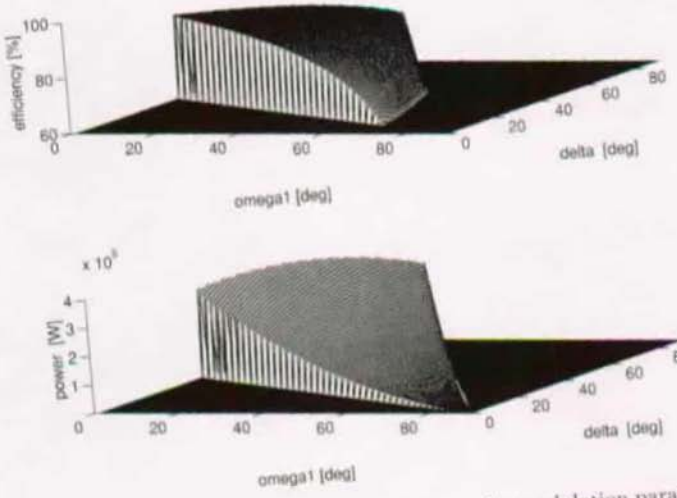

Figure 4.22: Efficiency and power in function of the modulation parameters

From the 3D graph shown in Figure (4.22), the following conclusions can be deduced from this analysis:

- If the two voltages U_{dc1} and U_{dc2} are equal, only the trapezoidal modulation method cannot be used. This has already been shown in the mathematical computing of the triangular mode.
- The main modulation parameter is δ. The other modulation parameters Ω_{d1} and Ω_{d2} are calculated in function of δ. If δ is varied from 0 to $\delta_{Pmax,tri}$ and from $\delta_{Pmin,trap}$ (which is equivalent to $\delta_{Pmax,tri}$) to $\delta_{Pmax,trap}$ the power is always increased constantly. This means that there is a certain proportionality between the parameter δ and the transferred power P_{dc2}. But it must be calculated at which value for δ it has to be switched between the two modes.

- If the two voltages U_{dc1} and U_{dc2} are not equal, a combined mode for the modulation is defined: For the power transfer from 0 to $P_{dc2_{(tri,max)}}$, the triangular current mode is used, because it is the most efficient way to transfer the power. At $P_{dc2_{(tri,max)}}$, the maximal possible transferable power for the triangular mode is reached. The the DC-DC converter has the highest possible efficiency for a hard-switched DC-DC converter. To transfer more power, the trapezoidal mode is taken, but with a small decrease of efficiency.

The following Figure (4.23) shows the efficiency for two different power switch techologies and the modulation parameters, if the described combined modulation method is used. The numerical values are taken from Appendix A.7. The efficiency for small phase-shifts of δ is poor. The highest efficiency is found at the transition from the triangular to the trapezoidal mode. The parameters for this computation is found in the Table (4.8):

U_{dc1}	1500V
U_{dc2}	2800V
$L_{\sigma tot}$	100μH
$P_{dc2_{(tri,max)}}$	326.45kW
$P_{dc2_{(trap,max)}}$	385.76kW

Table 4.8: Parameters to compute the efficiency

In this computing, the two voltage U_{dc1} and U_{dc2} are different. The maximal power transfer with the trapezoidal mode is slightly higher than the maximal power for the triangular mode.

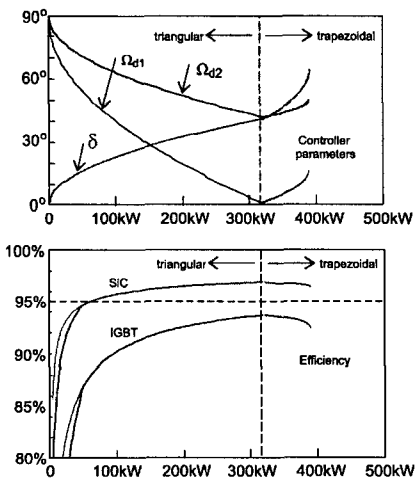

Figure 4.23: Efficiency and modulation parameters in function of transferred power

A modulator must be implemented for the combined triangular/trapezoidal modulation method. For this combined operation, there are eight different modulation states A,B,C,D,E,F,G and H. These states are shown in the Figure (4.24) as an example on the trapezoidal modulation method for both directions of the power transfer. The state machine is shown in Figure (4.26). If the power transfer is negative, the states are just sequenced in the inverse direction H,G,F,E,D,C,D and A. For the triangular modulation method, the stated C and G will not exist and must be jumped. The duration of the states are given in following Equation set:

$$\tau_{A,E} = \delta - \Omega_{d1} + \Omega_{d2} \tag{4.105}$$
$$\tau_{B,F} = \pi - \delta - \Omega_{d1} - \Omega_{d2} \tag{4.106}$$
$$\tau_{C,G} = \delta + \Omega_{d1} - \Omega_{d2} \tag{4.107}$$
$$\tau_{D,H} = -\delta + \Omega_{d1} + \Omega_{d2} \tag{4.108}$$

The state duration are expressed as angles and not as time values.

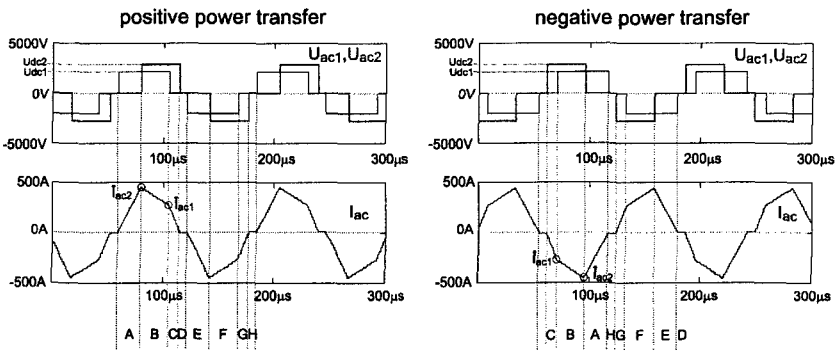

Figure 4.24: Modulator states shown on the trapezoidal mode

When the DC-DC converter is started up, there is no power consumption on the secondary side C_{dc2}. The voltage U_{dc2} will be zero. So neither the triangular mode nor the trapezoidal mode will be possible. To load the capacitor in this condition, a special modulation state machine is designed, consisting of the states K, L, M and N. In this modulation mode, only the primary side switches $T1$ to $T4$ are used to generate an alternative voltage. The secondary side works as a bridge rectifier and thus the capacitor C_{dc2} will charge. The graphs are visualized in the Figure (4.25). The output capacitor C_{dc2} is already charged to a small voltage value.

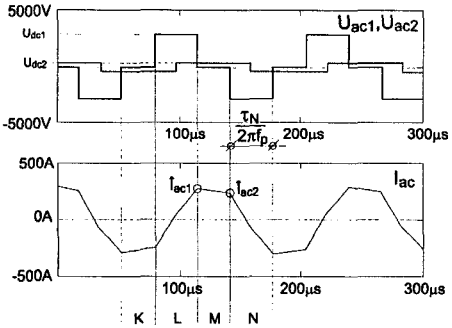

Figure 4.25: Load mode used to charge the output capacitor C_{dc2}

The capacitor will only be charged to a small voltage value (usually to 20% of the nominal value $U_{dc2(set)}$), afterwards the triangular mode can be applied to charge the DC-DC converter to the nominal output voltage. Only when the nominal value for U_{dc2} is established, a load current I_{ch2} should be accepted on the secondary side. The duration times for this modulation method have to be computed:

$$\tau_{K,M} = \pi - \frac{4\pi f_p \widehat{I}_{ac1(max)} L_{\sigma tot}}{U_{dc1}} \tag{4.109}$$

$$\tau_{L,N} = \frac{4\pi f_p \widehat{I}_{ac1(max)} L_{\sigma tot}}{U_{dc1}} \tag{4.110}$$

The corresponding time values for all the state duration angles can be found by:

$$T_{A,..,N} = \frac{\tau_{A,..,N}}{2\pi f_p} \tag{4.111}$$

A maximal peak current has to be chosen in order to decide which modulation time has to be selected. This peak current value should be at least 20% smaller than the inductor saturation current $\widehat{I}_{ac}$ and also should not exceed the maximal semiconductor current $I_{c(max)}$. The last state for the modulation is the state I, used for the DC-DC converter when no power is transferred. All the switches are open. The states with their switch positions are all represented in the Table (4.9):

State	T1	T2	T3	T4	T5	T6	T7	T8	U_{ac1}	U_{ac2}	Duration
A	1	0	0	1	1	1	0	0	$+U_{dc1}$	0	τ_A
B	1	0	0	1	0	1	1	0	$+U_{dc1}$	$+U_{dc2}$	τ_B
C	1	1	0	0	0	1	1	0	0	$+U_{dc2}$	τ_C
D	1	1	0	0	1	1	0	0	0	0	τ_D
E	0	1	1	0	1	1	0	0	$-U_{dc1}$	0	τ_A
F	0	1	1	0	1	0	0	1	$-U_{dc1}$	$-U_{dc2}$	τ_B
G	0	0	1	1	1	0	0	1	0	$-U_{dc2}$	τ_C
H	0	0	1	1	0	0	1	1	0	0	τ_D
I	0	0	0	0	0	0	0	0	0	0	-
K	0	0	1	1	0	0	0	0	0	$-U_{dc2}$	τ_K
L	1	0	0	1	0	0	0	0	$+U_{dc1}$	both	τ_N
M	1	1	0	0	0	0	0	0	0	$+U_{dc2}$	τ_K
N	0	1	1	0	0	0	0	0	$-U_{dc1}$	both	τ_N

Table 4.9: Modulator states for the combined triangular/trapezoidal modulation method

The efficiency and the power transfer capabilities of the DC-DC converter in the combined triangular/trapezoidal mode depend on the blanking time τ_{blank} chosen for the power semiconductor switches. This could be seen in the Equations (4.93) and (4.69). The blanking time for power semiconductors for a high power range is mostly more than $3\mu s$. The state times of D and H from this modulation method can never be shorter than τ_{blank}. When the maximum power $P_{dc2_{(max,tri)}}$ for the triangular current mode is reached, the two states D and H are during exactly the blanking time τ_{blank}.
The next Figure (4.26) shows the implemented modulation state graph for the combined triangular and trapezoidal modulation. Each time the modulator changes its state, the timer with t is reset. The start state for the modulation is the idle position I. As soon as power is transferred, the modulator starts with the state H, where both AC link voltages are zero. Changes of the modulation parameters are only tolerated, when the current I_{ac} is equal to zero, so in the states H and D. If the modulator is in the triangular modulation method, either the two states C and G are jumped ($U_{dc2} > U_{dc1}$) or the states A and E are jumped. ($U_{dc1} > U_{dc2}$). The load mode is a separate state loop with only one rotation direction. Depending on the sign of the modulation parameter δ (This means the sign of the power flow), the modulator states are sequenced clockwise (positive power) or inverse (negative power). If the modulator is disabled (variable E_n), the modulator can jump from any state back to the idle state I immediately.

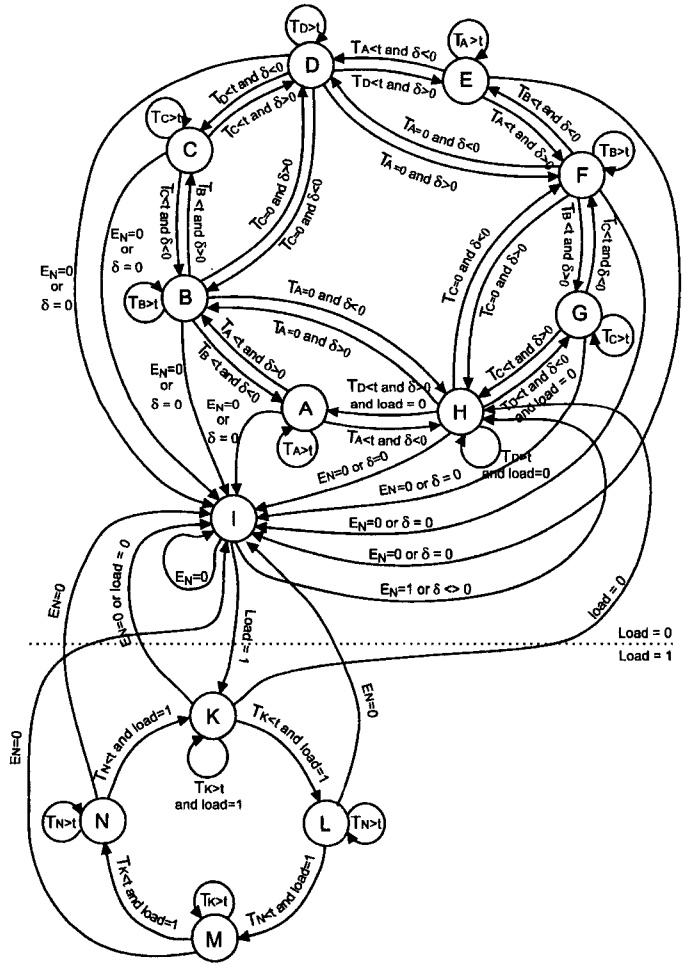

Figure 4.26: Entire state machine for the combined triangular/trapezoidal modulation method

Commutations of the combined trapezoidal and triangular mode

The combined triangular/trapezoidal modulation method acts with the two AC link voltages U_{ac1} and U_{ac2} on the current I_{ac}. By doing this and respecting the given mathematical rules, the current crosses zero at two switching events. This allows a significant reduction of the switching losses, while the conduction losses remain more or less the same. The conduction losses are about 25% of the total losses of the DC-DC converter in this power mode.

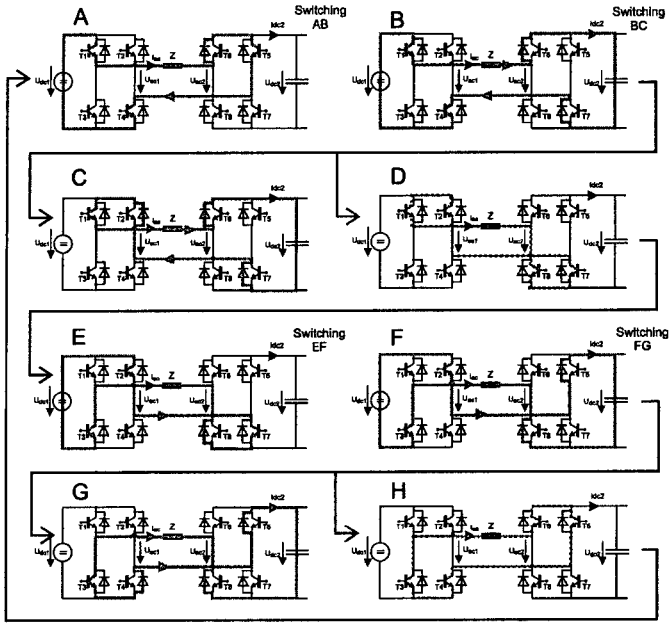

Figure 4.27: Current situation in a period of the triangular/trapezoidal mode

In the trapezoidal current mode, there are four switching situations, each with one power switch turn-off and a diode turn-on. All the four switching events are given in the Table (4.10).

Transition	Commutation	Seminconductor	U	I
AB	Turn-off T5	Switch	U_{dc2}	$\hat{I}_{ac2}$
	Turn-on D7	Diode	U_{dc2}	$\hat{I}_{ac2}$
BC	Turn-on T4	Switch	U_{dc1}	$\hat{I}_{ac1}$
	Turn-on D2	Diode	U_{dc1}	$\hat{I}_{ac1}$
EF	Turn-off T7	Switch	U_{dc2}	$\hat{I}_{ac2}$
	Turn-on D5	Diode	U_{dc2}	$\hat{I}_{ac2}$
FG	Turn-on T2	Switch	U_{dc1}	$\hat{I}_{ac1}$
	Turn-on D4	Diode	U_{dc1}	$\hat{I}_{ac1}$

Table 4.10: Commutation events in the trapezoidal mode

In the triangular mode, two of the eight states do not exist: The states C and G, in the case where $U_{dc2} > U_{dc1}$ and A and E is $U_{dc1} > U_{dc2}$. This is shown in Figure (4.27) by the red arrow bypassing a state of the modulation. This means the switching events BC and FG do not exist. The switching losses in the triangular mode are only caused

on that side of the converter, where the DC voltage is smaller. Furthermore the losses are always caused by the two same switches. In the case where $U_{dc2} > U_{dc1}$ it is the pair of switches $T5$ and $T7$ (leading half-bridge) and in the case where $U_{dc1} > U_{dc2}$ it it the switch pair $T2$ and $T4$. The case where $U_{dc2} > U_{dc1}$ is shown in the Table (4.11). The losses are in any case of the triangular mode only on one side of the DC-DC converter. If the diode does not commutate quickly, additional turn-on losses from the corresponding power switch are caused, described in page 114.

Transition	Commutation	Seminconductor	U	I
AB	Turn-off T5	Switch	U_{dc2}	$\hat{I}_{ac2}$
	Turn-on D7	Diode	U_{dc2}	$\hat{I}_{ac2}$
EF	Turn-off T7	Switch	U_{dc2}	$\hat{I}_{ac2}$
	Turn-on D5	Diode	U_{dc2}	$\hat{I}_{ac2}$

Table 4.11: Commutation events in the triangular mode

Some future developments can reduce even more the losses from a DC-DC converter operated in the triangular/trapezoidal mode. The next Figure (4.28) shows a DC-DC converter particularly optimized for a low-power loss operation.

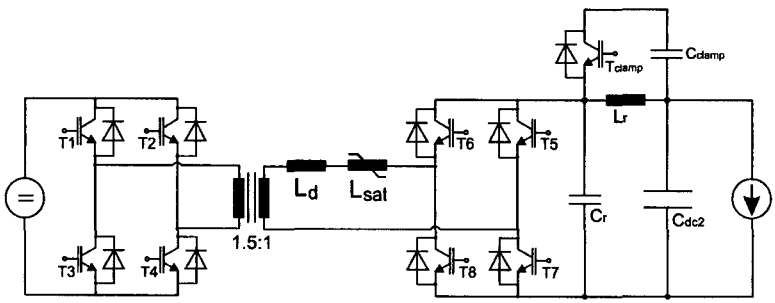

Figure 4.28: DC-DC converter with special features for the triangular/trapezoidal mode

The following observations have been done concerning the triangular/trapezoidal modulation method:

- The four switches $T1$, $T3$, $T6$ and $T8$ are never involved in any switching events. They are only causing conduction losses. Thus these switches need improved on-state characteristics. For the power switches this means a low saturation voltage for the on-state and for the diodes the forward voltage must be very small. Although these switches are only doing zero-current switching, these switches must still be relatively fast. The high switching frequency for the power semiconductors require a fast establishment of the low saturation values.
- The switch pair ($T2$, $T4$) and ($T5$, $T7$) are performing turn-off current switching. If the DC-DC converter is in the triangular mode, either only ($T2$, $T4$) will perform switching ($U_{dc1} > U_{dc2}$) or ($T5$, $T7$) will perform switching ($U_{dc2} > U_{dc1}$).

This switch pair inclusive the diodes must be very fast in order to have reduced commutation energies. For the case where only ($T5$, $T7$) are performing turn-off switching, the switches can be equipped with a turn-off snubber.

Due to the fact that the triangular current mode is the most efficient way to use the DC-DC converter in a hard-switched power-reversible mode, a DC-DC converter can be designed always working in the triangular mode, with a variable switching frequency f_p. The variable switching frequency is realized as follows: The states D and H of the modulator state machine shall have a fixed time value of τ_{blank}. All the other state times will be calculated in the same manner, as described in Equation (4.108). This means that if a low power is transferred, the switching frequency will be higher than the switching frequency with a high power transfer. Of course the lowest possible switching frequency must be fixed.

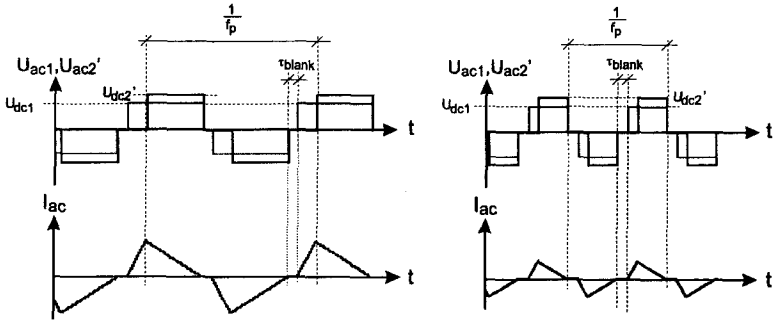

Figure 4.29: DC-DC converter in variable frequency mode

The advantage of the variable switching frequency is the fact that the power transfer behaves linear with the change of the phase shift δ. To stay always in the triangular mode and still be able to have to identical voltages U_{dc1} and U_{dc2} on both sides of the converter, a medium-frequency transformer with a winding ratio $w_r \neq 1$ must be taken. If a winding ratio of $w_r = 1.5 : 1$ is taken, the output voltage U_{dc2} can be around $\pm 25\%$ at the nominal value of the feeding voltage, without leaving the triangular current modulation. The fact that only the triangular modulation method is used makes the control and modulation algorithms easier to handle. The AC voltage referred to the primary side U'_{ac1} will be anyway bigger than U_{dc1}. In the Figure (4.29) the secondary side voltages U_{dc2} and U_{ac2} are referred to the primary side, so they are named U'_{dc2} and U'_{ac2}.

A last point to mention is that the switching losses are only caused on one half-bridge of the entire DC-DC converter. A additional inductor can put into the AC link, with the following behavior:

$$L_{sat} = \begin{cases} L_{sat} = L_{sat(norm)} & I_{ac} = 0 \\ L_{sat} = 0 & I_{ac} \neq 0 \end{cases} \tag{4.112}$$

This is the behavior of an inductor realized by a square loop core. The inductance is high at currents near zero and as soon as the current passes a certain threshold, the

inductance saturates and becomes immediately zero. This additional inductor with the described behavior can help the current turn-off when the current crosses zero, without causing any switching losses. The last point to be mentioned is the fact that the DC-DC converter will produce the only switching losses on two switches. This is assured by the use of the transformer and the fact that the converter will only work in the triangular mode. These two switches in the half bridge configuration could be realized by using high-speed elements such as Silicium Carbide (SiC) switches, which have optimized switching characteristics. But if the switches are ordinary power switches, they be supported in their turn-off operation by an active snubber technology like the salama turn-off snubber [39] or a auxiliary resonant commutated pole ARCP [40] or the resonant DC link RDCL [41].

Control using the combined modulation method

The control scheme implemented for the DC-DC converter in the combined triangular/trapezoidal modulation method is basically the same as been seen in Figure (4.18), page 118. The main difference is that the control system uses the inverse transfer function of the behavior of the DC-DC converter. This inverse transfer function allows to linearize the behavior of the PI controller operation. The reason for this design method is shown in this section. Three additional points must be respected in this control:

- The prediction value δ_2 calculated directly from the system perturbation values is now not only depending on U_{dc1} and I_{ch2}, but also on the output voltage U_{dc2}
- The system must calculate the desired current $\overline{I}_{dc2}$ and then must choose either the triangular or the trapezoidal modulation method to generate this current
- The trapezoidal and triangular mode have different modulation parameters depending on if U_{dc1} is bigger than U_{dc2} or not.

An algorithm is implemented in the control system to generate the appropriate modulation parameters. Ω_{d1} and Ω_{d2} are generated after a final value for δ is found. The overall schematics of the controller can be found in Figure (4.30). The converter consists of 8 different function blocks which are described on the next page.

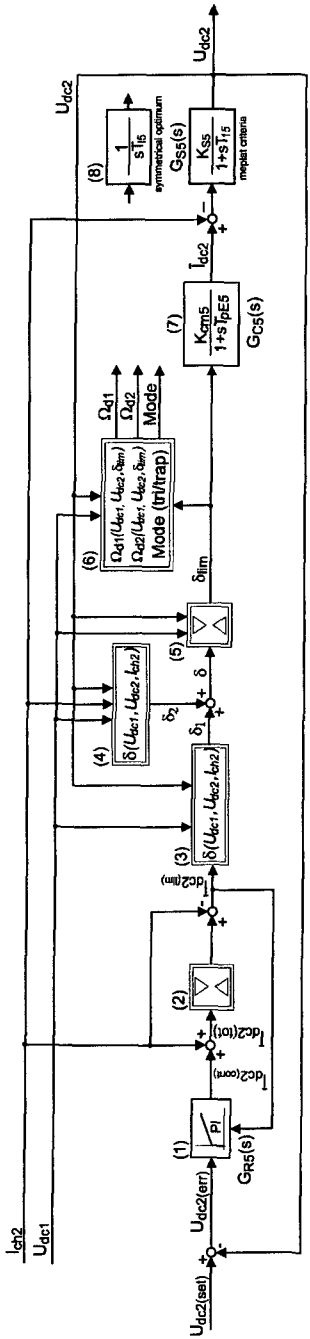

Figure 4.30: Overview of the triangular/trapezoidal control system

(1) The PI-controller is the same controller used for the rectangular mode shown in Figure (4.18), with an adaptive integral part K_{i5}. But this time the output value is not the phase-shift δ_1 but directly a desired current $\overline{I}_{dc2(a)}$.

(2) The limiter has a special function: First the current generated from the controller $\overline{I}_{dc2(cont)}$ is added to the load current I_{ch2}, resulting $\overline{I}_{dc2(tot)}$. This is an accurate value for the current, which will be generated by the converter. The current must be limited to a certain value in order to prevent too high currents destroying the semiconductors. After this, the load current I_{ch2} is subtracted from the controller current, with a resulting current $\overline{I}_{dc2(lim)}$

(3) This function blocks is the reverse transfer function of the signal delay function block $G_{cm5}(s)$. In this way the PI controller works always with a linear transfer function. This function block creates the correct value for δ, if the two DC voltages and the desired current is known. Of course these function blocks must make a difference between the two modulation methods. Each of the two function blocks generate a value for δ. δ_1 is the value coming from the controller generated by the error, while δ_2 is coming from the direct introduction of the perturbation values U_{dc1}, U_{dc2} and I_{ch2}.

(4) See in (3)

(5) The function block is a limiter. This limiter avoids that the calculated modulator parameters are out of the defined range. The maximal possible value for δ in the trapezoidal mode depends on the two voltages U_{dc1} and U_{dc2}. This was shown in Equation (4.56). The result of this function is the limited value δ_{lim}.

(6) The limited value of the phase-shift δ_{lim} enters this function block, where all the modulation parameters are calculated. This block is not in the closed loop of the control system, it only represents all the computing done in order to perform the modulation. First this block decides, whether to use the triangular or the trapezoidal modulation method. This is done by using Equation (4.55). After this, the remaining modulation parameters Ω_{d1} and Ω_{d2} are calculated.

(7) This function block contains the small time constants and the amplification between the phase-shift δ and the converter current $\overline{I}_{dc2}$.

(8) The last block is the small time constant transfer function with the two values K_{cm5} and T_{pE5}, resulting the generated current $\overline{I}_{dc2}$.

After a subtraction of the load current I_{ch2} from the converter current $\overline{I}_{dc2}$, the systems transfer function integrated the current differences and the output is the voltage U_{dc2}. The Table (4.12) shows the references to all the Equations which are used to perform the control of the DC-DC converter. These equations are particularly used by the function blocks (3), (4) and (6).

voltages mode	$U_{dc1} < U_{dc2}$ triangular	$U_{dc1} \geq U_{dc2}$ triangular	$U_{dc1} < U_{dc2}$ trapezoidal	$U_{dc1} \geq U_{dc2}$ trapezoidal
δ	Equation (4.81)	Equation (4.91)	Equation (4.66)	Equation (4.66) swap U_{dc1} with U_{dc2}
Ω_{d1}	Equation (4.77)	Equation (4.88)	Equation (4.57)	Equation (4.72)
Ω_{d2}	Equation (4.78)	Equation (4.89)	Equation (4.58)	Equation (4.73)

Table 4.12: All equations to calculate the parameters of the DC-DC converter

The next two Figures show the transfer function of the DC-DC converter in the combined triangular/trapezoidal mode. These Figures can be compared to the transfer function shown in Figure (4.17) of the rectangular modulation method. On the x-axis the phase-shift δ is represented, while on the y-axis the generated converter current $\overline{I}_{dc2}$ is visualized. The next variable parameter is the feeding voltage from a DC-link, U_{dc1}. The first Figure (4.31) shows the transfer function when the blanking time is small ($5\mu s$).

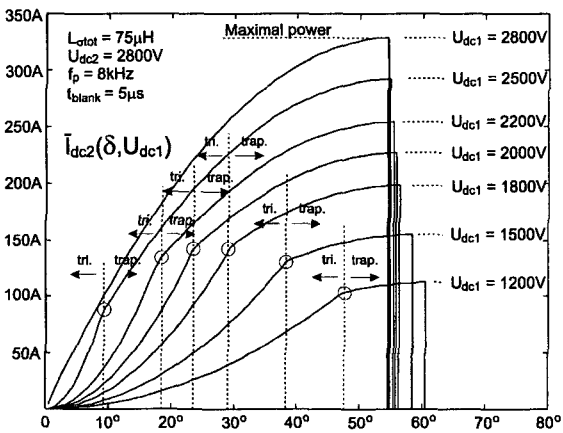

Figure 4.31: Transfer function of the DC-DC converter, small blanking time

The following Figure (4.32) shows the transfer function when the blanking time is rather high, even for high power switches ($10\mu s$).

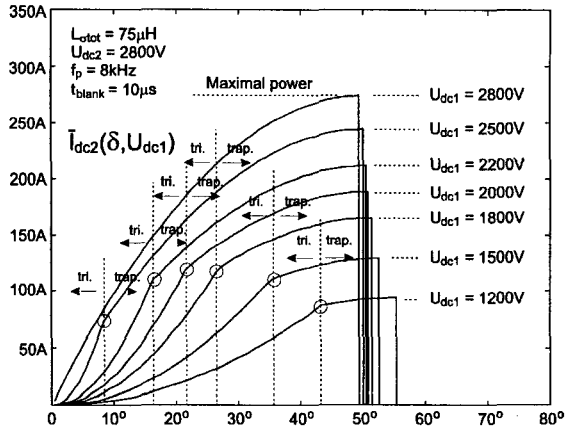

Figure 4.32: Transfer function of the DC-DC converter, big blanking time

The maximal power transfer of the DC-DC converter operating in the combined triangular/trapezoidal mode is depending on the ratio between the switching frequency f_p and the blanking time τ_{blank}. On the graphs it can also be observed that the maximal value for δ is variable with the voltage U_{dc1}. It can easily be seen that the transfer function is highly non-linear and depends not only on the two parameters U_{dc1} and δ, but also on the output voltage U_{dc2}. Depending on which modulation method is used, a different transfer function is used. Close to $\delta = 0$, the amplification factor for this transfer function can be nearly equal to zero if the triangular method is used. In order to avoid to linearize these graphs in an operation point, the inverse method is used. The input of the current PI controller is the error:

$$U_{dc2(err)} = U_{dc2(set)} - U_{dc2} \tag{4.113}$$

And the output is the current $\overline{I}_{dc2(cont)}$. For the rectangular mode, the controller output was the phase-shift δ, and the system parameters were linearized around and operating point. So the small time constant transfer function G_{cm5} sees a current as the input value, while the output is the generated current $\overline{I}_{dc2}$, generated with a small time delay T_{pE5}. So the amplification factor is:

$$K_{cm5} = 1 \tag{4.114}$$

All the over parameters for the controller are computed as shown before in the rectangular modulation method, 4.2.1, page 115. Also for this modulation type the adaptive integral part K_{i5} of the controller is implemented.
The combined modulation method has been implemented inclusive DC-DC converter and control in a MATLAB/SIMULINK model. The idea is to simulate the behavior of the DC-DC converter with the real power conditions for a multilevel converter. The following parameters have been used for the simulation:

U_{dc1}	2.5kVDC + 400VAC / 100Hz	Feeding voltage
$U_{dc2(nom)}$	2.8kV	Output voltage
$U_{dc2}\|_{t=0}$	500V	Output voltage initial condition
$P_{dc2(nom)}$	300kW	Nominal power
$L_{\sigma_{tot}}$	75μH	Decoupling inductance
C_{dc2}	750μF	Output capacitor
f_p	8kHz	switching frequency
$C_{d1} = C_{d2}$	200μF	Decoupling capacitor
T_{sample}	200μs	Sampling frequency
T_{r5}	80μs	Small time constants

Table 4.13: Numerical values for the simulated DC-DC converter

The load current I_{ch2} is a PWM current coming from the DC side of a four-quadrant converter. The 4Q-converter is modulated with a PWM modulation scheme. The parameters of the load current for this simulation is given in the Table (4.14):

I_{line}	200A	Effective line current
f_{line}	$33\frac{1}{3}$Hz	Line frequency
f_s	$166\frac{2}{3}$Hz	Switching frequency
k	0.98	Modulation degree PWM
α_c	0	Phase angle I_{line} to U_{line}
α_k	15^o	Phase angle U_{conv} to U_{line}

Table 4.14: Numerical values for 4Q-converter current

The control strategy for this DC-DC converter is to generate a current $\overline{I}_{dc2}$, which corresponds exactly to the time-variable value of the load current I_{ch2}. Some other control strategies for the DC-DC converter are presented in Section 5.1.2 on page 218. A number of observations can be done on the simulation results presented in the Figure (4.33). The simulation has been done with two perturbation values like the oscillating feeding voltage U_{dc1}, the PWM current as load I_{ch2}. The output voltage is controlled to 2.8kV and then is reduced to 1.9kV to see the performance on set value changes. Six points are marked with boxes on the simulation graphs shown in Figure (4.33).

(1) At this point, the output voltage U_{dc2} has the highest ripple due to a weak controller performance. The maximal deviation from the voltage set value is 55V, which corresponds to 2%. The amplitude of this oscillation occurs more or less proportional with the load current I_{ch2}. The main reason for this oscillation is the small time constant T_{pE5} of the system: even when there is a direct introduction of the perturbation value, the small time constant due to measurement, modulation and signal processing delays the generated current. This delay time causes the voltage oscillation. With a smaller time constant T_{pE5}, the voltage control performance would be better. Thanks to the adaptive integral part of the controller, there is no voltage overshoot when the set value $U_{dc2(set)}$ of the DC-DC converter is changed.

(2) The current $\overline{I}_{dc2}$ is limited to a maximal value of 330A. This is done by the limitation (2) in Figure (4.30). At this point it has to be mentioned that the turn-off currents $\hat{I}_{ac1}$ and $\hat{I}_{ac2}$ are flowing through the power semiconductors are important for the choice of the power switches.

(3) While charging the output capacitor C_{dc2}, the controller generates the maximal possible power so that the converter reaches as fast as possible the desired output voltage $U_{dc2(set)}$. That is why the phase-shift δ is limited to the maximal value δ_{max}. This limitation is done by the function block (5) of the Figure (4.30).

(4) The maximal value for δ is variable with the two DC voltage U_{dc1} and U_{dc2}. In every sampling period, the two voltages are measured and the new value for δ_{lim} is calculated.

(5) The two remaining modulation parameters Ω_{d1} and Ω_{d2} are calculated. A sudden change from the trapezoidal mode to the triangular mode is shown, due to the measured current I_{ch2} going immediately to zero. If the two voltages U_{dc1} and U_{dc2} are the same, the two parameters Ω_{d1} and Ω_{d2} are equal.

(6) The last observation is done on the set value change for the voltage U_{dc2}. In order to lower the voltage on the output capacitor C_{dc2}, the converter current $\overline{I}_{dc2}$ is negative. This shows the reversibility of the power in this DC-DC converter.

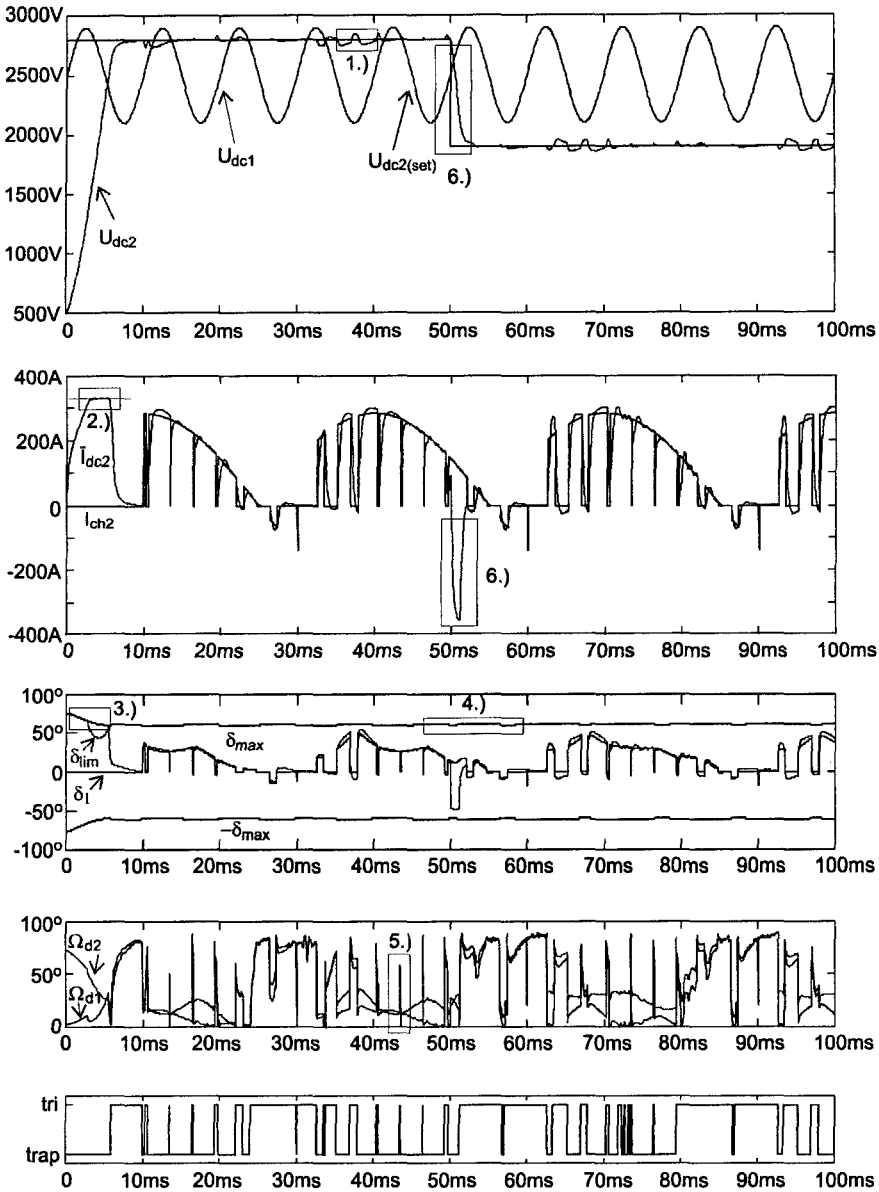

Figure 4.33: Simulation results on the simulated 300kW DC-DC converter

To complete the simulation results, a Fourier analysis or FFT analysis of the controlled output voltage U_{dc2} is computed and discussed, without any change of the voltage set value. In the multilevel application, the output voltage U_{dc2} is the feeding voltage for the 4Q-converters. So all the harmonics generated by the DC-DC converter will be seen afterwards on the line voltage U_{line} and so they will also be visible on the line current I_{line}. The simulations are done with a DC-DC converter the same parameters as been seen in the Table (4.13), with exception of the decoupling inductance $L_{\sigma tot}$ and the output capacitor C_{dc2}, which have been chosen as follows:

component	converter A	converter B
$L_{\sigma tot}$	75μH	50μH
C_{dc2}	750μF	500μF

Table 4.15: Two different DC-DC converter components

The load current I_{ch2} is coming from a typical four-quadrant converter, the same as used in the multilevel converter. The parameters used to simulate the four quadrant converter are shown in the Table (4.14). The simulation for the DC-DC converter A is shown in the Figure (4.34). The highest harmonic peak can be found at the frequency of $333\frac{1}{3}$Hz, which the resulting switching frequency from a four-quadrant converter $2 \cdot f_s$. But of course the PWM modulation generates a large spectrum of harmonics on the DC voltage due to the variable length of the pulses. The closed-loop transfer function of the DC-DC converter has a variable resonant frequency. This is due to the fact that an adaptive parameter is used, namely the integral amplification K_{i5} and of course the use of the inverse control method, where the system is linearized. Another frequency found on the DC voltage U_{dc2} is twice the line frequency. A peak at $33\frac{1}{3}$Hz can be seen coming from the sliding average value of the current I_{ch2}. The simulation have shown that there is no influence on the perturbation of the feeding voltages U_{dc1} to the secondary controlled voltage U_{dc2}. If the system is simulated with the superposed perturbation voltage on U_{dc1} (that has a frequency of 100Hz and an amplitude of 400V) and is compared with a perfectly stabilized DC voltage U_{dc1}, there is no difference in the analyzed harmonics.

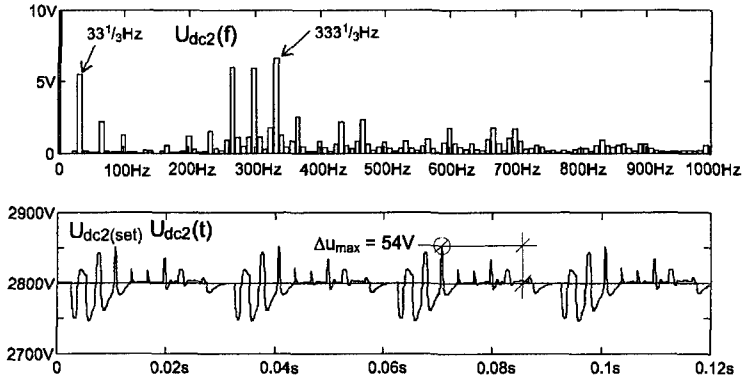

Figure 4.34: FFT on output voltage U_{dc2} of the DC-DC converter A

In order to save costs, a smaller output capacitor C_{dc2} has been chosen and the overall decoupling inductance $L_{\sigma tot}$ has been reduced. The low-order harmonics on the DC voltage U_{dc2} are remaining the same, but the amplitudes of the switching frequency harmonics are inverse-proportional to the output capacitor C_{dc2}.

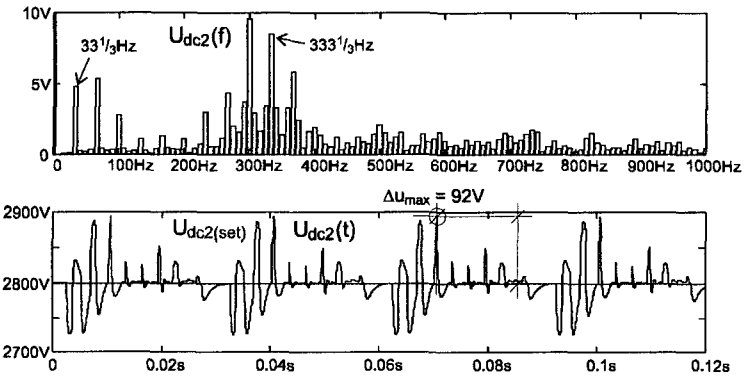

Figure 4.35: FFT on output voltage U_{dc2} of the DC-DC converter B

4.2.3 Design for multilevel converters

The proposed DC-DC converter is designed to feed four-quadrant converters, used in a multilevel configuration. In this section, some equations are developed, which are useful to design the parameters of the DC-DC converter but also to estimate the losses of a multilevel converter working in with n DC-DC converters feeding the four-quadrant converters. It is assumed that all the multilevel converter values on the line side are sinusoidal and that the line current I_{line} and the line voltage U_{line} are in phase. The

relations are shown in Figure (2.37), page 42. In this way, the trigonometric monophasor relationships can be used. For the multilevel converter output voltage it can be found:

$$U_{conv} = \sqrt{U_{line}^2 + (2\pi f_{line} L_{line} I_{line})^2} \tag{4.115}$$

The phase shift angle α_k between U_{conv} and I_{line} is:

$$\alpha_k = arctan\left(\frac{2\pi f_{line} I_{line} I_{line}}{U_{line}}\right) \tag{4.116}$$

The number of multilevel converter steps is well-known and in this way an average DC load current $\overline{I}_{ch2}$ for a period on the DC-DC converter secondary side is calculated:

$$\overline{I}_{dc2} = \overline{I}_{ch2} = \frac{\sqrt{2} P_{mot} k cos(\alpha_k)}{2U_{line}} = \frac{P_{mot}}{n \cdot U_{dc2}} \tag{4.117}$$

The modulation degree k is the global modulation degree, used for every 4Q-converter.

$$k = \frac{\widehat{U}_{conv}}{n \cdot U_{dc2}} = \frac{\sqrt{2U_{line}^4 + 8(\pi f_{line} L_{line} P_{mot})^2}}{n U_{dc2} U_{line}} \tag{4.118}$$

All the n steps of the multilevel converter are supposed to be active. The average current switched in the DC-DC converter is higher than the delivered output DC current $\overline{I}_{dc2}$. This is due to the fact that the AC current peak $\widehat{I}_{ac1}$, $\widehat{I}_{ac2}$ generated by the modulation method is turned off and that a negative DC current $\overline{I}_{dc2}$ is also switched. Negative currents are usual in the period of the line frequency f_{line}, due to the phase-shift between the converter voltage $U_{conv(i)}$ and the line current I_{line}. This can be seen in the simulation (4.33), where the phase-shift is relatively high. The next expression gives the absolute average DC current value entering the DC-DC converter:

$$\overline{I}_{dc2(abs)} = \widehat{I}_{line} k |sin(2\pi f_{line} + \alpha_k)| sin(2\pi f_{line}) \tag{4.119}$$

The Equation in (4.119) is evaluated using trigonometric relations. The result is:

$$\overline{I}_{dc2(abs)} = \frac{\widehat{I}_{line} k \pi sin(\alpha_k)}{2\alpha_k(\pi - \alpha_k)} \tag{4.120}$$

With this Equation, the average absolute power transfer of a DC-DC converter per line period $\frac{1}{f_{line}}$ can be evaluated. The average absolute power is certainly higher than the effective transferred power P_{dc2}. The negative and the positive currents are both counted as loss currents. For each modulation method, the average turn-off current must be calculated. This value for the turn-off currents depends especially on the decoupling inductance $L_{\sigma tot}$: The smaller the inductance is chosen, the smaller are the phase-shift values for δ doing the same power transmission. Thus, the lower is the part of reactive power. The turn-off currents are given in Equation (4.18) and (4.19) for the rectangular modulation method, but this time the phase-shift delta is replaced by the absolute average value $\overline{\delta}_{abs}$:

$$\hat{I}_{ac1(abs)} = \frac{U_{dc1}\pi U_{dc2}(2|\overline{\delta}_{abs}| - \pi)}{4\pi f_p L_{\sigma tot}} \tag{4.121}$$

$$\hat{I}_{ac2(abs)} = \frac{U_{dc1}(2|\overline{\delta}_{abs}| - \pi)U_{dc2}\pi}{4\pi f_p L_{\sigma tot}} \tag{4.122}$$

For the combined triangular/trapezoidal modulation, the turn-off currents were expressed in Equation (4.60) and (4.61):

$$\hat{I}_{ac1(abs)} = \frac{U_{dc2}(|\overline{\delta}_{abs}| - \Omega_{d2} + \Omega_{d1})}{2L_{\sigma tot}\pi f_p} \tag{4.123}$$

$$\hat{I}_{ac2(abs)} = \frac{U_{dc1}(|\overline{\delta}_{abs}| - \Omega_{d1} + \Omega_{d2})}{2L_{\sigma tot}\pi f_p} \tag{4.124}$$

These last expressions give the peak currents in the AC-link of the DC-DC converter. This current now depends obviously on the average absolute phase shift value $\overline{\delta}_{abs}$. From the power transfer Equations for P_{dc2}, this value is found for the rectangular modulation method:

$$\overline{\delta}_{abs} = \frac{\pi}{2}\frac{U_{dc1} - \sqrt{U_{dc1}^2 - 8U_{dc1}L_{\sigma tot}f_p\overline{I}_{dc2(abs)}}}{U_{dc1}} \tag{4.125}$$

For the combined modulation method, the Equation (4.81) for the triangular mode and Equation (4.66) for the prediction of δ can be used for the trapezoidal mode. First it has to be found out if the absolute average current $\overline{I}_{dc2(abs)}$ demanding the triangular or in the trapezoidal mode, and which DC voltage U_{dc1} or U_{dc2} is higher.

4.3 Medium frequency transformer

The described DC-DC converter needs a special type of transformers, which should fulfill special technical characteristics. Off the shelf solutions cannot be taken, due to the fact that the standard transformers are usually made for DC-DC converters with a winding ratio different from 1 and the potential of the output voltage does not change rapidly. The insulation between primary and secondary side must withstand very high voltages. It must be mentioned that typical currents for classical DC-DC converter applications are sinusoidal (resonant topologies), while the proposed DC-DC converter contains currents of special waveforms (triangular, trapezoidal) with high-frequency contents.
New transformer designs were searched by using the latest ideas for the transformer winding and magnetic core material. Instead of using the traditional ferrites with a limited flux density at $0.3T - 0.4T$ and limited size, the new amorphous core material has been taken for the design and has been tested. Several manufacturers offer those new core types allowing a high magnetic flux density of $1.56T$. One of the main goals for the multilevel converter is the reduction of the weight. So this goal is consequently pursued for the transformer design as well as the transformer is one of the weight-critical elements in the entire converter system. For the transformer design the general rule can be used:

$$weight \sim power \sim f_p \cdot B_{max} \tag{4.126}$$

Due to high losses the switching frequency f_p cannot be increased infinitely, but some improvement can be expected from the magnetic core material. Very often, the available medium-frequency transformers have the following characteristics:

- Stray inductance should be very weak. Especially for resonant DC-DC converters or for a direct coupling of the transformer to a rectifier bridge on the secondary side, very low stray inductance is required (below $1\mu H$ for 20kW/20kHz).
- High coupling capacity between primary and secondary side of the transformer. In normal DC-DC converter applications, the designer does not pay much attention to the coupling capacity. Coupling capacities above $200pF$ for converters (20kW/20kHz) are usual.
- Non-symmetrical design of the transformer. Transformers are mostly designed with winding ratio not equal to 1 and have in this way unsymmetrical behavior (different characteristics like stray inductance, parasitic resistance on primary and secondary side). The transformers are designed for a power flow only in one direction.
- The voltage isolation from primary to secondary side is limited to 2-3kV. This is due to the fact that in most applications the output voltage potential is not changing rapidly.
- No particular design to support high-frequency currents. The transformers in the high power range are designed for sinusoidal resonant currents with no high-frequency contents.

A transformer for the multilevel has different needs. These are especially adapted to the presented DC-DC converter topology with the decoupling inductance:

- The stray inductance has to be high. The inductance is needed for a decoupling of the medium-frequency AC voltages. The AC link with the transformer needs a inductive behavior (around $50\mu H$ for 20kW/20kHz). The decoupling allows the generation of the phase-shift between the two AC voltages.
- Very low coupling capacity between primary and secondary side. Due to the fact that the secondary side potential is always changing by the use of the PWM or step modulation method, capacitive coupling currents must be avoided. Coupling capacities below $50pF$ for converters (20kW/20kHz) should be achieved.
- The transformer should be designed symmetrically. The transformer is operating entirely symmetric with the reversible power possibilities. A symmetrical design (Stray inductance, decoupling capacitors) advantages the symmetrical operation.
- Very high voltage isolation between primary and secondary side. The transformer has to support in the worst case at least the voltage resulting of the addition of all possible step voltages.
- The transformer windings must be capable to withstand high-frequency currents.

To meet these design criteria, two different transformers are proposed optimized for the proposed DC-DC converter. Some transformers and inductors where designed in the framework of this thesis, for medium-frequency applications. The most efficient design method is the method using the area product A_P between the effective core cross-section (magnetic material) A_C and the winding area of the core (The core window), namely W_a. This product gives an idea of the overall power, that a transformer can support. This design method is supported by the most core manufacturers and is described in details in [42].

4.3.1 Coaxial transformer

Many different types of coaxial transformers have already been realized for DC-DC converters in the medium power range working with a medium switching frequency (from 8kHz to 50kHz). Some of them are used in resonant converters like the examples [43] and [20], others are used for hard-switched topologies [37].
The working principle of a coaxial transformer is very simple: A coaxial cable is chosen, which has already two galvanic insulated conductors inside. This cable is now wound around a magnetic core. Of course the magnetic loop must be closed (ring core or a cut core, which is put together). By taking the two ends of the coaxial cable, four connections to the cable can be done: The pair of the two interior cables are belonging together and can be used as the primary side. So the two exterior conductors of the coaxial cable are the secondary AC connector. For the experimental results of the DC-DC converter presented in Section 4.5, a coaxial transformer has been realized. The used coaxial transformer is shown in the Figure (4.36).

The advantages of a coaxial transformer concept for the presented application types are:

- Easy construction principle with an off-the-shelf telecommunications coaxial cable and any kind of cores (cut-cores or uncut cores are possible)

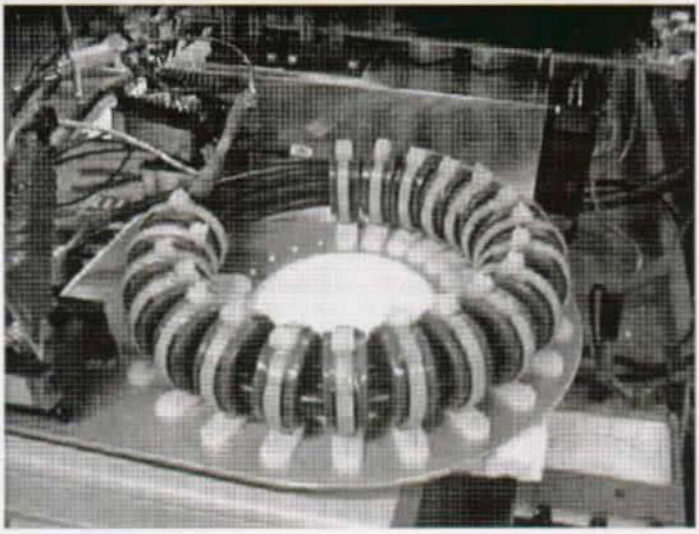

Figure 4.36: Coaxial transformer for designed for 20kVA

- Coaxial cables are a well-known technology by many manufacturers concerning the insulation possibilities. So a very high voltage insulation is possible between the primary and the secondary side of the transformer
- The coaxial transformer can easily be cooled by a water cooling system inside the internal coaxial conductor. This kind of cooling will allows very high current densities (up to $20\frac{A}{mm^2}$)
- Due to the distribution of the current in the coaxial cable, high current densities can be tolerated. There are no problems with the skin effect.
- The magnetizing current can be measured very easily. Only a current probe must be put around the coaxial cable (which contains the primary and the secondary side windings). This can be helpful for several applications

The coaxial transformer has some disadvantages, especially in the multilevel application field. The disadvantages are:

- The coaxial cables for high voltage insulation have a high minimal bending radius. This fact does not allow the construction of a very compact medium-frequency transformer. Also the window area W_a of the cores is very badly used (low fill-factor). The insulation material around every single winding takes a lot of space.
- The capacitive coupling between the primary and secondary side C_{tr} is relatively high. In a multilevel application, high capacitive currents would be generated when the voltage potentials change.

- There is no possibility to integrate a high decoupling inductance directly to the transformer.

- It is difficult to have a different winding ratio w_r than 1. The publication [43] shows a possibility, but the manufacturing of that type of transformer is very expensive.

A transformer has been designed for a power of 20kVA, to be used for the proposed DC-DC converter. The design procedure is shown in Appendix A.4. It consists of an aluminum support base, where ring cores where fixed on with plastic tube holders. The used ring cores are not cut and they where fabricated by Vacuumschmelze, the core material is Vitrovac 500F. These cores tolerate a maximal magentic flux density of $1.2T$. Twenty of those cores are used to create the necessary magnetic area A_c , details can be seen in [42] and in the Appendix A.4. The coaxial cable used is a standard 75Ω coaxial cable for telecommunication needs, with high voltage insulation. As to be seen in Figure (4.36), the minimal bending angle of the coaxial cable did impose the entire size of the transformer. The Figure (4.37) shows a cut view of the transformer through a magnetic core. While the magnetic field is circulating in the core in the direction of φ, the electrical field has only a radial component and stays inside the coaxial insulation material.

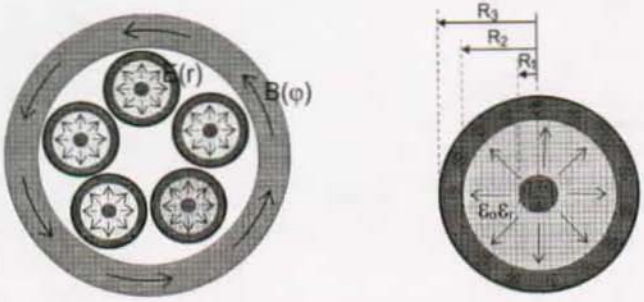

Figure 4.37: Cut of a coaxial transformer with 5 turns

The transformer parameters are measured and are given in the Table (4.17):

Feeding voltage	$U_{dc1(nom)}$, $U_{dc2(nom)}$	500V
Output current	$I_{dc2(nom)}$	40A
Output power	P_{dc2}	20kVA
Number of windings	N_1, N_2	5
Winding resistance	R_{p1}, R_{p2}	15mΩ
Natural stray inductance	$L_{\sigma 1}$, $L_{\sigma 2}$	3.1μH
Principle inductance	L_p	7mH
Coupling capacity	C_{tr}	310pF
Inner conductor radius	R_1	1.64mm
Outer conductor radius	R_2	5.75mm
Outer radius	R_3	5.93mm
Chosen current density	J	$7\frac{A}{mm^2}$
Insulation material	ε_r	2.3 (Polyethylen)
Fill factor	K_u	0.0595
Weight (without external inductors)		2.7kg
Weight of cores		1.66kg

Table 4.16: Parameters of the realized coaxial transformer

The effective conduction cross-section of the coaxial cable is $8.45mm^2$ for the inner conductor and $6.51mm^2$ for the outer one. There are only five turns, so the fill factor is not very high. The capacitor between the primary and secondary winding of a coaxial transformer is only determined by the geometry of the cable. As to be seen in Appendix A.5, the electrical field is only inside the cable. So the capacitance per meter of coaxial cable is:

$$C'_{tr} = \frac{2\pi\varepsilon_o\varepsilon_r}{ln(\frac{R_2}{R_1})} \tag{4.127}$$

The same can be said for the stray inductance. Of course there is also a stray inductance effect between the cables wound inside the ring cores. But this effect can be neglected.

$$L'_{\sigma 1,2} = \frac{\mu_o}{2\pi}\left[ln\left(\frac{R_2}{R_1}\right) + \frac{{R_3}^2}{2({R_3}^2 - {R_2}^2)} + \frac{{R_3}^2}{({R_3}^2 - {R_2}^2)^2} ln\left(\frac{R_3}{R_2}\right)\right] \tag{4.128}$$

The resistance per meter can be calculated by regarding the conduction cross-sections of the given coaxial cable.

4.3.2 Planar transformer with integrated decoupling inductances

A special planar transformer has been designed for the proposed DC-DC converter. The transformer windings in the planar technology are not like in other transformers made of cables, but the windings are directly integrated as circular planar tracks onto a printed circuit board (PCB), to be seen in [44]. The PCB are usually realized in a double-faced technology: A relatively thin epoxy carrier material of the printed circuit board is used as insulation material between the windings on the top side and on the bottom side of the PCB. Depending on the application, only two or more windings can be placed on

the PCB. The windings on the top side of the PCB are connected through a conduction bridge traversing the PCB with the windings on the bottom side. The input/output connection holes for the winding are placed on an extremity of the PCB. These must be placed in a way that allows an easy connection. The planar PCB windings are presented in the Figure (4.38).

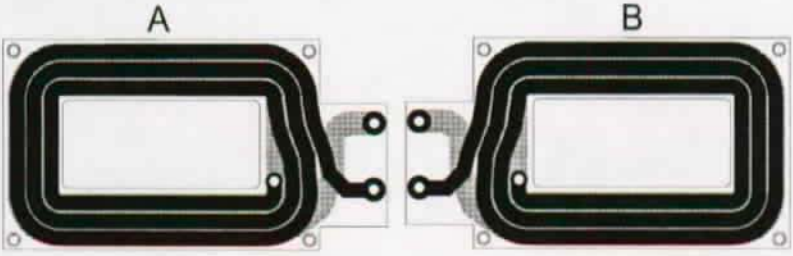

Figure 4.38: Two PCBs for the windings in the planar transformer

Of course the tracks on the PCB are not very thick (about 100μm) so they have the advantage to tolerate currents up to high frequencies without showing a significant rise in resistive losses due to the skin effect. But only with one PCB, only very few current can flow through the transformer. In order to allow more current through the planar windings, many of those PCBs are manufactured and they are stacked. All the stacked PCBs are afterwards connected together by the connection holes, therefore all the windings are in parallel. It depends on the window size W_a of the magnetical core how many winding-PCBs can be stacked together. This method will not rise the number of windings, only the conduction surface is multiplied and the transformer will handle higher currents.
In order to avoid an additional insulation film between each planar winding PCB, two different types of planar winding PCBs must be manufactured, shown already in the Figure (4.38): The type B is the mirrored version of the type A. In this way the PCB can be stacked without any additional insulation layer. The manufacturer only must pay attention to place the corresponding sides of the PCBs together. The realized planar transformer is shown in the Figures (4.41).

Advantages:

- The planar transformer can easily be manufactured in high quantities, due to the possibility of creating parallel winding stacks with the printed circuit boards (PCB).
- Very high fill factors of the conducting material can be achieved with a planar concept (Fill factors K_u up to 0.25 depending on the insulation capabilities).
- The planar transformer can be realized in a very compact size, allowing a maximal reduction of the transformer weight.
- Any kind of winding ratio can be realized, it is even possible to connect to the middle point of a transformer winding.
- Integration of the decoupling inductor L_d, shown later in this section.

Disadvantages:

- The planar transformers must use cut cores, because the windings are pre-fabricated on the circuit boards. Uncut cores cannot be put around the PCB windings. This means that the planar transformer usually will have lower main inductances.
- Many circuit boards must be put in parallel if a high current has to be achieved. This will rise the costs of the planar transformer.
- The planar transformer concept is difficult to cool actively. It is not very efficient to cool around PCBs, while the current conducting material is inside the epoxy-boards of the PCB.
- Due to the edges of the copper on the PCBs, many precautions have to be taken into account for a high-voltage design. The copper edges can create high electrical field densities and so the transformer insulation can be destroyed more easily. Anyway there are very few publications describing planar transformers working in a high-voltage environment.

Many planar transformers have been realized and are sold in high quantities for low-power applications. Several manufacturers offer planar transformers for the power range up to 10kVA. These planar transformers operate very well for normal DC-DC converter applications. They are especially usable for designs where the switching frequency is very high, because of the very small current conduction sections of the individual PCBs. But for a multilevel application they are not suitable. The main problem is that they are not designed for a high-voltage insulation, but they coupling capacitance C_{tr} between primary and secondary side is very high. The Figure (4.39) shows the typical used planar transformer.

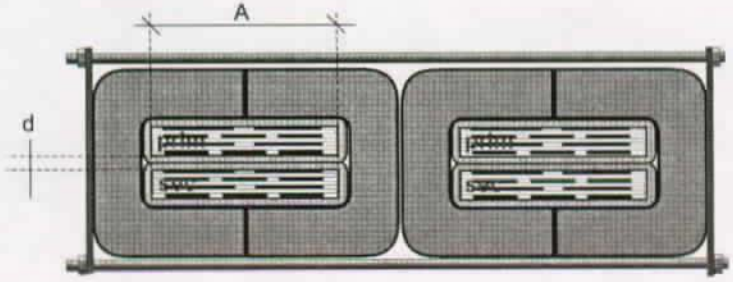

Figure 4.39: Side cut of a conventional planar transformer

The coupling capacitance depends on two factors: The distance d between the primary and the secondary side PCB stack and the surface A of the PCB tracks on the primary side, which is covered by the PCB tracks on the secondary side. It can be seen in Figure (4.39) that the surface of the PCB is very big. The core material is oriented in a way making the surface of a PCB maximal. The entire surface of the PCB windings is covered by the PCB on the secondary side. This is the usual way to manufacture the planar

transformers, because by doing this construction type the stray inductances become very small (very large conductors in a planar construction have very few inductivity, smaller than 1μH for 10kVA). But the designed DC-DC converter has the inverse needs. Big stray inductances and a small coupling capacitance. The proposed construction type for the DC-DC converter is shown in the Figure (4.40) and solves these problems:

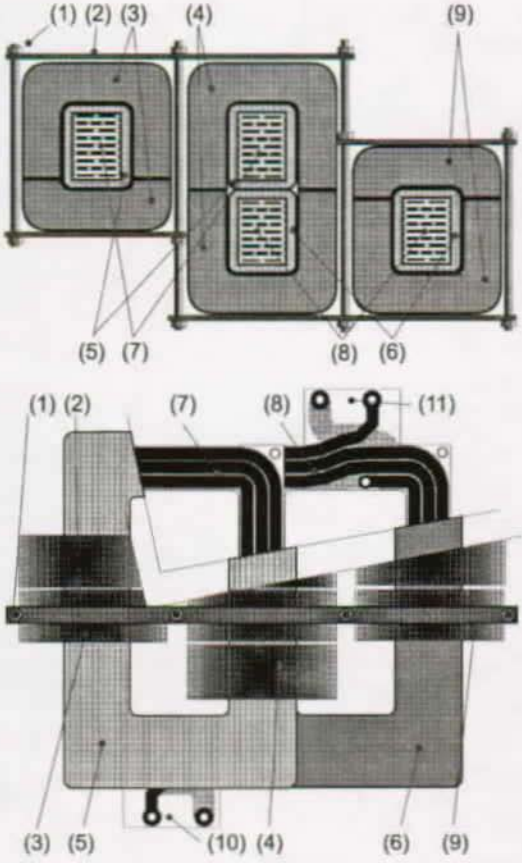

Figure 4.40: Side cut of the realized planar transformer

The idea to reduce the coupling capacitor C_{tr} is done by minimizing the surface A. This is done in two ways:
The surface of one fabricated PCB with the transformer turns shall be small. By orienting the PCBs inside the magnetic cores not for the long side (like shown in the Figure (4.39) to reduce the stray inducance) but for the short side (seen in Figure (4.40) for the same C-core size), this surface is of course reduce, but more PCBs must be fabricated to fill up the window area of the core. The copper window utilization factor K_u will remain

more or less the same, but the stray inductance is certainly higher. In the proposed application, more stray inductance is required.
The next improvement is done by the orientation of the two winding groups inside the transformer. Instead of aligning the two groups on each other in the transformer, which gives a maximal covering of the two PCB surfaces (shown in Figure (4.39)), only one side of the rectangular PCB stack is aligned. This reduces the covering surface A, seen in Figure (4.40). Only the aligned side of the rectangular PCB stacks are enclosed by the cores for the transformer.
The fact that each one side of the primary and secondary side PCB stack are not covering each other can be used to integrate additional decoupling inductances L_{d1} and L_{d2} on both sides. To do this, the opening surface of a rectangular PCB stack must be high enough to introduce the additional cores. The cut of the transformer shows the two cores for the additional inductors and the main transformer cores. The numbers given on the Image (4.40) are described below:

(1) Fixing poles with nuts to screw the magnetic cores together. The nuts must be tighten strongly for a good connection between the two C-core parts.

(2) Aluminum bars to tighten the cores together. Between the aluminum bar and the core there is a plastic plate to avoid a direct contact.

(3) C-cores for the primary side decoupling inductor. They are cut to a smaller shape in order to reduce weight. The cores give the magnetic path for the integrated decoupling inductors and only enclose either a primary or a secondary side winding stack.

(4) Large sized C-cores for the principle inductance of the transformer. The cores enclose both primary and secondary side PCB winding stacks.

(5) High-voltage insulation material for the primary side winding stack. The stack is moulded into the insulation material.

(6) High-voltage insulation material for the secondary side.

(7) Primary side PCB winding stack.

(8) Secondary side PCB winding stack.

(9) C-cores for the primary side decoupling inductor.

(10) Connections for the AC voltage on the primary side.

(11) Connections for the AC voltage on the secondary side.

The transformer was realized using four C-core pairs for the principle transformer inductance and each two C-core pairs for the inductors L_{d1} and L_{d2}. The same core types were used for the inductor and the transformer, with the same magnetic cross section A_C per core. But the cores for the inductors were adapted to the reduction of the used window area and were cut. This action is only done to reduce the weight of the transformer. If both cores for the inductors L_{d1}, L_{d2} and main transformer inductance L_p are the same and there is no air gap, the principle inductance would only be the same

value as the two decoupling inductances together L_d. Altogether there are four cores for both magnetic paths with the same number of turns. The principle inductance must be much higher than the decoupling inductors, as been seen in Equation (4.2), page 102. So either an air gap is introduced for the cores of the decoupling inductors (around 1mm) reducing the inductivity and rising the maximal saturation current $\hat{I}_{ac}$, or another core material is used with a smaller value for μ_r, like some ferrite type. In this application, an air gap is made between the two C-cores of the inductor.
The realized planar transformer is using cut C-cores from Allied signal, called Metglas Powerlite C-cores, AMCC-50. Theses cores have a relatively high magnetic saturation density of 1.5T and very big cores are available for medium and high power transformer designs. The same cores where cut in order to reduce weight for the additional stray inductances, which enclose each the primary and the secondary side windings.

Feeding voltage	$U_{dc1(nom)}$, $U_{dc2(nom)}$	600V
Output current	$\overline{I}_{dc2(nom)}$	> 50A
Output power	P_{dc2}	30kVA
Number of windings	N_1, N_2	5
Winding resistance	R_{p1}, R_{p2}	5mΩ
Natural stray inductance	$L_{\sigma 1}$, $L_{\sigma 2}$	1.2μH
Integrated decoupling inductance	L_{d1}, L_{d2}	33μH
Maximal inductor current	$\hat{I}_{ac}$	180A
Principle inductance	L_p	250μH
Coupling capacity	C_{tr}	35pF
Conductor width		2.3mm
Conductor thickness		100μm
Epoxy thickness		200μm
Number of parallel PCB		70
Chosen current density	J	$10\frac{A}{mm^2}$
Fill factor	K_u	0.115
Weight		4.6kg

Table 4.17: Parameters of the realized coaxial transformer

It is not surprising to see that this planar concept has better electrical performance values compared to the coaxial transformer: Twice the fill factor and especially ten times smaller coupling capacitor. The effective cross-section conducting the current I_{ac} is $16.1mm^2$. Theoretically this transformer can be rated twice the current compared to the coaxial transformer. To start the design of a planar transformer, the thickness of the copper tracks must be chosen. These must be calculated using the skin effect Equation (4.129):

$$\delta_{skin} = \sqrt{\frac{2}{\omega_p \mu_r \mu_0 \sigma_R}} \tag{4.129}$$

The conductor is made of copper tracks with the conductivity σ_R and the relative permeability of copper $\mu_r = 1$. If for the frequency the value $f_p = 20$kHz is chosen, the penetration depth of the current is δ_{skin} is 0.45mm. But the current of the modulation

methods is not sinusoidal and has a lot of harmonic contents. That is why the thickness of 100μm for the tracks is taken. Due to the PCB stacking with the mirrored PCB neighbor, the tracks of the next PCB will exactly cover the tracks of the first one. So the effective thickness of the tracks will be doubled. Instead of 100μm the tracks will be 200μm thick.
The next images presented in Figure (4.41) show the assembled stacks for the primary and the secondary side. Four C-cores are used for the principle inductance, while each two C-cores are used for the decoupling inductance (additional stray inductance).

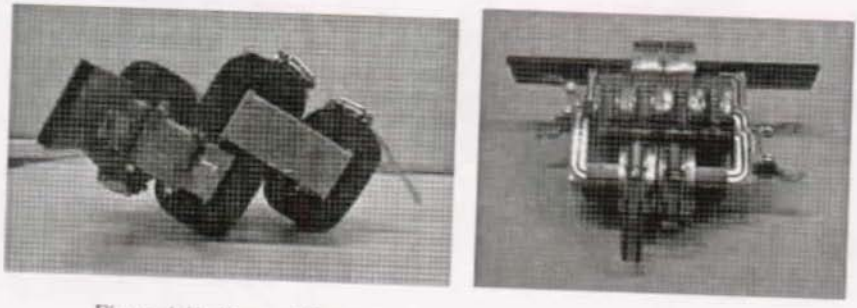

Figure 4.41: Top and front view of the realized planar transformer

One of PCB winding is photographed from both sides and shown in Figure (4.42). The tracks are not very large, but many of these PCBs are stacked, so the conducting surface is still sufficient. By using these relatively small PCB stripes with narrow windings, the incredibly low coupling capacitance C_{tr} of 35pF could be achieved.

Figure 4.42: Back and front side of a planar transformer winding

4.4 Experimental results for the rectangular mode

The first experimental results have been done on a low-power prototype, allowing several non-destructive tests on the AC link current like saturation effects and AC link resonance. The prototype was designed for an transferred power of about 100W and is based on power MOSFET semiconductors. Like in the prototype for the single-phase and three-phase multilevel converter, all the control algorithms were implemented on a PC equipped with several IO cards like AD converter, fiber-optical signal output card for power semiconductor firing signals and of course a modulator card containing a complex gate array to implement the modulator state machine. The PC can send digital values to the gate array. In this application, the value sent to the gate array is the phase-shift δ, a stop flag and the power flow direction. The parameters of the experimental setup are given in the Table (4.18):

Parameter	Symbol	Value
Feeding voltage	U_{dc1}	50V + variable AC
Nominal output voltage	$U_{dc2(nom)}$	50V
Nominal output current	$\overline{I}_{dc2}$	2A
Load current	I_{ch2}	variable AC
Switching frequency	f_p	19.5kHz
Power MOSFET	$U_{ds_{max}}, I_{d_{max}}$	200V,10A
Max. DC current	$I_{dc1_{max}}$	3A
Input capacitor	C_{dc1}	680μF
Output capacitor	C_{dc2}	680μF
Decoupling inductor	L_d	160μH
Decoupling capacitor	C_{d1}, C_{d2}	40μF / 25V
Blanking time	τ_{blank}	750ns
Sampling period	T_{sample}	200μs

Table 4.18: Realized DC-DC converter for 100W

Exactly the same parameters were used to simulate the system with the rectangular mode, shown in Figure (4.19), page 120. The feeding voltage U_{dc1} was generated by an voltage amplifier source. So by using a frequency generator, a set value can be generated for the voltage amplifier, in order to produce a non-ideal feeding source. The load on the secondary side of the converter was a bipolar current amplifier, which was able to generate any kind of current waveforms between $-1A$ and $1A$. Negative currents can be injected to test the negative power transfer with the DC-DC converter. The bipolar current amplifier sign value came also from a frequency generator. The first measurements can be seen in Figure (4.43):

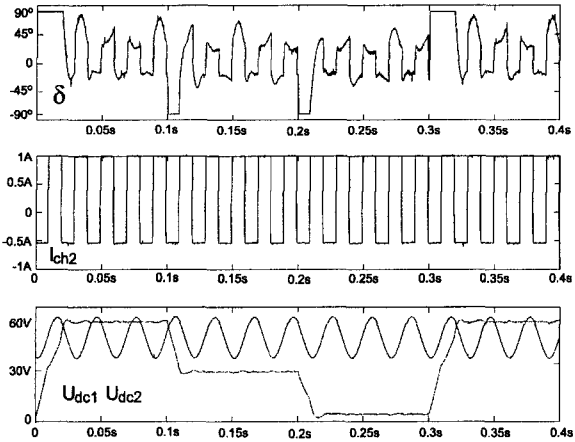

Figure 4.43: Measurements with the same parameters as in the simulation

The measurement in Figure (4.44) shows exactly the same result as the graphs achieved with the simulation in Figure (4.19), page 120. The measurements have been done by the AD-converter card of the PC. The load current I_{ch2} is a rectangular current using the two-quadrant possibilities of the DC-DC converter. When there is a negative current, the phase-shift δ is also negative. The fundamental frequency of the current is 50Hz. The voltage oscillation superposed on the DC value of U_{dc1} has a frequency of $33\frac{1}{3}$Hz with an amplitude of 15V. The output voltage changes its set value to show the controller performance. It can be seen that the output voltage is well stabilized. The maximal overshoot when changing the set value $U_{dc2(set)}$ is 5%, while the overshoot caused by the change of the perturbation value I_{ch2} is less than 1%.

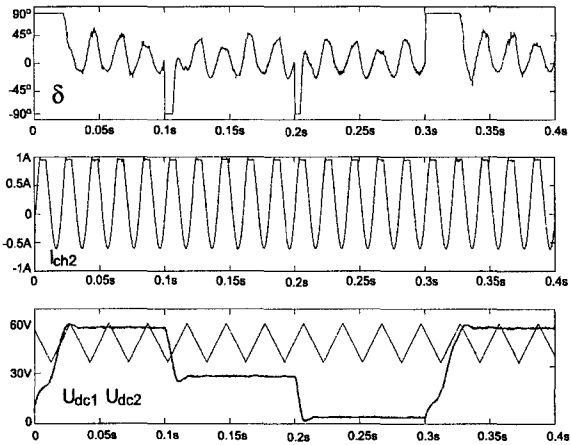

Figure 4.44: Measurements with special perturbation value waveforms

The measurements presented in the Figure (4.44) show the same output voltage control for U_{dc2}, but in this measurement a sinusoidal load current was generated and the feeding voltage U_{dc1} has got a triangular waveform. In any case of measurement it can be seen that the influence of the load current I_{ch2} as a perturbation value is higher than the influence of the feeding voltage U_{dc1}. The feeding voltage effects can be easily compensated with the controller and so do not interact directly on the output voltage value U_{dc2}.

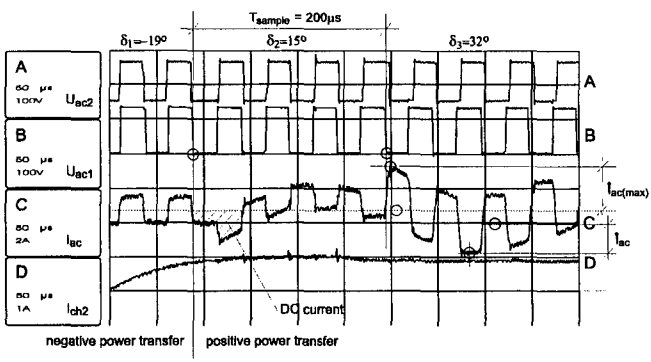

Figure 4.45: Measurements with a change of the power direction

The presented graphs in Figure (4.47) are done by an oscilloscope showing the AC-link values U_{ac1}, U_{ac2} and the current I_{ac}. The action of this measurement was a change of the current I_{ch2} (Graph D), changing from a negative value to a positive current. This

means that δ must change its sign value, which is shown on top of the graphs, where the value of δ is changing from -19^o to 32^o by an intermediary step. A resonant current is started as soon as the new value for δ is active and the sign value for δ has changed. The resonant frequency f_{LC} is:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_{\sigma tot}C_d}} = 2.8kHz \tag{4.130}$$

The resonance is damped after three periods of the resonance frequency f_{LC}. For a DC-DC converter for a small power, this does not cause any problems, but for high-power DC-DC converters this resonance will not damp in a few periods, because the resistive part of the transformer is proportionally smaller. The peak current from the resonance $\widehat{I}_{ac(max)}$ can destroy the semiconductors or cause a saturation of the decoupling inductor. A method to prevent this excitation of the resonant frequency can be easily implemented and is shown in the next Figure (4.46).

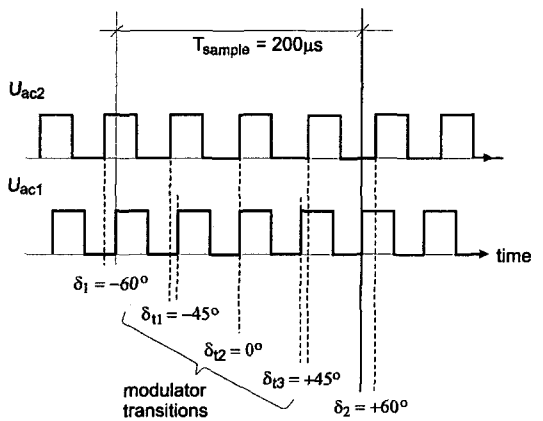

Figure 4.46: Soft changing of δ within the sampling period

The method consists of a soft changing modulator during a sampling period. If the modulation controller requires a change of the sign value for δ, the modulator will not directly apply the new value for δ (In the Figure this value is δ_2), but there will be some fixed intermediate steps, which are applied after every switching period. This soft-change of the controller output can be implemented in the modulator in a state machine. If the sampling time T_{sample} does not allow multiple intermediate steps, because the switching period $\frac{1}{f_p}$ is nearly the same time, at least the intermediate step with $\delta = 0$ must be applied to the modulator. This will avoid to create a short during DC current in the AC link and a resonance can be avoided.

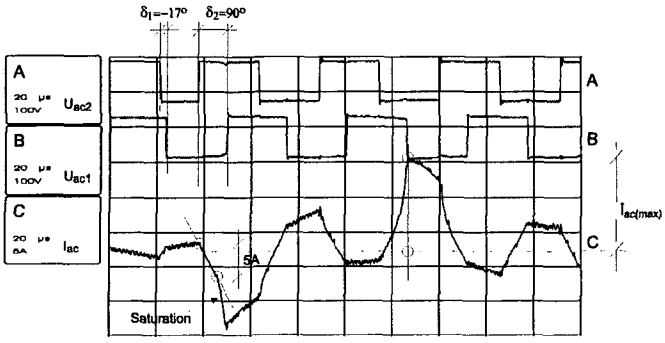

Figure 4.47: Measurements with saturated decoupling inductor

The last measurement in Figure (4.47) shows a radical change for δ, the angle difference is 107^o. A relatively high constant voltage is integrated over the decoupling inductor for too long, so the current I_{ac} is rising an saturates the inductor. Of course the current immediately becomes even bigger. A saturation of the inductor of this kind would immediately destroy the semiconductors in a high-power implementation.

4.5 Experimental results on a 20kW prototype for the combined modulation method

Some more experimental results have been achieved on a medium power prototype for 20kVA. The used semiconductor switches were IGBTs from FUJI. The entire experimental system is shown in the Figure (4.48)

The same PC setup has be used for the 20kVA prototype to realize the controller. The control algorithm on the PC calculates in each sampling period four time values T_A to T_D, the sign value for the power and a stop flag, to immediately stop the modulation and to go to the idle state I. This time values are sent over the PC bus to the modulator card, where the new state time values are updated. The DC-DC converter is fed by a three-phase variac, with a maximal power of 10kW. The output voltage of the variac is rectified through a three-phase rectifier bridge. Between the rectifier bridge and the DC-DC converter primary side, a set of electrolytic capacitors stabilize the feeding voltage U_{dc1}. No chopper was realized to dissipate the energy, if the DC-DC converter is operated in the generative mode (current $\overline{I}_{dc2}$ negative).
The parameters for the realized DC-DC converter are given in the Table (4.19). The transformer used for these measurements was the coaxial transformer, as described in the Table (4.17)

Due to the complex control algorithms, the sampling period is significantly longer than in the implementation with the rectangular current mode. Due to security reasons, the blanking time is chosen relatively long. The experimental results are presented in

Figure 4.48: Experimental system for the DC-DC converter

the following measurements.

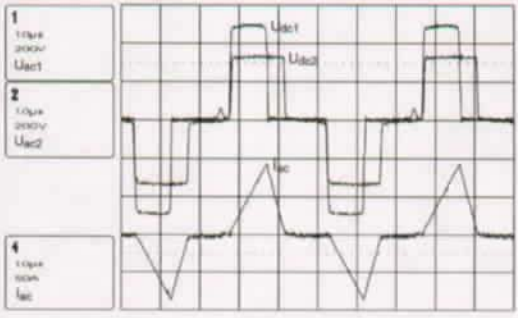

Figure 4.49: Experimental result on the DC-DC converter in the triangular mode

The first measurement is done when the DC-DC converter is working in the triangular mode. It is important that the control algorithm knows the exact value for the total decoupling inductance L_{ertot} and the blanking time, so that a correct zero-current turn-off is proceeded. Also all the electrical values like the load current I_{ch2} and the two DC voltages U_{dc1} and U_{dc2} must be measured correctly. The output voltage is controlled at 360V, while the feeding voltage U_{dc2} is fixed at 500V.

Parameter	Symbol	Value
Feeding voltage	U_{dc1}	100V - 600V
Nominal output voltage	$U_{dc2(nom)}$	500V
Nominal output current	$\overline{I}_{dc2}$	40A
Switching frequency	f_p	20kHz
Load resistor	Z_{load}	$50 - 150\Omega$
Power IGBT	$U_{ce_{max}}, I_{c_{max}}$	1200V,200A
Max. DC current	$I_{dc1_{max}}$	80A
Input capacitor	C_{dc1}	565μF
Output capacitor	C_{dc2}	565μF
Decoupling inductors	L_{d1}, L_{d2}	27μH
Decoupling capacitors	C_{d1}, C_{d2}	200μF / 25V
Blanking time	τ_{blank}	10μs
Sampling period	T_{sample}	300μs

Table 4.19: Realized DC-DC converter for 20kVA

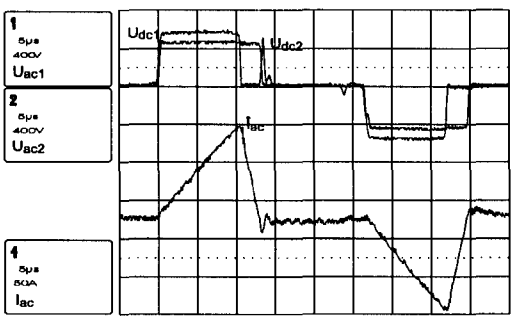

Figure 4.50: Experimental result on the DC-DC converter in the triangular mode

The second measurement is showing the triangular current mode with a turn-off current reaching $\widehat{I}_{ac1} = 125A$. The controlled output voltage is $U_{dc2} = 450V$. The overall transferred power is $P_{dc2} = 12.5kW$, which is the upper limit for the feeding variac. It can be seen that when the current I_{ac} is on a falling slope to zero, it becomes negative for a short time. This effect can switch-on an anti-parallel diode of a switch in the leading half-bridge to commutate. In this case the diode D1 was turned-on. This is why the AC voltage U_{ac1} is not equal to zero and is a positive value again. The positive voltage for U_{ac1} acts on the current I_{ac} and it falls back to zero. This problem can be avoided by having precise measured values for the electrical values and for the system components. An additional saturable inductor can also help to stop the current going negative. This is described on page 138.

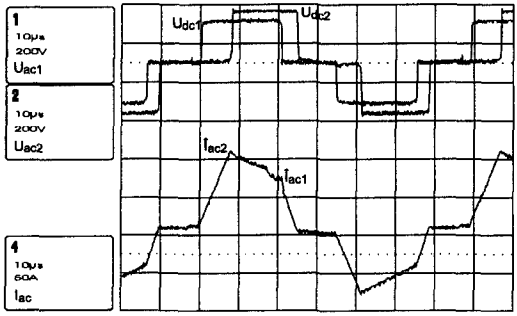

Figure 4.51: Experimental result on the DC-DC converter in the trapezoidal mode

In the measurement in Figure (4.51) of the DC-DC converter, the modulation is the trapezoidal current mode. The big blanking time can be seen. The current I_{ac} is of course equal to zero during this time. Due to the unprecise measurement of the two DC voltages and the load current, the current I_{ac} is not really turned off at the zero crossing. A remaining DC current is circulating in the AC link. For the trapezoidal mode, the turn-offs at the zero-crossing of the current are difficult to achieve and the implemented algorithms are relatively complicated.

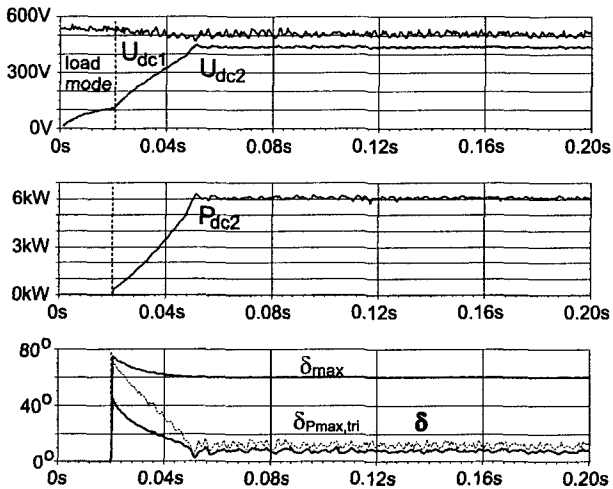

Figure 4.52: Experimental result of the controller system

The controller system working together with the modulation method are tested. The Figure (4.52) shows the measurements done by the measurements from the AD-converter card of the PC. At the beginning of the experiment the modulator is in the load mode,

where the output capacitor C_{dc2} is charged to 20% of the nominal voltage value. After this, the controller takes over, working always in the triangular mode. This can be seen by the fact that the value for δ is never higher than the maximal value for the triangular modulation $\delta_{Pmax,tri}$. The feeding voltage is at $500V$, while the output voltage is controlled to 450V. The load current is about $I_{ch2} = 12A$. It is a resistive load, that is why the transferred power is proportional to the output voltage.

Conclusions

The experimental results presented prove the feasibility of a medium-power DC-DC converter with a controlled output voltage working in a two quadrant mode: The DC-DC converter is operating in a hard-switched mode, but thanks to the proposed modulation algorithms causing zero current switching, the losses can be reduced in comparison to the existing modulation solutions (rectangular mode). The developed control algorithms allow a compensation of all perturbation values and the performance allows a reduction of the output capacitor. In combination with these modulation and control strategies, a coaxial and a new type of planar transformer were designed and realized. The transformers are adapted to this type of DC-DC converter.

Chapter 5

Multilevel converter systems

5.1 Single phase multilevel converter for traction applications

The single-phase multilevel converter is an ideal converter system for the front-end coupling of the locomotive to an AC catenary. The AC catenary is normally a high-voltage power line with a low frequency (15kV with $16\frac{2}{3}$Hz in Switzerland, Germany and Austria, but even 25kV with 50 Hz in France, Spain etc.). The present drive solutions uses a heavy low-frequency transformer to reduce the input voltage towards the converter. In this way, the classical converter scheme connected to a DC link (NPC converter or full-bridge converter) can be coupled to a AC voltage of a medium frequency (2.5kV-3kV). Power semiconductors like the GTO or lately IGBT and IGCT are used as converter switches.

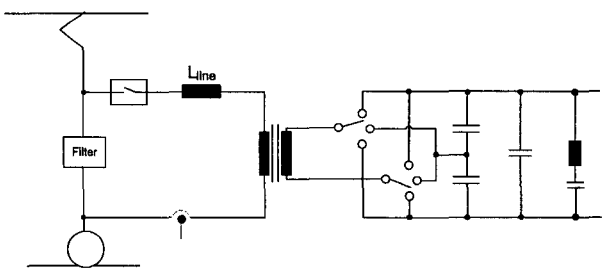

Figure 5.1: Classical converter scheme to connect locomotives to the catenary

The Figure (5.1) shows a classical solution using a NPC converter topology. The semiconductors used were usually GTOs, in order to handle the high currents. Some other solutions have been presented before using a high-voltage chopper converter at the line side in order to rise the line side frequency [45] and [46]. The proposed multilevel converter topology for drives presents a number of interesting advantages for this application. For instance, it can replace entirely the heavy-weight transformer. But there are some additional merits of the novel drive topology:

- The converter is directly coupled to the catenary and uses a certain number of multilevel steps, consisting of a 4Q-converter fed by a DC-DC converter. There is no low-frequency transformer any more, weighting up to 12 tons. The galvanic insulation is done by the medium-frequency transformers in the DC-DC converters. all the MF-transformers together weight about 1 ton.

- The multilevel topology generates an output voltage of a very high quality. This allows either to reduce the decoupling inductance L_{line} to a small value. This means a further gain of weight for the system.

- The resulting switching frequency of the ML-converter is a multiple of the effective semiconductor switching frequency. This allows to design a filter for a higher frequency than in the classical solution. The filter is smaller and the influence on the control dynamics will be reduced.

- In the ML-topology the voltage is high, resulting a smaller current comparing to the classical solutions. This allows the use of faster semiconductors. Combined with the high-voltage quality and a powerful processor for control the converter can not only be used as a AC-DC power converter, but also as an active filter in order to reduce the current harmonics in the power lines.

- The system is modular. The modular design allows an equal distribution of the converter cells in the locomotive. If there is a bulky low-frequency transformer, the locomotive has to be reinforced around the transformer, which causes additional weight and construction limitations. Also the modularity allows the creation of a failure-tolerant converter with the use of a number of redundant converter modules. The modules can be used for other ML-converter applications.

- The system can be configurable. By having a configurable system, the locomotive could be used on different power lines by changing its configuration.

- The ML-converter system has a better efficiency in the medium and high power range.

It can be easily seen that this topology presents an important number of advantages for future developments for railways. The main drawbacks of the system are of course the costs (it requires a lot of expensive semiconductors) and the complexity. The complexity of the system causes automatically a reduction of reliability. An ideal power semiconductor for this application is the IGBT switch. Presently, there are not many studies on the reliability of IGBT switches in such a multilevel configuration.
Figure (5.2) shows a generalized configuration of a ML-converter for traction applications.

In the presented figure, all the electrical values are defined. Two types of the ML-converter are presented. The idea is to control the power flow in order to feed the motors of the locomotive. The line current I_{line} must be controlled in a way that it has as few harmonics as possible. At the same time, it needs a very fast dynamic behavior when the set value changes. On the bottom of Figure (5.2) the different controllable power transfers are mentioned.
The entire ML-converter consists of a certain number of steps n. A step is composed of a four-quadrant converter with a DC-DC converter. An intermediate capacitor $C_{dc2(i)}$

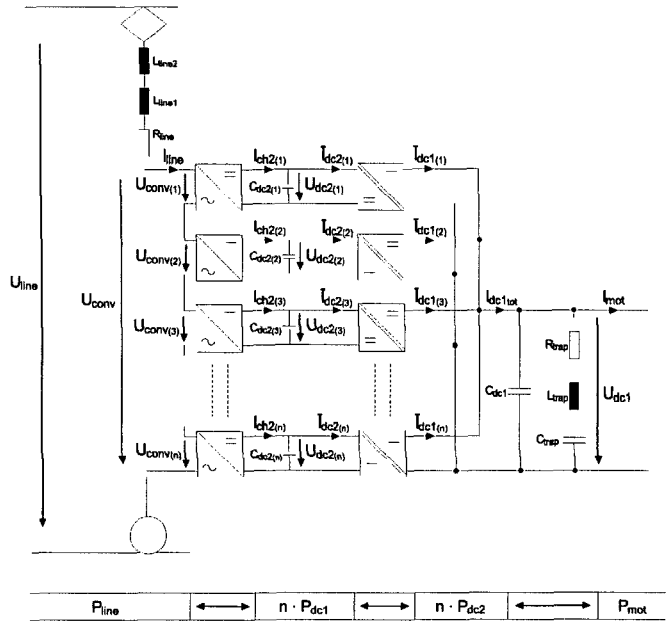

Figure 5.2: Multilevel converter setup for locomotive drives

stabilizes the voltage between the DC-DC converter and the 4Q-converter. Each of 4Q-converters can be modulated by a PWM modulation function with a modulation degree k. The DC-DC converter is feeding the 4Q-converter. The DC-DC converter can be controlled in two different ways: It can either control the primary side DC voltage U_{dc1} or the secondary side voltage U_{dc2}. This is one common voltage to control for all the DC-DC converters, because all the primary sides of the DC-DC converters are connected together. The other possibility is that each of the DC-DC converters control the secondary side voltage $U_{dc2(i)}$.

There is a special component in series with each capacitor $C_{dc2(i)}$ or C_{dc1}. The element is called short circuit current limiter (SCCL). This element is needed, if the capacitors are higher than $500\mu F$. This element becomes resistive as soon as the current exceeds a certain value. The element prevents a short circuit in the case of a capacitor failure and avoids the destruction of the entire multilevel cell by the energy discharge stored in the capacitor. For each $2mF$ of capacitor, an SCCL is needed. The only advantage is that this element causes extra weight (about 25kg) to the system.

To filter the harmonics caused by the resulting switching frequency $n \cdot f_s$, a passive filter is needed. The filter used for all the presented converters is shown in Figure (5.4):

The entire system is divided into three parts, which can be controlled separately. The ML-converter can be considered just as a simple AC-DC converter. On the AC side, the line parameters such as the decoupling inductance and the resistive part of this inductance can be found. The DC-side is shown with the DC-link and the optional

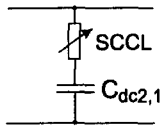

Figure 5.3: Short circuit current limiter in series with the capacitors

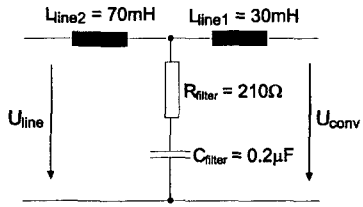

Figure 5.4: Passive filter in order to reduce harmonics caused by the switching frequency

low-frequency filter, called trap circuit.

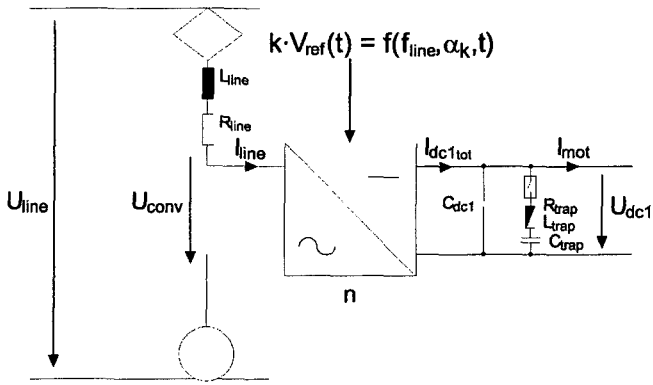

Figure 5.5: Multilevel converter system presented as AC-DC converter

The power supply lines of railways are in a single phase feeding. When the line voltage U_{line} is at its peak value, a maximum of power can be transferred. If the line voltage is zero, no power can be transferred. So the power coming into the DC-link is a pulsating power, it is not constant (This is only possible with three-phase systems or with DC power lines). The pulsating frequency has twice the line frequency. The motor of course needs a constant power. This means that a locomotive drive converter needs an energy storage system to provide the missing energy when the line voltage crosses zero. Usually the locomotive constructors use a series connected LC filter in parallel to the DC-link capacitor. This setup is called "trap circuit". It is designed to obtain a strong

U_{conv}	Multilevel converter output voltage [V]
U_{line}	Single phase line voltage from the catenary [V]
I_{line}	Line current, should be in phase with the line voltage [A]
f_{line}	Line voltage frequency [Hz]
V_{ref}	Modulation function for the global multilevel converter
k	Modulation degree of the global multilevel converter
$\tau_{blank(4Q)}$	Blanking time used for the 4Q-converters
f_s	Switching frequency for an independent 4Q-converter
α_k	Phase angle between the line voltage and the converter voltage [rad]
L_{line}	Decoupling inductance from the line [H]
R_{line}	Resistive part of the decoupling inductance [Ω]
n	number of multilevel steps

Table 5.1: Electrical values on the AC side of the converter

$I_{dcl_{tot}}$	Summarized DC-DC converter output currents [A]
I_{mot}	Motor current, comes from motor converter [A]
U_{dcl}	DC-link voltage [V]
C_{dcl}	DC-link capacitor [F]
C_{trap}	Trap circuit filter capacitor [F]
L_{trap}	Trap circuit filter inductance [H]
R_{trap}	Trap circuit parasitic resistance [Ω]

Table 5.2: Electrical values on the DC-link of the converter

attenuation of the pulsating power frequency.

The DC-side (with the DC-link) is characterized by Table (5.2):

The Equations for the AC part of this converter system are mentioned below. The line current I_{line} results from the difference of the two voltages U_{conv} and U_{line}:

$$\Delta U = U_{line} - U_{conv} = I_{line}R_{line} + L_{line}\frac{d}{dt}I_{line} \tag{5.1}$$

It is supposed that the voltage and current values are sinusoidal. The transformation of Equation (5.1) into the Laplace domain gives:

$$I_{line} = \frac{U_{line} - U_{conv}}{R_{line} + sL_{line}} = \frac{\Delta U}{R_{line}} + \frac{1}{s}\frac{\Delta U}{L_{line}} \tag{5.2}$$

The generated current behavior is thus a sum of a dominating integral behavior over the inductance and a resistive behavior. By using the trigonometric relations and by solving for the line current, the basic phasor diagram is helpful. In the shown phasor diagram (5.6), the current I_{line} is in phase with the line voltage U_{line}.

The equations are found by considering the trigonometric relations given in Figure (5.6). This means that the line voltage and current are always in phase.

$$I_{line} = \frac{\sqrt{{U_{conv}}^2{R_{line}}^2 + 4\pi^2{f_{line}}^2{L_{line}}^2({U_{conv}}^2 - {U_{line}}^2)} - U_{line}R_{line}}{{R_{line}}^2 + 4\pi^2{f_{line}}^2{L_{line}}^2} \tag{5.3}$$

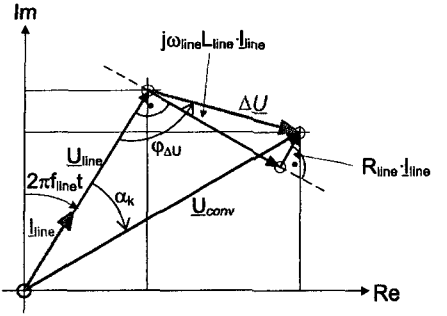

Figure 5.6: Phasor diagram for a single-phase AC-DC converter

and:

$$\alpha_k = \arctan\left(\frac{2\pi f_{line} L_{line} I_{line}}{U_{line} + R_{line} I_{line}}\right) \tag{5.4}$$

In most applications, the resistive part of the line impedance is negligible in comparison to the inductive part $2\pi f_{line} L_{line}$. But for traction applications, the inductance is chosen very small (around 20mH) in order to reduce weight and the line frequency is very low, therefore the ohmic part has taken into account. The aim of the AC-DC converter is to control the line current to a sinusoidal value. It is obvious that the current can be controlled by varying the converter voltage U_{conv}. More power is generated if the voltage $\Delta\underline{U}$ increases with a fixed angle $\varphi_{\Delta\underline{U}}$ towards U_{line}. The angle is given by:

$$\varphi_{\Delta\underline{U}} = \arctan\left(\frac{R_{line}}{\omega_{line} L_{line}}\right) + \frac{\pi}{2} \tag{5.5}$$

Therefore the converter voltage moves on the line defined by this angle (5.5), the current remains in phase with the line voltage and the amplitude can be modified. The peak value of the line current is given by:

$$\hat{I}_{line} = \sqrt{2}\frac{P_{mot}}{U_{line}} \tag{5.6}$$

of course $\hat{I}_{line}$ can also be expressed by using the modulation degree as a variable parameter:

$$\hat{I}_{line} = \frac{\sqrt{\left[\sum_{i=1}^{n} U_{dc2(i)}\left(k_{(i)} - \tau_{blank(4Q)} f_s\right)\right]^2 - \hat{U}_{line}^2}}{2\pi f_{line} L_{line}} \tag{5.7}$$

The modulation degree $k_{(i)}$ is considered to be the global modulation degree k and is given by the following equation, derived from (5.3):

$$k = \tau_{blank(4Q)} f_s + \frac{\sqrt{4\pi^2 {f_{line}}^2 {L_{line}}^2 \hat{I}_{line}^2 + \hat{U}_{line}^2}}{\sum_{i=1}^{n} U_{dc2(i)}} \tag{5.8}$$

The relation between the modulation degree k, the modulation function $V_{ref}(t)$ and the converter output voltage is given below:

$$U_{conv} = U_{dc2} \cdot V_{ref}(t) \cdot (k - \tau_{blank(4Q)} f_s) \tag{5.9}$$

$V_{ref}(t)$ must be a function in the time domain. The amplitude will usually vary in the interval $[-1, 1]$, just like a sine-wave. The number of steps used for the multilevel converter depends on the maximal possible peak voltage of U_{line}, on the decoupling inductance and the maximal possible current I_{line}. To generate a current with $cos(\varphi) = 1$, the converter voltage must always be higher than the line voltage U_{line}:

$$n \geq trunc\left(\frac{\sqrt{\hat{U}_{line}^2 + 4\pi^2 {f_{line}}^2 {L_{line}}^2 \hat{I}_{line}^2}}{U_{dc2}}\right) + 1 \tag{5.10}$$

The influence of the resistive part of the line inductance has been neglected. The next equations are describing the DC side of the AC-DC converter black-box behavior. The values are DC values with superposed AC harmonics, depending on the control system and the trap circuit (filter) used. If there is no trap circuit, the equation for the DC link is simple:

$$U_{dc1} = \frac{1}{C_{dc1}} \int (I_{dc1_{tot}} - I_{mot})\, dt + U_{dc1}\Big|_{t=0} \tag{5.11}$$

The initial condition on the DC-link is important, especially if it is desired to observe dynamic transitions when the trap circuit is used. The motor current is usually a constant current source. Normally, one DC-link is used to feed two motors. The DC-AC converters to feed the motors are usually standard three-phase NPC (neutral-point-clamped) converters [13]. The motor currents of course contain harmonics coming from the switching of the motor converters.

$$I_{mot} = \frac{P_{mot}}{U_{dc1}} \tag{5.12}$$

If the trap circuit is active, the behavior of the DC-link is more complicated. In any case, there is a dominant integral behavior due to the high capacitors. The impedance of the DC-link is evaluated in the Laplace-domain. There are three energy storage elements in the DC-link, so the order of the polynomial of the impedance will be 3.

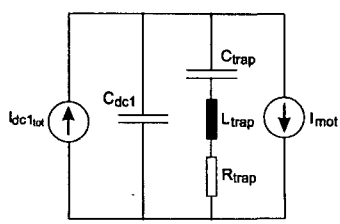

Figure 5.7: Schematics for the trap circuit

DC-link capacitor	12mF
Trap circuit capacitor	15mF
Trap circuit inductor	1.515mH
Trap circuit inductor resistance	$20m\Omega$

Table 5.3: Parameters for the trap circuit to filter $33\frac{1}{3}$Hz

The trap circuit is designed to filter the pulsating power transfer with the line frequency. The resulting impedance in the Laplace domain for the trap circuit of (5.7) is given below:

$$Z_{trap} = \frac{s^2 L_{trap} C_{trap} + s R_{trap} C_{trap} + 1}{s^3 L_{trap} C_{trap} C_{dcl} + s^2 R_{trap} C_{trap} C_{dcl} + s(C_{dcl} + C_{trap})} \tag{5.13}$$

It can bee seen from this equation that there will be a dominant integral behavior with the time constant $C_{trap} + C_{dcl}$. The parameters chosen for the trap circuit depend on the line frequency. If the line frequency is $16\frac{2}{3}$Hz, then the trap circuit has to be designed to filter $33\frac{1}{3}$Hz. The parameters for such a trap circuit are given below:

The next Figure (5.8) shows a Bode diagram of the designed trap circuit. The attenuation peak is exactly at $33\frac{1}{3}$Hz. But there is also an amplification peak (resonance) at 50.12Hz. It can be expected that the DC-link will have a superposed oscillation at 50Hz.

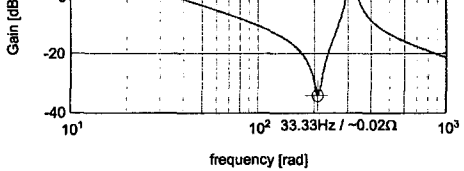

Figure 5.8: Bode diagram for the trap circuit impedance

The DC-DC converter has to be characterized mathematically in order to create a simulation model for the multilevel systems. The model must be simple in order to be able to simulate over long periods with a limited sample time, but still it must represent correctly the black-box behavior. The internal values of the DC-DC converter like the switching and conduction effects, modulation parameters or the peak current values are not important for this simulation. The next Figure shows the DC-DC converter as a black-box:

The new parameters and the electrical values for the DC-DC converter module are defined in the following table:

The basic Equation defining the whole behavior of the DC-DC converter, describes the ratio between input and output currents and voltages. The losses of the DC-DC converters are not taken into account for the simulation of the entire system. The losses

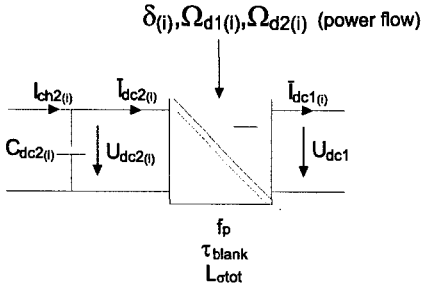

Figure 5.9: DC-DC converter represented as a black-box

i	Index to indicate the step number
$U_{dc2(i)}$	DC voltage between the DC-DC converter and the 4Q-converter
$\overline{I}_{dc1(i)}$	Current going from the DC-DC converter to the DC-link
$\overline{I}_{dc2(i)}$	Current going from the DC-DC converter to the 4Q-converter
τ_{blank}	Blanking time for the DC-DC converter switches
$C_{dc2(i)}$	Storage capacitor between 4Q-converter and DC-DC
$L_{\sigma tot}$	Decoupling inductance
f_p	Switching frequency
$\delta_{(i)}, \Omega_{d1(i)}, \Omega_{d2(i)}$	Modulation parameters

Table 5.4: Parameters for the DC-DC converter

might be around $3\% - 4\%$ so they will not influence the control behavior. So the input power of the DC-DC converter is the same as the output power:

$$\overline{I}_{dc2(i)} = \frac{U_{dc1}}{U_{dc2(i)}} \cdot \overline{I}_{dc1(i)} \tag{5.14}$$

The behavior of the voltage $U_{dc2(i)}$ over the capacitor is described by the next differential equation in the time domain. Of course it is an integral behavior, which has to be taken into account for the controller design.

$$U_{dc2(i)} = \frac{1}{C_{dc2(i)}} \int \left(I_{ch2(i)} - \overline{I}_{dc2(i)} \right) dt + U_{dc2(i)}\Big|_{t=0} \tag{5.15}$$

The current $I_{dc1_{tot}}$ flowing into the DC-link is composed of all the primary currents of the DC-DC converters:

$$I_{dc1_{tot}} = \sum_{i=1}^{n} \overline{I}_{dc1(i)} \tag{5.16}$$

Also some Equations are given to describe the black-box behavior of an independent four-quadrant converter. They are all connected in series over their AC side. Due to this series connection, all the generated AC voltages are added for the multilevel converter, generating the ML-converter output voltage U_{conv}.

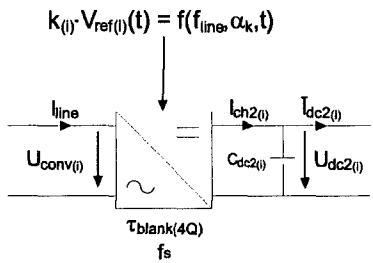

Figure 5.10: Independent four-quadrant converter represented as a black-box

$k_{(i)}$	Modulation degree for the independent 4Q-converter
$U_{conv(i)}$	AC voltage generated by an independent 4Q-converter
$I_{ch2(i)}$	Load current generated by the 4Q-converter
$I_{ch2dc(i)}$	DC part of the load current generated by the 4Q-converter
$k_{(i)} \cdot V_{ref(i)}$	Modulation function and degree for the 4Q-converter

Table 5.5: Parameters for the 4Q-converter module

Some new parameters are introduced. They are listed up in the table (5.8). The multilevel output voltage is given by the simple addition of all partial AC voltages from the 4Q-converters:

$$U_{conv} = \sum_{i=1}^{n} U_{conv(i)} \tag{5.17}$$

The peak voltage value of the multilevel converter depends of course on the number of steps used. The individual converter voltage is influenced by the blanking time of the switches. Especially by using fast switching frequencies f_s for the 4Q-converters, the influence of the blanking time $\tau_{blank(4Q)}$ decreases the maximal peak voltage value $\hat{U}_{conv}$. For a traction system converter, the switching frequencies chosen are rather low (between 200Hz and 400Hz, to avoid unnecessary losses). The adequate blanking time for the semiconductors has to be chosen considering the turn-on and turn-off times. The individual converter output voltage is defined:

$$U_{conv(i)} = U_{dc2(i)} \cdot V_{ref(i)} \cdot (k_{(i)} - \tau_{blank(4Q)} f_s) \tag{5.18}$$

If the 4Q-converter voltage is modulated by a sinusoidal function, the equation is:

$$U_{conv(i)} = U_{dc2(i)} sin(2\pi f_{line} t + \alpha)(k_{(i)} - \tau_{blank(4Q)} f_s) \tag{5.19}$$

So the total converter voltage is given by the Equation (5.20)

$$U_{conv} = \sum_{i=1}^{n} U_{dc2(i)} sin(2\pi f_{line} t + \alpha_k)(k_{(i)} - \tau_{blank(4Q)} f_s) \tag{5.20}$$

An interesting electrical value is the sliding average value of the current $I_{ch2(i)}$ coming from the 4Q-converter. The sliding average value is important for the control system, because the control system is not able to react on the independent switching events:

$$\overline{I}_{ch2(i)}(t) = I_{line} \cdot V_{ref(i)}(t) \cdot (k_{(i)} - \tau_{blank(4Q)} f_s) \tag{5.21}$$

Assuming that the modulation function $V_{ref(i)}$ is a sinusoidal function,

$$\overline{I}_{ch2(i)}(t) = \frac{1}{2}\hat{I}_{line}(k_{(i)} - \tau_{blank(4Q)} f_s)[cos(\alpha) - cos(4\pi f_{line} t + \alpha_k)] \tag{5.22}$$

This equation is important to calculate the voltage waveform on the capacitor $C_{dc2(i)}$. Is important to know that of course the current $\hat{I}_{line}$ is depending also on $k_{(i)}$. To calculate this, take Equation (5.8) has to be taken. The DC component of this current is given by:

$$I_{ch2dc(i)} = \frac{1}{\sqrt{2}}\hat{I}_{line}(k_{(i)} - \tau_{blank(4Q)} f_s) cos(\alpha_k) \tag{5.23}$$

5.1.1 Multilevel converter system without trap circuit

The first multilevel converter system tested is a concept without trap circuit filter. The basic idea is to renounce to all heavy filtering elements. The energy shall be stored on the capacitors C_{dc2} between the DC-DC converters and the 4Q-converters. Of course the voltage on these capacitors will oscillate. The power coming from the 4Q-converters is pulsating with twice the line frequency f_{line}. But the DC-DC converters will transfer a constant power to the DC-link. This means that the voltages $U_{dc2(i)}$ will oscillate with twice the line frequency f_{line}. By using a sophisticated control scheme, these voltages can oscillate with twice the line frequency, but there average value $U_{dc2_{av(i)}}$ will be kept constant. This system is very interesting, because the weight and volume of the system are reduced to a maximum. There are no remaining low-frequency elements.
The next Figure (5.11) shows the schematics of the traction converter with n steps without trap circuit:

For a real implementation of the system about 10-14 steps are needed. In this setup, all the DC-DC converters together have to control one single output voltage U_{dc1}. So the DC-DC converters see the all the same measured feedback value and, of course, the same controller set value. The current I_{dc1tot} is generated by n sub-currents $\overline{I}_{dc1(i)}$. Of course the voltages $U_{dc2(i)}$ are not controlled from the DC-DC converter. The oscillation with twice the line frequency can only be reduced by choosing the capacitor values $C_{dc2(i)}$ high enough. The voltage oscillation is proportional to the capacitor values. The capacitor value exceeds $500\mu F$, so a SCCL is needed in series to the capacitor. Comparing to a solution with trap circuit, these capacitors must be chosen of a much higher value.
The next equations are valid if the line current and voltage are in phase and the resistive part of the line inductor is neglected:

$$U_{dc2(i)}(t) = U_{dc2(i)}\Big|_{t=0} - \frac{\hat{I}_{line}(k_i - \tau_{blank(4Q)} f_s) sin(4\pi f_{line} t + \alpha_k)}{8\pi f_{line} C_{dc2(i)}} \tag{5.24}$$

The voltage oscillation (peak to peak value) is given by:

$$\Delta U_{dc2(i)} = \frac{\hat{I}_{line}(k_{(i)} - \tau_{blank(4Q)} f_s)}{4\pi f_{line} C_{dc2(i)}} \tag{5.25}$$

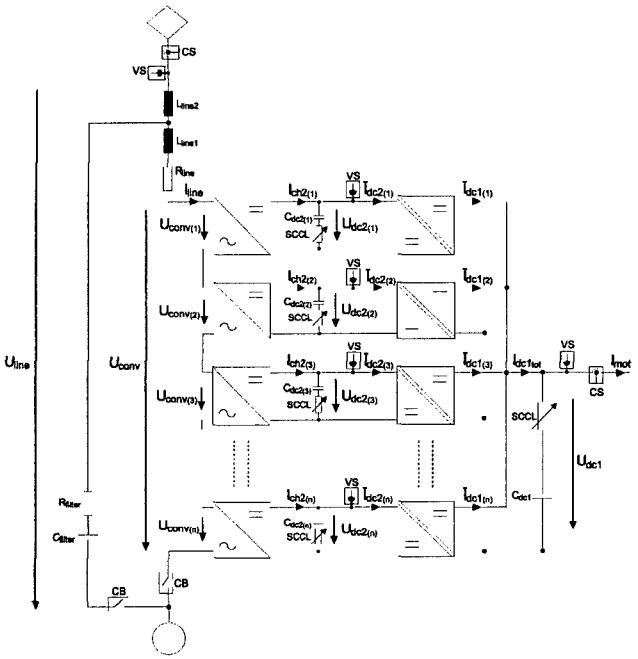

Figure 5.11: Multilevel system schematics without trap circuit in the DC-link

So the appropriate capacitor $C_{dc2(i)}$ can be chosen by deciding what voltage oscillation $\Delta U_{dc2(i)}$ wants to be tolerated:

$$C_{dc2(i)} = \frac{\hat{I}_{line}(k_{(i)} - \tau_{blank(4Q)} f_s)}{4\pi f_{line} \Delta U_{dc2(i)}} \tag{5.26}$$

The modulation degree $k_{(i)}$ is considered to be the global modulation degree k and can be calculated from Equation (5.8). Due to the oscillation of all the voltages $U_{dc2(i)}$, the generated converter voltage U_{conv} will be superposed by the same oscillation. To visualize this effect, the DC voltages are compared with the line voltage from the feeding catenary:

At the phase angle $\alpha_{U_{dc2(min)}}$, all the DC voltages $U_{dc2(i)}$ have their minimal value. It is important that the addition of all these voltages is sufficient in order to maintain the desired current I_{line}.

$$\alpha_{U_{dc2(min)}} = \frac{\pi}{2} + \alpha_k \tag{5.27}$$

The value for α_k can be found in Equation (5.4). If the line voltage U_{line} and U_{conv} is sinusoidal, the minimal needed voltage for U_{conv} can be found out. To calculate this, the trigonometric relations are used, presented in Figure (5.6). The DC-link voltage U_{dc1} of

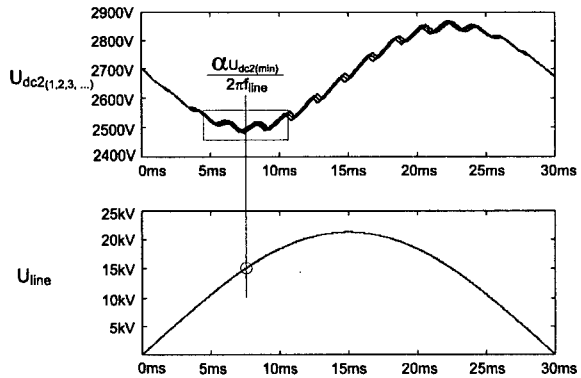

Figure 5.12: Comparison from U_{dc2} with U_{line} to detect the worst phase angle

this topology is controlled by all the DC-DC converters. The current I_{dc1tot} can give a quick response to any load changes. This allows a stabilization of the DC-link voltage. In this case, the DC-link capacitor can be chosen very small.

Control system

The control system proposed for this converter is composed of a structure of five controller systems in cascade of a high complexity. The overall set value for the control system is the desired motor power P_{mot} (Actually, the real set value is the motor speed, but the required power can be derived from the speed set value of the motor). This is the power taken from the DC-link with the capacitor C_{dc1}. It is known that in this topology the voltage U_{dc1} is kept constant, so the it can be said that the overall system set value is the motor current I_{mot}. The following criteria must be fulfilled by the controller:

- The current I_{line} must be sinusoidal with as few harmonics as possible and in phase with the line voltage U_{line}. Furthermore the line current shall not contain any DC component.
- The voltages $U_{dc2(i)}$ shall oscillate with twice the line frequency, but the DC component of the voltage $\overline{U}_{dc2(i)}$ must be constant. Of course the sum of all the average values $n \cdot U_{dc2av}(i)$ of these voltages must also be constant.
- The voltage U_{dc1} must remain perfectly stable and should not have any oscillation.
- The motor current I_{mot} should be able to make step changes of the set value without destabilizing the entire system.

The entire control system is presented in Figure (5.13). In the control system, five different sub-systems can be identified, each with a particular control function:

- The line current controller G_{R1}, combined with the direct introduction of all line values using the trigonometric phasor relations is implemented, given in Figure

(5.6). The controller is a simple PI-controller. The method has been presented in [26].

- The power flow controller G_{R2} in cascade with the line current controller. If the motor does not consume the same power as taken from the line, this controller adapts the demanded power.

- The controllers $G_{R3(i)}$ represented in function block (16). These controllers are responsible to control all DC components of the voltage U_{dc2} by adapting each modulation degree of the 4Q-converters.

- The active harmonic cancellation controllers $G_{R4(i)}$. These set of controllers generate an adapted current set value in order to eliminate all the chosen low-order harmonics and the DC component found on the line current I_{line}.

- The controller of the DC-DC converters, in order to stabilize the output voltage U_{dc1}. This controller is not described in this chapter (see chapter Control of DC-DC converter).

On the left side of the control system, three different set values can be detected: The motor current $I_{mot(set)}$ gives the desired motor power, this value is determined by the speed controller of the locomotive motor, the set value for DC component of the oscillating voltage $\overline{U}_{dc2(set)}$, because the voltage level of the voltages $U_{dc2(i)}$ can be chosen independently to the transferred power, and the amplitudes of the current harmonics $I_{harm(set)}$ that have to be filtered. Of course not all the harmonics can be filtered, this depends especially on the calculation speed of the DFT and IFT algorithm. With a modern processing architecture using signal processors, waveforms up to the 500Hz can be filtered actively.

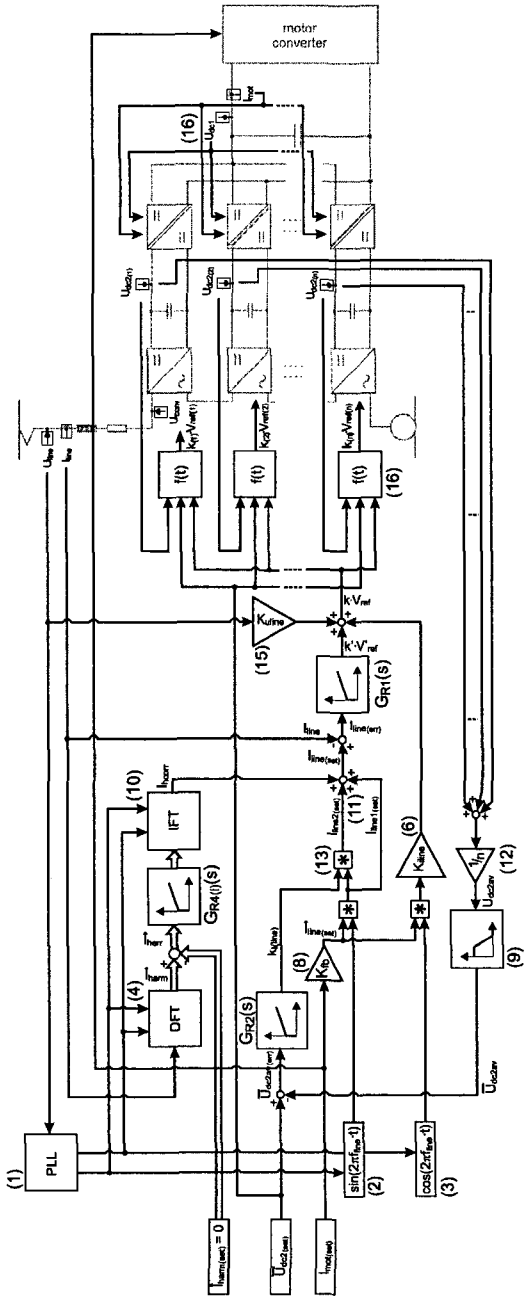

Figure 5.13: Overview over the control system for the system without trap circuit

For the controller structure, a ideal sine wave and a phase-shifted (90°) ideal sine wave is needed (The cosine function). To do this the line voltage U_{line} is measured and is introduced into a PLL circuit (1). The PLL is generating a sine wave (2) and the cosine wave (3), which are perfectly synchronized with the line voltage frequency f_{line} and the phase angles are respected (0° and 90°). These signals are important to generate a perfect sine wave template for the line current set value.

Cascaded controller for line current and power flow The detailed transfer function of the system is shown in Figure (5.15). There are n systems in parallel, the input value is a modulation function and the output is a partial converter voltage $U_{conv(i)}$. But to design the control system, only one global converter is considered U_{conv}, generating the converter current on the line inductance. By looking at the controller in this way, the elements of a cascaded controller can be identified. Figure (5.14) shows the simplified structure for the controller in cascade.

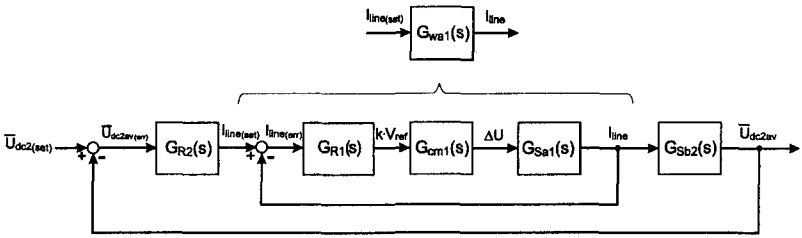

Figure 5.14: Overall control system seen as cascaded controller

The line current controller $G_{R1}(s)$ is the internal controller of the cascaded structure. It is a PI controller (the implemented controller is shown in Figure (5.16)), which generates a sinusoidal modulation function $k' \cdot V'_{ref}$. The set value introduced to the multilevel converter is a linear combination of the line current U_{line}, the cosine function generated with the PLL circuit representing the phase of the voltage drop ΔU over the line inductance L_{line} and of course the set value $k' \cdot V'_{ref}$ coming from the controller G_{R1}.

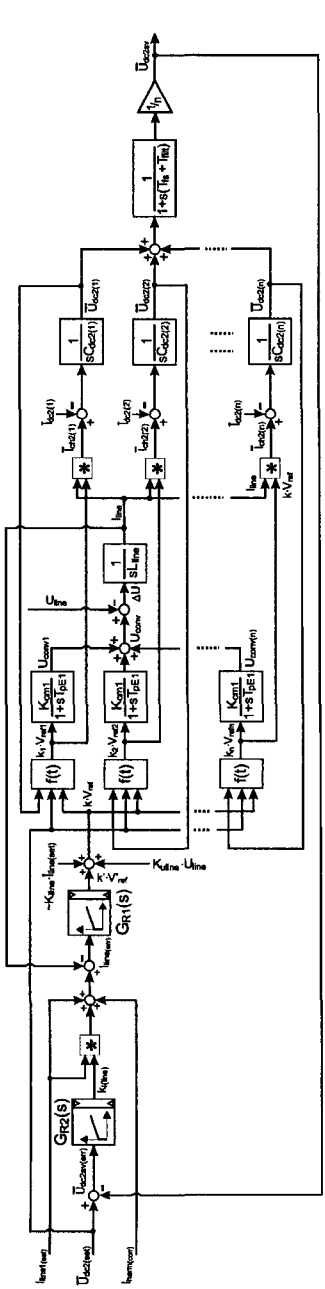

Figure 5.15: Cascaded controller for the power flow and the line current

The result of this addition is a global modulation function $k \cdot V_{ref}$.

$$k \cdot V_{ref} = K_{uline} U_{line}(t) + K_{iline} cos(2\pi f_{line} t) \widehat{I}_{line(set)} + k' \cdot V'_{ref} \tag{5.28}$$

This linear combination is done to pre-generate a sinusoidal set value of the current according to the trigonometric relations given in Figure (5.6), which allows the controller only to do a small correction of the current. The parameter K_{uline} is given by the Equation (5.29)

$$K_{uline} = \frac{1}{n \cdot U_{dc2(set)}} \tag{5.29}$$

The multiplication factor (6) direct introduction of the vector in direction of the voltage drop ΔU is given below:

$$K_{iline} = \frac{2\pi f_{line} L_{line}}{n \cdot U_{dc2(set)}} \tag{5.30}$$

It would also be possible to introduce directly a vector to the set value $k' \cdot V'_{ref}$, compensating the $33\frac{1}{3}$Hz voltage oscillation on the feeding voltages $U_{dc2(i)}$. The oscillation is seen afterwards on the converter voltage U_{conv}. This is why this vector must be in phase with U_{conv}, and thus must be in phase with the modulation function $k \cdot V_{ref}$. The correction factor to be multiplied with the modulation degree k is:

$$K_{udc2} = \frac{\overline{U}_{dc2av} - U_{dc2}}{n \cdot U_{dc2}} \tag{5.31}$$

In the nominator the AC ripple voltage on the capacitors C_{dc2} is found. The denominator normalizes this voltage to the maximal converter voltage $\widehat{U}_{conv}$, which corresponds to the modulation degree of $k = 1$. So the modulation function is multiplied with the factor K_{udc2} in order to get the correction vector. The resulting correction vector is added to the old modulation function.

$$k'' \cdot V''_{ref} = (1 + K_{udc2}) \cdot k \cdot V_{ref} \tag{5.32}$$

This additional feed-forward of the DC feeding voltage has not been implemented and is not shown in the Figure (5.15). But the method could also help to reduce the line current harmonics.
From the DC current set value for the motor converter $I_{mot(set)}$ it is necessary to know an equivalent amplitude of the AC line current I_{line}. The power set on the line side and on the DC-link side must be the same. The multiplication factor is:

$$K_{fb} = \frac{\sqrt{2} U_{dc1(set)}}{U_{line}} \tag{5.33}$$

The transfer function transferring the output value of the controller to a physical value is named $G_{cm1}(s)$ and is composed of an amplification factor and a small time delay:

$$G_{cm1}(s) = \frac{K'_{cm1}}{1 + sT_{pE1}} \tag{5.34}$$

The system transfer function parameters, which has to be controlled by the current controller shown in Figure (5.16), are given below:

$$K_{cm1} = U_{dc2(set)} \tag{5.35}$$

But due to the fact that the partial converter voltages $U_{conv(i)}$ are added, the amplification factor resulting for the control system is n times higher:

$$K'_{cm1} = n \cdot U_{dc2(set)} \tag{5.36}$$

and the small time constant of the system is composed of:

$$T_{pE1} = \frac{T_{sample}}{2} + T_{cm2} + T_{r2} \tag{5.37}$$

The small time constant is smaller for the overall converter system than for the individual 4Q-converter. This is due to the phase-shifted carrier signals, which allow a faster response on changes of the modulation function. The system delay time introduced by the modulation of the series-connected 4Q-converters, T_{cm2} can be calculated as follows:

$$T_{cm2} = \frac{1}{4n \cdot f_s} \tag{5.38}$$

This value is calculated like to times the resulting switching frequency of the entire multilevel converter. The system that has to be controller is called $G_{sa1}(s)$. This transfer function has an integral behavior.

$$G_{sa1}(s) = \frac{1}{sT_{I1}} \tag{5.39}$$

The dominant time constant for the integrating of the current comes from the line inductance:

$$T_{I1} = L_{line} \tag{5.40}$$

The controller is represented by the transfer function $G_{R1}(s)$. Due to the integral behavior of the current on a inductance, seen in Equation (5.39), the symmetrical optimum [30] is used to calculate the controller parameters. This design method is ideal for good stability against system perturbations. But the method is not optimized for variations of the set value. The two time constants of the controller are:

$$T_{n1} = 4 \cdot T_{pE1} \tag{5.41}$$

$$T_{i1} = \frac{8K'_{cm1}{T_{pE1}}^2}{T_{I1}} \tag{5.42}$$

And the parameters of the controller G_{R1} are given with:

$$K_{i1} = \frac{T_{sample}}{T_{i1}} \tag{5.43}$$

$$K_{p1} = \frac{T_{n1} - \frac{T_{sample}}{2}}{T_{i1}} \tag{5.44}$$

Due to the direct introduction of the phasor diagram into the set value after the controller, shown with Equation (5.28), and the addition of several controller outputs before generation of the set value, the obtained controller values are attenuated with a factor 3:

$$K_{i1} = \frac{K_{i1}}{3} \tag{5.45}$$

$$K_{p1} = \frac{K_{p1}}{3} \tag{5.46}$$

The power flow controller, given by the transfer function $G_{R2}(s)$, is the external controller of the cascaded structure. It is a PI controller, again implemented as shown in Figure (5.16)).

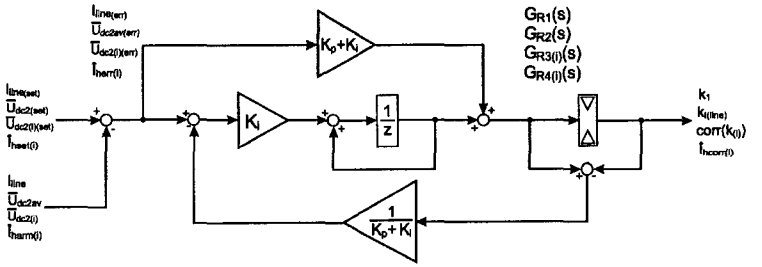

Figure 5.16: Used PI controller for current and voltage control

The controller shown in Figure (5.16) has a discrete time element z^{-1} with the sampling period. All the developments are actually done with the pseudo-continuous method as described in [30]. But the implementation in the simulator but also on PC are of course time-discrete.

The input value is the error of the sum of all DC components of the intermediary voltages $U_{dc2(i)}$. It generates a modulation degree $k_{I(line)}$. This modulation degree is a value limited within the boundaries $[-1, 1]$. This value is multiplied with the line current set value $I_{line1(set)}$, and is added again to the value $I_{line1(set)}$. This multiplication and addition allows to modify the set value, which is a sinusoidal value, without modifying the original waveform. This of course is only valid if the controller has very high time constants T_{n2}, T_{i2} compared to the period $\frac{1}{f_{line}}$ of the sinusoidal set value $I_{line1(set)}$. The power flow controller G_{R2} has to be prevented of introducing additional harmonics into the current set value. The internal controller loop is represented by a new transfer function named $G_{wa1}(s)$:

$$G_{wa1}(s) = \frac{G_{R1}G_{cm1}G_{sa1}}{1 + G_{R1}G_{cm1}G_{sa1}} \tag{5.47}$$

For the external control loop, this transfer function is seen like a function of a small time delay without any amplification:

$$G_{wa1}(s) \cong \frac{1}{1 + sT_{ea1}} = \frac{K_{cm2}}{1 + sT_{pE2}} \tag{5.48}$$

The internal controller was designed by the symmetrical optimum criteria, so the time constant T_{ea1} is given by:

$$K_{cm2} = 1 \tag{5.49}$$

$$T_{ea1} = T_{pE2} = 4T_{pa2}\left(1 + 2\frac{T_{pa2}}{T_{a2}}\right) \tag{5.50}$$

The time constant T_{pa2} is given by the time constant T_{cm2} from in the internal controller loop, added with the other small time constants in the feedback loop. The filter time constants to obtain the average value of $U_{dc2(i)}$ is introduced here.

$$T_{pa2} = T_{cm2} + T_{fs} + T_{filt} \tag{5.51}$$

The other time constant is given by the time constant of the internal control system.

$$T_{a2} = T_{l1} = L_{line} \tag{5.52}$$

The transfer function of the system that has to be controlled, is called $G_{sb2}(s)$. It is a transfer function of integral behavior:

$$G_{sb2}(s) = \frac{1}{sT_{I2}} = \frac{1}{sC_{dc2}} \tag{5.53}$$

By knowing all parameters, the external controller can be designed, represented by the transfer function $G_{R2}(s)$. Due to the integral behavior of the voltage on the capacitors, once again the symmetrical optimum [30] is used to calculate the controller parameters. The two time constants of the controller are:

$$T_{n2} = 4 \cdot T_{pE2} \tag{5.54}$$

$$T_{i2} = \frac{8K_{cm2}{T_{pE2}}^2}{T_{I2}} \tag{5.55}$$

And the parameters of the controller G_{R2} are given with:

$$K_{i2} = \frac{T_{sample}}{T_{i2}} \tag{5.56}$$

$$K_{p2} = \frac{T_{n2} - \frac{T_{sample}}{2}}{T_{i2}} \tag{5.57}$$

All the parameters for the cascaded controller are now calculated and can be used for the simulation.

Controller for the independent feeding voltages of the 4Q-converters Unfortunately, another controlling element is necessary to control the multilevel converter system. All the voltages $U_{dc2(i)}$ have to be controlled individually. It is known that all the voltages $U_{dc2(i)}$ are oscillating with twice the line frequency. But the DC component of these voltages $\overline{U}_{dc2(i)}$ have to be stabilized to a fixed value. To achieve this aim, all the average values of the currents $I_{ch2(i)}$ have to be equal to the currents $\overline{I}_{dc2(i)}$. In the present implementation, all the 4Q-converters see the same modulation function $k \cdot V_{ref}$. This means in theory that all the average values of the currents $I_{ch2(i)}$ will be the same. On the other side, the DC-DC converters have all the same set value on the primary side, so the current $\overline{I}_{dc2(i)}$ will be the same, if all the voltages $U_{dc2(i)}$ are equal. But there are two points that have to be taken into account:

- The voltages $U_{dc2(i)}$ cannot all have the same value, measurement equipment, measurement noise and different capacitor values due to normal imperfection of the production will always cause different DC components of the voltages $\overline{U}_{dc2(i)}$. This means the currents $\overline{I}_{dc2(i)}$ will not be all the same.

- Although the 4Q-converters all see the same modulation function, the average value of the currents $I_{ch2av(i)}$ cannot be perfectly the same. Different turn-on and turn-off times of the power semiconductors and phase-shift of the carrier modulation functions will cause different switch patterns for each 4Q-converter. This means that every current $I_{ch2(i)}$ will be different.

These two facts make the control of the individual voltages $U_{dc2(i)}$ necessary. The control can be done in two ways:

- The DC-DC converters can have a variable set values $I_{dc1(set)}$. This would cause a variable secondary side current $\overline{I}_{dc2(i)}$, which can be adapted to rise or fall the value of the voltage $\overline{U}_{dc2(i)}$. But the sum of all $\overline{I}_{dc1(i)}$ must be controlled equal to I_{mot}, in order to keep the DC-link voltage stabilized. A controller structure is proposed where controller adapts the set value $I_{dc1(set)}$ generated from the motor current I_{mot} divided through the number of ML steps n. The controller input is the voltage error of $\overline{U}_{dc2(i)}$. But all the current set values have to be adapted by a second controller in order to avoid that the sum of the set values is different from I_{mot}. The entire controller structure is proposed in Figure (5.17).

  The disadvantage is the fact that the DC-link voltage U_{dc1} cannot be controlled directly. The DC-link capacitor is very small, so the DC-link voltage U_{dc1} is easily disturbed.

- By modifying the global modulation function $k \cdot V_{ref}$ for each 4Q-converter to an independent modulation waveform $k_{(i)} \cdot V_{ref(i)}$, the power flow through each 4Q-converter can be controlled. If the amplitude of the partial ML-converter voltage $U_{conv(i)}$ is risen by the use of the partial modulation function $k_{(i)} \cdot V_{ref(i)}$, the current $I_{ch2(i)}$ becomes higher. This is shown in Equation (5.22). The disadvantage of this control method is that the creation of unequal partial voltage $U_{conv(i)}$ cause more harmonics on the line current I_{line}

In this report, the second method is implemented: the modulation function $k \cdot V_{ref}$ is adapted for each 4Q-converter by the controllers $G_{R3(i)}(s)$. There is no other local

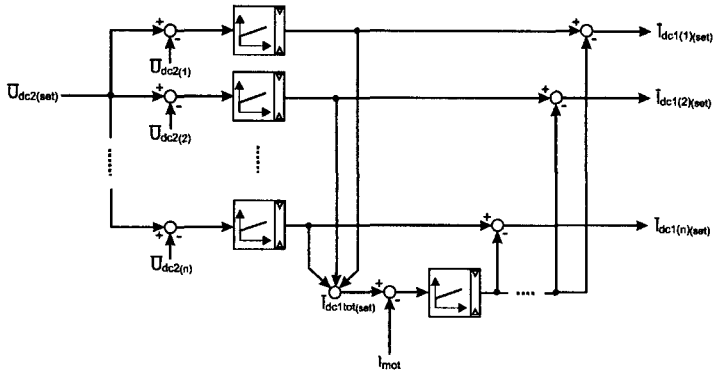

Figure 5.17: Variable set value for all DC-DC converters

controller interacting for each 4Q-converter, while each DC-DC converter already has its voltage controller $G_{R5(i)}(s)$. The proposed control system is given with the Figure (5.18).

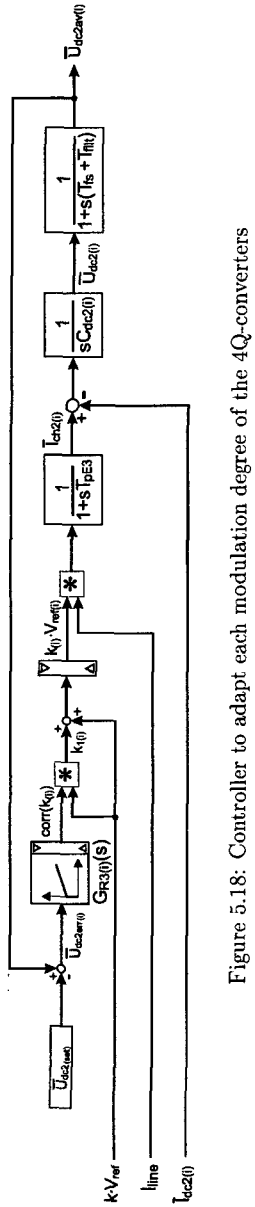

Figure 5.18: Controller to adapt each modulation degree of the 4Q-converters

The system is composed of a set of ordinary PI controllers $G_{R3(i)}$ with two limitations. The transfer function of the controller processing system is given by the equation below:

$$G_{cm3}(s) = \frac{K_{cm3}}{1 + sT'_{pE3}} \tag{5.58}$$

The amplification is not shown in the box of the Figure (5.18) because the amplification is done by the multiplication of the global modulation function $k \cdot V_{ref}$ with the output of the controller $corr(k_{(i)})$, which is the correction value for the modulation function. The value $corr(k_{(i)})$ is limited to the boundaries $[-1, 1]$, but actually the value remains very low, because only slight corrections of the modulation function are necessary to control the voltage $U_{dc2(i)}$ (around 1% to 2%). Once again the controller output is multiplied to the modulation function $k \cdot V_{ref}$ and afterwards added to $k \cdot V_{ref}$, in order to keep the same waveform and to change the DC value $corr(k_{(i)})$ to an alternative, sinusoidal waveform. The amplification is:

$$K_{cm3} = \frac{P_{mot}}{U_{line}} \tag{5.59}$$

The small time constant shown in the box of Figure (5.18) is not the same as shown in the Equation (5.58). The delay times of the low-pass filter have to be considered and added to the time constants of the processing system. So the time constant T'_{pE3} is given by the following equation:

$$T'_{pE3} = \frac{T_{sample}}{2} + T_{cm3} + T_{filt} + T_{fs} \tag{5.60}$$

The delay due to the modulator is given with the element T_{cm3}. It is different from the time constant used for the global controller, because the modulation frequency of a single 4Q-converter f_s is n times smaller than the overall modulation frequency.

$$T_{cm3} = \frac{1}{2 \cdot f_s} \tag{5.61}$$

The transfer function for the system is of course an integration element:

$$G_{s3}(s) = \frac{1}{sT_{I3}} = \frac{1}{sC_{dc2}} \tag{5.62}$$

Of course, the controller time constants are designed by using the symmetrical optimum:

$$T_{n3} = 4 \cdot T_{pE3} \tag{5.63}$$

$$T_{i3} = \frac{8K_{cm3}{T_{pE3}}^2}{T_{I3}} \tag{5.64}$$

And the parameters of the controllers $G_{R3(i)}$ are given with:

$$K_{i3} = \frac{T_{sample}}{T_{i3}} \tag{5.65}$$

$$K_{p3} = \frac{T_{n3} - \frac{T_{sample}}{2}}{T_{i3}} \tag{5.66}$$

An important component of the individual 4Q-converter controllers is the filter to get rid of the alternative component of the voltage U_{dc2}. It is important that this filter is able to compute the DC component without a high time delay and with a correct dynamic behavior. Instead of taken classical bandpass filters, which have high time constants, a FIR filter of an order of at least $n_d > 20$ is taken. The filter is presented in the Figure (5.19):

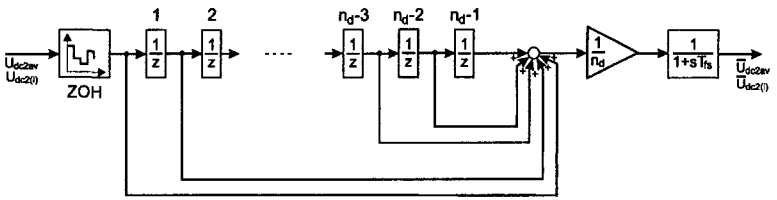

Figure 5.19: Filter used to avoid the oscillation at twice the line frequency

At the entrance of the filter, there is a zero order hold element in order to sample the time-continuous values of the measured voltage $U_{dc2(i)}$. This zero-order hold is not needed if the whole controller is implemented in a digital system and if the following equation is respected:

$$n_d = \frac{2}{T_{sample} f_{line}} \tag{5.67}$$

In this case, the systems sampling time is in the same time as the delay time of the filter elements, and no additional sampling element is needed. In the presented implementation the sampling time is $200\mu s$ and n_d is 20 and should be 600 to respect the Equation (5.67). The filter equation is given below:

$$\overline{U}_{dc2av(i)}(k) = \frac{1}{n_d} \sum_{i=0}^{n_d} U_{dc2av(i)} \left[(k - i \cdot n_d) \cdot \frac{1}{f_{line} n_d} \right] \tag{5.68}$$

The value k represents the discrete time steps. Due to the additional sampling to generate the filtered voltage, there is an additional time constant to smooth the filtered voltage output on order to get a continuous function within the the faster system sampling time T_{sample}.

$$G_{fs}(s) = \frac{1}{1 + sT_{fs}} \tag{5.69}$$

The time constant T_{fs} should be chosen equal to the high sampling frequency:

$$T_{fs} = \frac{1}{f_{line} n_d} \tag{5.70}$$

The next Figure (5.20) shows the oscillating voltage $U_{dc2(i)}$ and the equivalent filtered voltage $\overline{U}_{dc2(i)}$.

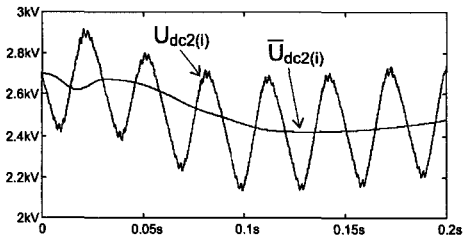

Figure 5.20: DC voltage $U_{dc2(i)}$ filtered and unfiltered

It can be seen that there is a small transient behavior at the beginning of the measurement. But after a full period, in this case $\frac{1}{2f_{line}}$, the filtered voltage $\overline{U}_{dc2(i)}$ follows the original value with a small delay and represents its DC component.

Active current filtering controller An active filtering is done in order to eliminate particular current harmonics found on the line current, but also to eliminate the DC-component I_{lineDC} of the line current. In this control subsystem, the fundamental current is not analyzed or modified. These harmonics are caused by different reasons:

- The closed loop behavior of the entire control system can introduce harmonics
- In reality, the line voltage U_{line} is mostly not sinusoidal and contains itself a lot of harmonics, due to old locomotives running with phase-cutting converters based on thyristor semiconductors. If the line voltage is not sinusoidal, automatically harmonics are introduced into the current.
- The oscillating DC voltages $U_{dc2(i)}$ will introduce harmonics of a low order. Also the fact that these voltages will not all have perfectly the same DC level causes additional harmonics.
- The resulting switching frequency $n \cdot f_s$ will introduce high-order harmonics. These frequencies are too high to be filtered by the active filter.

For all traction applications, it is very important to reduce all harmonics to a maximum. This is especially due to the normalization regulation of all countries, with the aim to avoid interference with telecommunication frequencies. The proposed system for the active filtering is given in the Figure (5.21)

To extract the amplitudes of the current harmonics $\hat{I}_{harm(i)}$ from the time base function I_{line}, the algorithm of the discrete Fourier transformation (DFT) is used. The DFT

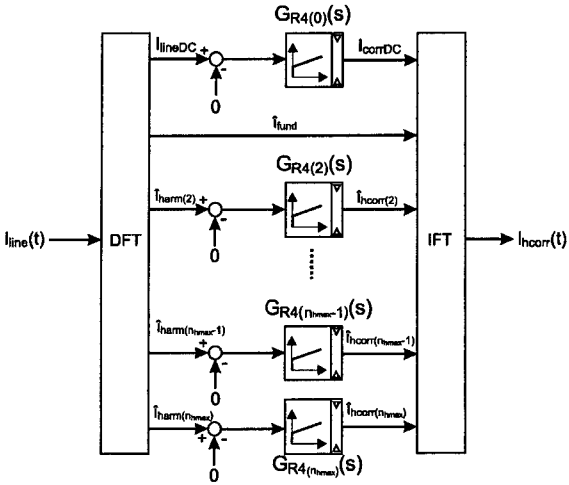

Figure 5.21: DFT analysis of the line current with DC current and harmonics cancellation

algorithm can be used to calculate each amplitude of the harmonics separately. If the sampling period used for the DFT algorithm is synchronous with the line frequency, the result of the DFT will be a set of all desired harmonic amplitudes. The two main parameters of the DFT are calculated by the following equations:

$$a_{n(harm)} = \frac{2}{n_{DFT}} \sum_{i=0}^{n_{DFT}-1} I_{line}(i \cdot T_{sample}) cos\left(n_{harm} \frac{2\pi}{n_{DFT}} i\right) \quad n = [0..n_{hmax}] \quad (5.71)$$

$$b_{n(harm)} = \frac{2}{n_{DFT}} \sum_{i=0}^{n_{DFT}-1} I_{line}(i \cdot T_{sample}) sin\left(n_{harm} \frac{2\pi}{n_{DFT}} i\right) \quad n = [1..n_{hmax}] \quad (5.72)$$

The parameter n_{hmax} defines the maximal order of the amplitude that has to be calculated. The parameter n_{DFT} indicates the number of sampling periods on a period of the fundamental frequency. It is defined by:

$$n_{DFT} = \frac{1}{f_{line} T_{sample}} \quad (5.73)$$

By using the parameter a_0, the DC component of the current is directly found. It can be seen that for the DFT algorithm, a sine wave and a cosine wave are needed being in phase with the analyzed current I_{line} and of course being in phase with the line voltage U_{line}. These two functions are generated by a phase locked loop (PLL). In the Figure (5.13) it can be seen at (4) and (10), that the PLL results are feed-forwarded to the DFT and the IFT. The final result of the DFT algorithm can be found by employing the next Equation:

$$\hat{I}_{harm}(i) = \frac{a_0}{2} + \sum_{n_{harm}=1}^{n_{hmax}} \left[a_{n(harm)} cos(n_{harm} \cdot i) + b_{n(harm)} sin(n_{harm} \cdot i)\right] \quad (5.74)$$

The function received from this Equation (5.74) is a set of amplitudes for each desired harmonic. The index i represents the order of the harmonic, so the frequency of the harmonic is $i \cdot f_{line}$. These amplitudes are subtracted from the desired set value $\tilde{I}_{harm(set)}$ and the error is introduced to a standard PI controller as shown in Figure (5.16). After the PI controller, the correction values for the currents have to be re-transformed into the time base. This is done by using the inverse Fourier transformation algorithm. The Equation describing this algorithm is given in Equation (5.75):

$$I_{harm(corr)}(i \cdot T_{sample}) = \frac{a_0}{2} + \sum_{i=1}^{n_{hmax}} \left[a_n cos\left(n \frac{2\pi}{T_{sample}} \cdot i \right) + b_n sin\left(n \frac{2\pi}{T_{sample}} \cdot i \right) \right] \quad (5.75)$$

After using Equation (5.72) to the set of calculated parameters $[a_n, b_n]$, the result is the time-discrete function of the current set value $I_{harm(corr)}$. The index i here represents an incremental value for the discrete timebase, sampled with the period T_{sample}.
The Equations for the DFT and IFT show that the harmonic results are given after a integration of the current over an entire period, with n_{DFT} sampling values. This means that the DFT-IFT combination cannot immediately give results out, one entire period must be over until the harmonic response is available. This is the additional dead time coming from the controller loop from the active filter controller.

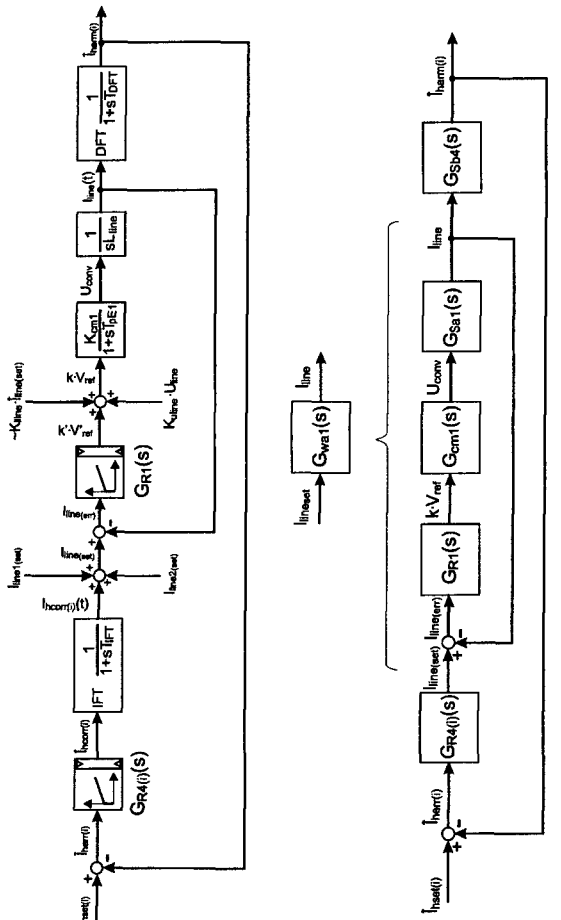

Figure 5.22: Cascaded controller system to control active harmonics filtering

To design the PI controller parameters, this dead time of a period has to be respected. The Figure (5.22) shows the structure of the cascade controller. The internal controller is the current controller G_{R1} the same as shown in Figure (5.14). The controller has been designed with the Equations (5.46) and will keep the same parameters. For the external control loop, this transfer function is seen like a function of a small time delay without any amplification, but will not be the same as presented in Equation (5.48). The internal controller was designed using the symmetrical optimum, so it can be found:

$$G_{wa4}(s) \cong \frac{1}{1+sT_{ea4}} = \frac{K_{cm4}}{1+sT_{pE4}} \tag{5.76}$$

The internal controller was designed by the symmetrical optimum criteria, the time constant T_{ea4} is given by:

$$T_{ea4} = 4T_{pa4}\left(1+2\frac{T_{pa4}}{T_{a4}}\right) \tag{5.77}$$

The time constant T_{pa4} is given by the time constant T_{cm2} from in the internal controller loop, added with the other small time constants in the feedback loop. The time constant of the external controller loop comes from the re-transformation algorithm of the IFT, which takes one sampling period:

$$T_{pa4} = T_{cm2} + T_{IFT} = T_{cm2} + T_{sample} \tag{5.78}$$

The other time constant is given by the time constant of the internal control system, as been seen before in Equation (5.52):

$$T_{a4} = T_{I1} = L_{line} \tag{5.79}$$

The transfer function of the system that has to be controlled, is called $G_{sb4}(s)$. It is a transfer function with the behavior of a PT_1-Element, but is approximated by an integral transfer function:

$$G_{sb4}(s) = \frac{1}{1+sT_{DFT}} = \frac{1}{1+s\frac{1}{f_{line}}} \cong \frac{1}{s\frac{1}{f_{line}}} = \frac{1}{sT_{I4}} \tag{5.80}$$

By knowing all parameters, the set of external controllers can be designed, represented by the transfer function $G_{R4(i)}(s)$. The system to be controlled is the integration time constant of the DFT algorithm. This time is usually equal to the line voltage period. This element does not really have an integral behavior, but it can be taken as integral element with the time constant T_{DFT} to use the symmetrical optimum design criteria to calculate the controller parameters. The two time constants of the controller are:

$$T_{n4} = 4 \cdot T_{pE2} \tag{5.81}$$

$$T_{i4} = \frac{8K_{cm2}{T_{pE2}}^2}{T_{I4}} \tag{5.82}$$

And the parameters of the controller $G_{R4(i)}$ are given with:

$$K_{i4} = \frac{T_{sample}}{T_{i2}} \tag{5.83}$$

$$K_{p4} = \frac{T_{n2} - \frac{T_{sample}}{2}}{T_{i2}} \tag{5.84}$$

Due to the addition of the values coming from the current controller G_{R1} and the direct introduction of the perturbation values shown with Equation (5.28), the obtained controller values are attenuated by the factor 3:

$$K_{i4} = \frac{K_{i4}}{3} \tag{5.85}$$

$$K_{p4} = \frac{K_{p4}}{3} \tag{5.86}$$

All the parameters for the cascaded controller are now calculated an can be used for the simulation.

Simulation results

The entire multilevel system shown in the Figure (5.11) has been implemented using MATLAB/SIMULINK software in order to verify if the proposed control scheme presents sufficient results. The parameters chosen for the simulated system are given in the Table (5.6). The converter consists of 10 multilevel steps and is coupled to a typical railway catenary found in Switzerland, Austria and Germany ($16\frac{2}{3}$Hz, $15kV$). The same principle would also work on the other European catenaries, like the French 50Hz, 25kV systems. Therefore more multilevel steps have to be foreseen.

On the capacitors $C_{dc2(i)}$ a maximal voltage oscillation of 400V is accepted in the full power operation. Of course this oscillation is proportional to the required power. So the capacitors are designed by using Equation (5.26). The DC component is set at $2.7kV$, so the maximal value will not exceed $2.9kV$. The first simulations shown are tested in order to show the necessity of such a complex converter system.

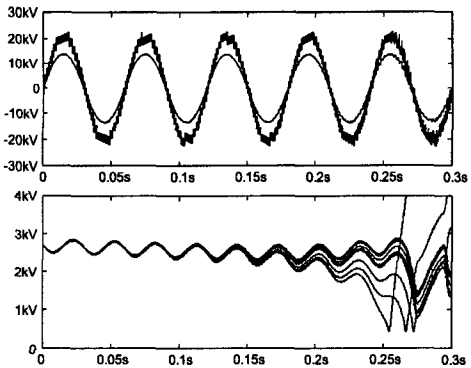

Figure 5.23: Destabilized voltages $U_{dc2(i)}$ due to reduced control system

n	10	Number of converter steps
$C_{dc2(i)}$	$\cong 2.65mF \pm 5\ \%$	Intermediary capacitors
C_{dc1}	$500\mu F$	DC-link capacitor
$\Delta U_{dc2(i)}$	$400V$	Voltage oscillation
$\overline{U}_{dc2(i)}$	$2.7kV$	DC component U_{dc2}
P_{mot}	$3MW$	Motor power, maximal value
U_{line}	$15kV$	Effective line voltage
f_{line}	$16\frac{2}{3}$Hz	Line frequency
L_{line}	$25\mu H$	Line inductance
R_{line}	$100m\Omega$	Line resistance
T_{sample}	$200\mu s$	Sampling time
f_s	50Hz	Switching frequency 4Q
f_p	8kHz	Switching frequency DC-DC
$\tau_{blank(4Q)}$	$3\mu s$	Blanking time 4Q
τ_{blank}	$4\mu s$	Blanking time DC-DC
$L_{\sigma tot}$	$65\mu H$	Decoupling inductance DC-DC
T_{r2}	$65\mu s$	Measurement delay
n_d	20	Order of the FIR filter

Table 5.6: Numerical values for the simulated system

The Figure (5.23) shows the multilevel converter in action without the controllers $G_{R3(i)}$ to control the independent 4Q-converter modulation degree and the controller G_{R2} to control the overall power flow. It can be seen that all the voltages are decreasing, due to the fact that the motor is consuming more power than the power that is delivered from the 4Q-converters. This is usually avoided with the controller G_{R2}. Of course all the voltages $U_{dc2(i)}$ do fluctuate due to imperfections in the converter discussed before.

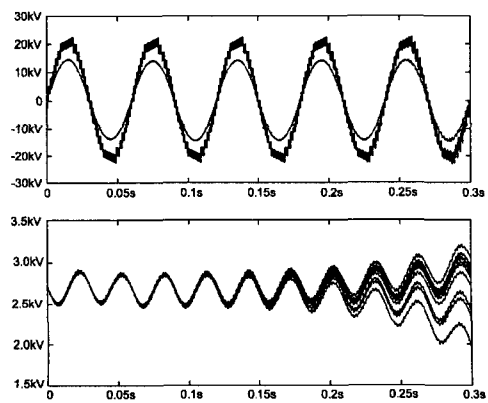

Figure 5.24: Average value of $U_{dc2(i)}$ stabilized thanks to overall power controller

The Figure (5.24) shows the multilevel converter without trap circuit, but this time an overall power flow controller G_{R2} has been implemented. Immediately it can be seen that the average value of the voltages $U_{dc2(i)}$ is stabilized on the set value $U_{dc2av} = 2.7kV$, but still the voltages themself fluctuate compared to each other. Therefore the combination of the set of controllers $G_{R3(i)}$ is necessary with the controller G_{R2}.

Finally, the converter is simulated with the full controller system. It is interesting to see that the converter voltage U_{conv} is composed of independent DC voltages $U_{dc2(i)}$, which are not constant. Due to the powerful control algorithm, the current I_{line} is nearly sinusoidal. Another interesting observation is the DC-link voltage U_{dc1}. In spite of the very small capacitor value, it remains perfectly stable. This voltage is controlled by $n = 10$ series-connected DC-DC converters.

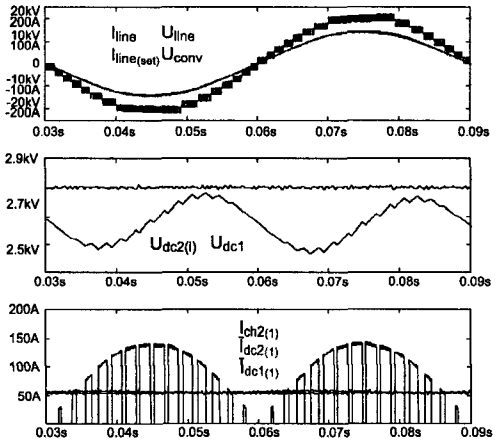

Figure 5.25: Entire electrical waveforms of the ML-converter without trap circuit

The last observation can be made on the currents $\overline{I}_{dc2(i)}$ and $\overline{I}_{dc1(i)}$. The uncontrolled current $\overline{I}_{dc2(i)}$ is a superposition of a DC component containing a oscillation at $2 \cdot f_{line}$. This oscillation is due to the fact that the DC-DC converter transfers a constant power, while the feeding voltage $U_{dc2(i)}$ are oscillating. Therefore $\overline{I}_{dc2(i)}$ will oscillate of course with a 180^o phase shift. $\overline{I}_{dc1(i)}$ is imposed by the DC-DC converter controller and stays constant.

The next simulations done for the ML-converter concerned the step response of the entire system. There are many controllers, so many parameters can be tested by changing immediately a set value. The three most important situations have been simulated and the stability of the system has been checked.

- The motor power is at $P_{mot} = 50\%$. The power is set immediately to 100% when the line current I_{line} is maximal.
- The motor power is at $P_{mot} = 50\%$. The power is set immediately to 100% when the DC feeding voltages $U_{dc2(i)}$ are minimal.
- The motor power is constant at 100%. The DC-link voltage U_{dc1} is reduced from $2.8kV$ to $2.2kV$ in order to start the motor.

The simulation results are shown in the next Figures. Step responses on the DC feeding voltages are not simulated, because this is not a typical situation occurring with the ML-converter system. By starting up the locomotive, usually the DC feeding voltages $U_{dc2(i)}$ are zero. Through an auxiliary converter coupled to the DC-link C_{dc1}, the DC-link voltage is established. Afterwards, all the DC feeding voltages are created by transferring power from the DC-link to all DC feeding voltages on $C_{dc2(i)}$. This can be done with the DC-DC converters in reverse power operation. Once all the DC voltages are created, the locomotive can be connected to the catenary.

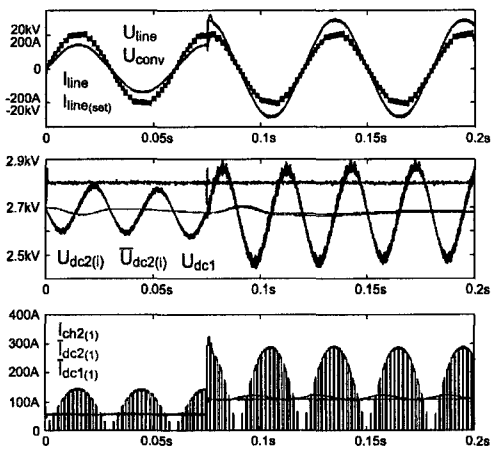

Figure 5.26: Step response changing the power at full line current I_{line}

The simulation shown in Figure (5.26) shows a step on the line current I_{line}, the set value is doubled at the moment $t = 75ms$. Of course the same happens with the motor current I_{mot}, which has doubled its value. The sum of the currents $\overline{I}_{dc1(i)}$ follows the current I_{mot} in order to stabilize the DC-link voltage U_{dc1}. There is only a small voltage oscillation on U_{dc1} of about $70V$ amplitude, which is 2.5% of the voltage value. The line current I_{line} is very quickly stabilized (after 5ms, which is about $\frac{1}{12}$ of the period). The

current overshoot is about 20% of the nominal value. The current reaches for a small instance $337A$. The influence on the oscillation of the DC feeding voltages $U_{dc2(i)}$ remains minimal. This is especially due to the fact that the current I_{line} is maximal when the voltages $U_{dc2(i)}$ are crossing their average value. It can be seen that the oscillation caused on the DC component $\overline{U}_{dc2(i)}$ is negligible.

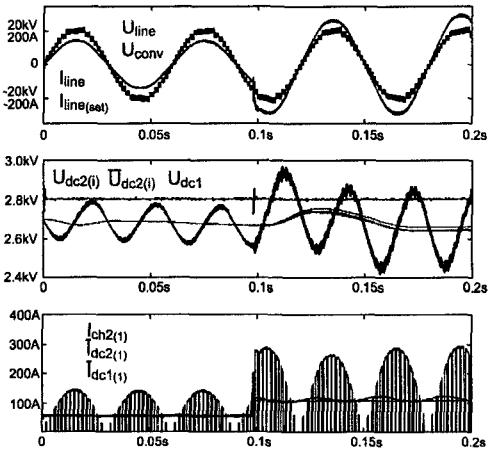

Figure 5.27: Step response changing the power at lowest point of DC feeding voltage $U_{dc2(i)}$

The Figure (5.27) shows a simulation, where the current set value for I_{line} is suddenly risen by 100%, but this time while the DC feeding voltages $U_{dc2(i)}$ are minimal. The time chosen for the step response is $t = 98.5ms$. The influence on the DC-link voltage U_{dc1} is minimal, thanks to the decoupling of primary and secondary side by the DC-DC converter controllers. Also the line current I_{line} has a very short transient, so the current follows the set value current only after less than $5ms$. But the step response causes an superposed oscillation on the DC feeding voltages, caused by the fact that the power is risen, when the DC feeding voltages $U_{dc2(i)}$ are minimal. This causes automatically a different DC component of this voltage, which does not correspond to the set value of $2.7kV$. But the controller of the 4Q-converters G_{R3} re-adapts the DC components at $2.7kV$. The voltage is stabilized after about $200ms$.

$\hat{U}_{harm(3)}$	20% of $\hat{U}_{line}$
$\hat{U}_{harm(5)}$	8.5%
$\hat{U}_{harm(7)}$	7.5%
$\hat{U}_{harm(9)}$	5%
$\hat{U}_{harm(11)}$	4.5%

Table 5.7: Amplitude values of the line voltage harmonics

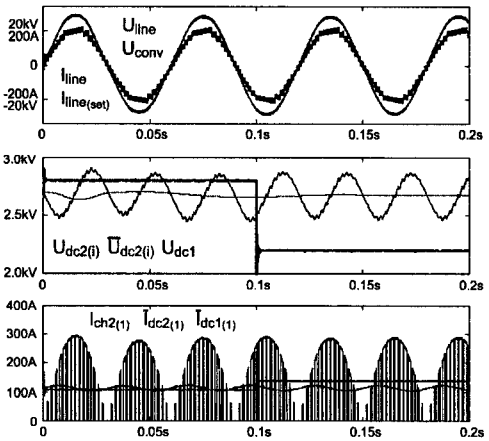

Figure 5.28: Step response changing the DC-link voltage

The last simulation in Figure (5.28) with step responses on the set values are done on the DC-link side of the converter system. The DC-link voltage is reduced from $2.8kV$ to $2.2kV$, without reducing the motor power P_{mot}. Of course this means that the current I_{dc1} has to be risen in order to provide the same power to the motor. This simulation shows that it is possible to vary the DC-link voltage without having any impact on the line current I_{line} and the DC feeding voltages $U_{dc2(i)}$. A big oscillation on the current $\overline{I}_{dc1(i)}$ (80% overshoot) and the voltage $U_{dc2(i)}$ can be observed. This is especially due to the fact that all controllers have been designed by the symmetrical optimum, which shows good performance towards the step response of the perturbation value, but not towards the step response of the set values.

The Figure (5.30) shows the two line voltages U_{line} used for the simulation and the line currents. Of course the voltages are not chosen sinusoidal. The first line voltage waveform is taken as worst case for the multilevel system without trap circuit. The Table (5.7) shows the harmonic content of this voltage. The harmonics are chosen in a way to create a local maximal voltage near the phase angle $\alpha_{Udc2(min)}$. At this phase angle, the supply voltages for the 4Q-converter is the smallest (at 2.5kV). The voltage waveform is created by a simple addition of these waveforms, without any phase shift angle. The voltages are visualized in Figure (5.30). It can be seen that the converter voltage U_{conv} is composed of all the $n = 10$ mulitlevel voltage steps. The other voltage generated is a sinusoidal waveform, but there is an voltage limitation at 95% of the amplitude. This generates additional harmonics in the current. The converter voltage U_{conv} is generated only by using $n = 8$ steps, due to the more or less sinusoidal line voltage U_{line}. The Figure (5.29) shows the function generator creating this voltage U_{line}.

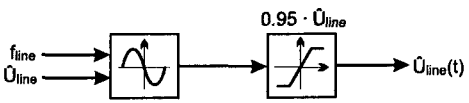

Figure 5.29: Generation of a non-ideal line voltage

It is interesting to see the uncontrolled and oscillating supply voltages. There is a point where the sum of 10 voltage steps (at 72ms) is smaller than the sum of 9 voltage steps (at 78ms). The currents are supposed to be sinusoidal. The resulting switching frequency can be seen at 5kHz.

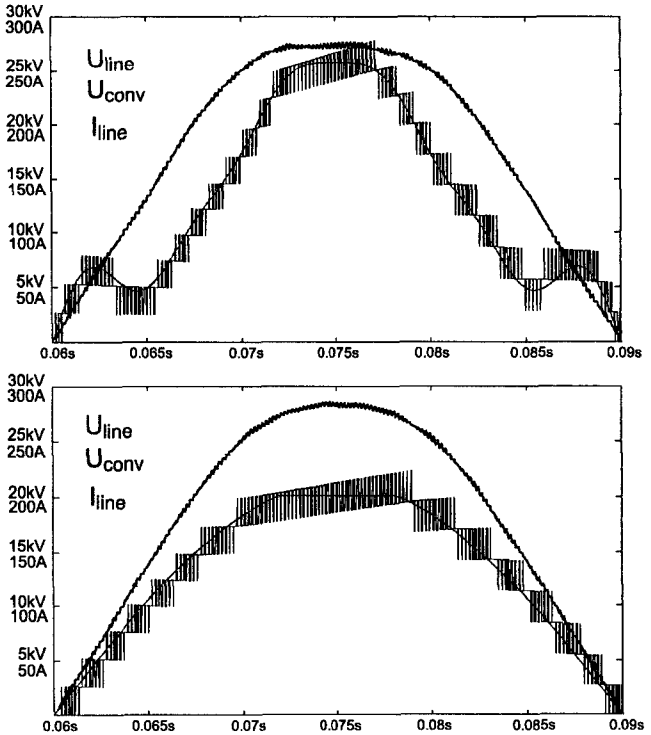

Figure 5.30: The two simulated voltage waveforms U_{line}

With the first line voltage U_{line} containing many harmonics, the current cannot be controlled in exactly the same quality as in the second one. On the current waveform it can be seen that there is a low-order harmonic content.

The next simulation in Figure (5.31) has been done in order to analyze the harmonic contents of the current. The line voltage U_{line} with the flat has been taken. The current harmonic filters have been implemented. The upper graphs shows the FFT analysis of the current harmonics up to 6kHz. This has been done to show the harmonics of the resulting switching frequency. The passive filter for these harmonics is disabled. It can be seen that none of these high-order harmonics have an amplitude higher than 0.5A. The middle graphs show the low-order harmonics, which are actively filtered. To simplify the simulations, the implemented controller was a simple proportional controller without any integral part. The harmonics up to the 11th order were filtered. None of the low-order harmonics have an amplitude above 1A.

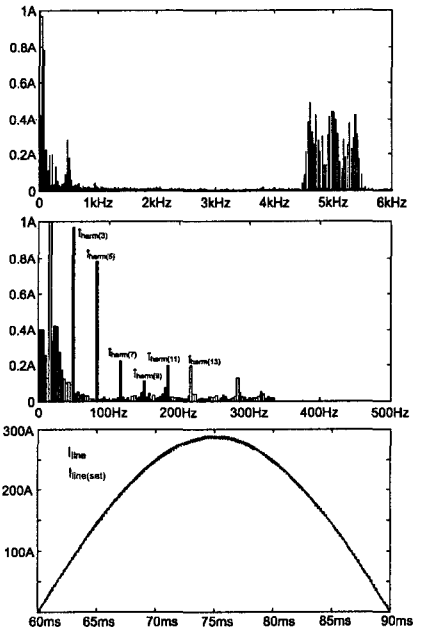

Figure 5.31: FFT of the line current, with active filtering of the current

By implementing a real PI-controller, the steady-state error of the harmonics would be better eliminated and in this way would even show better results.

5.1.2 Multilevel converter system with trap circuit

The second multilevel converter system examined is a classical concept with trap circuit filter. The trap circuit must guarantee that the motor converters are always fed by a constant voltage U_{dc1}. In the previous multilevel system, this voltage was controlled actively. In this multilevel system, a high low-frequency filter shall avoid a high voltage oscillation on the DC-link. The DC-DC converters are in this case used to control each 4Q-converter feeding voltage $U_{dc2(i)}$. In this way, the capacitors between the DC-DC converters and the 4Q-converters $C_{dc2(i)}$ can be reduced to a minimum, depending on the performance of the controller G_{R5} of the DC-DC converter. The 4Q-converters will always see a stabilized voltage, which will be applied to the high-voltage catenary. Of course this is an advantage to avoid the generation of harmonics. This reduction of the capacitors presents an important advantage: the capacitors are installed on the high-voltage part of the converter system, where a complicated an high-cost insulation box must isolate these elements from the ground. This isolated part of the converter system should be as small as possible in order to avoid high costs for the insulation structure. The disadvantage is the use of big and heavy filter elements for the DC-link and a DC-link voltage, which is not easy to control.
The next Figure (5.32) shows the schematics of the traction converter with n steps with the trap circuit:

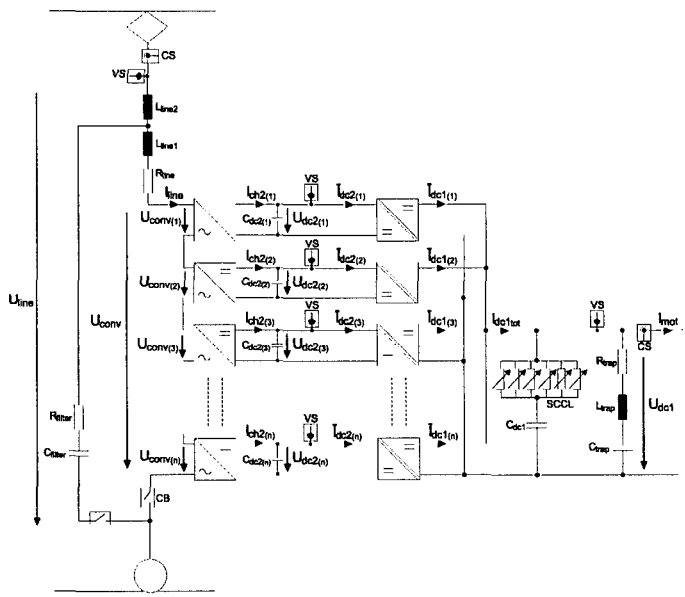

Figure 5.32: Multilevel system schematics with trap circuit on the DC-link

Once again a real implementation of this converter system would need about 10-14 steps to connect the converter to a 15kV AC catenary. The DC-link capacitor C_{dc1} is

set in series with 6 short-circuit current limiters (SCCL). For $2mF$ of capacitance, one SCCL is needed.

Control system

For the multilevel system, a control structure is proposed using four controller systems (instead of five as proposed before for the ML-converter without trap circuit). The set value for the system is the motor power P_{mot} or just the motor current I_{mot}. The following tasks are fulfilled by the controller structure:

- The current I_{line} must be a sine-wave function with very few harmonics and has to be in phase with the voltage U_{line}. The current should contain no DC component.
- All the voltages $U_{dc2(i)}$ and the DC-link voltage U_{dc1} shall be as stable as possible. The oscillation with $2 \cdot f_{line}$ should be reduced to a maximum.
- The motor current I_{mot} must be able to make steps and must be able to change its sign value at any time without destabilizing any value of the system (Especially the DC-link voltage U_{dc1}).

The overview of the proposed control system is given in Figure (5.33). The control system is less complicated than the controller for the ML-converter with trap circuit. In this case, four controller levels can be identified:

- The line current controller G_{R1}, combined with the direct introduction of all line values using the trigonometric phasor relations given in Figure (5.6). The controller is a simple PI-controller.
- The power flow controller G_{R2} in cascade with the line current controller. If the motor does not require the same power as taken from the line, this controller adapts the demanded power. This controller can take influence on the value of the voltage on the DC-link.
- The active harmonic cancellation controllers $G_{R4(i)}$. These set of controllers compute an adapted current set value in order to eliminate all the chosen low-order harmonics and the DC component found on the line current I_{line}.
- The controller of the DC-DC converters, in order to stabilize the output voltage U_{dc1}. This controller is not described in this chapter (see chapter Control of DC-DC converter)

There is no controller regulating each modulation degree k_i of the 4Q-converters. Every 4Q-converter will see exactly the same modulation degree. Although there is a low-frequency filter, there will always be an oscillation in the voltage U_{dc1}. The controllers $G_{R4(i)}$ are responsible for the active current filtering. The set values for the control system are now: The motor current $I_{mot(set)}$ setting the overall power of the system, the DC component of the DC-link voltage $\overline{U}_{dc1(set)}$ and finally the values of the current harmonics of a certain order $I_{harm(set)}$. In any case, not all the current harmonics can be filtered actively. The controller of the DC-DC converters have an internal set value $U_{dc2(set)}$, determining the controlled output voltage $U_{dc2(i)}$.

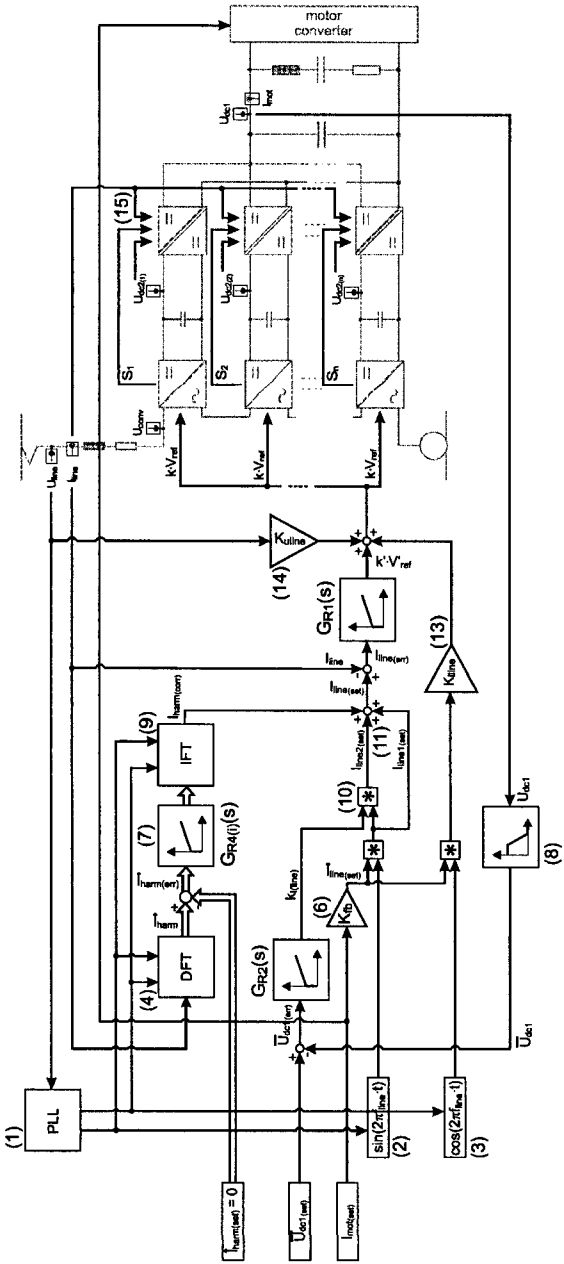

Figure 5.33: Overview of the controller for the system with trap circuit

DC-DC controller strategy In the ML-structure with trap circuit, the DC-link voltage U_{dc1} was controlled by all the n DC-DC converters. The DC-DC converters work independently of the other controllers. In this control system, The DC-DC converters stabilize the voltage $U_{dc2(i)}$. It has to be mentioned that to control the voltage $U_{dc2(i)}$, the DC-DC converter has to generate a current $\overline{I}_{dc2(i)}$, which has to be the same as the current $I_{ch2(i)}$. The input parameters for this controller is the voltage U_{dc1} and the load current $I_{ch2(i)}$. This is shown in the system overview in Figure (5.33) at function block (15). For this aim, not all the currents $I_{ch2(i)}$ have to be measured. If only the current I_{line} is measured and the switch pattern of the concerned 4Q-converter is known, the current $I_{ch2(i)}$ can be recalculated by respecting the Equation (5.21).
There are three possibilities how to control the 4Q-converter feeding voltages $U_{dc2(i)}$. A result of the different control possibilities is shown in Figure (5.34), where the control methods have to be implemented into the controller system.

- Due to the fast response of the DC-DC converter generating a current I_{dc2}, the exact waveform of the current I_{ch2} can be generated in order to stabilize the voltage U_{dc2} (In the Figure (5.34), the voltage is shown in the red color with a peak-to-peak oscillation of 100V). This has the advantage that the capacitors C_{dc2} can be reduced to a very small value (750 μF). But the DC-DC converter changes the set value with the current pulse pattern, which corresponds to the switching frequency of a 4Q-converter $2 \cdot f_s$, in this example 500Hz. This way of changing the set in any way more losses. The current I_{dc2} generated negative current peaks, which cause more losses than the control of a simple DC current.

- The DC-DC converter can generate the waveform of the current $\overline{I}_{ch2}$, which is the sliding average value of the current. This is a current with a DC-component I_{ch2dc} and a superposed oscillation with two times the line frequency $2 \cdot f_{line}$, in this example $33\frac{1}{3}$Hz. The voltage U_{dc2} is shown in Figure (5.34), shown in the blue colour. The peak-to-peak oscillation is about 200V. To have the same voltage stability, the value of capacitors C_{dc2} have to be doubled. It should not be forgotten that the DC-DC converters are voltage-controlled. Therefore to implement this controller type, the measured value of U_{dc2} must be filtered by a low-pass filter with a cut-off frequency at $2 \cdot f_s$. Otherwise the controller will immediately try to correct the voltage oscillation caused by the switching.

- The DC-DC converter can generate only the DC-component I_{ch2dc} of the current I_{ch2}. This control strategy is comparable to the method used in the ML-converter without trap circuit. The DC-DC converter sees a DC value as a set value and so the losses can be reduced to a maximum. But the capacitors C_{dc2} have to be chosen respecting the Equation (5.26), to keep the voltage oscillation within a given boundary. The peak-to-peak voltage oscillation is 1400V, which is of course caused by the small capacitor value of C_{dc2}. Therefore to implement this controller type, the measured value of U_{dc2} must be filtered by a low-pass filter with a cut-off frequency at $2 \cdot f_{line}$.

In order to reduce the systems weight to a maximum and to take advantage of the powerful control system of the DC-DC converter, the DC-DC converter generates the full waveform of the current $I_{ch2}(t)$. The other methods have not been simulated in the entire system.

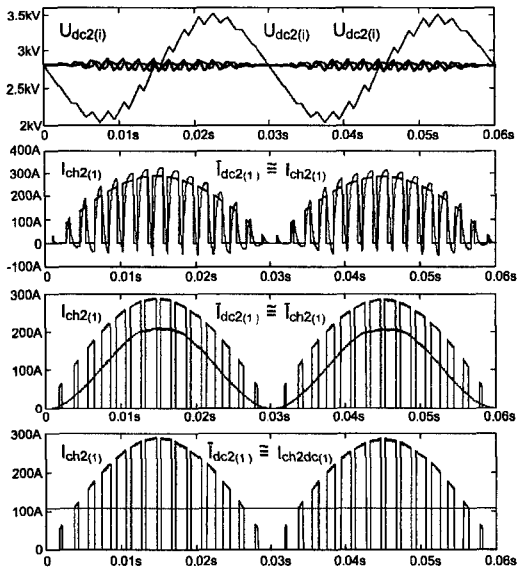

Figure 5.34: Comparison of the three control methods of the DC-DC converter

Cascaded power flow controller for stabilizing the DC-link voltage The only way to stabilize the DC component of the DC-link voltage U_{dc1} can be done by the rather slow global power flow controller G_{R2}, which is in cascade with the current controller G_{R1}. The overview of the controller system is shown in Figure (5.35). The global modulation function $k \cdot V_{ref}$ is generated by the controller G_{R1}. There are n PT_1-Elements in parallel generating each the a partial multilevel converter voltage $U_{conv(n)}$, which are all added to create U_{conv}. After the subtraction of the line voltage U_{line}, the line current is generated by an integral element. The load currents $I_{ch2(n)}$ of the 4Q-converters are generated by the multiplication of the modulation function $k \cdot V_{ref}$ with the line current I_{line}. The primary side currents of the DC-DC converters $I_{dc1(n)}$ are a result of the controller action, which generates a current $I_{dc2(n)}$. The current must be equal to $I_{ch2(n)}$. The Equation of the DC-DC converter (5.14) can be respected to generate the primary side current. The total current charged into the capacitor is the difference of the motor current I_{mot} and the sum of all primary side currents I_{dc1tot}.

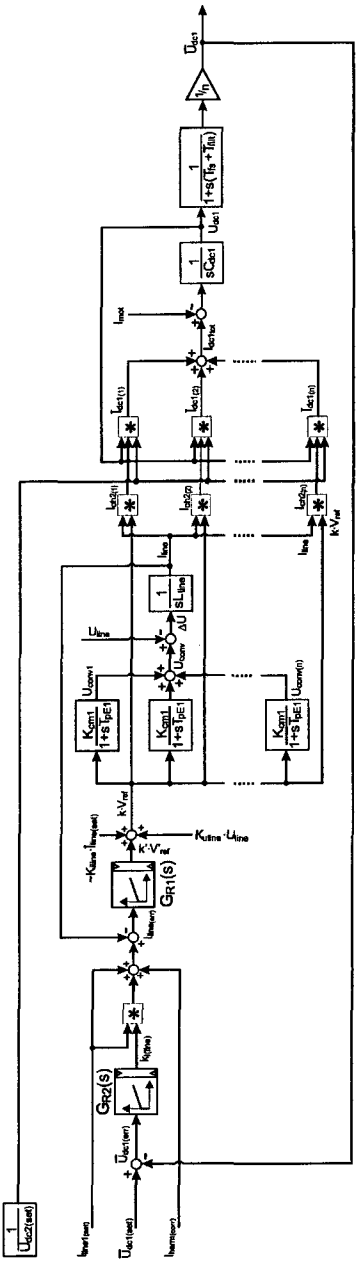

Figure 5.35: Cascaded controller for the power flow and the line current

Unfortunately, the voltage U_{dc1} is not free of oscillation due to the behavior of the trap circuit. This is why the trap circuit is filtered. The global power flow controller sees the measured value $\overline{U}_{dc1}$, which is the DC component of the voltage U_{dc1}. The same filter is needed as described in Equation (5.68) and in the Figure (5.19). This filter takes out the oscillation at $2 \cdot f_{line}$. To design the controller parameters, the Figure (5.36) shows the cascaded controller simplified to a minimum.

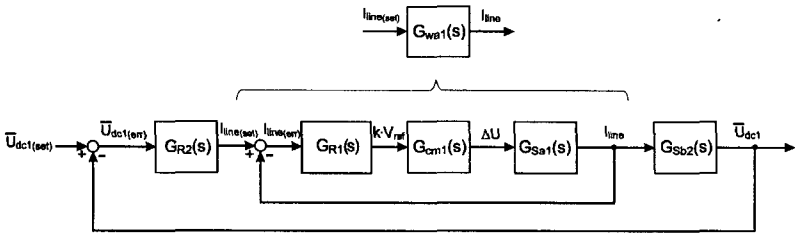

Figure 5.36: Simplified structure of the cascaded controller

The transfer function which transfers the modulation function $k \cdot V_{ref}$ of the controller to a physical value ΔU is named $G_{cm1}(s)$ and is composed of an amplification factor and a small time delay:

$$G_{cm1}(s) = \frac{K'_{cm1}}{1 + sT_{pE1}} \tag{5.87}$$

For each transfer function, the amplification factor K_{cm1} is given by Equation (5.35). But due to the fact that the partial converter voltages $U_{conv(i)}$ are added, the amplification factor resulting for the control system is n times bigger, expressed with K'_{cm1}. The Equation (5.36) shows this value. K'_{cm1} represents the proportionality between to the amplitude of the converter output voltage $\widehat{U}_{conv}$ and the modulation degree k. The converter voltage amplitude of course depends on the 4Q-converter feeding voltages $U_{dc2(i)}$. In this converter type, the voltages $U_{dc2(i)}$ are controlled, so there is no need to feed-forward a correction value to compensate the effects of the voltages $U_{dc2(i)}$ and the value for K'_{cm1} is constant.
The small time constant of the transfer function is given by Equation (5.37). Of course the small time constant is smaller for the overall converter system than for the individual 4Q-converter. The system delay time introduced by the modulation of the series-connected 4Q-converters is T_{cm2} , and is given with Equation (5.38). This value is calculated like to times the resulting switching frequency of the entire multilevel converter. The system that has to be controller is called $G_{sa1}(s)$. This transfer function has an integral behavior.

$$G_{sa1}(s) = \frac{1}{sT_{I1}} \tag{5.88}$$

The current is generated on the line inductance:

$$T_{I1} = L_{line} \tag{5.89}$$

The controller is represented by the transfer function $G_{R1}(s)$. The symmetrical optimum is used to calculate the controller parameters. The two time constants for the controller are given by the Equation (5.42) And the parameters of the controller G_{R1} are given with:

$$K_{i1} = \frac{T_{sample}}{T_{i1}} \tag{5.90}$$

$$K_{p1} = \frac{T_{n1} - \frac{T_{sample}}{2}}{T_{i1}} \tag{5.91}$$

Due to the direct introduction of the phasor diagram into the set value after the controller, shown with Equation (5.28), and the addition of several controller outputs before generation of the set value, the obtained controller values are attenuated by the factor 3, seen in Equation (5.46).
The power flow controller, given by the transfer function $G_{R2}(s)$, is the external controller of the cascaded structure. It is a PI controller like in Figure (5.16). The input value is the error of the DC component from the DC-link voltage voltage U_{dc1}. It generates a modulation degree $k_{I(line)}$. This modulation degree is a value limited within the boundaries $[-1, 1]$. This value is multiplied with the line current set value $I_{line1(set)}$, and is afterwards added again to the value $I_{line1(set)}$. This multiplication and addition allows to modify the set value, which is a sinusoidal value, without modifying the original waveform.
The power flow controller G_{R2} has to be prevented of introducing additional harmonics into the current set value. The internal controller loop is represented by a new transfer function named $G_{wa1}(s)$. This transfer function is described in Equation (5.47). For the external control loop, this transfer function is seen like a function of a small time delay without any amplification:

$$G_{wa1}(s) \cong \frac{1}{1 + sT_{ea1}} = \frac{K_{cm2}}{1 + sT_{pE2}} \tag{5.92}$$

The internal controller was designed by the symmetrical optimum criteria, so the time constant T_{ea1} is given by Equation (5.50). The time constant T_{pa2} is given by the time constant T_{cm2} from in the internal controller loop, added with the other small time constants in the feedback loop. The filter time constants to obtain the DC component of the voltage U_{dc1} are introduced here:

$$T_{pa2} = T_{cm2} + T_{fs} + T_{filt} \tag{5.93}$$

The other time constant is given by the time constant of the internal control system, described by Equation (5.52). The transfer function of the system that has to be controlled, is called $G_{sb2}(s)$. It is a transfer function of integral behavior, describing the voltage integrated on the DC link capacitor C_{dc1}:

$$G_{sb2}(s) = \frac{1}{sT_{I2}} = \frac{1}{sC_{dc1}} \tag{5.94}$$

By knowing all parameters, the external controller can be designed, represented by the transfer function $G_{R2}(s)$. Due to the integral behavior of the voltage on the capacitors,

n	10	Number of converter steps
$C_{dc2(i)}$	$\cong 750\mu F \pm 5\ \%$	Intermediary capacitors
C_{dc1}	$12mF$	DC-link capacitor
C_{trap}	$15mF$	Trap circuit capacitor
L_{trap}	$1.52mH$	Trap circuit inductor
R_{trap}	$100m\Omega$	Resistive part trap circuit inductor
$\overline{U}_{dc1}$	$2.8kV$	DC component U_{dc1}
P_{mot}	$3MW$	Motor power, maximal value
U_{line}	$15kV$	Effective line voltage
f_{line}	$16\frac{2}{3}$Hz	Line frequency
L_{line}	$25\mu H$	Line inductance
R_{line}	$100m\Omega$	Line resistance
T_{sample}	$200\mu s$	Sampling time
f_s	50Hz	Switching frequency 4Q
f_p	8kHz	Switching frequency DC-DC
$\tau_{blank(4Q)}$	$3\mu s$	Blanking time 4Q
τ_{blank}	$4\mu s$	Blanking time DC-DC
$L_{\sigma tot}$	$65\mu H$	Decoupling inductance DC-DC
T_{r2}	$65\mu s$	Measurement delay

Table 5.8: Numerical values for the simulated system with trap circuit

the symmetrical optimum is used. The two time constants of the controller are given with Equation (5.55). The parameters of the controller G_{R2} are given with:

$$K_{i2} = \frac{T_{sample}}{T_{i2}} \tag{5.95}$$

$$K_{p2} = \frac{T_{n2} - \frac{T_{sample}}{2}}{T_{i2}} \tag{5.96}$$

All the parameters for the cascaded controller can now be calculated. The parameters for the active current filter controllers $G_{R4(i)}$ are calculated exactly like in the system without trap circuit in Section 5.1.1. The controller parameters depend on the line inductance.

Simulation results

The entire multilevel system has been again implemented on MATLAB/SIMULINK. The parameters chosen for the simulated system are given in the Table (5.8). The converter consists of 10 multilevel steps and is coupled to a typical railway catenary found in Switzerland, Austria and Germany ($16\frac{2}{3}Hz, 15kV$). A multiple of simulations have been done in order to simulate the behavior of the entire system.

The capacitors $C_{dc2(i)}$ will see a stabilized voltage, while the DC-link capacitor needs a filter, in order to stabilize the oscillation with $2 \cdot f_{line}$. If this voltage is not filtered, this oscillation is seen on the motor converter. This phenomenon has to be avoided.

The next simulation result shows a simulation of the converter with the entire control system. This time the converter voltage U_{conv} is composed of independent DC voltages $U_{dc2(i)}$, which are more or less constant. A zoom on the voltage $U_{dc2(1)}$ is shown in the second graph. The peak-peak voltage oscillation is only 50V (about 2 % of the amplitude) and is due to the size of the intermediate capacitor $C_{dc2(1)}$ and the speed of the control system (small time constants). The current I_{line} is nearly sinusoidal. Another interesting observation is the DC link voltage U_{dc1} oscillating with a mix of the two frequencies 50.12Hz (The resonant frequency of the filter) and $33\frac{1}{3}$Hz (The frequency of the power). This voltage is not entirely stabilized. The voltage oscillation is about 150 volts peak-peak around the desired output voltage $2.8kV$. If the trap circuit would be removed, the peak-peak oscillation would be 900V. The blue line shows $\overline{U}_{dc1}$, which is the DC link voltage after having been filtered by an low-pass filter, as described in Figure (5.19). This value is needed in order to implement the global power flow controller G_{R2}.

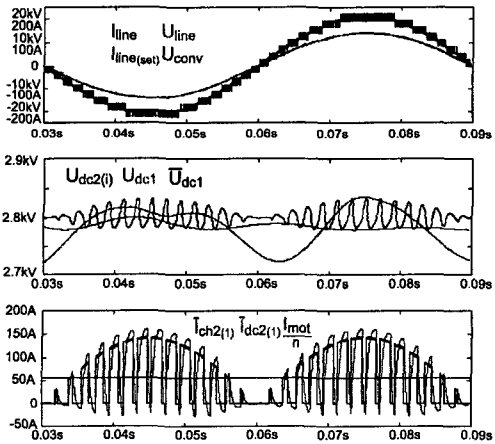

Figure 5.37: Entire electrical waveforms of the ML-converter with trap circuit

Also the current on the DC link side and the intermediate capacitor side are shown. The current $I_{ch2(1)}$ (black), coming from the 4Q-converter is followed by the current $\overline{I}_{dc2(1)}$ (red), generated by the controller of each DC-DC converter. If the two currents are perfectly the same, the voltage $U_{dc2(1)}$ would not oscillate. The blue graph shows the constant motor current on the DC-link side.

The next simulations done for the ML-converter concerned the step response of the entire system. There are many controllers, so many parameters can be tested by changing immediately a set value. Four different important situations have been simulated and the stability of the system has been checked. The simulations done are more or less the same as those been done to simulate the system without trap circuit:

- The motor power is at $P_{mot} = 50\%$. The power is set immediately to 100% when the line current I_{line} is maximal.
- The motor power is at $P_{mot} = 100\%$. The set value of the power is reversed, when the current I_{line} passes trough zero.
- The motor power is at $P_{mot} = 50\%$. The power is set immediately to 100% when the line current I_{line} is maximal. The line voltage U_{line} is not sinusoidal.
- The motor power is constant at 100%. The DC-link voltage U_{dc1} is reduced from $2.8kV$ to $2.4kV$ in order to start the motor.

The simulation results for the situations described above are shown in the next four Figures.

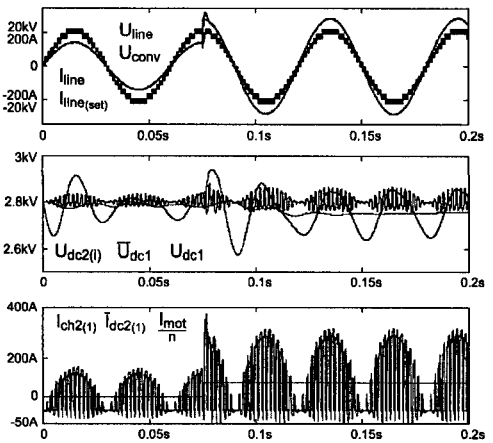

Figure 5.38: Step response changing the power at full line current I_{line}

The simulation shown in Figure (5.38) shows a step on the line current I_{line}, the set value is doubled at the moment $t = 75ms$. The same happens with the motor current I_{mot} in order to keep the input and output power at the same value. The line current I_{line} is controlled with the same performance as in Figure (5.26), where the step response has been done with a ML-system without trap circuit. The oscillation on the 4Q-converter feeding voltages $U_{dc2(i)}$ is twice as high with twice the power transferred. The DC link voltage has a short transient response of about 30ms and stays oscillating with the frequency $2 \cdot f_{line}$ and the peak-peak amplitude of 230V. The intermediary

currents are shown in the last graph. The DC-DC converter control has a fast response, this means the current $I_{ch2(i)}$ and the current $\overline{I}_{dc2(i)}$ have nearly the same waveform. The voltages $U_{dc2(i)}$ have thus a negligible transient response.

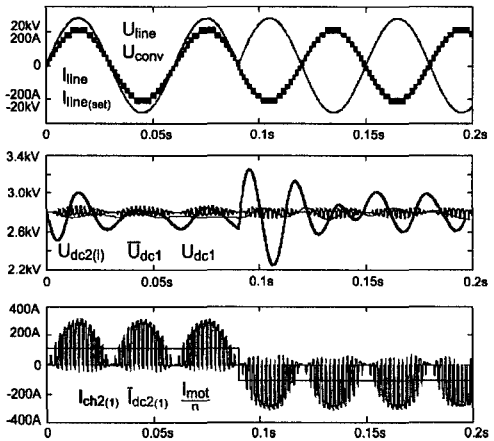

Figure 5.39: Step response changing the power sign

The Figure (5.39) shows a simulation, where the current set value for I_{line} suddenly changes its sign value. This means the power flow is reversed at once. This is done when the line current crosses zero at $t = 90ms$. Due to the powerful line current controller and the fact that the sign value is changed during the current zero-crossing, the line current follows perfectly the sign value. Also the currents $I_{ch2(i)}$, $\overline{I}_{dc2(i)}$ and I_{mot} have no particular transient behavior due to the same effects. While the 4Q-converter feeding voltages $U_{dc2(i)}$ have no particular transient response, the influence on the DC link voltage U_{dc1} is big. The overshoot of the voltage after the step is about 300V, which is more than 10% compared to the set value, this although the controller parameters have been designed with the symmetrical optimum. After $150ms$, the transient response is established and the voltage continues to oscillate with the frequency $2 \cdot f_{line}$ and a peak-peak amplitude of 200V. At least the primary side and the secondary side of the DC-DC converter are entirely decoupled and do not show any correlation on their behavior.

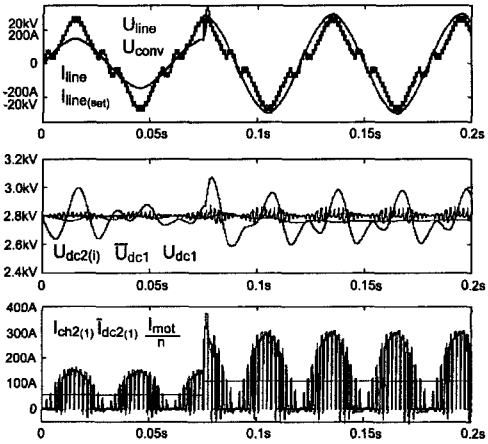

Figure 5.40: Step response changing the line current with a non-sinusoidal line voltage

The simulation shown in Figure (5.40) shows a step on the line current I_{line}, the set value is doubled at the moment $t = 75ms$. It is the same simulation as seen in Figure (5.38), but this time the line voltage is not sinusoidal and contains itself many harmonics, as shown in the Table (5.7). The line current I_{line} is controlled once again with more or less the same performance as in Figure (5.26). But the oscillation on the 4Q-converter feeding voltages $U_{dc2(i)}$ is much more important than before. The DC link voltage has a short transient response of about 20ms and in the steady state it stays oscillating with the frequency $2 \cdot f_{line}$ and the peak-peak amplitude of 400V. While the line voltage U_{line} is not sinusoidal and the line current I_{line} is controlled sinusoidal, the power transfer is not a sinusoidal waveform. This allows the DC link voltage to oscillate with another waveform than in the simulation in Figure (5.38).

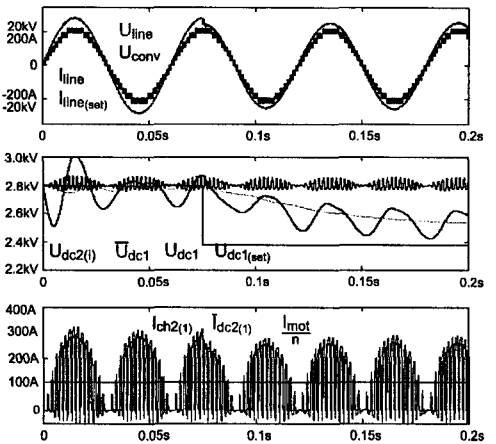

Figure 5.41: Step response changing the DC link voltage

The last step response showed in Figure (5.41) shows a step response on the DC link capacitor. The voltage is controlled by the relatively slow global power flow controller G_{R2}. This simulation shows the possibility of the voltage reduction on the DC link. The DC link voltage is establishes its steady state after $300ms$. During the operation, the DC link voltage oscillates with a peak-peak amplitude of 250V. If the global power flow controller is designed for faster speeds, the new set value for the DC link voltage U_{dc1} could be established faster.

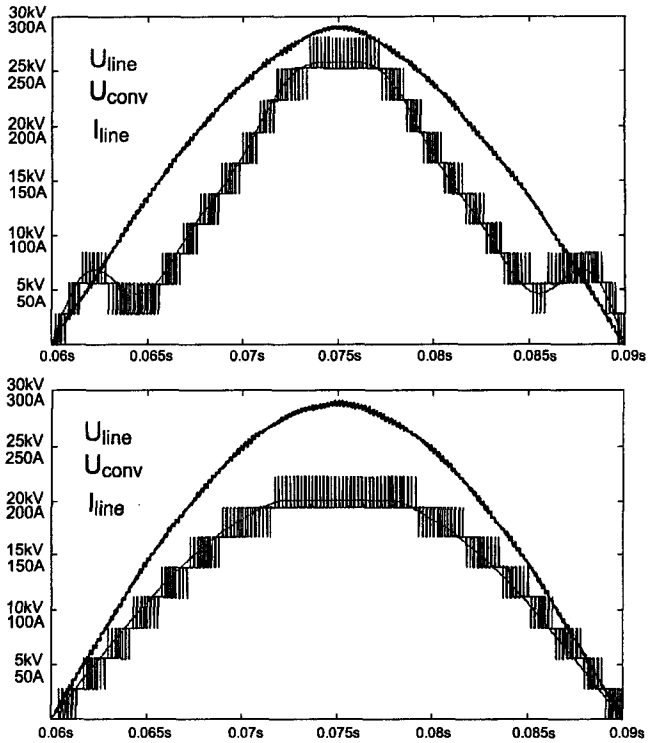

Figure 5.42: The two simulated voltage waveforms U_{line} for a system with trap circuit

The Figure (5.42) shows the two line voltages U_{line} used for the simulation and the line currents. Both the voltages are not chosen sinusoidal, as shown already in the Figure (5.30). In the Table (5.7) the harmonic content of the voltage in the upper graph is described. This voltage has been used for the step response simulation in Figure (5.40). The other voltage generated is a sinusoidal waveform, but there is an voltage limitation at 95% of the amplitude. In this simulation, the supply voltages are constant. Of course with the first line voltage U_{line} containing many harmonics, the current cannot be controlled in exactly the same quality as in the second one. On the current waveform it can be seen that there is a low-order harmonic content.

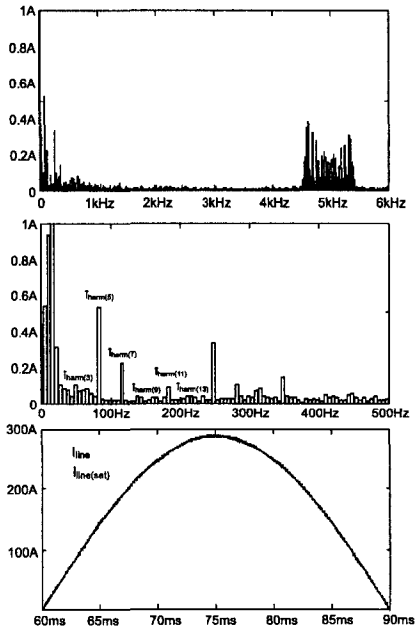

Figure 5.43: FFT of the line current, the line voltage containing flat part

The next simulation in Figure (5.43) has been done in order to analyze the harmonic contents of the current, when the 4Q-converter feeding voltages are controlled. The first simulations are done with line voltage U_{line} combined with the flat part. The current harmonic filters have been implemented. The upper graphs shows the FFT analysis of the current harmonics up to 6kHz. This has been done to show the harmonics of the resulting switching frequency around 5kHz. Only the fifth order harmonic has an amplitude higher than 0.5A. The middle graphs show the low-order harmonics, which are actively filtered. It is interesting to see that the third order harmonic is hardly visible. The implemented harmonics controller G_{RA} has only a simple proportional behavior. The harmonics up to the 11th order are filtered. On the third graph, the current is controlled with its set value, showing very few deviation. By implementing a real PI-controller, the steady-state error of the harmonics would be better eliminated and in this way would even show better results.

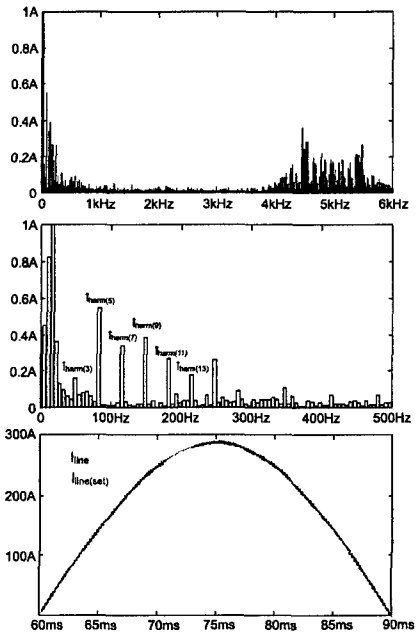

Figure 5.44: FFT of the line current, the line voltage U_{line} containing worst-case harmonics

The next simulation (5.44) has been done in order to analyze the harmonic contents of the current, when the 4Q-converter feeding voltages are controlled and the line voltage is containing the worst-case harmonics as described in Table (5.7). The amplitudes of the harmonics are in this case more important than before, especially the 3rd, 5th and 13th harmonic are higher. On the upper graph, where the harmonics are shown up to the frequency of 6kHz, a group of harmonics with the frequency 250Hz and 500Hz can be detected. This is the basic switching frequency and its second order harmonics. But the amplitudes of these harmonics are very weak (0.35A). Thanks to the active current filter the current is once again controlled to a nearly sinusoidal function.

5.2 Configurable multilevel converters for AC and DC power lines

The last multilevel system tested in this report is a special setup, which allows a changeable configuration for different traction lines. This special configuration allows the construction of a locomotive able to adapt to different European power lines for a fast transeuropean operation. The principle has been invented during this work and was patented together with the industrial partner, to be seen in [47]. The basic elements of this multilevel configuration is once again a voltage-controlled DC-DC converter feeding a 4Q-converter. By connecting certain number of these elements in a special way, shown in Figure (5.45), the locomotive can be easily connected to two different power lines. This variant allows the coupling of the locomotive to a single phase, high voltage AC power line (as described before by the two systems with and without the trap circuit), but also the coupling to a medium-voltage DC catenary (for instance 3kV DC like in Italy, Spain, etc.). Besides the standard multilevel converter, the system consists of a number of power switches $S1$ to $S(m+1)$, which allow to change the schematics on the AC-side of the 4Q-converters:

- The coupling to the high-voltage AC catenary is done by connecting all the multilevel converter elements in series (4Q-converter inclusive feeding by DC-DC converter). In this way, the highest possible voltage can be generated. This configuration corresponds to the two converters simulated before, to be seen in Chapter 5.1.2, page 215.

- The coupling to a DC voltage power line is done by connecting two 4Q-converters in series and then to connect these pairs of 4Q-converters in parallel. Each pair of 4Q-converters has its own partial decoupling inductance $L_{line(i)}$ and they work as two-quadrant DC-DC converters with PWM modulation.

The configuration of the converter can be changed by a number of power switches. This is described in the next two paragraphs. In the Figure (5.45), a general implementation of the configurable converter is shown.

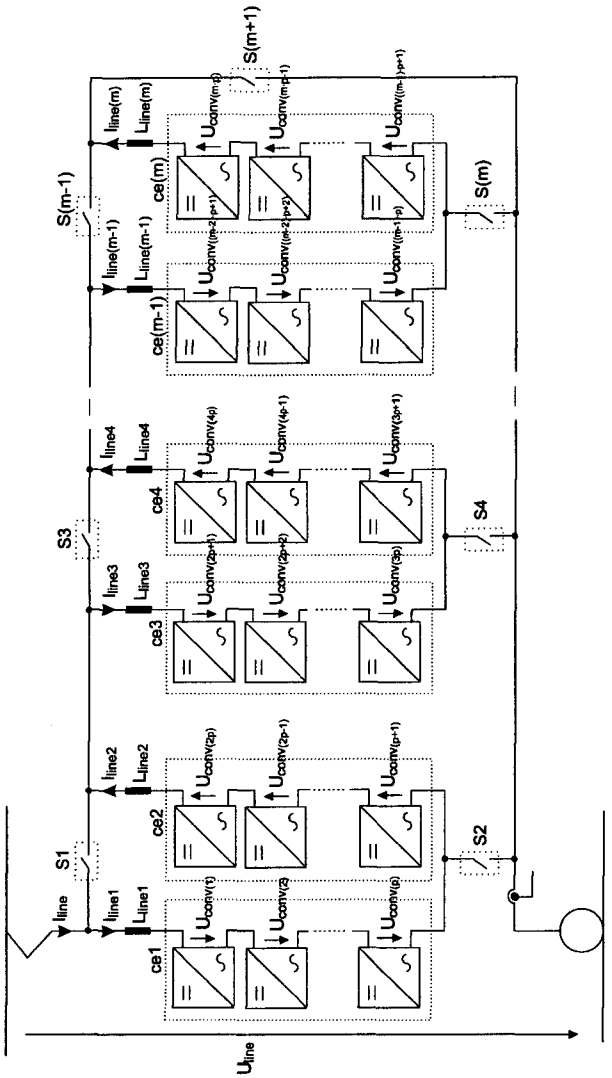

Figure 5.45: Configurable multilevel converter for different power lines

The multilevel converter cells (on the Figure (5.45), the DC-DC converters are not shown, they are connected to the DC side of the 4Q-converters) are grouped in p elements in series. Depending on the application (or of course of the DC voltage to be coupled) the desired number of converters can be connected in series within the group $ce(i)$. At the same time there are m of these 4Q-converter groups $ce(i)$ connected in parallel. The entire number n of the converter cells is in the following trivial relation with m and p:

$$n = m \cdot p \tag{5.97}$$

The converter can be called $2s/5p$, if the index m is equal to 5. This means there are groups of two converter cells in series and 5 in parallel.

5.2.1 Coupling to a high voltage AC catenary

With the series-connection of n converter cells an AC voltage with a maximal amplitude of $n \cdot U_{dc2}$. This high voltage is needed to connect the converter to a high voltage AC link. This can be achieved if all the converter cells are connected in series. All these converter groups $ce1 - ce(m)$ are connected in series by opening the all the switches $S1$ to $S(m)$ and by closing the switch $S(m+1)$. In this way, the multilevel converter is in the high-voltage AC operation mode. If the number of 4Q-converters with their DC-DC converter is $n = 10$, the configuration is called $10s$ due to the full series-connection. The Equation for the generated converter voltage is of course the simple addition of all partial AC voltages:

$$U_{conv} = \sum_{i=1}^{n} U_{conv(i)} \tag{5.98}$$

All the partial line currents are connected in series, so they are all the same. The Equation for I_{line} is:

$$I_{line} = I_{line(i)} \qquad \forall i = [1, .., m] \tag{5.99}$$

The decoupling inductance seen between the line voltage and the converter voltage is the sum of all partial inductances:

$$L_{line} = \sum_{i=1}^{m} L_{line(i)} \tag{5.100}$$

The configuration of the switches is given in the Table (5.9) below. A switch position 1 indicates that the switch is conducting the current.

$S1$	0
$S2$	0
$\vdots$	$\vdots$
$S(m-1)$	0
$S(m)$	0
$S(m+1)$	1

Table 5.9: Switch positions for an AC coupling

This converter corresponds to the converters simulated in the chapters before. In this chapter, no further simulations are done to explain this converter type.

5.2.2 Coupling to a medium voltage DC catenary

For a different railway network, the converter has to be connected to a medium-voltage DC link, for instance a typical 3kV DC link. This type of railway feeding can be found in many countries. For this aim, the 4Q-converters are organized in m groups $ce(i)$ of converters, all of them are connected in parallel. One group contains a series-connection of p 4Q-converters with each a DC-DC converter. Each group $ce(i)$ of series-connected multilevel cells contains a decoupling inductance $L_{line(i)}$. For instance if the number of groups $m = 5$ and the number of series-connected 4Q-converters is $p = 2$, the configuration of the converter is called $2s/5p$. The Table (5.10) gives the position of the switches to configure the converter for the medium-voltage DC catenary:

$S1$	1
$S2$	1
$\vdots$	$\vdots$
$S(m-1)$	1
$S(m)$	1
$S(m+1)$	0

Table 5.10: Switch positions for an medium-voltage DC coupling

Every converter group $ce(i)$ works as a two-level DC-DC converter towards the DC-power line. With this DC-DC converter, a four-quadrant operation is possible. A converter cell group can generate five different voltage steps ($-2U_{dc2}$,$-U_{dc2}$,0,U_{dc2},$2U_{dc2}$) and applies this voltage to the decoupling inductance $L_{line(i)}$. On the other side of the inductance, there is the DC voltage of the catenary. The current $I_{line(i)}$ is generated by the voltage difference between the line voltage U_{line} and the converter group voltage $U_{ce(i)}$. This voltage is an addition of p 4Q-converter AC voltages, expressed in the following Equation (5.101).

$$U_{ce(i)} = (-1)^{i+1} \sum_{j=(i-1)\cdot k}^{i\cdot p} U_{conv(j)} \tag{5.101}$$

The line current I_{line} is generated in a node, where all the partial currents $I_{line(i)}$ are flowing together. So it is the sum of all partial line currents

$$I_{line} = \sum_{i=1}^{m} I_{line(i)} \tag{5.102}$$

The Equation (5.101) adds a set of inverted voltages, if the index i is a pair number. This is necessary, if the basic scheme in Figure (5.45) is considered: The second, fourth group of 4Q-converters are oriented in the inverse direction in the $2s/5p$ configuration compared to the full series connection $10s$. This must also be respected when the modulator is implemented. The voltage difference generates a current in the decoupling inductance. If the current must be fully controlled and it has to change its sign value, the voltage $U_{ce(i)}$ should be able to be higher than the line voltage U_{line}. That is why a desired number of converter cells are put in series. In this way, a desired line current can be controlled, even if the line voltage is not constant.

Modulation strategy to reduce current ripple

By respecting a particular modulation strategy for the 4Q-converter groups $U_{ce(i)}$, the current ripple can be reduced. The currents $I_{line(1)}$ to $I_{line(m)}$ are the currents generated by the converter groups. They are all independent of each other. Each of the 4Q-converters is modulated with a PWM modulation scheme, using triangular carrier functions with a horizontal shift (HSCS method, to be seen in Section 2.4.2). For a converter group with p steps, $2p$ carrier signals are needed, just like a single-phased multilevel converter with the same optimization of the switching signals, to be seen on page (33).
In order to achieve more reduction of the current harmonics, the triangular carrier signals of each converter group must be phase-shifted equally. The Equation (5.103) below gives the mathematical functions for the triangular carrier signals. The carrier signals are indexed with i represent the 4Q-converter cell inside the converter group $ce(j)$, going from 1 to p. The index j is to count the converter group $ce(j)$, going from 1 to m. Equation (2.29) on page 34 and Equation (5.104) gives the two phase-shift angles that have to be respected to calculate the phase angles.

$$aux_{i,j}(t) = \begin{cases} \frac{1}{2}\left(1 + \frac{2}{\pi}\arcsin\left[\sin(2\pi f_s t + \Delta\varphi_i + \Delta\psi_j)\right]\right) \\ i = [1, .., p] \\ j = [1, .., m] \\ \frac{1}{2}\left(-1 + \frac{2}{\pi}\arcsin\left[\sin(2\pi f_s t + \Delta\varphi_{i+1-p} + \Delta\psi_{j+1-m})\right]\right) \\ i = [p+1, .., 2p] \\ j = [m+1, .., 2m] \end{cases} \tag{5.103}$$

The phase-shift value between the carrier signals of a converter group $ce(i)$ and the neighbor group $ce(i+1)$ is given with (5.104)

$$\Delta\psi_i = \frac{360^0}{m} \cdot (i-1) \qquad i = [1, 2, \ldots, m] \tag{5.104}$$

There are in all m different phase angles $\Delta\psi_i$. The current of one converter group $ce(i)$ will have a triangular waveform with the period:

$$T_{Iline(i)} = \frac{1}{2p \cdot f_s} \tag{5.105}$$

This period must be divided by the number of converter groups $ce(i)$. Therefore the time-shift between two partial line currents corresponds to the period of the overall line current I_{line}. The period is shown in Equation (5.106):

$$T_{Iline} = \frac{1}{2pm \cdot f_s} = \frac{1}{2n \cdot f_s} \tag{5.106}$$

The Figure (5.46) visualizes all the partial currents $I_{line(i)}$ with the overall current I_{line} of a DC coupled ML-converter in the configuration $2s/5p$. The period of the partial currents is $m = 5$ times higher than the period of the overall line current. The harmonics reduction is in the order of a factor 15.

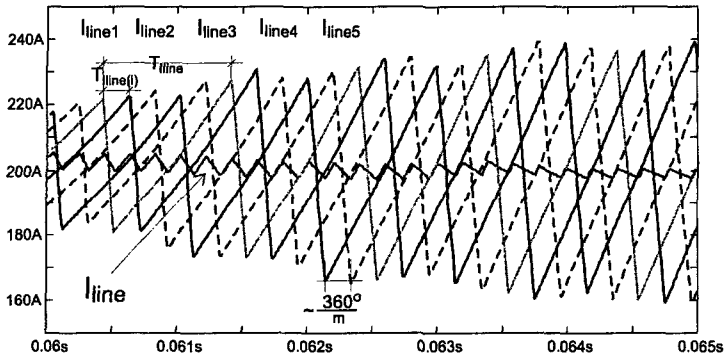

Figure 5.46: Cancellation of the current ripple with phase-shifted currents

The current ripple characteristics can be calculated in function of the modulation degree k. A multilevel converter system consists of m converter groups $ce(i)$. These converter groups generate an independent current. The current ripple characteristics of one converter group can be computed as follows:

$$I_{ripple(i)} = \frac{1}{L_{line(i)}} \int_0^{D \cdot T_{lline(i)}} U_{dc2}(1-D)dt \tag{5.107}$$

The variable D is an expression for the duty cycle. When U_{line} is going through the interval $[i \cdot Udc2 \quad \ldots \quad i+1 \cdot Udc2]$, the duty cycle goes from 0 to 1. The details of this calculation can be found in [27], page 98. After the integration and some mathematical transformations it can be found:

$$I_{ripple(i)} = \frac{U_{dc2} D(1-D)}{2pf_s L_{line(i)}} \tag{5.108}$$

Of course the duty cycle is not useful in this application and has to be replaced by the modulation degree k, which is directly generated by the controller:

$$D = p \cdot k - trunc(p \cdot k) \qquad [-1 < k < 1] \tag{5.109}$$

The relation between the line voltage U_{line} and the 4Q-converter feeding voltage U_{dc2} is given with the Equation (5.110). This equation must be respected, if the line current I_{linei} should be a DC current with a superposed switching ripple.

$$U_{line} = p \cdot k \cdot U_{dc2} \tag{5.110}$$

If know the overall line current I_{line} is created and the phase-shifting strategy is used, the current ripple I_{ripple} on the line current can be calculated. This strategy has been implemented in [48] and [49].

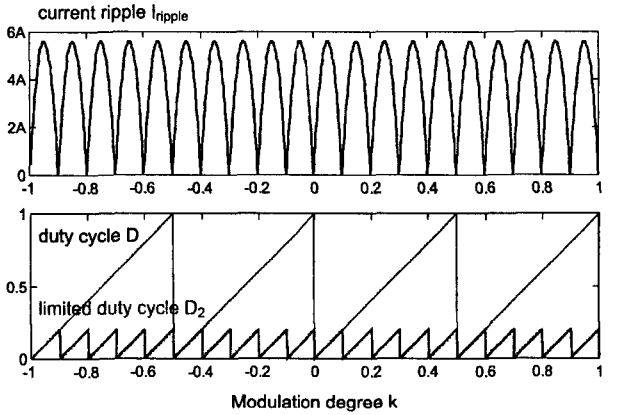

Figure 5.47: The current ripple I_{ripple} in dependence of the modulation degree

The overall current is composed of the m partial currents, which are equally time-shifted by the value T_{Iline}.

$$I_{line} = \sum_{i=1}^{m} I_{line(i)} = \sum_{i=0}^{m-1} I_{line(1)}\,(t - i \cdot T_{Iline}) \tag{5.111}$$

The current $I_{line(i)}$ is a DC current with a triangular waveform, this means there is a rising and a falling part of the current. The Equation for the rising current is:

$$I_{line(i,rise)} = I_{min} + \frac{U_{dc2}(1-D)}{L_{line}} t \tag{5.112}$$

The Equation for the falling current is:

$$I_{line(i,fall)} = I_{max} - \frac{D \cdot U_{dc2}}{L_{line}} t \tag{5.113}$$

By evaluation the Equation (5.111) by using the Equations (5.112) and (5.113) in a period T_{Iline}, the ripple characteristics can be found.

$$I_{ripple} = \frac{U_{dc2} \cdot D(1-mD)}{2nf_s L_{line(i)}} \qquad \left[0 \le D \le \frac{1}{m}\right] \tag{5.114}$$

The Equation given with (5.114) is only valid in the limited interval of the duty cycle D. But as it could be seen in [49], the ripple current characteristics is repeated in every interval $[\frac{i}{m} .. \frac{i+1}{m}]$ of the duty cycle D. To take this effect into account, a limited duty cycle is defined, called D_2:

$$D_2 = [p \cdot k - trunc(p \cdot k)] - \frac{trunc\,[m(p \cdot k - trunc(p \cdot k))]}{m} \quad [-1 \le k \le 1] \tag{5.115}$$

The limited duty cycle never exceeds the value $\frac{1}{m}$ for D_2. Therefore the final equation for the current ripple is given below:

$$I_{ripple} = \frac{U_{dc2} \cdot D_2(1 - mD_2)}{2nf_s L_{line(i)}} \tag{5.116}$$

The variable D_2 has to be replaced by the expression given in (5.115). In this way, the current ripple can be visualized all over the whole modulation degree interval of k. The result of this Equation is visualized in the Figure (5.47). In this Figure, the current ripple of a configurable multilevel converter with the parameters $m = 5$ and $p = 2$ is evaluated, in function of the modulation degree k. The algorithm for MATLAB is given in Appendix A.6.

Control strategy

The DC coupling of the multilevel converter can be controlled by the use of one PI-controller $G_{R6(i)}$ per series-connected 4Q-converter group. Therefore the entire system needs m PI-controllers. The PI-controllers are implemented as shown in the Figure (5.16). There is no active harmonic cancellation, implemented before with the controllers G_{R4}. Of course the DC-DC converters are once again voltage-controlled. In this configuration type of the multilevel converter, the DC-DC converters will always control the voltages $U_{dc2(i)}$, with the uncontrolled input voltage U_{dc1} coupled to a DC-link. Due to the DC exchange of the power, there is no pulsating energy. This fact reduces the control problem to keep the DC voltages constant, feeding the 4Q-converters. Of course there will be less harmonics on the line current I_{line}. In this application context, an uncontrolled DC-DC converter can easily be used, as described in [20]. The control system global set value for the current, which is the motor current set value. The relation below gives the set value for the DC line current:

$$I_{line} = \frac{U_{dc1(set)}}{U_{line}} \tag{5.117}$$

At the beginning (1), this set value is calculated with Equation (5.117). The given value $I_{line(set)}$ is divided through the number m of 4Q-converter groups (2). Each converter group forms a DC-DC converter creating its own current. All these partial currents $I_{line(i)}$ are added (8) to generate the overall line current I_{line}. The partial set values $I_{line(i)_{(set)}}$ are filtered by a low-pass filter (3) with the cut-off time constant T_{filt6} in order to avoid fast changes on the set value. This is done to suppress current overshoot when the set value is abruptly changed.

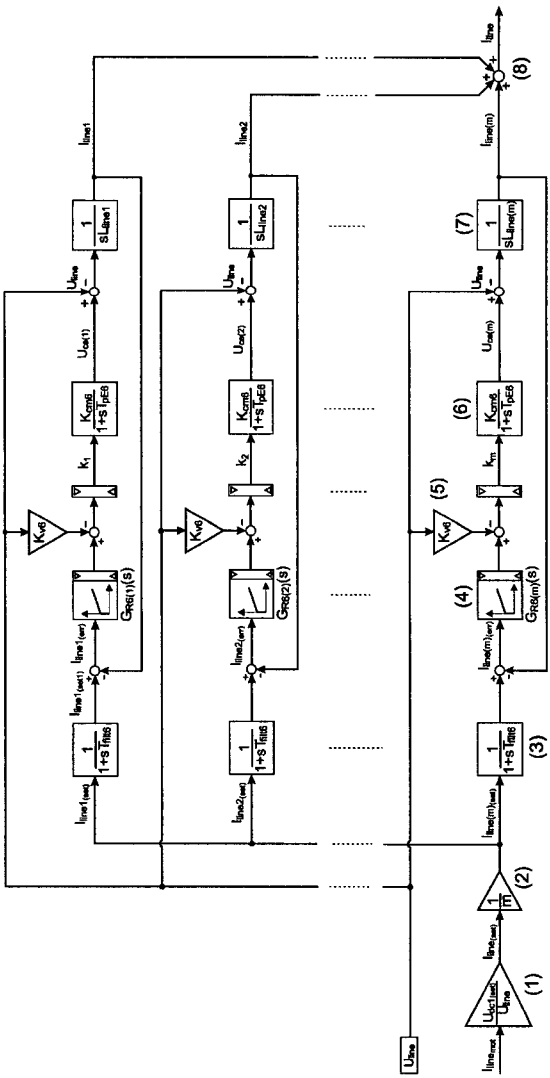

Figure 5.48: Control system to control the DC currents of the ML-system

Block number (4) on the Figure (5.48) shows the current PI-controller and block (5) shows the direct addition of the perturbation value U_{line} to the output value of the controller. The result of this addition is the modulation degree k_i, which is considered as a DC value (There is no multiplication with a time-depending function $V_{ref(i)}$). The current on an inductor behaves like the Equation (5.118).

$$I_{line(i)} = \frac{1}{L_{line(i)}} \int_0^t U_{ce(i)} - U_{line} dt \tag{5.118}$$

The sum of the converter voltages $U_{ce(i)}$ are controlled by the output value of the controller, but U_{line} is a value which cannot be controlled and is so considered as the perturbation value of the system. By introducing a proportional value of U_{line} to the controller output, all changes on this value can easily be compensated. In the function block (6) the transfer function of the modulator together with p 4Q-converter cells is given. The small time constants of the modulator and the control algorithm are respected here. At last, the function block (7) describes the integral behavior of the current on the inductor.
The transfer function containing the modulator and the p 4Q-converter cells is given by:

$$G_{cm6}(s) = \frac{K_{cm6}}{1 + sT_{pe6}} \tag{5.119}$$

The amplification factor is the maximal amplitude of the voltage generated by a converter group $ce(i)$:

$$K_{cm6} = p \cdot U_{dc2(set)} \tag{5.120}$$

The small time constant is also depending on the number of series-connected 4Q-converters p:

$$T_{pE6} = \frac{T_{sample}}{2} + T_{cm6} + T_{r2} \tag{5.121}$$

The measurement delay T_{r2} for the control system is the same as before given in Table (5.6). The delay generated by the modulator is:

$$T_{cm6} = \frac{1}{4p \cdot f_s} + T_{cm6} + T_{r2} \tag{5.122}$$

The direct introduction of the perturbation value is of course the inverse of the amplification factor K_{cm6}:

$$K_{v6} = \frac{1}{p \cdot U_{dc2(set)}} \tag{5.123}$$

The system that has to be controlled is the current integrated on an inductor. The transfer function G_{s6} is:

$$G_{s6}(s) = \frac{1}{sT_{i6}} = \frac{1}{sL_{line(i)}} \tag{5.124}$$

The time constant T_{filt} of the filter for the set value a numerical value of $30ms$ has been chosen. The symmetrical optimum is once again used to compute the controller parameters. The Equation for the two controller time constant is given in (5.126)

$$T_{n6} = 4 \cdot T_{pE6} \tag{5.125}$$

$$T_{i6} = \frac{8K_{cm6}T_{pE6}{}^2}{T_{I6}} \tag{5.126}$$

The amplification factors of the controllers $G_{R6(i)}$ are given with:

$$K_{i6} = \frac{T_{sample}}{T_{i6}} \tag{5.127}$$

$$K_{p6} = \frac{T_{n6} - \frac{T_{sample}}{2}}{T_{i6}} \tag{5.128}$$

These parameters are used for the simulation results presented in the next chapter.

Simulation results

Of course the configuration $2s/5p$ for the coupling with the medium-voltage DC catenary has been simulated, using 10 4Q-converters combined with the DC-DC converters. The setup for the simulation is shown in Figure (5.49). The implementation of the system was done with MATLAB/SIMULINK, where the simulated system could also be configured for AC high voltage and DC medium voltage coupling.

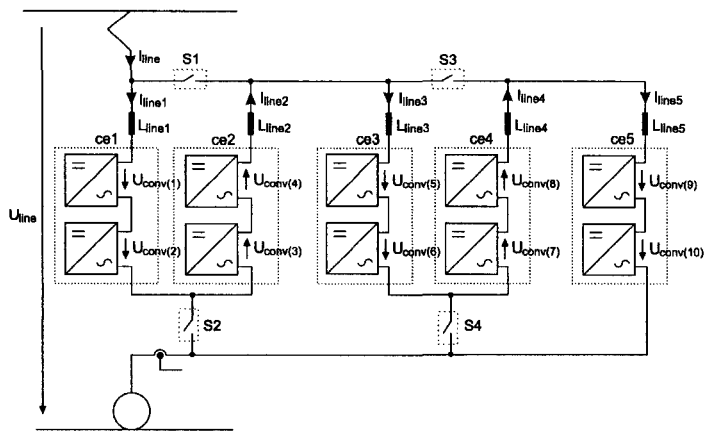

Figure 5.49: Simulated configurable multilevel converter

There are some parameters of the simulation, which have not been given before. The Table (5.11) shows the used parameters:

n	10	Number of converter steps
m	5	Number of parallel switched converter groups
p	2	Number of 4Q-converters in series per group
$L_{line(i)}$	$5\mu H$	Value of a partial line inductance
$R_{line(i)}$	$20m\Omega$	Partial line resistance
$U_{line(DC)}$	$3kV \pm 10\%$	Decoupling inductance DC-DC
T_{filt6}	$3ms$	Filter time constant for set value

Table 5.11: Numerical values for the simulated system with DC coupling

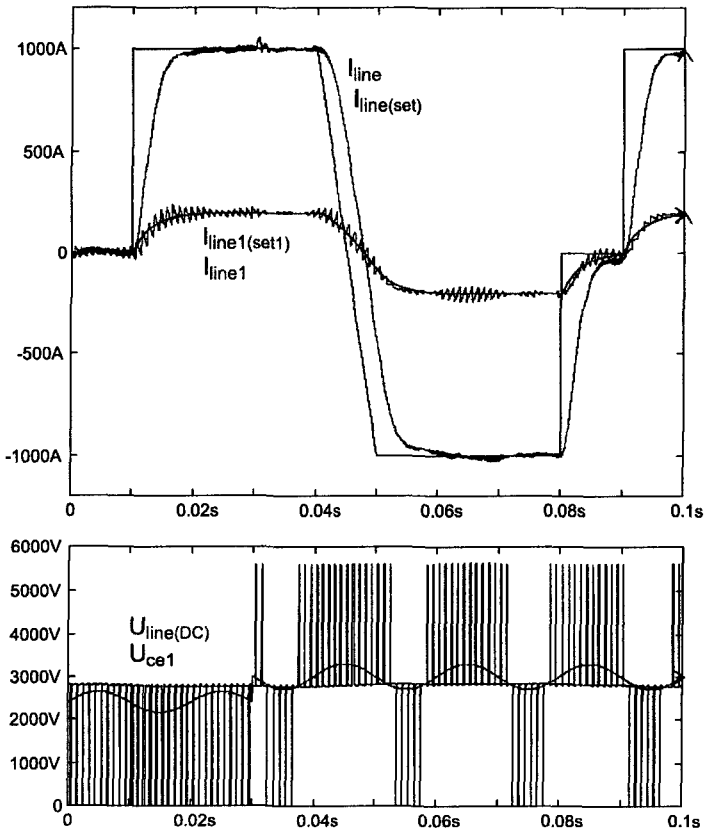

Figure 5.50: Simulation of a DC power line with the coupled ML-converter

The first simulation (5.50) shows a variable DC line voltage $U_{line(DC)}$, together with one of the converter group voltages, $U_{ce(1)}$. $U_{ce(1)}$ is a voltage able to be on 5 different voltage levels. But in this case, only the zero voltage and the two positive voltages are

used. The DC line voltage contains a step and a superposed oscillation, in order to observe the influence on the current quality. The set value for the line current I_{line} is variable. There are steps at $t = 10mS$, $t = 80ms$ and $t = 90ms$, in the same time the current goes from a maximal positive value of 1kA (motor mode) to a negative current (generator mode) of 1kA. Due to the filtering of the step value, there is no current overshoot, which helps to reduce losses and prevents the destruction of the semiconductors. By looking at the time moment $t = 72.5ms$, it can be seen that the line voltage U_{line} is equal to two times the 4Q-converter feeding voltage $U_{dc2(i)}$. This means theoretically that the current ripple is zero. By looking at the line current I_{line} and the partial line current $I_{line(i)}$ it can be seen that the current ripple is nearly zero. It is particularly interesting to compare the partial line current $I_{line(1)}$ with the global line current I_{line}. The partial line current is following the filtered set value. The current oscillation has a high amplitude (up to 80A peak-peak, which is 40% compared to the average current value). The overall line current ripple is only at about 8A peak-to-peak. This performance is due to the phase-shifted modulation strategy described before.

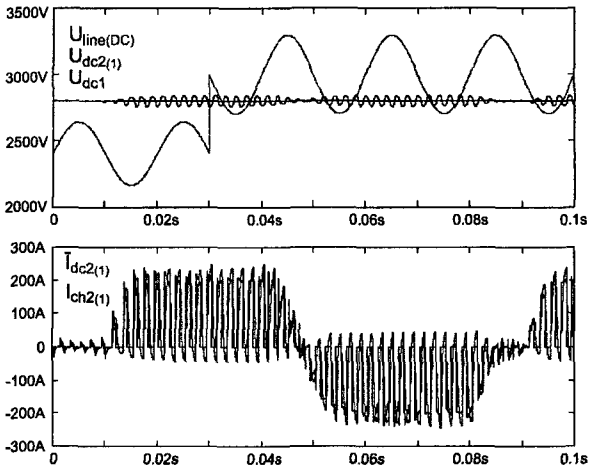

Figure 5.51: Simulation of the voltages and currents on the ML-converter

The graphs showed in Figure (5.51) are showing a comparison of the DC line voltage $U_{line(DC)}$ compared with the feeding voltage of the 4Q-converters, $U_{dc2(1)}$. This voltage is controlled actively by the DC-DC converters. The graphs beneath are showing the current $I_{ch2(1)}$ generated by the modulation of the 4Q-converters. The DC-DC converter tries to follow this current in this implementation. The current $\overline{I}_{dc2(1)}$ is generated by the DC-DC converter. The oscillation on the voltages $U_{dc2(i)}$ can be explained by the difference between the two currents $\overline{I}_{dc2(i)}$ and $I_{ch2(i)}$. This difference cannot be eliminated, the cause is the small time constant of the DC-DC converter (modulation) and its control system (measurement delay, sampling period).

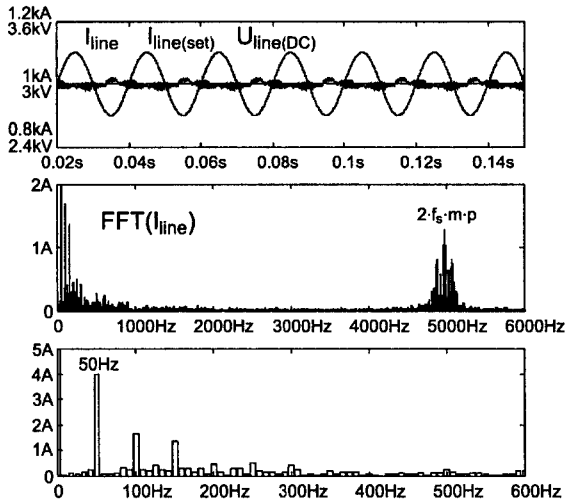

Figure 5.52: Analysis of the current harmonics in the DC current mode

In the simulation (5.52) the current has been analyzed by an FFT. The step response on the voltage U_{line} has been eliminated and the current is controlled constant. Due to the ripple cancellation of the current by the modulation there is only a very small current ripple on the line frequency at the resulting switching frequency $2f_s mp$. An additional passive filter can reduce these harmonics. The low-frequency harmonics are due to the voltage oscillation superposed on the line voltage U_{line}. The oscillation has a peak-peak value of 600V, which is 20% compared to the DC value of the voltage. The voltage oscillation has a frequency of 50Hz. This frequency and the harmonics of this frequency can be seen on the line current I_{line}. An active filter principle as described in Section 5.1.1, page 199 can reduce these harmonics.

Advanced control methods for the configurable converter

There are two more methods how to control the configurable converter coupled to a DC link catenary. Both of them aim a reduction of the current harmonics on the line I_{line}. They use the fact that at several points of the modulation degree k the current harmonics are entirely cancelled, shown in Figure (5.47). The proposed multilevel converter consists of voltage-controlled DC-DC converters, which behavior is optimized to change the set value for the DC output voltage $U_{dc2(set)}$. This can be used for the configurable multilevel converter to achieve always an entire current harmonic cancellation.

- The first method proposes a multilevel converter system in the DC catenary coupling configuration, where the front-end 4Q-converters still work as series-connected DC-DC converters. But the voltage set value of the DC-DC converters is adapted

to the line voltage U_{line}. In this way the modulation degree k for the front-end 4Q-converters can be always in a point where the current harmonics are cancelled. The following example is given: A converter system with $m = 5$ converter groups $ce(i)$ is taken, using $p = 2$ series-connected 4Q-converters. The DC link voltage U_{dc1} is 2.8kV, while the DC catenary voltage is fixed at 3.1kV. The output voltage of the DC-DC converters U_{dc2} must in this case be either controlled to $U_{dc2(set)} = 3.1kV$ or to the nearest voltage $U_{dc2(set)} = 0.8 \cdot 3.1kV = 2.48kV$. In this way the modulation degree for the 4Q-converters k will be in forced to work in a minimum value and the current harmonics are nearly entirely cancelled. This is also possible if the catenary voltage is disturbed by an superposed AC voltage. In this case the set values of the DC-DC converters must be constantly updated.

- The second method consists in the fact that the 4Q-converters are only used to let the line current I_{line} pass trough to the DC-DC converter output voltage U_{dc2} feeding the concerned 4Q-converter. In this way, the DC-DC converter output voltages of one converter group $ce(i)$ are connected in series and are directly coupled to the catenary over the decoupling inductance. There is no modulation on the 4Q-converters, which allows a reduction of the losses. The line current is controlled through a variation of the sum of the voltages $U_{dc2(i)}$ in a converter group. This is done by a cascaded controller, where the internal controller is the DC-DC converter output voltage and the external controller is the line current controller. The DC-DC converters must be able to change their output voltage U_{dc2} quickly in order to provide a good current control. But this is no problem due to the fact that the line current is a DC-value.

These two variations of the control of the configurable DC-DC converter are not documented in this report.

Conclusions

Three different multilevel converter systems are developed for traction applications. The system is used as front-end power transformer for high-voltage AC coupling. For these three converter types, a complete control systems was developed. All the elements of the controllers are computed analytically depending on the system parameters. A complex simulation environment was implemented and the converters were simulated with the desired parameters. The simulation environment can take many parasitic effects of the real world into account and allows a realistic system evaluation. The most original solution is the presented configurable multilevel converter, which has been patented. This chapter shows the application potential of the presented multilevel converter. But many more system application can be imagined such as static VAR compensators [14], FACTS for high voltage power lines , electronic transformers etc.

Chapter 6

Conclusions

In this thesis, multilevel converters with symmetrical DC feeding have been studied. The used multilevel topology are the series-connected four-quadrant converters (SCFQ). Special emphasis was given on four-quadrant converters supplied by voltage-controlled DC-DC converters. The DC-DC converter can operate in a two-quadrant mode, allowing reversible power. The conclusions on the work are grouped for each chapter:

In chapter 2 describing the single-phase multilevel converters, a general single phase multilevel converter topology is presented using a certain number of four-quadrant converters. They are connected in series (SCFQ). All four-quadrant converters are fed symmetrically. This converter type is compared with other existing solutions for a multilevel converter implementation. For the proposed converter type, several feeding methods are compared. For the modulation of this converter type, the step and the PWM modulation method has been analyzed and optimized for the multilevel operation. The optimization consists of symmetrical load sharing, the avoiding of voltage cancellation between two multilevel steps and linearization of the proposed modulators. A single phase control strategy for the multilevel converter has been developed, using a rotating coordinate system in the complex phasor plane combined with the PWM modulation. This novel control method uses only two PI controllers and allows to achieve good dynamic performance together with a strong reduction of all low-order harmonics on the line current. A low-power prototype has been developed and experimental results have been done to underline the analyzed modulation and control methods. Future developments in this fields can be found in many high power single-phase applications like electronic transformers and amplifiers.

A three phase multilevel converter has been defined in chapter 3, based on the same structure (SCFQ) as the single phase converter. The individual steps are fed by an identical DC voltages (symmetrical feeding). A step, PWM and a vector modulation have been developed for this converter type. The methods are compared to each other. The vector modulation is a new kind of modulation method for the multilevel converter. A three-dimensional approach has been developed, allowing the reduction of the switching losses to a minimal value. All the developments on the three-phase multilevel converter are tested and compared by simulations. A prototype of 10kW has been developed and all

the methods of modulation were implemented and tested. A field-oriented vector control for speed on an induction motor was implemented. The vector control was combined with the vector modulation and many interesting measurements were done.
Possible future applications for this converter type are high-power industrial drives where motors must be fed with high voltages, but also high-speed motor drives like the hallbach magnetical arrays, where the voltage output must be of very high quality, even at high motor speeds. Motors based on the hallbach magnetical arrays have only got a very small phase inductance so they feeding must be done with a very high quality voltage. In the future, these motors can be used to drive flywheels and turbines at speeds up to 200'000rpm.

The DC-DC converter presented in chapter 4 is adapted to the feeding needs of the four-quadrant converters in a multilevel converter setup. The DC-DC converter proposed has a controlled output voltage and provides two-quadrant operation, where the feeding voltage is always positive and the load current can be positive and negative. Different modulation methods have been developed and an appropriate control system has been studied. Two different methods are defined: The rectangular current mode and the new combined triangular/trapezoidal current mode. The last method allows the DC-DC converter to operate in a hard-switched mode, but still with very few losses. The studied modulator types including their control system have been simulated and implemented on a 20kVA prototype. Two different medium-frequency transformer types have been studied and designed, namely a coaxial and a planar transformer. Of course a prototype for each transformer type has been realized in the laboratory. The transformers have been used in the experimental measurements with the proposed DC-DC converter.
The proposed DC-DC converter with the combined triangular/trapezoidal modulation seems to be the most efficient way to realize a voltage controlled DC-DC converter. However, the implementation of both methods is complicated and needs accurate measurements of all electrical values. As a result from this work a special DC-DC converter type is proposed, using only the triangular modulation method. A medium-frequency transformer with a winding ratio unequal to one is necessary.

Chapter 5 with the multilevel converter systems show simulations of the multilevel converter in three different configuration types for the same application: The front-end power AC-DC converter for locomotives, replacing the heavy low-frequency transformer and reducing the filtering elements. The three topologies are new converter types and they all present different advantages depending on their use. The first type show an implementation, where the locomotive does not need a line frequency filter for the pulsating power. This type is especially interesting for its low weight. A second type is a conventional type with controlled voltages feeding the four-quadrant converters. This type shows excellent performance concerning the line current quality. The third and last type is a configurable converter, which can be connected to the high voltage AC grid (15kV, $16\frac{2}{3}$Hz). By changing its configuration, the converter can be coupled to medium-frequency DC power lines (3kVDC). For all these three converter types, a complete simulation environment has been defined and many simulations have been done. Many other multilevel converter systems could be simulated using the same multilevel

converter principle, like a static VAR compensators, FACTS, electronic transformers for high-voltage lines.

My overall conclusion is that the multilevel converter has a large potential for various future applications.

Appendix A

Algorithms and mathematical developments

A.1 Harmonics on converter voltage using step modulation

The developed equations are based on a sum of square wave signals with different commutation angles. All of those functions are summed.

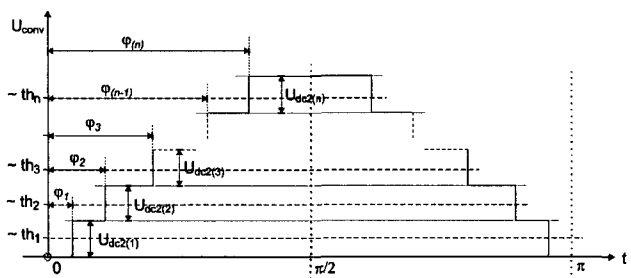

Figure A.1: Generalized step modulation waveform

The basic equation for the fourrier series is given with (A.1):

$$u(t) = \frac{a_0}{2} + \sum_{p=1}^{\infty} \left(a_p cos \frac{p\pi t}{T_{line}} + b_p sin \frac{p\pi t}{T_{line}} \right) \tag{A.1}$$

The average value of the waveform is equal to zero, so all the parameter a_0 is zero. The function is developed around a fundamental sinusoidal function, so all parameters a_p are zero too. By replacing the period T with π, the following series is found:

$$u(t) = \sum_{p=1}^{\infty} \frac{1}{\pi} \int_0^{2\pi} f(t) sin(pt) dt \cdot sin(pt)$$

$$= \frac{4}{\pi} \cdot \sum_{p=odd}^{\infty} \left(U_{dc2(1)} \cdot \int_{\varphi_1}^{\frac{\pi}{2}} sin(pt)dt + U_{dc2(2)} \cdot \int_{\varphi_2}^{\frac{\pi}{2}} sin(pt)dt + ... \right. \quad \text{(A.2)}$$
$$\left. + U_{dc2(n)} \cdot \int_{\varphi_n}^{\frac{\pi}{2}} sin(pt)dt \right) sin(pt)$$

The letter n represents the number of 4Q-converters used for the ML-converter. The feeding voltage is constant and is represented now by the symbol $U_{dc2(i)}$. The index i is for the step number and is in the interval $[0..n]$. Of course all the feeding voltages are equal:

$$U_{dc2(i)} = U_{dc2(1)} = U_{dc2(2)} = ... = U_{dc2(n)} \quad \text{(A.3)}$$

$$U_{conv}(t) = \frac{4U_{dc2(i)}}{\pi} \sum_{j=odd}^{\infty} \left(\left[\frac{-cos(jt)}{j} \right]_{\varphi_1}^{\frac{\pi}{2}} + \left[\frac{-cos(jt)}{j} \right]_{\varphi_2}^{\frac{\pi}{2}} + .. \right.$$
$$\left. + \left[\frac{-cos(jt)}{j} \right]_{\varphi_n}^{\frac{\pi}{2}} \right) sin(jt) \quad \text{(A.4)}$$

In this series it can be seen that the expression

$$cos\left(\frac{n\pi}{2}\right) = 0 \quad \text{(A.5)}$$

is zero if n is an odd number. The next Expression (A.6) gives all the harmonics in relation with a timebase t and a fundamental frequency ω_{line}:

$$U_{conv}(t) = \frac{4U_{dc2(i)}}{\pi} \sum_{j=odd}^{\infty} \sum_{k=1}^{n} cos(j \cdot \varphi_k) \frac{sin(j\omega_{line}t)}{j} \quad \text{(A.6)}$$

A.2 Algorithm for PWM voltage symmetrization

The presented algorithm is used for the equal distribution of all commutation events for a PWM multilevel voltage. This algorithm looks at the sequence of the values of the phase voltage u_R. If there is a rising voltage, one of the three partial voltages is risen. The next time when u_R is risen, the next partial voltage is risen. The same algorithm is applied to the falling voltages of u_R.

```
risefall[i+1]=uR[i]-uR[i+1]

if risefall[i+1] = -1
    if rise1 = 0
        uR1[i+1] := uR1[i]+1;
        uR2[i+1] := uR2[i];
        uR3[i+1] := uR3[i];
        rise1    := 1;
        elseif rise2 = 0
            uR1[i+1] := uR1[i];
            uR2[i+1] := uR2[i]+1;
            uR3[i+1] := uR3[i];
            rise2    := 1;
            elseif rise3 = 0
```

```
                uR1[i+1] := uR1[i];
                uR2[i+1] := uR2[i];
                uR3[i+1] := uR3[i]+1;
                rise3    := 1;
            end
        end
    end
end

if risefall[i+1] = 1
    if fall1 = 0
        uR1[i+1] := uR1[i]-1;
        uR2[i+1] := uR2[i];
        uR3[i+1] := uR3[i];
        fall1    := 1;
        elseif fall2 = 0
            uR1[i+1] := uR1[i];
            uR2[i+1] := uR2[i]-1;
            uR3[i+1] := uR3[i];
            fall2    := 1;
            elseif fall3 = 0
                uR1[i+1] := uR1[i];
                uR2[i+1] := uR2[i];
                uR3[i+1] := uR3[i]-1;
                fall3    := 1;
            end
        end
    end
end

if risefall[i+1] = 0
    uR1[i+1] := uR1[i];
    uR2[i+1] := uR2[i];
    uR3[i+1] := uR3[i];
end
```

By applying this algorithm to all the three phase voltages, the losses in commutation and conduction are shared equally by each four-quadrant converter.

A.3 Evaluations on the AC link of the DC-DC converter

The AC link of the DC-DC converter is reduced only to one impendance and is shown in Figure (A.2). From the two AC voltages U_{ac1} and U_{ac2}, only the fundamental sine wave is taken. Therefore with the Fourrier series the fundamental of the rectangular square wave could be found, named U_{s1} and U_{s2}:

$$U_{ac1} = \frac{4}{\pi} U_{dc1} \left[cos(\Omega_{d1}) sin(\omega_p t + \delta) + \frac{1}{3} cos(3\Omega_{d1}) sin(3\omega_p t + 3\delta) + \frac{1}{5} \ldots \right] \quad \text{(A.7)}$$

The fundamental wave is given by Equation (A.8)

$$U_{s1} = \frac{4}{\pi} U_{dc1} cos(\Omega_{d1}) sin(\omega_p t + \delta) \quad \text{(A.8)}$$

With the same Fourrier series evaluation, the expression for the second full-bridge is found:

$$U_{ac2} = \frac{4}{\pi} U_{dc2} \left[cos(\Omega_{d2}) sin(\omega_p t) + \frac{1}{3} cos(3\Omega_{d2}) sin(3\omega_p t) + \frac{1}{5} cos(5\Omega_{d2}) \ldots \right] \quad \text{(A.9)}$$

The fundamental wave is given by Equation (A.10)

$$U_{s2} = \frac{4}{\pi} U_{dc2} cos(\Omega_{d2}) sin(\omega_p t) \tag{A.10}$$

For an easier handling of the equations, the voltages and currents will now only be expressed by their fundamentals. This also allows to work with the phasors in the complex plane. Therefore the new expressions for the phasors are mentioned below:

$$\underline{U}_{s1} = U_{s1} \exp(j\omega_p t + j\delta) \tag{A.11}$$
$$\underline{U}_{s2} = U_{s2} \exp(j\omega_p t) \tag{A.12}$$
$$\Delta\underline{U}_s = \Delta U_s \exp(j\omega_p t + j\varphi_{\Delta U_s}) \tag{A.13}$$

The amplitudes $\hat{U}_{s1}$ and $\hat{U}_{s2}$ are defined in the Equation set (A.17). The amplitude $\Delta\hat{U}_s$ and the phase angle $\varphi_{\Delta U_s}$ can be calculated using trigonometric relations.

$$\hat{U}_{s1} = \frac{4}{\pi} U_{dc1} cos(\Omega_{d1}) \tag{A.14}$$
$$\hat{U}_{s2} = \frac{4}{\pi} U_{dc2} cos(\Omega_{d2}) \tag{A.15}$$
$$\Delta\hat{U}_s = \sqrt{\hat{U}_{s1}^2 + \hat{U}_{s2}^2 - 2\hat{U}_{s1}\hat{U}_{s2} cos(\delta)} \tag{A.16}$$
$$\varphi_{\Delta U_s} = \arctan\left(\frac{\hat{U}_{s2} - \hat{U}_{s1} cos(\delta)}{\hat{U}_{s1} sin(\delta)}\right) + sgn(\delta)\frac{\pi}{2} \tag{A.17}$$

These phasors are now related to a reduced equivalent scheme of the intermediary circuit shown in Figure (A.2).

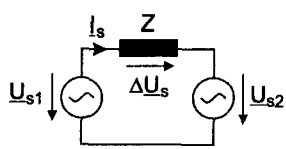

Figure A.2: Equivalent scheme for the AC intermediary circuit

The next Figure shows the phasor diagram for the equivalent circuit. All the following Equations for the DC-DC converter are based on this vector representation.

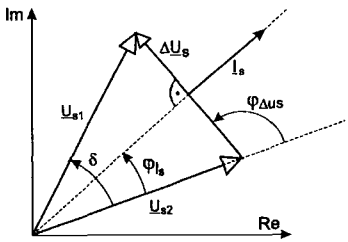

Figure A.3: Phasor diagram for the values on the intermediary circuit

In accordance to the components given in Figure (A.3), the impedance Z of the reduced equivalent circuit has to be calculated as follows: The value of the two resistance R_p of the transformer and inductor windings are very small (about 50mΩ for a 50kW transformer), so they can be neglected. The two capacitors for the filtering of the DC current are relatively big. In the stationary operation mode of the converter their influence is small and so they can be considered as a short-circuit. The main inductance of the transformer causes a magnetizing current I_m. By solving the Equations of Kirchhoff for the circuit in Figure (4.4), it can be seen that the magnetizing current has no influence on the current I_s. It has to be mentioned that due to the transformer ratio of one, primary and secondary currents have the same amplitude. The only components defining the current in the intermediary circuit are the two values of the stray inductance $L_{\sigma 1}$ and $L_{\sigma 2}$ and the decoupling inductance L_d. Therefore the impedance Z is:

$$L_{\sigma tot} = L_{\sigma 1} + L_{\sigma 2} + L_d \tag{A.18}$$

$$Z = 2\pi f_p L_{\sigma tot} \tag{A.19}$$

With the impedance Z the amplitude and phase angle of the current $\underline{I}_s$ can be found:

$$\hat{I}_s = \frac{\Delta \hat{U}_s}{Z} \tag{A.20}$$

$$\varphi_{Is} = \varphi_{\Delta U_s} - \frac{\pi}{2} \tag{A.21}$$

With these Equations the ideal behavior of the DC-DC converter is described only be using the fundamental waves of the electrical values. The current seen on the secondary side of the DC-DC converter, I_{dc2}, can be expressed by the average value of real part of the phasor current I_s. Also the voltage U_{dc2} can be expressed as the average value of the real part from $\underline{U}_{s2}$. Expressed in equations, the active power on the output of the converter can be found.

$$P_{dc2} = Re(\underline{U}_{s2} \cdot \underline{I}_s^*) \tag{A.22}$$

where $\underline{I}_s^*$ is the complex conjugate of the current $\underline{I}_s$. After several steps of mathematical evaluation:

$$P_{dc2} = \frac{\hat{U}_{s1}\hat{U}_{s2}sin(\delta) + \hat{U}_{s1}\hat{U}_{s2}sin(\delta + 2\omega_p t) + \hat{U}_{s2}^2 sin(2\omega_p t)}{2Z} \tag{A.23}$$

For the evaluation of the transfer function, all the oscillating components with two times the switching frequency $2\omega_p = 4\pi f_p$ components are not interesting. The aim is only to calculate the average power transfer. After removing the parts oscillating with 2ω and substituting $\hat{U}_{s1}$ and $\hat{U}_{s2}$ with the Equations (A.17) and (A.17), the final expression for the power transfer function can be found:

$$P_{dc2} = \overline{I}_{dc2} \cdot U_{dc2} = \frac{4U_{dc1}U_{dc2}sin(\delta)cos(\Omega_{d1})cos(\Omega_{d2})}{\pi^3 f_p L_{\sigma tot}} \tag{A.24}$$

The current $\overline{I}_{dc2}$ is the DC part of the DC-DC converter current I_{dc2}. The reactive power on the AC sides of the intermediary circuit can also be calculated. The following expression defines the reactive power:

$$Q_{ac1,2} = Im(\underline{U}_{s1,2} \cdot \underline{I}_s^*) \tag{A.25}$$

Equation (A.27) gives the reactive power for the primary and secondary side.

$$Q_{ac1} = \frac{4[{U_{dc1}}^2 cos^2(\Omega_{d1}) - U_{dc1}U_{dc2}cos(\delta)cos(\Omega_{d1})cos(\Omega_{d2})]}{\pi^3 f_p L_{\sigma tot}} \tag{A.26}$$

$$Q_{ac2} = \frac{4[U_{dc1}U_{dc2}cos(\delta)cos(\Omega_{d1})cos(\Omega_{d2}) - {U_{dc2}}^2 cos^2(\Omega_{d2})]}{\pi^3 f_p L_{\sigma tot}} \tag{A.27}$$

A.4 Design procedure for a medium-frequency transformer

In this appendix, a medium frequency transformer is designed using the procedure described in [42]. The design method starts on page 95. Many parameters for different core types are already given. A coaxial transformer with the following parameters is designed:

DC input voltage	U_{dc1}	500V
DC output voltage	U_{dc2}	500V
DC output current	$\overline{I}_{dc2}$	40A
DC output power	P_{dc2}	$20kVA$
Switching frequency	f_p	19.5kHz
Efficiency	η	$> 99.5\%$
Used maximal flux density	B_{max}	1T
Core maximal flux desnity	B_{max}	1.2T
AC voltage type		square wave
Core type		Tape wound ring core

Table A.1: Parameters for the designed coaxial transformer

The first step consists of calculating the effective DC output power

$$P_{dc2} = U_{dc2} \cdot \overline{I}_{dc2} = 20kW \tag{A.28}$$

The instantaneous power P_{inst} is defined in (A.29) and is calculated:

$$P_{inst} = P_{dc2} \cdot \left(\frac{\sqrt{2}}{\eta} + \sqrt{2} \right) = 56.57kW \tag{A.29}$$

The area product A_P is defined in the next Equation:

$$A_P = \left(\frac{P_{inst} 10^4}{K_f B_{max} f_p K_u J} \right)^{k_x} \quad \left[cm^4\right] \tag{A.30}$$

The area product A_P is also the defined as the product between the sum of the magnetic cross section of one core A_C and the window area W_a. The number of cores n_{cores} has to be found.

$$A_P = n_{cores} \cdot A_C \cdot W_a \quad \left[cm^4\right] \tag{A.31}$$

Fill factor (window utilization factor)	K_u	0.062	
Core geometrie constant	k_x	1.16	C-core
		1.15	Tape wound core
		1.14	Powder core
Voltage waveform constant	K_f	4	square wave
		4.44	sine wave
Current density	J	365	$\left[\frac{A}{cm^2}\right]$
Used maximal flux density	B_{max}	1	$[T]$
Surface of the window	W_a	12.57	$[cm^2]$
Magnetical cross-section one core	A_C	0.8	$[cm^2]$
Inductivity per turn	A_L	14	μH
Weight of one core		83	[g]

Table A.2: The equation coefficients

The numerical value for the area product is given in (A.32).

$$A_P = 762 \quad \left[cm^4\right] \tag{A.32}$$

In this moment, a core must be chosen, which corresponds to the desired application. In this case it has been decided to take uncut ring cores For each core the area product $A_P(core)$ must be calculated. The

$$A_{P(core)} = A_C \cdot W_a \quad \left[cm^4\right] \tag{A.33}$$

With the the next Equation (A.34), the number of needed cores are computed:

$$n_{core} = round\left(\frac{A_P}{A_{P(core)}} \right) = 20 \tag{A.34}$$

The number of needed turns on both sides of the transformer is based on the next Expression:

$$K_u \cdot W_a = N_1 \frac{I_{dc1}}{J} + N_2 \frac{I_{dc2}}{J} \tag{A.35}$$

The following expression is needed to calculate the number of turns in the transformator. Due to the symmetrical design for primary and secondary side, the number of turns is the same for both sides:

$$N_{1,2} = \frac{U_{dc1,2 \cdot 10^4}}{K_f B_{max} f_p n_{core} A_C} \tag{A.36}$$

The following Equation (A.38) set is used for the computing of the principle transformer inductance. The numerical value for A_L is usually given by the core manufacturer:

$$L_{p1} = N_1{}^2 \cdot A_L \tag{A.37}$$
$$L_{p2} = N_2{}^2 \cdot A_L \tag{A.38}$$

An aproximation for the inductance values can be given with the Equation (A.39)

$$L_{p1,2} \approx \frac{\mu_0 \mu_r N_{1,2} n_{core} A_C}{l} \tag{A.39}$$

The variable l is the length of the winding part inside of the magnetical cores. The maximal flux density in the cores must be checked and is given with:

$$B_{max} = \frac{\hat{I}_{ac1,2} \cdot L_{p1,2}}{n_{core} A_C N_{1,2}} \tag{A.40}$$

A.5 Coaxial transformer parameters

The Equations for the stray inductance and the coupling capacitance of a coaxial cable have been calculated analytically. The entire mathematical development can be found below. The Figure (A.4) is a cut view of the cable, where 3 diameters $R1$ to $R3$ are defined. The stored energy in a electrical field is defined by:

$$W = \int_{Vol} \frac{1}{2} \vec{D} \vec{E} dVol \tag{A.41}$$

For the dielectrical field, it can be found:

$$\vec{D} = \varepsilon \cdot \vec{E} \tag{A.42}$$

The parameter ε is the dielectrical constant of the insulation material. The electrical field $\vec{E}$ has only got a radial component. The variables φ_1 and φ_2 are the electrical potentials.

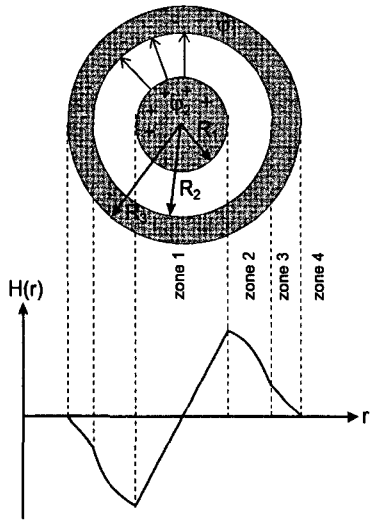

Figure A.4: View through a coaxial cable with the H-Field profile

The electrical field can be calculated as follows, by taking a constant A and saying that the field is inverse proportional to r:

$$U = \int_{R_1}^{R_2} E dr = \int_{R_1}^{R_2} \frac{A}{r} dr = A \cdot \ln \frac{R_2}{R_1} \tag{A.43}$$

After same developments:

$$A = \frac{\varphi_1 - \varphi_2}{ln\left(\frac{R_2}{R_1}\right)} \tag{A.44}$$

Therefore the electrical field with only a radial component is:

$$E_r = \frac{\varphi_1 - \varphi_2}{r ln\left(\frac{R_2}{R_1}\right)} = \frac{U}{r \cdot ln\left(\frac{R_2}{R_1}\right)} \tag{A.45}$$

So the mathematical development of Equation (A.41) gives the energy stored in the electrical field, depending on the cable length.

$$W = \int\int\int_{Vol} \frac{1}{2} \vec{D}\vec{E} dVol = \frac{1}{2}\varepsilon \int\int\int \vec{E}^2 dVol = \frac{1}{2}\varepsilon l \int_{R_1}^{R_2} 2\pi r \vec{E}^2 dr \tag{A.46}$$

$$= \pi\varepsilon l \int_{R_1}^{R_2} r \frac{(\varphi_1 - \varphi_2)^2}{r^2 ln\left(\frac{R_2}{R_1}\right)^2} dr = \pi\varepsilon\varphi \frac{(\varphi_1 - \varphi_2)^2}{ln\left(\frac{R_2}{R_1}\right)^2} \int_{R_1}^{R_2} \frac{1}{r} dr \tag{A.47}$$

$$= \pi\varepsilon l \frac{(\varphi_1 - \varphi_2)^2}{ln\left(\frac{R_2}{R_1}\right)^2} ln\left(\frac{R_2}{R_1}\right) = \pi\varepsilon_o\varepsilon_r l \frac{U^2}{ln\left(\frac{R_2}{R_1}\right)} \tag{A.48}$$

The Equation (A.48) can be divided by the length of the coaxial cable l. So the resulting Equation is the energy per meter cable:

$$\frac{W}{l} = \pi\varepsilon_o\varepsilon_r \frac{U}{ln\left(\frac{R_2}{R_1}\right)} \tag{A.49}$$

The Energy in a capcitor is definded by the following Equation and can be compared with Equation (A.48):

$$W = \frac{1}{2}CU^2 = \pi\varepsilon_o\varepsilon_r l \frac{U^2}{ln\left(\frac{R_2}{R_1}\right)} \tag{A.50}$$

By resolving the Equation to the capacitor C and eliminating the voltage U, it can be found:

$$C'_{tr} = \frac{2\pi\varepsilon_o\varepsilon_r}{ln\left(\frac{R_2}{R_1}\right)} \tag{A.51}$$

Now the inductivity for a coaxial cable is calculated, depending on the cable length. It is started with the energy W stored in a magnetical field:

$$W = \frac{1}{2}\int_{vol} \vec{B}\vec{H} \quad dvol = \frac{1}{2}\int\int\int_{vol} \mu_o \vec{H}^2 \, dvol \tag{A.52}$$

The magnetic field only has a component in the φ direction (tangential direction). Therefore it can be found:

$$W = \int_0^{R_3} \mu_0 H_\varphi(r)^2 2\pi r l \quad dr \tag{A.53}$$

The magentic field per length l of the cable is:

$$\frac{W}{l} = \mu_0 \int_0^{R_3} H_\varphi(r)^2 2\pi r \quad dr \tag{A.54}$$

From the Equation (A.54) is can be learned that the magnetic field in the tangential direction $H_\varphi(r)$ must be known. The Equation from Maxwell sais:

$$\oint_{\delta F} \vec{H}\vec{dl} = \int\int_F \vec{j}\vec{dF} = I \tag{A.55}$$

Adapted to the relative simple field situation in the coaxial cable, the Equation (A.55) can be rewritten in the following form given in Equation (A.56). The current I is the current flowing in the coaxial cable.

$$H_\varphi 2\pi r = I\frac{\pi r^2}{R_1{}^2} \tag{A.56}$$

The coaxial cable must now be analyzed in different radial zones. The zones are described in the Figure (A.4). For the *zone* 1, the following magentic field is found:

$$H_\varphi \cdot 2\pi r = I\frac{\pi r^2}{\pi {R_1}^2} \tag{A.57}$$

$$H_\varphi = \frac{I \cdot r}{2\pi {R_1}^2} \tag{A.58}$$

For the *zone* 2 it can be found:

$$H_\varphi \cdot 2\pi r = I \tag{A.59}$$

$$H_\varphi = \frac{I}{2\pi r} \tag{A.60}$$

The *zone* 3 is:

$$H_\varphi \cdot 2\pi r = I - I\frac{\pi(r^2 - {R_3}^2)}{\pi({R_3}^2 - {R_2}^2)} \tag{A.61}$$

$$H_\varphi = \frac{I}{2\pi r}\left(1 + \frac{{R_3}^2 - r^2}{{R_3}^2 - {R_2}^2}\right) \tag{A.62}$$

And finally for the *zone* 4 it can be found:

$$H_\varphi = 0 \tag{A.63}$$

And now by taking the Equation (A.54), the energy W per length l is calculated for the magnetic field.

$$\frac{W}{l} = \frac{\mu_o}{2}\left[\int_0^{R_1}\left(\frac{Ir}{2\pi {R_1}^2}\right)^2 2\pi r\,dr + \int_{R_1}^{R_2}\left(\frac{I}{2\pi r}\right)^2 2\pi r\,dr + \int_{R_2}^{R_3}\left[\frac{I}{2\pi r}\left(\frac{{R_3}^2 - r^2}{{R_3}^2 - {R_2}^2}\right)\right]^2 2\pi r\,dr\right] \tag{A.64}$$

The Equation (A.64) is resolved and set equal to the Equation

$$L'_{\sigma 1,2} = \frac{L}{l} = \frac{2}{I^2}\frac{W}{l} \tag{A.65}$$

After replacing $\frac{W}{l}$ with the result of Equation (A.64) the final Equation for the inductance per length for the coaxial cable is found:

$$L'_{\sigma 1,2} = \frac{\mu_o}{2\pi}\left[ln\left(\frac{R_2}{R_1}\right) + \frac{{R_3}^2}{2({R_3}^2 - {R_2}^2)} + \frac{{R_3}^2}{({R_3}^2 - {R_2}^2)^2} ln\left(\frac{R_3}{R_2}\right)\right] \tag{A.66}$$

A.6 DC ripple current

A MATLAB algorithm is shown in this appendix, in order to calculate the DC ripple current for an m to p configurable multilevel converter.

```
% parameters

Udc2    = 2800;
p   = 2;
m   = 5;
fs  = 250;
Lline   = 0.005;

% algorithm

n   = m*p;

for i = 1:1000

k(i)    = i/500-1;
D(i)    = p*k(i)-floor(p*k(i));
D2(i)   = D(i)-floor(m*D(i))/m;
Ipp(i)  = Udc2/Lline/2/n/fs*(1-m*D2(i))*D2(i);

end %for

subplot(211);
plot(k,Ipp);
subplot(212);
plot(k,D,k,D2);
```

A.7 Numerical values to compute the losses

The following Table (A.3) are showing the loss energies for power energies. The IGBT losses are calculated losses taken from the datasheets of Eupec power modules, with the maximal switched voltage 4.5kV and maximal on-state current of 400A. The silicium carbide values are only estimated future values.

Semiconductor technology	Switched voltage	Switched current	Switching loss energy	Saturation voltage
IGBT	2.8kV	250A	$W_{off} = 1.1$Ws $W_{on} = 0.98$Ws	$U_{ce(sat)} = 4.2$V
IGBT diode			$W_{off} = 0.32$Ws	$U_d = 3.1$V
SiC	2.8kV	250A	$W_{off} = 0.3$Ws $W_{on} = 0.27$Ws	$U_{ce(sat)} = 5$V
SiC diode			$W_{off} = 0.12$Ws	$U_d = 3.6$V

Table A.3: Numerical values used for the losses evaluation

The losses are considered to depend linearly on the switched voltage and current. The following equation shows the losses computing:

$$P_{loss} = f_s \cdot \frac{I_C}{250A} \cdot \frac{U_{CE}}{2.8kV} \cdot W_{on,off} \tag{A.67}$$

The conduction losses are computed depending on the on-state current. The saturation voltage is considered to be constant.

Appendix B

Polyphase transformers for AC feeding

The first low-frequency transformer feeding circuit is shown in Figure (B.1). This is not a polyphase transformer. Each secondary transformer winding has a three-phase rectifier, feeding a 4Q-converter of the multilevel converter. There is no problem of symmetrical power sharing, independent of the number of multilevel cells.

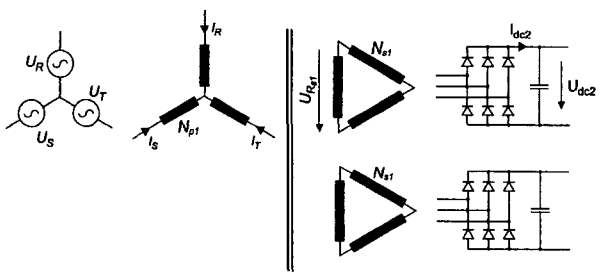

Figure B.1: Multilevel converter feeding by three-phase diode bridges

Due to the fact that there are three phases, there will be a oscillation of 300Hz on the capacitors at load. This can be seen in the Figure (B.2). This Figure represents a simulation done with SIMPLORER using the parameters of the Table (B.1):

Parameter	Symbol	Value
Line voltage	$\hat{U}_{R,S,T}$	$400V$
Winding ratio	$w_r = \frac{N_{s1}}{N_{p1}}$	2.188
DC output voltage	U_{dc2}	$400V \cdot \sqrt{3}$
DC output power	P_{dc2}	$28kW$
Stray resistance primary	R_{p1}	$300m\Omega$
Stray resistance secondary	R_{p2}	$400m\Omega$
Stray inductance primary	$L_{\sigma 1}$	$1mH$
Stray inductance secondary	$L_{\sigma 2}$	$900\mu H$
Main inductance transformer	L_p	$100mH$
DC Output capacitor	C_{dc2}	$680\mu F$
Internal resistance current source	R_{dc2}	2Ω

Table B.1: Simulation parameters for the three-phase rectifier

The simulation shows the currents on the AC side, where the grid is feeding the transformer. The currents are not sinusoidal and have a important harmonic at 300Hz. But the use of three-phase rectifier bridges only leaves a small ripple voltage on the output DC capacitor with the same frequency of 300Hz.

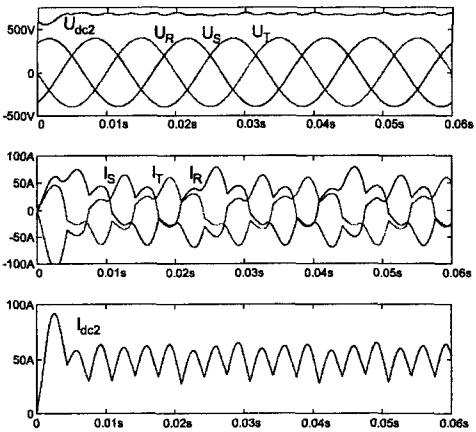

Figure B.2: Simulation of the feeding with simple three-phase rectifier bridge

The rectifier bridges at least generate AC currents with no DC component on the primary side, but there is much low-order harmonic content. The proposed solution with the rectifier bridges can be improved. The disadvantage of this solution is the poor current quality by having non-sinusoidal peak currents on the line side. Therefore the basic idea is to use several secondary coils, each of them generating a phase-shift between the phase of the voltage and the current, called polyphase transformers.

The transformer circuit can be improved by using a special transformer winding on

the secondary side, taking advantage of the possibility to generate phase-shifted voltages on the secondary side of the transformer, to be seen in [21]. These types of transformers are called polyphase transformers. The feeding topology below shows a solution, if the number of multilevel converter cells are a multiple of 2:

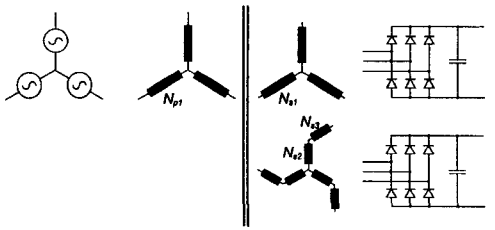

Figure B.3: Multilevel converter fed by 12-pulse polyphase transformer

The upper coil in star configuration does not generate any phase shift comparing to the primary side. But the lower one with the special middle-point connection generates a phase-shift of 30^o. This generates two pairs of phase-shifted current peaks. For the whole transformer, there are twelve current peaks. That is why the transformer is called 12-pulse polyphase transformer. This is a well-known transformer configuration, so no simulation is done on this topology. The next Figure (B.4) shows a special transformer with phase-shifted secondary windings of 20^o. This transformer is ideal, if the number of multilevel cells is a multiple of 3.

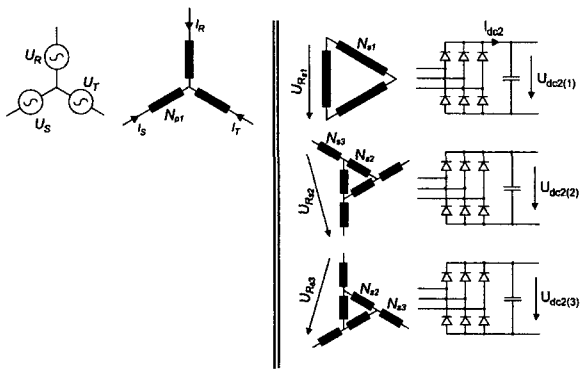

Figure B.4: Multilevel converter fed by 18-pulse polyphase transformer

The topology generates three three-phase voltage systems, each of them with a phase shift of 20^o. A simulation of this topology has been done using Simplorer. The Table (B.2) contains the used parameters for the simulation:

Parameter	Symbol	Value
Line voltage	$\hat{U}_{R,S,T}$	$400V$
Winding ratio 1	$w_r = \frac{N_{s1}}{N_{p1}}$	0.76
Winding ratio 2	$w_r = \frac{N_{s2}}{N_{p1}}$	0.864
DC output voltage	U_{dc2}	$400V \cdot \sqrt{2}$
DC output power	$P_{dc_{1,2,3}}$	$28kW$
Stray resistance primary	R_{p1}	$300m\Omega$
Stray resistance secondary	R_{p2}	$400m\Omega$
Stray inductance primary	$L_{\sigma 1}$	$1mH$
Stray inductance secondary	$L_{\sigma 2}$	$900\mu H$
Main inductance transformer	L_p	$100mH$
DC Output capacitor	C_{dc2}	$680\mu F$
Internal resistance current source	R_{dc2}	2Ω

Table B.2: Simulation parameters for the 18-pulse polyphase transformer

The simulation results are given with Figure (B.5):

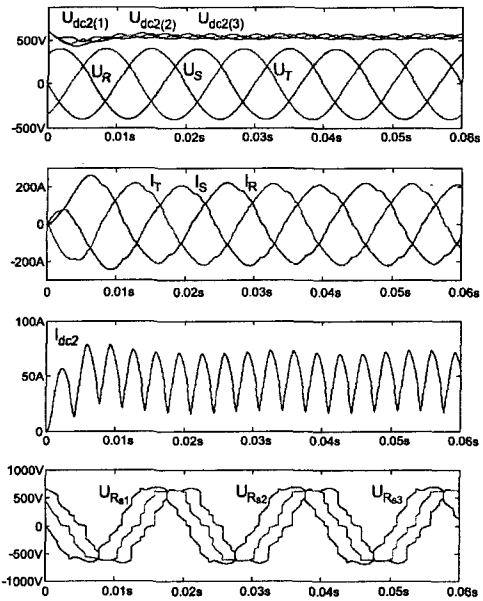

Figure B.5: Simulation of the feeding with 18-pulse polyphase transformer

The main difference between the two simulations is the quality of the current on the line side of the feeding: By using the 18-pulse transformer, the currents are nearly sinusoidal, due to the passive current harmonics cancellation. The currents are phase-shifted comparing with the concerning phase voltages. The transformer is an inductive

load, so the currents are delayed comparing to the voltages. The last graph of the simulation shows the voltages on the secondary side of the transformer, all from phase R: The special winding of the transformer has created a phase-shift of 20^o between the voltages $U_{R_{s1}}$, $U_{R_{s2}}$ and $U_{R_{s3}}$.

Appendix C

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Appendix D

Glossary

α_k	Phase shift angle between U_{line} and U_{conv}
α_c	Phase shift angle between U_{line} and I_{line}
δ	Phase-shift as a modulation parameter of the DC-DC converter
δ_1, δ_2	Preliminary phase-shift values for δ
δ_{skin}	Penetration depth due to the skin effect
ε_o	Dielectrical constant ($8.854 \cdot 10^{-12}$)
ε_r	Relative dielectricity (insulation material)
$\overline{\delta}_{abs}$	Absolute average value for δ
δ_{lim}	Limited value for δ from the controller
δ_{nom}	Nominal phase-shift for the DC-DC converter
δ_{max}	Maximal tolerated phase-shift on the the AC link voltages
$\delta_{Pmin,rec}$	Value for δ for minimal power in the rectangular mode
$\delta_{Pmax,rec}$	Value for δ for maximal power in the rectangular mode
$\delta_{Pmin,trap}$	Value for δ for minimal power in the trapezoidal mode
$\delta_{Pmax,trap}$	Value for δ for maximal power in the trapezoidal mode
$\delta_{Pmin,tri}$	Value for δ for minimal power in the triangular mode
$\delta_{Pmax,tri}$	Value for δ for maximal power in the triangular mode
$\Delta\varphi_i$	Phase-shift angles between modulation carrier signals
$\Delta\varphi_{R(i),S(i),T(i)}$	Phase-shift angles between carrier signals of the phases R, S, T
$\Delta\psi_i$	Phase-shift angles between modulation carrier signals for configurable converter
$\Delta\underline{p}$	Difference between two power vector points (three-phase)
$\Delta\underline{u}$	Difference between two voltage vector points (three-phase)
$\Delta\underline{U}_s$	Differential voltage vector over the total inductance $L_{\sigma tot}$
$\Delta U_{dc2(i)}$	Peak-peak voltage oscillation
η	Efficiency (DC-DC converter)
μ_0	Magnetical constant ($4\pi 10^{-7}$)
$\varphi_{(i)}$	Firing angles for the step modulation
φ_R, φ_S, φ_T	Phase angle R,S and T for motor converter
$\varphi_{\Delta\underline{U}}$	Phase shift angle between U_{line} and $\Delta\underline{U}$
ω	Frequency
ω_{line}	Frequency of the line voltage

ω_p	Fundamental frequency of the AC voltages in the DC-DC converter
ω_{res}	Resonant frequency of a controller
ω_s	Fundamental frequency of the switching in a 4Q-converter
Ω_{d1},$\Omega_{d1(i)}$	Primary side DC-DC converter modulation parameter
Ω_{d2},$\Omega_{d2(i)}$	Secondary side DC-DC converter modulation parameter
σ	Attenuation factor of observer transfer function
σ_R	Conductivity of the material. Copper: $\frac{1}{1.7 \cdot 10^{-8}}$
$\tau_{blank(4Q)}$	Blanking time 4Q
τ_{blank}	Blanking time DC-DC
τ_{offset}	Threshold value to activate the step modulator
a	Component of the linear equation $ax + b$ to find the reference triangle
$\underline{a}$	Linear combination vector for vector modulation
aux_i	Carrier signals for the PWM modulation
A	Geometrical surface (conductors)
A_C	Magnetical core effective cross-section
A_P	Area product of the transformer
$\underline{A}$	System matrix of the observer
b	Component of the linear equation $ax + b$ to find the reference triangle
$\underline{b}$	Linear combination vector for vector modulation
B_{max}	Maximal flux density of a transformer
$\underline{c}^T$	Output vector of the observer
$ce(i)$	Multilevel converter group
$C_{(i)}$	Capacitors
C_{clamp}	Clamping capacitor for DC-DC converter snubber
C_{d1},C_{d2}	AC link decoupling capacitors
C_d	Simplified AC link decoupling capacitor
C_{dc2}, $C_{dc2(i)}$	Intermediary capacitors to stabilize 4Q-converter feeding
$C_{dc2R,S,T}$	Intermediary capacitors in the three-phase converter
C_{dc1}	DC link capacitor
$C_{para(i)}$	Parasitic capacitors of power semiconductors
C_R	Resonant capacitors for a DC-DC converter
C_{trap}	Trap circuit filter capacitor
C_{tr}	Coupling capacitor primary-secondary side
C'_{tr}	Coupling capacitor per meter coaxial cable
C_{filter}	Filter capacitor for the front end multilevel switching
$CL_{(i)}$	Clamping diodes for a NPC converter type
d	Geometrical distance
$d_{1new,2new,3new}$	Distances used in vector modulation
D	Duty cycle of a switched converter voltage
$D1 - D8$	Power diodes of the DC-DC converter
D_2	Limited duty cycle for computing
ex_1,ex_2,ex_3	Expression simplification parameter
f_{line}	Line frequency

f_{mod}	Fundamental frequency for motor converter modulation
f_s	Switching frequency 4Q
f_p	Switching frequency DC-DC
$f_{p(max)}$	Maximal possible switching frequency for the DC-DC converter
f_{LC}	Resonant frequency LC circuit of the AC link
$f_{res(HSCS)}$	Resulting switching frequency for the HSCS PWM modulation
$f_{res(VSCS)}$	Resulting switching frequency for the VSCS PWM modulation
$\underline{g}$	Feedback vector of the observer
$G_{cm1}(s)$	Transfer function for the line current controller
$G_{cm3}(s)$	Transfer function constant individual 4Q-converter controller
$G_{cm5}(s)$	Transfer function in the DC-DC converter
$G_{cm6}(s)$	Transfer function in the configurable converter (DC)
$G_{R1}(s)$	Line current controller transfer function
$G_{R1\alpha}(s)$, $G_{R1\beta}(s)$	Two components of the line current controller
$G_{R2}(s)$	Power flow controller transfer function
$G_{R3(i)}(s)$	Controller number i for the modulation degree for each 4Q-converter
$G_{R4(i)}(s)$	Active current filtering controller for each harmonic
$G_{R5}(s)$, $G_{R5(i)}(s)$	Controller number i to control the voltage of the DC-DC converters
$G_{R6(i)}(s)$	DC current controller for the configurable converter
$G_{sa1}(s)$	System transfer function inner system cascaded power flow controller
$G_{sb2}(s)$	System transfer function outer system cascaded power flow controller
$G_{sb2}(s)$	System transfer function outer system active current filtering
$G_{s5}(s)$	System transfer function of the DC-DC converter
$G_{wa1}(s)$	Internal controller loop cascaded power flow controller
$G_{wa4}(s)$	Internal controller loop active filtering controller
$\underline{h}$	Observer output vector generating imaginary part
i	Index used for the step number
I^r_α, I^r_β	Components of the current referenced to a rotating coordinate system
$I^r_{\alpha(set)}$, $I^r_{\beta(set)}$	Set value components referenced to the rotating coordinate system
$I^r_{\alpha(err)}$, $I^r_{\beta(err)}$	Error value components referenced to the rotating coordinate system
I_{ac}	Medium-frequency AC current in a DC-DC converter transformer
$\hat{I}_{ac}$	Peak current value in the AC link for inductor design
$\hat{I}_{ac1}$, $\hat{I}_{ac2}$	Peak current values in the DC-DC converter AC link
$\hat{I}_{ac1(abs)}$, $\hat{I}_{ac2(abs)}$	Average absolute turn-off currents
$\hat{I}_{ac1(max)}$	Peak current in the load mode of the DC-DC converter
$I_{C(i)}$	Capacitor currents imbricated cells
$I_{c(max)}$	Maximal collector current of an IGBT
$I_{corr(DC)}$	Correction value for the DC current
I_{ch2}, $I_{ch2(i)}$	DC current generated by the 4Q-converter
$I_{ch2R,S,T}$	DC current from 4Q-converter in three-phase configuration
$I_{ch2(max)}$	DC current generated by the 4Q-converter
$\hat{I}_{ch2}$	Maximal load current
$\overline{I}_{dc1(i)}$	Partial DC link feeding currents (coming from DC-DC converter)

$I_{dc1(tot)}$	Overall DC link feeding current
I_{dc2}	Intermediary capacitor feeding current (coming from DC-DC converter)
$\overline{I}_{dc2}$, $\overline{I}_{dc2(i)}$	DC component of the DC-DC converter current
$\overline{I}_{dc2(abs)}$	Absolute average DC-DC converter current
$\overline{I}_{dc2(cont)}$	PI-controller value current from the tri/trap modulation
$\overline{I}_{dc2(lim)}$	Limited value for the DC-DC converter current
$\overline{I}_{dc2(tot)}$	Total to be limited current from the DC-DC converter
$\widehat{I}_{harm(i)}$	Current amplitudes of the harmonics
$\widehat{I}_{harm(i)(set)}$	Current set value amplitudes for the harmonics
$\widehat{I}_{hcorr(i)}$	Current amplitudes from active filtering controller
I_{hcorr}	Time-dependent current from the active filtering controllers
I_{line}	Line voltage going to the catenary
$\widehat{I}_{line}$	Monophasor amplitude (line current amplitude)
$\underline{I}_{line}$	Monophasor vector for the line current
$I_{line(im)}$	Current phasor in the complex plane, y-component
$I_{line(re)}$	Current phasor in the complex plane, x-component
$I_{line(DC)}$	DC component of the line current
$I_{line(i)}$	Partial line voltage in the configurable converter
$I_{line(err)}$	Error of the line current
$I_{line(set)}$	Set value for the line current I_{line}
I_{margin}	Security margin current for the inductor L_d
I_m	Magnetizing current of the transformer
I_{mot}	Motor current consumed from the DC-link
$I_{mot(set)}$	Set value for the motor current
$\underline{I}^r$	Current vector references to the rotating coordinate system
$\underline{I}^r_{set}$	Current vector set value for the rotating coordinate system
I_{ripple}	AC current ripple on the line current, in the configurable converter
$I_{ripple(i)}$	AC current ripple on the partial line current
I_s	Fundamental sine-wave of the DC-DC converter AC link current
$\underline{I}_s$	Monophasor of the sine-wave of the DC-DC converter AC link current
$\widehat{I}_s$	Amplitude of the monophasor of the AC link current
j	Index used for summations
J	Current density in conductors
k	Modulation degree applied to the converter modulator
k'	Modulation degree coming from the current controller
$\underline{k}^r$	Modulation vector in the rotating coordinate system
$\underline{kk}^r$	Controller output vector in the rotating coordinate system
k^r_α, k^r_β	Vector components of the modulation vector
kk^r_α, kk^r_β	Vector components of the controller output vector
$k_{(i)}$	Modulation degree for an independent 4Q-converter
$k_{c_{1,2,3}}$	Correction value for the vector modulation
$k_{n_{1,2,3}}$	Distance parameter for the vector modulation
$k_{R,S,T}$	Modulation degree of phase R,S and T

K_{cm1}	Amplification factor between k and a 4Q-converter
K'_{cm1}	Amplification factor between k and a multilevel converter
K_{cm3}	Amplification factor individual 4Q-converter controller
K_{cm5}	Amplification factor of the DC-DC converter control
K_{cm6}	Amplification factor of a converter group $ce(i)$, configurable converter
K_{iline}	Current feed-forward amplification
K_{fb}	Proportionality between AC line current and DC current value
K_{p1}, K_{i1}	Proportional and integral part line current controller
K_{p2}, K_{i2}	Proportional and integral part power flow controller
K_{p3}, K_{i3}	Proportional and integral part 4Q-converter modulation degree controller
K_{p4}, K_{i4}	Proportional and integral part active current filtering controller
K_{p5}, K_{i5}	Proportional and integral part DC-DC converter voltage controller
K_{p6}, K_{i6}	Proportional and integral part DC current controller (configurable converter)
K_{s1}	Amplification of the line current transfer function
K_{s5}	Amplification of the DC-DC converter transfer function
K_u	Fill factor or window utilization factor
K_{udc2}	DC voltage U_{dc2} feed-forward amplification
K_{uline}	Voltage feed-forward amplification
K_{v6}	Amplification direct introduction of perturbation value
l	Length, distance
l_1, l_2, l_3	Distance between proposed and optimal switching pattern
$L_{\sigma tot}$	Decoupling inductance DC-DC
$L_{\sigma 1}$, $L_{\sigma 2}$	Primary and secondary side stray inductance
$L'_{\sigma 1}$, $L'_{\sigma 2}$	Stray inductance per meter coaxial cable
L_{line}	Line inductance
$L_{line(i)}$	Partial line inductance (configurable converter)
L_{trap}	Trap circuit filter inductor
L_{p1}, L_{p2}, L_p	Primary, secondary and total principle inductance
L_r	Resonant inductor used for snubber in a DC-DC converter
L_{r1}, L_{r2}	Resonant inductors for a DC-DC converter
L_{sat}	Square loop core inductor for DC-DC converter
m	Number of multilevel converter groups
n_c	Number of switching operations in one sampling time T_{sample}
n_{core}	Number of cores for a transformer
n_d	Order of the FIR filter
n	Number of converter steps
n_{aux}	Number of carrier signals per multilevel converter
n_c	Number of switched voltage levels
$n_{c_{min}}$	Minimal number of switched voltage levels
n_{DFT}	Number of sampling periods for the DFT algorithm
n_h	Number of the hexagon of the voltage phasor points
n_{hmax}	Maximal order of the filtered current harmonics
n_{harm}	Order of the current harmonics

n_{phasor}	Number of visible phasor vector points
n_s	Number of redundant voltage phasor patterns for one phasor point
n_{step}	Number of active steps during the step modulation
$n_{voltage}$	Number of different voltage steps generated by a ML-converter with n steps
$\underline{n}$	Unity vector
$\underline{n}_{power}$	3D current direction vector
N_1	Number of windings on the primary transformer side
N_2	Number of windings on the secondary transformer side
p	Number of 4Q-converters in a multilevel converter group
$\underline{p}$	Normalized power vector for vector modulation
p_{observ}	Characteristical polynomial of the observer
P_{dc2}	*Output power of the DC-DC converter*
$P_{dc2(nom)}$	Nominal power of the DC-DC converter
P_{mot}	Motor power, maximal value
P_{tot}	Multilevel converter power
P_α^s	Power phasor plane axis to represent the motor power, x-axis
P_β^s	Power phasor plane axis to represent the motor power, y-axis
Q_{ac1}, Q_{ac2}	Reactive power on both sides of the AC link
$\underline{r}$	Decomposition vector for vector modulation
$\underline{r}_1$, $\underline{r}_2$, $\underline{r}_3$	Projection vectors for switching losses optimization
res	Resolution of an AD-converter
R	Resistor
$\underline{R}$	Rotation matrix to turn coordinates by 90° clockwise
R_1, R_2, R_3	Radius of the coaxial cable
R_{chop}	Chopper resistance
R_{dc2}	Internal resistance DC source
R_{filter}	Filter resistor for the front end multilevel switching
R_{line}	Resistive part of the line inductance
R_{p1}, R_{p2}	Primary and secondary side stray resistance
R_{trap}	Resistive part of the trap circuit inductor
$\underline{s}$	Decomposition vector for vector modulation
s_i	Non-optimized switching function for the power semiconductors
s_i'	Optimized switching function
s_1, s_2	Poles of the characteristic polynomial
S_j	Quantification function for a modulation
t_a, t_b	Proportional factors of the modulation times in the vector modulation
$th_{(i)}$	Threshold values for the step modulation
$\underline{T}$, $\underline{T}^{-1}$	Transformation matrix for the rotating coordinate system
$T1 - T8$	Power semiconductors of the DC-DC converter
T_{11}	*System transfer function time constant for meplat design criteria*
T_{15}	DC-DC converter transfer function time constant for meplat design criteria
T_a, T_b, T_c	Modulation times for the vector modulation
T_a2	Time constant inner controller loop cascaded controller power flow controller

T_a4	Time constant inner controller loop cascaded controller active filter
T_{clamp}	Clamping power semiconductor
T_{cm2}	Small time constant due to the 4Q-converter modulation
T_{cm5}	Small time constant due to the DC-DC converter modulation
T_{cm6}	Small time constant of a converter group $ce(i)$, configurable converter
T_{filt6}	Filter time constant for DC current controller configurable converter
T_{fs}	$33\frac{1}{3}$Hz frequency filter sampling time
T_{I1}	Integral time constant of the line inductor in monophased control
T_{I2}	Integral time constant of the cascaded power flow controller
T_{I5}	Integral time constant of the DC-DC converter output capacitor
T_{Iline}	Overall line current fundamental period, configurable converter
$T_{Iline(i)}$	Partial line current fundamental period
T_{line}	Line voltage fundamental period
T_{n1}, T_{i1}	Proportional and integral part line current controller
T_{n2}, T_{i2}	Two time constants of power flow controller
T_{n3}, T_{i3}	Two time constants of 4Q-converter modulation degree controller
T_{n4}, T_{i4}	Two time constants of active current filtering controller
T_{n5}, T_{i5}	Two time constants of DC-DC converter voltage controller
T_{n6}, T_{i6}	Two time constants of part DC current controller (configurable converter)
T_{on}, T_{off}	Switching times for power semiconductors
T_{pE1}	Small time constant line current controller
T'_{pE3}	Small time constant individual 4Q-converter controller
T_{pE5}	Small time constant DC-DC converter controller
T_{pE6}	Small time constant configurable converter, DC configuration
T_{r2}, T_{r5}	Measurement delay and delay time generated by the control algorithm
T_{sample}	Sampling time
$u_\alpha{}^s$, $u_\beta{}^s$	Normalized phasor vector components
u_0	Normalized zero-point voltage of the three phase converter
$\underline{u}_1$, $\underline{u}_2$, $\underline{u}_3$	Normalized voltage vectors from the reference triangle
$\underline{u}_{new}$	Resulting new voltage vector from an algorithm
u_R, u_S, u_T	Normalized phase voltages of a motor converter
$\underline{u}_{ref}$	Normalized reference vector for modulation
$\hat{u}_{ref}$	Amplitude reference vector for modulation
$\underline{u}_{ref_x}$, $\underline{u}_{ref_y}$	Reference vector for modulation components
$U_\alpha{}^s$, $U_\beta{}^s$	Phasor vector components
U_0	Zero-point voltage of the three phase converter
U_{ac1}, U_{ac2}	Medium-frequency AC voltages applied to the transformer
U'_{ac2}	Medium-frequency AC voltage referred to the primary side
$U_{c(i)}$	Capacitor voltages imbricated cells multilevel converter
$\overline{U}_{c(i)}$	Average capacitor voltages imbricated cells converter
$U_{cd_{max}}$	Maximal decoupling capacitor voltage
$U_{ce(i)}$	Multilevel converter group voltage (configurable converter)
$U_{ce(max)}$	Maximal allowed voltage across an IGBT power switch

$U_{ce(sat)}$	On-state saturation voltage of IGBT
U_{conv}	Multilevel converter output voltage
$U_{conv(i)}$	Output voltage of a 4Q-converter, usually AC
$\hat{U}_{conv}$	Fundamental voltage of the converter voltage U_{conv}
$U_{conv(max)}$	Maximal possible amplitude of the converter voltage U_{conv}
U_d	On-state voltage drop on a power diode
U_{dc1}	DC link voltage
$\overline{U}_{dc1}$	DC component of the voltage U_{dc1}
$U_{dc1(nom)}$	Nominal value for the voltage U_{dc1}
U_{dc2}, $U_{dc2(i)}$	Feeding voltage for the 4Q-converters
U'_{dc2}	Feeding voltage referred to the primary side over a transformer
$\overline{U}_{dc2(i)}$	DC component U_{dc2}
$U_{dc2(nom)}$	Nominal value for the voltages $U_{dc2(i)}$
$U_{dc2(set)}$	Set value for the voltages $U_{dc2(i)}$
$\overline{U}_{dc2(set)}$	Set value for the DC component of the voltage $U_{dc2(i)}$
U_{dc2av}	Average value of all DC voltages $U_{dc2(i)}$
$\overline{U}_{dc2av}$	DC component of the average value of all DC voltages $U_{dc2(i)}$
$\hat{U}_{harm(i)}$	The harmonic amplitudes of the converter voltage U_{conv}
U_{line}	Effective line voltage
$U_{line(DC)}$	DC line voltage (configurable converter)
$U_{R,S,T}$	Phase voltages of a motor converter from the multilevel converter
$U_{R(i),S(i),T(i)}$	Phase voltages of a motor converter from the 4Q-converter
$\hat{U}_{R,S,T}$	Amplitude of phase voltages of a motor converter
$U_{R_{s1},R_{s2},R_{s3}}$	Phase-shifted voltages on secondary side of polyphase transformer
$\underline{U}_{ref}$	Reference voltage vector rotating in the complex phasor plane
U_{s1}, U_{s2}	Fundamental sine wave of the medium frequency voltages
$\underline{U}_{s1}$, $\underline{U}_{s2}$	Monophasors of the medium frequency voltages
$\hat{U}_{s1}$, $\hat{U}_{s2}$	Fundamental sine wave of the medium frequency voltages
U^s_α	Voltage phasor point in the complex plane, x-component
U^s_β	Voltage phasor point in the complex plane, y-component
V_{ref}	Reference function for the modulator
$V_{ref(i)}$	Reference function for an independent 4Q-converter i
V'_{ref}	Reference function for the modulator, coming from the current controller
$\underline{V}'_{ref}$	Monophasor reference function from the controller
$V'_{ref(im)}$	Imaginary part of the reference function monophasor
$V'_{ref(re)}$	Real part of the reference function monophasor
w_r	Winding ratio of the medium-frequency transformer
W_a	Window surface of a magnetical core
Z	AC link equivalent impedance
Z_{load}	Load impedance of a converter

Curriculum vitae

Nikolaus P. Schibli	Born on November the 14th 1970 in New York, USA
1976	Moved to Chur, Switzerland
1977-1985	Obligatory elementary school in Chur, Switzerland
1985-1990	Cantonal grammar school of Grisons, in Chur, Switzerland Scientific A-levels (Maturity type C)
1991-1995	Electrical engineering studies at the Swiss Federal Institute of Technology ETHZ Zurich, Switzerland Specialisation in the fields of computer science and power electronics
1995-1996	Masters degree at the Swiss Federal Institute of Technology of Lausanne EPFL Lausanne, Switzerland in the Industrial Electronics Laboratory (LEI)
1996-2000	Assistant in the Industrial Electronics Laboratory Research activities on multilevel converters and smart digital cameras for industrial inspection