2024 International Symposium on Power Electronics, Electrical Drives, Automation and Motion - SPEEDAM

Analysis of a DC Data Center Power Supply with Series-Connected Active and Passive Rectifiers

A. Cervone, L. Arbogast, and D. Dujic

POWER ELECTRONICS LABORATORY
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

Analysis of a DC Data Center Power Supply with Series-Connected Active and Passive Rectifiers

Andrea Cervone, *Member, IEEE*, Louis Arbogast, and Drazen Dujic *Senior Member, IEEE*
Power Electronics Laboratory (PEL) - École Polytechnique Fédérale de Lausanne (EPFL) - Switzerland

***Abstract*—In future Data Centers with DC power distribution, unidirectional rectification is required to provide a constant DC voltage from the AC grid. Given the unidirectionality requirement, an inverter-based Active Front End (AFE) solution could be ideally replaced by a passive Diode Rectifier (DR) unit, leading to a simpler, more robust and cheaper solution. However, a purely passive solution would not be able to provide the DC-bus voltage stabilization in spite of the $\pm 10\%$ AC voltage fluctuations in the supplying grid, and would also lead to operation at non-unitary power factor and to harmonic current pollution. Therefore, this work analyzes a hybrid solution relying on the simultaneous utilization of an AFE and of a DR unit, whose DC outputs are connected in series with one another. By employing both a passive and an active rectifier, this solution could potentially reduce the sizing requirements for the AFE while achieving at the same time the desired target requirements in terms of DC-bus voltage stabilization and unitary power factor operation. The potential benefits and limitations of this approach are analyzed in this work. From an idealized design it is shown that, at the expense of a increased system complexity, the analyzed hybrid solution would theoretically achieve a 37.5% reduction in the sizing requirements of the AFE, but that in practical designs this ideal optimum might not be compatible with the voltage class of available semiconductor devices, in which case a sub-optimal solution could be instead designed, with a potential $25 \div 28\%$ reduction in the AFE sizing requirements, while achieving similar control and efficiency performances as in a full-AFE solution.**

***Index Terms*—Data Center DC power supply, Active-Front-End (AFE), Diode-Rectifier (DR), Partial Power Processing.**

I. Introduction

In the ever-evolving landscape of digital infrastructure, Data Centers stand as critical hubs for data processing and storage, necessitating a continuous and reliable power supply to ensure uninterrupted operations. Conventionally, the power distribution in a data center is realized in AC. In this case, a low frequency transformer (LFT) is typically used to step down the AC grid from medium voltage (MV) levels to low voltage (LV, typically at $400\,\mathrm{V}$ AC), and is then followed by an AC/AC Uninterruptible Power Supply (UPS) unit. The AC power is then distributed to the server racks, where the server Power Supply Units (PSUs), typically realized as a double stage with an input AC/DC Power Factor Corrector (PFC) and an output isolated DC/DC converter, are used to locally supply the IT equipment (typically at $12\,\mathrm{V}$-$48\,\mathrm{V}$) [1].

However, more recently, a new solution based on a DC distribution for future data centers has started attracting the interest of the technical community [1]–[4]. In this case, the main PFC conversion can be centralized in a single unit and the server racks, directly supplied in DC, would only need the isolated DC/DC converters to step down the DC voltage to the IT equipment levels, while a DC/DC UPS could be directly connected to the main DC-bus of the distribution system. This architecture could potentially decrease the number of required conversion steps and improve the overall system efficiency [2], [3], [5], [6]. Different voltage levels have been proposed for the DC energy distribution in future data centers. Nominal values have been proposed in the range from $240\,\mathrm{V}$ to $800\,\mathrm{V}$ ($\pm 400\,\mathrm{V}$), but recently a standard value that is being more widely recognized is of $760\,\mathrm{V}$ ($\pm 380\,\mathrm{V}$, with the value of $380\,\mathrm{V}$ being a standard voltage for IT equipment [6]–[8]).

In this case, the conversion from the AC supply to the DC distribution could be achieved by employing standard two-levels three-phase Active Front End (AFE) converters, that can be connected to the MVAC distribution grid through a step-down LFT, as shown in Fig. 1a. However, in data center applications, the power flow is unidirectional, and the majority of it is consumed by the servers, with limited options for energy recovery (mainly from the generated heat). In this framework, the AFE converter for the interface between the AC grid and the DC distribution system could be replaced by an uncontrolled Diode Rectifier (DR). Indeed, the intrinsic simplicity of a DR solution, which does not require any measurement or gate-driving circuitry, would theoretically allow to achieve a more robust and cost-effective solution [2].

Nevertheless, the use of a DR comes with some drawbacks, which are mainly represented by:

- the lack of regulation of the output DC-bus voltage (which reflects any variation in the AC grid voltages);
- the absorption of a reactive power from the AC grid (typically in the range of $15 \div 20\%$ of the active power);
- the introduction of low-order harmonic components in the AC currents (caused by the non-linear rectifier operation).

While the harmonic content introduced by the diode rectifier can be mitigated by using multiple phase-shifted units (e.g., twelve-pulse rectifiers, eighteen-pulse rectifier, etc...), the reactive power absorption and the lack of regulation of the DC-bus voltage require additional counteracting measures.

Different options can be conceived to counteract these drawbacks. A possible solution, that is examined in this work, is represented in Fig. 1b, and is based on a hybrid circuit architecture relying on both a passive and an active rectifier unit at the same time. These two units are supplied by the same AC grid by means of a multi-winding transformer, and are connected in series with one another at their DC terminals. This hybrid solution would potentially allow the use of a reduced-sized AFE unit to compensate the drawbacks of the DR, and can be considered as a Partial-Power-Processing

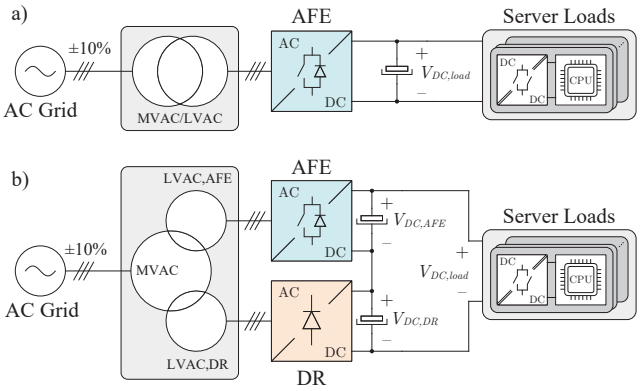

Fig. 1. Simplified scheme of a Data Center power supply based on a MVAC/LVDC conversion system realized with: a) a LFT and a full-scale AFE; b) a multi-winding LFT and a series connection of a DR and an AFE. This hybrid solution could potentially allow a reduction in the AFE ratings.

conversion approach. In this case, the main tasks of the AFE are to compensate for the DC-bus voltage fluctuation due to the $\pm 10\%$ allowed variation in the AC grid voltage [9] (*DC Voltage Compensation* requirement) and to compensate the reactive power absorption of the DR (*Active Power Filtering* requirement). As an additional feature, the same AFE unit can also be used as an active filter to compensate the low-order harmonics introduced by the DR unit in the AC currents (*Harmonic Filtering* requirement), in a way to improve the overall power quality of the structure towards the AC grid.

To assess the feasibility and convenience of this hybrid structure, a relevant research question is to evaluate the achievable design savings that could be obtained compared to a standard circuit as in Fig. 1a. These aspects are analyzed in this work, that is organized as follows. First, some preliminary considerations are given in Section II to review some basic knowledge about steady-state operation of AFEs and define a key performance indicator for the analysis and comparisons. Secondly, in Section III, a theoretical analysis is provided to identify, in ideal conditions, what would be the design power of the hybrid series-connected DR+AFE solution, compared to a full-scaled AFE unit. A design example, aided with simulation results, is then provided in Section IV-V considering a specific application example. Finally, Section VI summarizes the main conclusions of this work.

The analysis will explicitly take as example the design of a $250\,\mathrm{kW}$-$6.6\,\mathrm{kV_{AC}}$-$760\,\mathrm{V_{DC}}$ data center supply, of special interest for the research project supporting this work. Higher power ratings, of deeper interest for hyperscale data centers, will share similar conclusions if implemented with multiple parallel-connected devices or conversion units. Similarly, other application areas, like electric vehicle charging stations or electrolyzers, also share similar requirements and can therefore employ similar circuit architectures.

II. Preliminary Considerations

This section reviews some basic knowledge on the AFE operation and defines the main Key Performance Indicator (KPI) used in the following analysis.

In what follows, unless otherwise specified, all the AC fundamental variables will implicitly refer to their Root Mean Square (RMS) value, and the AC voltages will refer to the phase-to-phase quantities. The subscripts "min" and "max" will refer to the minimum and maximum values that can be assumed by the specified variables in the assigned operating conditions. The subscript "nom" will instead refer to the nominal operating conditions.

A. Power requirements of an Active Front End

As known, the Active and Reactive Power that an AFE unit transfers during operation are respectively defined as

$$P = \sqrt{3}\, V_{AC}\, I_{AC} \cos\phi \tag{1}$$

$$Q = \sqrt{3}\, V_{AC}\, I_{AC} \sin\phi \tag{2}$$

and, considering only the operation at the fundamental frequency, the Apparent Power of the structure is defined as:

$$S = \sqrt{P^2 + Q^2} = \sqrt{3}\, V_{AC}\, I_{AC} \tag{3}$$

By neglecting the power losses on the conversion devices, the Active power P in (1) corresponds to the power delivered to the DC-side of the structure, defined as:

$$P = V_{DC}\, I_{DC} \tag{4}$$

B. Modulation Index

As known, a grid-connected voltage source inverter behaves as a boost, and the ratio between the AC and the DC voltage defines the *Modulation Index* of the structure:

$$M_{ind} = \frac{V_{AC,peak,ph-n}}{V_{DC}/2} = \frac{2\sqrt{2}}{\sqrt{3}}\frac{V_{AC}}{V_{DC}} \tag{5}$$

The modulation index is limited to a maximum value of $2/\sqrt{3} \approx 1.15$ in presence of a zero-sequence injection on the pulse width modulated voltages (e.g., using a third-harmonic injection, a min-max injection or a space-vector modulation algorithm). Therefore, the maximum AC voltage that can be generated is

$$V_{AC,max} = V_{DC}/\sqrt{2} \tag{6}$$

C. Sizing Power of an Active Front End

Consider a standard three-phase voltage source inverter used as an AFE. The converter is realized based on six controllable semiconductor devices (e.g., MOSFETs or IGBTs), selected to withstand a certain drain-source voltage (namely V_{switch}) and to conduct a certain maximum current (namely I_{switch}). The voltage V_{switch} is typically chosen considering a specific safety margin with respect to the drain-source breakdown voltage of the device (e.g., considering the maximum V_{switch} being $65\% \div 75\%$ of the blocking voltage), while the current I_{switch} is chosen depending on the switching frequency, on the thermal characteristics of the device, and on the adopted cooling system, in a way to limit the maximum junction temperature within a desired safety limit.

The required values V_{switch} and I_{switch} depend on the maximum voltage and current stresses that each device needs

to withstand during the worst-case operating conditions of the converter. In this case, the maximum voltage stress V_{switch} that a device needs to sustain is the maximum DC bus voltage of the AFE, meaning that $V_{switch} = V_{DC,max}$. Similarly, the maximum current stress I_{switch} can be considered as the maximum peak current that could flow in the device during its conduction state, which is equal to the maximum peak AC phase current, meaning that $I_{switch} = \sqrt{2}\, I_{AC,max}$.

Based on V_{switch} and I_{switch}, one could compute the theoretical power that an ideal converter, designed to work at both maximum voltage and current at the same time, would be able to deliver. From (3)-(6), this power would be:

$$\begin{aligned} S_{AFE,SP} &= \sqrt{3}\ V_{AC,max}\ I_{AC,max} = \\ &= (\sqrt{3/2})\ V_{DC,max}\, I_{AC,max} = \\ &= (\sqrt{3}/2)\ V_{switch}\, I_{switch} \end{aligned} \tag{7}$$

This value, further on named as "*Sizing Power*" of the AFE, is an indicator of the installed capacity of the semiconductor devices in the overall converter, and it will be used as the main KPI for the following analysis and comparisons. Indeed, a design with a lower $S_{AFE,SP}$ is associated to lower voltage and/or current stresses for the switching devices, which is typically associated to a more cost-effective solution.

As it will be exemplified and clarified in the following, the sizing power $S_{AFE,SP}$ defined by (7) is generally higher than the maximum required apparent power $S_{AFE,max}$ of the AFE, found as per (3). This is because $S_{AFE,SP}$ is defined by taking into account the extreme voltage/current operating conditions, which in the real structure may not coexist at the same time. In other words, since the AFE needs to guarantee the required power flow not only in nominal operation, but in a defined range of operating conditions (including, e.g., different grid voltages), its design will necessarily be oversized compared to the nominal point. Furthermore, another reason for oversizing is the availability of commercial devices in the market, whose voltage and/or current ratings may not match the required ones, leading to a sub-optimal design.

III. Theoretical Design

This section presents a theoretical comparison between the design of a full AFE solution and of the considered hybrid series-connected AFE/DR circuit, as represented in Fig. 1. The aim is to determine the maximum theoretical reduction of the sizing requirements for the AFE unit, allowed by the simultaneous use of the uncontrolled diode rectifier, generally cheaper and more efficient.

In all the subsequent analysis, the complexity and design requirements of the DR and of the transformer unit for the interconnection to the MVAC grid will not be taken into account, considering their technology to be mature and sufficiently well-established compared to the AFE. Additionally, for the sake of simplicity, in this section, no restrictions will be posed on which voltage/current ratings are commercially available. Finally, to facilitate the analysis, the idealized investigation developed in this section relies on some simplifying assumptions, that will be introduced along the text.

A. Design of the Full-AFE Solution

Considering a full-AFE solution as in Fig. 1a, the aim of the conversion circuit is to provide a constant DC-bus voltage $V_{DC,load}$ to the load, in the whole range of the input power (i.e., from no-load to $P_{load,max}$) and considering a $\pm 10\%$ possible variation on the MVAC voltage V_{MVAC}.

Since the DC-bus voltage is fixed, the required voltage withstand capabilities V_{switch} is automatically defined, and it results that $V_{DC,AFE,max} = V_{switch} = V_{DC,load}$.

The (fixed) DC-bus voltage imposes a constraint on the maximum LVAC voltage of the system, which is obtained when the MVAC voltage is subject to a $+10\%$ increase from its rated value. Assuming, for the considered structure, a maximum modulation index $M_{ind,max}$, from (5) it is possible to compute the nominal LVAC voltage of the AFE as

$$V_{LVAC,AFE,nom} = \frac{\sqrt{3}}{2\sqrt{2}} \frac{M_{ind,max} \cdot V_{DC,load}}{1.1} \tag{8}$$

The maximum modulation index $M_{ind,max}$ can be chosen to consider some margin to compensate the voltage drops on the transformer and grid impedances. In the considered $250\,\mathrm{kW}$-$760\,\mathrm{V}$ example, assuming $M_{ind,max} \approx 1.00$ (to allow a 15% margin), the required LVAC voltage is approximately equal to $V_{LVAC,AFE,nom} \approx 425\,\mathrm{V}$.

The maximum current of the AFE is instead obtained when the full power $P_{load,max}$ needs to be transferred in case of the minimum LVAC voltage of the structure, which is obtained when the MVAC voltage is subject to a -10% drift from the rated value. Assuming operation at unitary power factor, the maximum AC current can be found from (1):

$$I_{LVAC,AFE,max} = \frac{P_{load,max}}{\sqrt{3} \cdot 0.9 \cdot V_{LVAC,AFE,nom}} \tag{9}$$

In the considered example, the required AC current in each AFE phase is approximately $I_{LVAC,AFE,max} \approx 380\,\mathrm{A}$.

Finally, the maximum AC current $I_{LVAC,AFE,max}$ and DC voltage $V_{DC,AFE,max}$ define the maximum stresses on the semiconductor devices, from which it is possible to compute the sizing power of the AFE. In this case, by replacing (8) and (9) in (7), and by simplifying homologous terms, it results that:

$$S_{AFE,SP} = \frac{1.1 \cdot 2}{0.9 \cdot \sqrt{3}}\ \frac{P_{load,max}}{M_{ind,max}} \tag{10}$$

From (10) it can be concluded that, in order for the AFE unit to guarantee proper DC-bus voltage stabilization in the whole range of output load power and considering a possible AC grid variation of $\pm 10\%$, the sizing power of the converter must be oversized compared to the sole full-load power $P_{load,max}$. In the considered $250\,\mathrm{kW}$-$760\,\mathrm{V}$ example, the required sizing power of the AFE is around $S_{AFE,SP} \approx 350\,\mathrm{kVA}$ (i.e., with a 40% oversizing compared to the $250\,\mathrm{kW}$ rated load).

B. Design of the Hybrid AFE+DR solution

The design of the hybrid AFE+DR circuit of Fig. 1b depends on multiple factors and parameters. In what follows, for simplicity reasons, the design of the DR unit is not

explicitly evaluated, and it is instead assumed that the DR unit has the same equivalent terminal behavior regardless of the adopted rectifier circuit (e.g., six-pulse, twelve-pulse, etc..). Moreover, it is assumed that the output DC voltage of the DR has negligible variation with the absorbed power (i.e., negligible effect of the AC line impedances), and that is instead solely dependent on the magnitude of input AC voltage, thus reflecting any variation of the grid voltage in the $\pm 10\%$ range allowed by the grid codes. Furthermore, it is assumed that the reactive power consumption of the DR unit is proportional to its active power consumption and defined by a constant factor $q_{DR} = Q_{DR}/P_{DR}$ (which can be considered to be around $0.20 \div 0.25$ [2], [10]). Finally, it is assumed that in all operating conditions the power needed from the AFE for harmonic filtering purposes is negligible compared to the fundamental active and reactive power[1]. Some of these assumptions will be relaxed in a subsequent analysis stage.

To start this analysis, it is possible to assume that the system is designed in a way that, in nominal operating conditions (i.e., with rated AC voltage and full load), the power is shared between the AFE and the DR units as the percentages $X_{AFE,nom}$ and $X_{DR,nom}$ (with $X_{AFE,nom} + X_{DR,nom} = 100\%$ and, ideally, a low percentage value for $X_{AFE,nom}$). Since the DR and the AFE are connected in series on the DC side, they share the same DC output current and, consequently, $X_{DR,nom}$ and $X_{AFE,nom}$ also represent the fraction of the rated DC voltages of the two structures. For example, considering the 250 kW-760 V ratings introduced earlier, if the AFE and the DR are designed to respectively provide the 25% and the 75% of the rated output power (i.e., $X_{AFE,nom} = 0.25$ and $X_{DR,nom} = 0.75$), then the rated DC-bus voltages of the AFE and of the DR units would be 190 V and 570 V, respectively.

Since the DC voltage of the DR unit directly reflects any change in the grid, a $\pm 10\%$ variation in the grid voltage corresponds to a $\pm 10\%$ change in the DC voltage $V_{DC,DR}$. In order for the system to keep providing a stable output voltage $V_{DC,load}$, the AFE needs to compensate the variation on the DR unit, as graphically exemplified in Fig. 2. Therefore, the maximum and minimum DC voltages of the AFE units are:

$$V_{DC,AFE,max} = (1 - 0.9 \cdot X_{DR,nom})\, V_{DC,load} \tag{11}$$

$$V_{DC,AFE,min} = (1 - 1.1 \cdot X_{DR,nom})\, V_{DC,load} \tag{12}$$

In the considered example, $V_{DC,AFE,max} = 247\,\text{V}$ (obtained for the minimum AC grid voltage) and $V_{DC,AFE,min} = 133\,\text{V}$ (obtained for the maximum AC grid voltage). Naturally, since $V_{DC,AFE}$ is intrinsically a positive quantity, the expression (12) also defines the maximum theoretical value of $X_{DR,nom}$, which cannot exceed $1/1.1 \approx 0.91$.

On one hand, the maximum DC voltage $V_{DC,AFE,max}$ is automatically establishing the required voltage withstand value V_{switch} for the devices employed in the AFE unit.

[1]In this case, either the harmonic filtering requirement is not required (e.g., in case the AC side power quality is not relevant, or in case there is another dedicated equipment for filtering), or its presence will bring an additional oversizing of the AFE unit for the required harmonics to inject.

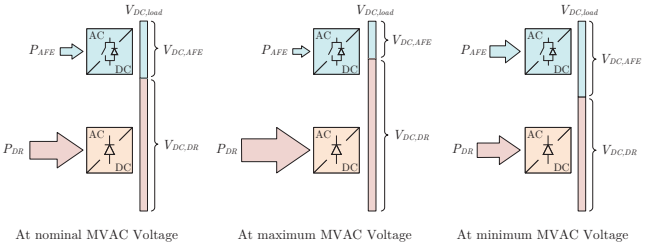

Fig. 2. Qualitative representation of the different DC-bus voltage and power sharing between the AFE and the DR unit for different MVAC voltage magnitudes. The required power and voltage are proportional to one another, and in case of variation in the MVAC grid, the AFE needs to compensate for the corresponding change on the DR unit.

On the other hand, similarly to how it has been done in the previous subsection, the minimum DC voltage $V_{DC,AFE,min}$ can be used to compute the required LVAC voltage of the AFE. However, in this case, it is worth stressing out that the minimum DC voltage of the AFE unit is obtained for the maximum AC grid input voltage, since this condition corresponds to the maximum DC voltage of the DR unit (as shown in Fig. 2). Therefore, from (5), the required LVAC voltage of the AFE unit can be found as

$$V_{LVAC,AFE,nom} = \frac{\sqrt{3}}{2\sqrt{2}} \frac{M_{ind,max} \cdot V_{DC,AFE,min}}{1.1} \tag{13}$$

In the analyzed example parameters, considering once again $M_{ind,max} = 1.00$, the required LVAC voltage of the AFE unit would be $V_{LVAC,AFE,nom} \approx 74\,\text{V}$.

Regarding the required power, the worst-case operating condition for the AFE is obtained when the AC grid voltage is at its minimum value. Indeed, in this case, the AFE needs to compensate not only for the voltage loss, but also for the power decrease of the DR unit, which is proportional to it.

In this case, the maximum active power that the AFE is required to transfer is:

$$P_{AFE,max} = (1 - 0.9 \cdot X_{DR,nom})\, P_{load,max} \tag{14}$$

and, in the considered example, $P_{AFE,max} \approx 81.25\,\text{kW}$.

On top of the active power, the AFE is also asked to compensate the reactive power consumption of the DR, which can be assumed to be around 20% of the active power transferred by the DR unit itself (i.e., considering $q_{DR} \approx 0.2$). Therefore, the reactive power requirement would be[2]:

$$Q_{AFE,V_{min}} = q_{DR} \cdot 0.9 \cdot X_{DR,nom} \cdot P_{load,max} \tag{15}$$

and, in the considered example, $Q_{AFE,V_{min}} \approx 34\,\text{kVAr}$.

Then, the worst-case apparent power of the AFE is:

$$S_{AFE,max} = \sqrt{P_{AFE,max}^2 + Q_{AFE,V_{min}}^2} \tag{16}$$

and, in the considered case study, $S_{AFE,max} \approx 88\,\text{kVA}$.

[2]More rigorously, when the input grid voltage is at its minimum value, also the reactive power consumption of the DR would be at its minimum value. However, it can be easily shown that this would still be the worst case scenario for the overall apparent power of the structure, as long as $X_{DR} < 87\%$ (which, as shown in the following, is the range of interest for the design). The proof is based on a simple function minimization and it is omitted from this discussion for conciseness of the analysis.

Finally, from the maximum apparent power $S_{AFE,max}$, which is obtained at the minimum input AC voltage, the maximum AC current can be found from (3) to be:

$$I_{LVAC,AFE,max} = \frac{S_{AFE,max}}{\sqrt{3} \cdot 0.9 \cdot V_{LVAC,AFE,nom}} \quad (17)$$

which, in the considered example, results in a current of around $I_{LVAC,AFE,max} \approx 763\,\text{A}$.

As also done for the full-AFE solution of Section III-A, also in this case the knowledge of the maximum DC voltage and of the maximum AC current can be used to compute the sizing power of the AFE unit using (7). Considering the analyzed example, it can be verified that $S_{AFE,SP} \approx 230\,\text{kVA}$. This value could seem an oversizing compared to the $S_{AFE,max} \approx 88\,\text{kVA}$ value computed earlier, and it means that the sizing power (computed from the extreme voltage and current stresses of the devices) is sensibly higher than the maximum apparent power of the AFE during functioning (which, instead, depends on the operating condition). However, if compared to the full-sized solution examined in Section III-A (with a sizing power of around 350 kVA), the hybrid design only requires around 65% of the sizing power (i.e., it allows for a 35% reduction in the combined voltage/current stress of the active semiconductor devices), thanks to the use of the DR unit that can manage part of the actual required power.

IV. Design Example and Discussion

A. Theoretical Optimal Design for the Hybrid Architecture

The design of the AFE+DR solution described in the previous section is based on the choice of the parameter $X_{DR,nom}$, which defines the fraction of the overall load power that is provided by the DR in rated operating conditions. The same procedure can be, therefore, repeated for different values of $X_{DR,nom} \in [0;1]$, in a way to determine the optimal value that can minimize the sizing power $S_{AFE,SP}$ of the AFE.

The results of this procedure are graphically depicted in Fig. 3, that show the Sizing Power $S_{AFE,SP}$, the maximum DC-bus voltage $V_{DC,AFE,max}$ and the maximum LVAC current $I_{LVAC,AFE,max}$ of the AFE unit for varying $X_{DR,nom}$ ratio in the range $[0\%;90\%]$. All the variables are normalized with respect to the same design requirements in absence of any DR unit, previously computed in Section III-A.

As can be noted, the progressive increase of the ratio $X_{DR,nom}$ allows a reduction of the maximum DC voltage requirements of the AFE unit, that progressively allows a reduction of the overall sizing power $S_{AFE,SP}$. However, since the AFE unit must compensate for both the voltage and power fluctuations of the DR (caused by the $\pm 10\%$ allowed variation in the grid voltage), the LVAC current requirements are progressively increasing. As a result, for high values of $X_{DR,nom}$, the reduction in the voltage requirements for the semiconductor devices in the AFE unit is not anymore sufficient to help reducing the overall sizing power, since the current requirements are progressively increasing.

Considering the adopted simplifying assumptions, the theoretical optimal design that minimize $S_{AFE,SP}$ is obtained for

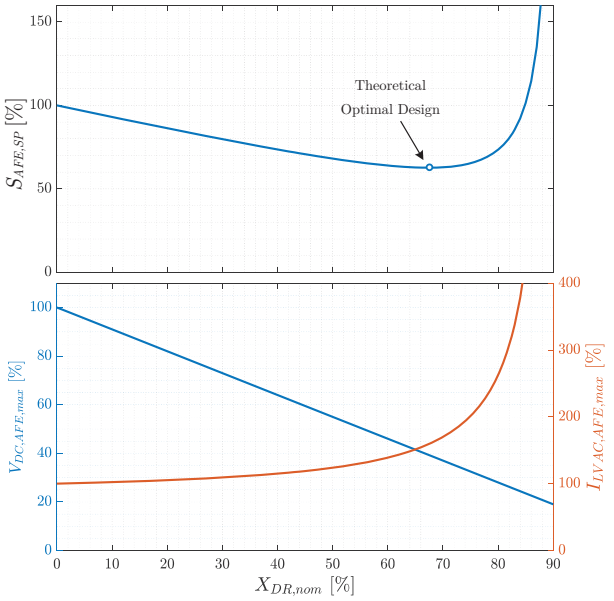

Fig. 3. Sizing Power, Maximum DC-Bus Voltage, and Maximum AC Current of the AFE unit for varying nominal DR ratio $X_{DR,nom}$, normalized by the corresponding values in absence of DR.

$X_{DR,nom} \approx 67\%$, and in this case the sizing power of the AFE is around 62.5% of the power required in absence of the DR unit (i.e., it allows a 37.5% reduction). In this case, the DC-bus voltage withstanding requirements of the AFE unit are around 40% of the voltage required in absence of the DR, while the maximum current of the AFE unit is increased of around 60% compared to the full-AFE solution.

B. Effect of limited voltage class availability

The results of the previous analysis show potential benefits of the hybrid design. However, they have been obtained without considering the actual availability of voltage and current ratings of the commercial devices, which would bring additional constraints in the real design stage.

For example, considering the 250 kW-760 V design that has been examined in the previous examples, in the theoretical optimal design (i.e., with $X_{DR} \approx 67\%$), the maximum DC-bus voltage of the AFE unit would be around 300 V, while the maximum AC current would be around 600 A, resulting in a sizing power of around 220 kVA. However, considering a voltage utilization of around 70%, the required devices would need to have a voltage withstanding of around 430 V, and the closest voltage class of commercially available devices is 600 V. Using this voltage class with the same current specifications would unfortunately result in an unnecessarily increased sizing power of the AFE unit (of around $600\,\text{V}/430\,\text{V} \approx 40\%$), thus nullifying the potential savings of the hybrid architecture compared to the full-AFE solution.

This means, that, considering realistic values for commercial devices, a more convenient solution would be obtained considering a different value of $X_{DR,nom}$, in a way that $V_{DC,AFE,max}$ expressed as per (11) would be close enough to the voltage withstanding of commercial devices (while still

considering a $65 \div 75\%$ utilization to provide sufficient safety margin). With respect to the theoretical optimal design (with $X_{DR,nom} \approx 67\%$), and considering the analyzed test scenario, it is either possible to choose a higher $X_{DR,nom}$ value and get closer to voltage class of $400\,\mathrm{V}$, or to choose a lower $X_{DR,nom}$ value and get closer to the voltage class of $600\,\mathrm{V}$. Among these two options, the latter is considered by the authors to generally be more convenient. The reason for that is due to the lower AFE current requirements guaranteed by a lower $X_{DR,nom}$ and by the flatness of the $S_{AFE,SP}$ characteristics on the left of the minimal point, as previously depicted in Fig. 3.

Therefore, for the specific application example considered in this work, a good design can be obtained by choosing $X_{DR,nom} \approx 50\%$ (i.e., with AFE and DR providing equal power in nominal operating conditions). This would lead to a maximum DC-bus voltage of $418\,\mathrm{V}$, which is very close to the $420\,\mathrm{V}$ voltage withstanding obtained with $600\,\mathrm{V}$ class devices at a 70% utilization. Following the design procedure described in Section III-B it can be computed that the current requirement in this case would be $I_{LVAC,AFE,max} \approx 470\,\mathrm{A}$, and the resulting sizing power would amount to $240\,\mathrm{kVA}$ (around 8% higher than the theoretical optimal solution).

Finally, a further increase in the sizing requirements may be needed to compensate the load-dependent voltage drop of the DR unit and to provide harmonic compensation features, whose effects have been previously neglected. The specific required oversizing depends on many factors, including the adopted DR unit (e.g., six-pulse, twelve-pulse, etc...), its AC grid inductances (strongly depending on the short-circuit impedance of the transformer unit), and its operating point. For a simple analysis, an empirical 15% increase in the apparent power requirement can be considered for both effects, leading to a resulting sizing power of around $280\,\mathrm{kVA}$.

In this framework, to provide a fair comparison, it is also worth recalling that also the full-AFE solution is normally affected by the limited voltage class availability in the market. In the considered example, as discussed in Section III-A, the DC-bus voltage would be fixed at the value of $760\,\mathrm{V}$. Considering again an utilization of around 70% of the voltage withstanding capabilities of the devices, the semiconductors to be chosen for the full-AFE solution need to have breakdown voltage higher than $1.08\,\mathrm{kV}$. The closest voltage class available on the market is of $1.2\,\mathrm{kV}$, meaning that an additional oversizing of around $1.2\,\mathrm{kV}/1.08\,\mathrm{kV} \approx 11\%$ is required for the full-AFE solution. In the considered example, by choosing $1.2\,\mathrm{kV}$ class IGBTs, and by still considering the required AC current of around $380\,\mathrm{A}$, the sizing power of a more realistic full-AFE solution would be of around $391\,\mathrm{kVA}$ instead of the $350\,\mathrm{kVA}$ computed with the theoretical design discussed in Section III-A.

In view of these consideration, by considering the voltage class availability of semiconductor devices, the design of the hybrid solution in the example under analysis can be around 61% of the full-AFE solution in case of no harmonic filtering requirement (i.e., around 39% overall saving), and around 72% in case of harmonic filtering requirement (i.e., around 28% overall saving). These results are summarized in Table I.

TABLE I
SUMMARY OF THE SIZING RESULTS

Parameter	Full AFE (Ideal)	Full AFE (Example)	AFE+DR (Ideal)	AFE+DR (Example)
$P_{AFE,nom}$	250 kW	250 kW	83 kW	125 kW
$V_{LVAC,AFE,nom}$	425 V	425 V	111 V	190 V
$V_{DC,AFE,max}$	760 V	760 V	301 V	418 V
$I_{LVAC,AFE,max}$	380 A	380 A	600 A	540 A
V_{switch} (*)	760 V	840 V	301 V	420 V
I_{switch}	537 A	537 A	850 A	760 A
$S_{AFE,max}$	250 kVA	250 kVA	104 kVA	160 kVA
$S_{AFE,SP}$	350 kVA	391 kVA	220 kVA	240 kVA

(*) Considering a 70% utilization of the devices' blocking voltage.

V. SIMULATION RESULTS

To show the operating behavior of the analyzed hybrid circuit architecture, and to also have an estimation of the overall efficiency that could be achieved, some simulation results are reported in this section.

A. System Parameters and Control Algorithm

The analyzed hybrid circuit has been realized as the series connection of a twelve-pulse DR (with parallel-connected DC-buses) and of a standard two-level three-phase AFE, with the parameters reported in Table II.

The adopted control diagram for the AFE unit in the examined hybrid AFE+DR circuit architecture is schematically shown in Fig. 4. In this control diagram, the DC-bus voltage reference for the AFE unit is first computed by comparing the overall reference DC voltage of the load (i.e., $760\,\mathrm{V}$ in the considered example) with the measured DC-bus voltage at the output of the DR unit (which depends on the MVAC voltages magnitude). Based on the error between this voltage reference and the measured DC-bus voltage of the AFE unit, a standard Proportional-Integral (PI) controller is used to compute the reference direct axis current for the AFE unit. The quadrature axis current reference for the AFE unit is instead aimed at neutralizing the reactive power consumption of the DR, and is therefore computed to cancel the quadrature current absorbed by the DR (considering proper factors for scaling and/or shifting due to the transformer).

Then, a standard PI controller with cross-decoupling is used in the dq reference frame to control the fundamental d and q axes components of the AFE currents. In parallel, harmonic controllers are executed to compensate the low-order harmonics introduced in the AC grid by the DR unit. In the considered example, four Proportional-Resonant (PR) controllers have been implemented to compensate for the 11-th, 13-th, 23-rd and 25-th harmonics introduced by the twelve-pulse rectifier unit, and these harmonics have been extracted using selective Band-Pass Filters (BPFs).

Finally, the outputs of the fundamental and of the harmonic controllers are summed together and with the scaled AC grid voltages, to compute the reference voltages for the AFE unit, applied through a standard space-vector Pulse-Width-Modulation (PWM) algorithm. A Phase-Locked-Loop (PLL) algorithm has been used to extract the angular frequency and the instantaneous angle of the MVAC grid voltages.

TABLE II
SYSTEM PARAMETERS FOR THE SIMULATION RESULTS

Parameter		Value
MVAC Rated Voltage	$V_{MVAC,nom}$	6.6 kV
Load DC Rated Voltage	$V_{DC,load,nom}$	760 V
Rated Power	$P_{load,nom}$	250 kW
AC Grid Frequency	f_{AC}	50 Hz
LVAC Rated Voltage (AFE)	$V_{LVAC,AFE,nom}$	190 V
LVAC Rated Voltage (DR)	$V_{LVAC,DR,nom}$	270 V
Transf. Short-circuit Impedance (AFE)	$Z_{sc,AFE}$	3%
Transf. Short-Circuit Impedance (DR)	$Z_{sc,DR}$	3%
DC-Bus Capacitance (AFE)	$C_{DC,AFE}$	25 mF
DC-Bus Capacitance (DR)	$C_{DC,DR}$	25 mF
AFE Switching Frequency	$f_{sw,AFE}$	10 kHz

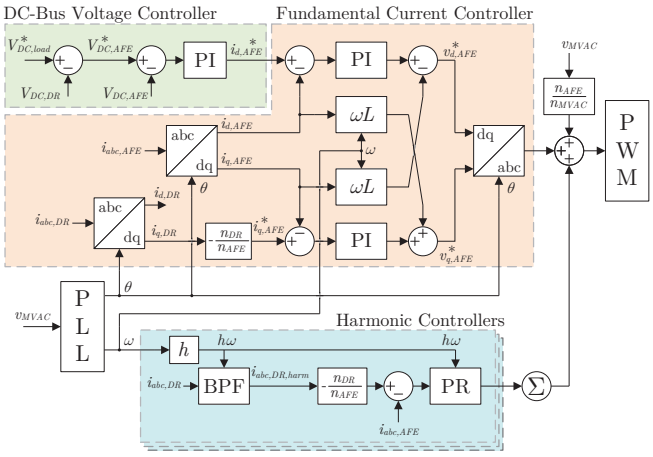

Fig. 4. Control diagram for the AFE in the hybrid circuit architecture.

B. Dynamic Test of the Structure

To illustrate an example of the ordinary operation of the analyzed hybrid circuit, some simulation results are reported in Fig. 5, showing the MVAC voltages and currents, the LVAC currents of the AFE and of the DR[3], the DC-bus voltages of the AFE and of the DR units, and the overall DC-bus voltage of the DC load. The test scenario is described as follows.

The whole test has been conducted at rated MVAC voltage. Initially, the system is working at no load, and no current is absorbed from the MVAC grid. The DR and the AFE have the same DC-bus voltage of 380 V, and the overall load is correctly stabilized at the rated 760 V voltage.

After 20 ms, the load is instantaneously changed to the full 250 kW rated power of the structure. As can be noted, as a non-ideal effect of the DR, the DC-bus voltage $V_{DC,DR}$ is subject to a small drop of around 15 V. This load-dependent drop, which was not modeled in the theoretical analysis of the previous sections, is however quickly compensated by the AFE control and the overall DC-bus voltage, after a small transient, is correctly stabilized to the desired 760 V.

[3]For better clarity, the results show the equivalent LVAC current absorbed from the twelve-pulse rectifier, instead of the two sets of LVAC currents absorbed by the two separate six-pulse diode bridge rectifier units.

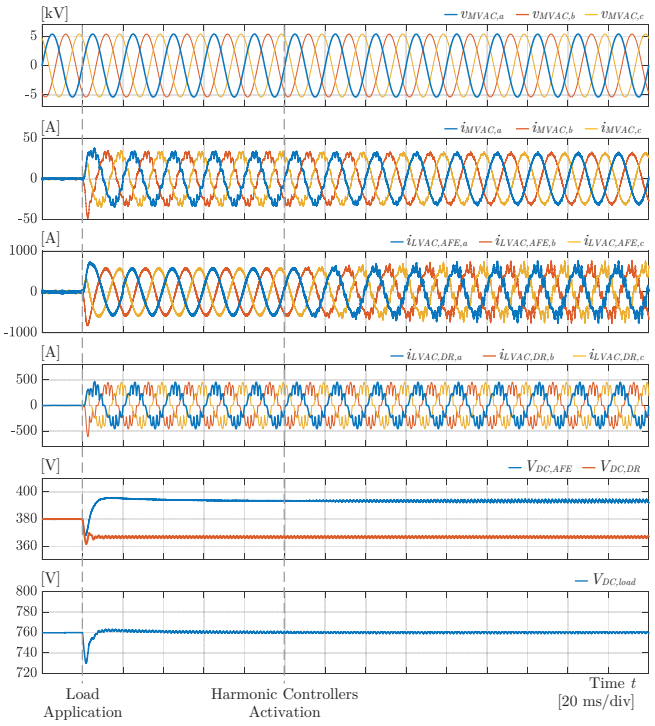

Fig. 5. Simulation results using the analyzed hybrid AFE+DR circuit in the analyzed dynamic test scenario.

In this stage, the AFE is only controlled for voltage stabilization and reactive power compensation. As a result, and as can be seen from Fig. 5, the AC currents of the AFE are sinusoidal, while the overall currents absorbed from the MVAC grid contain low-order harmonics with high magnitude, caused by the uncontrolled rectification of the DR unit.

After other 100 ms, the harmonic controllers in the AFE are activated. As can be noted, minimal differences can be noticed on the DC-bus voltages, while the AC currents are visibly modified. In this case, the AFE unit actively starts to absorb non-sinusoidal currents in a way to compensate the low-order harmonics of the DR unit. As can be seen in the last interval of Fig. 5, after a small transient, the harmonic pollution on the overall AC currents absorbed from the MVAC grid is greatly mitigated, at the expense of higher AC currents on the AFE (with a Root Mean Square (RMS) increase of around 3%).

C. Steady-State Operation at different MVAC Voltages

To provide a more complete picture of the system operation in different operating scenarios, Fig. 6 shows the steady-state simulation results considering the case when the full rated power of 250 kW is absorbed by the load in case the MVAC grid voltages are at their minimum and maximum value (respectively −10% and +10% of the rated 6.6 kV). The results are shown both when the harmonic compensation is disabled and when it is enabled.

As can be noted, when the MVAC voltage is at its minimum magnitude, the DC-bus voltage $V_{DC,DR}$ of the DR unit is sensibly lower than 380 V (in the simulation results it drops

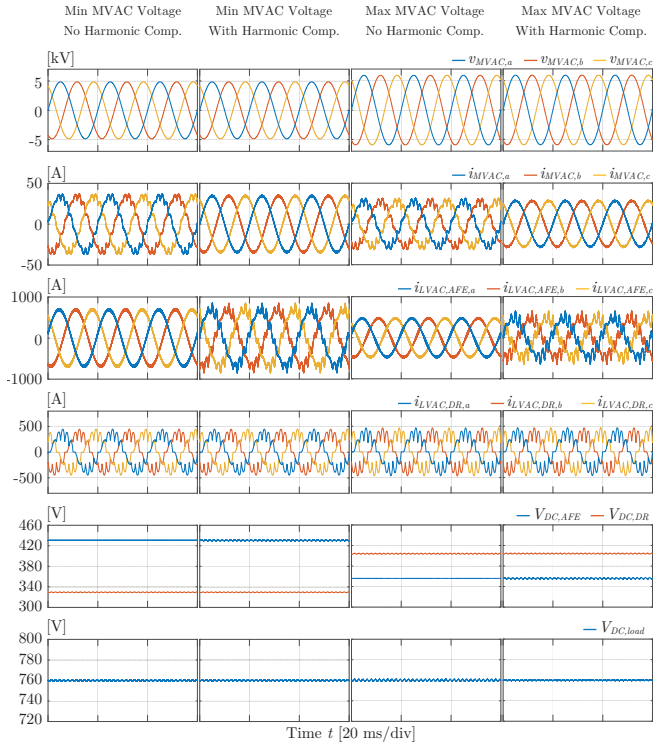

Fig. 6. Simulation results using the analyzed hybrid AFE+DR circuit at the minimum and maximum MVAC voltage and rated power.

to around 329 V), and the DC-bus voltage $V_{DC,AFE}$ of the AFE is increased to compensate for it. In this way, the overall DC-bus voltage of the load is correctly stabilized at the rated 760 V value. The opposite behavior instead happens when the MVAC voltage is at its maximum magnitude. In this case the DC-bus voltage of the DR unit is increased (to around 403 V), and the DC-bus voltage of the AFE is instead decreased.

As can be seen, in both cases, the activation of the harmonic controllers helps in achieving less polluted AC currents absorbed from the MVAC grid, at the expense of a higher current absorption from the AFE. Considering different operating conditions, the overall RMS of the currents is increased by around $2 \div 5\%$ by the harmonic filtering requirement.

The harmonic spectra of the MVAC currents and of the AFE currents in the analyzed operating conditions are reported in Fig. 7. As can be noted, due to the effect of the adopted twelve-pulse rectifier circuit, the first sensible higher order harmonics of the system are the 11-th and 13-th, followed by the 23-rd and 25-th. The activation of the harmonic controllers in the AFE control algorithm does not influence the magnitude of the fundamental components at 50 Hz, while it has a sensible impact on the higher order harmonics, that are shifted from the MVAC to the LVAC AFE currents.

D. Efficiency Estimation

To have an estimation of the possible efficiency values that the hybrid AFE+DR circuit could achieve, a set of numerical tests has been executed for different values of loading power (computed from 10% to 100% of the rated 250 kW load)

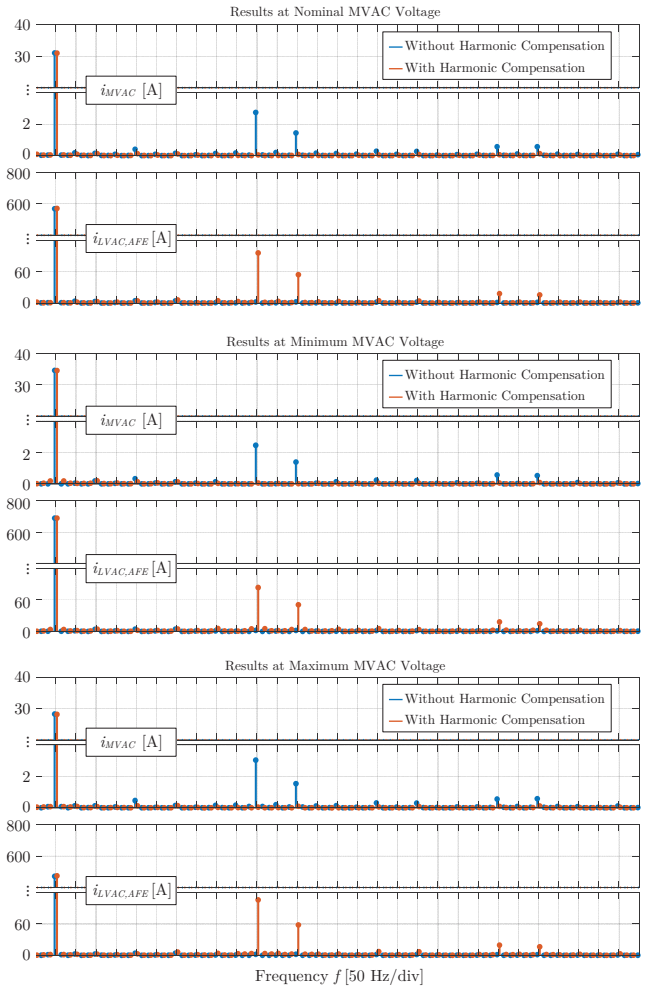

Fig. 7. Harmonic content of the MVAC currents and of the AFE currents without and with the harmonic compensation control, obtained at full load for different MVAC voltage values.

and of MVAC voltages (considering the $\pm 10\%$ tolerance band compared to the rated 6.6 kV voltage).

The losses have been evaluated in the PLECS environment considering parallel-connected Infineon FF400R06KE3 IGBT modules for the AFE unit (with voltage class of 600 V) and GeneSiC GD2X100MPS06N Shottky Diodes for the twelve-pulse rectifier unit (with voltage class of 650 V). For simplicity reasons, the losses have been evaluated considering the characteristics of all devices at 25 °C case temperature.

Fig. 8 show the efficiency plots in all the different examined operating conditions. The efficiencies have been computed considering the harmonic controllers to be activated (which, as previously shown, corresponds to the case with the highest AFE AC currents). The computation has taken into account both conduction and switching losses of all semiconductor devices in the structure (taking into account both the AFE and the DR), but has not considered the losses in the transformer (whose design is out of the scope of this work).

As can be noted, the hybrid AFE+DR circuit can achieve efficiencies around 98%, which is similar to the efficiency that could be achieved through standard full-AFE solutions.

VI. Conclusions

This work analyzed the utilization of an hybrid circuit architecture, based on the series connection of a passive diode rectifier (DR) and an active front end (AFE), as a power supply for future data centers in DC. The main idea is to rely on the simplicity, robustness and cost-effectiveness of the DR, and to use the AFE to compensate its drawbacks, being the lack of DC-bus voltage regulation, the reactive power consumption and the absorption of low-order current harmonics.

From a theoretical analysis it has been shown that, under the requirement of compensating for $\pm 10\%$ voltage variation in the AC grid under any loading condition, the hybrid circuit could ideally lead to a reduction of around 37.5% in the sizing power of the AFE unit, compared to the sizing power in absence of DR. To achieve this reduction, the DR should be designed to provide around 67% of the overall DC-bus voltage and of the required power in rated operating conditions.

However, the presence of a limited voltage class availability of commercial semiconductor devices can impact the design of the system, leading to a sub-optimal solution. This work has considered, as an example, an overall DC-bus voltage of $760\,\mathrm{V}$, for which the theoretical optimum would not be achievable with the commercially available voltage classes. In this case, a more convenient design could be obtained considering an equal 50% split of the DC-bus voltage and of the rated load between the AFE and the DR, allowing the use of $600\,\mathrm{V}$ class semiconductor devices. In this case, the reduction of the size of the AFE would be of just around $25 \div 28\%$ compared to the case without DR.

A simplified design for a $250\,\mathrm{kW}$-$6.6\,\mathrm{kV_{AC}}$-$760\,\mathrm{V_{DC}}$ data center power supply, supported by simulation results in the PLECS environment, has shown that the hybrid circuit can effectively stabilize the overall DC bus voltage and compensate for both reactive power and low-order harmonic pollution towards the AC grid, and that it can achieve similar efficiency performances as a full-scale AFE solution (i.e., around 98%, excluding the transformer losses), despite the presence of more semiconductor devices.

However, the increased complexity in the design of the transformer unit and the sizing power in the DR unit (both aspects which have not been considered in the analysis of this work) can limit the attractiveness of the hybrid solution, which would only be justified if the aforementioned reduction in the AFE sizing power could overcome the required investment in this more complex design (and thus, it can likely be justified only for very high power requirements).

Acknowledgments

The results presented in this paper are part of the project "*Heating Bits*", funded by the École Polytechnique Fédérale de Lausanne (EPFL) through a call *Solutions4Sustainability*.

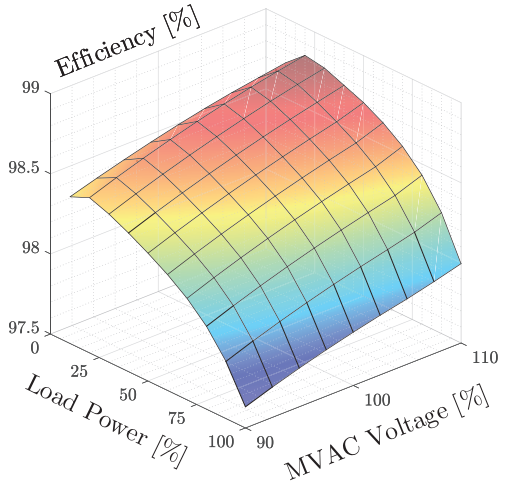

Fig. 8. Efficiency map of the simulated hybrid AFE+DR circuit for varying MVAC voltage magnitude and loading power.

References

[1] Y. Chen, K. Shi, M. Chen, and D. Xu, "Data center power supply systems: From grid edge to point-of-load," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, DOI 10.1109/JESTPE.2022.3229063, no. 3, pp. 2441–2456, 2023.

[2] J. Huber, P. Wallmeier, R. Pieper, F. Schafmeister, and J. W. Kolar, "Comparative evaluation of mvac-lvdc sst and hybrid transformer concepts for future datacenters," in *2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)*, DOI 10.23919/IPEC-Himeji2022-ECCE53331.2022.9807028, pp. 2027–2034, 2022.

[3] P. T. Krein, "Data center challenges and their power electronics," *CPSS Transactions on Power Electronics and Applications*, vol. 2, DOI 10.24295/CPSSTPEA.2017.00005, no. 1, pp. 39–46, 2017.

[4] V. Sithimolada and P. W. Sauer, "Facility-level dc vs. typical ac distribution for data centers: A comparative reliability study," in *TENCON 2010 - 2010 IEEE Region 10 Conference*, DOI 10.1109/TENCON.2010.5686625, pp. 2102–2107, 2010.

[5] Open Compute Project, *Open Compute Project M-CRPS Version 1.04 RC3*, Std., 2024, accessed: 2024-05-18. [Online]. Available: https://drive.google.com/file/d/1b97aRO_2w_SQcgmHw4N_CxOCRVi2v61k/view?usp=drive_link

[6] B. R. Shrestha, U. Tamrakar, T. M. Hansen, B. P. Bhattarai, S. James, and R. Tonkoski, "Efficiency and reliability analyses of ac and 380 v dc distribution in data centers," *IEEE Access*, vol. 6, DOI 10.1109/ACCESS.2018.2877354, pp. 63 305–63 315, 2018.

[7] A. N. S. Institute and BICSI., *ANSI/BICSI 002-2011: Data Center Design and Implementation Best Practices*. BICSI, 2011. [Online]. Available: https://books.google.ch/books?id=dtdqngEACAAJ

[8] European Telecommunications Standards Institute (ETSI), *ETSI EN 300 132-3 V2.3.1 (2023-01)*, Std., Jan. 2023, accessed: 2024-05-18. [Online]. Available: https://www.etsi.org/deliver/etsi_en/300100_300199/30013203/02.03.01_60/en_30013203v020301p.pdf

[9] European Committee for Electrotechnical Standardization (CENELEC), *EN 50160: Voltage characteristics of electricity supplied by public distribution networks*, Std., 2010, accessed: 2024-05-18.

[10] P. Pejovic and J. W. Kolar, "Exact analysis of three-phase rectifiers with constant voltage loads," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 55, DOI 10.1109/TCSII.2008.922462, no. 8, pp. 743–747, 2008.