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DC Power Distribution Networks with Direct Current Transformers

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Abstract

The shift towards DC power distribution networks, enabled by power electronics technologies, is changing the nature of electrical power systems. Nowadays, DC power distribution networks can effectively support the high penetration of distributed energy resources and energy storage integration (both increasingly being DC by nature) in future electrical systems.

To facilitate this transition, a converter that brings the features and simplicity of the AC transformer to the DC systems is needed. In this context, the DC transformer serves as an analogy to the AC transformer, playing a crucial role in developing advanced DC power systems by integrating various power sources and loads across different voltage levels. More specifically, the DC transformer, built on the LLC converter, is capable of establishing the current path between two DC buses following the natural power flow of the system. This passive behavior is possible through its open-loop operation and a nearly constant gain under various load conditions, particularly for near-resonant frequency operation. Consequently, the simple nature of AC transformers can be replicated in the DC transformer with the assistance of some additional operational logic.

The focus of this thesis is to investigate the DC transformer, its features, and its impact on the DC power distribution networks. This thesis is divided into two parts. The first part concerns the DC transformer. It demonstrates the essential strategies for reliable open-loop operation. This thesis presents the strategies of power reversal to allow bidirectional operation, soft start for smooth initialization, and idle mode operation to avoid unnecessary no-load losses. The developed methods are validated with two low-voltage prototypes developed in the laboratory. Besides that, the scalability aspect of the DC transformers by connecting several units in parallel is investigated with a sensitivity analysis of the resonant parameters. This analysis is performed using the input impedance to predict the current sharing unbalance between modules, and a strategy to enhance the current sharing is proposed to compensate for the parameter tolerances and ensure a satisfying current sharing. Lastly, a medium voltage prototype was built as a result of the research project, and two aspects of static voltage balancing for the Neutral-Point Clamped leg are investigated, along with an evaluation of the dynamic voltage balancing to ensure Zero-Voltage Switching during operation.

The second part of the thesis focuses on the system-level analysis of DC power distribution networks with DC transformers. The required mathematical tools and the developed methodology are presented and evaluated for DC systems. This methodology is independent of the AC system loop, where the system's representation is based on the Modified Nodal Analysis, and uses the Harmonic Resonance Mode Analysis for the frequency domain representation. Furthermore, with the assistance of a developed hardware-in-the-loop platform, more complex DC power distribution networks were evaluated focusing on the operation of the system. The impact of different DC power distribution architectures, the speed of the AC-DC voltage control, and the AC grid impedance on the resonant characteristics of the system are evaluated and demonstrated under various scenarios. The developments allow the investigation regarding the planning and expansion aspects, operability, and stability verification of the future DC power distribution networks with DC Transformers.

The main contributions of this thesis are the demonstration of the essential features of DC transformers and to the development of a scalable methodology for system analysis of multi-converter DC power distribution networks with DC transformers. The modeling framework and methodology are described, discussed, and validated with experimental results.

Keywords: dc power distribution networks, direct current transformers, hardware-in-the-loop, LLC resonant converter, modified nodal analysis, modal resonant analysis, solid-state transformer.

Résumé

La transition vers des réseaux de distribution d'énergie en courant continu, rendue possible par les technologies de l'électronique de puissance, modifie la nature des systèmes de distribution électrique. Actuellement, les réseaux de distribution d'énergie en courant continu peuvent efficacement soutenir la forte pénétration des ressources énergétiques distribuées et l'intégration de stockage d'énergie dans les futurs systèmes électriques.

Pour faciliter cette transition, un convertisseur capable de transposer les caractéristiques et la simplicité du transformateur CA aux systèmes CC est nécessaire. Dans ce contexte, le transformateur CC joue un rôle crucial analogique au transformateur CA, ainsi, il permet le développement de systèmes d'alimentation en courant continu avancés en interfaçant diverses sources et charges de niveaux de tension différents. Plus spécifiquement, le transformateur CC, fondé sur le convertisseur LLC, est capable d'interconnecter deux bus CC en établissant un transfert de puissance naturel. Ce comportement passif est possible grâce à son fonctionnement en boucle ouverte et à un gain en tension presque constant dans diverses conditions de charge, en particulier pour une opération à fréquence quasi résonante. Par conséquent, la nature simple des transformateurs CA peut être reproduite dans le transformateur CC à l'aide d'une logique opérationnelle supplémentaire.

Le focus de cette thèse est d'étudier le transformateur CC, ses caractéristiques et son impact sur les réseaux de distribution d'énergie en CC. Cette thèse est divisée en deux parties. La première partie concerne le transformateur CC. Elle présente les stratégies essentielles pour le fonctionnement en boucle ouverte fiable du transformateur CC. Cette thèse expose les stratégies d'inversion de puissance pour permettre un fonctionnement bidirectionnel, un démarrage en douceur pour une initialisation fluide, et un fonctionnement en mode veille pour éviter les pertes inutiles à vide. Les méthodes développées sont validées avec deux prototypes basse tension développés en laboratoire. De plus, l'aspect de la scalabilité des transformateurs CC en connectant plusieurs unités en parallèle est étudié avec une analyse de sensibilité des paramètres résonants. Cette analyse est réalisée en utilisant l'impédance d'entrée pour prédire le déséquilibre dans le partage de courant entre les modules, et une stratégie pour améliorer cet équilibre est proposée pour corriger les tolérance des paramètres et assurer un partage de courant satisfaisant. Enfin, un prototype moyenne tension a été construit à la suite du projet de recherche, et deux aspects d'équilibrage statique pour la branche NPC sont étudiés, ainsi qu'une évaluation de l'équilibrage dynamique pour assurer le fonctionnement en commutation à tension nulle.

La deuxième partie de la thèse se concentre sur des réseaux de distribution d'énergie en CC avec des transformateurs CC. Les outils mathématiques nécessaires et la méthodologie développée sont présentés et évalués pour les systèmes en courant continu. Cette méthodologie est indépendante de la boucle du système en courant alternatif, où la représentation du système est basée sur l'Analyse Nodale Modifiée, et utilise l'Analyse de Mode de Résonance Harmonique pour la représentation en domaine fréquentiel. De plus, à l'aide d'une plateforme "hardware-in-the-loop", des réseaux de distribution d'énergie en CC plus complexes ont été évalués en se concentrant sur le fonctionnement du système. L'impact de différentes architectures de distribution d'énergie en CC, la vitesse du contrôle de tension CA-CC, et l'impédance du réseau CA sur les caractéristiques résonantes du système sont évalués et démontrés sous divers scénarios. Les développements permettent d'explorer les aspects de planification et d'expansion, d'exploitabilité et de vérification de la stabilité des futurs réseaux de distribution d'énergie en CC avec des transformateurs CC.

Les principales contributions de cette thèse sont de démontrer les caractéristiques essentielles des

transformateurs CC et de développer une méthodologie extensible pour l'analyse du système des réseaux de distribution d'énergie en CC à plusieurs convertisseurs avec des transformateurs CC. Le cadre de modélisation et la méthodologie sont décrits, discutés et validés avec des résultats expérimentaux.

Keywords: Analyse de Mode de Résonance Harmonique, Analyse Nodale Modifiée, Convertisseur LLC, Distribution d'énergie CC, Hardware-in-the-Loop, transformateur CC, transformateur à semi-conducteurs.

Resumo

A mudança para redes de distribuição de energia em CC, possibilitada pelas tecnologias de eletrônica de potência, está alterando a natureza dos sistemas elétricos. Atualmente, as redes de distribuição de energia em CC podem efetivamente suportar a alta penetração de recursos de energia distribuída e a integração de sistemas de armazenamento de energia, ambos cada vez mais baseados em CC, nos sistemas elétricos futuros.

Para facilitar essa transição, é necessário um conversor que traga as características e a simplicidade do transformador CA para os sistemas em CC. Neste contexto, o transformador CC atua como uma analogia ao transformador CA, desempenhando um papel crucial no desenvolvimento de sistemas avançados de energia em CC, integrando diversas fontes de energia e cargas em diferentes níveis de tensão. Mais especificamente, o transformador CC, baseado no conversor LLC, é capaz de estabelecer o caminho da corrente entre dois barramentos de CC, seguindo o fluxo natural de energia do sistema. Esse comportamento passivo é possível por meio de sua operação em laço aberto e um ganho quase constante sob várias condições de carga, especialmente para operação em frequência próxima da ressonância. Consequentemente, a natureza simples dos transformadores em CA pode ser replicada nos transformadores em CC com a ajuda de algumas lógicas adicionais.

O foco desta tese é investigar o transformador CC, suas características e seu impacto nas redes de distribuição de energia em CC. Esta tese é dividida em duas partes. A primeira parte aborda o transformador CC ressonante, demonstrando as estratégias essenciais para a operação em laço aberto. Ela apresenta as estratégias de reversão de energia para permitir a operação bidirecional, a partida suave para inicialização e a operação em modo ocioso para evitar perdas desnecessárias sem carga. Os métodos desenvolvidos são validados com dois protótipos de baixa tensão desenvolvidos em laboratório. Além disso, a escalabilidade dos transformadores em CC, conectando várias unidades em paralelo, é investigada com uma análise de sensibilidade dos parâmetros ressonantes. Esta análise utiliza a impedância de entrada para prever o desequilíbrio no compartilhamento de corrente entre os módulos. Assim, uma estratégia para melhorar o compartilhamento de corrente e corrigir as tolerância de parâmetros é proposta. Por fim, um protótipo de média tensão foi construído como resultado do projeto de pesquisa, e dois aspectos do balanceamento estático para o estágio de potência foram avaliados assim como a avaliação do balanceamento dinâmico para garantir comutação com zero tensão durante a operação.

A segunda parte da tese foca na análise em nível de sistema das redes de distribuição de energia em CC com transformadores em CC. As ferramentas matemáticas necessárias e a metodologia desenvolvida são apresentadas e avaliadas para sistemas em CC. Esta metodologia é independente do laço do sistema em CA, onde a representação do sistema se baseia na Análise Nodal Modificada e utiliza a Análise do Modo de Ressonância Harmônica para a representação no domínio da frequência. Além disso, com a plataforma hardware-in-the-loop desenvolvida, redes de distribuição de energia em CC mais complexas foram avaliadas, focando na operação do sistema. O impacto de diferentes arquiteturas de distribuição de energia em CC, da velocidade do controle de tensão CC e a impedância da rede em CA nas características ressonantes do sistema são avaliados e demonstrados em vários cenários. Os desenvolvimentos permitem a investigação sobre os aspectos de planejamento e expansão, operabilidade e verificação de estabilidade das futuras redes de distribuição de energia em CC com transformadores CC.

As principais contribuições desta tese são a demonstração das características essenciais dos transformadores CC e o desenvolvimento de uma metodologia escalável para a análise de sistemas de redes

de distribuição de energia CC com transformadores CC. Os modelos e metodologia são descritas, discutidas e validadas com resultados experimentais.

Keywords: Análise resonante modal, Analise Nodal Modificada, Conversor LCC, Distribuição de energia CC, Hardware-in-the-Loop, Transformador CC, Transformador de estado sólido.

Acknowledgments

Your true self is your best self
Anonymous

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List of Abbreviations

CHIL	Control Hardware-in-the-Loop
CPL	Constant Power Load
DAB	Dual Active Bridge
DCT	DC Transformer
DFT	Discrete Fourier Transform
DSP	Digital Signal Processor
ESS	Energy Storage Systems
EV	Electric Vehicle
FB	Full-Bridge
FC	Flying Capacitor
FHA	First Harmonic Approximation
GNC	Generalized Nyquist Criterion
GUI	Graphic User Interface
HB	Half-Bridge
HIL	Hardware-in-the-loop
HVAC	Heating, Ventilation, and Air Conditioning
HVDC	High Voltage DC
IBR	Inverter-Based Resources
LVAC	Low Voltage AC
LVDC	Low Voltage DC
MFT	Medium Frequency Transformer
MNA	Modified Nodal Analysis
MTDC	Multi-Terminal DC
MVDC	Medium Voltage DC
NPC	Neutral Point Clamped
NZE	Net Zero Emission

PCC	Point of Common Coupling
PDN	Power Distribution Network
PEBB	Power Electronics Building Block
PHIL	Power Hardware-in-the-Loop
PRBS	Pseudo-Random Binary Sequence
PRC	Parallel Resonant Converter
PRM	Power Reversal Method
PV	Photovoltaics
QZCS	Quasi-Zero Current Switching
RMA	Resonant Modal Analysis
SCR	Short-Circuit Ratio
SFP	Small Form-factor Pluggable
SRC	Series Resonant Converter
SST	Solid-State Transformer
VSD	Variable Speed Drives
VSI	Voltage Source Inverter

List of Symbols

$\boldsymbol{H_z}$	Impedance transfer function matrix
$\boldsymbol{I}$	Current vector
$\boldsymbol{V}$	Voltage vector
$\boldsymbol{Y_{nodal}}$	Admittance nodal matrix
C_r	Resonant capacitance
G_x	Conductance x
$I_{DCT,x}$	DC current of the DCT x
$I_{dc,x}$	DC current of port x
$I_{red,x}$	Resonant current of side x
$I_{res,x}^{rms}$	RMS value of the resonant current of the side x
I_{th}	Threshold value current
L_m	Magnetizing Inductance
L_r	Leakage Inductance
P_{DCT}^{th}	Threshold value for the power of the DCT
P_{dc}	DC power
R_l	Load resistance
T_s	Switching period
V_{ab}	Voltage applied to the resonant tank
$V_{dc,x}$	DC voltage of port x
Y_l	Load equivalent admittance
Y_s	Source equivalent admittance
Y_x	Admittance x
Z_{dct}	Input impedance of the DCT
Z_{in}	Input impedance
Z_o	Output impedance
$\Delta V_{DCT,x}$	Voltage difference across the DCT x
ΔV_{DCT}^{th}	Threshold value for the voltage difference across DCT
Δ_f	Frequency variation
$\delta_{I(m,n)}$	Input impedance ratio between DCTs m and n
a	Transformation ratio of the transformer
f_r	Resonant frequency
f_s	Switching frequency
u_x	Undefined DC voltage of port x

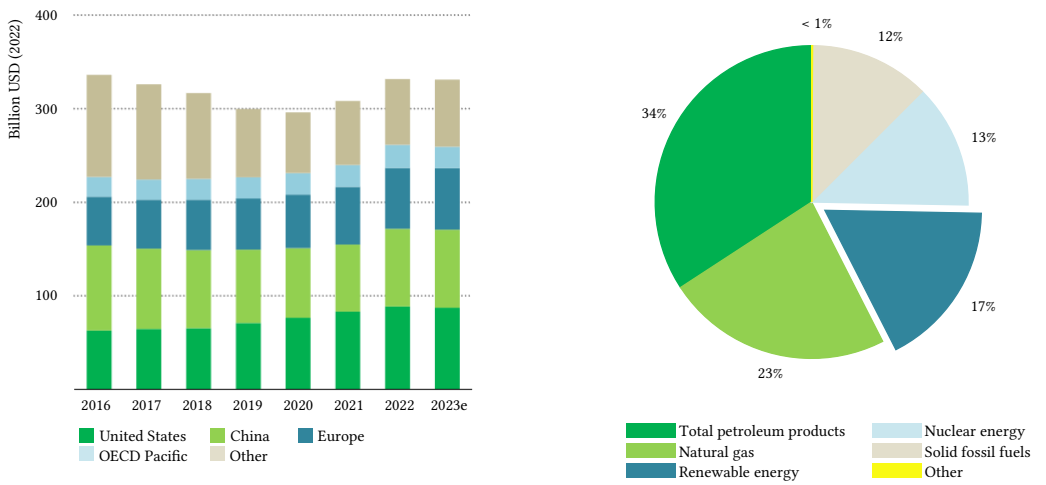
Contents

1 Introduction

1.1 The Future of Power Distribution Systems

Over the years, society has recognized the need to change the way of producing, transmitting, and using electrical energy. Particularly, after decades of climate change investigation [1] and the recent energy crisis [2], investments in R&D continue to rise over the years focusing on developing more eco-friendly and efficient electrical systems [3]. In particular, investments related to grid infrastructure have recovered after a downtrend as shown in **Fig. 1.1a**.

Apart from this movement, there is an interest from governments, and policymakers to promote the use of electrical energy in the mobility sector [4]–[6]. At first glance, such incentives seem contradictory to the climate-related agreements [7], considering that most of the electrical energy mix is based on fossil fuels, as detailed in **Fig. 1.1b**. However, this puts pressure on the energy providers to react to society's demands and increase the use of renewables in the generation matrix.



(a) (b)

Fig. 1.1 (a) Investment in power grid infrastructure by geography from 2016 to 2023e (expected) from [3]. (b) Details on the mix of electrical energy consumption of EU in 2021, adapted from [8].

With all these new demands, the power grid needs to adapt to deal with the incoming new loads and intermittent and distributed generation of the future. This leaves space for some reconsideration related to the traditional methods of power distribution and raises the question if there are other

options that could assist the transition to a Net Zero Emission (NZE) energy sector [9].

The electrical distribution system of today relies on well-established concepts of AC technology. The main advantage of the AC is the simple voltage adaptation using power transformers, which allows the transmission and distribution of energy with different voltage levels.

On the other hand, DC technology has been used for many years for power transmission over long distances due to reduced transmission losses, however, by the fact that the voltage adaptation is not so simple, the distribution in DC is not broadly used. Nevertheless, considering its benefits with the new type of loads and generations, DC distribution is considered an option for the required energy transition.

In particular, the Medium Voltage DC (MVDC) Power Distribution Network (PDN) has been studied as a potential solution to revolutionize the way we distribute power [10]. The DC PDN has several advantages when considering Energy Storage Systems (ESS) and Photovoltaics (PV) which are naturally DC, and the new types of loads as electric vehicles (EVs), which can be easily integrated into the DC system. In some cases, the DC PDN has already been considered a good solution for Wind Farm collectors [11] and PDN in marine vessels [12]. However, one essential technology to enable a more complex DC PDN is still underdeveloped, which is the equivalent element to the AC transformer - DC Transformer (DCT), and the main topic of this thesis.

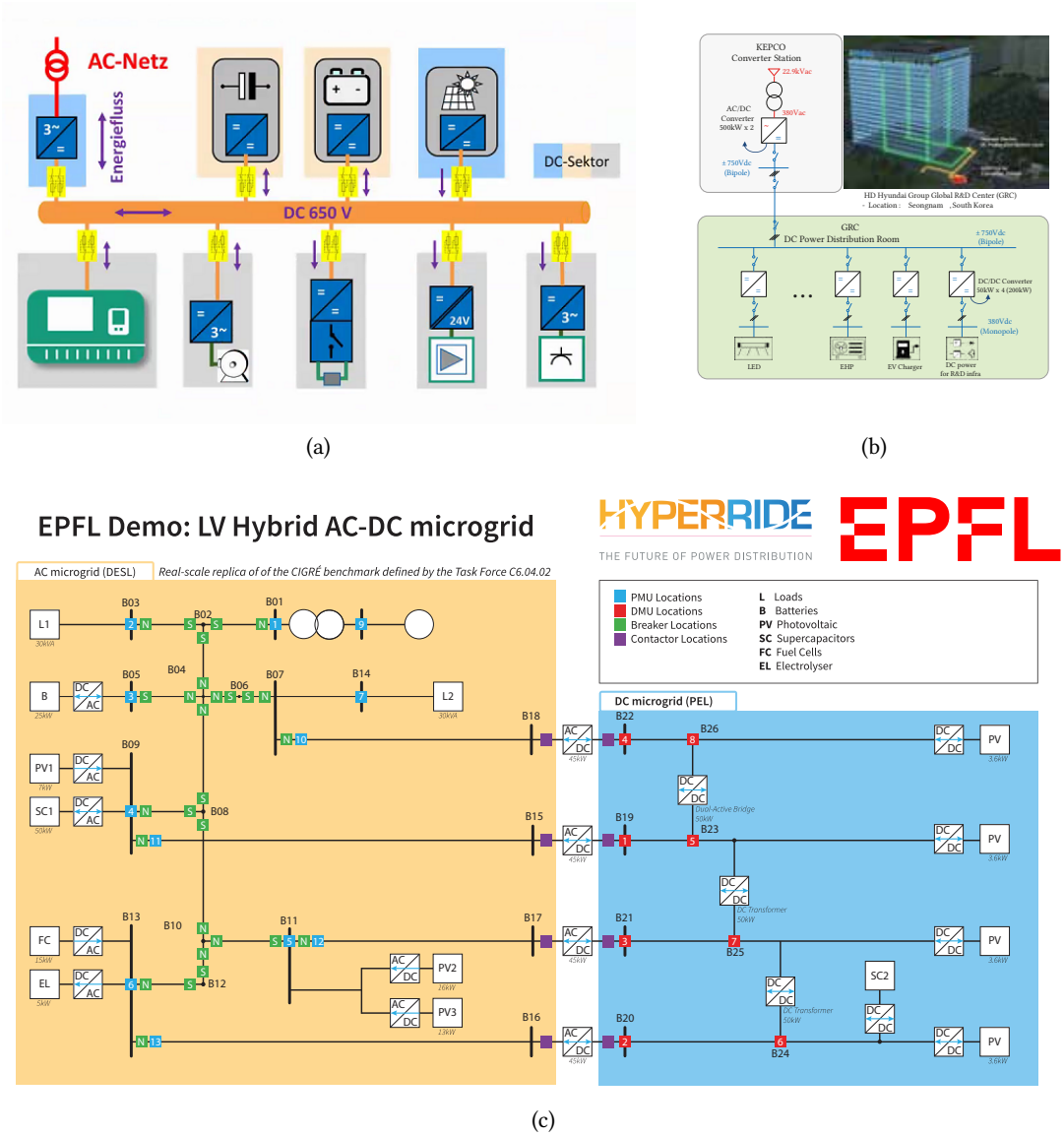
Although numerous challenges are yet to be overcome regarding MVDC PDN, the next generation of power distribution will be supported by new technologies that empower the new type of demand of society and meet the regulatory guidelines for clean energy consumption. In the next sections, the challenges of the DC PDN and the DCT will be further discussed, with examples of the ongoing projects.

1.2 DC Technologies and MVDC Perspectives

For every device used in our daily life, there is a solution in AC or DC, in all voltage ranges. From the most basic use for lighting to more complex uses for Variable Speed Drives (VSD). Usually, the choice for a specific technology is driven by reliability and cost, and its break-even point, as it is for long-distance power transmission with High Voltage DC (HVDC), and house installations with Low Voltage AC (LVAC). Furthermore, once the solution dominates the market, it takes a long time for the alternative or emerging solution to be reconsidered. For that to happen, extensive research and demonstrations are required to create enough evidence and clear benefits for new investments.

Nowadays, with the increasing interest in distributed Inverter-Based Resources (IBR) combined with ESS, the DC PDN emerges as a solution for easy integration of such technologies. This is supported by concerns about the safe operation of the classical grids when IBR are massively deployed. In literature, some works have reported that the massive inclusion of intermittent power generation in AC grids can cause stability problems [13], mainly in weak AC grids. Also, when considering these sources in the same level of power capacity as the controlled sources (e.g., Hydro generation, Gas, Nuclear, etc.), the system is highly dependent on good power management.

The main advantage of the DC PDN is to allow easy integration and simple power flow control. In the last few years, several projects have been focused on developing the Low Voltage DC (LVDC) PDN, in the range of $0 - 1.5$ kV [14]. **Fig. 1.2** shows three examples of projects and relevant layouts.



(a) (b)

(c)

Fig. 1.2 (a) DC INDUSTRIE I and II [15], focused on demonstrating the feasibility of DC PDN for factories and reducing the number of AC-DC conversions. (b) Hyundai DC Building [16], focused on the demonstration of the DC PDN for buildings. And (c) HYPERRIDE Project [17], focused on demonstrating the AC-DC Hybrid grid operation, protection, and feasibility.

One of the most prominent projects in this area is the DC INDUSTRIE I and II [15]. In this project, the partners worked to investigate and deploy a DC infrastructure in factories, to reduce losses by removing the AC-DC conversion stages. Furthermore, the project explores the integration of renewable on the DC system and proposes standards in terms of voltage levels and protection schemes. Out of this project, the Open DC Alliance (ODCA) was created to disseminate the discoveries, promote activities of DC grids, and bring the DC technologies to the market [18].

Similarly, the CurrentOS foundation [19] aims to create an ecosystem of manufacturers of compatible

Tab. 1.1 Nominal operating voltages of different LVDC PDN projects, highlighting the lack of standards.

Project	Voltage level (V)	Focus
DC INDUSTRIE [15]	650 540	DC PDN for factories
Hyundai DC Building [16]	±750 380	Lighting, HVAC and EV Chargers
ABB Ship On-board DC PDN [25]	1000	Ferry, Platform support
Siemens Ship On-board DC PDN [26]	1000	Ferry, Offshore construction and support
HYPERRIDE [17]	750	Feasibility and protection investigation
Current OS [19]	700 350	Integration of DC technology
EnergyVille [23]	±500	Operation of DC PDN with ESS
Seogeochado DC Microgrid [27]	±750 750 ±190	Operation of DC microgrid
Tangjia Bay MVDC distribution pilot project [28]	±10000 ±375 ±110	ESS and IBS interface
Datacenter EPRI [21]	±190	DC PDN for DC loads

products to ensure reliable and safe DC systems. It identifies the gaps in standards and promotes a set of rules concerning voltage levels, communication protocols, and safety requirements.

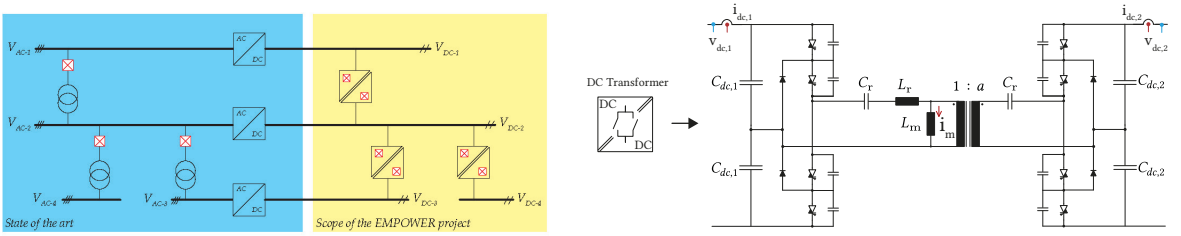
Another example of LVDC PDN is the Hyundai DC building [16]. In this case, a DC PDN was installed to study the feasibility and provide energy to the lighting, Heating, Ventilation, and Air Conditioning (HVAC) system, EV charging stations, and laboratory facilities. According to the report in [20], it is expected to reach an energy savings of over 10% per year compared to the AC supply method.

It is noteworthy to mention that another application of LVDC is in the PDNs of data centers [21]. With a DC PDN, benefits are expected in terms of the reduced number of conversion stages, which can increase the overall efficiency, and reduce the complexity of the systems [22].

In the research side of the LVDC systems, the HYPERRIDE project [17], focuses on demonstrating the operational feasibility of DC PDN in a hybrid AC-DC system. In this project, several partners work in different aspects focusing on protection, system operation, and implementation. Similarly, campus Energy Ville [23], investigates the LVDC PDN operability, considering the integration of renewables and ESS as a solution for buildings and communities. Also, the project TIGON [24] investigates the hybrid AC-DC grid evaluating its performance, cost efficiency, reliability, and resilience.

In summary, the LVDC PDNs have been developing over the years and this step is crucial to develop the market for the broader implementation of DC systems. Furthermore, all these projects mention the lack of standards for such a system, which are essential for the development of the complete ecosystem. **Tab. 1.1** shows the nominal operating voltage of several use cases of LVDC PDN, showing the lack of standards.

When considering MVDC systems, the DC voltage range is from 1.5 kV to ±50 kV [29]. Several applications have been using this voltage range to transmit power or to drive machines. In shipboard



(a) (b)

Fig. 1.3 (a) Example of an MVDC PDN and scope of the EMPOWER project in yellow. (b) DCT based on resonant LLC converter used for bus interface.

PDN, the use of MVDC PDN brings potentially big savings by reducing the weight of the vessel, leading to less fuel consumption [30]. Applications such as point-to-point links [31], and offshore Wind Farms collectors also choose MVDC to reduce construction area, and transmission losses [32].

However, all these applications are derived from the HVDC know-how, hence the simplicity of the system. When considering the power distribution system and integration of ESS and IBR, more advanced architectures are required, together with different voltage levels, and in some cases, a centralized system operator.

In this sense, several projects investigate the MVDC grid feasibility [33], [34], its implementation [35], the economic viability [36], protection [37], and the grid optimization as a solution for the power distribution of the future [38]. However, the commercialization aspect is still weak. The lack of standards, protection schemes, and economic benefits put this solution on hold. Still, the development of protection devices, MV converters, and tools for planning and operation of the DC PDN is crucial to solving the drawbacks of the MVDC grid.

The project EMPOWER [39], aims to develop the DCT to provide the transformer features for the DC PDN and investigate the operability of a system with a large number of these converters. **Fig. 1.3a** shows the scope of the project. In short, this project focuses on the development of a bidirectional, isolated, MV DC-DC resonant LLC converter. Besides that, the project includes the investigation of the operational principles and functionalities of the DCT, and the planning and operation analysis of the DC PDN with DCTs.

Conceptually, DCTs can be considered the missing link to enable DC PDN in a broad sense [40]. The DCT is the converter capable of providing the current path between two DC buses without the need for a set point or a reference from a control point of view. It simply follows the natural power flow of the system, bringing the simplicity of the power transformer that enabled the extraordinary development of AC distribution systems. However, there are a few extra challenges that require special attention, mainly in terms of the design and performance using the existing technologies and costs.

1.3 DC-DC Converters for MVDC Power Distribution Networks

To achieve the necessary power ratings, required voltage adaptation, and operational features, the MV DC-DC converters can be designed in two different ways. The first type relies on fractional

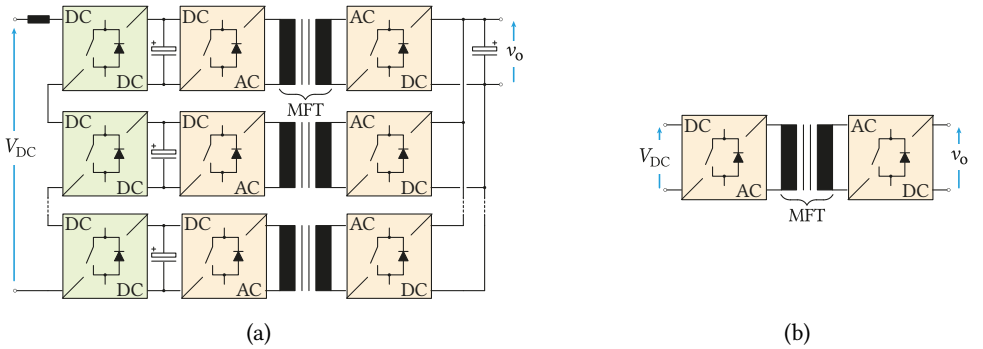


Fig. 1.4 (a) Example of fractional power processing, with multiples MFTs. (b) Example of bulk power processing, with a single MFT.

power processing, where the power electronics building blocks (PEBBs) are connected in series and parallel to reach the specifications, each of them with its own Medium Frequency Transformer (MFT). **Fig. 1.4a** shows an example of series input and parallel output configuration. The main advantage of this approach is the easy scaling of the overall converter, while extra units could be added for redundancy. However, the disadvantage is that the system's reliability is compromised due to the number of components.

The second approach focuses on developing a single converter with higher ratings, upscaling the switches in series or parallel if necessary, with a single MFT as shown in **Fig. 1.4b**. This monolithic approach can be considered simpler, having a reduced amount of components improving reliability, and reducing control complexity. In particular, when considering the MVDC PDNs application, the DC-DC converter needs to achieve high levels of reliability, which benefits from this solution.

Fig. 1.5 shows three MV DC-DC prototype converters. Two of them are based on the Dual Active Bridge (DAB) converter, and one is on the Series Resonant Converter (SRC). Firstly, **Fig. 1.5a** shows an IGCT-based, 5 : 5 kV, 5.6 MW, 1 kHz 3ph-DAB. This prototype was developed as part of the FEN project [35], which consists of a demonstration of MVDC PDN. The second converter, shown in **Fig. 1.5b** is an IGCT-based, 10 : 10 kV, 3 MW, 600 Hz DAB. In this prototype, a series of connections of devices to reach this voltage and soft commutation modulation was used successfully [41]. The third converter, shown in **Fig. 1.5c**, is an IGCT-based, 10 : 5 kV, 1 MW, 5 kHz LLC converter. This prototype is developed as part of the EMPOWER project [39], and its highlight is the high-frequency switching of IGCTs.

Notably, when considering bulk power processing, the IGCT-based converter is preferred due to the high current capability, high voltage ratings, and most importantly, low conduction losses [43]. In the area of fractional power processing, especially for MV power converters in traction power supply [44] and railway applications [45], [46], IGBT switches have been used successfully, taking advantage of the reduced size compared to the IGCT solution.

Ultimately, the main objectives of the DCT for MVDC PDNs are: i) Expansion of the existing power system; and ii) Assisting the penetration of renewable energy sources. Thus, the power converter needs to focus on high efficiency, simplicity, robustness, and reliability. Another very welcome feature for the DC PDNs is the load-independent behavior of the LLC converter when operating close to the resonant frequency. This natural feature enables the operation without a closed-loop control and

(a) (b) (c)

Fig. 1.5 MV DC-DC converter based on bulk power processing. (a) 5:5 kV DAB prototype developed by E-ON Aachen University [42], (b) 10:10 kV DAB prototype developed by Tsinghua University [41], and (c) 10:5 kV LLC prototype in development by EPFL.

guarantees a stiff voltage gain for any load condition. In this sense, the LLC converter follows the power flow given by the DC buses naturally.

Works investigating high-power medium voltage LLC converters have highlighted the challenges of its operation [47] and construction [48], [49]. These challenges consist of the safe operation of power stages, the investigation related to the use of higher rating switches, and the development of MV DCT PEBB. Nevertheless, further development and investigation are still required to demonstrate such a solution on a full scale.

Finally, although the scalability of the monolithic approach is not so simple compared to the fractional power processing approach, this solution is well suited for MVDC PDNs when ratings and regulations are set. Further, the LLC converter as the DCT provides all the most-wanted features of a transformer and its development and impact on the DC PDN requires further investigation.

1.4 Objectives and Contribution of the Thesis

Given the above discussion, there is still a long journey for a broad implementation of MVDC distribution systems taking advantage of DCTs for voltage adaptation. This work focuses on the requirements of DCTs for an open-loop operation and performs system-level studies for the DC system's planning and operation. The main objectives of the thesis can be summarized by the following points:

- Development and demonstration of DCT.
  - Development and investigation of the required control strategies for the reliable open loop operation of DCT, including different operation modes. This includes the evaluation of different methods for power reversal, soft-start speed, no-load operation, and parallel operation.
  - Development and construction of the prototypes, control and protections, and test setup. Two LV DCT prototypes were built to validate control strategies and DC grid studies. Also, one MV DCT was built as part of the project to demonstrate the technology for future MVDC PDNs.

- Investigation of DC PDNs operational performances with several converters and DCTs.
  - This includes modeling, simulation, stability analysis, and power flow studies with a multi-converter DC system. The planning and operating aspect of DC PDN is addressed to identify critical points of operation.
  - This thesis also includes the development of a Real-Time (RT) Hardware-In-The-Loop (HIL) platform for modeling and simulation of large DC PDN. The operation of an MVDC PDN is demonstrated in this thesis validating the proposed methodology to evaluate DC grids.

The main contributions of the thesis are highlighted:

- Development and demonstration of most important control strategies for the open-loop operation of DCT.
- Evaluation of the scalability capability of DCTs, and development of a solution for current sharing unbalance.
- Development of a scalable methodology to analyze DC PDN with DCTs without the support of AC system variables.
- Development of an RT-HIL platform for large DC PDN analysis.

1.5 Outline of the Thesis

The thesis is organized in two parts and contains nine chapters. The first part focuses on the power electronics side of the research, which includes the DCT modeling, development of control strategies for open-loop operation, sensitivity analysis for scalability purposes, and the development of prototypes. This part is divided as follows:

- **Chapter 2** describes the resonant LLC converter and relevant equivalent models. It includes the operating principles of resonant converters and pertinent modeling tools. In this chapter, the first harmonic approximation, the most used model for resonant converters, is employed to draw the design rules of the DCT. Further, the DC terminals' behavior model and the small signal modeling are discussed as both are used in this thesis. With this comprehensive overview, this chapter provides the basic foundation for all the subsequent discussions in the thesis.
- **Chapter 3** details the operation principles of DCT. In this chapter, the developed control algorithms are presented, discussed, and demonstrated with an LV prototype. It includes the evaluation of the soft-start strategy to protect the converter against over-current and saturation during start-up. Also, this chapter explores four distinct power reversal methods that determine the power direction of the DCT based on measurements. Lastly, the idle mode is explained, wherein the converter remains idle when no power is being transferred, effectively reducing no-load losses. All these strategies together guide the operation of the DCT.
- **Chapter 4** details the design of the MV DCT prototype. In this chapter, the challenges of the dynamic and static voltage balancing of the split-capacitor IGCT 3L-NPC leg operating in a two-level, 50% duty cycle mode are investigated. It includes the analysis of the switching transient behavior under different turn-off current conditions and the performance of the dynamic balancing with a low-value capacitor snubber. Further, a comparative analysis of two

static balancing strategies is presented, considering the simple use of balancing resistors in parallel to each IGCT and the use of a single symmetrizing resistor in parallel to the inner two IGCTs. The snubbers' designs are verified by experiments on the 5 kV 3L-NPC stack.

- **Chapter 5** focuses on the scalability aspect of DCTs. In this chapter, the parallel operation of DCTs is evaluated with a sensitivity analysis to identify the quality of such an arrangement and point out the limitations, trade-offs, and a solution to achieve satisfying current sharing. The analysis is based on the input impedance of the small signal model, where the critical parameters are identified, and the impact of the different levels of parameter variation on the current sharing of DCTs is evaluated. Then, design constraints based on the model are set to achieve satisfying current sharing considering the resultant input impedance. Furthermore, the impact of the switching frequency, considered the only design degree of freedom, on the input impedance, is used to modify the current sharing between the modules. Experimental results with the two LV DCT prototypes validate the methodology.

The second part focuses on the system-level analysis of DC PDNs with DCTs. In this part, the required mathematical tools and the developed methodology are presented and evaluated for DC systems. Further, with the assistance of the HIL platform, a more complex DC PDN is evaluated focusing on the operation of the system. This part is divided as follows:

- **Chapter 6** presents the modeling tools and developed methodology to evaluate DC PDNs. In this chapter, the Modified Nodal Analysis (MNA), and the Harmonic Resonance Modal Analysis (RMA) are described for DC systems and evaluated with relevant studies. The MNA allows the solution to overcome the lack of the voltage angle and reactive power to calculate the power flow using a nodal approach. With the RMA, each element is characterized with the equivalent impedance in the frequency domain, allowing one to compute the node's impedance, within the voltage control bandwidth. In the end, this methodology allows a scalable and straightforward procedure to compute each node impedance regardless of the system configuration. This enables further studies with larger systems, system planning and operation analysis, stability analysis, and others.

- **Chapter 7** extends the developed methodology to analyze DC PDN. It includes the evaluation of the transmission line, DCT's location, and AC-DC converter's control speed impact on the system's resonant characteristics. In this chapter, the methodology presented in Chapter 6 is tested under different scenarios showing that it provides enough information to predict the system performances for future DC PDNs. The system stability is tested for the system expansion by including an extra converter to the grid and verified by eigenanalysis. Lastly, the methodology is tested for different network architectures, aiming to verify and test the solver for radial, ring, and meshed systems.

- **Chapter 8** presents the RT-HIL platform developed for system analysis. The RT-HIL is used to demonstrate the developed methodology in a large system with real controllers. This chapter investigates the system operation with several DCTs operating together in a meshed system. The power load flow and the DC nodal impedances are analyzed and compared with the mathematical model. The HIL simulation is also used to investigate the elements that impact the modes of the system, and the operation limits of the system. The system is tested without centralized control, relying only on the controlled converters at each DC bus. In the end, the HIL simulation assisted in verifying the proposed methodology to analyze DC PDNs.

- **Chapter 9** provides the summary of the findings, contributions of this thesis and the future work to be carried out.

1.6 List of Publications

Journal papers [50]–[52]:

J1. **R. P. Barcelos** and D. Dujic, "Scalability Assessment of the Parallel Operation of Direct Current Transformer," *CPSS Transactions on Power Electronics and Applications*, vol. 8, no. 4, pp. 397–410, 2023.

J2. **R. P. Barcelos**, J. Kucka, and D. Dujic, "Power Reversal Algorithm for Resonant Direct Current Transformers for DC Networks," *IEEE Access*, vol. 10, pp. 117 - 127, 2022.

J3. **R. P. Barcelos** and D. Dujic, "Direct Current Transformer Impact on the DC Power Distribution Networks," *IEEE Transactions on Smart Grid*, vol. 13, no. 4, pp. 2547–2556, 2022.

Conference papers [53]–[57]:

C1. **R. P. Barcelos**, N. Djekanovic, and D. Dujic, " Static and Dynamic Voltage Balancing for an IGCT-Based Resonant DC Transformer", in *2024 IEEE 10th International Power Electronics and Motion Control Conference (IPEMC2024-ECCE Asia)*, 2024.

C2. **R. P. Barcelos** and D. Dujic, "Voltage Balancing of a Split-Capacitor IGCT 3L-NPC Leg for the Resonant DC Transformer," in *PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2024.

C3. **R. P. Barcelos** and D. Dujić, "On Features of Direct Current Transformers," in *2023 11th International Conference on Power Electronics and ECCE Asia (ICPE 2023 - ECCE Asia)*, 2023, pp. 1912–1918.

C4. **R. P. Barcelos** and D. Dujic, "Parallel Operation of Direct Current Transformers," in *PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2023, pp. 1–10.

C5. **R. P. Barcelos** and D. Dujic, "Nodal Impedance Assessment in DC Power Distribution Networks," in *2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL)*, 2021, pp. 1–8.

Tutorials [58], [59]:

T1. D. Dujic and **R. P. Barcelos**, "Direct Current Transformer for MVDC Applications," *TUTORIAL at: 17th Brazilian Power Electronics Conference and 8th Southern Power Electronics Conference (COBEP/SPEC 2023), Florianopolis, Brazil, November, 26-29,* 2023.

T2. D. Dujic, J. Kucka, G. Ulissi, N. Djekanovic, and **R. Barcelos**, "Bulk DC-DC Conversion for MVDC Applications," *TUTORIAL at: EPE'22 ECCE Europe, European Conference on Power Electronics and Applications, Hannover, Germany, September, 5-9*, 2022.

Other publications [60]–[62]:

O1. D. Dujic, A. Cervone, **R. P. Barcelos**, J. Mace, and M. Dupont, "Learning with your PETS," *IEEE Power Electronics Magazine*, vol. 10, no. 4, pp. 53–61, 2023.

O2. J. Mace, **R. P. Barcelos**, M. Dupont, A. Cervone, and D. Dujic, "Dynamics Analysis for DC Transformers Integration in Hybrid AC-DC Power Distribution Networks," *IET Power Electronics*, vol. 16, no. 13, pp. 2215–2227, 2023.

O3. J. Mace, **R. P. Barcelos**, M. Dupont, A. Cervone, and D. Dujic, "DC Transformer Impact on Voltage Dynamics in Hybrid AC-DC power Distribution Networks," in *PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2023, pp. 1–10.

2

Modeling and Operating Principles of the Direct Current Transformer

This chapter covers the operating principles of the LLC converter. The LLC converter is well-known for its high efficiency and variable-frequency operation. Further, due to its behavior when operating around the resonant frequency, this converter can act as a DCT for DC systems. Important models and design guidelines are derived and described in detail. All the other chapters, addressing specific applications and operations of DCT, rely on the modeling framework presented here.

2.1 Introduction

The LLC converter is part of the resonant converters family. These DC-DC converters utilize a resonant circuit excited by square waves for power conversion. The most common resonant converters are: Series Resonant Converter (SRC), Parallel Resonant Converter (PRC), LLC, and LCC converters. Some examples of isolated versions for resonant converters are shown in **Fig. 2.1**.

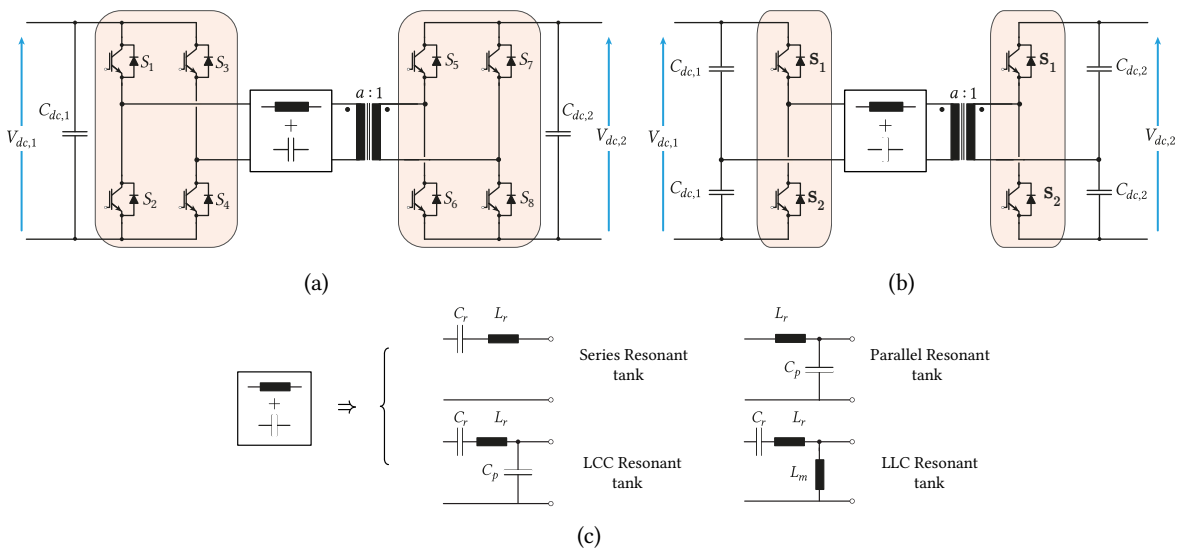


Fig. 2.1 (a) Resonant topology with Full-Bridge (FB) power stage, where the voltage applied to the resonant tank varies between $-V_{dc}$ and V_{dc}. (b) Resonant topology with split capacitor Half-Bridge (HB) power stage, where the voltage varies between $-V_{dc}/2$ and $V_{dc}/2$, (c) The most common resonant tank structure creating the SRC, PRC, LCC, and LLC type of converters.

In addition to the circuits shown in **Fig. 2.1**, there are other similar circuits with different power stages, different connections, and non-isolated versions. Diverse variations also exist on the resonant tank, for instance, using more elements for the resonance, and using the DC link capacitor for the resonant circuit, among other variations. In general, these converters stand out for their wide input operating voltage range, reduced size, and high efficiency [63].

The SRC and PRC are called single resonance converters. The SRC can operate similarly to a buck converter and the PRC can operate similarly to a buck-boost converter. The PRC is usually used for applications where the load does not vary much [64]. This converter is extremely load-dependent for operating frequencies close to the resonant frequency and has poor partial-load efficiency. The SRC has no problem with the operation with low load, and its behavior around the switching frequency can be load-independent to some extent [65].

On the other hand, multi-resonant converters such as LLC and LCC were derived from the previously mentioned converters to improve their range of operation. The LCC converter includes a second capacitor in series with the resonant tank. This converter creates a load-independent region around the main resonant frequency ($\omega_r = 1/\sqrt{C_r L_r}$), however, the impedance of the resonant tank has capacitive characteristics in that region [66]. Consequently, the soft-switching is lost.

Similarly, the LLC converter is created by reducing the magnetizing inductance of the transformer. In this case, the load-independent behavior is also achieved for operating close to the resonant frequency. In this case, the impedance of the resonant tank is inductive, meaning that the current lags the voltage applied and, consequently, ensures the ZVS. More details regarding the region of operation and operating principles will be discussed in the following sections. Thus, the LLC converter stands out for featuring soft-switching and having a load-independent operating point.

On the downside, the typical method to control the converter's gain is to operate it with a variable switching frequency, which presents challenges for the designing of magnetic components such as loss management and frequency range of operation. Also, the modeling and control are considered more complex than a duty-cycle-controlled converter. Nevertheless, these drawbacks have been successfully tackled over the years and this converter is used in diverse applications nowadays.

In the range of medium and high-power converters, the LLC converter has been the subject of several research topics for many years. In the range of 10-50 kW, the LLC converter has been considered for the next-generation data centers' power supplies [67]. In the range of up to 500 kW, the most common application of the LLC is to act as an isolated front or back end in building blocks for Solid-State Transformer (SST) application [68]. For higher power ratings, the application has been restricted to the SST domain. In [69] a 1.5 MW/5 kHz multi-winding MFT was developed as a demonstrator for traction application. Also, for a similar application, a 1.2 MVA/1.75 kHz was developed in [46].

As discussed, the LLC converter has a broad application, and most of the time, for high-power applications, it is used purely to provide an isolation and voltage adaptation between the two DC ports, with no closed-loop control. Consequently, the DC transformer is created by considering this converter as the main path between two DC buses.

The next sections will describe the pertinent models for this thesis, which allow the design, sensitivity analysis, and system-level investigation of this converter in DC PDNs.

2.2 First Harmonic Approximation

The First Harmonic Approximation (FHA) is the most used equivalent circuit for the analysis of the resonant converters. This model is extremely useful for understanding the operation principles and setting design guidelines. It considers that the resonant tank is excited by the first harmonic sinusoidal waveform of the otherwise used rectangular voltage excitation. The rectifier, output filter, and load can be represented by an equivalent resistance on the primary side. **Fig. 2.2a** shows the circuit used for the FHA analysis.

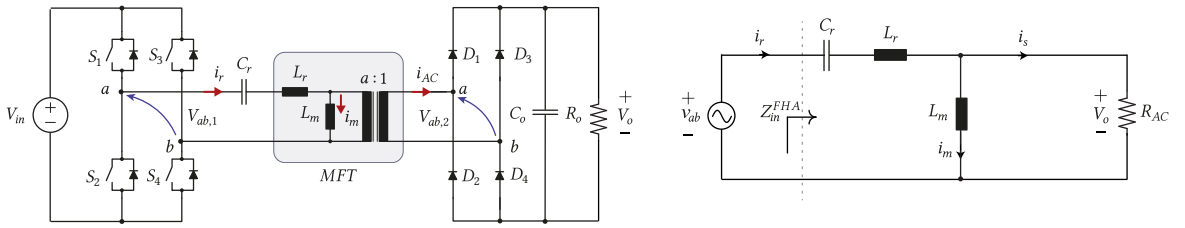


Fig. 2.2 (a) Considered LLC converter for the FHA modeling with the simplifications and considerations. (b) The FHA equivalent circuit.

From this circuit, the derivation of the FHA equivalent circuit is straightforward. Firstly, it is assumed only the first harmonic of the square-wave voltage, resulting in:

$$V_{\mathrm{ab},1} = \frac{4V_{\mathrm{in}}}{\pi} \sin\left(\omega_{\mathrm{s}} t\right). \tag{2.1}$$

Hence, this voltage excites the resonant tank, which assumed to be purely sinusoidal, generates a current in the secondary of the transformer as follows:

$$i_{\mathrm{AC}} = \sqrt{2} I_{\mathrm{AC}} \sin\left(\omega_{\mathrm{s}} t\right), \tag{2.2}$$

where I_{AC} is the RMS value of the resonant tank current of the rectifier side. Assuming that the load current is purely DC, the average output current is:

$$I_o = \frac{1}{2\pi} \int_0^{\pi} i_{AC} dt = \frac{2\sqrt{2}}{\pi} I_{AC}. \tag{2.3}$$

Now, the power dissipation on the load resistor (R_o) is modeled as a resistor (R_{AC}) with the same power dissipation, i.e. $P_{AC} = P_o$. The equivalent resistor R_{AC} is a representation of the rectifier and the DC load. For the full bridge rectifier, and with the turns ratio $a = N_p/N_s$, it yields,

$$P_{AC} = P_o \rightarrow R_{AC} I_{AC}^2 = a^2 R_o {I_o}^2 \rightarrow R_{AC} I_{AC}^2 = a^2 R_o \left(\frac{2\sqrt{2}}{\pi} I_{AC}\right)^2 \rightarrow R_{AC} = a^2 \frac{8}{\pi^2} R_o. \tag{2.4}$$

The resulting circuit is shown in **Fig. 2.2b**. Other two parameters are often defined and used for analysis: i) The natural impedance of the resonant tank, given by (2.5), is the impedance of the resonant tank during the power transferring period, and ii) the quality factor, given by (2.6), which relates the natural impedance and the load, meaning that low values correspond to low loading, and for high values, high loading.

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{2.5}$$

$$Q = \frac{Z_r}{R_{AC}} \tag{2.6}$$

The LLC converter exhibits two resonant frequencies. The first occurs when the converter is actively transferring power to the secondary. During this period, the magnetizing inductance is clamped by the reflected output voltage through the transformer and does not actively contribute to the circuit. The second resonant frequency occurs during the discontinuous period when the power stage operates with a switching frequency $f_s < f_r$, and the magnetizing inductance is included in the circuit. These resonant frequencies are defined as:

$$f_{\mathrm{r}} = \frac{1}{2\pi\sqrt{L_{\mathrm{r}}C_{\mathrm{r}}}} \qquad \text{and} \qquad f_{\mathrm{r}}^{dcm} = \frac{1}{2\pi\sqrt{\left(L_{\mathrm{r}} + L_m\right)C_{\mathrm{r}}}} \tag{2.7}$$

Now, the transfer characteristics of the LLC converter can be derived by analyzing the circuit of **Fig. 2.2b**.

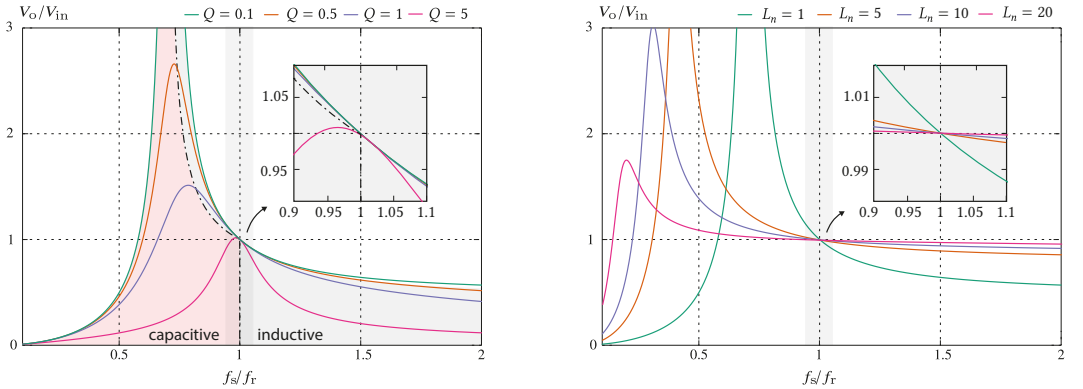
$$\frac{V_o}{V_{in}} = \frac{R_{AC} \| Z_{Lm}}{Z_{Cr} + Z_{Lr} + R_{AC} \| Z_{Lm}} \tag{2.8}$$

This equation can be normalized using the quality factor, inductance ratio ($L_n = L_m/L_r$) and frequency ratio ($\omega_n = \omega_s/\omega_r$), resulting in:

$$\frac{V_{\mathrm{o}}}{V_{in}} = \frac{L_n\omega_n^2}{\sqrt{\left(\omega_n^2\left(L_n+1\right)-1\right)^2 + \left(\omega_n L_n Q\left(\omega_n^2-1\right)\right)^2}}. \tag{2.9}$$

Thus, (2.9) is the transfer characteristic of the LLC converter as a function of the switching frequency and maps the effect of the resonant parameters and load (i.e. quality factor). **Fig. 2.3** shows transfer characteristics for different values of quality factor and different inductance ratios.

Fig. 2.3a shows the effect of the quality factor on the curve characteristics. Essentially, the quality factor shows the effect of the load on the converter's characteristics, wherein to maintain the same



(a) $L_n = 1$ (b) $Q = 0.1$

Fig. 2.3 Transfer characteristics of LLC converter using (2.8) with $a = 1$. (a) Impact of different quality factors, by changing the load value. (b) Impact of the inductance ratio, by changing the magnetizing inductance value. The zoom-in shows the behavior around the switching frequency of the LLC converter.

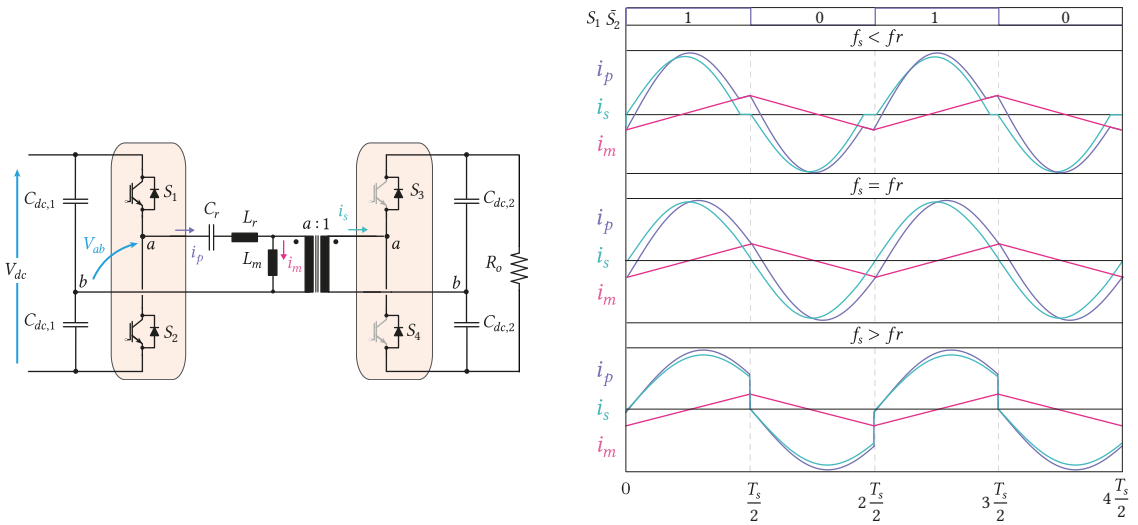
V_o/V_{in} behavior, the switching frequency needs to vary over a wider range if the variation of quality factor is also big. Further, in this figure, the dash-dotted line represents the limit between the capacitive and inductive regions of operation, obtained by the input impedance Z_{in}^{FHA}. For the case where the converter operates in the inductive region, the resonant tank current lags the voltage, resulting naturally in ZVS. However, if the converter operates in the capacitive region, the soft-switching is lost. In this scenario, as shown in the zoom-in details, for the case where the converter operates with a fixed frequency of $f_s/f_r = 0.95$, the converter would operate in the inductive region for $Q \leq 1$, but for $Q = 5$, the converter is in the capacitive region, losing the soft-switching.

Fig. 2.3b shows the impact of the inductance ratio on the curve characteristics. It shows the impact of the magnetizing inductance, where high values of L_m flatten the curve for the same L_r. In this sense, the gain is less sensitive to switching frequency change.

Consequently, from the previously discussed characteristics, one can conclude that for the DCT operating close to the resonant frequency, it is desired to i) Operate always in the inductive region having soft-switching features (defined by Z_{in}^{FHA}); ii) be load-independent (having low value for the quality factor at maximum load), and iii) have a stiff voltage characteristic for wide frequency range (having high value of inductance ratio.) The trade-offs and criteria used for the prototypes will elaborated in the following sections.

Thus, with the assistance of the typical LLC waveforms shown in **Fig. 2.4**, other aspects of the converter characteristics can be discussed. **Fig. 2.4a** shows the circuit under analysis and **Fig. 2.4b** shows the waveform for the switching frequency under resonance, at the resonance, and above the resonance frequency.

- **Operation under resonance**: The waveform for this case is shown on top of **Fig. 2.4b**. In this case, the switching frequency is less than the resonant frequency, hence, the switching period is longer than the resonant period. Thus, the resonance finishes within the switching period and enters into half-cycle DCM operation, where for the remaining period no power is transferred to the secondary, and only magnetizing current (reactive) is circulating in the circuit. In this



(a) (b)

Fig. 2.4 (a) Exemplary circuit for the current waveform illustration with measurements references. (b) Illustration of the main waveform for the operation of the power stage under, at, and above the switching frequency from the top to the bottom.

case, the ZVS of the primary switches is guaranteed and the turn-off current is defined by the magnetizing current. Yet, as this current is often designed to be several times lower than the RMS current during nominal operation, it can be considered Quasi-Zero Current Switching (QZCS). Also, extra conduction losses of the anti-parallel diode appear, and the secondary side is soft-switched and features ZCS at both turn-on and turn-off.

- **Operation at the resonance**: This operation mode is hard to achieve due to parameter variation and natural imperfections. In this case, the resonant current becomes equal to the magnetizing current at the same instant the transition occurs. This leads to the ZVS and QZCS of the primary switches and the secondary side has an idealized transition of the diodes transferring current to the load. In theory, this case is the most efficient operating point where the current in the resonant tank is purely sinusoidal, and all the possible soft-switching conditions are met.

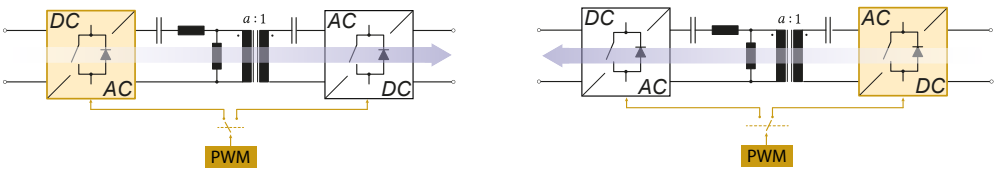
- **Operation above resonance**: For the operation above the resonance, the ZVS on the primary side is guaranteed, however, the turn-off current is higher than the magnetizing current, leading to higher losses on the primary switches. Similarly, on the secondary side, the diodes are not soft-switched once the switching instant occurs before the oscillating half-period expires.

Thus, from the discussed three operating points, and considering the high power application, the under-resonance operation is preferable considering the benefit of a well-defined turn-off current for any load condition. Nevertheless, the operation under resonance also brings challenges that need to be understood and properly mapped to ensure the safe operation of the power stage. These effects will be further discussed in the following section.

2.2.1 General Characteristics of LLC Resonant Converter

Knowing the converter characteristics, and basic principles of operation, the general characteristics of the LLC converter that make it attractive for the DCT application are:

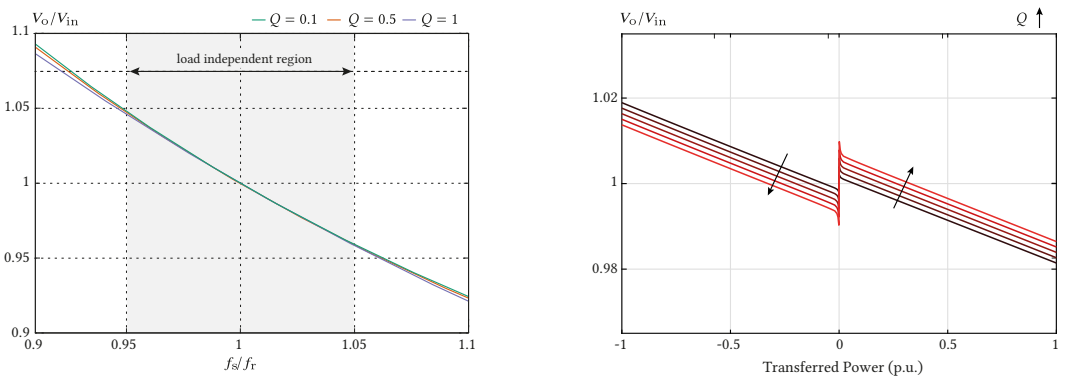
Bidirectionally: The bidirectionally is achieved by simply switching one side at a time (see **Fig. 2.5**). Each power stage can operate individually and does not require any synchronization between them.



(a) (b)

Fig. 2.5 Illustration of the bidirectional scheme with one power stage active at a time. In (a) the forward operation when the power stage of the primary side is active, and in (b) the backward operation when the secondary power stage is active.

Load independent operation: This converter provides a stiff voltage relationship between primary and secondary voltage when operating with a fixed frequency close to the resonant frequency. This feature is desired when this converter operates as a DCT, and the voltages/power of the system are controlled by other converters of the system. This is the case for most of the applications in the SST domain [70], and DC PDNs. As an example, **Fig. 2.6a** shows the transfer characteristics around the resonant frequency for different quality factors. It shows that independently of the load the converter has practically the same characteristics. Also, **Fig. 2.6b** shows another way of representing the converter's characteristics. In this case, the curve shows the power transfer characteristics for the voltage ratio at its terminals. Thus, depending on the voltage ratio the LLC operating at a fixed frequency will output a certain amount of power according to its intrinsic characteristics.



(a) $L_n = 1$ (b) $f_n = 0.9$

Fig. 2.6 (a) Converter transfer characteristics zoomed around the resonant frequency showing the load independent region for different Q. (b) Power transfer characteristics of the LLC converter operating at a fixed frequency. The Q varies from 0.05 to 0.5, simulating different resonant tank parameters, adapted from [71].

Isolation and voltage adaptation: A MFT is used for isolation and voltage adaptation purposes. The voltage adaptation is an important feature to enable the connection of technologies with different voltage levels to the same main DC backbone. The isolation is important to isolate the two systems for safety reasons. For instance, if the two systems have two different grounds, the system needs to have galvanic isolation to avoid the wrong return path for undesired currents. Both cases are illustrated in **Fig. 2.7**

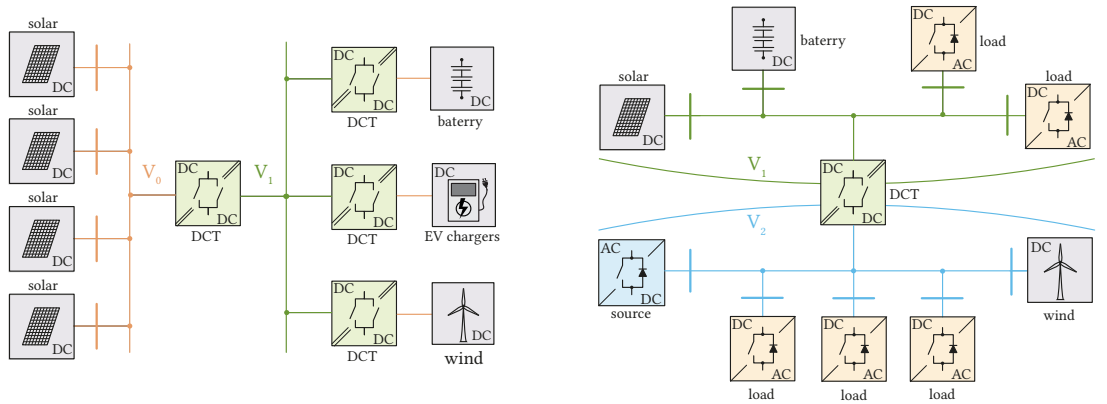


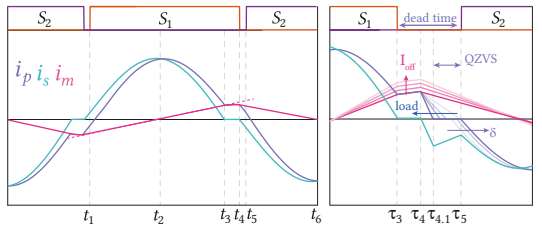
Fig. 2.7 (a) The use of DCTs to integrate other technologies into the main distribution system. (b) A power distribution network with one DCT interconnecting two different buses. An isolation and voltage adaptation is needed for both operability and safety reasons.

Soft Switching: The soft-switching feature was briefly elaborated when discussing the operating principles of the LLC in the previous section. Clearly, soft-switching is not an exclusive feature of the LLC converter and many converters can have it. The following discussion shows the step-by-step operating states of the LLC converter, and how the soft-switching is achieved. **Fig. 2.8** shows the detailed operating stages with the turn-on and turn-off transient for the positive half-cycle period and the under-resonant switching frequency. The operating stages are described as follows:

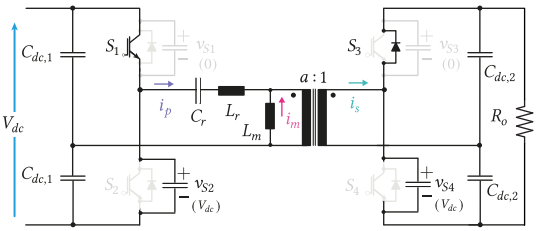
(a) The switching pulses ($S1$ and $S2$), dead-time (δ), the resonant currents of the primary and secondary (i_p and i_s), and the magnetizing current (i_m) are shown. The highlighted time instants exemplify the turn OFF of S_1 and turn ON of S_2. On the right side the behavior when the LLC features ZVS. On the left side the case when the transition happens with the loss of ZVS, and the time instants are market with τ.

(b) Represents the first operating state with the S_1 ON and S_2 OFF. In this example, this period consists of power transferring to the secondary side with both primary and secondary current positive, while the magnetizing is negative until t_2. The arrows the direction of the current or voltage at each period.

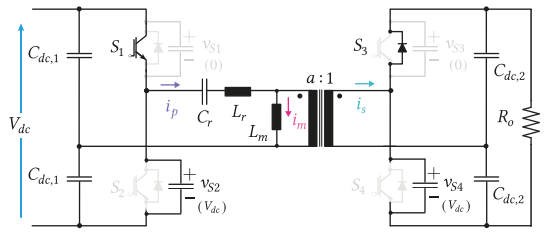
(c) After reaching t_2, the magnetizing current changes polarity, and the power is still been transferred to the secondary. No other changes happen during this period.



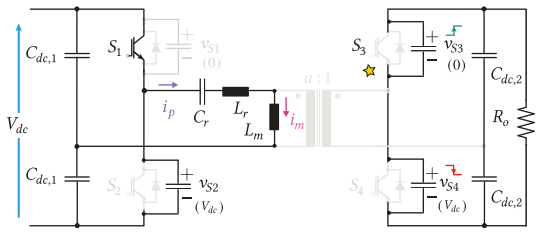
(a)



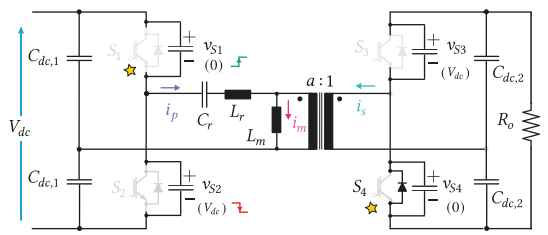
(b) $t_1 \rightarrow t_2$



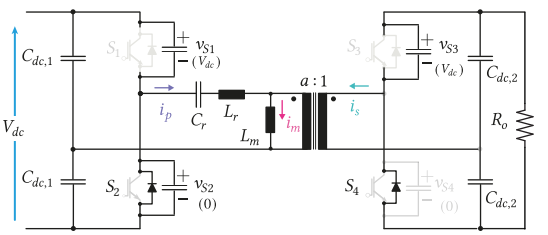
(c) $t_2 \rightarrow t_3$



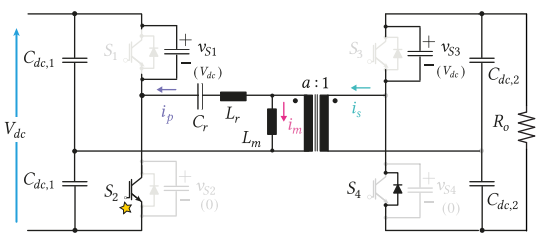
(d) $t_3 \rightarrow t_4$



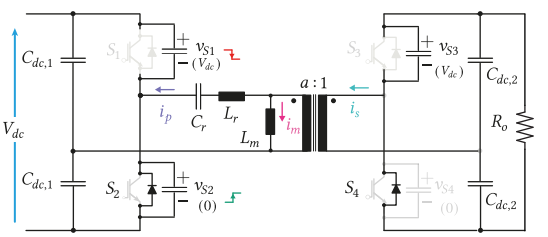
(e) $t_4 \rightarrow t_5$ (I)



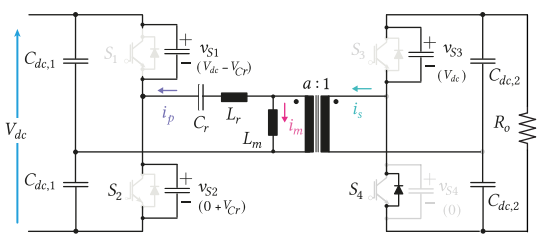
(f) $t_4 \rightarrow t_5$ (II)



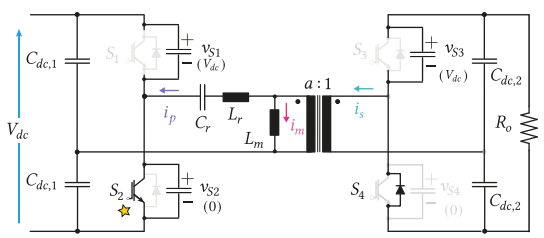
(g) $t_5 \rightarrow t_6$



(h) $\tau_4 \rightarrow \tau_{4.1}$



(i) $\tau_{4.1} \rightarrow \tau_5$



(j) $\tau_5 \rightarrow t_6$

Fig. 2.8 Operating stages of the LLC converter with $f_s < f_r$. (a-g) Show the different configurations for the positive half-cycle. (h-j) show the different configuration for the case with loss of ZVS.

(d) The resonance has finished before the switching period and the power transferring to the secondary has stopped. At this moment the primary current becomes the magnetizing current and S_1 is ready to turn OFF with QZCS. The current follows the resonant tank circuit including the magnetizing inductance, leading to a different current behavior. On the secondary side, the anti-parallel diode of S_3 has turned OFF with ZCS as the secondary current has been gradually and softly driven towards zero, and the output capacitor starts to charge. The yellow stars represent a commutation.

(e) In this period, S_1 has successfully turned OFF and the output capacitor starts to charge. This happens within the dead-time period. During this time, the output capacitor of S_2 needs to be completely discharged so that the anti-parallell diode can be forward biased and ensure ZVS. On the secondary side, the output capacitor of switch S_3 has completely charged, and the anti-parallel diode of S_4 became forward biased and started gradually increasing its current from zero, featuring ZCS.

(f) At t_5, the anti-parallel diode of S_2 is forward biased and the switch S_2 is ready to turn ON with ZVS. At this stage, if the primary current has not changed its sign, the anti-parallel diode of S_2 will continue to conduct current until the signal for turning the switch on is active. The secondary side remains the same as the previous state.

(g) The switch S_2 is successfully turned ON with ZVS, and the negative half-cycle starts. The secondary side remains the same as the previous state, and the same process starts over for the opposite switches.

(h) Starting at τ_4, which is a special case following (f), the secondary current has brought the primary current to zero before the dead time is over. In this case the current changed its polarity within the dead time, and the current starts charging the output capacitor of S_2 once again. At this point, if the switching pulse turns switch S_2 ON, the switch will feature QZVS.

(i) At $\tau_{4.1}$, the voltage of the output capacitor of S_2 is equal to the voltage at the terminals of the resonant capacitor, and the secondary current starts to decrease, due to the reflected magnetizing current. The resonant capacitor voltage is typically several times smaller than the DC-link voltage. For that reason, the QZVS can be assumed as the losses are still minimal.

(j) The switch S_2 is turned ON with QZVS, and the negative half-cycle starts. The loss of ZVS was caused by the change of polarity of the primary current before the switch S_2 is turned ON. Several aspects affect this transient and they are highlighted on the right plot of (a). The increase of the load current anticipates the change of polarity of the current. The increase of the turn-off current provides a higher starting point for the current to reach zero, which postpones the loss of ZVS. Lastly, to mitigate the QZVS, shorter dead time could be used to anticipate the turning ON of switch S_2.

These basic characteristics and operating principles are especially attractive for the DCT, and this will guide the design specifications for the LLC converter.

2.3 Design Guidelines

The design guidelines presented here use the simplifications of the FHA circuit, which can provide approximated values useful for prototype construction, but not for optimized designs. Also, depend-

ing on the application and the used power switches, different methodologies can be found in the literature [71]–[74].

For the design of the LLC converter for the DCT application, some important objectives need to be met: i) Load-independent behavior (definition of maximum quality factor); ii) Desired resonant frequency (definition based on the power switches and desired operating switching frequency.); and iii) Desired magnetizing inductance for the turn-off current (a compromise between ZVS and QZCS.)

2.3.1 Resonant Tank Parameters

The resonant parameters consist of the series resonant inductance and the series resonant capacitor. The resonant inductance can be integrated into the MFT, if previously set as a desired leakage inductance during the MFT design, together with the magnetizing inductance. The resonant capacitor is added externally.

These two elements determine the resonant frequency of the converter and represent the resonant tank's natural impedance, consequently, they impact the quality factor. Hence, after relating all these criteria their value can be computed.

Firstly, it is desired to have a load-independent behavior feature, thus, the maximum value for the quality factor needs to be defined. The quality factor depends on the resonant parameters and the load, and the value can be chosen by the desired curve characteristics for the maximum loading. Thus, the first equation can be written as:

$$Q^*_{max} = \frac{Z_r}{a^2 \frac{8}{\pi^2} \frac{Vo^2}{P_n^{max}}} \tag{2.10}$$

where, P_n^{max} is the maximum power at which the converter will operate, which leads to maximum quality factor.

Secondly, it is desired to operate the power stages close to the resonant frequency, in particular, below the resonant frequency to take advantage of the well-defined turn-off current. Thus, combining the switching frequency and resonant frequency, a second equation can be written as:

$$f_s^* < f_r^* = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2.11}$$

2.3.2 Magnetizing Inductance

The design of the magnetizing inductance is a critical factor for the LLC converter, particularly when operating at $f_s < f_r$. This inductance determines the turn-off current of the switches, which, in turn, dictates the rate of discharge for the output capacitors. The current flowing through the magnetizing inductor is directly related to the voltage applied to the inductor over the switching period. During the discontinuous period, the peak current can be estimated by:

$$\hat{I}_m = \frac{V_{in} T_s}{4 L_m} \tag{2.12}$$

One approach to calculating the magnetizing inductance is by choosing a desired turn-off current that satisfies the loss budget for the power switches. The losses are then limited if QZCS and ZVS conditions are fulfilled. In this case, the equation is given by (2.12), replacing the peak current for a desired turn-off current (I_{off}), resulting in:

$$L_m < \frac{V_{in}}{4 f_s I_{off}}. \tag{2.13}$$

Ensuring ZVS not only requires the magnetizing current to be sufficient for discharging the output capacitance of the switches but also demands that the current maintains the same polarity throughout the dead time. If the current changes polarity, it recharges the output capacitance and the ZVS is lost (as discussed in **Fig. 2.8**). **Fig. 2.9** shows the typical waveforms during the dead time and a situation where the current changes polarity within the dead time.

In **Fig. 2.9**, the current behavior during the dead time is better illustrated for different load conditions. Notably, the current slope during the dead time increases with the rising load. At a certain point, the current may cross zero before the dead time is over, resulting in the loss of ZVS. Therefore, a proper converter design needs to ensure the tank current zero-crossing to the right of the switching events under all operating conditions.

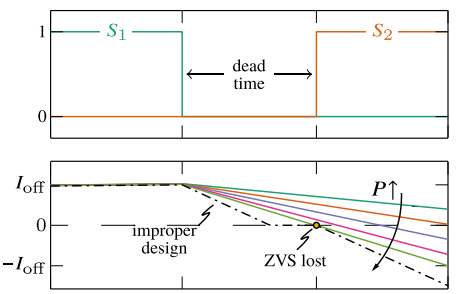


Fig. 2.9 Resonant tank current during dead-time, adapted from [59].

2.4 Other Equivalent Circuits

As previously mentioned, the most popular modeling approach for the resonant converter is based on the FHA. This model allows very simple and direct converter design rules, providing the resonant tank and voltage gain characteristics, and a good representation of the load impact in the converter characteristics. However, as only the first harmonic is considered, the current is considered to be sinusoidal, and the elements are ideal, which leads to a very approximated version of the real circuit.

Alternatively, models with more details are derived based on the DC terminal dynamics [75], time domain equations [76], model in rotational frame [77]–[79], and small signal modeling [80]–[84]. In this thesis, two other models are used. The dynamic equivalent model, which represents the DC terminals' behavior, is used for the system analysis, and the small-signal modeling is mainly used to derive control to output transfer functions. Here it is used for sensitivity analysis of the resonant tank parameters.

2.4.1 Dynamic Equivalent Model

For applications where the LLC converter is used as a DCT, the interest lies in its terminal voltage and current behavior. In this case, the DCT dynamics can be represented by a passive equivalent circuit, which is based on the converter's losses.

A generic derivation of the equivalent circuit based on the energy conservation principle is derived in [85], [86]. In this model, the losses and the amount of stored energy in the resonant circuit are equal to the losses and stored energy of the equivalent circuit. With this assumption, the DCT can be represented as shown in **Fig. 2.10a**.

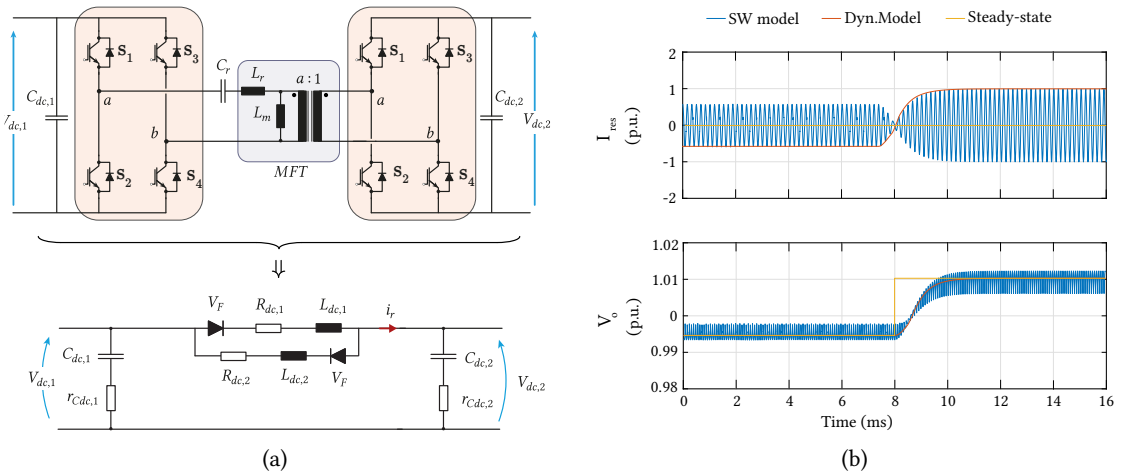


Fig. 2.10 (a) Dynamic Equivalent model, adapted from [85], with different values for forward and backward operation considering possible unbalances. (b) Simulation waveform of voltage and current of an exemplary DCT using data provided in **Chap. 6**, and the model representation response, with the switching model, the dynamic equivalent model, and the steady-state response with only R_{dc}.

The equivalent circuit is defined by the local average of the resonant current (over half a switching period), $\bar{i}_{\mathrm{R}}$, and the RMS current $\tilde{i}_{\mathrm{R}}$. The equivalent voltage drop V_F represents all the semiconductors' voltage drops in the current path. The capacitors at each side have the same value as the switched circuit. R_{dc} represents the load-dependent losses of the complete converter, with R_{total} as the total series resistance in the current path, thus,

$$\tilde{i}_{\mathrm{R}}^2 R_{\mathrm{dc}} \stackrel{!}{=} \tilde{i}_{\mathrm{R}}^2 R_{\mathrm{total}} \Rightarrow R_{\mathrm{dc}} = \beta^2 R_{\mathrm{total}} \quad \text{with} \quad \beta^2 := \frac{\tilde{i}_{\mathrm{R}}^2}{\bar{i}_{\mathrm{R}}^2}. \tag{2.14}$$

Also, the parasitic series resistance of the DC-link capacitors can be included to R_{dc} as shown in (2.15).

$$R_{\mathrm{dc}} = \beta^2 R_{\mathrm{total}} + \left(\beta^2 - 1\right)\left(r_{c1} + r'_{c2}\right) \tag{2.15}$$

where r_{c1} and r'_{c2} are the equivalent series resistance of the DC-link capacitor from the primary and the secondary reflected primary, respectively.

The equivalent L_{dc} is defined by the stored energy in the resonant tank, according to

$$E_{\text{stored}} = \frac{1}{2} L_r \hat{i}_{\text{R}}^2 \quad \text{with} \quad \hat{i}_{\text{R}} = f(P). \tag{2.16}$$

where $\hat{i}$, is the peak resonant tank current which is power-dependent. Thus,

$$\tilde{i}_{\text{R}}^2 L_{\text{dc}} \stackrel{!}{=} \hat{i}_{\text{R}}^2 L_r \Rightarrow L_{\text{dc}} = \alpha^2 L_r \quad \text{with} \quad \alpha^2 := \frac{\hat{i}_{\text{R}}^2}{\tilde{i}_{\text{R}}^2}. \tag{2.17}$$

In particular, in the case of the piecewise sinusoidal current, α and β can be simply found by:

$$\alpha = \frac{\pi}{2} \frac{f_r}{f_{\text{s}}} \quad \text{and} \quad \beta = \frac{\pi}{2\sqrt{2}} \sqrt{\frac{f_r}{f_{\text{s}}}}, \tag{2.18}$$

otherwise, the coefficients are calculated by (2.19) using the data from experiments or simulation.

$$\alpha := \frac{\hat{i}_{\text{R}}}{\tilde{i}_{\text{R}}} \quad \text{and} \quad \beta := \frac{\tilde{i}_{\text{R}}}{\tilde{i}_{\text{R}}} \tag{2.19}$$

Therefore, this model represents the DC terminal's behavior, good for system-level studies. Furthermore, the information of the R_{dc} can be used to precisely set threshold values for the open loop operation. As an example, **Fig. 2.10b** shows a simulation of the switching converter and the model representation. In this thesis, this model is used in **Chap. 3**, **Chap. 6**, and **Chap. 7**.

2.4.2 Small Signal Modeling

The small signal modeling is usually used for control purposes. Some of the control techniques of the LLC converter are based on the resonant capacitor charge control [87], hysteresis current [88], and voltage control [89], among others. The most common approach for deriving the small signal model is based on the extended describing function method [90], and several works have improved, simplified, and used this method for deriving transfer functions and having a circuit for simulation.

An equivalent small signal model for the LLC converter using a third-order equivalent circuit was derived in [91]. In this model, analytical solutions for all the transfer functions were described, which can be very helpful for control, sensitivity analysis, and design.

In short, to create the small signal model, firstly the circuit is separated for the operation of $f_s \geq f_r$ and $f_s < f_r$. After that, for each operating stage, a new equivalent circuit is created which repeats every half period, as shown in **Fig. 2.8** for the $f_s < f_r$ case. Thus, the model can be described as the steady-state model shown in **Fig. 2.11a**. From this circuit, the small signal model can be derived and it is represented by **Fig. 2.11b**. Now in order to create a unified equivalent circuit model valid for

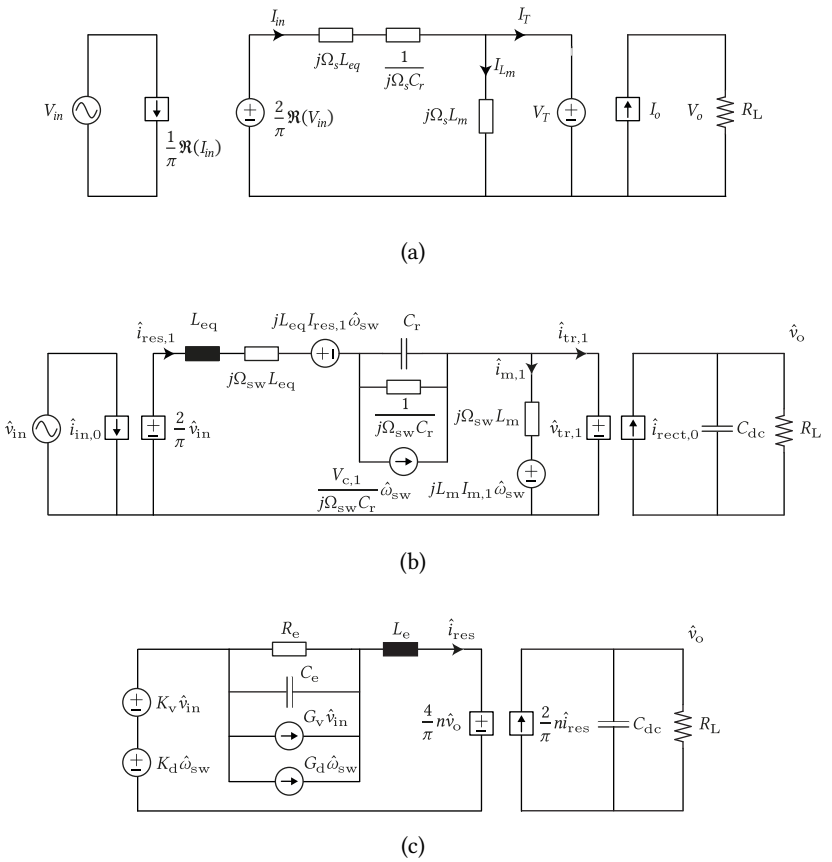


Fig. 2.11 (a) Steady-state model of LLC $f_s < f_r$ (b) Small-signal model for $f_s < f_r$. (c) Unified equivalent circuit model for $f_s \geq f_r$ and $f_s < f_r$, adapted from [91].

both $f_s \geq f_r$ and $f_s < f_r$, the resultant circuit is shown in **Fig. 2.11c**. Simplifications, assumptions, and details on the parameters can be found in [92].

The interesting aspect of this model for this thesis is the representation of the resonant parameters for the calculation of the input impedance. With this model, the input impedance can be described by (2.20), where L_e, R_{eq}, and X_{eq} are presented in (2.21).

$$Z_{in}(s) = \begin{cases} \frac{\pi^2}{2}\left(sL_e + \frac{\frac{8a^2}{\pi^2}R_L}{R_L C_{dc} s + 1}\right), & \text{for } \omega_s < \omega_r \\ \frac{\pi^2}{2}\frac{\left(s^2\ L_e^2 + sL_eR_{eq} + X_{eq}^2\right)(1 + R_L C_{dc} s) + R_{eq}\left(sL_e + R_{eq}\right)}{s^2\ L_e C_{dc} R_L + sL_e + sC_{dc}R_L\frac{R_{eq}^3}{R_{eq}^2 + X_{eq}^2} + R_{eq}}, & \text{for } \omega_s \geq \omega_r \end{cases} \tag{2.20}$$

$$
\begin{aligned}
L_e &= \begin{cases} \left(1+\frac{1}{\omega_n^2}\right) L_r & \text{for } \omega_n \geq 1 \\ \left(1+\frac{1}{\omega_n^2}\right) L_r + (1-\omega_n)\, L_m & \text{for } \omega_n < 1 \end{cases} \\
R_{eq} &= \frac{8}{\pi^2} n^2 R_L \\
X_{eq} &= \omega_s L_r - \frac{1}{\omega_s C_r}
\end{aligned}
\tag{2.21}
$$

This equation allows a better representation of the input impedance compared to the FHA including the output capacitor, the impact of the magnetizing inductance, and a better representation of operating frequencies away from the resonant frequency. The input impedance from the small signal modeling is used for sensitivity analysis in **Chap. 5**.

2.5 Resonant DC Transformer

Taking advantage of the open-loop behavior of the LLC converter operating close to the resonant frequency, this converter can act as a transformer for the DC systems. The lack of closed-loop control, makes the DCT be driven by the natural power flow of the DC PDN, which is beneficial for the system's dynamic and stability [52], [93], [94]. Consequently, the open-loop operation of the DCT reduces the complexity of the system, by not forcing any set points on its nodes. This behavior is similar to AC systems, where the voltages at each port are controlled by other equipment depending on the bus loading.

The purpose of the DCT in DC PDN is to be the energy router for different DC buses. **Fig. 2.12** shows a simple example of two DC buses with two converters connected to each, and the DCT is included to interconnect both systems. After the inclusion, the DCT will assist the sources to feed the load by transferring power from one bus to another, following the voltage dynamics, which depends on the load behavior and the capability of the source to regulate the voltage.

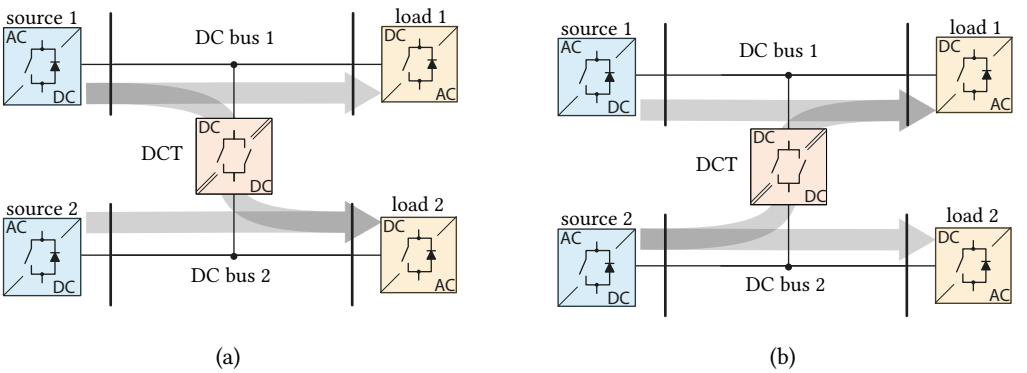


Fig. 2.12 Illustration of the DCT in a DC PDN system for routing power according to system's demand. In (a) the power flow from DC bus 1 to DC bus 2, and (b) the power flow from DC bus 2 to DC bus 1.

In these systems, the DCT does not impose any operational point. Yet, although the DCT does not have the over-current capability of an AC transformer, it can support briefly a faulted current, and

act as a protection device, disconnecting the faulted bus from the system [95], adding some extra features for the grid support.

Nevertheless, to support the DCT's operation principles, some open-loop strategies need to be implemented. The goal of such strategies is to assist in a reliable operation of the DCT in DC PDNs, and they need to be fine-tuned and adjusted based on the converter characteristics. For that reason, the essential strategies and features of the DCT are investigated in the next chapter.

2.6 Summary and Conclusion

This chapter described the basic principles of the LLC converter, with relevant models for the thesis. Although the complete derivation of the models was not described, all the required information for the following developments is present. Both FHA, the Dynamic Equivalent model, and the small signal model were developed by other works and are considered state-of-the-art for the LLC converter.

The FHA is the most important model for understanding the principle of resonant conversion. This model leads to a simple transfer characteristics equation, which allows mapping the effect of the switching frequency on the voltage gain and design rules for the resonant tank parameters.

The Dynamic Equivalent Model represents the DC terminals' behavior of the LLC converter operating at a fixed frequency. This model is useful when the interest lies in the DC terminals' behavior as it is for setting the threshold values for the open-loop strategies and system-level analysis of the DCT.

The small signal modeling was discussed and the input impedance parameter was described. Here, only the input impedance is used for the sensitivity analysis of the resonant parameters. One could argue that this model is too detailed for this purpose, as it was developed for other reasons. However, the representation of the input impedance by this model is accurate in a wide range of frequencies, which is required for sensitivity analysis, and justifies its use.

In the end, the operation of the DCT is based on the DC terminals' behavior of the LLC converter. Thus, a comprehensive understanding of the converter functionality is crucial for setting correctly the operation limits and dealing with the non-linearities neglected by models, but present in real prototypes. The next chapter will describe the essential features required to allow a reliable operation of the DCT.

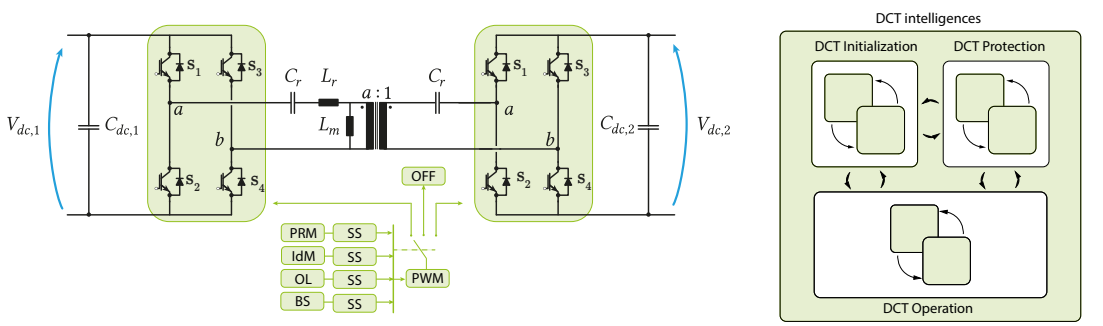
3

On Features of Direct Current Transformers

Due to its similar behavior to the AC transformer, the open loop operation of the LLC converter is what makes this topology the best fit to be the DCT in the DC PDNs. However, a few additional intelligence are required to ensure a safe operation. This chapter investigates the required control logic to enable a reliable operation of the DCTs. It focuses on the developed methods for power reversal, and the no-load operation strategy, and presents its implementation and validation with the LV DCT prototypes.

3.1 Introduction

While the DCT operates in an open loop, it requires additional intelligence for tasks such as initiation, operation, and protection. This intelligence is programmed to guide the converter throughout its operation. **Fig. 3.1a** shows the DCT based on the LLC converter explored in **Chap. 2**, with multiple logics controlling its operation, demonstrated in this chapter. Essentially, all these strategies are dedicated states of a state machine that manages the operating modes.



(a) (b)

Fig. 3.1 (a) DCT with the main features for its operation in DC PDNs, including Power Reversal Methods (PRM), Soft-start (SS), Idle Mode (IdM), Over-load protection (OL), Black-Start (BS). (b) Interconnection of the three main blocks for an autonomous operation of the DCT.

This chapter discusses three key features of the DCT that allow its basic operating principles. The first feature is the soft-start strategy, which ensures a smooth initialization of the DCT from an idle state to a steady-state. This strategy aims to protect the converter from inrush currents. The second strategy is the Power Reversal Algorithm, which determines the power transfer direction. This algorithm utilizes available sensors to identify the power direction and reverses when it is needed.

Lastly, the idle mode operation is explained as a mode designed to enhance the efficiency of the

DCT, by avoiding no-load losses. This mode also relies on available sensors to determine if power is being transferred between buses. If not, only no-load losses are present in the DCT, allowing the converter to be shut down until its operation is requested again by the system. All these strategies are extensively described and demonstrated with the prototypes developed in the laboratory.

3.2 Description of LV DCT Prototypes

Two LV prototypes were built for testing and validating the control algorithms. The DCT uses a three-phase Voltage Source Inverter (VSI) PEBB developed in the lab, with only two legs operated as FB. The power stage consists of 3×IGBT modules of 1.7 kV/300 A ($SKM400GB176D$) [96], the gate driver is ABB's GD D852A, and the power stages are controlled by ABB's AC 800PEC. **Fig. 3.2** and **Fig. 3.3** show the two LV DCTs developed for the investigations in this chapter. **Tab. 3.1** shows the specifications of the prototypes.

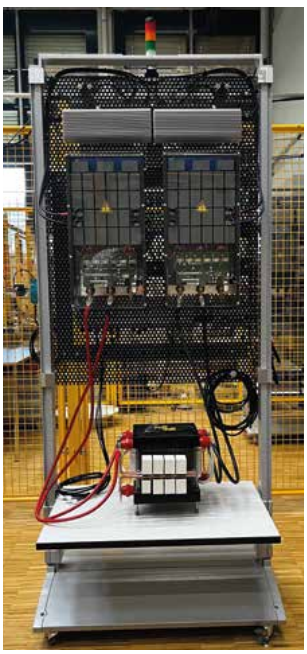


Fig. 3.2 DCT 1

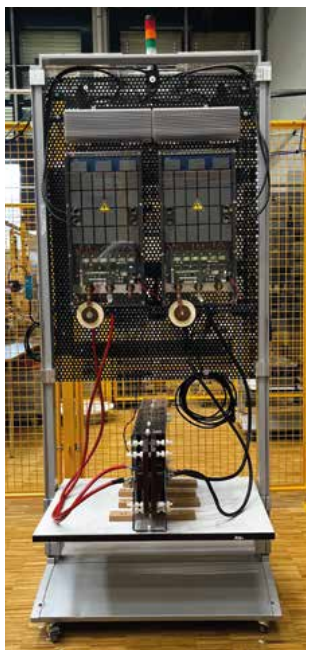


Fig. 3.3 DCT 2

Description	Symbol (Unit)	DCT
DC Voltage	V_{dc} (V)	750
Grid ind.	L_s (μH)	30
Grid res.	R_s (Ω)	0.1
Tuns ratio	$a:1$	1 : 1
DC link	C_{dc} (μF)	1020[a]
Lim. Resistor	R_{lim} (Ω)	10
Sw. frequency	f_{sw} (kHz)	10
Dead time	δ_{dt} (μs)	4
Cable res.	R_c (Ω)	0.15

[a] ± 5% tolerance

Tab. 3.1 DCTs parameters

The DCTs are constructed as symmetric LLC converters with split capacitors on each side of the MFT. The MFTs were built upon the same design specifications: 100 kW, 750 : 750 V, and 10 kHz. The first MFT shown in **Fig. 3.4**, is a core type MFT made with square litz wire, air-insulated, core of SiFerrite (UU9316 - CF139) with air-cooled heatsink, and resonant capacitors mounted closely to the MFT [97].

The second MFT shown in **Fig. 3.5**, is a planar type with windings made of the same litz wire, nano-crystalline core (VITROPERM 500F), solid insulation (cast resin), and forced air cooling, with external resonant capacitors [98], as can be seen in **Fig. 3.3**.

Both prototypes have a DC-link pre-charge circuit with a limiting resistor. The ABB's COMBI-IO equipment is used for the light tower, relays, fans, ground switch, and pre-charge resistor temperature measurement.

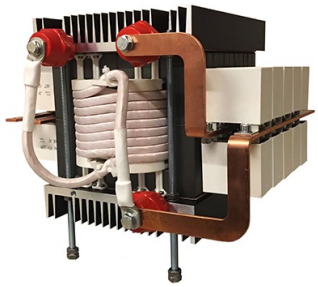


Fig. 3.4 MFT 1

Description	Symbol (Unit)	DCT
Leakage inductance	L_r (μH)	11.6
Magnetizing inductance	L_m (μH)	750
Resonant capacitor	C_r (μF)	37.5[a]
Resonant frequency	f_r (kHz)	10.8
Quality factor	Q	0.059
Inductance ratio	L_n	64.65

[a] ± 5% tolerance

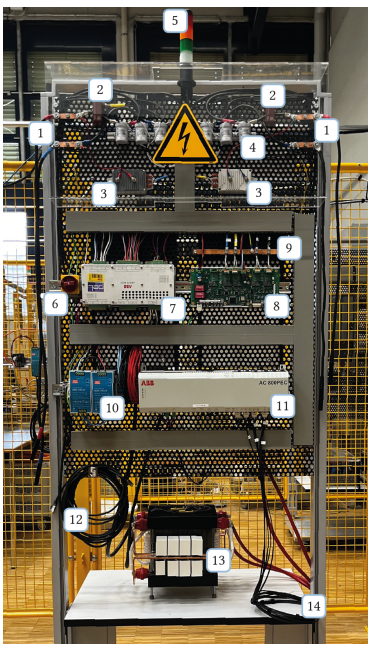
Tab. 3.2 MFT 1 parameters

Fig. 3.5 MFT 2

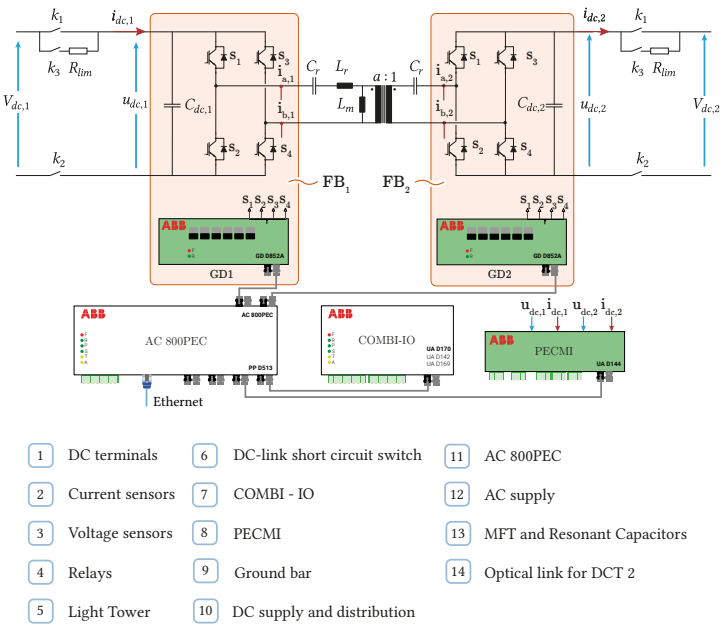
Description	Symbol (Unit)	DCT
Leakage inductance	L_r (μH)	9.5
Magnetizing inductance	L_m (μH)	1100
Resonant capacitor	C_r (μF)	37[b]
Resonant frequency	f_r (kHz)	12
Quality factor	Q	0.054
Inductance ratio	L_n	115.79

[b] ± 10% tolerance

Tab. 3.3 MFT 2 parameters



(a)



(b)

Fig. 3.6 (a) Back panel of DCT 1 showing the remaining equipment. (b) Schematic of the DCT.

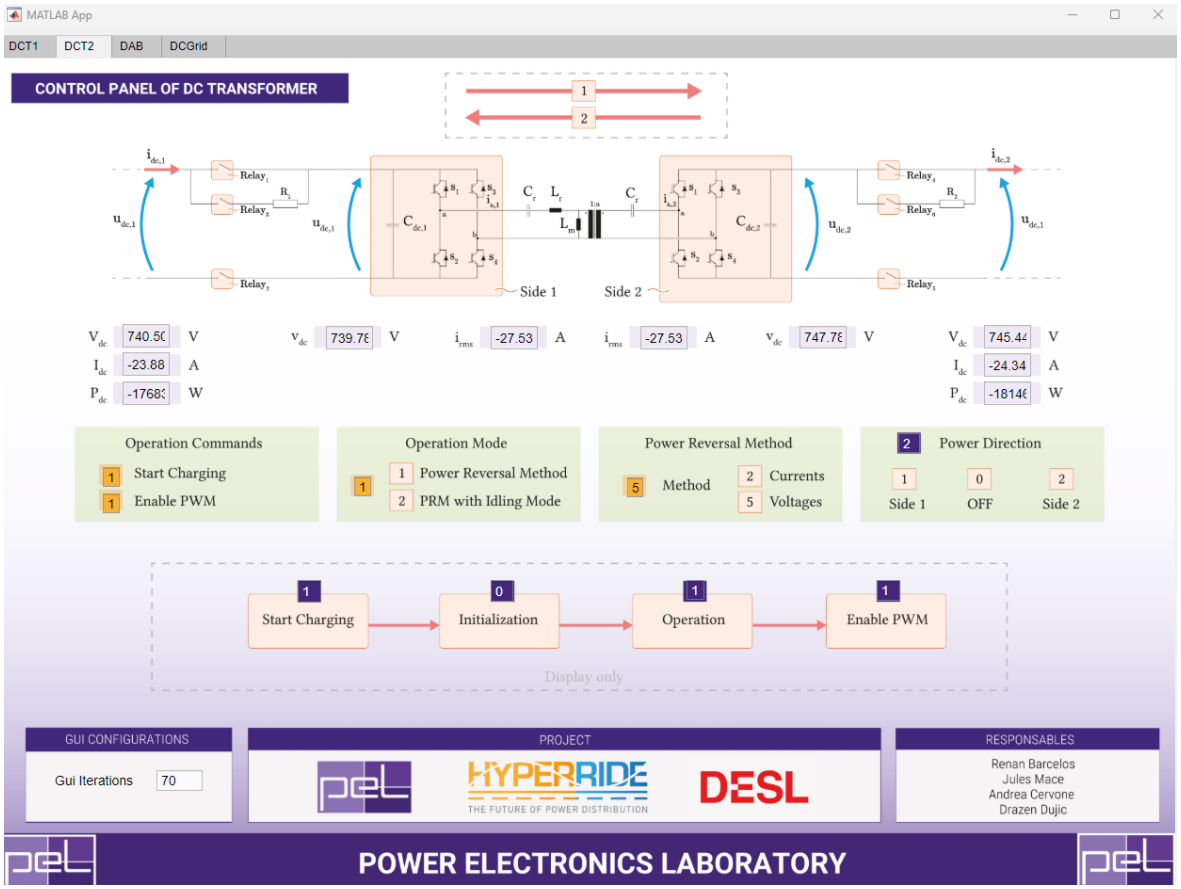


Fig. 3.7 GUI for the operation of the DCTs and visualization of important parameters developed for Hyperride project [17]. This figure shows the tab of DCT 2, with $P_{dc} \approx 18$ kW being transferred from secondary to primary (hence the negative sign).

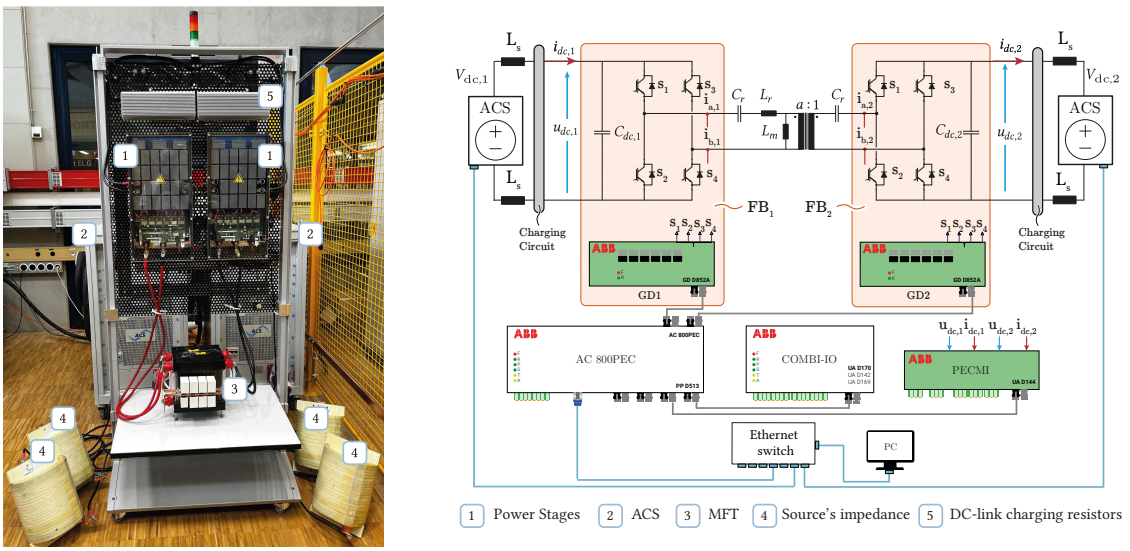
The ABB's PECMI equipment is used for reading the voltage and current measurements of the DC terminals. The DC-link voltage and resonant current are measured by the gate driver. All the signals communicate with the central controller via an optical link. **Fig. 3.6a** shows the back panel of DCT 1 with the mentioned equipment and **Fig. 3.6b** the schematic.

Also, the DCTs have a Graphic User Interface (GUI) for the visualization of important parameters via PC, and selection of desired control strategies options, as shown in **Fig. 3.7**.

3.2.1 Steady-State Operation of the DCT

Firstly, each DCT was built and tested. The testing setup and schematic are shown in **Fig. 3.8**. The DC buses are created with two switched power amplifiers - TC.ACS.50.528.72 from Regatron, where two legs of 3-phase 50 kW power rating were used, reducing the DC power ratings available for the experiments to $P_{dc} \approx 20$ kW [99]. Four inductors with their winding resistance, referred to as grid inductance and grid resistance, were employed to connect the source with the DCT **Tab. 3.1**.

The experimental setup consists of two energized DC buses connected to the DC ports of the DCT. An initial startup sequence proceeds to charge the DC-link capacitors through the charging resistors,

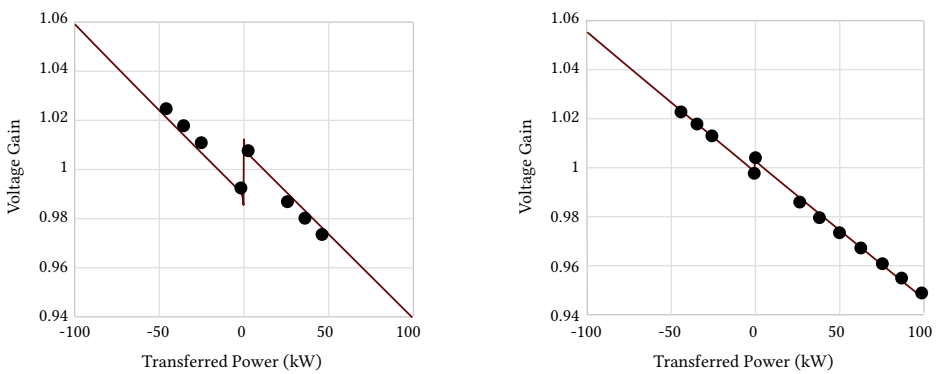


(a) (b)

Fig. 3.8 (a) Test setup with two ACS and extra inductors. (b) Schematic of the test setup with detailed measurements corresponding to the actual measurements for each waveform. For the test setup system, the controller, and power sources are accessed through the PC.

which are bypassed during operation. The DC bus 1 is regulated to $V_{DC,1} = 750$ V, while the DC bus 2 is modulated to provoke various power flows. The power flow is created by setting a voltage difference between the two DC ports. As the DCT operates in an open loop, with a fixed frequency, the power transferred is given by the voltage difference between both DC ports.

Each DCT requires a characterization to identify the power transfer characteristics, which are based on the losses of the converter. These characteristics provide information on how much power DCT will transmit according to the voltage difference of its DC terminals. In other words, the power transfer characteristic helps to identify the correspondent power for a given voltage difference.

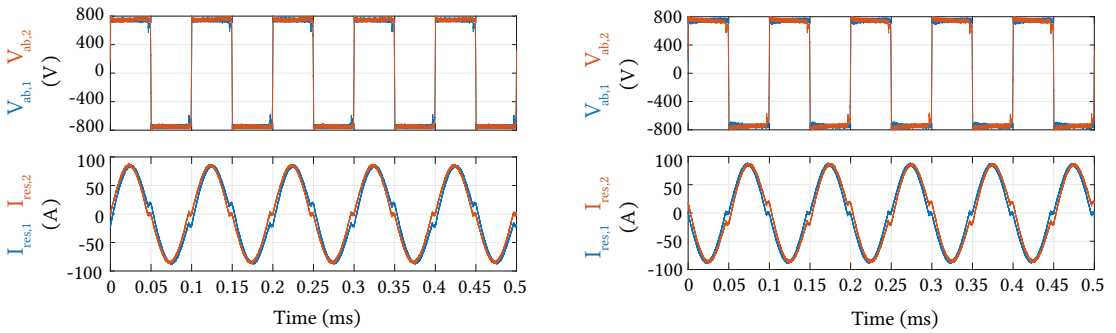


(a) DCT 1 (b) DCT 2

Fig. 3.9 Power transfer characteristic of the two DCT prototypes with experimental data. (a) DCT 1 and (b) DCT 2. The voltage gain is $V_{dc,2}/V_{dc,1} = G_v$, which leads to a positive power transfer for a forward operation.

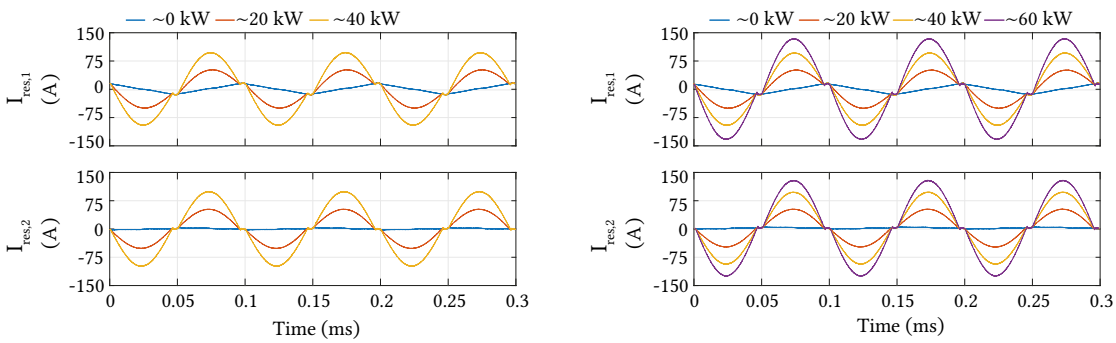
This curve can also be derived by simulations or by the dynamic equivalent model and is validated with experimental results. **Fig. 3.9** shows the power transfer characteristics of the two LV DCT prototypes. Both DCTs have similar characteristics, and it can be noticed that differences of 10 V (i.e. $G_v \approx 1.135$ and $G_v \approx 0.987$) can lead to $P_{dc} \approx \pm 25$ kW for DCT 1 and $P_{dc} \approx \pm 30$ kW for DCT 2.

Now, a voltage difference is required to provoke the desired power flow. Firstly, **Fig. 3.10** shows the steady-state operation of the DCT 1, for the forward and backward operation. In each test, the DCT 1 is processing $P_{dc} \approx 40$ kW. On top, it shows the voltage applied to the resonant tank and the secondary voltage at the power stage terminals, and on the bottom, the primary and secondary currents. As can be seen, in **Fig. 3.10a** for the forward operation, the current on the primary of the MFT (blue waveform of the bottom plot) becomes the magnetizing current before the next switching event. At this moment, the secondary is disconnected and the current is zero. Similar conclusions can be drawn for the backward operation in **Fig. 3.10b**.



(a) DCT 1 Forward Operation (b) DCT 1 Backward Operation

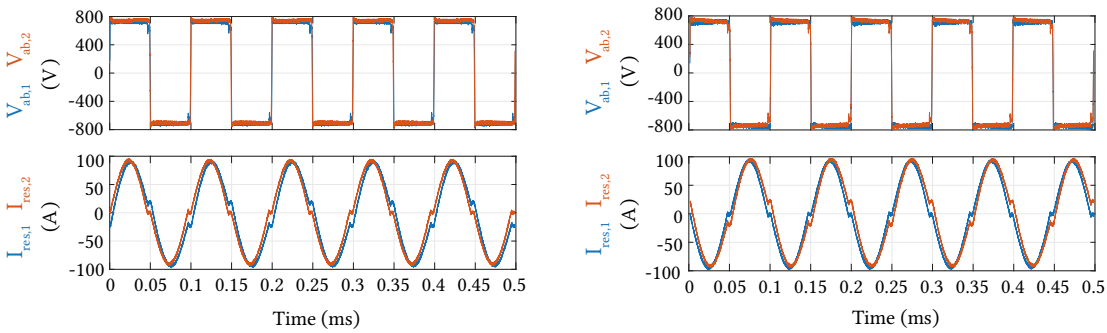
Fig. 3.10 Experimental waveforms of the voltages (on top) and resonant currents (on bottom) of the DCT 1 for forward and backward operation. In blue are the waveforms of the primary, and in orange are the waveforms of the secondary of the MFT.



(a) DCT 1 (b) DCT 2

Fig. 3.11 Experimental waveforms of the primary and secondary resonant currents for (a) DCT 1 and (b) DCT 2 at different power levels.

Fig. 3.11 shows only the primary and secondary currents, for different loads. At the no-load condition, only the magnetizing current is present as shown in blue for both graphs. In this plot, it is easy to



(a) DCT 2 Forward Operation

(b) DCT 2 Backward Operation

Fig. 3.12 Experimental waveforms of the voltages (on top) and resonant currents (on bottom) of the DCT 2 for forward and backward operation. In blue are the waveforms of the primary, and orange of the secondary of the MFT.

identify the magnetizing current, at the moment of the switching. Thus, the turn-off current of DCT 1 is $I_{off,1} \approx 22$ A and for DCT 2 is $I_{off,2} \approx 17$ A.

Lastly, **Fig. 3.12** shows the forward and backward operation of DCT 2. The DCT 2 is also processing $P_{dc} \approx 40$ kW, with only subtle differences compared to DCT 1. One can note the two small differences in the resonant current of DCT 2 which reaches a higher value of peak current, showing two characteristics: i) resonant frequency is higher than DCT 1, and ii) the losses in the resonant tank are smaller. Both tests were performed with the same voltage difference between the DC buses, $V_{dc,1} = 750$ V and $V_{dc,2} = 731$ V.

3.3 Development of the DCT Features

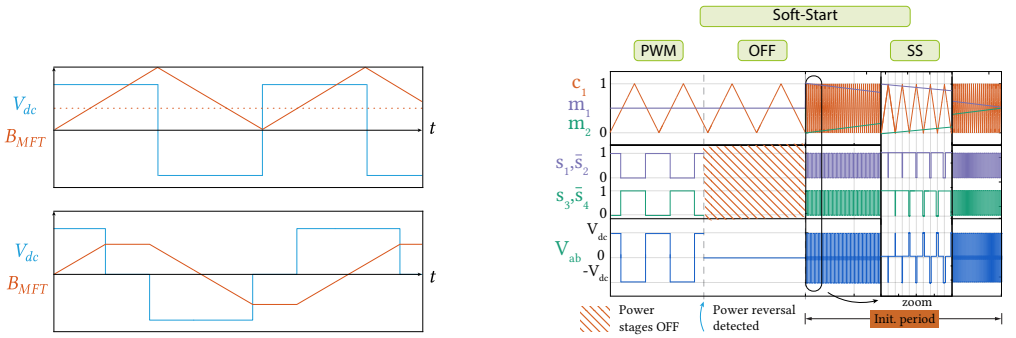
Operating the LLC converter in an open loop is not enough to ensure the full functionality of the DCT for DC PDNs. As previously mentioned, some intelligence needs to be implemented to allow its basic functionalities.

Starting with the soft-start, this feature is commonly implemented for practically every converter to protect the hardware against inrush currents. Secondly, the power reversal strategy is what determines the power direction and makes the DCT bidirectional. This logic can be implemented in numerous manners and ideally, it should be fast, simple, cheap, precise, and not cause extra disturbances to the system. Lastly, the idle mode is created to avoid unnecessary no-load losses of the DCT. This operation mode is derived especially for DC PDN where, in some cases, the DC buses can be well regulated and the DCT does not need to transfer power for long periods. Consequently, the DCT can stay idle for a long time and start its operation only when needed.

In this section, all these three features are described and experimentally demonstrated.

3.3.1 Soft-start Strategy

Whether it is the initial moment or after a reversal, the soft start takes place to ensure a smooth initialization of the DCT. Soft-start strategies for LLC converters are well-known and demonstrated in the literature. Many methods are already available [100]–[103], and here the duty cycle modulation



(a) (b)

Fig. 3.13 (a) Magnetic flux on the MFT for full 50% duty cycle starts creating a DC offset (top). Below is the waveform for a 3L waveform and the magnetic flux behavior. (b) Illustration of the soft-start strategy. The DCT operates with unipolar PWM. Firstly, modulation indices are set to 0.5 generating a square 2L waveform. Then, the PWM is disabled and the converter stops. At the moment to start again, the modulation indices are gradually increased from 0 to 50%, hence using 3L modulation until 50% duty cycle is reached and modulation is turned into 2L (no use of zero voltage state).

is used in every DCT initialization. This strategy creates a 3L waveform to the resonant tank which does not require a change of the operating frequency and achieves the two main goals of the soft-start strategy.

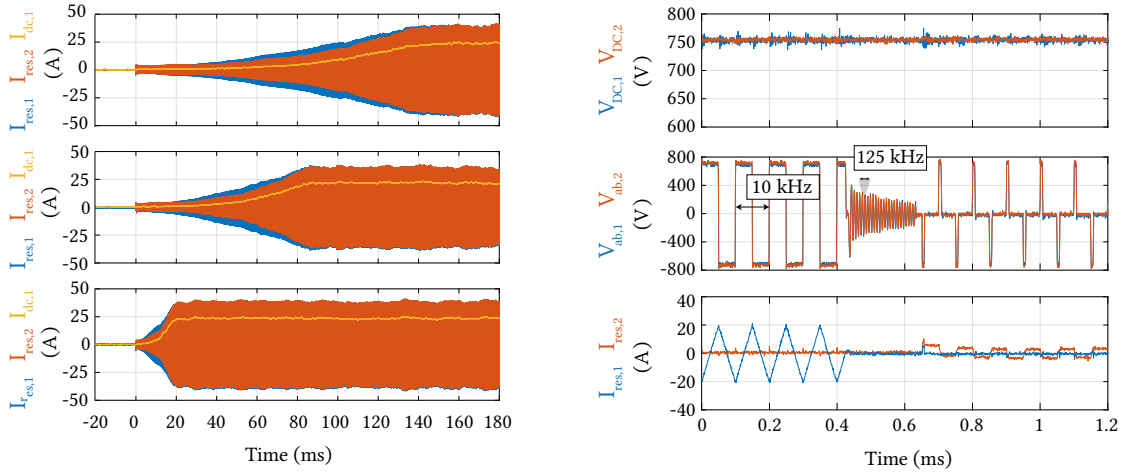
The primary goal is to safeguard the hardware from inrush current. This is achieved by limiting the voltage pulse to a short duration, thus, the current in the circuit experiences only a brief growth period, preventing it from reaching the protection limits. Consequently, both the resonant tank and the system's capacitors charge gradually.

A second advantage of employing a 3L waveform for soft-start is to mitigate issues such as MFT saturation and DC offset of the magnetic flux. **Fig. 3.13a** shows an illustrative example highlighting the difference between applying a direct 50% duty cycle during the start-up and a controlled 3L voltage waveform to the MFT. It is evident that directly starting with a 50% duty cycle voltage waveform results in a DC offset in the magnetic flux, altering the operational characteristics and potentially causing MFT saturation during operation.

On the other hand, using the 3L waveform prevents the creation of a DC offset at startup. The benefit of this soft start is that it allows the DC component to diminish during the gradual ramp-up phase. This phase must be slower than the decay time, ensuring that the peak flux remains sufficiently low. After the start transient, the 50% duty cycle causes no problem to the MFT.

The implementation of the soft start strategy follows the illustration in **Fig. 3.13b**. At first, the power stage is switching with both modulation indices of the unipolar PWM at 0.5. Then, at some point, the DCT turns OFF and is required to restart the operation. Thus, the modulation starts from 0 and increases to 50%, creating the 3L waveform during the start and is gradually brought to a 2L.

During this transient period (the soft-start initialization phase), the DCT exhibits strong non-linearity until the modulation indices revert to 0.5. Consequently, a key aspect of the soft-start strategy is its flexibility in adjusting the soft-start duration based on power demand. The duration can be



(a) (b)

Fig. 3.14 (a) Experimental waveforms showing the soft-start with duration of 0.14 s, 0.08 s, and 0.014 s. (b) Experimental waveforms showing the stop, the idle period for $2T_s$, and soft start with the 3L waveform. During the idle period, a resonance occurs in the resonant tank to equalize the voltages across the switches. Once equalized, the resulting voltage in the resonant tank becomes zero.

predetermined through prior characterization and selected either by monitoring the power or voltage of the system, or by using rate of change information and converting it into a slope duration.

In this way, the speed of the soft-start can be determined by the rate of change of the voltage ($\Delta V'_{DCT}$). If this value is high the soft-start will be fast (short) and if it is low the soft-start will be slow (longer).

To demonstrate the different dynamics for different soft-start speeds, **Fig. 3.14a** shows experimental results for the soft-start with three different speeds. The considered cases consist of i) fast soft-start ($140T_s$), when the rate of change of the voltage is $\Delta V' > 0.1$ V/μs; ii) Medium speed ($800T_s$), when the rate of change of the voltage is between $0.01 < \Delta V' < 0.1$; iii) Slow soft-start of ($1400T_s$) when the rate of change of the voltage is $\Delta V' < 0.01$ V/μs. In **Fig. 3.14b** a detail on a transition of turning DCT OFF, staying OFF for two switching periods, and starting the DCT again with soft-start, showing the 3L waveform.

Finally, the soft-start is a parameter for the DCT intelligence, where depending on the load dynamics, the initialization of the DCT is set accordingly. The soft-start is present in every transition, be it for simple initialization of the DCT or power reversal.

3.3.2 Power Reversal Methods

To allow bidirectional operation, the DCT needs to identify which power stage should be active at the time. Various methods can be developed for this function, however, as they rely on measurements and sensors, an important aspect is the availability of such variables. For the developed prototype, most of the variables of the DCT are available for control, thus, several strategies were created and compared to evaluate its performance.

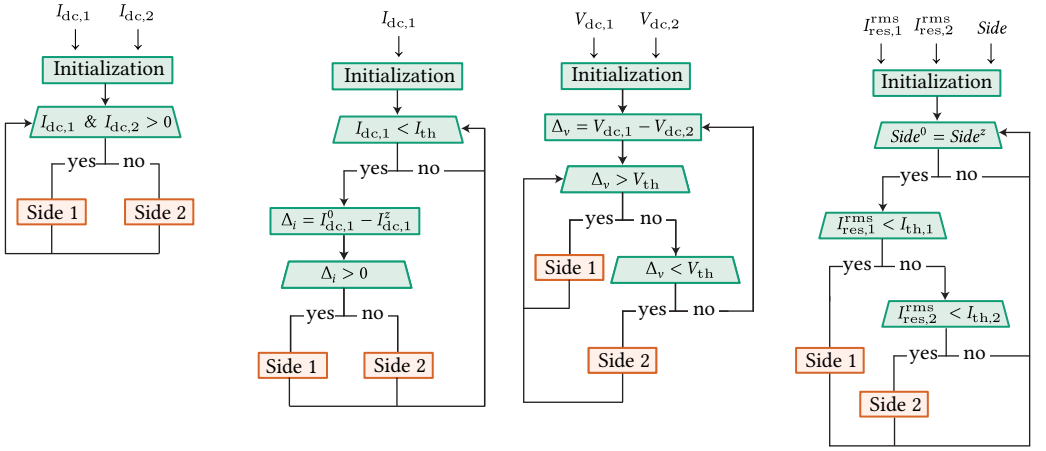


Fig. 3.15 Flow chart of the power reversal methods based on (a) DC Currents, (b) DC current delay, (c) DC Voltages, and (d) Resonant Currents.

In total, four Power Reversal Methods (PRMs) were evaluated for proper identification of the load change and rejection of the system perturbation. **Fig. 3.15** shows the flow chart of the investigated methods.

The first method is based on the DC currents of the two DC ports. For this method, one or both currents can be used to determine the power reversal. The method will detect the change once one or both DC currents cross zero and change their polarity. This is described in **Fig. 3.15a**.

Similarly, by using only one DC current measurement and a delayed sample of it, the power reversal can be detected with the current variation, as shown in **Fig. 3.15b**. This method can be a lead indicator, where as soon as the power reversal is imminent, the method does not wait for the zero crossing to command the power reversal. Thus, this method can anticipate the power reversal, and this can be beneficial for the fast transition dynamics.

Another approach using the DC voltages indicates the power flow direction by acknowledging which DC port is higher/lower than the other. The threshold of this method is defined by the DCT losses, or by the minimum voltage difference that causes no power transfer - only internal power circulation. This solution, differently from DC current method, will identify the power reversal after the DC current crosses zero. Nevertheless, this method is well suited for DC PDN where both DC buses have the voltage controlled by other converters, and therefore the PRM dynamic is well tied to the DC PDN dynamic. A limitation of this solution is the precision of the voltage sensor and noise in the measurement. However, both limitations can be taken into account when defining the voltage threshold. The flowchart for the DC voltage method is shown in **Fig. 3.15c**.

The last evaluated method was based on the resonant currents. The resonant currents bring the information when the power flow is changing direction based on the reduction in the resonant peak value. This method can identify the power direction by checking on which side the current is higher/lower, for this both sides need to be measured, and the flow chart is shown in **Fig. 3.15d**. The same idea could also be applied to the capacitor voltage of the resonant tank. In this case, the method

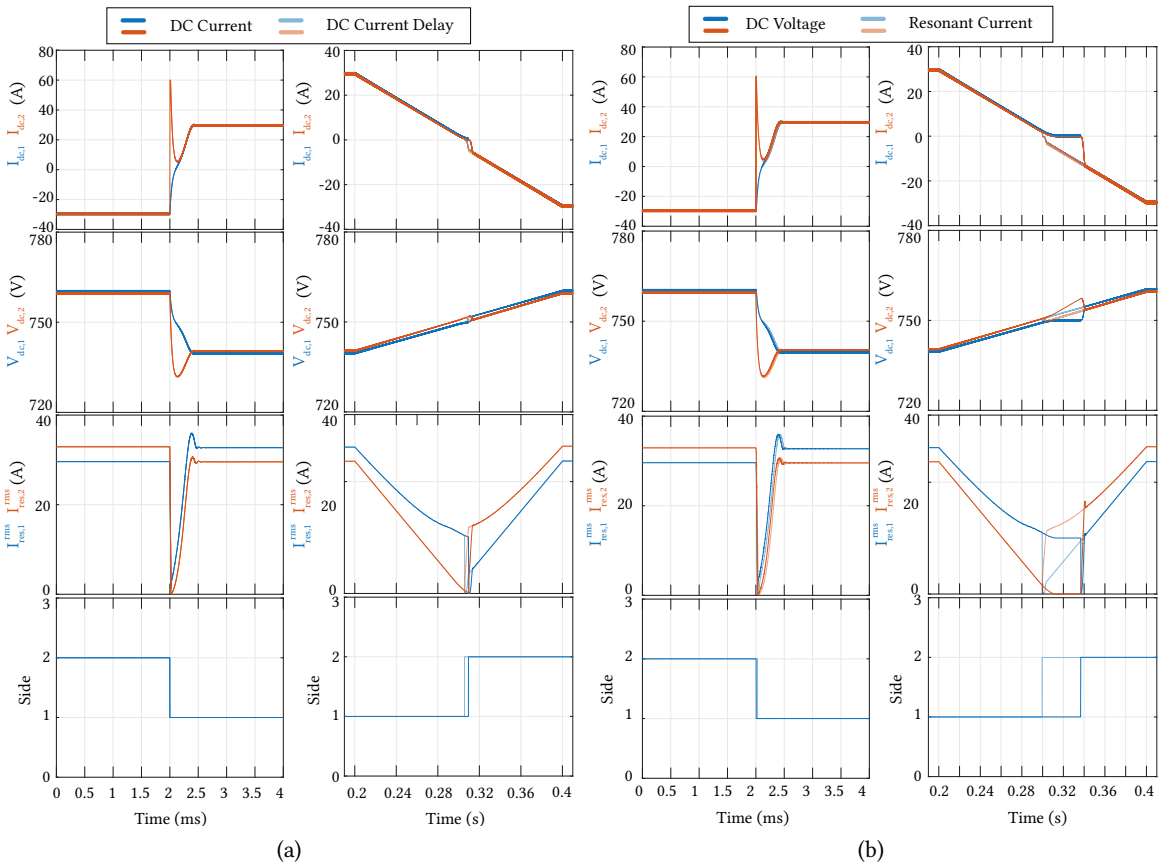
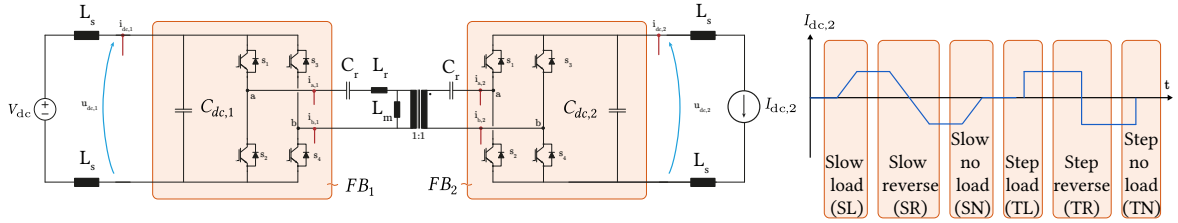


Fig. 3.16 Simulation in PLECS of the four methods for a step (left) and a ramp test (right). (a) The DC currents and the DC current delay methods are shown together, and in (b) the DC voltage and the Resonant Current methods are shown. From the top to the bottom, each plot shows the DC currents ($I_{dc,1}, I_{dc,2}$), DC voltages ($V_{dc,1}, V_{dc,2}$), resonant current RMS value ($\tilde{i}_{res,1}$,$\tilde{i}_{res,2}$) and side command corresponds to the power stage 1 and 2 being active, respectively.

also requires the measurement of both sides in order to identify the power direction and to identify the reversal when the voltage reduces to the range of detection and hits a target minimum value.

In **Fig. 3.16** the four methods were simulated in PLECS to verify its dynamics versus very aggressive step change and slow ramp power reversal. At the time $t = 2\ ms$, the voltage of DC bus 2 decreases and reverses the power flow, and at $t = 0.2\ s$ the voltage ramp-up of DC bus 2 is performed.

For the step change, all the methods performed similarly, without any noticeable differences. Some differences can be noticed in the ramp-up tests. It can be noticed for the DC Current Delay method, that once the current reached the threshold value, $I_{th} = 2\ A$, the method already sent the command to switch sides, while the DC Current method waited for both DC currents zero crossing to switch sides, similarly to the RMS resonant currents method. Further, it is noticeable that the DC voltage method took longer to detect the power reversal once the voltage difference needed to change polarity and hit the threshold $V_{th} = 5$ V. Nevertheless, all the methods performed properly as expected.



(a) (b)

Fig. 3.17 DCT and load profile under study, (a) schematic of the simulated and experimental system, and (b) Load profile with $I_{dc,2}$ variations.

Tab. 3.4 The time delay indicates the duration each PRM required to detect the power reversal following the load inversion. For details on the load profile and acronyms, refer to **Fig. 3.17**.

PRM	SL	SR[1]	SN	TL	TR	TN	OV	UD
DC Current	9.5 *ms*	2 μs	no	70 μs	2 μs	yes	-	-
DC Current Delay	49 *ms*	−10 *ms*	no	2.4 μs	2 μs	yes	-	-
DC Voltage	36 *ms*	27 *ms*	no	140 μs	74 μs	no	0.63 μs	0.12 *ms*
Resonant Current	50 *ms*	−5 *ms*	no	181μs	1 μs	yes	-	-

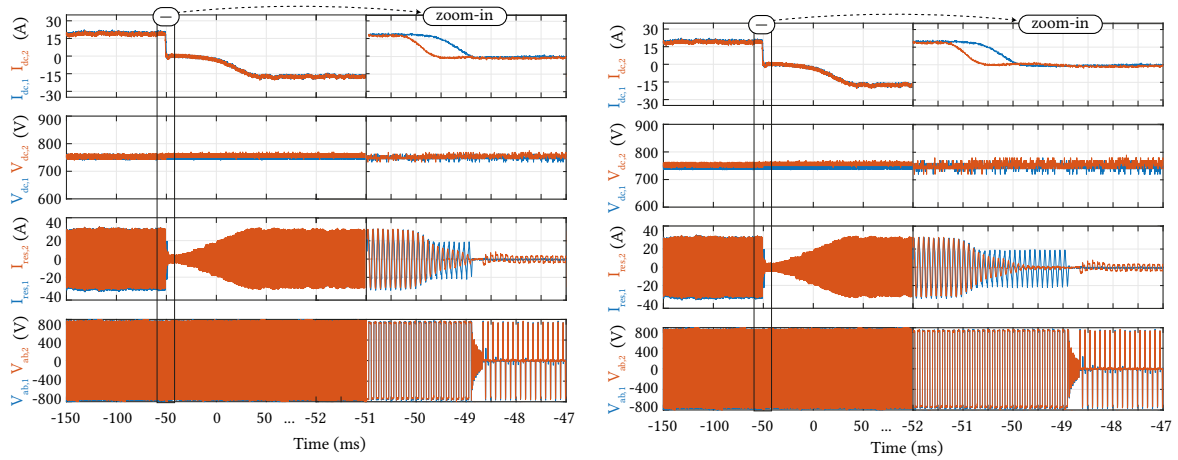
[1] Time relative to the zero crossing of dc current. Negative means leading signal

To perform a quantitative evaluation of the previously discussed methods, **Tab. 3.4** shows the reaction time for different load dynamics and system perturbation. In this simulation, several different loads were applied according to the scheme shown in **Fig. 3.17**.

The two system perturbations performed are: i) Overvoltage (OV), a spike of 10% of the voltage during 10 μs, and ii) Undervoltage (UV), a drop of 10% of the voltage during 10 μs. These two system perturbations were performed in the DC bus 1 ($V_{dc,1}$), with nominal load conditions in the forward direction (bus 1 to bus 2). By performing the system perturbation, the PRM should not be triggered by such an event, and if triggered, should return to the correct set point after perturbation.

It can be seen in **Tab. 3.4** that for the step/ramp to no load simulation (refer to SN and TN), it is not a problem if the PRM sets a new direction because all methods in steady-state can identify the power flow direction. From the system perturbation point of view, the DC current methods performed perfectly without setting a new reference for a reversal. The DC Voltage method set a reference to reverse power during both events and corrected its set point after the perturbation. However setting this reference during this event could provoke a very high current in the DCT, and this should be avoided with a protective layer. One option is to implement a consolidation period for setting a power reversal, ensuring that a power reversal is needed after tens of microseconds, for example.

The load steps were mainly led by the dynamic of the DC bus 2 voltage, which created a high current overshoot and triggered the PRMs almost instantly. For ramp loads, all the methods also had a similar behavior among the analyzed PRM. The fastest method for the slow load test (SL) was the DC Current method, which does not depend on an error calculation (i.e. ΔV, or ΔI) to set the power reversal and identify the power direction. But, for the other tests, the DC Current Delay was faster.



(a) DC Current Delay Method

(b) DC Currents Method

Fig. 3.18 Experimental waveforms showing the response of the DCT for the step reverse ($dv/dt = 5\ V/\mu s$), for the DC current delay and DC currents methods. Zoom shows the moment of the power reversal, where it is possible to note that DCT enters idle mode and starts its initialization sequence with a three-level waveform. Before the method detects the power reversal, the DCT operates for some time with only the magnetizing current noticeable in the third plot in blue.

In the slow reversal test (SR) one can see the advantage of the DC Current Delay method by predicting the imminent reversal before the current reach zero. The Resonant Current method also predicted the imminent reversal due to the well-tuned threshold value for this system. This can be reached in case the DCT and DC PDN are well known, however, parameter variations can alter the DCT characteristics and this behavior is not always true.

3.3.2.1 Experimental Verification

The three methods based on the DC terminal variables were implemented in the LV DCT prototypes, and similar tests were performed. The period between the turn-OFF and soft-start was set to a fixed value of two switching periods to eliminate its influence.

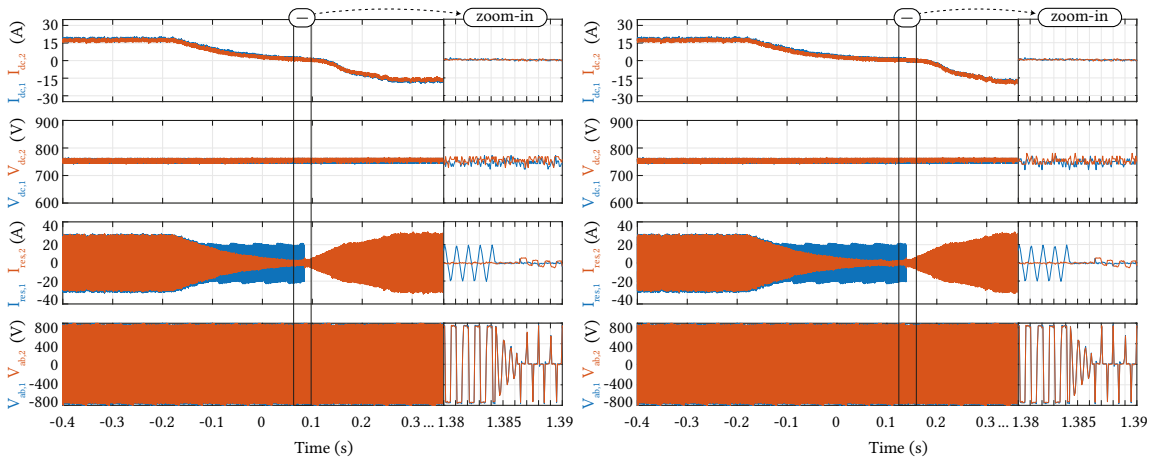
The load step is performed by regulating the $V_{dc,1} = 750\ V$ and changing $V_{dc,2} = 742\ V$ to $V_{dc,2} = 755\ V$ with a slope of $dv/dt = 5\ V/\mu s$. In this experiment, the DCT is feeding a load with forward operating mode, and suddenly, the load changes, inverting the power flow. **Fig. 3.18** shows the step change for the DC current methods. Both methods had similar performance as expected. The detection was in the order of a few microseconds.

Fig. 3.19 shows the ramp reverse with a slope of $dv/dt = 0.025\ V/ms$. For this test, the DC Current Delay was faster and detected the reversal of approximately 400 ms before the DC Current method. This is mainly due to the pre-set threshold of the DC current delay of $I_{th} = 2$ A and for the DC current, the threshold band is set to $I_{th} = 1$ A.

Fig. 3.20 shows the step and ramp reverse for the DC voltage method. Clearly, this method detects the power reversal later than the strategies based on currents, as noticeable from the magnetizing current before the reversal indicated in blue. Nevertheless, it detected correctly the power reversal.

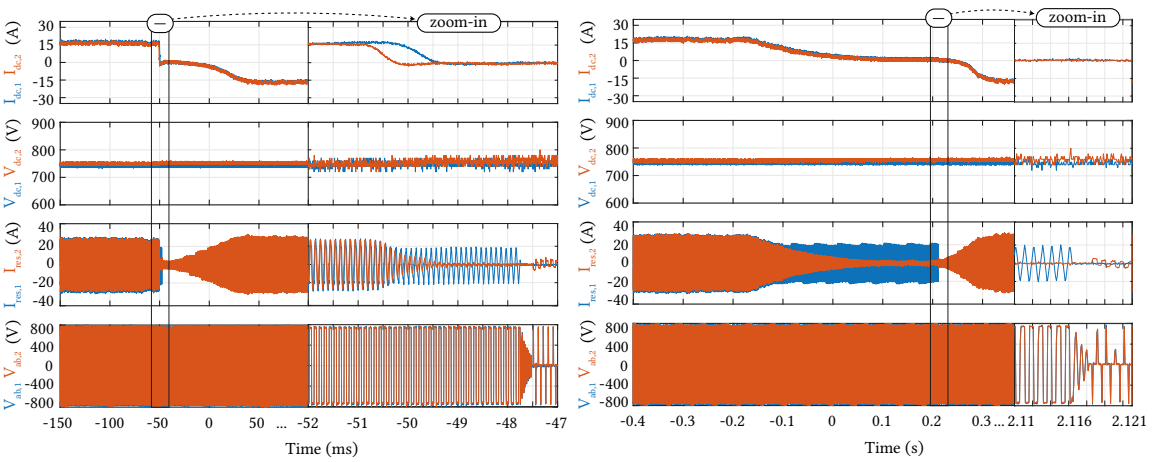
Any of these methods can serve as the power reversal technique for the DCT. However, a notable

advantage of the DC Voltages method is its ability to discern the correct power direction even when the DCT is OFF. This is possible because the DC voltages are always available at the DC ports, enabling the DCT to initiate immediately with the correct power flow direction. Moreover, the DC voltages directly correspond to the power transfer within the DCT. By relying on these voltage measurements, the DCT can accurately determine the amount of power being transferred. Therefore, in situations where only circulating power is present, the DCT can be turned off to prevent no-load losses.



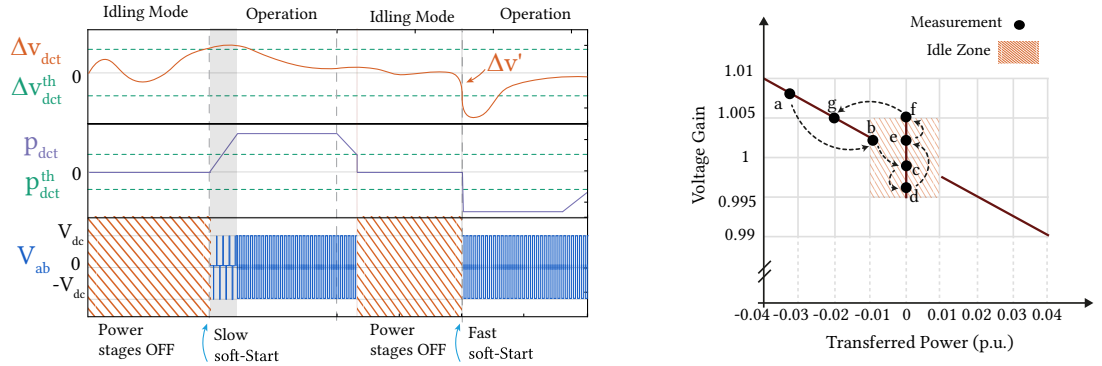
(a) DC Current Delay Method (b) DC Current Method

Fig. 3.19 Experimental waveforms showing the response of the DCT for the ramp reverse ($dv/dt = 0.025\ V/ms$), for the DC current delay and DC currents methods.



(a) DC Voltage Method (b) DC Voltage Method

Fig. 3.20 Experimental waveforms showing the response of the DCT for the step reference reversal ($dv/dt = 5\ V/\mu s$) and ramp reverse ($dv/dt = 0.025\ V/ms$), using the DC voltages method. Zoom shows the moment of the power reversal, where it is possible to note that DCT enters idle mode and starts its initialization sequence with a three-level waveform.



(a) (b)

Fig. 3.21 (a) Illustration of the idle mode operation principle. The DCT is initialized with a slow soft-start only when the ΔV_{DCT} overcomes ΔV^{th}_{DCT}. In case the voltage variation is too aggressive, the soft-start period is reduced. At the moment the power processed by DCT is below the P^{th}_{DCT}, and the DCT stops switching. (b) Example of idle mode profile implemented in the LV DCT prototypes.

3.3.3 Idle Mode

The idle mode is the operating mode used to improve the efficiency of the DCT, by avoiding the no-load losses. In this sense, this mode defines when the DCT should turn ON and turn OFF. **Fig. 3.21** illustrates the idle mode operation principle.

At first, the DC voltages difference is small, not enough to cause a power flow throughout the DCT. This corresponds to the first section of **Fig. 3.21a** where the DC voltage difference varies but does not reach a level where any power is transferred besides the no-load losses of the DCT. As soon as the voltage difference between the primary and secondary side ($\Delta V_{DCT} = V_{dc,1} - V_{dc,2}$) is above the threshold level, the DCT starts transmitting power. At that moment the DCT is activated until the power being processed contains only the no-load losses of the converter. Thus, the DCT enters idle mode and stays inactive until the voltage difference overcomes the pre-defined threshold again.

The no-load losses of DCT correspond to the losses on the power stages, resonant circuit, and MFT. This value can be computed or experimentally determined and set as a power level threshold. **Fig. 3.21b** shows an illustrative example of the idle zone on the voltage difference and power characteristics of the DCT, implemented for controlling the idle mode.

Firstly, the control unit measures the voltage and computes the voltage difference, starting at point **a** of **Fig. 3.21b**. Then, the voltages change, and the power moves along the line. At some point the power being processed hits the threshold at point **b**, meaning that DCT is only processing the no-load losses, and then it enters into idle mode. The voltages keep changing (**c**,**d**,**e**) but the voltage difference is still below the voltage threshold. At the moment the voltage difference reaches a threshold at point **f**, the processed power would be more than only no-load losses. Therefore, the DCT starts its operation and moves to point **g**, and transfers the required power.

Essentially, this mode defines the operation range of the DCT. To start there needs to be some voltage difference between the DC terminal which means that power needs to be transferred, and it stops when only circulating power is present. Further, the introduction of an idle period during transition avoids possible jittering around zero when computing power reversal. Also, at every start of the

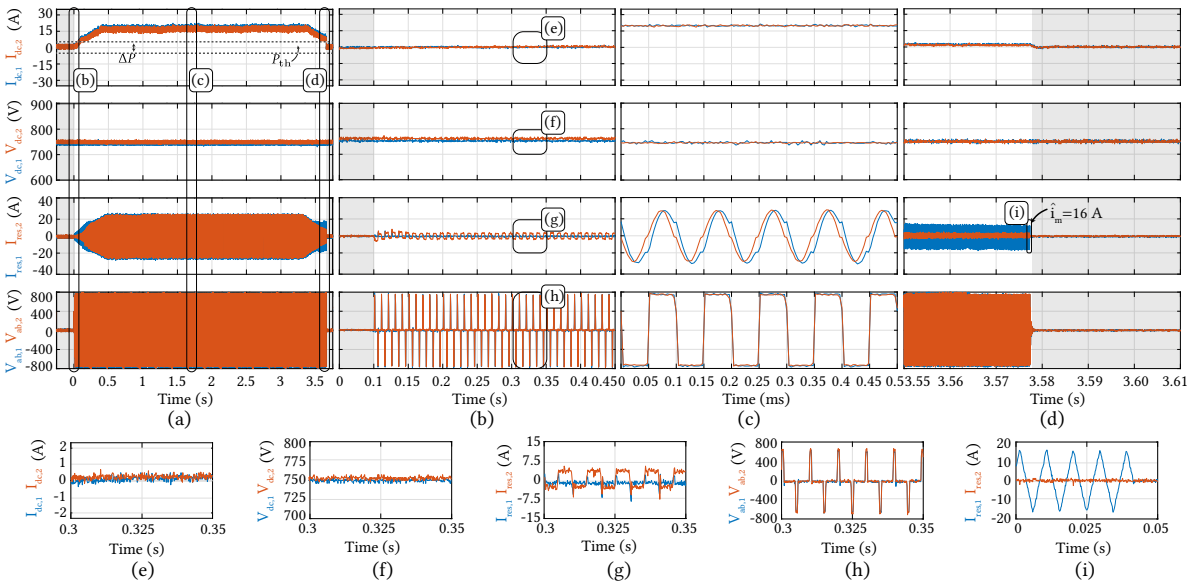


Fig. 3.22 Experimental waveforms showing the DCT in idle mode, with a power threshold: (a) an overview of the Idle mode operation; (b) details on the soft-start; (c) the operation waveforms; and (d) details on the turn-off moment. During the shaded period, DCT is in an idle state waiting for the expected power to overcome its threshold. At $t = 0\ s$ the DCT turns on by noticing the DC voltages mismatch. Once the DC buses return to equilibrium after $t = 3.5\ s$, the DCT turns off, as the power is below the threshold value. In (e), (f), (g), and (h) zoom-in on the soft-start waveforms is given; (e) details on the DC current; (f) details on the DC voltages; (g) details on the resonant currents; (h) details on the 3L voltage applied to the resonant tank. In (i), zoom-in on the resonant current when DCT is processing only the magnetizing current is shown.

DCT, the correct direction is set by the voltage difference threshold, which avoids the trial and error approach [71].

Fig. 3.22 shows the experimental demonstration of this operation mode. At first, the two buses are in equilibrium, and no power is transferred. Then, at $t = 0\ s$, the DCT detected the $\Delta V_{DCT} > \Delta V_{DCT}^{th}$ (which in this example is $\Delta V_{DCT}^{th} = 3$ V), and the DCT starts its operation. After $t = 3.3\ s$, the DC buses return to equilibrium. At that moment, the DCT stops switching to reduce losses, when there is no need for DCT to transfer any power. In this experiment, the power threshold was set to $P_{DCT}^{th} = 1$ kW, based on the MFT losses and power stages [104].

Other variables could also be used to identify that only no-load losses are present in the DCT. For instance, the threshold can be set by observing both resonant currents and verifying if only a magnetizing current exists. In any case, threshold values need to be set according to the parameters of the DCT, preferentially based on experimental verification.

With this operating mode, the no-load losses can be avoided if DCT intelligence turns OFF DCT and enters idle mode. For the case of the DCT 1, the no-load losses represent 0.45% of rated power (100 kW). Also, the idle mode defines when the DCT turns ON, and it computes the required speed of the soft-start based on the rate of change of the voltage difference, which combines all the logic to create a complete algorithm for operating the DCT.

3.4 Complete Operation of DCT

The complete operation of the DCT includes all the previously mentioned logic interconnected. In summary, the idle mode determines when the DCT should be activated, the soft-start determines how fast the power transition should be according to the load dynamic, and lastly, the PRM determines the active power stage of the DCT.

A complete scheme for the Power Reversal Algorithm (PRA) is shown in **Fig. 3.23**. The PRA refers to the complete algorithm, with a PRM, idle mode, and different speeds for the soft-start depending on the load dynamics. With this logic, the DCT has a well-defined open-loop operation. The DCT starts operating when the voltage difference reaches a certain level, with a soft start weighted by the load dynamics, always in the correct direction. The DCT stops only when the processed power is below a defined power threshold. In this sense, the PRA is a robust strategy because, in case of a voltage spike or big transients in the voltage, the PRA will not issue any command, while the power stays above the minimum limit.

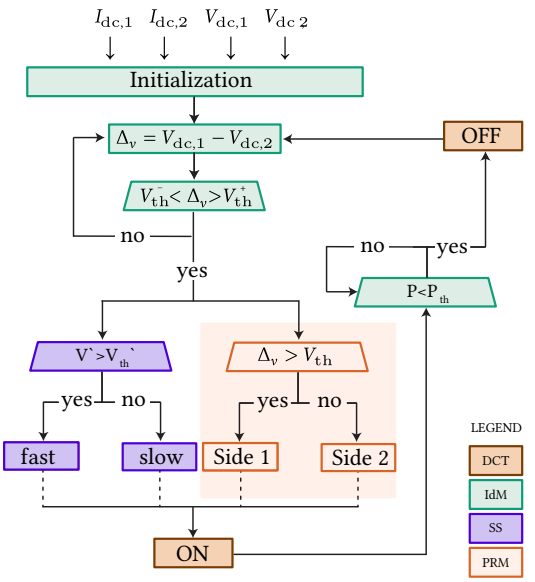


Fig. 3.23 Power Reversal Algorithm, with PRM strategy based on the DC voltages. Each color corresponds to a different section of the operation strategy. Variations of this scheme can be created according to the available measurements.

A complete test is shown in **Fig. 3.24** with the step load and ramp load variation. This figure demonstrates each function of the PRA. Firstly, the DCT is processing $P_{dc} \approx 18$ kW, when suddenly, the power reverses when $V_{DC,2}$ increases from $V_{DCT,2} = 744 \rightarrow 760$ V, with a slope of $(dv/dt = 5\,V/\mu s)$. The PRA, quickly identifies that the power was reduced and puts DCT in idle, when the minimum power was reached (here set to $P_{th} = 3$kW for demonstration); by noticing that the power direction changed and the variation of the voltage is higher than the $\Delta V'_{th}$, (here set to $\Delta V'_{th} = 0.01\ V/\mu s$), the PRA triggered the fast initialization of the DCT, for the power stage 2.

The details of the first transition can be seen in **Fig. 3.25**. On the left the details in the transition from the operation mode to the idle mode are shown, and on the right the details of the soft-start initialization with a fast initialization time of $t_{ss} = 14$ms.

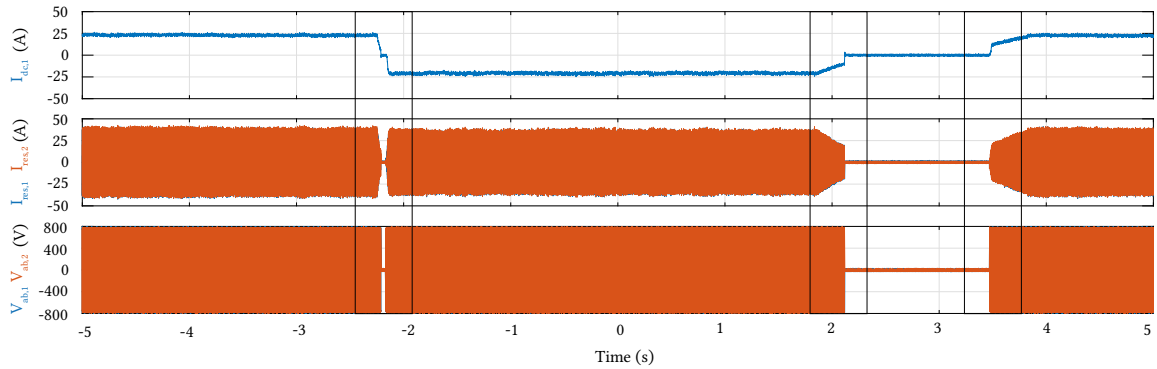


Fig. 3.24 Experimental waveforms showing the response of the DCT for a fast power reversal, and slow power reversal. The DCT uses PRA to determine its operation limits and set the proper initialization time. The DCT processes power in both directions and a load profile is set to test and validate the PRA. Squares mark the zoom available in **Fig. 3.25** and **Fig. 3.26**

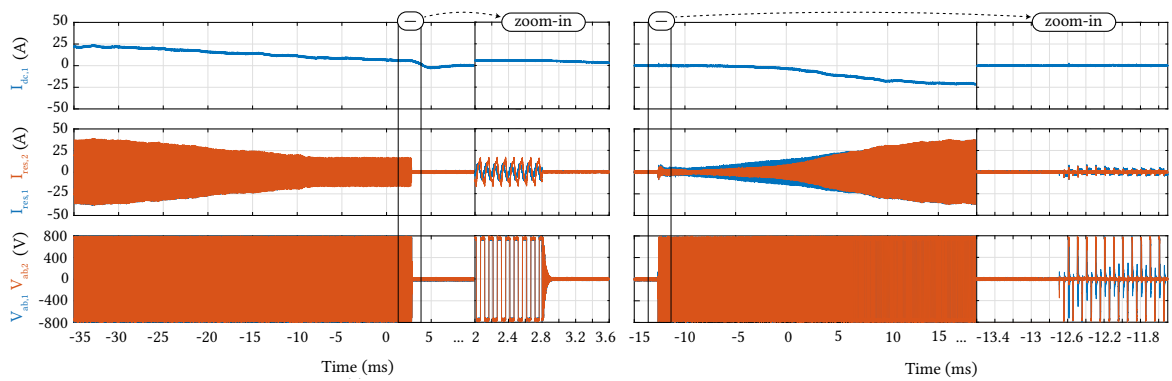


Fig. 3.25 Experimental waveforms showing the response of the DCT for the fast power reversal (zoom in the first transition). On the left, the moment DCT enters idle mode by reducing the processed power below the threshold (zoom in at the moment DCT goes idle). On the right, the moment DCT starts the soft-start with a fast dynamic load (zoom in at the moment the power stage starts switching.)

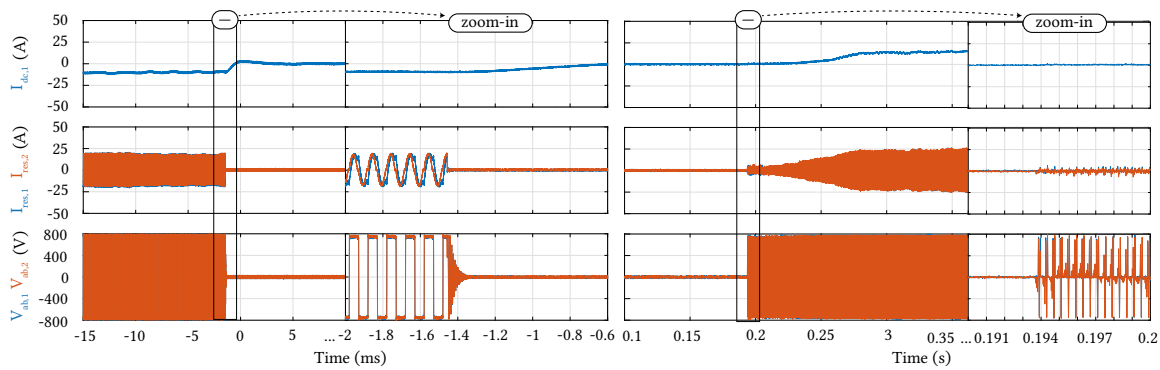


Fig. 3.26 Experimental waveforms showing the response of the DCT for the slow power reversal (zoom-in in the second and third transition). On the left, the moment DCT enters idle mode by reducing the processed power below the threshold. Zoom-in at the moment DCT goes idle. On the right, the moment DCT starts the soft-start with a slow dynamic load. Zoom-in at the moment the power stage starts switching.

After some time, the load changes again and starts decreasing the $V_{dc,2}$ voltage slowly. At this moment, as soon as the power reduces and reaches the power threshold, the DCT enters idle mode. Then, the $V_{dc,2}$ voltage keeps decreasing until the voltage difference between the two DC ports is bigger than the voltage threshold Δ^{th}_{DCT} (here set to Δ^{th}_{DCT} = 3V.) At that moment, the DCT notices the voltage difference and initializes its operation with a slow soft-start as the rate of change of the voltage is $\Delta V' < 0.01$ V/μs.

Fig. 3.26 details the dynamics of the second and third transitions. Firstly, on the left, the DCT enters the idle mode at the moment the processing power is below the threshold. Then, on the right side, the soft-start of the power stage 1 happens with t_{ss} = 0.14s, as the load variation is slow.

Several variations of the schematic of **Fig. 3.23** could be created by using different power reversal methods, different variables to set the idle mode, different variables to set the soft-start speed, etc. Also, another option is to combine measurements to use the best of every method. This all depends on the available variables for control.

Ultimately, the PRA performed effectively and as anticipated. This algorithm enabled the DCT to be appropriately guided to naturally follow the power flow dictated by the DC buses. All the threshold values used were established based on an understanding of the DCT's parameters and for demonstration purposes.

3.5 Summary and Conclusion

This chapter presented the essential open-loop control strategies for the reliable operation of DCTs. Firstly, the soft start strategy was presented, followed by the evaluation of four power reversal methods, identifying their advantages and drawbacks. Later the Idle mode was presented which is used to avoid no-load losses when the DCT is not transferring any power. In the end, the development of a complete algorithm led to a more robust open loop strategy to set the operating range and allow bidirectionally of the DCT.

The developed strategies were tested with the LV DCT prototypes and were proven to be effective for the DCT operation. However, it is important to point out that all the tests were conducted in the laboratory environment, and the operation with real DC PDN might impose some challenges, such as big DC bus voltage oscillation, noise on measurements, data acquisition bandwidth, etc.

Finally, with the developments of this chapter, the operation of DCT becomes very similar to the AC transformers, which are the desired characteristics for DC PDNs. Nevertheless, other features such as overload protection, black-start capability, and DC bus voltage control, are other tasks that the DCT might need for even more advanced DC PDNs, not addressed in the thesis.

4

Medium Voltage Direct Current Transformer

This chapter presents part of the development of an MV resonant DC transformer based on a split-capacitor IGCT 3L-NPC leg. It investigates both the dynamic and static balancing of the 3L-NPC when operating in a two-level, 50% duty cycle mode. The investigation includes the analysis of the switching transient behavior under different turn-off current conditions, the performance of the dynamic voltage balancing with a low-value capacitor snubber, and a comparative evaluation of two static voltage balancing strategies. This chapter also includes details of the MV DCT design and the construction of the prototype. Finally, the snubber designs are verified by experiments using a prototype built in the laboratory.

4.1 Introduction

The development of high-power MV converters presents multiple challenges in ensuring their safe and reliable operation, incorporating high-voltage devices, and operating at medium frequencies. To build an MV DCT, medium voltage technologies must be used. The power switches, medium voltage insulated MFT, and all the equipment around the converter must agree with the rated operating values and safety requirements.

In the previous chapter, the DCT was built with full-bridge power stages, that allowed the use of equipment and switches rated at the top end of the LV devices. To upscale the power stage and reach MV ratings, one option would be using the series/parallel arrangements of devices. However with this approach, the number of devices increases drastically, and accordingly, the price and the losses also increase.

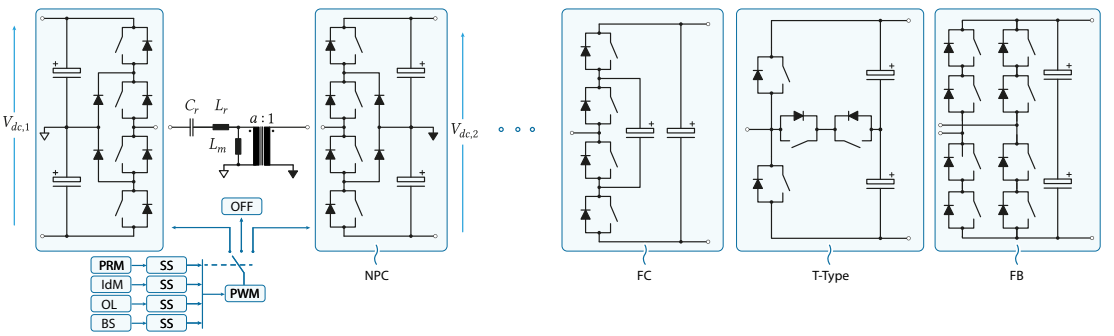


Fig. 4.1 MV DCT with different possible power stages to achieve higher voltages. Example of different power stages one could use to build a DCT.

Another solution is to use multi-level topologies which are more suitable for higher ratings require-

ments. Topologies such as Neutral Point Clamped (NPC), Flying Capacitor (FC), and T-type inverter, among other variations, as shown in **Fig. 4.1**, are common solutions for high-power converters. These topologies use less power semiconductors than the FB solution and are capable of providing 2L and 3L voltage waveforms for their use in DCTs.

In a 3L-NPC as shown in **Fig. 4.1**, each power device faces half of the DC-link voltage, allowing its design for higher voltage levels. In fact, the NPC power stage is widely used in MV drives in the industry. The family of converters from [105], uses the Reverse Conducting (RC) IGCTs to build the NPC stacks and assemble a converter up to 5MW. These devices, as discussed in the introduction, are suitable for MV high-power converters due to their high current capability, high voltage ratings, and low conduction losses.

Therefore, taking advantage of the well-known technology, a 3L-NPC leg with RC-IGCTs was selected for the DCT. The next sections discuss the design and prototyping of the 10 : 5 kV/kV DCT and experiments toward the commissioning of the power stages. Noted that the complete prototype was not fully finalized during the Ph.D. work, only no-load tests were performed.

4.2 Design and prototype of the MV DCT

The MV DCT prototype consists of a 10 : 5 kV Split-Capacitor 3L-NPC converter. The primary side is supported by 10 kV RC-IGCTs and clamping diodes acquired as engineering samples from Hitachi Energy Semiconductors. The secondary side operates with a 4.5 kV RC-IGCTs (5SGX1445H0001), and clamping diodes (5SDF10H4503). A simplified schematic of the converter is shown in **Fig. 4.2a**.

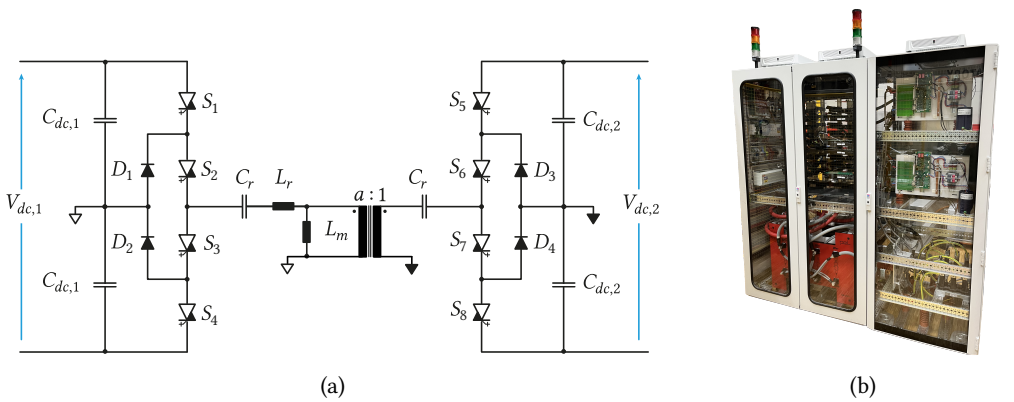


Fig. 4.2 (a) Simplified schematic of the Split-Capacitor IGCT-based 3L-NPC converter. (b) Photograph of the complete MV DCT prototype.

During the design and assembling phase of the DCT, different aspects of the design were addressed in other works. The design and prototype of the MFT was developed in [106], and in [107] and [108] the IGCTs operation for the 5 kV, 5 kHz, and low turn-off current was investigated. In this work, the assembly of the 3L-NPC power stage with the MFT was completed, and the no-load operation was tested.

Fig. 4.2b shows a photo of the DCT prototype. The complete converter fits inside the cabinet, besides the water cooling unit which is located outside and connected to the laboratory water supply system.

Description	Symbol (Unit)	Value
DC Voltage 1	$V_{\mathrm{dc},1}$ (kV)	10
DC Voltage 2	$V_{\mathrm{dc},2}$ (kV)	5
Rated power	P_{n} (MW)	1
Cable inductance	L_s (μH)	30^b
Cable resistance	R_s (mΩ)	2^b
DC-link capacitance 1	$C_{dc,1}$ (μF)	400
DC-link parasite resistance 1	$R_{Cdc,1}$ (mΩ)	2
DC-link balancing resistor 1	$R_{p,1}$ (kΩ)	200
DC-link discharge resistor 1	$R_{dis,1}$ (kΩ)	250
DC-link capacitance 2	$C_{dc,2}$ (mF)	2.6^a
DC-link parasite resistance 2	$R_{Cdc,2}$ (mΩ)	1
DC-link balancing resistor 2	$R_{p,2}$ (kΩ)	200
DC-link discharge resistor 2	$R_{dis,2}$ (kΩ)	50

^{a} ± 10% tolerance, ^{b} estimated

Tab. 4.1 General information about the MV DCT

Description	Symbol (Unit)	Value
RC-IGCT - 5SGX 1445H0001		
Slope resistance	r_{on} (mΩ)	2
ON inductance	L_{on} (μH)	1
Threshold Voltage	V_{f} (V)	1.65
Parasitic Capacitance	C_{p} (nF)	$1-3$
Leakage Current	I_{DMR} (mA)	20
RD ON resistance	$r_{\mathrm{on,d}}$ (mΩ)	4.3
RD Threshold Voltage	$V_{\mathrm{f,d}}$ (V)	2.53
Crit. rise of on-state	di_{tr}/dt_{er} (A/μs)	285
Turn on delay time	$t_{d,on}$ (μs)	3
Turn off delay time	$t_{d,off}$ (μs)	6
Diodes - 5SDF 10H4503		
Diode ON resistance	$r_{\mathrm{on,D}}$ (mΩ)	0.88
Diode ON inductance	$L_{\mathrm{on,D}}$ (μH)	0.5
Diode Forward Voltage	$V_{\mathrm{f,D}}$ (V)	2.53

Tab. 4.2 Power semiconductors details

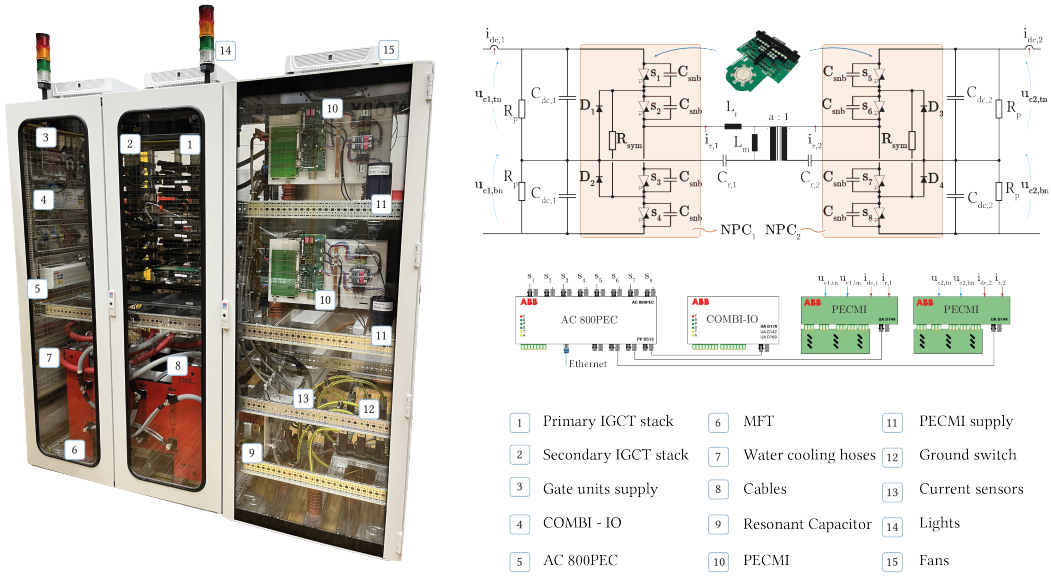
The main parameters of the MV DCT are given in **Sec. 4.2** and **Tab. 4.2**.

Fig. 4.3 shows the details of the MV DCT prototype. The stack itself is a pre-engineered, commercial product and is in regular use in ABB's ACS1000 product series of hard switching power converters. The stack consists of an NPC leg, with the IGCTs and diodes, alternating heat sinks, all held by a mechanical clamp. The heat sink provides a thermal interface for the heat exchange between the press-pack devices and the deionized water.

Each gate driver unit has a dedicated external power supply. The IGCTs are controlled by ABB's AC800PEC. The ABB's COMBI-IO equipment is used for the light tower, door signal, fans, ground switch, and relays. The ABB's PECMI equipment is used to capture the current and voltage sensor information. The voltage is sensed by the HV measurement board, directly connected to PECMI. All the signals communicate with the central controller via an optical link.

The DC-link capacitors discharging circuit was designed to ensure a discharge from nominal voltage to 50 V within 5 minutes. A relay is connected in series with the resistors for the charge/discharge operation.

The resonant tank is composed of the leakage and magnetizing inductances of the MFT and the high current-rated resonant capacitors. These elements are discussed in detail in the following section.



(a) (b)

Fig. 4.3 (a) Photo of the MV DCT with descriptions. (b) Schematic of the MV DCT.

4.2.1 Medium Frequency Transformer

The MFT for this prototype was designed in [106]. In that work, several aspects of modeling and designing an MW-rated MFT were evaluated. As a result of the analysis, an optimization algorithm to compute the most important parameters of an MFT was developed to find designs that fit the application requirements, having as trade-offs the power density and efficiency. Ultimately, an optimization routine was applied to select the best design and potential candidates for prototyping.

For the development of the MFT, both the leakage and the magnetizing inductance were designed to meet the requirements of the MV DCT prototype. Following studies performed in [108], using the IGCT-based stack for medium frequency soft-switching application, the suggested value of magnetizing inductance is in the range of 25 – 50 mH. This value would result in a turn-off current for the 5 kV side of $I_{off} \approx 20$ A and for the 10 kV side, $I_{off} \approx 10$ A, which would fulfill the power budget and result in safe switching transients.

Furthermore, to ensure stiff voltage characteristics (by having a big inductance ratio of around a thousand) the leakage inductance was chosen to be in the range of 25 – 50μH. This value also corresponds to a feasible resonant capacitor which could be realized with external capacitors, as it will be further discussed in the following section.

Among diverse technologies that can be used to build an MFT, this prototype explored the nanocrystalline air-cooled core and hollow copper oil-insulated water-cooled windings. Consequently, as an output from the optimization routine, a design was selected for the prototype [106]. The prototype was designed for 5 kHz, and oversized to allow the operation with lower switching frequencies, down to 1kHz, without entering into saturation.

Fig. 4.4 shows the MFT prototype and **Tab. 4.3** shows the essential parameters for this thesis. To complete the resonant tank, the capacitors are mounted externally. Further, for all the experiments in

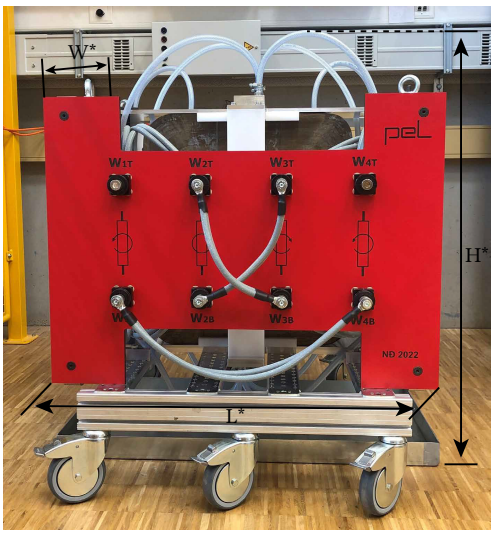


Fig. 4.4 1 MW MFT prototype

Description	Symbol (Unit)	DCT
Leakage inductance (2:1)	L_r (μH)	42.86
Leakage inductance (1:1)	L_r (μH)	11.1
Magnetizing inductance	L_m (mH)	10.7
Winding resistance	R_w (mΩ)	40
Operating frequency	f_s (kHz)	$1-5$
Inductance ratio	L_n	964
Calculated Turn-off Current	$I_{off}(A)$	11.682
Calculated Peak Current	$\hat{I}_{Lr}(A)$	830

Tab. 4.3 MFT main parameters

this thesis, the winding was connected in a parallel-parallel connection [106], used for 5 : 5 kV/kV operation, as the 10kV operation is out of the scope of the thesis.

4.2.2 Resonant Capacitors

The initial step in choosing the resonant capacitors involves considering the required voltage and current ratings. The voltage stress across the capacitor is determined using the expression (4.1), which establishes a relationship between the resonant capacitor voltage and the output load current [107]. Similarly, the peak current is derived from the output load current using (4.2). Consequently, the capacitor can be chosen to endure these calculated stresses.

$$V_{C,r} = \frac{\pi}{n\omega_n} Z_r I_0 \tag{4.1}$$

$$I_{C,r} = \frac{\pi}{2}\frac{1}{a} I_0 \tag{4.2}$$

The value of the resonant capacitor has a direct impact on the resonant frequency of the resonant tank. If this capacitor's value is considerably lower than that of the DC-link capacitors, it becomes the primary factor influencing the resonant frequency. However, when the capacitance is similar to that of the DC-link capacitors, the impact of the DC-link capacitor also needs to be considered.

In situations where the DC-link capacitance on each side differs, such as in the case of the MV DCT prototype, each side of the DCT has a distinct impact on the equivalent capacitance. To ensure smooth bidirectional operation, it becomes crucial to ensure that both sides of the resonant tank impedance loops exhibit similar impedance characteristics. This requires calculating the equivalent capacitance for each side and any additional required capacitance (resonant capacitor) should be incorporated accordingly.

Using the schematic of **Fig. 4.2a**, the equivalent capacitance of the primary and secondary sides can be calculated according to the following:

- Primary side

$$C_1 = \frac{\left(C_{dc,1} + C_{dc,1}\right) \times C_{r,1}}{\left(C_{dc,1} + C_{dc,1}\right) + C_{r,1}} = \frac{2C_{dc,1} \times C_{r,1}}{2C_{dc,1} + C_{r,1}} \tag{4.3}$$

- Secondary side

$$C_2 = \frac{\left(C_{dc,2} + C_{dc,2}\right) \times C_{r,2}}{\left(C_{dc,2} + C_{dc,2}\right) + C_{r,2}} = \frac{2C_{dc,2} \times C_{r,2}}{2C_{dc,2} + C_{r,2}} \tag{4.4}$$

where C_1 and C_2 are the equivalent capacitance of each side of the MFT. Now, the total equivalent capacitance, reflected to the primary, can be written as:

$$C_{tot} = \frac{C_1 \times C_2'}{C_1 + C_2'} = \frac{C_1 \times \frac{C_2}{a^2}}{C_1 + \frac{C_2}{a^2}} = \frac{\left(\frac{2C_{dc,1} \times C_{r,1}}{2C_{dc,1} + C_{r,1}}\right) \times \left(\frac{1}{a^2} \frac{2C_{dc,2} \times C_{r,2}}{2C_{dc,2} + C_{r,2}}\right)}{\left(\frac{2C_{dc,1} \times C_{r,1}}{2C_{dc,1} + C_{r,1}}\right) + \left(\frac{1}{a^2} \frac{2C_{dc,2} \times C_{r,2}}{2C_{dc,2} + C_{r,2}}\right)}, \tag{4.5}$$

$$C_{tot} = \frac{2C_{dc,1}2C_{dc,2}C_{r,1}C_{r,2}}{2C_{dc,1}2C_{dc,2}C_{r,2} + 2C_{dc,2}C_{r,1}C_{r,2} + 2C_{dc,1}2C_{dc,2}C_{r,1}a^2 + 2C_{dc,1}C_{r,1}C_{r,2}a^2} \tag{4.6}$$

Thus, (4.6) is the generic equation for the equivalent capacitance which contributes to determining the resonance frequency. From this equation, some simplifications can be applied considering the available MFT configurations:

- For $a = 1$

$$C_{tot}|_{1:1} = \frac{C_{r,1}C_{r,2}}{C_{r,1} + C_{r,2} + C_{r,1}C_{r,2}\left(\frac{1}{2C_{dc,1}} + \frac{1}{2C_{dc,2}}\right)} \tag{4.7}$$

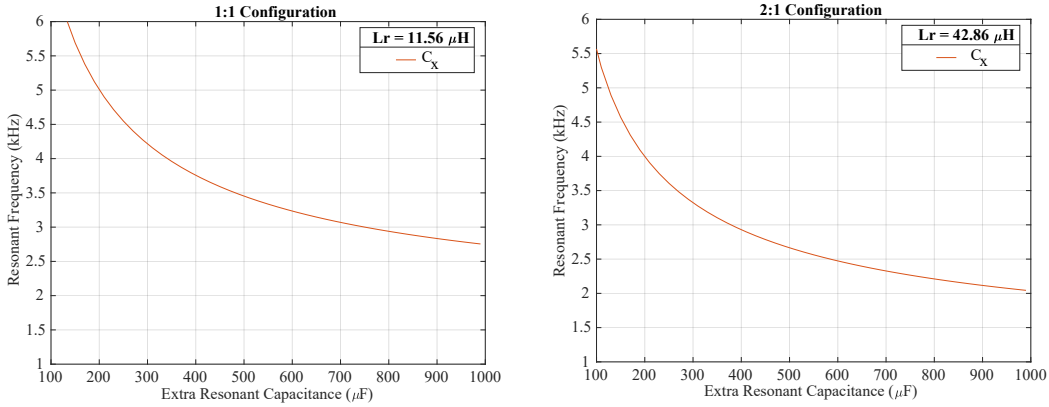
  and, if it is considered that the resonant capacitor is added on both sides of the MFT and has the same value C_x, the equation becomes:

$$C_{tot}|_{1:1} = \frac{C_x}{\frac{2C_{dc,1}+2C_{dc,2}}{2C_{dc,1}2C_{dc,2}}C_x + 2} \tag{4.8}$$

- For $a = 2$

$$C_{tot}|_{2:1} = \frac{C_{r,1}C_{r,2}}{4C_{r,1} + C_{r,2} + C_{r,1}C_{r,2}\left(\frac{1}{2C_{dc,1}} + \frac{4}{2C_{dc,2}}\right)} \tag{4.9}$$

  and, if it is considered that both resonant capacitors will have the same value C_x, the equation becomes:



(a) (b)

Fig. 4.5 Required extra capacitance considering the same value of capacitor at each side, to reach a desired resonant frequency for the (a) 1 : 1 turns-ratio configuration and (b) 2 : 1 turns-ratio configuration.

$$C_{tot}|_{2:1} = \frac{C_x}{\frac{8C_{dc,1}2C_{dc,2}}{2C_{dc,1}+2C_{dc,2}}C_x + 5} \tag{4.10}$$

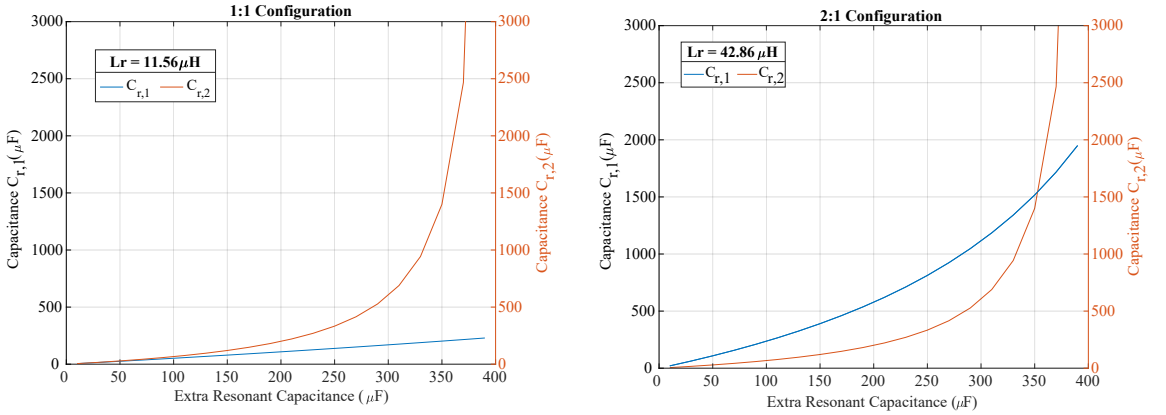
With the C_{tot} equations, one can find the value of the resonant capacitor for the desired resonant frequency. Further, to select a combination of resonant capacitors which would result in the same equivalent capacitance for each side of the MFT, i.e. $C_1 = C_2$, a second equation is created.

$$C_1 = C_2 \rightarrow \frac{2C_{dc,1} \times C_{r,1}}{2C_{dc,1} + C_{r,1}} = \frac{2C_{dc,2} \times C_{r,2}}{2C_{dc,2} + C_{r,2}} \rightarrow 2C_{dc,2}C_{r,2}(2C_{dc,1}+C_{r,1}) = 2C_{dc,1}C_{r,1}a^2(2C_{dc,2}+C_{r,2}) \tag{4.11}$$

In this way, (4.6) and (4.11) create a system of equations to find the combination of the resonant capacitor to have the same total equivalent capacitance for each side.

Firstly, **Fig. 4.5** shows the equivalent extra capacitance required to realize a desired resonant frequency, considering the same value of capacitor on each side, for the 1 : 1 turns-ratio configuration (**Fig. 4.5a**) and the 2 : 1 turns-ratio configuration (**Fig. 4.5b**). It can be seen that the total resonant capacitance to realize 5 kHz resonant frequency is around $C_x = 200$ μF for the 1 : 1 turns-ratio configuration and around $C_x = 125$ μF for the 2 : 1 turns-ratio configuration. With this information, any combination of extra capacitors added to the resonant tank that results in this specific capacitance would meet the requirement for the resonant frequency.

However, if it is desired to have the same equivalent capacitance value for each side of the MFT (i.e. $C_1 = C_2$), each resonant capacitor needs to combine and compensate the DC-link capacitance. Thus, **Fig. 4.6** shows the possible combinations for low values of extra resonant capacitance for the two possible MFT configurations under analysis. To fulfill this requirement, the extra capacitance on the secondary side needs to be much higher due to the already high capacitance values of the DC-link.



(a) (b)

Fig. 4.6 Capacitance value of each resonant capacitor considering same equivalent capacitance at each side of the MFT. (a) Capacitance values for $1:1$ turns-ratio configuration, and (b) Capacitance values for $2:1$ turns-ratio configuration.

After a requirement of $C_x = 350\mu$F of extra capacitance, the capacitance value for the secondary becomes too high, making its implementation more challenging.

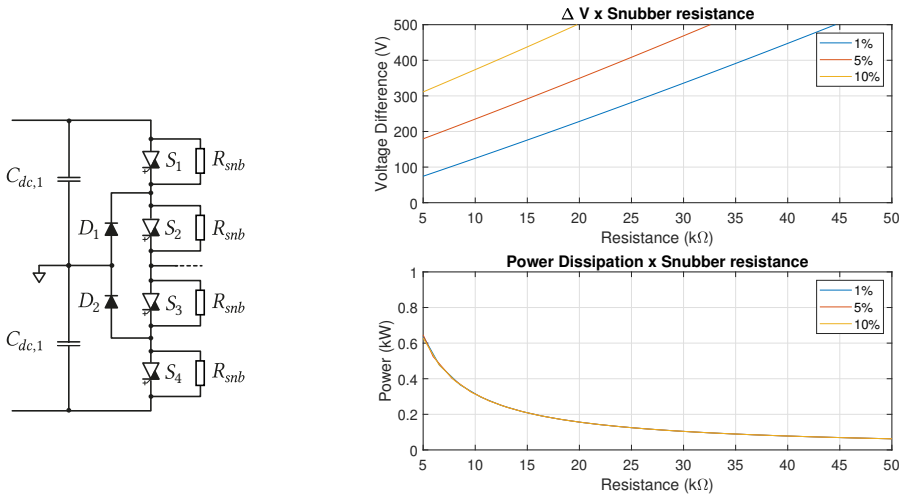
Ultimately, by knowing the required extra capacitance to be added to the circuit, different resonant frequencies can be realized to have a good frequency ratio. For a switching frequency of 5 kHz, and a $1:1$ turns-ratio configuration, the selected extra capacitance is $C_x = 122\ \mu$F resulting in a frequency ratio of $f_n = 1.2$.

4.3 Static Voltage Balancing

The 3L operation of the 3L-NPC plays a crucial role in the protection of the DCT, providing soft-start and current-limiting capabilities. Nevertheless, during regular operation, the power stage operates in a 2L, 50% duty cycle to drive the resonant tank. This means that the zero state is bypassed, and the NPC operates with the two upper and two lower IGCTs complementary. In this way, the IGCTs are essentially connected in series, and therefore, both the dynamic and static voltage balancing need to be investigated.

In contrast to IGBTs, which can take advantage of active voltage balancing, series-connected IGCTs rely on snubbers and balancing resistors to ensure both dynamic and static voltage sharing. For static voltage balancing, the snubber is specifically designed to ensure the switches operate safely during blocking periods.

In this thesis, two methods for static voltage balancing are evaluated. The first one is the use of the resistors in parallel with each power switch. This approach is both effective and straightforward for addressing the issue. However, it requires an individual resistor for each device, leading to increased power losses. The second method uses a single resistor in parallel to the inner two IGCTs of the NPC-leg, solving the static voltage balancing with only one resistor, benefiting from the lower losses.



(a) (b)

Fig. 4.7 (a) Schematic of the parallel resistor snubber. (b) Pertinent plots for the resistor design with different resistance tolerances. On top the expected/allowed voltage unbalance is shown and below the total corresponding power dissipation of the selected resistor is given.

4.3.1 Parallel resistor

The static voltage balancing resistors ensure voltage balance across the series-connected devices by conducting a current greater than the maximum leakage current of these devices. Specifically, in this scenario, the resistors are required to carry a current that exceeds the leakage current of the RC-IGCTs and their antiparallel diodes when they are in the OFF state.

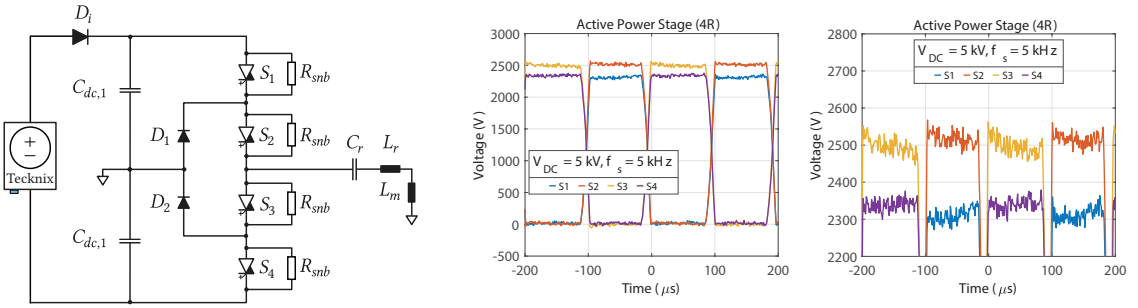
A sizing rule for these resistors is derived in [109], where the resistor value is sized considering the allowed voltage difference between the series connected devices, and the resistance tolerance of the resistors. This sizing rule leads to the following relationship:

$$\Delta V = \frac{V_{op} + \Delta V}{R_{snb} + \Delta R}\Delta R + I'_{leak,0}(R_{snb} + \Delta R) \tag{4.12}$$

where $I'_{leak,0}$ is the maximum leakage current of the devices at the operating voltage V_{op}, R_{snb} and ΔR are the values of the balancing resistor and its tolerance ($1\% \longrightarrow \Delta R = R \times 0.01$), and ΔV is the maximum voltage deviation between the series connected devices. To correlate the leakage current with the actual operating voltage, the leakage current is,

$$I'_{leak,0} = \hat{I}_{leak,0}\sqrt{\frac{\frac{V_{op}}{n} + \frac{\Delta V}{n-1}}{V_{IGCT,0}}} \tag{4.13}$$

where $\hat{I}_{leak,0}$ is the maximum leakage current of the device, n is the number of series connected devices,



(a) (b)

Fig. 4.8 Individual test of four parallel resistors. (a) Schematic of the test, (b) experimental waveforms of the voltages across the IGCTs, at 5 kV and 5 kHz. The dead time was set to 30μs, and a C-snubber of 20nF was used for the dynamic voltage balancing.

and $V_{IGCT,0}$ is the reference voltage of the IGCT test. For the device in question, the $\hat{I}_{leak,0} = 20$ mA at $V_{IGCT,0} = 5.5$ kV.

Thus, this equation can be solved and the relationship between the allowed voltage deviation and the resistance value can be drawn. **Fig. 4.7a** shows the schematic of the power stage with the resistors in parallel, and **Fig. 4.7b** shows the resistance value versus the voltage deviation for different tolerances. At the bottom of **Fig. 4.7b**, the power dissipation shows the power dissipation of a single device for half of the period when the current is flowing throughout the resistance.

From this plot, a resistor can be selected to maintain the difference between the voltages of the IGCTs below 10% of the DC-link voltage ($\Delta V = 500$ V for the $V_{DC} = 5$ kV DC-link). Thus, a value of $R_{snb} = 10$ kΩ with a 5% tolerance is selected to have a safe margin. With this resistor, the static balancing resistor will dissipate $P_{snb} = 4 \times 320$ W $= 1280$ W in total per stack.

This solution was experimentally tested with the prototype. The experiment proceeds by connecting the power stage to the 5 kV supply with the secondary disconnected as shown in **Fig. 4.8a**. In **Fig. 4.8b** one can see the experimental results for the balancing resistors operating with 5 kV, 5 kHz. It shows the voltage across the IGCTs and a zoom-in on the voltage difference during the blocking period. The voltage difference was as expected and around $\Delta V = 200$ V.

4.3.2 Symmetrizing resistor

Taking advantage of the NPC-leg, which has the clamping diodes between the devices and the neutral point, a single symmetrizing resistor can be used for static voltage balancing. The resistor is positioned in parallel to the inner two IGCTs of the NPC-leg. Differently, from the previous strategy, this resistor needs to compensate only the leakage current difference of the devices. **Fig. 4.9** illustrates the role of the clamping diode on the static voltage balancing, and **Fig. 4.10** illustrates the role of the symmetrizing resistor.

Firstly, **Fig. 4.9** shows an illustration when S_1 and S_2 are blocking, and the device S_2 has a higher leakage current. In this case, the voltage on S_2 will decrease and forward bias the clamping diode D_1. Consequently, an extra current will flow to compensate for the leakage current, and voltage S_2 is clamped to the capacitor voltage $C_{dc,2}$, approximately $V_{dc}/2$.

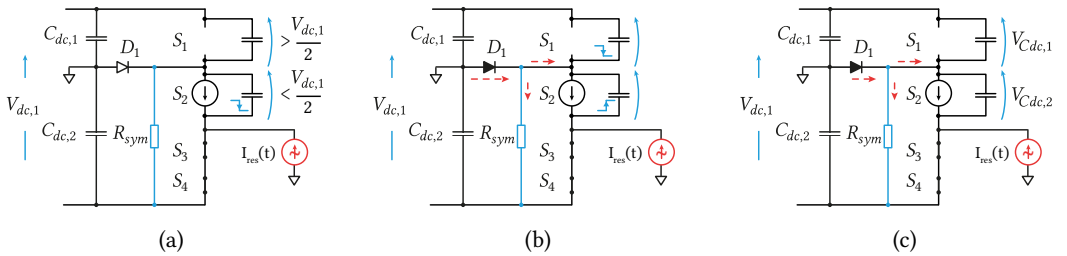


Fig. 4.9 Illustrative example of the clamping diode acting when S_2 has a higher leakage current. (a) Leakage current of S_2 discharges the output capacitance and the S_2 voltage decreases, while the S_1 voltage starts increasing and can reach a destructive level. (b) The diode is forward-biased and provides a current path. (c) The voltage of S_2 is clamped to $C_{dc,2}$ voltage, approximately $V_{dc}/2$.

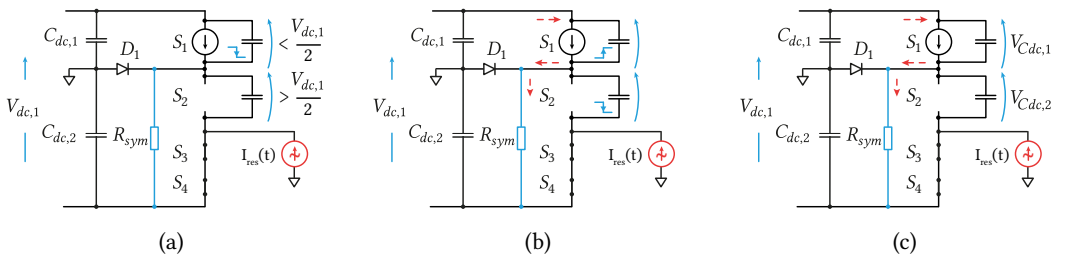


Fig. 4.10 Illustrative example for the basic principles of the static voltage balance with an NPC symmetrizing resistor. The case when the device S_1 has a higher leakage current. (a) Leakage current of S_1 discharges the output capacitance and voltage of S_1 starts increasing, potentially reaching destructive levels. (b) The resistor R_{sym} provides an extra current path so that the leakage current of S_2 and current through R_{sym} are bigger than the leakage of S_1. Hence, R_{sym} handles the difference between leakage current mismatch. (c) The voltage of S_1 is clamped to $C_{dc,1}$ voltage, approximately $V_{dc}/2$.

On the other hand, **Fig. 4.10** shows the case when the device S_1 has a higher leakage current. In this case, the voltage of S_1 will decrease and the diode will not forward-bias itself, but the symmetrizing resistor will provide the current path to compensate for the leakage current, preventing voltage across S_2 from reaching destructive voltage levels. This current should be big enough to properly compensate for the higher leakage current value of S_1.

Consequently, following immediately this case, the sizing rule of the symmetrizing resistor can be drawn. **Fig. 4.11** shows a more detailed illustration relevant to the derivation of the sizing rule. Firstly, it is known that the voltage difference given by the leakage current flowing to the adjacent device and charging the output capacitance is in the form of,

$$\Delta V = \frac{1}{C_{out}} I_u T_s, \tag{4.14}$$

where I_u is the surplus current from the leakage current flowing to the other device. Also, by a current divider, this current correlates to the leakage current by,

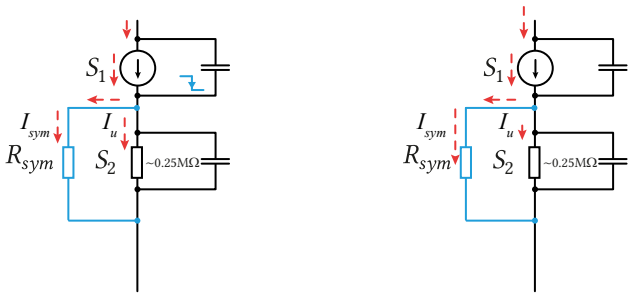


Fig. 4.11 Illustration on the procedure to compute the symmetrizing resistor for the voltage static balancing of the switches. (a) Improper design using a resistance value too high leads to low current flow throughout its branch. (b) Proper design allows the majority of the current to flow throughout the resistor branch.

$$I_u = \frac{R_{sym}}{R_{sym} + R_{leak,s2}} \hat{I}'_{leak,0} \tag{4.15}$$

where R_{sym} is the symmetrizing resistance, $R_{leak,s2}$ is the equivalent leakage current resistance for the operating voltage given by (4.16), and $\hat{I}_{leak,0}$ is the leakage current.

$$R_{leak,S2} = \frac{V_{dc}}{2\hat{I}_{leak,0}} \tag{4.16}$$

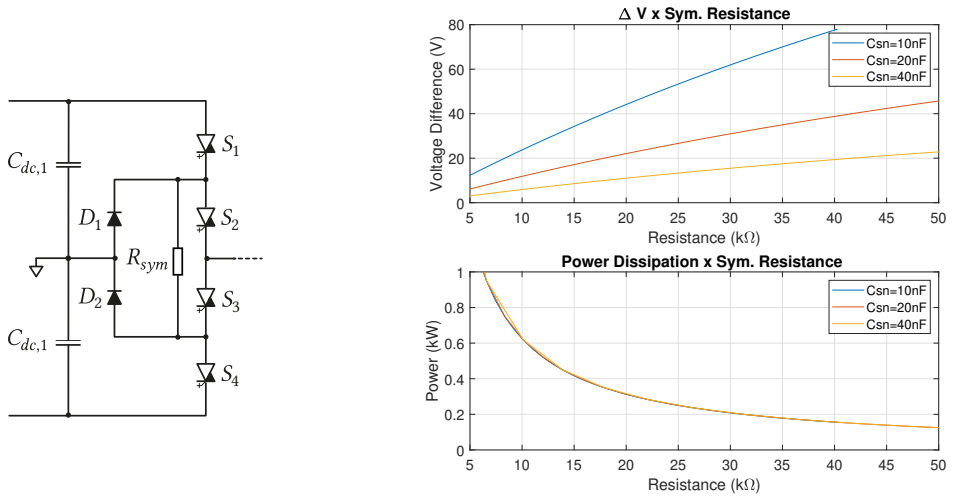
Finally, substituting (4.15) in (4.14) it yields,

$$\frac{\Delta V C_{out}}{T_s} = \frac{R_{sym}}{R_{sym} + R_{leak,S2}} \hat{I}_{leak,0} \rightarrow \Delta V = \frac{R_{sym}}{R_{sym} + \frac{V_{dc}}{2I'_{leak,0}}} \frac{I'_{leak,0} T_s}{C_{out}} \tag{4.17}$$

Thus, (4.17) relates the voltage difference between the devices and the resistance value of the symmetrizing resistance depending on the capacitance value in parallel with the device. This capacitance value impacts the rate of change to discharge the voltage with the leakage current. In (4.17) this capacitance is written as C_{out}, being the output capacitance of the device; however, if a snubber is included, it should be considered for proper calculation.

Fig. 4.12a shows the schematic of the 3L-NPC using a symmetrizing resistor and **Fig. 4.12b** shows the design of the symmetrizing resistor using (4.17). At the bottom of **Fig. 4.12b**, the power dissipation is shown for the symmetrizing resistor. Using this plot, the resistance value is chosen to be $R_{sym} = 20\,\text{k}\Omega$ resulting in a power consumption of $P_{Rsym} = 320$ W per stack.

This resistor was tested with MV DCT prototype by supplying the 5kV stack with the secondary disconnected as shown in **Fig. 4.13a**. **Fig. 4.13b** shows the experimental results for the voltage across the IGCTs during the 2L operation with 5kV and 5kHz. It can be seen that in this case, the voltage unbalance was mitigated by the snubber.



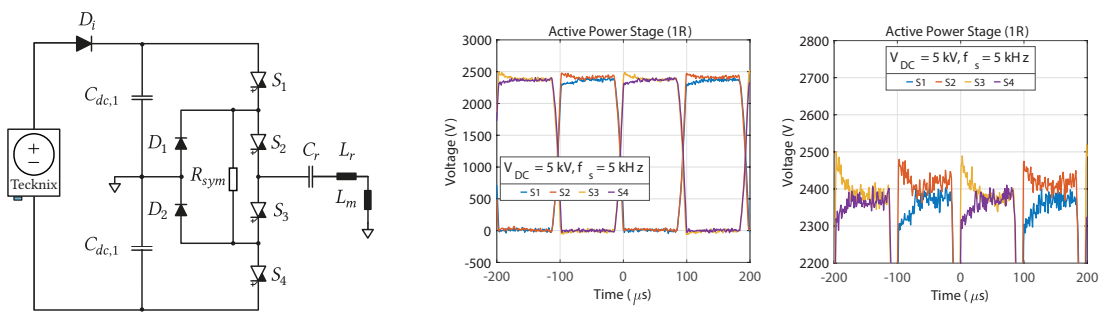
(a) (b)

Fig. 4.12 (a) Schematic of the 3L-NPC with symmetrizing resistor. (b) Pertinent plots for the symmetrizing resistor design. On top of the expected/allowed voltage unbalance and below the total corresponding power dissipation of the selected resistor.

4.3.3 Comparison of the two static voltage balancing strategies

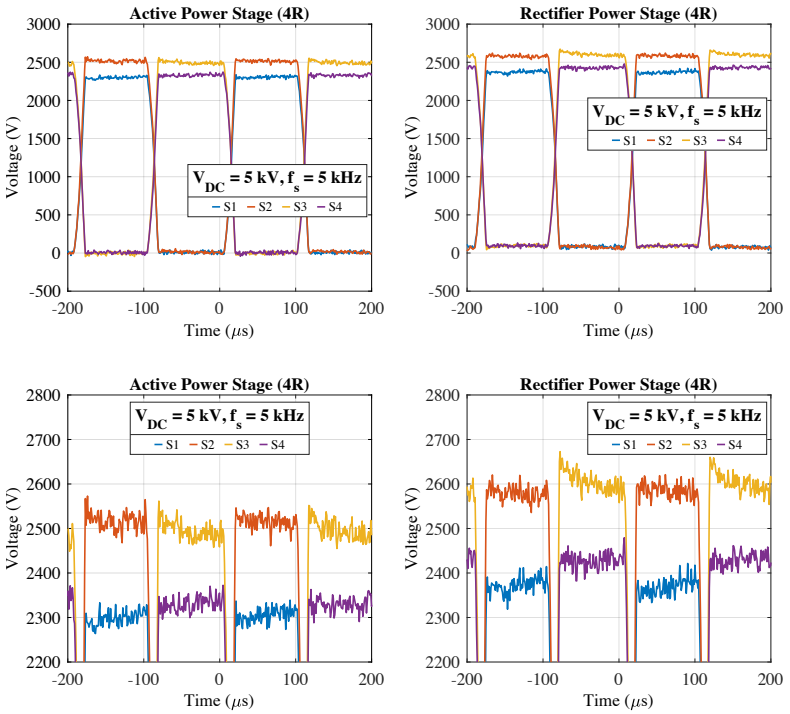
The two previously discussed strategies were implemented in the active and passive power stages to test their performance. The experiments were carried out by operating the DCT with the 5kV input voltage, in a 1 : 1 turns-ratio configuration, with the primary power stage active with a 50% duty cycle, and using the secondary power stage as a passive rectifier with no load.

Fig. 4.14 shows the experimental results for the voltage across the IGCTs, from the active and passive side for the 5 kV and 5 kHz operation. **Fig. 4.14a** shows the experimental waveforms for the balancing resistor, with 10 kΩ resistor.

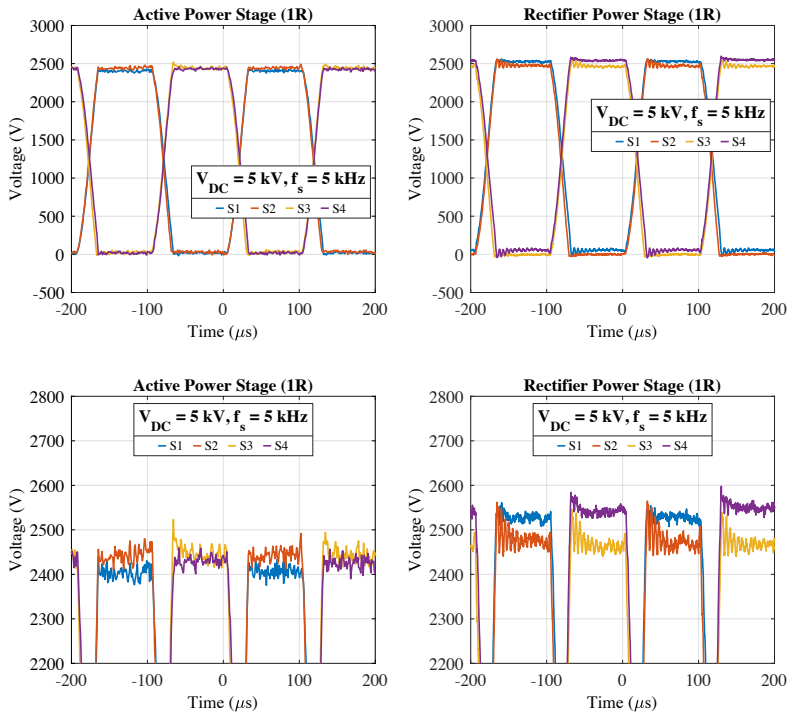


(a) (b)

Fig. 4.13 Individual test of a single symmetrizing resistor. (a) Schematic of the test, (b) experimental waveforms of the voltages across the IGCTs, at 5 kV and 5 kHz. The dead time was set to 30μs and a C-snubber of 20nF was used in parallel with the IGCTs for the dynamic voltage balancing.



(a)



(b)

Fig. 4.14 Experimental waveform of the voltage across the IGCTs for the active and passive stack for the 5 kV and 5 kHz no-load operation. (a) Parallel resistor (b) NPC symmetrizing resistor. The slightly higher voltage level of the secondary side is a result of no load condition with the output capacitor connected.

Tab. 4.4 Comparison between R_{sym} and R_{snb}.

	NPC-Symmetrizing Resistor	Paralleling Resistor
Losses per stack	340 W	1260 W
ΔV of Active stack	41 V	182 V
ΔV of Passive stack	76 V	219 V
Cost per stack	228 $	456 $

By using the four parallel resistors at each stack, the snubber consumes in total $P_{snb,tot} = 2 \times 1280 = 2560$ W, having a voltage difference of approximately 200 V. This power dissipation represents 0.256% of the nominal power (1 MW).

Now, **Fig. 4.14b** shows the experimental results using the NPC symmetrizing resistor. A 20 kΩ was used which results in a total of $P_{snb,tot} = 2 \times 320 = 640$ W, with a voltage difference around 50V at the secondary. The power dissipation represents 0.064% of the nominal power. Although the power consumption of this snubber is already much lower than the other strategy, this experiment shows that the resistance value could be increased even further to reduce the losses and allow a higher voltage difference between the IGCTs.

In conclusion, the NPC symmetrizing resistor is a better solution in terms of performance, cost, and losses. This is mostly due to the use of one versus four resistors of the parallel resistor solution. The resistors used are compared, and **Tab. 4.4** shows the side-by-side comparison.

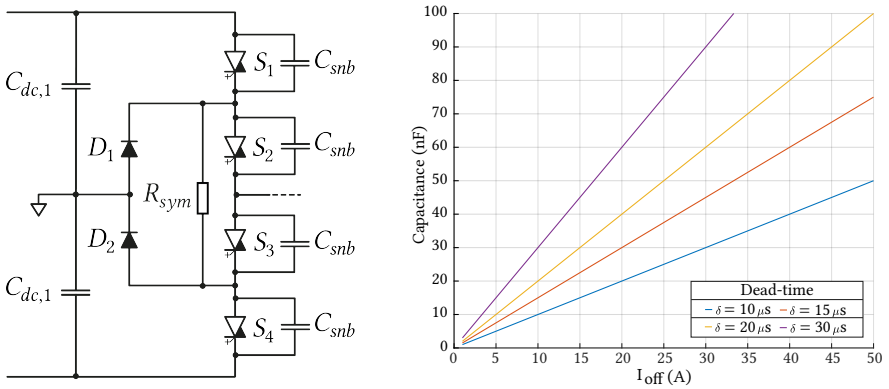
4.4 Dynamic voltage balancing

The dynamic voltage balancing is designed to ensure safe operation during the switching transitions. The sizing of the snubber for the series connected IGCTs is affected by both the maximum acceptable dynamic voltage imbalance, and by the expected turn-off current level. The main question when considering the IGCT-based DCT under investigation is: How to deal with the series connected IGCTs with the low turn-off current and the medium frequency switching?

Indeed such conditions are special and different from the usual low-frequency switching and hard-switching applications. With the low turn-off current, the voltage rise time increases drastically, due to the small rate of change of the current. Further, the sum of the gate unit delay and voltage rise (around $t_{delay} + t_{rise} = 15$ μs [110]), falls into a comparable range of the available switching period of 100 μs per state.

Nevertheless, compared to the usual RCD snubber required for hard-switching applications, the soft-switching conditions bring the possibility to simplify the dynamic balancing circuit. Firstly, as the switching transients happen with ZVS and QZCS, there is no danger linked to the discharge of the snubber capacitance into the device about to turn ON. Consequently, a purely capacitive snubber is enough for this application bringing advantages such as size, cost, and efficiency. **Fig. 4.15a** shows capacitor snubbers in parallel with the IGCTs.

In this way, the capacitor snubber should be designed to have the transitions as fast as possible. Assuming that the IGCT output capacitance is negligible, the maximum snubber capacitance can be found by:



(a) (b)

Fig. 4.15 (a) 3L-NPC leg with C snubber (b) Maximum snubber capacitance vs turn-off current for different dead time values.

$$C_{snb,max} = \frac{i_{off} \cdot t_{dt} \cdot n}{4V_{dc}} \tag{4.18}$$

where i_{off} is the IGCT turn off current, t_{dt} is the dead-time, V_{dc} is the DC voltage and n the number of series connected IGCTs. **Fig. 4.15b** shows the relationship between the maximum capacitance value and turn-off current for different dead times. This plot shows the maximum capacitance value, for a given current to perform a safe ZVS. If this criterion is not fulfilled, the ZVS will be lost and extra losses due to partial shoot-through will appear [108].

Thus, knowing that the worst scenario has a turn-off current of $I_{off} \approx 10$ A, a $C_{snb} = 20$ nF was selected to ensure the dynamic voltage balance of the stack. With this capacitance and this turn-off current, the dead time needs to be set as $\delta \geq 20\ \mu$s, therefore, a $\delta = 25\ \mu$s was used.

Fig. 4.16 shows the switching transition of the IGCTs using a $C_{snb} = 20$ nF snubber, for different turn-off currents. Concerning the blue waveform is the 5 kV, 5 kHz operation. For this case, it can be seen that the turn-off current is $I_{off} \approx 8$ A, which results in a transition time of 19μs. The voltage mismatch after the first IGCT is closed is around 350 V. This experiment verified that the low turn-off current leads to a very slow transition, consequently, requiring a very conservative dead time. A dead time of $\delta = 25\ \mu$s consists of 25% of the switching period, leaving only 75% of the switching period for transferring power, which is not ideal for the converter operation.

Therefore, other switching frequencies were tested to evaluate the switching transient with different turn-off currents. The switching frequencies of $f_s = 4$ kHz and $f_s = 3$ kHz were tested and the experimental waveforms are also shown in **Fig. 4.16**, in yellow and green, respectively. For the case of $f_s = 4$ kHz the turn-off, the current is $I_{off} \approx 11$ A, resulting in approximately 16 μs for the transition, and a voltage imbalance of 300 V. Lastly, for $f_s = 3$ kHz, the turn-off current is $I_{off} \approx 17$ A, and the transition period is 13μs. This operation led to a voltage imbalance of 250 V.

It can be noticed that with a lower switching frequency, which results in a higher turn-off current, the transition duration is shorter. Further, a lower value of the snubber capacitor could be used in an attempt to speed up the transition even more. The minimum required capacitance value to achieve

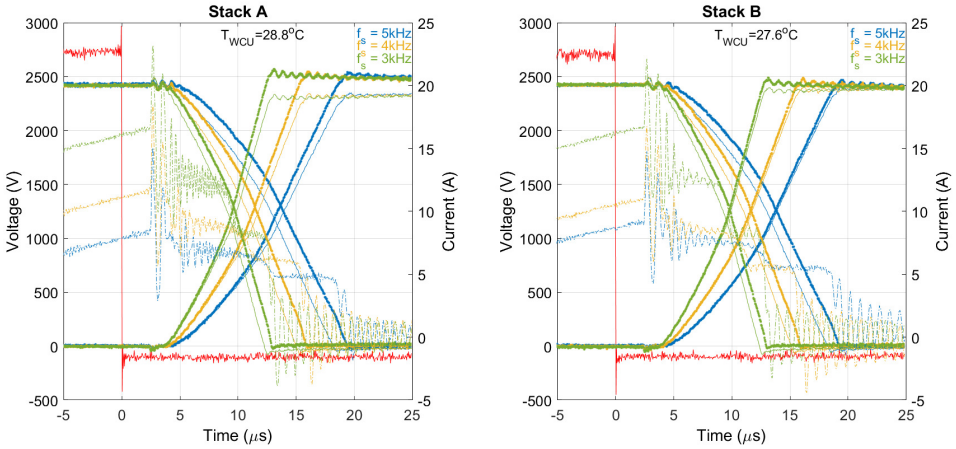


Fig. 4.16 Experimental waveforms for the 2L transition with a $C_{snb} = 20$ nF snubber, with different switching frequencies. The thick lines represent the outer device (S_1 and S_4), and the light line the inner device (S_2 and S_3). The solid lines are the voltages over the IGCTs and the dash-dotted lines are the currents. Stack A and Stack B represent the primary and secondary stacks. The red pulse is the turn-off signal.

dynamic voltage balance is such that all IGCTs possess the same equivalent parallel capacitance, which includes the device output capacitance and snubber capacitance.

Finally, the dynamic voltage balancing with a C-snubber was validated for the no-load operation with the two 3L-NPC stacks. These experiments were carried out with an NPC symmetrizing resistor of $R_{sym} = 20$ kΩ for the static voltage balancing.

4.5 Summary and Conclusion

This chapter described the MV DCT prototype and the design of the resonant tank. Furthermore, the MV DCT was used to perform experiments toward the commissioning of the power stages with the MFT integrated into the setup. It has been demonstrated that the development of an MV DCT encompasses a diverse range of power electronics aspects, highlighting the essential need for a well-organized and meticulously planned development approach.

In this chapter, the IGCT-based split capacitor 3L-NPC DCT was fully assembled, and it focused on investigating both static and dynamic voltage balancing. Firstly, two strategies of static voltage balancing were evaluated, the parallel resistor snubber and the NPC symmetrizing resistor. The investigation has shown that the NPC symmetrizing resistor snubber is as effective as the parallel resistor snubber, offering the advantage of using a single resistor compared to four in the alternative solution. Consequently, it successfully achieves static voltage balancing with lower losses.

Later, the C-snubber was tested and computed for the dynamic voltage balancing. Experimental results demonstrated that the very low value of the C-snubber is sufficient to ensure a safe dynamic transition thanks to the very low turn-off current. The switching transients were explored for different turn-off currents, indicating a potential for a faster transition - more suitable for a better use of the resonant conversion. However, extra validation is required during load operation.

Finally, experiments involving the prototype under load were not performed due to a combination

of encountered damages and delays in the production of new devices. The encountered damages raised concerns about the requirements for additional protection circuits in the setup. As a result, the decision was made to postpone subsequent experiments until the damages were repaired, and new protection elements were added.

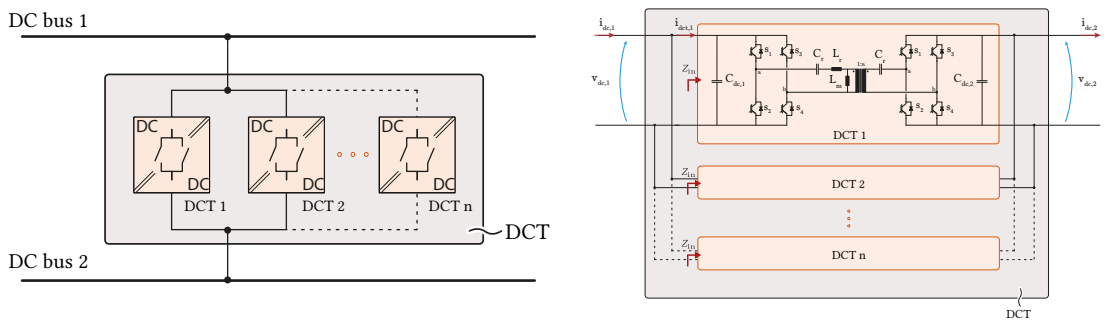
5

Parallel Operation of Direct Current Transformers

To achieve scalability in terms of power increase for the same input/output voltages, one option is to connect several DCTs in parallel. This approach eliminates the necessity to redesign an entire converter for higher power while still allowing for an increase in the power rating of the connection between the two DC buses. However, as no closed-control loop is available and the converter is sensitive to parameter variations, ways to assess and solve the current sharing unbalance are required. This chapter analyses the parallel operation of DCTs based on the DCT's input impedance. It investigates the resonant parameters' sensitivity and proposes a solution to alter the input impedance using the switching frequency and improve the current sharing.

5.1 Parallel Connection of Power Converters

Having a converter design, power hardware, and control method that facilitates easy paralleling can offer significant advantages to the application by providing flexibility to create new systems while using the same building block. The primary benefit of connecting power converter modules in parallel is the ability to increase the overall power ratings of the system, given that the converter can be operated and each module shares the current properly.



(a) (b)

Fig. 5.1 (a) A high-power DCT composed of several DCTs operating in parallel. Every DCT operates in an open loop. (b) Details on the arrangement of several DCTs connected in parallel.

The parallel operation of converters has been extensively analyzed and demonstrated for different converters topologies [111], [112]. With this configuration, the building block can be connected in parallel keeping the same operational principle [71] (as illustrated in **Fig. 5.1**). However, in practice, every parallel module is likely slightly different due to variations and tolerances of parameters, which

creates a natural power/current unbalance between the modules. In this way, the parallel operation brings challenges around the parameter variation and the converter interaction that need to be addressed to ensure a satisfying current sharing.

In the literature, the active methods are based on the use of control loops, adjusting the switching frequency or resonant parameters by detecting the current of each module and realizing a satisfactory current sharing. For instance, in [113] and [114] the current feedback is used to adjust the power of each converter ensuring the correct current sharing. In [115] current sharing problem is solved by using a switch-controlled capacitor to modulate the voltage gain of individual power converters.

Different approaches rely on the passive solutions by means of hardware integration or as a complete integrated design with multi-winding transformer [116]–[118]. The main advantage of these methods is the absence of current measurements to ensure the current sharing, but they require extra elements and internal connection between modules.

All the mentioned solutions perform the analysis aiming to draw design rules and promote correction on the current sharing unbalance using the available degrees of freedom (e.g. control, hardware changes, etc. [119]–[124].) However, when considering the DCT, it is assumed that each module operates in an open loop at the fixed switching frequency, without any connection in the resonant tank between the paralleled modules as in [119]. Thus, the converter characteristics dictate the current sharing unbalance and the feasibility of parallel connection, which must be understood, modeled, and eventually controlled.

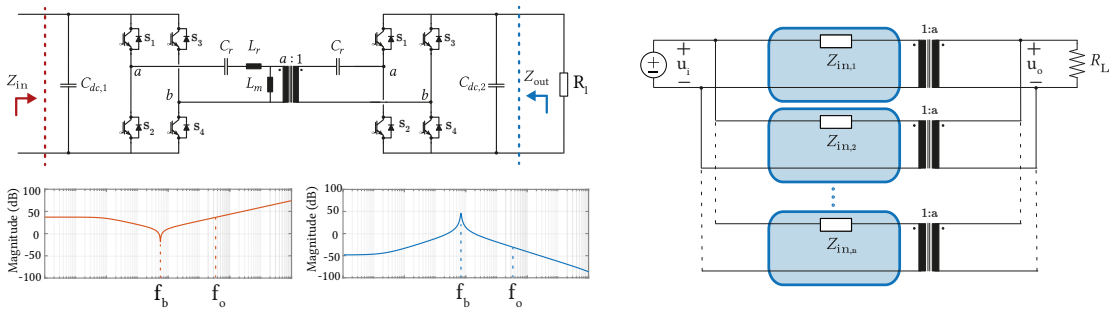
To quantify this analysis, the next section analyses the input impedance to evaluate the viability of parallel operation of DCTs. Firstly, the parallel connection of the DCTs is analyzed by considering all combinations of parameter variations, in certain ranges. Secondly, the current sharing unbalance is mapped and predicted in order to ensure the operation of DCT within the requirements. And finally, if the predicted current sharing unbalance satisfies the requirements (e.g. being less than tolerated or within ratings of each DCT module), the high-power DCT can be operated with the selected design constraints.

5.2 Sensitivity Analysis of the Input Impedance of DCT

The sensitivity analysis of the input impedance is performed using the small signal model to highlight the impact of each contributor on the input impedance and the current sharing performance. The input impedance has been the focus of works related to stability analysis, as in [125], however, it can also be used for current sharing prediction. In fact, either the input or the output impedance could be used to evaluate the power-sharing of parallel connected DCTs, as open loop operation is considered. From one side, the output impedance defines the contribution of each DCT block to provide current to the output load. And from the other side, the input impedance indicates how much current is taken from the primary source. **Fig. 5.2a** shows an illustration of input/output impedance.

There are several types of variations that occur on a DCT that impact the impedance, two of them are: i) resonant tank parameters variations, and ii) switching frequency. In this sense, the impedance of the DCT can be described as a function of all of these parameters,

$$Z_{in}(\omega) = f(L_r, C_r, L_m, f_s, R_l, R_{losses}). \tag{5.1}$$



(a) (b)

Fig. 5.2 (a) DCT circuit and illustration of the input impedance vs output impedance for the sub-resonant operation, adapted from [81]. f_0 is the resonant frequency, and f_b is the beat frequency pole given by $L_r\left(1+(\omega_0/\omega_s)^2\right)$ and output capacitor C_{dc}. (b) Resultant input impedance circuit of the converter with ideal transformer representation when paralleling several modules.

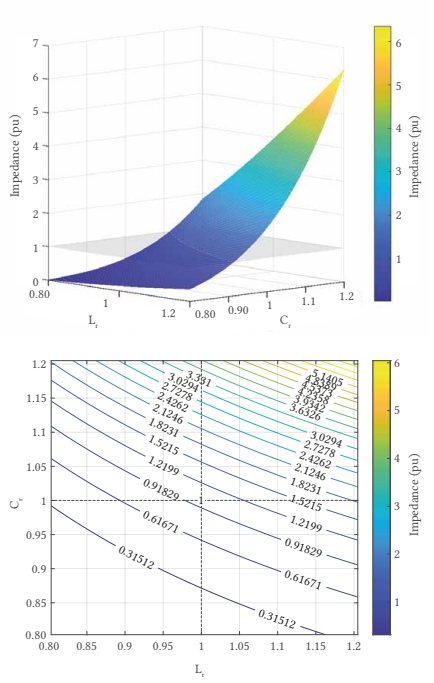
The analysis is performed with normalized values in order to make it as general as possible, and the impedance is computed at the switching frequency, where the power is transferred. And, to represent results more clearly, the leakage inductance and resonant capacitance are the bases of the input impedance surface. The base parameters used are presented in **Tab. 5.1** (the same as for the LV DCT 1 prototype), and the range of values for each of the allowed tolerances under analysis is detailed in **Tab. 5.2**. Thus, **Fig. 5.3** shows the resulting input impedance at switching frequency for an allowed parameters variation of ±20%, ±10%, ±5%, ±1% on L_r and C_r.

Tab. 5.1 Base DCT parameters.

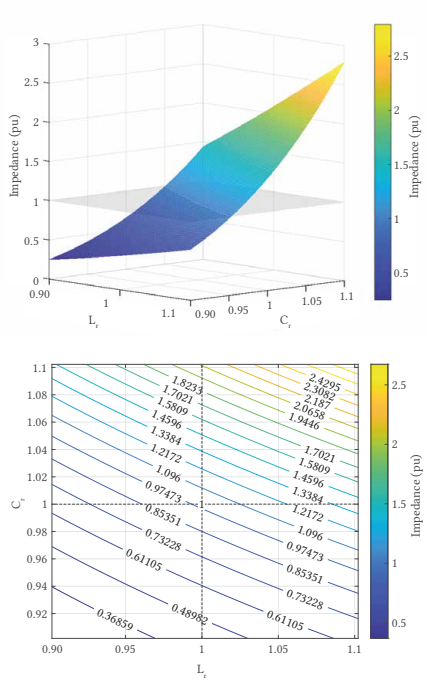
Description	Symbol (Unit)	DCT
DC Voltage 1	$V_{\mathrm{dc},1}$ (V)	750
Turns ratio	a	1
Load	P_{dc} (kW)	50
Switching frequency	f_{sw} (kHz)	10
Magnetizing inductance	L_{m} (μH)	750
Leakage inductance	L_{r} (μH)	11.6
Resonant Capacitor	C_{r} (μF)	37.5

Tab. 5.2 Range of parameter variation around the rated value for sensitivity analysis.

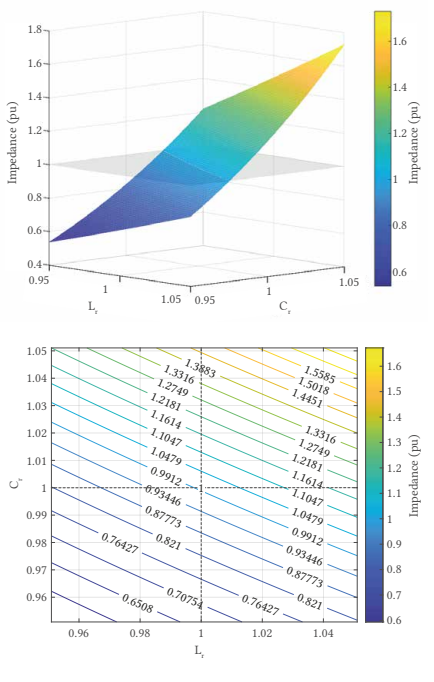
Tol	L_r (μH)	C_r (μF)	L_m (μH)	f_s (kHz)
Rated	11.6	37.5	750	10
±20%	9.28↔13.92	30↔45	-	-
±15%	9.86↔13.34	31.875↔43.125	-	-
±10%	10.44↔12.76	33.75↔41.25	675, 750, 825	9, 10, 11
±5%	11.02↔12.18	35.62↔39.37	-	-
±1%	11.48↔11.71	37.12↔37.87	-	-



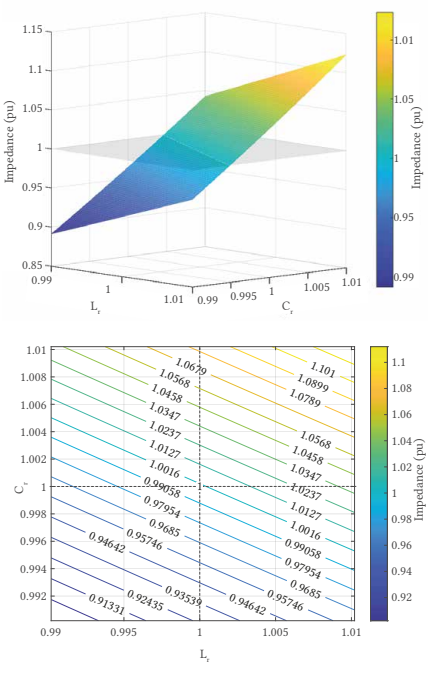
(a) ±20%



(b) ±10%



(c) ±5%



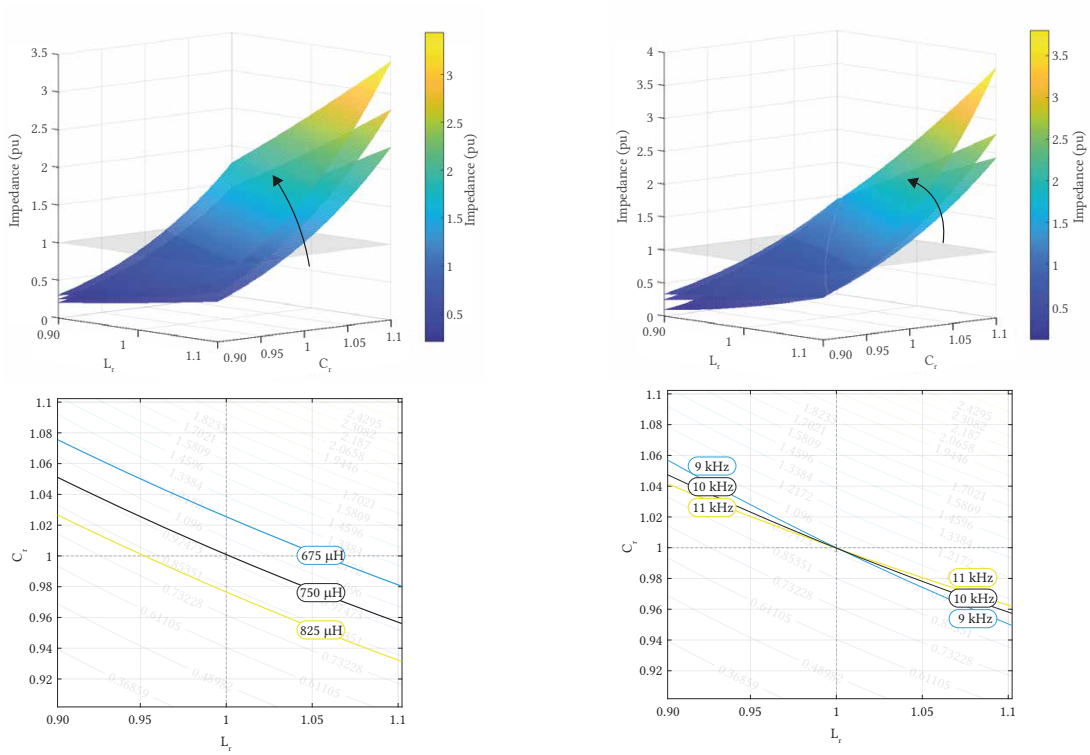
(d) ±1%

Fig. 5.3 Magnitude of the input impedance at the switching frequency for different L_r and C_r tolerance. In (a) allowed variation of ±20% can lead to a maximum variation of 7 times the rated value; in (b) ±10% with a maximum variation of almost 3 times; in (c) ±5% with a maximum variation of almost 1.8 times; and (d) ±1% with a maximum variation of almost 1.15 times. The unity plane represents the impedance having the same value as the base values. The contour plot details the variation of the input impedance.

With a tolerance of ±20% on L_r and C_r, as shown in **Fig. 5.3a**, the value of the input impedance can reach almost 7 times the rated value. This shows that the parameter variation has a big impact on the input impedance value. The contour plot on the bottom details the impedance variation. It highlights the impact of the higher resonant frequency - resulting in a bigger difference between resonant and switching frequency - which leads to a higher input impedance.

However, if the allowed variation is reduced to ±10% as shown in **Fig. 5.3b**, the maximum value of input impedance is around 2.5 times the rated value. Even further, if the allowed variation is reduced to ±5% and ±1% the maximum deviation of the rated input impedance value is reduced to almost 1.8 and 1.15 times the rated value, respectively. Nevertheless, from these plots, the impact of small variations on the resonant tank parameters is visible as their big influence on the input impedance.

In the previous plots, the switching frequency and magnetizing inductance were fixed at the rated value. However, they also influence the input impedance. The variation of the magnetizing inductance and switching frequency are shown in **Fig. 5.4**, and the simulated values are also described in **Tab. 5.2**. It is considered ±10% tolerance on these two values, which is a realistic and affordable tolerance.



(a) L_m (b) f_s

Fig. 5.4 Magnitude of the input impedance at the switching frequency for ±10% tolerance on L_r and C_r. The arrow represents the increase in the value under analysis. In (a) the impact of magnetizing inductance, considering 3 discrete values of −10%, 0%, and +10% of tolerance of the magnetizing inductance. In (b) the impact of switching frequency on the input impedance, considering 3 discrete values of −10%, 0%, and +10% of tolerance for the switching frequency. The contour plot details the surface interception with a unity plane, showing the displacement and rotation/tilt of the curves.

In **Fig. 5.4a** the impact of the magnetizing inductance is shown. The magnetizing inductance impacts the main input impedance magnitude and not directly the curve. Its impact is directly related to the resonant tank impedance as the magnetizing inductance is in parallel with the load and in series with resonant inductance and capacitance.

The change in the switching frequency also impacts the input impedance characteristics. By changing the switching frequency, the inclination of the surface changes as shown in **Fig. 5.4b**. In this case, the switching frequency alters the curve more expressively. Therefore, it is possible to observe that the impedance can be modified to some extent, for the same set of parameters only by changing the switching frequency. As will be demonstrated later, by increasing or decreasing the switching frequency one can increase or decrease the input impedance, respectively.

5.3 Current Sharing Unbalance of the DCTs

Having determined input impedance dependence on the variations of various parameters, the current sharing unbalance is calculated according to the currents flowing on each branch. In this way, relating to the schematic in **Fig. 5.2b** considering only two DCTs, the currents of each branch are:

$$i_{dct,1} = \frac{u_o - u_i}{Z_{dct,1}}, \tag{5.2}$$

and

$$i_{dct,2} = \frac{u_o - u_i}{Z_{dct,2}}. \tag{5.3}$$

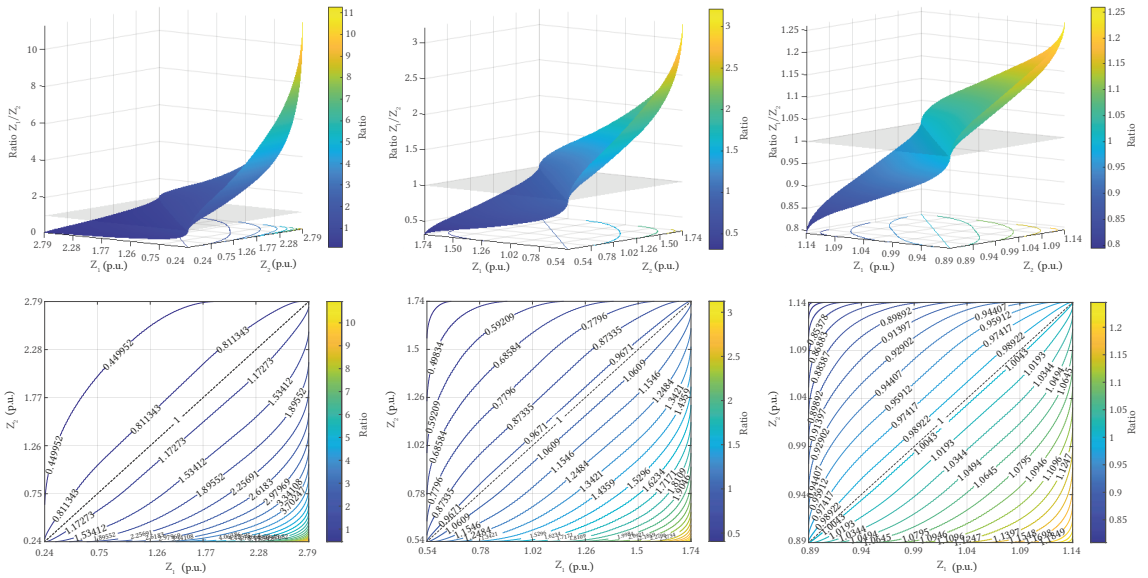
As the voltage drop across the DCTs is the same, i.e. $\Delta V_{dct,1} = u_o - u_i = \Delta V_{dct,2}$, the impedance ratio for the case of two DCTs can be defined as (5.4).

$$\frac{i_{dct,1}}{i_{dct,2}} = \frac{Z_{dct,2}}{Z_{dct,1}} = \delta_I \tag{5.4}$$

Thus, the impedance ratio brings information regarding the current sharing between the two involved impedances. This definition leads to the following conclusion:

- If $\delta_I = 1$, representing an ideal case, unreachable in practice, where two the impedances are absolutely identical.
- If $\delta_I < 1$, the impedance of DCT 1 is bigger than the impedance of DCT2 which will conduct more current, until the extreme case where $\delta_I \approx 0$, implying that all power (2 p.u.) is taken by DCT 1 rated for 1 p.u., which is not feasible nor desired in practice.
- If $\delta_I > 1$, similar to the previous case for but DCT 2.

Fig. 5.5 shows the impedance ratio of two DCTs considering a parameters tolerance of ±10%, ±5%, and ±1%. As can be seen, the combination of two DCT designs can result in any point on the surfaces of **Fig. 5.5**, with the specified parameters tolerance. For the case of ±10% shown in **Fig. 5.5a**, the



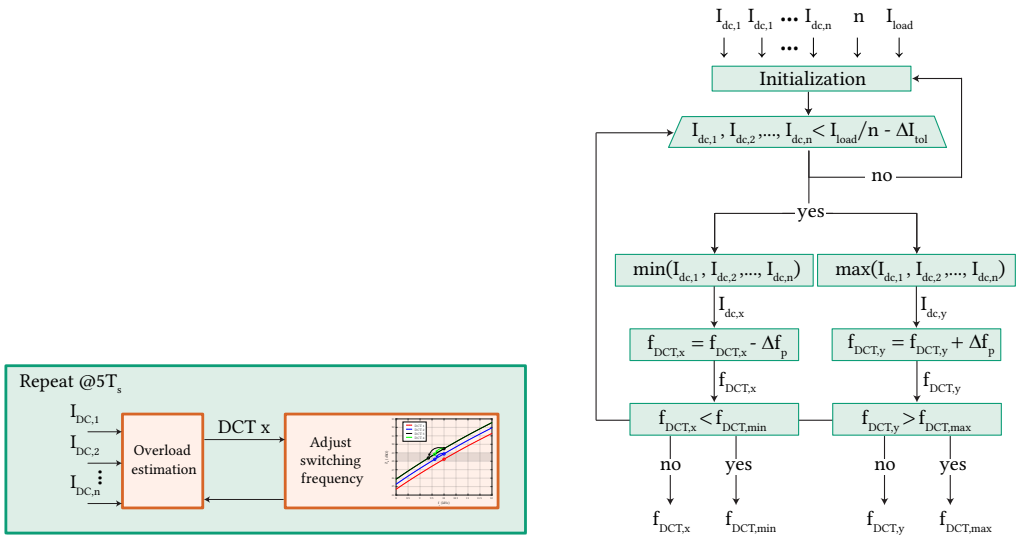
(a) ±10% (b) ±5% (c) ±1%

Fig. 5.5 Input impedance ratio for two DCTs considering a variation of ±10%, ±5%, and ±5% on L_r and C_r. The unity plane represents the ideal case when the impedance is the same. In (a) parameters variation of ±10%; (b) ±5%, and (c) ±1%. The contour plot details the variation of the impedance ratio value.

impedance ratio can reach a very high value of almost 11 times the ideal case; consisting in the extreme case of one impedance being the highest and other the lowest, among the values provided in **Fig. 5.3b**. However, when reducing the tolerance to ±5%, the maximum reached is 3 times, and when considering ±1%, 1.25 times.

From **Fig. 5.5** one can derive some important conclusions:

- Even with a highly restrictive parameter tolerance of ±1%, there is a possibility that a combination of DCTs could result in an impedance ratio of 0.79 and 1.25, as shown in **Fig. 5.5c**. These situations are a result of a combination of parameters where each DCT has its variation at the extreme opposite of the considered spectrum, i.e. DCT 1: +1% on L_r and C_r; and DCT 2: −1% on L_r and C_r. Thus, with ±1% tolerance on L_r and C_r, the combination of two DCTs can result in a worst case of 25% current sharing unbalance, meaning that for a total load current of 2 p.u., e.g. DCT 1 will conduct 1.11 p.u. and DCT 2 will conduct 0.89 p.u. This requirement is hard and expensive to impose on the designs. Still, DCT 1 will have to be oversized for 1.11 p.u. or more, knowing the expected unbalance.
- For designs with a maximum allowed parameter tolerance of ±5%, the worst combination leads to an impedance ratio of 0.31 and 3.2, as shown in **Fig. 5.5b**. This worst-case combination results in an overload in DCT 1 of 1.52 p.u. and DCT 2 0.48 p.u. for a 2 p.u load current. Similarly to the previous case, the DCT 1 will have to be oversized to 1.52 p.u. or more.
- If one considers ±10% or higher, there will be more combinations with higher deviation, which can lead to poor current sharing. For the designs with ±10% as shown in **Fig. 5.5a**, the worst case is $\delta_I = 0.08$, meaning that practically all the current will flow in only one branch. For the



(a) (b)

Fig. 5.6 (a) Finite state machine for parallel operation. Online adjustment of switching frequency to alter the input impedance and improve current sharing unbalance. (b) More aggressive logic to correct the current sharing with switching frequency. ΔI_{tol} the allowed unbalance, and Δf_p is the step in frequency.

case of 2 p.u. load current, DCT 1 will conduct 0.15 p.u. and DCT 2 1.85 p.u. As the parameters can vary in a wider range, the possible combinations between two DCTs increase, and therefore, there will be more chance that the ratio of two DCTs is far away from the unity value, resulting in an unfeasible current sharing situation.

In the case of more DCTs in parallel, the same approach can be used to assess the current sharing conditions. Extending the criteria for the current sharing error, the maximum deviation can be found by:

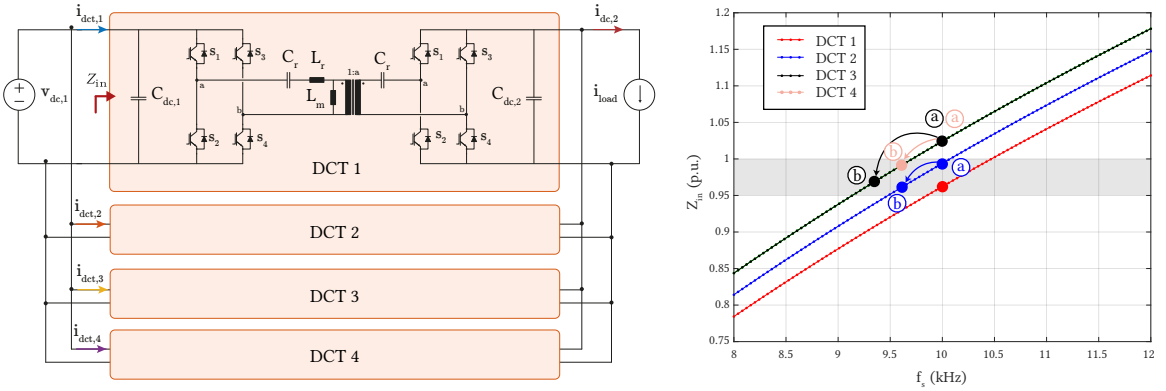
$$\delta_{I(1,2,..,n)} = max(\delta_{I(1,2)}, \delta_{I(1,3)}, \delta_{I(2,3)}, \ldots, \delta_{I(m,n)}) \tag{5.5}$$

In this case, this function takes the maximum unbalance of all the possible dual combinations, and therefore, the final result will give the maximum current sharing error for the set of DCTs. As a consequence, the result highlights the two most extreme impedances, that could be adjusted to enhance the current sharing unbalance.

5.3.1 Solutions for the Current Sharing Unbalance

Notably, due to the impact of the parameter variations on the converter's characteristics, the current sharing of the DCTs is hard to achieve. However, one way to achieve it is to use the only degree of freedom of the DCT, which is the switching frequency, to modify the input impedance and realize a satisfying current sharing. Thus, this information can be used during the commissioning phase or as a closed-loop control to adjust the impedance.

The first idea is to characterize the DCTs experimentally and adjust the switching frequency correcting the parameter differences. With this approach, no closed-loop control is added to the DCT.



(a) (b)

Fig. 5.7 (a) Four DCTs in parallel to create a higher power DCT. (b) The input impedance of DCTs for different switching frequencies. The operating point at ⓐ shows the operation at 10 kHz, and the operating point at ⓑ is the final switching frequency used for simulation results. Shaded area with acceptable current sharing range.

Nevertheless, in this approach, further variations due to temperature, components aging, and other effects can also impact the input impedance and lead to unexpected unbalances.

Another idea is to include an upper-level supervisory logic to control the current sharing unbalance. Ideally, this is integrated with the logic to activate and deactivate DCTs when the load changes, focusing on the best efficiency of the overall system.

Fig. 5.6 shows two approaches for the closed-loop control for the current sharing unbalance. Firstly, a finite state machine could be created as shown in **Fig. 5.6a**. With this extra layer of operation logic, the arrangement will identify the overloaded module and adjust the switching frequency of the DCTs to improve the current sharing. Another option is to use a more aggressive logic where the strategy always tries to correct the modules to share the current, as shown in **Fig. 5.6b**. This logic focuses on increasing the power consumption of the DCT consuming less power/current and decreasing the power of the DCT consuming more power/current.

5.3.2 Simulation of DCTs in Parallel

The simulation of four parallel connected DCTs is performed to demonstrate and verify the proposed methodology. The system is shown in **Fig. 5.7a**, and **Tab. 5.3** summarizes the DCTs parameters. DCT 2 is chosen to be the reference base. DCT 1 is chosen to have −10% variation on L_r and C_r, and DCT 3 and DCT 4 are chosen to be the same top extreme for the case of +10% variation on L_r and C_r, to show that both DCTs create the same current sharing unbalance, for different power levels.

Each DCT operates by itself, in an open loop, and PWM pulses are not synchronized nor interleaved, with an initial phase shift of +5° between them with 10 kHz switching frequency. After every load step, another DCT is added to ensure that there will be always enough leverage to verify the current sharing unbalance and modify it by changing the switching frequency.

Fig. 5.7b shows the input impedance of the four simulated DCTs for different switching frequencies. From this plot, one can reduce or increase the switching frequency to change the input impedance and improve the current sharing.

Tab. 5.3 DCTs parameters of simulation.

Description	DCT 1	DCT 2	DCT 3	DCT 4	Unit
DC Voltage 1		750			V
Rated power		50			kW
Switching Freq.		10			kHz
Magnetizing Ind.		750			μH
Leakage Ind.	10.35	11.5	12.65	12.65	μH
Resonant Capacitor	34.537	38.375	42.212	42.212	μF
Leakage Ind.	-10	0	+10	+10	%
Resonant Capacitor	-10	0	+10	+10	%
Total load		50, 100, 150, 200			kW

Tab. 5.4 Most significant input impedance in p.u., and expected and simulated current sharing unbalance (100% perfect sharing, 0% no sharing).

Case	Lower Z_{dct}	Higher Z_{dct}	Analytical	Simulated
①	0.24	1	24.9%	25.7%
②	0.31	0.33	96.7%	97.2%
③	0.31	1.79	17.3%	18.2%
④	0.29	0.31	93.93%	94.41%
⑤	0.29	1.79	16.2%	17.5%
⑥	0.29	0.34	85.3%	86.6%
⑦	0.29	0.34	85.3%	86.2%

In this context, **Fig. 5.8** shows the complete simulation of four DCTs. Firstly, only DCT 1 is operating with the nominal load. At $t = 0.025$ s, the DCT 2 is added to share the total current. At this moment the expected current sharing unbalance is $\delta_I = 0.24$, which leads DCT 1 to conduct 0.76 p.u., and DCT 2, 0.24 p.u. of total power. A summary of the cases with analytical and simulation results is detailed in **Tab. 5.4**.

One way to correct the current sharing is by changing the switching frequency. In this case, the switching frequency of DCT 2 is reduced to $f_s = 9.9$ kHz, and the new expected current sharing unbalance is $\delta_I = 0.33$. Reducing the switching frequency even further, a good current sharing is achieved when DCT 2 operates at $f_s = 9.6$ kHz with a current sharing unbalance of $\delta_I = 0.82$. To further adjust it, the switching frequency of DCT 1 increases to $f_s = 10.1$ kHz, resulting in a current sharing unbalance of $\delta_I = 0.96$. Still, further adjustment and fine-tuning of the switching frequency for an even better current sharing is also possible.

At the time $t = 0.1$ s, the load increases to 2 p.u. (100 kW). At this moment, the fact that both DCTs are already sharing the current leads to an equal increase in power. Then, the DCT 3 is activated. At this instant, the current sharing unbalance of DCT 3 with DCT 1 is $\delta_I = 0.17$, and with DCT 2 is $\delta_I = 0.22$, resulting in $\delta_{I(1,2,3)} = [(0.96), (\mathbf{0.17}), (0.22)]$. Therefore, the worst current sharing unbalance is given by DCT 1/DCT 3, and DCT 3 will barely conduct any current, as shown in case ③.

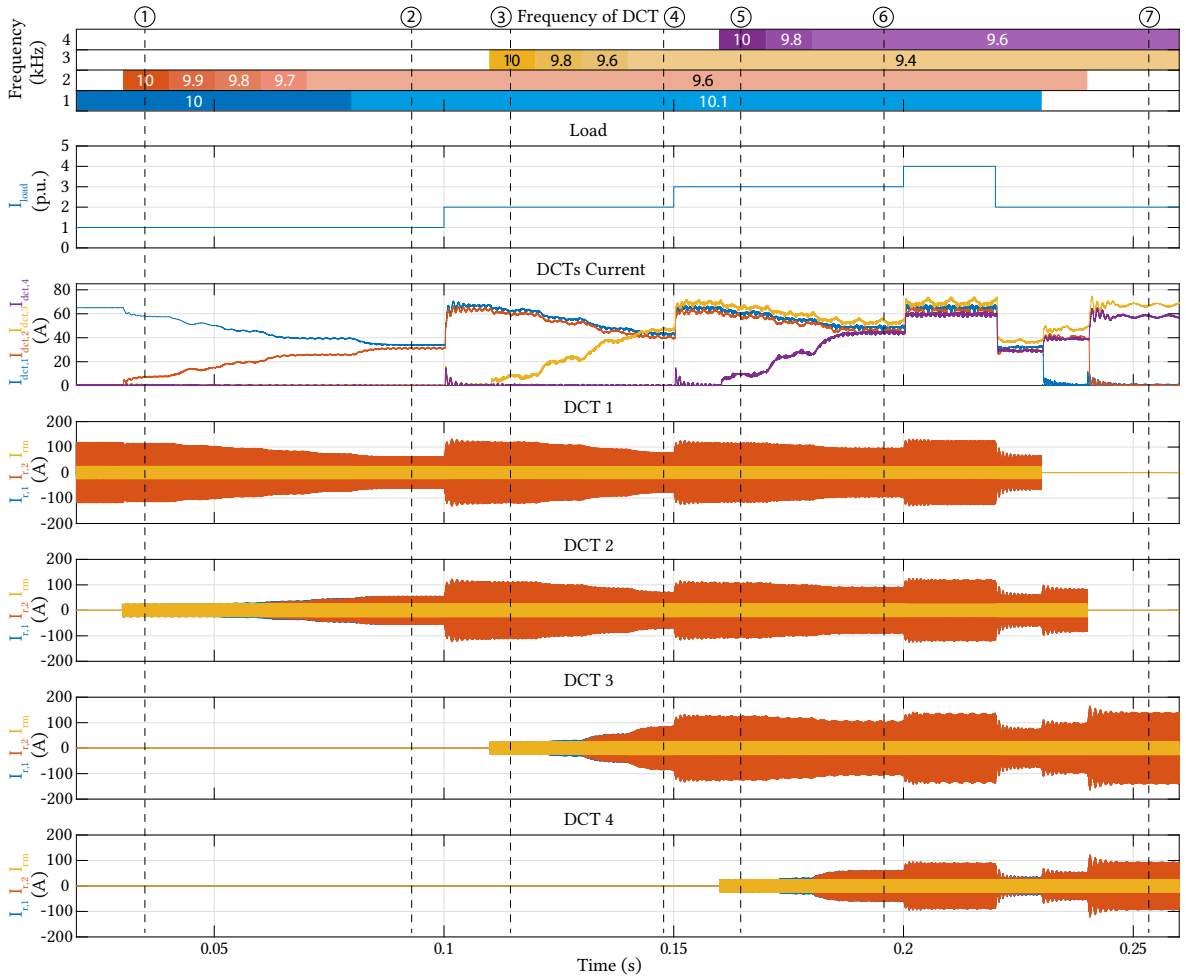


Fig. 5.8 Simulation results for the parallel operation of four DCTs. From top to bottom: DCTs switching frequency; Load profile; Output DC current of DCTs; Resonant current of primary and secondary side, and magnetizing current of each DCT. Circled numbers correspond to described cases.

In this situation, the arrangement will not support the 3 p.u. load and an increase in the load would cause overload for DCT 1 and DCT 2. Thus, the same process of adjusting the switching frequency of DCT 3 is performed to reduce the input impedance and enhance the current sharing. The DCT 3 reduces the switching frequency to $f_s = 9.4$ kHz, resulting in a maximum current sharing unbalance of $\delta_I = 0.94$. This is presented as case ④.

At the time $t = 0.15$ s, the load increases to 3 p.u. (150 kW), and similarly to the previous case, all DCTs increase the processed power equally.

Later, DCT 4 is activated and starts conducting current according to the current sharing unbalance with the other DCTs of $\delta_{I(1,2,3,4)} = [(0.96), (0.85), (0.21), (0.93), (0.23), (\mathbf{0.18})]$, as shown in case ⑤.

Then, the switching frequency of DCT 4 is adjusted to $f_s = 9.6$ kHz, resulting in a maximum current sharing unbalance of $\delta_I = 0.85$, given by the combination of DCT 3/DCT 4. Thus, at time $t = 0.2$ s, the load increases to 4 p.u. (200 kW), all DCTs increase the processed power equally. As the current

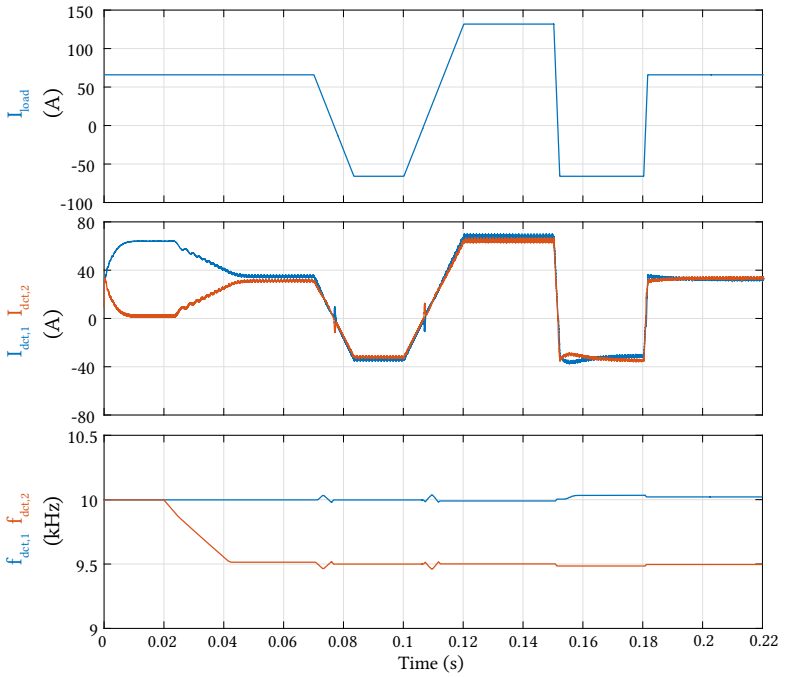


Fig. 5.9 Simulation of the parallel operation of DCT 1 and DCT 2 with the logic to enhance the current sharing with switching frequency described in **Fig. 5.6b**. Test with rated power and two times the rated power, with power reversal.

sharing unbalance with DCT 4 is $\delta_I = 0.85$, this leads to an overload of almost 1.2 p.u. of DCT 3, as can be seen in the DC currents of **Fig. 5.8**.

In the end, the load decreases to 2 p.u., and DCT 1 is deactivated. At the time $t = 0.225$ s, it is possible to observe that the current sharing unbalance is still determined by the maximum current sharing unbalance between DCT 3 and DCT 4. Thus, DCT 2 is deactivated and the current sharing unbalance remains the same, now operating only with DCT 3 and DCT 4, showing that the maximum current sharing unbalance predicted by the most significant impedance remains true in any case, and it is not affected by the load.

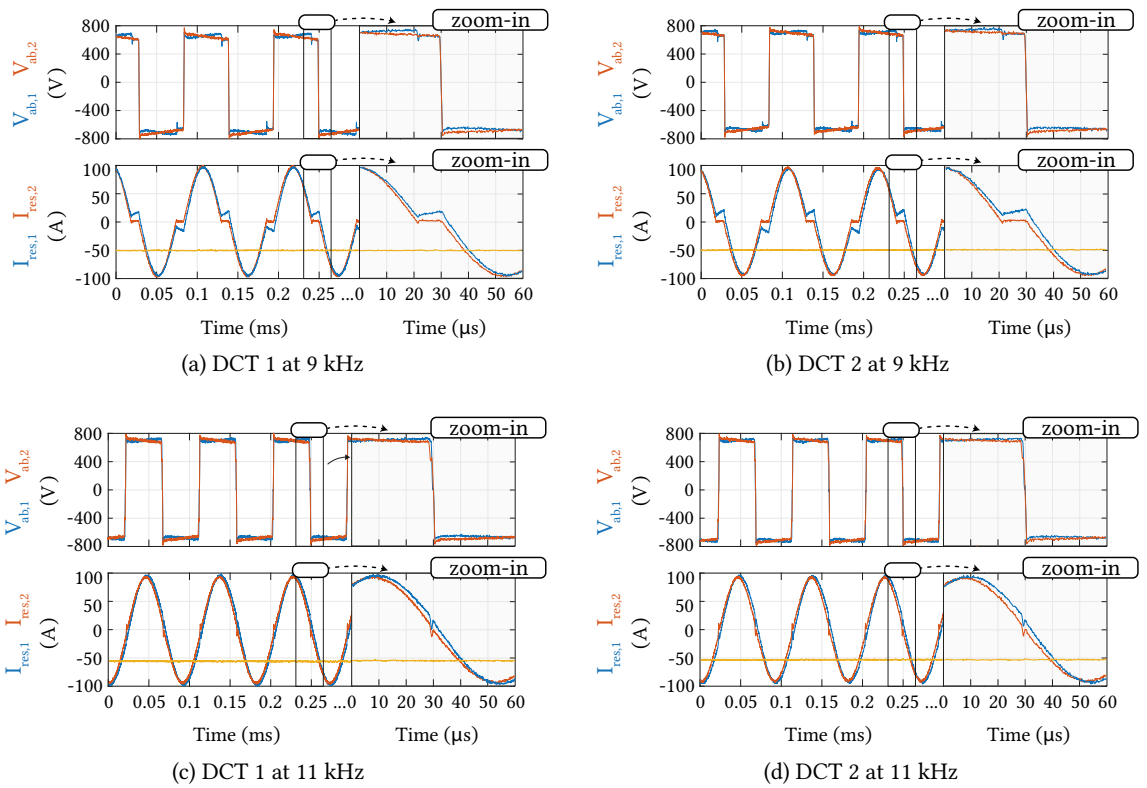
Now, considering only two DCTs (DCT 1 and DCT 2), the closed-loop control described in **Fig. 5.6b** was implemented in PLECS to verify its performance along with the other features of the DCT including power reversal. **Fig. 5.9** shows the total current, the individual DC current, and the switching frequency.

It can be seen that during the start-up of converters, due to the non-linear behavior of the converter during the soft-start, the current sharing is not yet established. Then as the DCTs enter in steady state the current sharing is determined by given impedance ratios. At the time $t = 0.02$ s, the logic to correct the current sharing unbalance is activated. Immediately, the frequency of DCT 2 decreased to 9.5 kHz, reaching the acceptable current sharing unbalance pre-defined at 5 A, and the steps of frequency were set to 0.1 Hz/ms. Later, a load profile is performed to reverse the power with ramp and step dynamics, showing that only small corrections are performed to fine-tune the current sharing. In the end, this closed-loop control logic managed to alter the switching frequency properly and ensure a satisfying current sharing.

5.4 Experimental Results

The experimental verification is performed using the two LV DCT prototypes. Firstly, the two prototypes were tested in different switching frequencies to validate their operation. Two frequencies were tested as considered top and bottom limits for the parallel operation: i) 9 kHz, and ii) 11 kHz.

Fig. 5.10 shows the current and voltage waveform for these operating points. The operation with 9 kHz is below the resonant frequency. It can be seen in **Fig. 5.10a** and **Fig. 5.10b** for both DCTs the primary resonant current lands on the magnetizing current before the next switching state. The operation with 11 kHz is slightly above the resonant frequency (**Fig. 5.10c** and **Fig. 5.10d**). It can be seen the primary resonant current is interrupted, without landing on the magnetizing current.



(a) DCT 1 at 9 kHz

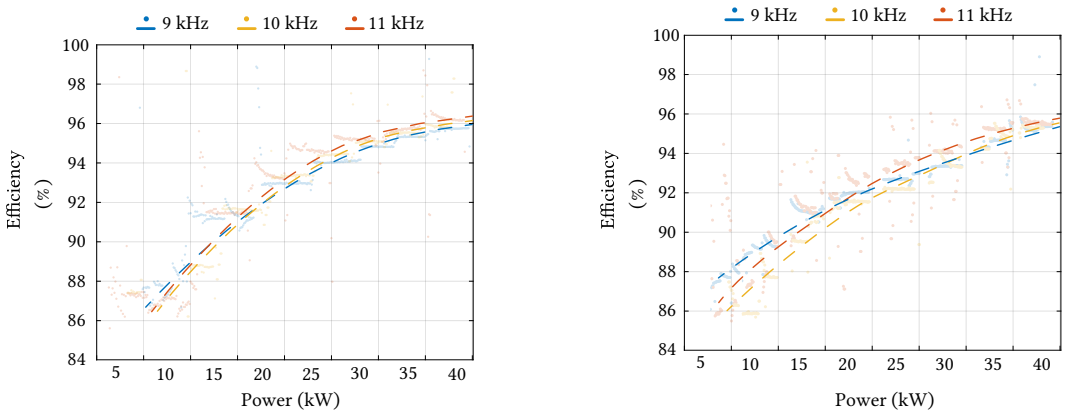
(b) DCT 2 at 9 kHz

(c) DCT 1 at 11 kHz

(d) DCT 2 at 11 kHz

Fig. 5.10 Current and voltage waveforms for DCT 1 and DCT 2 operating at 9 kHz and 11 kHz. On top (a) and (b), the operation below the resonant frequency with 9 kHz of DCT 1 and DCT 2 respectively. Operation is characterized by the resonant current landing on the magnetizing current before the next switching pulse. On the bottom (c) and (d), the operation above the resonant frequency with 11 kHz of DCT 1 and DCT 2 respectively.

The efficiency of the DCTs for the tested three switching frequencies was experimentally extracted with a power analyzer PPA5530 - N4L. The power analyzer has an expected error of ±0.1% [126], the voltage probe ±2% [127], and the current probe ±1% [128], which leads to ≈ 97% accuracy of measurement - and an error of ±3% of the recorded efficiency. **Fig. 5.11** shows the efficiency of the two LV DCTs. The data points are the recorded data with the PPA data logger for different power steps, and the efficiency trend is obtained by parabolic curve-fitting from the Matlab plot.



(a) DCT 1 (b) DCT 2

Fig. 5.11 Efficiency curve of the two DCTs for 9 kHz, 10 kHz, and 11 kHz. The data points are the recorded measurements for 5 minutes at the specified power. The curve-fitting represents approximately the efficiency trend.

5.4.1 Parallel Operation

For this test, the two DCTs were hard paralleled as shown in **Fig. 5.12**, and the calculated input impedance of the DCTs are shown in **Fig. 5.13**. The experiment proceeds as follows: i) First the two DC buses are energized, and DCTs DC links are charged; ii) DCT 1 starts its operation and transmits the power according to the voltage difference of the two DC ports; iii) Later, the DCT 2 starts its operation and DCTs start sharing the current naturally.

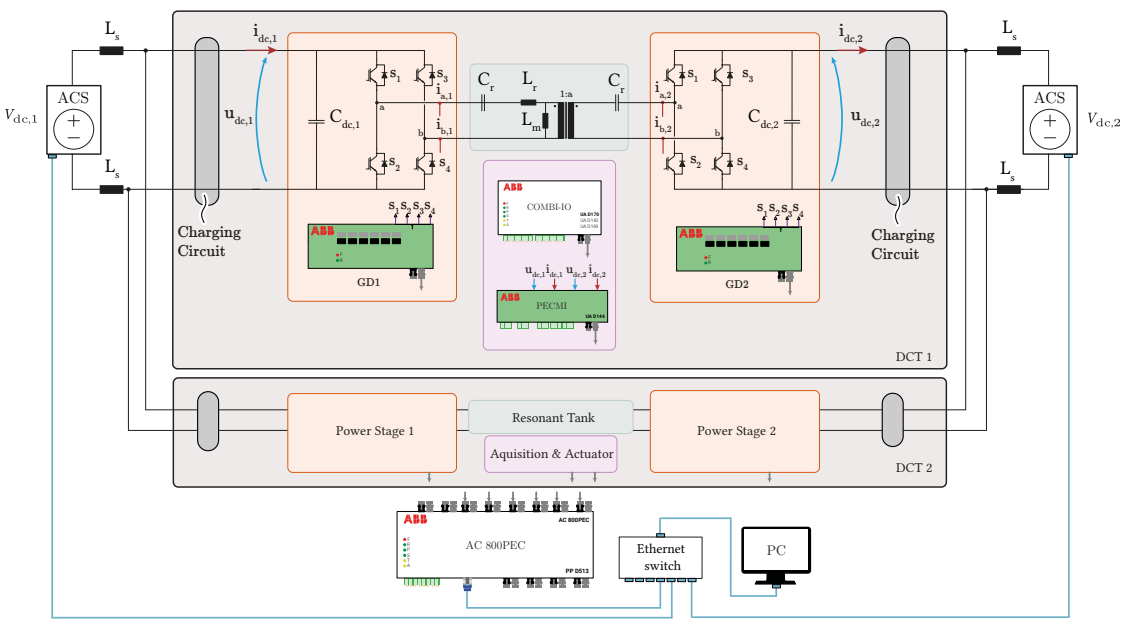


Fig. 5.12 Schematic of the complete system. The two DC buses are created with voltage sources. For the test setup system, the controller, relays, and power sources are accessed through the PC.

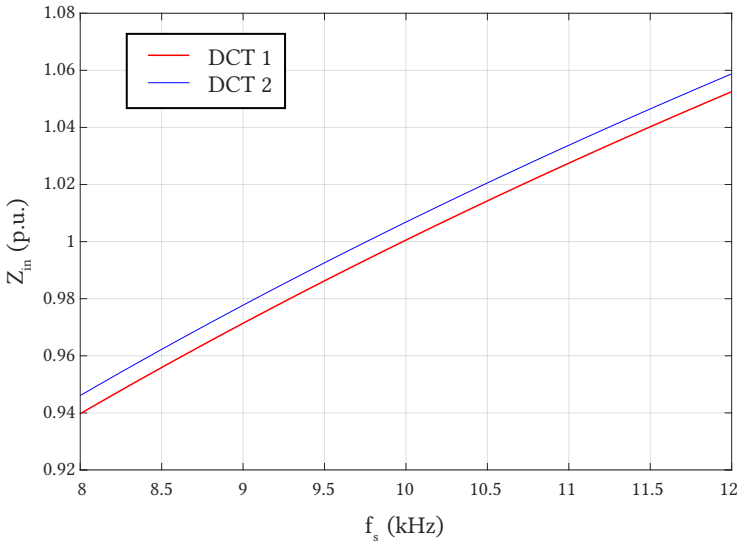
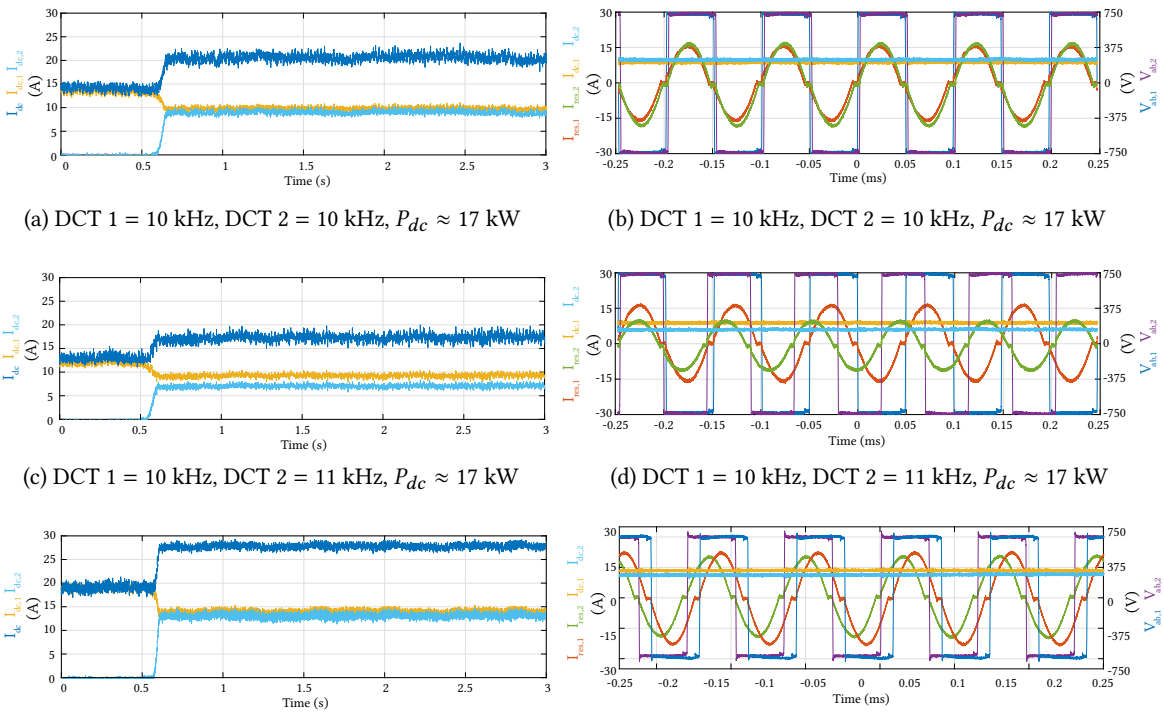


Fig. 5.13 Variation of the input impedance of the LV DCT prototypes for different switching frequencies, using the analytical model, for nominal load. The difference between both input impedances is minimal.



(a) DCT 1 = 10 kHz, DCT 2 = 10 kHz, $P_{dc} \approx 17$ kW

(b) DCT 1 = 10 kHz, DCT 2 = 10 kHz, $P_{dc} \approx 17$ kW

(c) DCT 1 = 10 kHz, DCT 2 = 11 kHz, $P_{dc} \approx 17$ kW

(d) DCT 1 = 10 kHz, DCT 2 = 11 kHz, $P_{dc} \approx 17$ kW

(e) DCT 1 = 10 kHz, DCT 2 = 10 kHz, $P_{dc} \approx 20$ kW

(f) DCT 1 = 10 kHz, DCT 2 = 10 kHz, $P_{dc} \approx 20$ kW

Fig. 5.14 Experimental waveforms of the parallel operation of 2 DCTs. On the left side the total DC current and DCT output currents. On the right side, the DCT output currents, secondary resonant currents, and voltage are applied to the resonant tank. At first, only DCT 1 is operating and at 0.5, DCT 2 is enabled to share the load current.

Fig. 5.14 shows all the experimental waveforms for the parallel operation. The first row shows the experimental waveform for the parallel operation with both DCTs at 10 kHz; On the left side the DC currents ($I_{DCT,1}$, $I_{DCT,2}$, and I_{DC}), and on the right side the DCT's secondary resonant current ($I_{res,1}$,$I_{res,2}$), DC currents ($I_{DC,1}$, $I_{DC,2}$), and resonant tank voltages ($V_{ab,1}$, $V_{ab,2}$). In this experiment, the DCT 1 is operating alone at first, and at time $t = 0.5$ s, the DCT 2 is enabled. After the inclusion of DCT 2, the soft-start logic dictates the transient dynamics until the steady-state operation is met.

This experiment showed that despite minor differences in the input impedances of the two impedances, the additional impedance introduced by the cable connecting the resonant tank makes this difference negligible. As a result, the current is evenly distributed between them.

The second experiment is shown in the second row of **Fig. 5.14**, with the experimental waveforms with DCT 2 operating at 11 kHz. This experiment was performed to evaluate the switching frequency impact on the current sharing unbalance. Here, it can see that by increasing the switching frequency of DCT 2 the input impedance also increased, creating an unbalance in the current sharing.

Lastly, in **Fig. 5.14** third row, the experimental waveforms for both DCTs at 10 kHz with $P_{dc} \approx 20$ kW are shown to check the load impact on the current sharing behavior. The current sharing behavior is the same as for the first test shown on the first row of **Fig. 5.14**.

5.5 Summary and Conclusion

Clearly, achieving perfect current sharing through a design is hard, next to impossible. The presented analysis on the parallel operation of DCTs helps to solve several questions regarding the requirements and restrictions on the parameter tolerance. The variation in the resonance parameters has a big impact on the current sharing when paralleling DCTs and the impedance of the DCT dictates current sharing. Thus, the only degree of freedom to correct the current sharing is the switching frequency.

This chapter presented a methodology to assess the quality of the parallel operation, and how to quantify the current sharing unbalance based on the input impedance. With the presented methodology, the design constraints considering the required current sharing percentage can be defined. Besides that, the impact of the switching frequency on the input impedance was investigated to enhance the current sharing. However, this solution would require some attention to its effect on the power stages (an increase of losses), circulating current at the DC-link (inclusion of beat frequency oscillations), and different operation points at the resonant tank (higher period during discontinuity).

Furthermore, the parallel operation of DCTs is challenging and requires a few trade-offs. The input impedance is very sensitive to the resonant tank parameters and small deviations in any parameter lead to a high difference in the input impedance. Consequently, the current sharing is directly affected. From the analytical modeling, parameters tolerance from ±1% to a maximum of ±5%, are preferable to be the target tolerance to ensure a minimum current sharing unbalance for any possible design. After that, the input impedance needs to be verified if DCTs will achieve satisfying current sharing.

Ultimately, this chapter showed how to assess the quality of the parallel operation of the DCTs through an analysis of the input impedance. Additionally, the two LV DCT prototypes were tested in parallel, and the influence of the switching frequency on the current sharing was highlighted.

6

Modeling of the DC Power Distribution Network for System Analysis

The DC power distribution network is composed of several power converters operating at different operating points, different frequencies, and with different control dynamics. In these systems, one challenge is to create a scalable and faithful model to analyze large systems. Thus, this chapter describes the developed methodology to compute the DC power flow without the AC power flow loop and assess the nodal impedance, based on adaptations of the available tools for analyzing AC systems.

6.1 Multi-Converter System's Modeling

In a multi-converter system with a broad use of power electronics converters (e.g., parallel connections, DC buses with multiple converters, DC networks, etc.), modeling tools to analyze the operation and stability of these systems require closer attention. Depending on the required level of detail, the analysis can be very demanding, and sometimes not feasible.

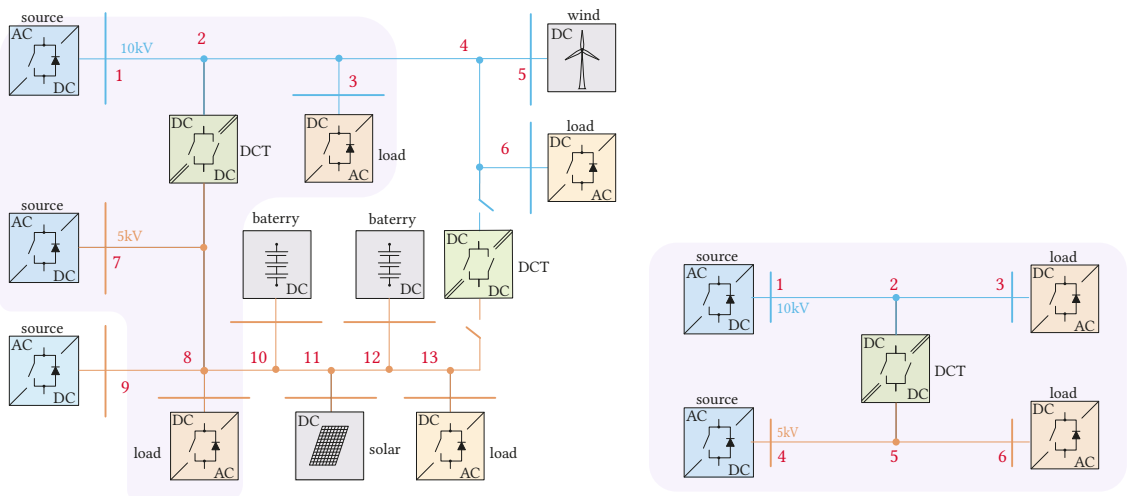


Fig. 6.1 (a) DC PDN with several power converters. This system has voltage-controlled converters, current-controlled converters, integration of renewable generation, and ESS interconnected by DCTs. (b) Simplified DC PDN from the highlighted area, used for the analysis of this chapter.

The DC PDN of the future will integrate converters from different manufacturers, technologies, and control dynamics in a single system. **Fig. 6.1a** shows an illustrative example of such a system. For

these systems, the level of detail of the power converter needs to be reduced to a certain extent for a proper analysis, and this is discussed in this chapter.

The highlighted area of this system shows one of the simplest architectures of the DC PDN (redrawn in **Fig. 6.1b**). Two main DC buses feed their main loads through a transmission line, and a DCT interfaces the DC buses. The DC PDN is formed by some type of AC/DC converter aiming to supply the DC voltage and feed loads; or by renewable generation with power converter energy processing, where the source aims to inject its maximum power generation to the grid, feeding loads and energy storage units. The loads are power-electronics-driven loads usually seen as Constant Power Load (CPL).

Therefore, the interaction between different sources and different control strategies brings extra challenges in terms of power management. Also, the CPL has a negative incremental impedance behavior [129], whose characteristics reduce the effective damping of the system and may induce destabilizing effects into the system [130]. Hence, it is crucial to correctly identify the system's characteristics, including these elements and their contribution to the whole system response. In fact, the primary concern is to provide a scalable solution to identify the system's operating point and frequency behavior, allowing safe operation and determining its critical limits.

The standard approaches for analyzing this system involve simplifying the connection path, specifically the DCT connection, and determining a parallel equivalent for both the source and the load side [131]–[134]. This methodology is well justified when the converters have similar dynamic behavior. However, when relating to systems with power converters from different manufacturers (unknown topology, controls strategy), different switching frequencies, unequal transmission line sizes, and non-negligible connection path impedance, this approach is not suitable anymore.

Other works approach the DC and hybrid DC-AC power systems from a control point of view, matching system dynamics and power converters' responses to ensure system operability and stability. A usual approach for hybrid DC/AC microgrids is employing centralized controllers [94], [135], [136], and power flow control converters [93], [137], [138]. However, these methodologies always require high-level communication between nodes and access to the controller's gains, usually not available for external use. Some solutions include decentralized control loops for hybrid DC/AC microgrids [139], [140]. Although these solutions can ensure system stability and improve the system response, they are local to each converter and do not provide any information regarding the system's characteristics, and its capacity to extend the grid.

Alternatively, harmonic resonance analysis and its tools to analyze electrical power systems have been studied in some works to identify DC-AC power system interaction [141]–[143]. This solution identifies relevant resonant frequencies in the system, and usually brings enough information to perform the system operation, stability, planning, and expansion studies.

Nevertheless, this approach in a purely DC power system has not been studied before. For the system shown in **Fig. 6.1a**, the harmonic content in a certain node of interest is formed by several contributors. Another challenge is to include the contributions from the control loops of different converters to the linearized equivalent system properly. Nonetheless, a dominant frequency range can be explored to identify the system-level operation, ruled by the outer loop regulation and the passive elements of the system. Consequently, this allows the determination of the system's resonances, and therefore, the system's characteristics.

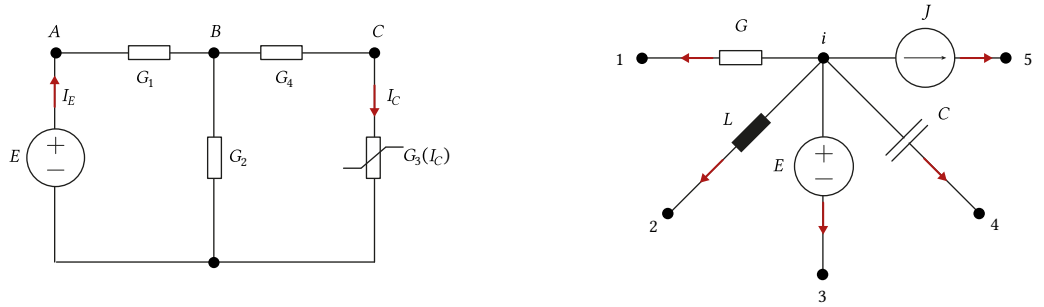


Fig. 6.2 (a) Example network with different elements and a non-linear conductance connected at node C. (b) Example of a general node with the elements that can be included in the MNA, adapted from [146].

6.2 System Analysis of DC Power Distribution Network

This section describes the essential information to perform the steady-state evaluation of the DC PDN with the Modified Nodal Analysis (MNA) and frequency-dependent response with the Resonant Modal Analysis (RMA) methodology.

6.2.1 Modified Nodal Analysis

The MNA is an extension of the classic nodal analysis developed by [144], [145]. It was created focusing on solving analog signal circuits with an elevated number of nodes. With this method, it is possible to deal in a nodal approach with the current-dependent elements in both linear and nonlinear representations of them.

Fig. 6.2a shows an example useful to explain the MNA [146]. In this figure, a three-node circuit is presented with one voltage source, three conductances, and one current-dependent conductance connected to node C. Two currents I_E and I_C are considered unknown. Thus, branch relations are introduced for the voltage source and the nonlinear conductance. The solution is written in the form of (6.1), where Y_{nodal} is the Nodal Admittance matrix, the vectors J and F are the excitation, B contains the Kirchhoff current equations concerning the additional current variable, C and D are the branch constructive relations, differentiated to the unknown vector.

$$\underbrace{\begin{bmatrix} Y_{nodal} & B \\ C & D \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} V \\ I \end{bmatrix}}_{x} = \underbrace{\begin{bmatrix} J \\ F \end{bmatrix}}_{b} \tag{6.1}$$

For the given example of **Fig. 6.2a**, the resultant system is:

$$\begin{bmatrix} G_1 & -G_1 & 0 & -1 & 0 \\ -G_1 & G_1+G_2+G_4 & -G_4 & 0 & 0 \\ 0 & -G_4 & G_4 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_3 & 0 & -1+\frac{\partial G_3}{\partial I_3} v_C \end{bmatrix} \begin{bmatrix} v_A \\ v_B \\ v_C \\ I_E \\ I_3 \end{bmatrix} = \begin{bmatrix} i_A \\ i_B \\ i_C \\ E \\ 0 \end{bmatrix} \tag{6.2}$$

Thus, the nonlinearity can be easily solved by an iterative method such as Newton-Raphson. With the inclusion of these extra matrices in the solution, the classical nodal approach can be extended and its usage becomes completely general. Another advantage pointed out by [146] is that by using the nodal approach for these systems, the set-up time to create the matrix is drastically reduced, as well as its solver time.

For the DC PDN, the MNA is needed for the steady-state analysis. In the literature, usual solutions to the power flow calculation in DC systems are supported by an external AC power flow loop [147], [148], which is not present in a purely DC power system. Thus, as there is no inductance/capacitance, nor angle difference at steady state in the DC system, it is impossible to compute the source's power injection to the system using a nodal approach, without adding some additional equations. For that reason, the formulation of the MNA includes an extra node/branch equation to compute the voltages/currents of the system.

Other approaches have been suggested using the Modified Augmented Nodal Analysis (MANA) [149]. This method enhances the MNA by adding extra equations, including various element constraints, to the admittance matrix. As a result, this approach enables the direct incorporation of ideal branch dependency relations into the matrix equations, as detailed in [150]. Ultimately, the most suitable approach depends on the considered model used for the elements of the system.

6.2.2 Harmonic Resonance Mode Analysis

The Resonance Modal analysis is a method to determine the resonance characteristics of a system. Essentially, the method consists of finding the modal parameters that determine the natural frequency and modes. A mode of the system corresponds to a signature of the system when an external force is applied [151].

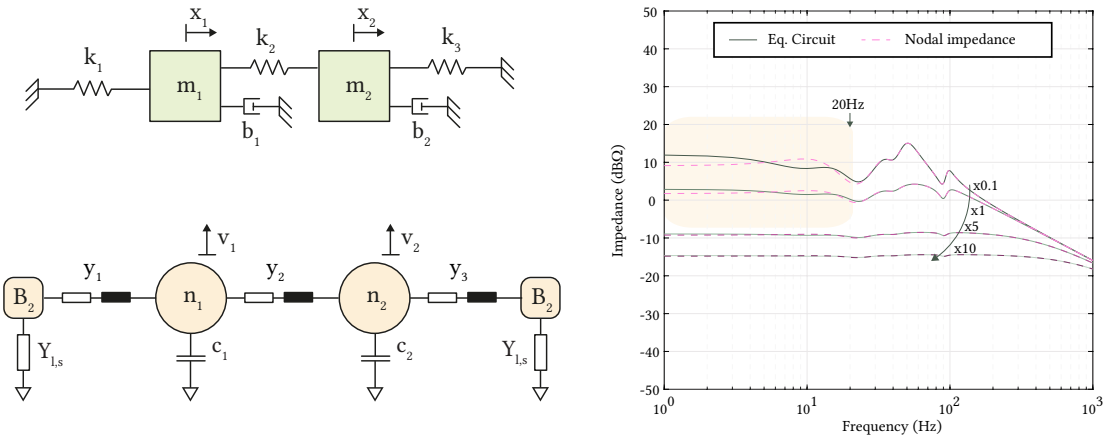
When talking about electrical systems, the study is usually related to analyzing the harmonic content of the system, in order to identify the natural frequencies and modes of the power system [152]. In this way, one can identify and characterize the system, find the driving points, and mitigate its adverse effects. With this approach, the complete eigenanalysis can be performed meaning that the harmonic resonance response can be extracted, and stability analysis can be performed [153].

In the last few years, the modal analysis for a meshed DC system has been used to study the interaction between an Multi-Terminal DC (MTDC) system and the AC power system [154], [155]. This approach identifies the modal coupling between both power systems and allows the identification of the DC dynamic impacts on the low-frequency synchronous machine stability. Also, it is used for extracting the modal response of offshore wind power plants, in which, due to the long undersea cables, the equivalent capacitance of the line has a big impact on the harmonic response [153]. In this chapter, this methodology is used to study the DC PDN with DCT and investigate the impact of the DCT on the DC PDN characteristics.

6.2.2.1 Response for Multiple Degrees of Freedom

Electrical systems have (especially DC electrical systems) dynamic behavior highly related to the properties of the voltage in the system. An analogy with the mass-spring-damper system is shown in **Fig. 6.3a**. In this way, let us consider the voltage description of the elements for a current excitation:

$$\boldsymbol{Q}\ddot{\boldsymbol{v}} + \boldsymbol{C}\dot{\boldsymbol{v}} + \boldsymbol{Y}\boldsymbol{v} = \boldsymbol{I}, \tag{6.3}$$



(a) (b)

Fig. 6.3 (a) Illustration of the equivalent circuit of the mass-spring-damper system. The displacement of the mechanical system is the voltage of the nodes, where the external force is a current perturbation. (b) Exemplification of the Nodal Impedance characteristics, including the control loop of its own node is visible in the low-frequency band.

where **Q** is the charge matrix, **C** is a capacitance matrix, **Y** admittance matrix, and **I** is the current external force. The second derivative of the voltage is out of the scope of this work.

Assuming the solution in the form of $v = Ve^{st}$, and replacing it in (6.3), with $v(0) = 0$,

$$\boldsymbol{CsVe^{st} + YVe^{st} = Ie^{st}}, \tag{6.4}$$

$$\boldsymbol{V} = \underbrace{[Cs + Y]^{-1}}_{Z}\boldsymbol{I}. \tag{6.5}$$

Thus, **Z** is called the impedance matrix of the system and each element of this matrix represents a transfer function. Each transfer function gives the response of the voltage for an excitation in current. In addition to that, the control loop is another dynamic relating the voltage and current present in the system, where the control loop is described by,

$$\frac{\Delta i_{dc}}{\Delta v_{dc}} = f(s) = T. \tag{6.6}$$

Thus, the final transfer function matrix is:

$$\boldsymbol{V} = \underbrace{[Cs + Y + T]^{-1}}_{\boldsymbol{H_z}}\boldsymbol{I}, \tag{6.7}$$

where H_z is the impedance transfer function. Although the control loops in the equivalent models derived in the next section are already in the form of admittance and can easily be added to the **Y** matrix, adding the control loops as an external matrix **T** allows to use the nodal admittance as the

Y matrix. Therefore, **Y** will always describe the system configuration, **T** will depend on the control strategy available at the node, and **C** represents the node capacitance value. It should be noted that the matrix's rank and other properties were not examined in detail. Such an investigation could be valuable for analysis, particularly when dealing with non-linear modeling.

From (6.7), the nodal impedance and the response for multiple degrees of freedom of the voltage can be described. With this approach, the nodal impedance is easily extracted and the frequency characteristic is calculated for any node of the system. Additionally, it is noteworthy that nodal impedance incorporates its control loop within the transfer function. This aspect, depending on the characteristics of the plant/controller, can influence performance in the low-frequency range, as it is illustrated in **Fig. 6.3b**.

6.2.3 Summary of the used Methodology

The solution to analyze the DC PDNs can be addressed separately in two steps. Firstly, the steady-state solution for the load flow calculation, and secondly, in the frequency domain for the resonance analysis. The load flow solution is used to provide information about the system operating point. The frequency analysis provides crucial information about the system characteristics. It describes each node's impedance characteristic. Therefore, the critical resonances and their damping will be highlighted.

- **Part I - Steady-state solution**

  The steady-state solution is calculated through the following steps:

  1. Determine the nodal admittance matrix

  $$\boldsymbol{I} = \boldsymbol{Y_{nodal}}\boldsymbol{V}, \tag{6.8}$$

  where, **I** is the node current, **V** the node voltage and $\boldsymbol{Y_{nodal}}$ the admittance nodal matrix.

  2. Describe the MNA matrices

  $$\underbrace{\begin{bmatrix} Y_{nodal} & B \\ C & D \end{bmatrix}}_{A}\underbrace{\begin{bmatrix} V \\ I \end{bmatrix}}_{x} = \underbrace{\begin{bmatrix} J \\ F \end{bmatrix}}_{b}, \tag{6.9}$$

  3. Solve linear system of (6.9)

  $$\boldsymbol{x} = \boldsymbol{A}^{-1}\boldsymbol{b} \tag{6.10}$$

  After finding the current and voltages, the current flow and power injection can easily be found for each node, and therefore, the operating system point can be identified.

- **Part II - Frequency domain solution**

  The second part is finding an analytical solution to identify the driving points of the system. The following steps describe the procedure for conducting such analysis:

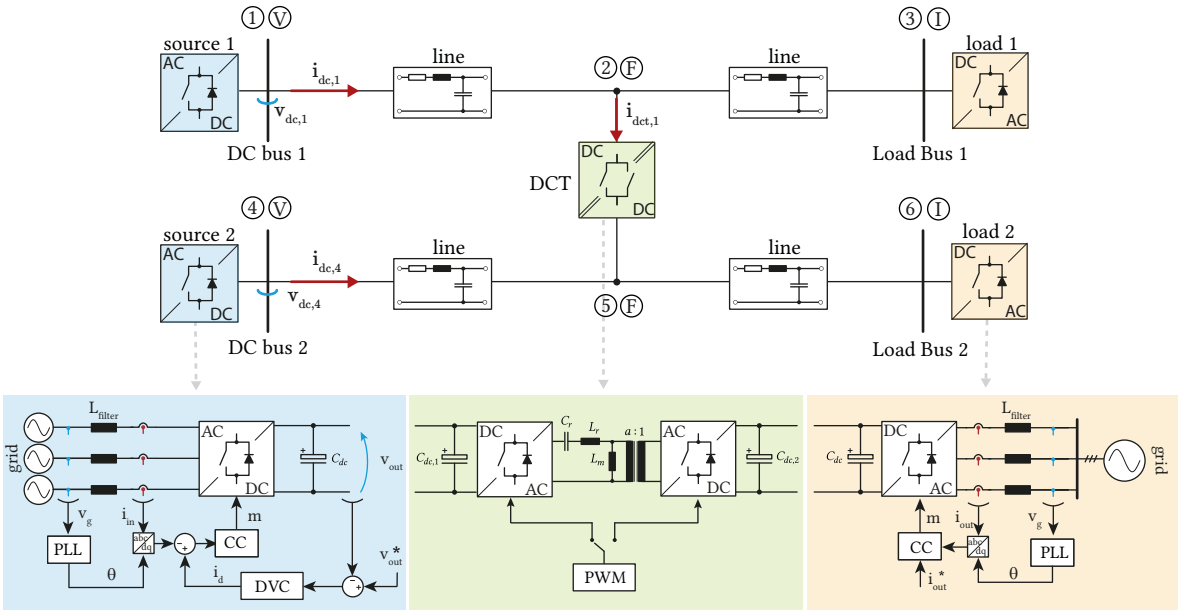


Fig. 6.4 DC power distribution network with six nodes and one DCT. On the bottom are the details of the power converters.

1. Determine the Nodal Admittance matrix with the linearized small-signal model

$$\boldsymbol{I} = \boldsymbol{Y_{nodal}V} \tag{6.11}$$

2. Compute the matrix **C** and **T** of (6.5) and (6.6),

$$\begin{aligned} \mathbf{C} &= \text{diag}\,(c_1, c_2, \ldots, c_i) \quad i = 1, 2, \ldots, n \\ \mathbf{T} &= \text{diag}\,\left(Y_{s/l,1}, Y_{s/l,2}, \ldots, Y_{s/l,i}\right) \quad i = 1, 2, \ldots, n \end{aligned} \tag{6.12}$$

   where, n is the number of nodes and s/l is source or load.

3. Find the impedance's transfer function according to (6.7):

$$\boldsymbol{V} = \boldsymbol{H_z I} \tag{6.13}$$

   where **V** is the node's voltage, $\boldsymbol{H_z}$ the impedance transfer function and **I** the node's current.

6.3 System Description

The system of **Fig. 6.4** shows a DC PDN with six nodes and one DCT, where Nodes 1 and 4 have a source type converter and Nodes 3 and 6 are with load type converters. The source and load converters can change their roles during operation. Nodes 2 and 5 are the DCT connection nodes with no voltage or current being regulated by the DCT, as these are determined by the voltage drops and loads of the system.

When considered as a source, in the context of this thesis, the AC-DC converters control their DC output voltage, while as loads, they control the output AC power/current. Thus, the first challenge is

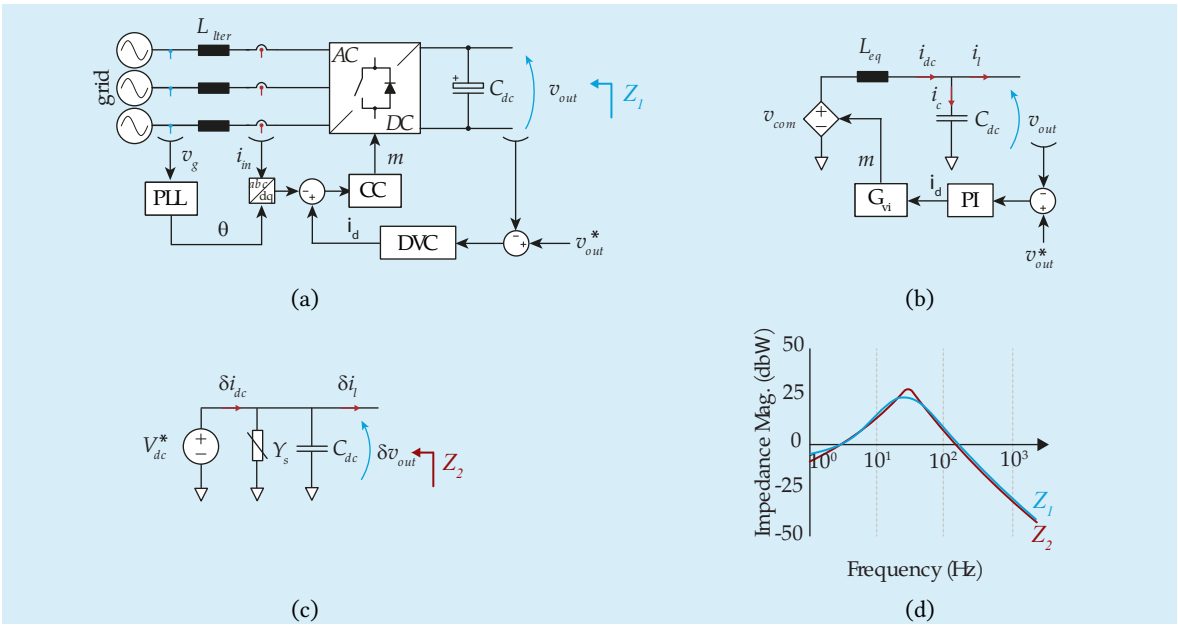


Fig. 6.5 AC-DC power converter: (a) converter switched model, (b) converter dynamic equivalent model, (c) converter frequency equivalent linearized model, (d) illustrative example of the closed-loop output impedance of the switched circuit and the equivalent linearized model response.

determining the nodal admittance matrix, including the power converters and their control loops. The models described in this section use the simplifications often adopted for linear analysis of power converters, and they can be easily found in the literature.

6.3.1 Source Converters Equivalent Model

Fig. 6.5a shows the schematic of the AC-DC power converter under study. This converter creates and regulates the DC voltage at its output, using the AC grid as the primary source. **Fig. 6.5b** shows the equivalent linear model of the converter, considering the outer voltage control loop regulated by a PI controller. This model is built by the average model of the power converter including the control loops available in the frequency range of interest.

The frequency equivalent linear model of the converter, considering that the slower outer voltage control loop determines its behavior in the frequency domain is shown in **Fig. 6.5c**. This model is valid within the voltage control bandwidth and represents the output admittance of the power converter. As this admittance is located as a shunt element, this element can easily be added to the nodal admittance matrix. Note that the voltage source is only a representation that the node is voltage-controlled. This approach is also used for the inclusion of the power converters in the admittance matrix from the AC side solutions [156].

Thus, considering the switched power converter schematic of **Fig. 6.5a**, with the PI voltage controller, the source admittance value is,

$$Y_s = \frac{sK_p + K_i}{s} \times K_{G_{vi}}, \tag{6.14}$$

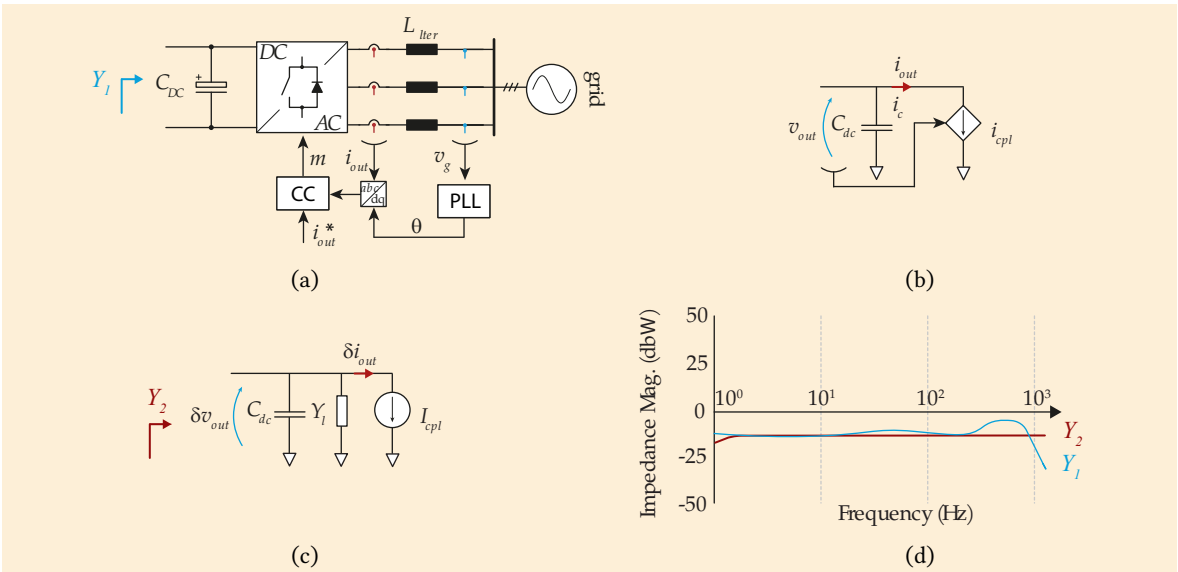


Fig. 6.6 DC-AC power converter: (a) converter switched model, (b) load dynamic equivalent model, (c) load linearized model, (d) illustrative example of the closed loop input admittance of the switched circuit and the equivalent linearized model.

where, K_p and K_i are the proportional and integration gain, respectively, and $K_{G_{vi}}$ is the inner control loop compensation gain, usually $K_{G_{vi}} = 3V_d/2V_{dc}$.

Finally, **Fig. 6.5d** shows an illustrative example of a closed-loop impedance frequency response, comparing the switched circuit shown in **Fig. 6.5a** and the linearized model in **Fig. 6.5c**. This behavior is expected for any grid-connected power converter output impedance, and this characteristic deviates for different system parameters (i.e., voltage/current ratings, capacitance value, control loop gains, etc.). At low frequencies, the system has a flat or slightly inductive behavior given by the control system impact. In the medium frequency range, around the grid frequency and its harmonics, it is expected to see the main resonances, and after that, the capacitive behavior predominates until another resonance defined by passive elements of the system occurs. The switching frequency and other power converter-related effects can appear in the impedance bode plot for higher frequencies. This Bode plot illustrates the expected simplifications of the model by using the linearized model, where a good representation can be found for a defined frequency range.

6.3.2 Load Converters Equivalent Model

A similar approach is applied to the load power converter model. However, the power converter's goal now is to process the necessary power to feed the load. **Fig. 6.6a** shows a schematic of the DC-AC power converter under study. The power converter is the same one used for the source power converter, but with the control loop regulating the AC power/current. In this way, the loads are the DC-AC power converters modeled as CPLs at each Load node. In the case of distributed loads along the line, the equivalent lumped model should be applied, following the development from [157], and the load properly added to the nodes in question.

Then, **Fig. 6.6b** shows the equivalent CPL model, where the dependent current source is demanding a current that changes when the voltage changes. **Fig. 6.6c** shows the equivalent linearized CPL

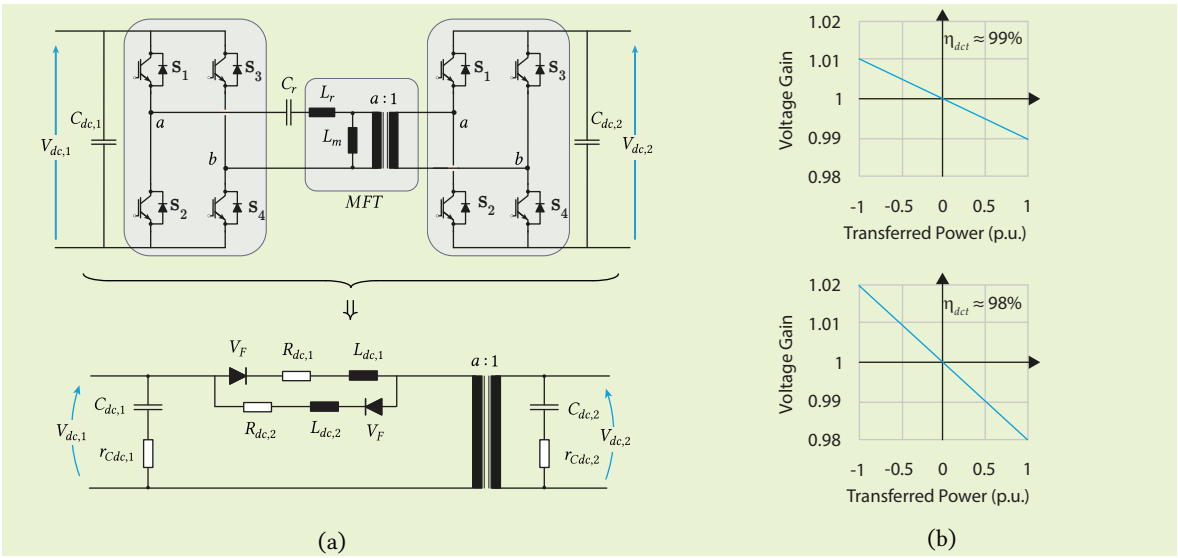


Fig. 6.7 DC transformer; (a) DCT switched model and DCT dynamic equivalent model, (c) dependence of the voltage gain on the power transferred.

model [130], where the dependent current source is considered to have a linear behavior for a given operation point - output voltage V_o, where the load admittance value is:

$$Y_l = -\frac{P_{cpl}}{V_o^2}, \tag{6.15}$$

and the current source,

$$I_{cpl} = 2\frac{P_{cpl}}{V_o}. \tag{6.16}$$

Therefore, the linearized CPL model has its admittance value acting as a gain to the node where it is connected. Its inclusion in the nodal admittance matrix follows the same approach as applied to any shunt element. **Fig. 6.6d** illustrates an expected frequency response of the closed-loop input admittance of the switched circuit **Fig. 6.6a** and the equivalent linearized model **Fig. 6.6c**. It is expected a CPL behavior for the control bandwidth range, while in high frequency, the resonance appears and leads the response to an inductive behavior. This response changes according to the converter and load characteristics, and this figure illustrates the simplifications and valid frequency range of the linearized model.

6.3.3 DC Transformer Equivalent Model

One of the differences from the state-of-the-art analysis in this area is related to the considerations towards the DC transformer. The inclusion of this element in the DC PDN creates the connection between two DC buses, and the power flow in the branch follows the voltage of the nodes. With such behavior, this element can be included in the nodal admittance matrix using the DC terminals' model, presented in **Chap. 2** and repeated in **Fig. 6.7a**.

To create a linearized model, the diodes and the transformer are removed from the equivalent model, by neglecting the power semiconductor losses (which are usually small compared to other losses at

Tab. 6.1 Buried medium voltage cable data [158].

	Value	Unit
Nominal current	1	kA
Voltage	11	kV
Resistance	17.6	mΩ/km
Inductance	0.268	mH/km
Capacitance	0.904	μF/km

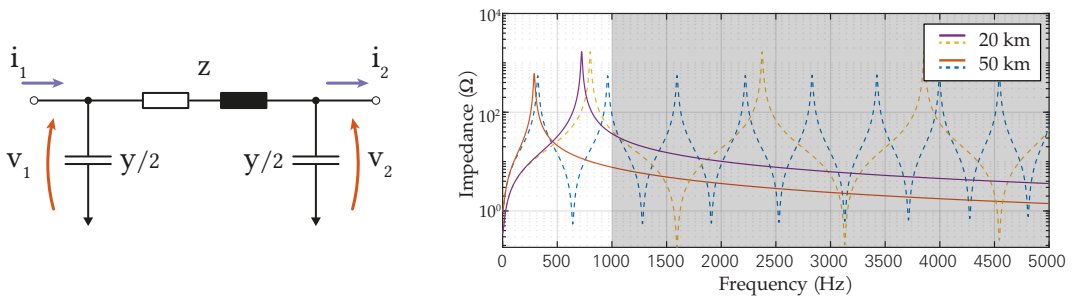
the medium/high voltage level of the system). Therefore, this circuit becomes another element to include in the nodal matrix.

6.3.4 Transmission Line Representation

Lines and cables play an important role in harmonic resonances. Depending on the range of frequency and the length, the effects of the long line become a critical aspect. Also, the capacitive effect of the overhead or buried cables is different, and special care should be given to the transmission line modeling.

When referring to DC systems, it is reasonable to consider that new DC PDNs will be constructed with buried cables, for safety and aesthetic reasons. Thus, a buried medium voltage cable with the data in **Tab. 6.1** is considered for this analysis. **Fig. 6.8b** shows the frequency response for different models; i) using distributed parameters and ii) one section π-equivalent model. Two different cable lengths of 20 km and 50 km are simulated to demonstrate the model difference.

As stated in this figure, the considered cable can be faithfully represented by the one section π-equivalent model for the 20 km cable length until 1kHz, and it is also expected for shorter cable lengths. However, if considering the line of 50 km length, one section π-equivalent model does not correctly capture the frequency response above 500 Hz. Then, more π-sections or a frequency-dependent model should be used to capture the frequency response for long cables faithfully.



(a) (b)

Fig. 6.8 (a) Equivalent π-lumped section. (b) Comparison of the distributed parameters (dashed) and one section π-lumped (solid line) model for the medium voltage cable with 20 km and 50 km length. The shaded part shows the frequency out of the scope of the analysis.

In summary, the transmission lines are modeled as a constant parameter line in only one frequency (f_g = 50 Hz) [144], due to adopted simplifications and limitations of the chosen simulation software. Nevertheless, other models could be used such as the frequency-dependent [159] and the wide-band models [160].

6.4 Evaluation of the Linear Equivalent Representation

The complete linearized circuit is shown in **Fig. 6.9**, using the previously discussed descriptions of the elements. There are three types of nodes in this system: i) Source node (V controlled, I unknown); ii) Load node (V unknown, I controlled); and iii) Floating node - zero injection node (V unknown, I unknown). This description is sufficient once the current is given purely by the voltage difference between nodes. **Tab. 6.2** shows the parameters of the simulation, and **Tab. 6.3** shows the controllers gain. Also, in simulation, the AC grid is modeled as an ideal voltage source and a series impedance of $z_s = 0.001 + j0.01$ p.u. Each transmission line has 10 km of length.

6.4.1 Steady-state Response

At first, the steady-state solution is computed to identify the operation point. The calculation of this part is performed in a per unit system, which bases correspond to the rated power and voltages of the system. Both loads are set to 0.5 p.u. Thus, the first step is to define the matrices of the MNA.

The admittance matrix was built with the following incidence matrix (element\node):

$$\mathrm{a} = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \end{bmatrix}. \tag{6.17}$$

The primitive admittance for the steady-state solution is:

$$y_p = diag(0.0508 \quad 0.0508 \quad 0.0014 \quad 0.0127 \quad 0.0127)^{-1} \tag{6.18}$$

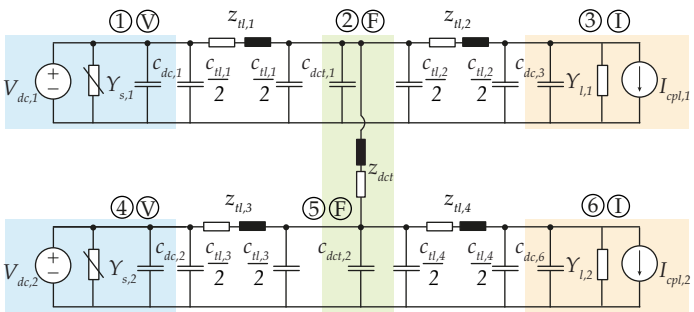


Fig. 6.9 Linearized model of the DC PDN with six nodes and one DCT, two power converters as source and two power converters as load, in node 1 – 4 and 3 – 6 respectively. The voltage sources at nodes 1 and 4 are only illustrative, showing that these are voltage-controlled nodes.

Tab. 6.2 Simulated DC PDN parameters for validating the methodology in PLECS.

	Symbol	Value	Unit
Bus rated power	$S_{1,2}$	10.4	MW
Source grid 1	$V_{dc,1}$	6	kV
Source grid 2	$V_{dc,2}$	12	kV
Load grid 1	$i_{cpl,1}$	866.67	A
Load 1 power	$P_{cpl,1}$	5.2	MW
Load grid 2	$i_{cpl,2}$	433.33	A
Load 2 power	$P_{cpl,2}$	5.2	MW
TL length	l_{tl}	20	km
TL impedance	z_{tl}	$0.0176 + s0.268 \times 10^{-3}$	Ω/km
TL capacitance	c_{tl}	0.904×10^{-6}	F/km
DCT equivalent impedance	z_{dct}	$0.014 + s39.97 \times 10^{-6}$	Ω
DCT capacitance	c_{dct}	8	mF
DCT MFT ratio	$1 : a$	1:2	-
AFE capacitance	c_{dc}	2.5	mF
AFE 1 switching frequency	f_s	5	kHz
AFE 2 switching frequency	f_s	2	kHz
DCT switching frequency	f_{DCT}	5	kHz

Tab. 6.3 Controllers gain.

	Symbol	AFE 1	AFE 2
Voltage Control	k_p	0.2	0.125
Voltage Control	k_i	20	0.05
Anti-Windup V	k_w	10	8
Current Control	k_p	10	6.9
Current Control	k_i	100	0.63
Anti-Windup I	k_w	1	0.15

and then, the nodal admittance is calculated by (6.19).

$$Y_{nodal} = a^T y_p a. \tag{6.19}$$

The matrices to complete the MNA equation are:

$$\mathrm{B}^T = \begin{bmatrix} -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 \end{bmatrix}, \tag{6.20}$$

$$\mathrm{C} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix}, \tag{6.21}$$

$$\mathrm{D} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}, \tag{6.22}$$

and

$$\mathrm{J}|\mathrm{F}^T = \left[\begin{array}{cccccc|cc} 0 & 0 & -0.5 & 0 & 0 & -0.5 & 1 & 1 \end{array}\right]. \tag{6.23}$$

Therefore, solving (6.9) for x, the voltages of the nodes and the current for the two voltage sources can be found. **Tab. 6.4** shows the steady-state solution comparing Part I - Steady-state calculation of the methodology computed in Matlab and the switched model simulated in PLECS. It shows the voltage and current of the system, with good matching of results. The current direction is stated in **Fig. 6.4**.

Tab. 6.4 Steady state solution comparing the solution from MNA computed in Matlab and the switched solution simulated in PLECS.

Voltage	Calculated	Simulated	Unit
Node 1	6	6	kV
Node 2	5.937	5.936	kV
Node 3	5.784	5.783	kV
Node 4	12	12	kV
Node 5	11.879	11.878	kV
Node 6	11.8032	11.803	kV
Current	Calculated	Simulated	Unit
Node 1	358.22	360.39	A
Node 4	687.55	687.67	A
DCT	-254.22	-254.30	A

6.4.2 Nodal Impedance assessment

The RMA can be computed as described by [152], and the nodal impedance can be extracted, as well as its resonance characteristics.

For Part II - Frequency domain solution, the nodal admittance matrix is computed with the same incidence matrix, including the inductance in the primitive admittance vector. The calculation for this part is performed in SI values. This choice is just for convenience as the switched model in PLECS is computed in SI values. If using per-unit values, the correct base should be used to find the impedance value for the desirable side after the calculation. Thus, before including the impedances to the admittance nodal matrix, it is necessary to reflect all the parameters correctly to the desirable node's side before computing H_z in (6.7). Then, for the nodes at the lower voltage side, this yields,

$$y_p = diag(10.z_{tl} \quad 10.z_{tl} \quad z_{DCT} \quad 10.z'_{tl} \quad 10.z'_{tl})^{-1}. \tag{6.24}$$

where $z'_i = 1/a^2.z_i$, and the construction of Y_{nodal} follows equation (6.19).

The shunt capacitance matrix and control equivalent matrix also need to be reflected to the lower voltage side for calculation. Then,

$$C = diag(c_{dc} \quad c_{DCT} \quad c_{dc} \quad c'_{dc} \quad c'_{DCT} \quad c'_{dc}), \tag{6.25}$$

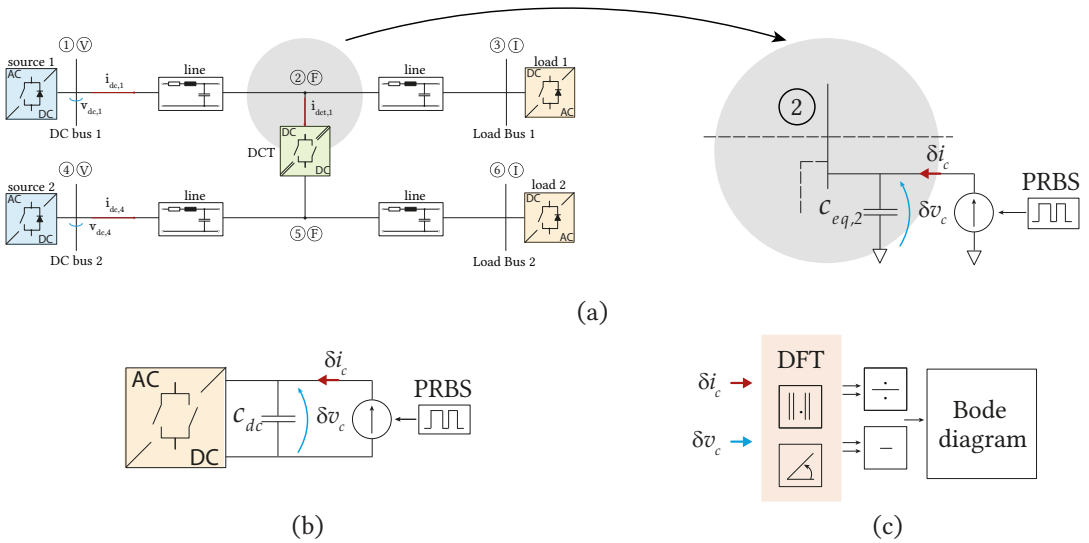


Fig. 6.10 Impedance measurement procedure for a (a) DC PDN node, and (b) at the DC terminals of DC-AC converters. (c) Bode plot process after extracting the current and voltage perturbation measurements.

and,

$$T = diag(Y_{s,1} \quad 0 \quad Y_{l,1} \quad Y'_{l,2} \quad 0 \quad Y'_{s,2}), \tag{6.26}$$

where $c'_i = a^2.c_i$ and $Y'_i = a^2.Y_i$.

To select the desirable transfer function from (6.13), vectors V and I act as pointers, where I is the current injection in a certain node and V is the resultant voltage of a certain node.

Therefore, as an example, if it is desired to compute the impedance of node 3, all the elements of V and I of (6.13) are zeros, except for the 3rd row that has value 1, thus:

$$V_3 = H_{3,3}I_3, \tag{6.27}$$

where $H_{3,3}$, is the impedance transfer function of node 3.

Thus, the nodal impedance is computed and compared with the measured impedance in PLECS. The impedance/admittance measurement in PLECS can be carried out by injecting a multi-tone perturbation as current/voltage at the terminals and by measuring the corresponding voltage/current. Therefore, the ratio of the measured signals gives the impedance/admittance at frequencies of interest.

While measuring the impedance response of a specific DC PDN node, the perturbation is injected into the node and measured in the same node. The process is illustrated in **Fig. 6.10**, for any power converter and for the DC PDN Node. In this simulation, the signal was generated by a 12-bit-length shift register resulting in a 4095-bit-long Pseudo-Random Binary Sequence (PRBS) signal. The sequence was generated with a 5 kHz generation frequency, which sets the injection time at 0.819 s [161]. Therefore, after recording the current and voltage of interest, taking the Discrete Fourier Transform (DFT), and plotting it in the bode diagram, one can determine the impedance characteristic in the frequency domain. The capacitor $C_{eq,2}$ in **Fig. 6.10** represents the equivalent capacitance of the node, which is, in this case, the sum of the DCT capacitor and the contribution of the π-equivalent of the transmission line.

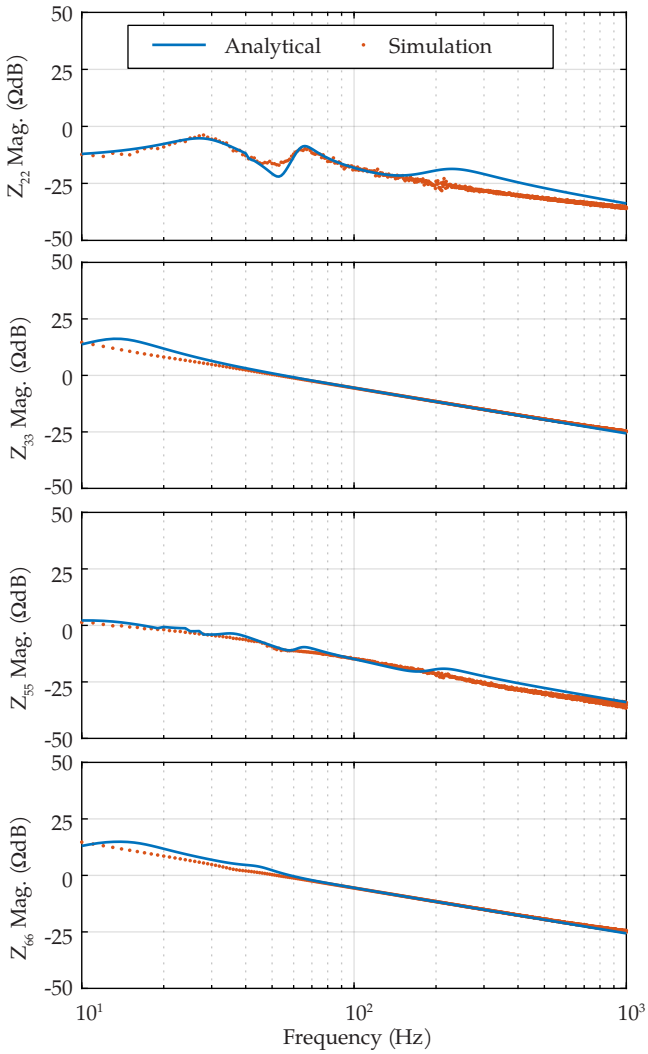


Fig. 6.11 (a) Impedance characteristic of nodes 2, 3, 5, 6, from RMA and impedance measurement from the switched system in PLECS.

Finally, **Fig. 6.11** shows the node's impedance for Nodes 2, 3, 5, and 6, using RMA (nodal impedance) and the impedance measurement on the switched system in PLECS. The Z_{mn} response means the impedance characteristics for the current injection in node m and voltage measurement in node n. This subscript brings the information of the transfer function location in the RMA matrix and the node or branch of interest in the system. The method faithfully identified the system's resonances and followed the impedance magnitude within the frequency range of interest.

The mismatch around 200 Hz and 300 Hz is due to the DCT model, whose equivalent circuit (dynamic equivalent model) does not map all the passive elements, in particular the resonant capacitor. Yet, it is interesting to note (comparing Z_{22} and Z_{55}) that the lower voltage side has its resonances less damped than the higher voltage side.

Identifying the nodes' impedance is an essential step to understanding the whole system behavior in the frequency domain. With the information provided by **Fig. 6.11** one can identify the nodes

that have features close to the source's or load's behavior, the critical resonance frequencies, and the impact of the voltage level on the impedance characteristic, for example.

Besides that, from **Fig. 6.11**, it can be concluded that the DC PDN has a certain impedance at the connection point and the possibility of adding new elements to the grid can be studied, investigating the resonances and the stability of the systems. All these analyses and others are performed in the next chapter.

6.5 Summary and Conclusion

This chapter presented the developed methodology to analyze the DC PDN with DCTs, computing the steady-state solution (load flow) and the frequency characteristics (nodal impedance) in a purely DC system. The solution was divided into two parts, and simulations were performed to evaluate the method.

The solution of Part I - Steady-state overcomes the lack of angle and reactive power to calculate the power flow using a nodal approach, allowing the extensibility of the methodology. Part II - Frequency domain analysis, provides the frequency characteristic of the systems by computing the node's impedance, showing that this approach computes the impedance correctly within the voltage control bandwidth. These solutions can be used for the DC power system analysis and allow further investigation in this area.

Although this methodology is scalable, it has some limitations. Due to the fact the power converters are linearized with simplifications, the error of representation sums up and might lead to wrong results for large systems. Also, this method relies on the resonant modal analysis with the admittance models for the frequency representation, which can use the eigenanalysis theory for the system analysis, however, it lacks the representation of the states of the system for the dynamic response evaluation.

In the next chapter, this methodology is used to investigate the impact of the DCT in the DC PDN, further investigating the element's participation factor, the node's contribution to the resonances, and other aspects using the developed models.

7

Nodal Impedance and DC System Analysis

This chapter assesses the impact of the DCT on the system's characteristics. It delves into various aspects, such as the DCT's location in the grid, the dynamics of AC-DC converter control, and the impact of the introduction of an additional power converter to the system. Additionally, it covers stability analysis for DC PDNs and explores diverse network architectures within a dynamic power flow context. Finally, this chapter evaluates several scenarios exploring the aspects of planning, operating, and stability analysis of DC PDN using the proposed methodology.

7.1 Introduction

The resonance characteristic of the system is composed of several elements, such as the power converters, transmission line, network configuration, etc., and identifying the critical nodes and frequencies of the system is an important metric for the operation, planning, and stability analysis. In particular, there is one key question to be answered: Where can new equipment be added without creating any or significant disturbances to an already stable and performing system? To answer this question, information about critical nodes is essential to find the proper location and identify possible unstable conditions.

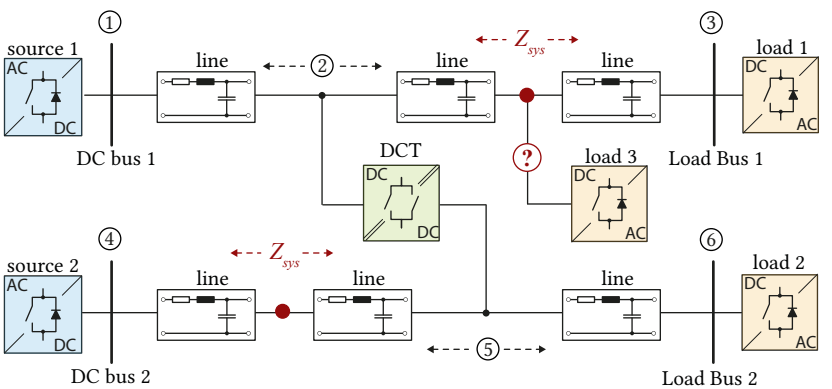


Fig. 7.1 DC power distribution network with six nodes and one DCT. Nodes 2 and 5 change their location for the system evaluation. Red dot pointing to an arbitrary location on the transmission line to the impedance measurement. An extra element ready to join the PDN.

In this chapter, the DC PDN of **Fig. 7.1** is investigated in all three aspects: i) Operation - the impact of the DCT as an open-loop element on the steady-state response of the system; ii) Planning - the addition of an extra converter to the system and its effects on both steady-state and resonance responses; and iii) Stability - the metrics to verify the stability of the system and its application. In the

following sections, all these studies are performed using the developments of **Chap. 6** and compared with simulation results in PLECS.

7.2 Impact of DCT on the DC PDN Characteristics

In this section, the impact of the DCT on the power flow and on the nodal impedance is investigated. The system under analysis is shown in **Fig. 7.1** and the data was presented in **Chap. 6**.

7.2.1 Power Flow Characteristic

For the system shown in **Fig. 7.1**, the operation aspect is given by the power sources which regulate the voltage, the loads of the system, and the DCT which is the connection path for the power exchange between the buses. However, as the DCT transmits power according to the voltages at its terminals, its location on the DC PDN changes the power flow and influences the loading of the converters.

In practice, the DCT could be connected in any location along the transmission line, as its position is assumed uncertain for an exemplary system. In this way, by changing the DCT's connection point both the power flow and the nodal impedance changes. To investigate this effect, a simulation was carried out changing the connection points along the transmission line.

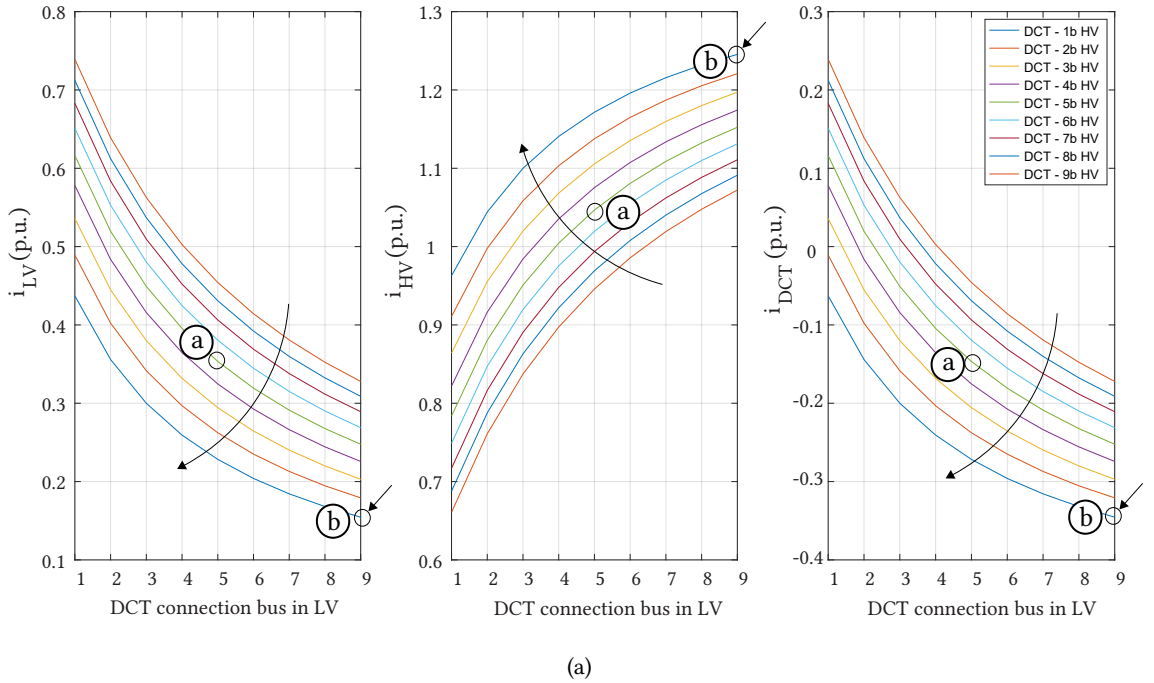
It is assumed that the two DC buses have 20 km of transmission line length, to which the DCT can be connected. The simulations to evaluate the impact of the DCT were performed by changing the connection point by 2 km from the previous location for each new iteration. In this way, one DCT's port has 9 possible positions in a 20 km long bus, and each connection has a sequential code starting from the source to the load. The "LV" and "HV" codes represent the lower voltage (Grid 1) side and higher voltage (Grid 2) side, respectively. For example, if one DCT's port is connected within 2 km from the Grid 1 source power converter, this point is called "1-LV", whereas if the other port is connected 18 km from the Grid 2, the point is called "9-HV",

Fig. 7.2 shows the results for the impact of the DCT on the power flow. **Fig. 7.2a** shows the currents at the power source nodes (Node 1 and 4), and the DCT current. It can be seen that the DCT branch provides a low-impedance path for the HV side to feed the load on the LV side. Also, depending on the DCT's location on the DC PDN, the system might result in a forbidden configuration, overloading the HV source. In this figure, two scenarios are highlighted and exemplified in **Fig. 7.2b** and **Fig. 7.2c** marked with ⓐ and ⓑ.

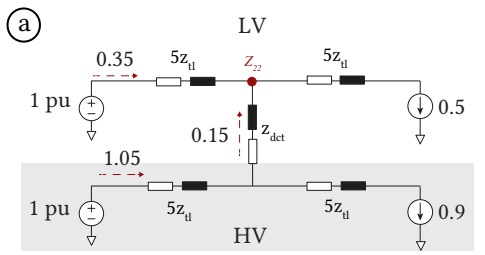
In the scenario marked as ⓐ, the DCT connection points are in the middle of the transmission line. It can be seen in this example, that the HV voltage side feeds its own load plus a fraction of the load on the LV side. This behavior is mostly due to the higher voltage bus that sees the transmission line with lower resistance, and therefore, has a lower impedance path to feed the load. In other words, the losses on the HV side are lower. Consequently, the power source manages to impose a well-controlled voltage for longer distances, without any voltage drop. This leads to a higher voltage at the DCT terminals compared to its equivalence on the LV side.

For the case marked as ⓑ, the DCT is connected close to Grid 2, and far away from Grid 1. In this situation, the impedance path to the HV side to feed the LV side load is even lower than in the previous case. This leads to a configuration that overloads the voltage-controlled converter of the HV side. Thus, a strategy to operate this system will have to be implemented, which could involve

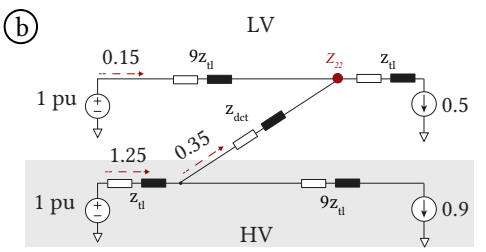
some coordination between the two DC voltage nodes, modifying the voltages, or limiting the power injection of the HV side. This shows that a supervisory system is required for DC PDNs as it is required for AC distribution grids.



(a)



(b)

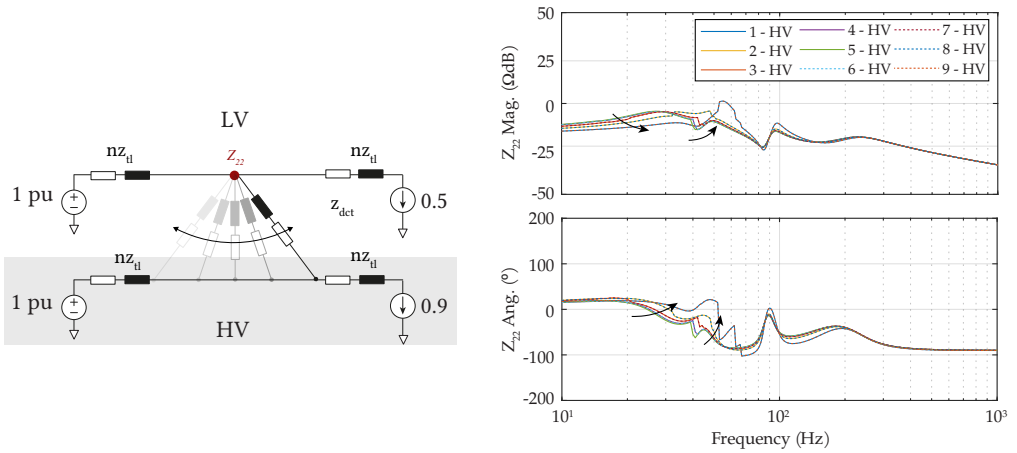


(c)

Fig. 7.2 Impact of the DCT on the power flow of the system. (a) Sources' current and DCT current for different connection points of the DCT. In this example a 2 p.u. system is feeding 1.4 p.u. load, hence the underutilization of the DCT. (b) and (c) an exemplary case marked as ⓐ and ⓑ on the current plot. The variation on the HV bus is represented by a different color and the LV bus on the x-axis.

7.2.2 Impedance Characteristic

The DCT impacts both the load flow and the nodal impedance of the system. This characteristic is affected by the new operating point and new resonance characteristics. Similarly to the previous simulation, the DCT's connection moves 2 km each step, but now, one side remains fixed. **Fig. 7.3** shows the frequency response of Z_{22}, with a fixed point at the LV side.Node 2 was chosen to demonstrate the impact of the DCT due to its lower damping in some frequency ranges.



(a) (b)

Fig. 7.3 (a) Exemplification of the case under analysis with the fixed point at the LV side, varying the HV side. (b) Impedance characteristic of Node 2, with fixed DCT LV connection point (2-LV). The arrows represent the movement of the response when the DCT connection point approaches the extremes of the HV bus.

Fig. 7.3a shows the case under study, and **Fig. 7.3b** shows the frequency response of the nodal impedance, where the arrow represents the movement of the DCT connection to the extremes of the transmission line. The fixed point at the LV side is 2-LV (4 km from the voltage source and 16 km from the load), and the possible connections on the HV side are from 1-HV to 9-HV.

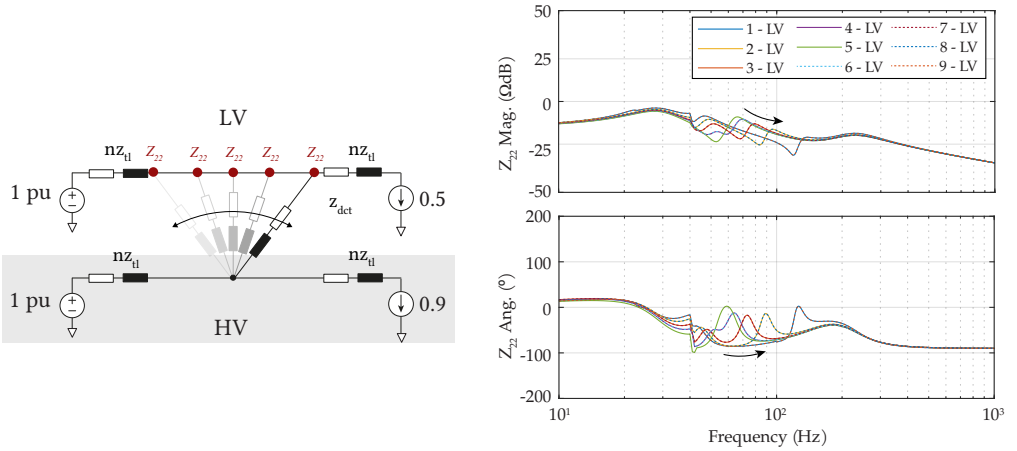
While changing the connection on the HV side, the DC gain is changing due to a new operational point, and the resonance around 40 – 60 Hz moves to higher frequencies with less damping when the DCT is approaching the extreme points of the bus. Due to the symmetry of this example, the impedance response when moving the DCT connection point to the right half side is the same for the left half side of the transmission line - assuming that there is no control action from the converters.

On the other hand, **Fig. 7.4** shows the frequency response of Z_{22}, with a fixed point at the HV side. **Fig. 7.4a** shows the example under study with a fixed node at 4-HV, and the connection in the LV side varied from 1-LV to 9-LV. For this situation, the resonance around 40 – 60 Hz moves to high frequency while decreasing its magnitude, for DCTs' connection points approaching the extremes of the transmission line, as shown in **Fig. 7.4b**.

In both situations, the operation point changes, and to keep the analysis accurate, it is crucial to verify that this new scenario is a valid solution of the system. It means verifying that the steady-state solution exists for such configuration (within the boundaries of operation). All the presented results do not violate any voltage/current limits. Moreover, according to both figures, it can be concluded that in order not to reduce the damping due to the DCT location, allocating it to the middle of the line would be the best option, even though this may not be possible in all scenarios.

7.2.3 Impedance Measurement Point

The impedance measurement point is an artificially created node that changes its position on the bus to identify the impedance characteristic at different points of the system. For a specific DCT location



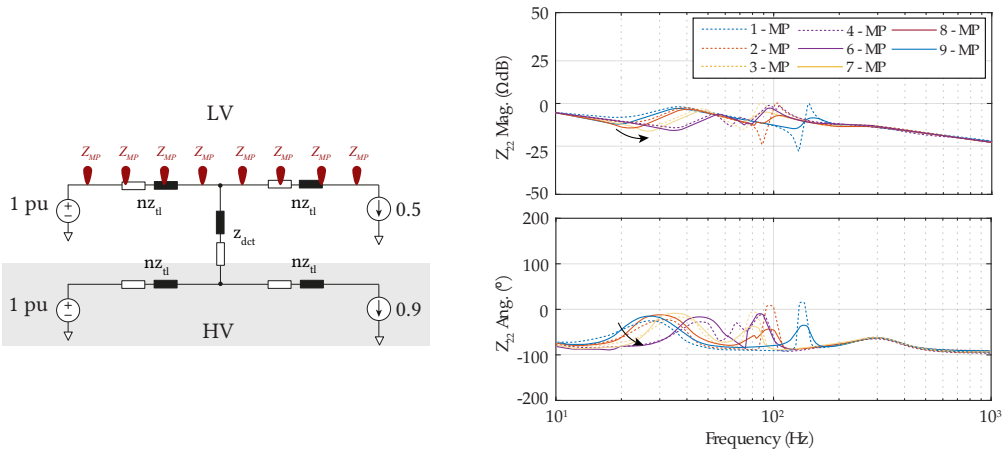
(a) (b)

Fig. 7.4 (a) Exemplification of the case under analysis with the fixed point at the HV side, varying the LV side. (b) Impedance characteristic of Node 2, with fixed DCT HV connection point (4-HV). The arrow represents the movement of the response when the DCT connection point approaches the extremes of the LV bus.

and operational point, this point measures the impedance at the connection point to evaluate its value (see red dot in **Fig. 7.1**).

For this part, the DCT connection point is assumed fixed at 5-LV:5-HV. Therefore, the system can be constructed with an extra node, and its connections depend on the desirable measuring point. The analysis is performed with the same as before, only now, with an extra node.

Fig. 7.5a shows the measurement points in the LV side from 1-LV to 9-LV, excluding 5-LV which is the DCT connection. In **Fig. 7.5b**, the impedance from the right side of the DCT is shown in a solid line and the left side is in dots. The nomenclature 1-MP means 2 km from the grid and 18 km from the load. The responses of the right side of the DCT (load side) have more characteristics of load type with more damping than the measured points on the source side, in the frequency range under analysis. It can be checked by comparing 1-MP and 9-MP both in blue, where the dots have less damping and the contribution of the source's controller (Y_s) is higher (which is in lower frequency compared to the current-control loop). The measuring point in the HV side results in the same results, once the system has the same features. With this information, one can identify the best location for adding another element to the grid, using classical impedance-based stability analysis as in [162].



(a) (b)

Fig. 7.5 (a) Impedance characteristic of measurement point in LV side of the dc power system with DCT in 5LV-5HV. The arrows represent the movement of the response when the DCT connection point approaches the extremes of the LV bus.

7.3 Extending the System with an Additional Power converter

In order to check the impact of the inclusion of a new power converter to the grid and its effect on the system, a new converter, considered as load, is added to the analytical model in order to calculate the resultant system's impedance characteristic.

Let us consider that a new controlled power converter (load type) will be added to the LV side. The DC PDN is built as **Fig. 7.1**, with a DCT connection in 5-LV:5-HV, and it is desirable to study the possibility of including it at Node 2 or 3. The admittance of the power converter before connecting the DC PDN is measured and shown in **Fig. 7.6**, highlighting that the CPL behavior is predominant in the frequency range of interest, and **Tab. 7.1** details the converter parameters.

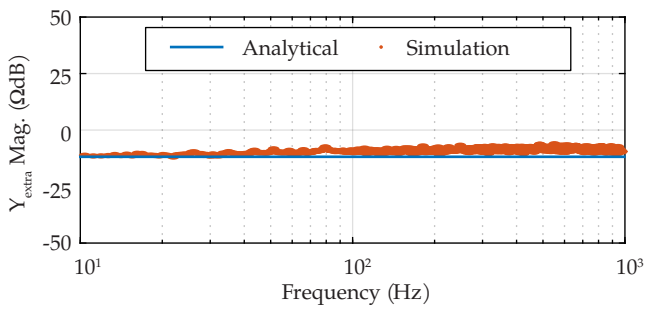


Fig. 7.6 Admittance response of the extra power converter using the linearized model and the impedance measurement from the switched system in PLECS, operating in 40% of nominal load.

The main goal is to verify the equivalent impedance response of the system and the time domain simulation after including the additional power converter. From the impedance response point of view, a crucial point is the system's resultant impedance from the sources. The complete system is seen as a

Tab. 7.1 Extra power converter information.

	Value	Unit
Rated power	10.4	MW
Voltage	6	kV
AFE switching frequency	2	kHz
CC k_p	2.2	Ω
CC k_I	0.2	Ω/s

load by the sources, and the sources will feed the system through its connection point. Therefore, the impedance response of the Nodes 1 and 4 are computed to identify their critical resonances. **Fig. 7.7** shows the desired impedance characteristics.

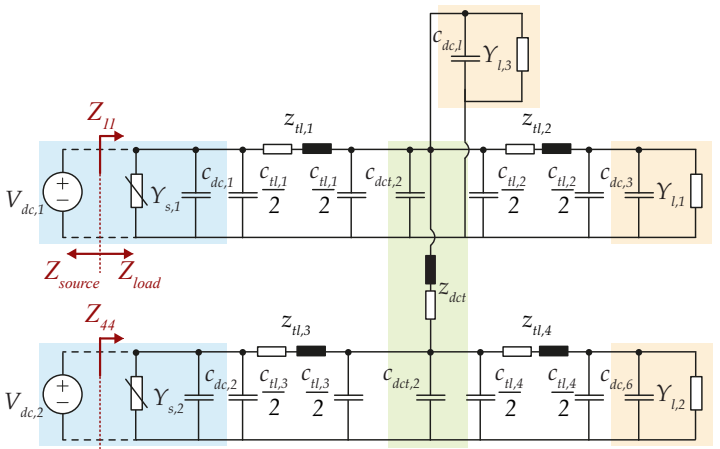


Fig. 7.7 Source's impedance nodes. Nodes 1 and 4 are the power sources' nodes and the remaining system is a load—extra power converter connected to Node 2, with negligible line impedance.

Fig. 7.8 shows the simulation results. For this analysis, it is assumed that the system is stable only if the voltage oscillation is below 5% in per-unit values (i.e., 0.05 pu), after that, the system is considered oscillatory, although still stable according to stability criteria (shown in details in the next section). Further, the transient response is not of interest to the analysis.

Firstly, the new converter is connected in Node 3, and the new impedance response of Nodes 1 and 4 are shown in **Fig. 7.8a**. The new power converter increases the low band gain of the nodes' impedance response (as seen on the left plots of **Fig. 7.8a**). As expected, the system has a very high impedance in this frequency range, where the voltage control loop operates. It creates a disturbance feedback that impacts the current control task of regulating the current, and impacts the node voltage. Thus, this controller operates saturated for a long period, leading to the oscillations shown in **Fig. 7.8a**.

In another scenario, the power converter is now connected to Node 2. The inclusion of the new converter in this node has a similar impact on the nodes' impedance response, increasing the low band gain and reducing the damping. However, unlike the previous case, the sum of all the capacitances connected to this node is lower, leading to a fast voltage dynamic. Therefore, the new impedance response is shown in **Fig. 7.8b** with a notable difference between 10 Hz and 70 Hz.

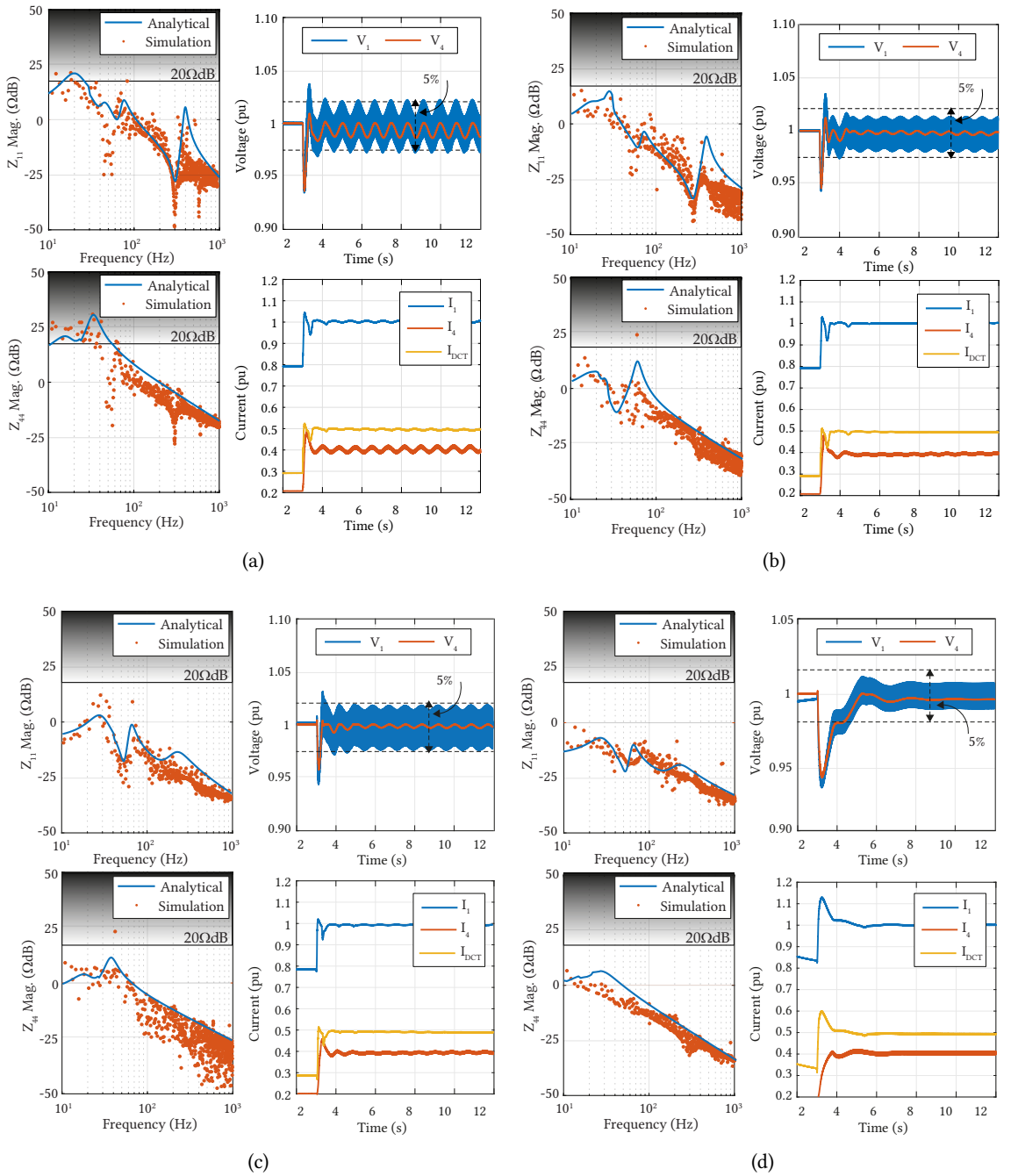


Fig. 7.8 Impedance response of Z_{11} and Z_{44} from RMA and using the switched circuit in PLECS on the left, and on the right the time domain simulation in PLECS with voltages and current of the Source's nodes and DCT current. (a) Oscillatory case, with extra power converter in Node 3. (b) Stable case, with extra power converter in Node 2. (c) Stable case, with extra power converter in Node 3, and new gains for the HV side. (d) Stable case, with extra power converter in Node 3, and new gains for LV side. The shaded part is the drafted stable limit rule. Time waveforms are filtered for the switching frequency.

Tab. 7.2 Controllers gains.

	Symbol	New AFE 1	New AFE 2
Voltage Control	k_p	0.2	0.125
Voltage Control	k_i	2	0.5
Anti-Windup V	k_w	10	8
Current Control	k_p	10	6.9
Current Control	k_i	100	0.63
Anti-Windup I	k_w	1	0.15

Fig. 7.8b shows the sources' voltages and currents and DCT current for this case. Therefore, the new power converter, connected to Node 2 of the DC PDN, resulted in a stable case with a voltage variation below the defined limit.

Let us now consider that the same power converter demanding 0.4 pu of current on the LV side needs to be added to Node 3. There are still several parameters to be modified to change system characteristics and make this feasible. One of the typical approaches is changing the controllers' gains. Even though these parameters are not always accessible by the operator, this simulation is performed to verify their impact on the proposed method.

Two new integral gains are used as an example to modify the system's dynamic, making it faster and slower. The first situation is given by letting the voltage control of the HV side be ten times faster than the magnitude optimum tuning [163]. The new controllers gain are available shown in **Tab. 7.2**

Fig. 7.8c shows the impedance of Nodes 1 and 4 for the load connected at Node 3 for the different controller gain on the HV side. The impedance behavior shows less damping in some frequencies but not elevated gain in low frequencies. In **Fig. 7.8c**, it is possible to note that the response is faster than in the case shown in **Fig. 7.8a**, and the system stayed well-behaved for a long period.

Now, returning the HV side voltage control gains to their original values and decreasing the integral gain of the LV side by ten times. **Fig. 7.8d** shows the frequency and time response. It is possible to note that the system is predominately capacitive, not having high gain in low frequencies. Thus, although being notably slow, the time response of the system regulated the voltage/current properly.

An infinite set of combinations could be performed to determine the system operability, however, the idea is to demonstrate that with the nodal impedance information, it is possible to identify possible oscillations on the DC grid as well. Furthermore, the impact of the linearized control loop shows a significant impact in the low-frequency range when changing the controller gains, which is a point to be investigated for a fully controlled DC system to achieve optimal operation behavior.

Finally, by checking the nodal impedance it is possible to identify the system's behavior and predict some operational challenges. However, in the sense of stability investigation of the system, the direct comparison usually used with a power converter, e.g. Generalized Nyquist Criterion (GNC), cannot be directly applied with the nodal impedance information. Thus, the stability assessment using the nodal impedance is discussed in the next section.

7.4 Resonance Modes and Stability Assessment

Although the previous analysis showed the impact of the addition of an extra converter in certain nodes making the system oscillatory, it did not show the metrics for the evaluation of the system from a stability point of view. This section aims to describe the stability analysis of the DC PDN with DCT.

7.4.1 Impedance-based Stability Analysis

The impedance-based stability analysis of systems with IBR has been used and studied over the years due to its advantages when dealing with power converters. Such advantages are i) the simple representation of the converters by its Norton or Thevenin equivalent circuit; ii) the possibility of black-box representation with frequency scanning; and iii) a scalable solution for large systems.

With this technique, two approaches can be used for system analysis. The first approach is usually referred to as single bus analysis, which relies on the GNC to evaluate the stability of the system [164], [165]. In this case, the stability assessment is carried out by calculating the bus admittance, defined by all the terminal admittance connected to the node as the stability indicator [166], [167]. This approach is usually used in works investigating the interaction between converters and system [162], focusing on the control design of converters [168].

The second approach is using the overall system model to directly evaluate the system stability from the frequency domain nodal admittance matrix [169], [170]. In this case, the stability assessment is performed by checking if all the modal resistances are positive [171], or by acknowledging the phase crossing of the eigenvalues [172], among other methods [165], [173]. Besides that, the critical nodes of the systems can be computed based on the frequency-domain participation factor analysis [174], highlighting the critical resonances and the damping of the system [175]. This solution is usually used for the purpose of converter location optimization [170], and investigations on the critical modes of the system [141], [173]. The relationship between the two approaches was studied in the literature and, although the methods represent different stability information [176], they are relatable and commutable for certain special cases [177].

In this sense, the multi-bus analysis is preferable to perform the stability analysis on the system-level DC PDN. This approach can use the same admittance matrix to evaluate the stability of the system. Thus, in this section, the system under analysis will be used to exemplify the stability assessment of the DC PDN.

7.4.2 Stability Assessment of DC PDN

The system under analysis is the six nodes DC PDN with one DCT, shown at the beginning of this chapter (redrawn in **Fig. 7.9** for clarity). It is assumed that the extra converter was added in Node 3, resulting in the oscillatory behavior shown in **Fig. 7.8a**. However, the system was not unstable, as verified in simulations, it only has an oscillatory behavior.

Fig. 7.10 shows the details of the waveforms of the simulated system. This figure shows the voltage at Nodes 1 and 4, which are voltage-controlled nodes. From this waveform and the FFT analysis, it can be noticed that a few harmonics are present. At Node 1, the oscillation of 300 Hz is predominant, similar to Node 4 which also has the switching frequency content at 2 kHz. In low frequency, there is an oscillation of 50 Hz in both waveforms, which can be noticed in the peaks of the blue curve.

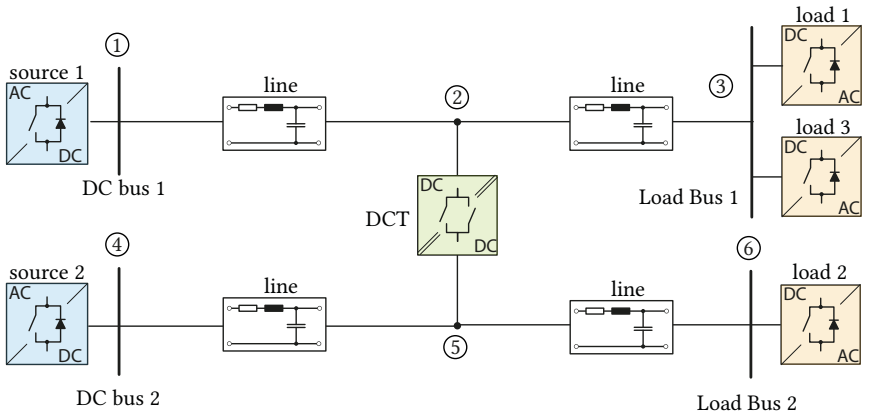


Fig. 7.9 DC power distribution network with six nodes and one DCT. The DCT is connected to position 5-LV:5-HV. An extra element connected to Node 3 with negligible line impedance.

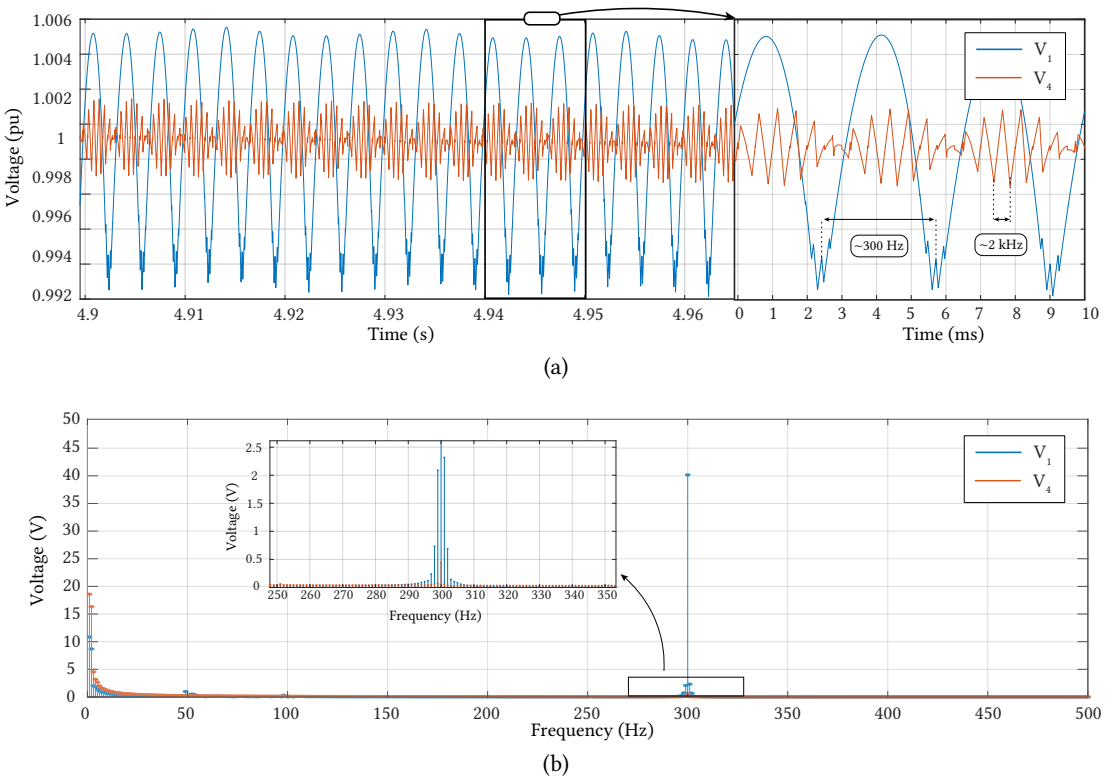
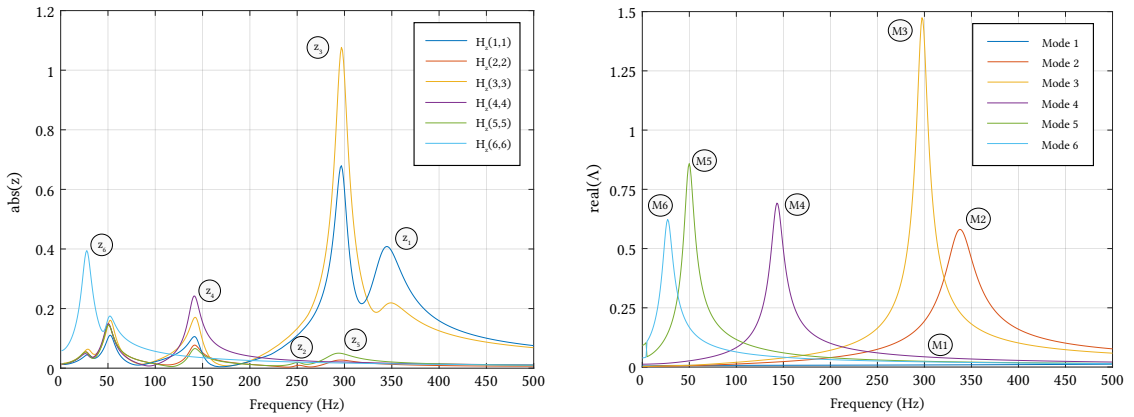


Fig. 7.10 (a) Voltage waveform of Node 1 and Node 4 and (b) FFT of the voltages. The most critical frequency is around 300 Hz.

Such oscillations are explained by plotting the driving point (i.e. transfer impedance) and the modes of the system in **Fig. 7.11**. Essentially, the driving points of the system show the elements of the matrix that exhibit a resonant condition, but not directly the node of the system. Each transfer function contains the contribution of all the branches connected to its node. On the other hand, the modes are the signature of the complete system, which represents the resonances of the system, and brings

the information where each mode experiences its resonance. This is useful to identify the nodes contributing to a specific frequency and act on it if needed.



(a) (b)

Fig. 7.11 (a) Driving points, showing the behavior of the transfer impedance over the frequency. (b) Modes of the system, showing the resonance modes for the system under analysis. Λ is the diagonal eigenvalues matrix of the system.

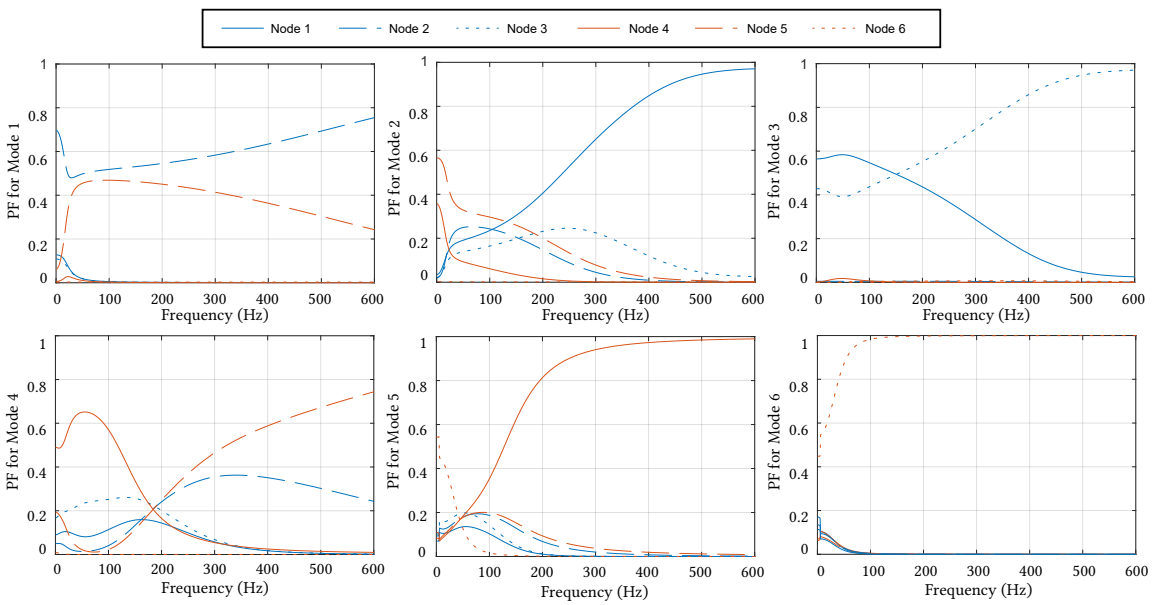
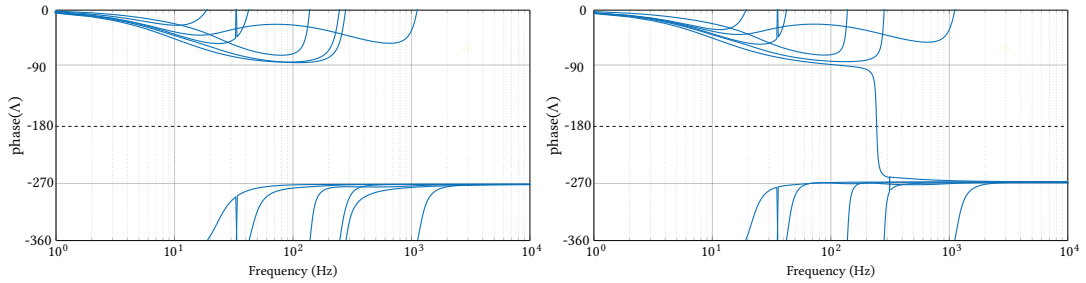


Fig. 7.12 Participation factor of each Node to the each Mode. The blue line represents the nodes on the LV side, and the orange is the HV side.

It can be noticed in **Fig. 7.11b** that Mode 3 has the higher peak among the modes in this range of frequency. Thus, to identify the nodes that contribute to each node, **Fig. 7.12** shows the participation factor for each mode in this range of frequency. First, one can see in the participation factor for Mode 3 that the Node 1 and Node 3 share its responsibility up to 400 Hz where Node 3 is predominant. At



(a) Stable case (b) Unstable case

Fig. 7.13 (a) Phase plot of all eigenloci for the frequency range under analysis with a stable case. (b) Phase plot of all the eigenloci for the unstable case.

the moment of the resonance Node 1 has $PF \approx 0.3$ and Node 3 has $PF \approx 0.7$, and all the other nodes have almost no contribution to this mode.

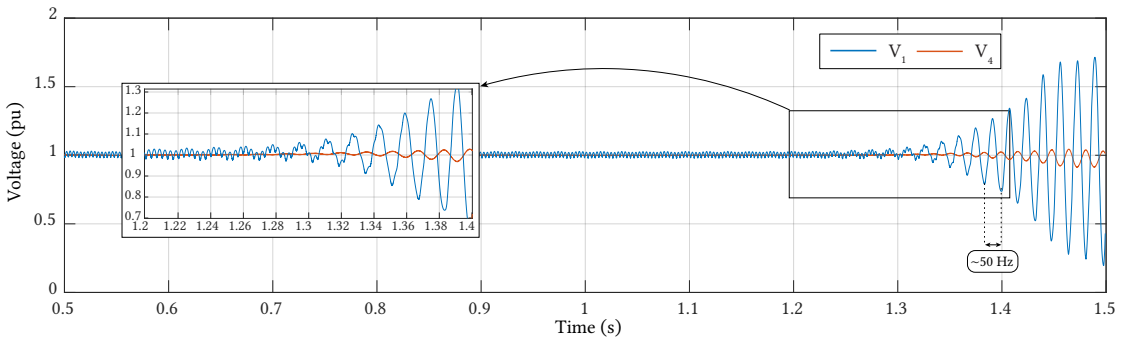
The other two important modes are Mode 2 and Mode 5 where the predominant node is the two source nodes of the system. Mode 2 has its resonance between 300 Hz and 350 Hz and is mostly dominated by the source of the LV Side. Mode 5 on the other hand, has the second-highest peak contribution for the resonances of the system, and Node 4 which is the source of the HV side, has a big participation factor for it. It is worth mentioning that these resonances concern the system configuration, the transmission line, and considered converters described in the previous chapter.

Fig. 7.13a shows the phase plot of all eigenloci of Y_{nodal} for the entire system, including control loops. Notably, within the analyzed frequency range, no phase crossing of any eigenvalue is observed, confirming the system's stability. The inclusion of a phase plot offers the added benefit of identifying the frequency at which phase crossing occurs in the event of system instability.

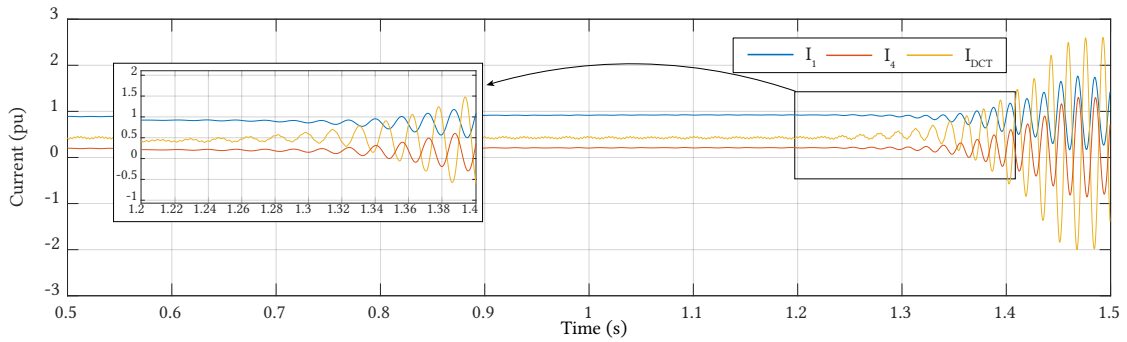
Now, let's assume a poor controller tuning for the voltage controller of the LV source converter, with the bandwidth of 100 Hz ($k_p/k_i = 0.2/200$). This is essentially the opposite of the simulation of **Fig. 7.8d**, making the integral gain ten times bigger. In this case, the voltage controller will amplify the 50 Hz oscillation and cause the instability of the system. Other scenarios could be performed to trigger instability, however, modifying the controller gains does not alter the operating point of the system, which excludes the impact of other converters on the analysis.

Fig. 7.14 shows the simulation results for the system with new controller gains. At time $t = 1$ s the news gains are implemented for demonstration and after a few seconds, the system collapses. **Fig. 7.13b** shows the phase plot of the eigenvalues for this case. One can note that in this system with these controller gains, there is one eigenvalue that has a phase crossing. Using this criteria [172], a system is considered unstable if the number of downward phase crossing points is different from the upward phase crossing points, which in this case is different.

With this example, the stability assessment of the DC PDN system with DCT was demonstrated using the well-established stability criteria for analyzing AC and hybrid AC-DC systems. This allows the use of this methodology for larger systems, and further, considering black box models of the power converter which can improve drastically the converter representation.



(a)



(b)

Fig. 7.14 (a) Voltage and current waveform of Node 1 and Node 4 and (b) Current of Node 1, Node 4 DCT. Simulation with new integral gain for the LV source converter at 1 s, resulting in an unstable case, as predicted by the phase plot of the eigenvalues in **Fig. 7.13b**.

7.5 Investigation on Different Network Architectures

In order to investigate the planning of the DC PDN, the methodology described in **Chap. 7** can be used to compare different PDN architectures. The evaluated distribution system was adopted from [178], creating a DC DPN as the energy distribution system. In total 3 cases were demonstrated in [178] which were adapted and evaluated using this methodology in [179].

One of the systems under analysis is the district of Chapelle-sur-Moudon in Switzerland. This district consists of 57 residential blocks and 9 farms with a total of 88 consumers. There are two PV production plants, one with a peak installed power of 72 kW, and another with 192 kW [178]. **Fig. 7.15a** shows an areal view of the district and **Fig. 7.15b** shows the existing AC distribution grid. From this schematic, the DC PDN was projected.

The power converters were selected by the maximum power and voltage ratings required. There are four types of power converters in this system; i) AC-DC source, 1 unit, ii) DC-AC load, 6 units, iii) DCTs, 2 units, and iv) PV source, 2 units. the power converters were selected according to table **Tab. 7.3**, based on the maximum power of each node.

Tab. 7.4 shows the data of the aggregated consumption for each load node and the maximum generation of the photovoltaic panels. Each load node corresponds to a few consumers classified by zones (based on location). The lines were drawn following the streets, assuming better accessibility and the PVs

(a) (b)

Fig. 7.15 (a) Aerial view of Chapelle-sur-Moudon (District case) with the location of the grid (blue), 6 consumers (white), and 2 PVs (yellow). (b) Actual power grid at Chapelle-sur-Moudon demo site [178].

Tab. 7.3 Power converter characteristics

Type	Power (kW)	Voltage (kV)	Number of units	C_{dc} (mF)	f_s (kHz)	VC k_p/k_i	CC k_p/k_i
AC-DC Source	500	3	1	10	2	0.125/0.5	6.9/0.63
DC-AC load	60	3	5	5	2		6.9/0.63
DC-AC load	30	1.5	1	5	2		6.9/0.63
PV Source [1]	100	1.5	3	2			
DCT	200	3:1.5	2	2	5		

[1]PV modeled as a current source

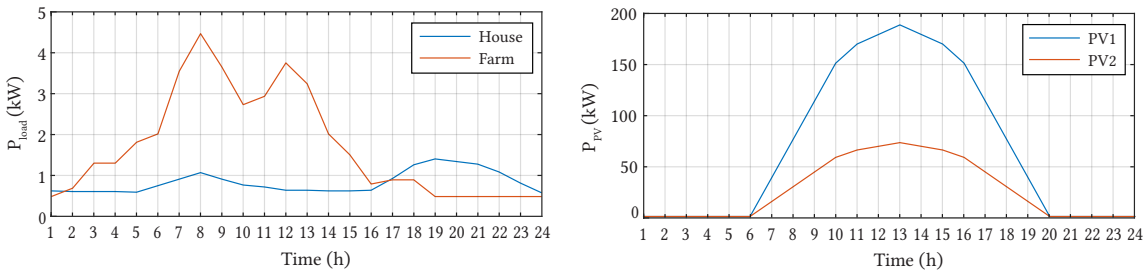
are located where photovoltaic panels are currently installed. The dynamic load profile for the house and farm type was adapted from [180] and is shown in **Fig. 7.16a**. The PV generation follows a simple profile of sun irradiation shown in **Fig. 7.16b**.

Finally, a DC PDN was created with different network architectures as shown in **Fig. 7.17**. The left side shows the schematic of the DC PDN, and the right side the projected distribution lines in the district. The radial, ring, and meshed architecture were projected for comparison purposes, without any optimization. Also, protection schemes and other aspects were not considered in these examples; only the converter placement aspect for power flow is of interest. The information for the line lengths is shown in **Tab. 7.5**, and the cable is considered the same used in previous studies given by **Tab. 6.1**

Tab. 7.4 Number of consumers at each point considered for the power converters ratings, and PV peak power.

Load	Consumers	Load	Consumers	Source	Power (kW)
a1	20 (H)	b1	6 (H)	PV1	192
a2	10 (H)	b2	2 (H), 2 (F)	PV2	72
a3	10 (H), 3 (F)	c	9 (H), 4 (F)		

(H) residential house load type, (F) farm load type



(a) (b)

Fig. 7.16 (a) Load profile for each hour, and (b) PV power generation injected into the grid.

Tab. 7.5 Lines information for the three configurations

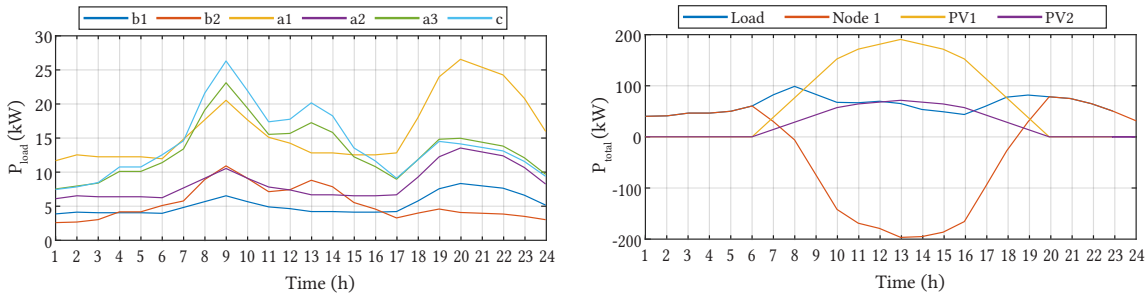
Line	Length (m)	Line	Length (m)	Line	Length (m)	Line	Length (m)
Radial Configuration							
$l_{1,8}$	5000	$l_{6,5}$	77	$l_{11,12}$	91	$l_{8,16}$	331
$l_{8,2}$	270	$l_{6,7}$	97	$l_{12,13}$	57		
$l_{2,3}$	16	$l_{11,9}$	83	$l_{12,14}$	90		
$l_{2,4}$	53	$l_{8,11}$	106	$l_{11,15}$	51		
Ring Configuration							
$l_{1,8}$	5000	$l_{6,5}$	77	$l_{11,16}$	285	$l_{12,17}$	334
$l_{8,9}$	70	$l_{6,7}$	97	$l_{12,13}$	57	$l_{2,17}$	140
$l_{2,3}$	16	$l_{8,11}$	46	$l_{12,14}$	90	$l_{9,17}$	60
$l_{2,4}$	53	$l_{11,15}$	120	$l_{12,16}$	560		
Mesh Configuration							
$l_{1,8}$	5000	$l_{6,5}$	77	$l_{11,12}$	91	$l_{8,16}$	311
$l_{8,2}$	270	$l_{5,7}$	97	$l_{12,13}$	57	$l_{16,14}$	386
$l_{2,3}$	16	$l_{11,9}$	83	$l_{12,14}$	90	$l_{10,6}$	423
$l_{2,4}$	53	$l_{8,11}$	106	$l_{11,15}$	51		

7.5.1 Dynamic power flow

The dynamic power flow was computed to emulate a day-long simulation. In this sense, to include the dynamic load in the MNA, the solution is solved for each instant of time, and later included in a single vector to build the solution. **Fig. 7.18a** shows the total load for each considered node, and **Fig. 7.18b** shows an overview of the dynamic power flow simulation.

During the day, when the PV is generating energy, it can supply all the loads of the system and return some power to the grid as shown in the Node 1 power curve (orange in **Fig. 7.18b**). During the night the energy comes from Node 1 to supply the loads. The total load is the sum of all the loads of the system. From the point of view of Node 1, regardless of the network architecture, the total load and PV generation are always the same, with small deviations due to the losses on the extra lines for the mesh and ring configurations.

Fig. 7.17 Considered DC PDN for the district of Chapello-sur-Moudon. (a) and (b) Radial Configuration; (c) and (d) Ring Configuration; (e) and (f) Mesh Configuration. The three DC PDNs have 16 nodes, except for the ring configuration where an extra node was created between the two PV generations. Satellite photos from Google Earth.



(a) (b)

Fig. 7.18 (a) Total load profile of the specified nodes of the system under analysis, and (b) Results of the dynamic power flow with the total load of the system (blue), total power of the voltage-regulated Node 1 (orange), and PV generation (yellow and purple.)

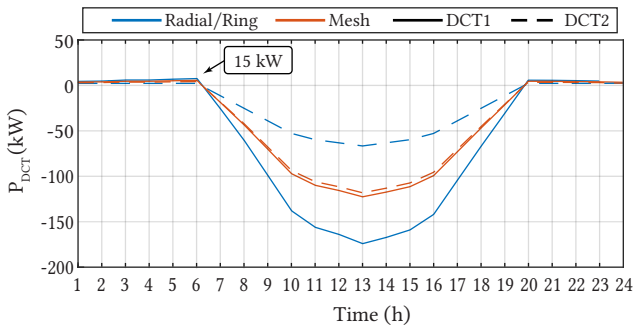


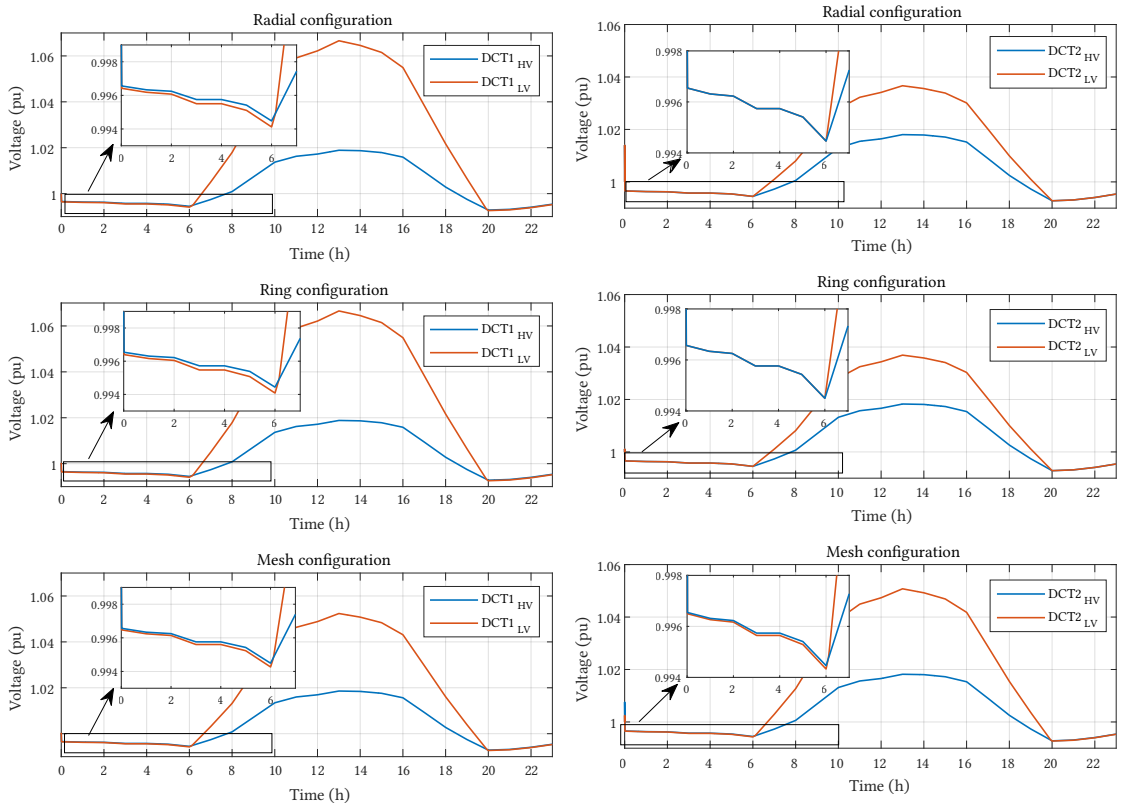
Fig. 7.19 Power flow in the DCT for different network configurations. For the case of the Meshed system, it can be noticed that both DCTs have almost the same load flow characteristics. Radial and Ring are the same as in **Fig. 7.17**.

Fig. 7.19 shows the power flowing through the two DCTs for the three different network architectures. As can be noticed in this plot, the radial and ring configurations have the same behavior once both have the same connections to the PV and grid. That led to a big consumption for the DCT 1 and lower to DCT 2 given by the PV generation. On the other hand, for the mesh configuration, the DCTs almost share the same responsibility due to the extra line connecting both terminals at the lower voltage side.

Furthermore, based on the dynamic power flow calculation, taking into consideration the load profile and PV power plant under study, both DCTs reverse the direction of power flow only twice a day. These moments are when the PV generation is not enough to feed the load, and the energy comes from the main backbone.

Fig. 7.20 shows the voltage at the DC terminals of the DCTs, for the three configurations during the day. As the system is relatively small, the voltage is well-regulated for the whole system. In this figure, one can notice that only for the mesh configuration the DCTs have almost the same voltages due to the extra line connecting the two PV generations, which can be beneficial for the system where the rating of both DCTs can be the same and fully used.

In the end, although the loads of the distribution system can vary considerably, with this power flow analysis, the system does not require several power reversals of the DCT during the day. This behavior



(a) DCT 1 (b) DCT 2

Fig. 7.20 Voltages at the DC terminals of the DCTs. (a) DCT 1 for the three configurations and (b) DCT 2. Only two power reversals during the day for both DCTs.

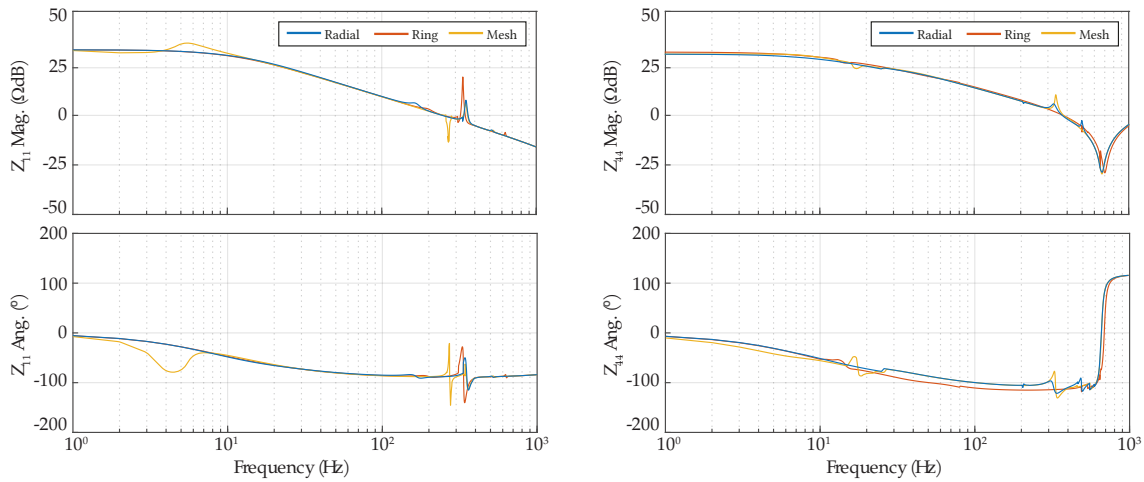
is expected in most of the configurations for distribution systems where the power generation is still very centralized, and renewable energy generation is always considered as a support to the system. Nevertheless, other systems might have different load profiles and require more power reversals. Thus, each case must be investigated individually.

7.5.2 Nodal Impedance Characteristics

In order to evaluate the impact of the network architecture on the nodal impedance, the same system was computed, and two nodes were evaluated as an example. **Fig. 7.21** shows the nodal impedance response for Node 1 - voltage-controlled node, and Node 4 - DCT 1 higher voltage side.

For all three different network configurations, the response was practically the same. The resonances occur around 200 Hz, and for the DCT another resonance appears around 700 Hz. The system has a capacitive behavior for most of the range of frequency under analysis. In low frequencies (0 to 10 Hz) the behavior is almost flat and the impact of the short lines, is practically not visible. Nevertheless, the mesh configuration showed extra resonances. At Node 1, a resonance in low frequency $\approx$ 8 Hz appears with less damping than in the other configurations. Similar behavior happens with Node 4, with the oscillation around 20 Hz.

In this sense, for this case study, the impact of different network architectures did not show a strong effect on the nodal impedance. This highlights the impact of the transmission line on this characteristic. The case exemplified here features short line lengths and at a distribution level can be considered small. Thus, for systems with similar characteristics, no problem should arise from the modal resonance point of view.



(a) Node 1 - Source AC-DC converter

(b) Node 4 - DCT 1 HV-port

Fig. 7.21 (a) Nodal impedance response of Node 1 and (b) Nodal impedance response of Node 4, for the three network architectures under analysis.

7.6 Summary and Conclusion

This chapter evaluated the MNA and RMA methodology to investigate the DC PDN with DCT in a few case studies. Firstly, the impact of the DCT on the power flow characteristics and nodal impedance was investigated. Later, the use of the nodal impedance information to evaluate the system's dynamics, and the stability provision of the system for adding an extra converter to the grid was presented. Ultimately, an evaluation of different architectures of DC PDN with dynamic power flow was demonstrated.

It was shown that the aspects of operation and stability assessment, and planning of DC PDN are possible with this approach. Further due to the nodal approach, the system can include a high number of nodes and power converters. And, as already highlighted in the previous chapter, the representation of the power converter can be extended to black box modeling which improves its representation. From the results obtained in this chapter, the DCT does not have any negative effects on the grid, considering the range of frequency under analysis. Yet, as noted by the RMA, the predominant resonances of the DC PDN come from the transmission line, and this aspect needs to be carefully modeled for a proper evaluation.

Finally, with the increased use of DC technologies, tools and methodologies to investigate DC systems and the power converter's impact on the grid are ever important. This chapter showed that all the tools used in AC systems can be used for DC systems with some adaptations.

8

RT-HIL Platform for DC Power Distribution Networks

In this chapter, a real-time hardware-in-the-loop platform for studying complex DC power distribution networks was developed. This platform allows system-level simulations using real controllers, resulting in a flexible environment to carry out long simulations with many converters. Consequently, the resonance nodal analysis is evaluated for larger systems and compared with the real-time simulation. Additionally, an operational analysis of a highly meshed MVDC power distribution network is performed. This includes assessing how system control affects impedance characteristics, as well as the influence of the grid impedance on the DC nodal impedance.

8.1 RT-HIL PDN Platform

Hardware-in-the-loop (HIL) simulations are increasingly used as a tool to simulate complex systems and test complex control algorithms. In this context, the two predominant variants are the Control Hardware-in-the-Loop (CHIL) which focuses on the real-time interaction between a physical controller and an emulated system [181]–[183], and the Power Hardware-in-the-Loop (PHIL), which extends this concept to include actual power components [184]–[186].

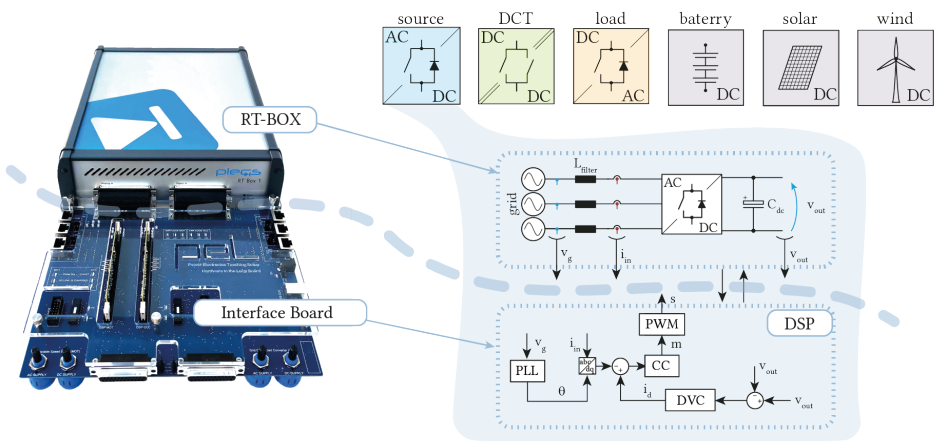


Fig. 8.1 Example of an RT Box with an interface board with Digital Signal Processors (DSPs); and the representation of several elements with the hardware part simulated in RT Box and control embedded in DSP.

In a CHIL system, the real controller generates PWM signals which are sensed, and sampled by the real-time HIL (RT-HIL) simulator, and the system state variables are updated and relevant signals are

fed back to the controller as analog signals. **Fig. 8.1** shows the real-time simulator (RT Box [187]) with the developed interface board with two DSPs (TI TMS320F28335). The RT Box simulates the hardware component and produces the necessary signals for control, while the interface board enables the transfer of signals between the RT Box and the DSP in both directions.

In this simulation, one usual limitation is the discretization time to simulate all the elements of the system. This limits the hardware representation, which impacts the speed at which signals can be exchanged between the simulator and controller. For instance, PWM signals for power converters are in the range of tens to hundreds of kilo Hertz, thus, the simulation needs to be fast enough to capture all the signals and generate a different simulation state before the next switching state.

For that reason, the power converters are usually modeled to maintain realistic responses from the controller's point of view, and this limits the valid range of analysis. Fortunately, the system-level studies performed in this thesis are not affected by this limitation since the considered converters have a maximum switching frequency of $f_s = 10$ kHz, and the frequency range of interest is even lower. Nevertheless, the transient response is limited, as well as the representation of fast and non-linear behavior of the models.

Another limitation arises when considering the maximum analog input/analog output (AI/AO) and digital input/digital output (DI/DO) ports. This limitation leads to the partitioning scheme of the converters to create the DC PDN. **Fig. 8.2** shows the considered partitioning of the system, using the two DSPs and the available AO/AI signals.

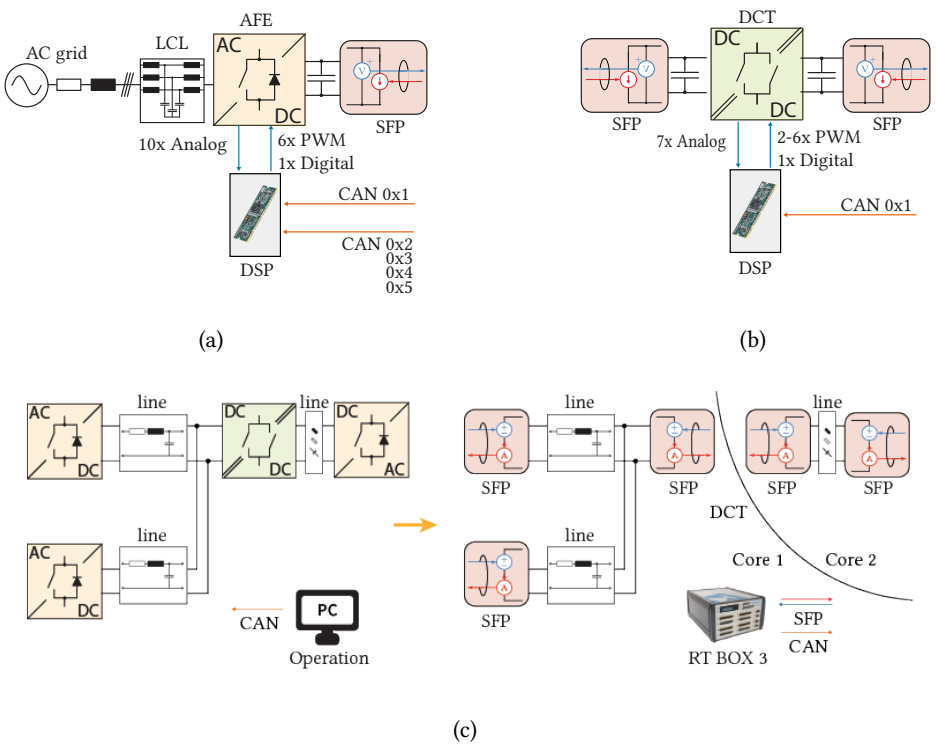


Fig. 8.2 Details on the connections using the required DO/DI, AO/AI, and the SFP-link for (a) AFE converter and (b) DCT. (a) and (b) are the converters inside RT Box 1. (c) Example of SFP-link connections to create a DC PDN in RT Box 3. A split of the system happens with the DCT.

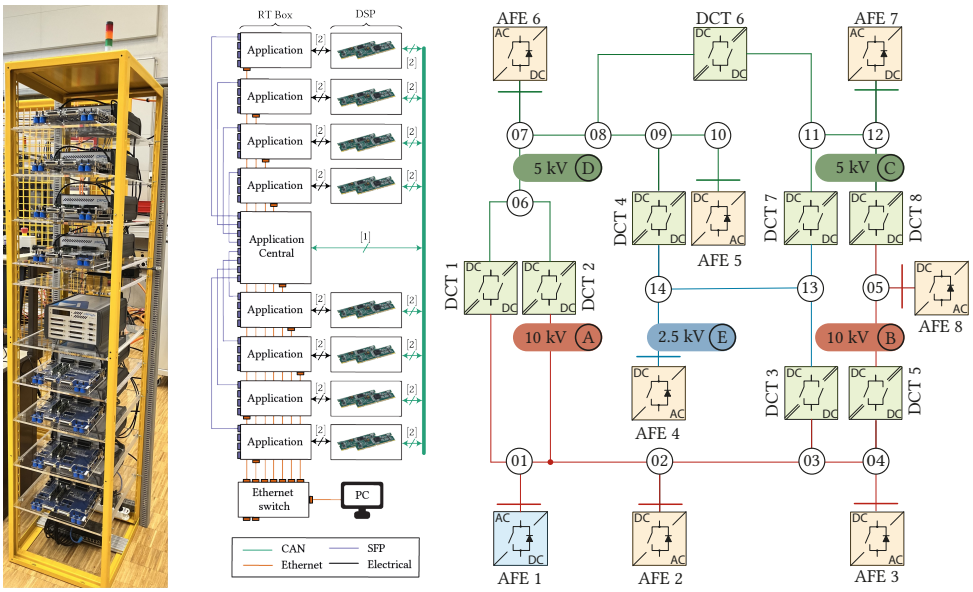


Fig. 8.3 (a) RT-HIL platform used for DC PDN studies. (b) RT-HIL structure showing the connection between RT Boxes. The central application manages the system and routes the DC PDN. RT Box 3 runs at 4 μs while RT Box 1 runs at 8 μs. (c) Highly meshed MVDC PDN used for system analysis in this chapter.

Each RT Box 1 simulates two converters, one acting as an AC-DC converter (AFE) (**Fig. 8.2a**) and another as a DC-DC converter (DCT) (**Fig. 8.2b**). This division is used for simple upscaling of the system. Nevertheless, these elements can have different tasks and even change responsibilities depending on the specific application.

To create a big system out of several RT Boxes, the Small Form-factor Pluggable (SFP) communication channel is used. With this link, any simulated data can be exchanged between RT boxes, at a rate of 6.25 Gb/s. RT Boxes 1 have four SFP-link ports, while RT Box 3 has eight ports. Consequently, the system can be split into diverse ways, and a more complex system or converter can be simulated using several RT Boxes. In the schematics shown in **Fig. 8.2**, each DC port of every converter is connected to an SFP link in the form of a controlled current source and voltage measurement.

In total eight RT Boxes 1 are used to create the DC PDN. To manage all the data from the RT Boxes 1, an RT Box 3 is used as a central application. This central application receives all the signals to create the DC PDN. Inside RT Box 3 the system is created routing the SFP-link data from RT Box 1 and providing the required feedback signal for the operation. An example is shown in **Fig. 8.2c**. In addition, the RT Box 3 simulates the transmission lines between the nodes. Also, inside the RT Box 3 the system is split into the three available cores, aiming to optimize the CPU usage.

The RT Box 3 also serves as a GUI interface for operating the system. It manages the CAN communication signals to perform the tasks of i) Enabling/Disabling the converter; ii) Selecting the AFE mode (Current controlled, or Voltage controlled); iii) External trigger; iv) V_{dc} reference; v) i_d reference; and iv) i_q reference. Using this communication system, the converters can be left to operate with a unique set point, and a natural power flow is established, or a central control loop can be implemented to test diverse scenarios.

The complete DC PDN HIL platform is shown in **Fig. 8.3a**, and the connections of the RT Boxes are shown in **Fig. 8.3b**. This scheme was used to reduce the cabling and simplify the connections between them using only the central RT Box 3 interface. The DSPs are connected to a CAN bus via the interface board.

Finally, the highly meshed MVDC PDN of **Fig. 8.3c** is created. This configuration uses all the available resources to create a system with several DCTs and several sources and loads. This system has three DC bus voltage levels, voltage-controlled and power-controlled sources, DCTs, transmission lines, and loads. Thus, this system is used for the investigations in this chapter.

8.2 RT-HIL Elements

Every element of the system was modeled in simulation and validated using the real-time simulator. The converters were designed with the same schematic and control structure outlined in **Chap. 6**. This section provides a detailed description of both the AFE and DCT in RT-HIL.

8.2.1 Active Front End

The AFE consists of a three-phase grid-connected inverter with PLL, DC voltage, and current control loops. All the control loops are coded in the DSP, which sends the PWM signals to RT Box. The model receives the PWM signals and digital inputs to simulate the complete converter and control the desired variables. The complete schematic is shown in **Fig. 8.4a**, and the HIL model in **Fig. 8.4b**.

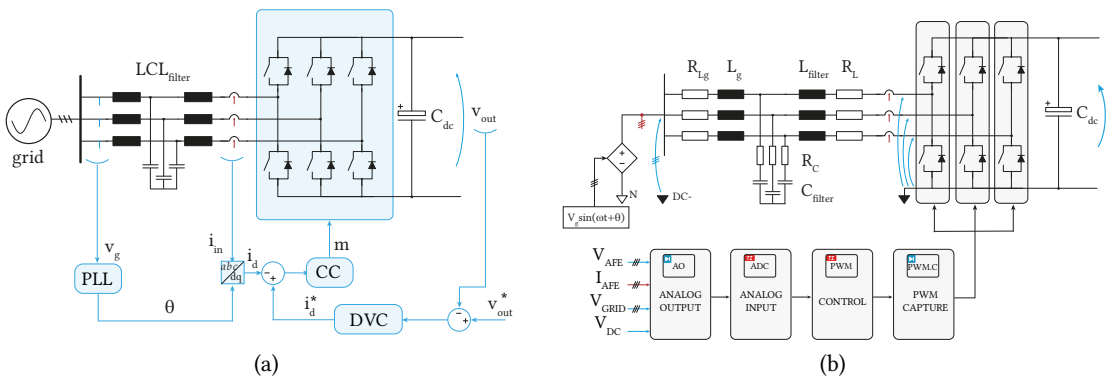


Fig. 8.4 (a) Considered AFE with control loops and measurements, and (b) block diagram of the converter representation on HIL with the required signals output for control.

Inside RT Box, each leg of the three-phase inverter is modeled with a half-bridge sub-cycle averaged block. This block receives the PWM signal from the PWM Capture function and modulates the resultant current/voltage of each half-bridge block. Using this approach, the power converter loses its ability to simulate the non-linearities of each power switch, limiting the analysis in terms of power converter losses, and the frequency analysis is limited by the discretization time of the simulator.

Nevertheless, this model can reproduce well the dynamic behavior of control loops, and validate the control algorithm with real ADC delays. The RT Box sends to DSP three signals of voltage at the voltage source terminals, three currents and three voltages at the converter terminals, and the DC-link voltage.

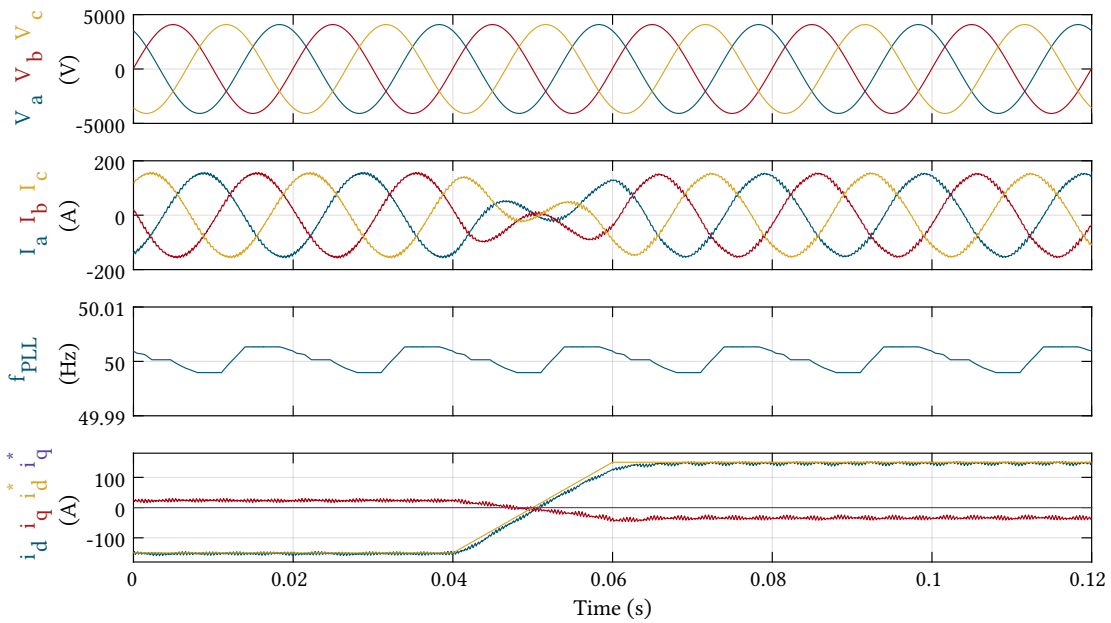


Fig. 8.5 RT simulation results of the MV AFE. A power reversal in a current control loop. Firstly, the AFE is consuming power with $i_d^* = -150$ A, and after $t = 0.04$ s the reference changes to $i_d^* = 150$ A with a slope of $\Delta i/\Delta t = 0.015$ A/μs. Consequently, the AFE starts injecting synchronized current into the AC grid.

The AFEs are designed following well-known and consolidated practices in literature. The DC-link capacitance is calculated according to the required energy storage for half a grid period:

$$E = \frac{1}{2} C_{DC} {V_{DC}}^2 \rightarrow C_{DC} = 2 \frac{P_{\max}}{{V_{DC}}^2} \frac{1}{2} \frac{1}{f_g} \tag{8.1}$$

The LCL filter is designed using (8.2). The maximum peak-to-peak current ripple was selected to be 10% of the rated current $\Delta I_{L,max} = 0.1 I_{max}$. The capacitor is selected to be 5% of the capacitance base of the system, and the inductor on the grid side is designed to have a 20% attenuation factor on the harmonics resulting with $k_a = 0.2$ [188].

$$L_1 = \frac{V_{\mathrm{DC}}}{6 f_s \Delta I_{\mathrm{Lmax}}} \qquad C_f = 0.05 \frac{P_n}{\omega_g {V_{AC}}^2} \qquad L_2 = \frac{\sqrt{\frac{1}{k_a^2}} + 1}{C_f \omega_s^2} \tag{8.2}$$

The controller gains for the current control are calculated according to the magnitude optimum criteria [163], with maximum/minimal output for the reference voltage of $\pm 0.95 V_{dc}/2$. To avoid saturation at the output limits, back-calculation with the coefficient $k_{bc} = k_p/k_i$ is used as an anti-windup. The DC-voltage control loop is tuned with the symmetric optimum. The equations for the tuning are described in (8.3).

$$CC = \begin{cases} k_p = 2\pi L f_{CC}/f_g \\ k_i = 2\pi k_p f_{CC}/4 \end{cases} \qquad VC = \begin{cases} k_p = 2\pi V_{dc} C_{dc} f_{VC} \\ k_i = 2\pi k_p f_{VC}/4 \end{cases} \qquad PLL = \begin{cases} k_p = 2\pi f_{PLL} \\ k_i = 2\pi k_p f_{PLL}/4 \end{cases} \tag{8.3}$$

These equations were implemented in Matlab and each converter is automatically created from a set of initial parameters such as rated power, rated DC and AC voltage, grid frequency, and switching frequency.

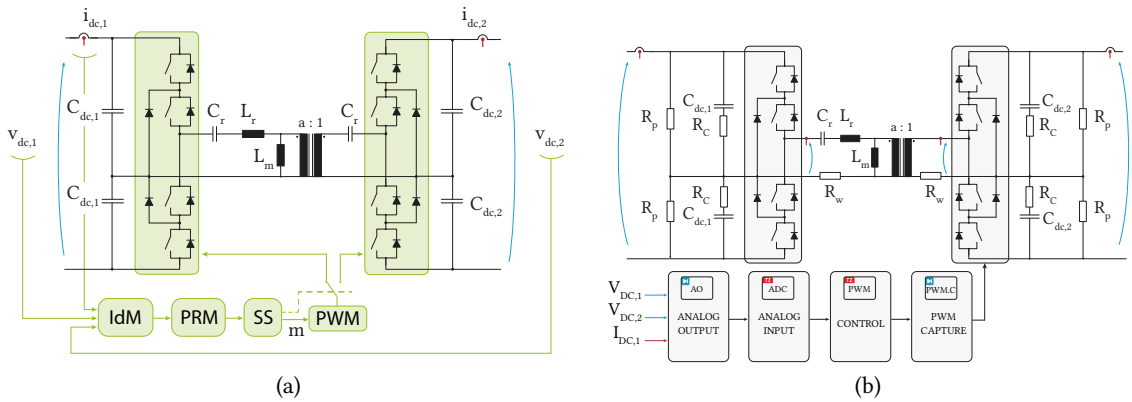


Fig. 8.6 (a) Considered MV DCT with open loop strategies for the complete autonomous operation of the DCT. (b) Block diagram of the converter representation on HIL with the required signals output for control.

Finally, to demonstrate the functionality of this convert in RT Box, an AFE converter was created and tested. **Fig. 8.5** shows the results of the real-time simulation. It shows the MV AFE for a reverse of current reference, from consuming to injecting current to the AC grid. More details of the power converter parameters are shown in the system parameters section.

8.2.2 Direct Current Transformer

The DCT is built with NPC power stages and it has a soft-start, idle mode, and power reversal method for the complete operation of the DCT, as described in **Chap. 3**. **Fig. 8.6a** shows the DCT schematic and **Fig. 8.6b** shows its representation in HIL. Similarly to AFE, the power stages are simulated as sub-cycle average equivalent circuits.

The simulation of the LLC converter in HIL is challenging due to the discontinuous period with only magnetizing current flowing in the resonant tank. However, due to the relatively low switching frequency, the DCT requires no further simplifications.

Nevertheless, some challenges appear for the soft-start and the idle mode functions. For instance, the PWM Capture is not capable of providing the required resolution for the proper switching pulses to create a 3L waveform. This is a limitation on the speed of the PWM Capture, which generated an average signal compatible with the sub-cycle module but is incapable of generating fast pulses for the 3L waveform. Consequently, the transient performance is degraded, and the soft-start starts at 20% duty cycle.

Thus, all the essential features were implemented in a state machine in the DSP, and the DC terminal's behavior could be faithfully replicated. **Fig. 8.7** shows an experiment demonstrating the power reversal, soft-start, and idle mode. In this simulation, a power reversal is performed by manipulating the secondary DC voltage to reverse the power. At the time $t = 0.05$ s, the source starts to increase its value in a ramp with a rate of change equal to $\Delta v/\Delta t = 0.015$ V/μs. At time $t = 0.1$ s, both DC voltages are close to each other, and only magnetizing current is flowing as can be seen in yellow on the third plot. After some time, the DCT turns OFF completely. Finally, after $t = 0.28$ s, the DCT noted the voltage difference and turned ON again, knowing that some power would be transferred. Then it leaves the idle mode, reversing the power in a slow turn-on as the voltage difference rate of change was slow.

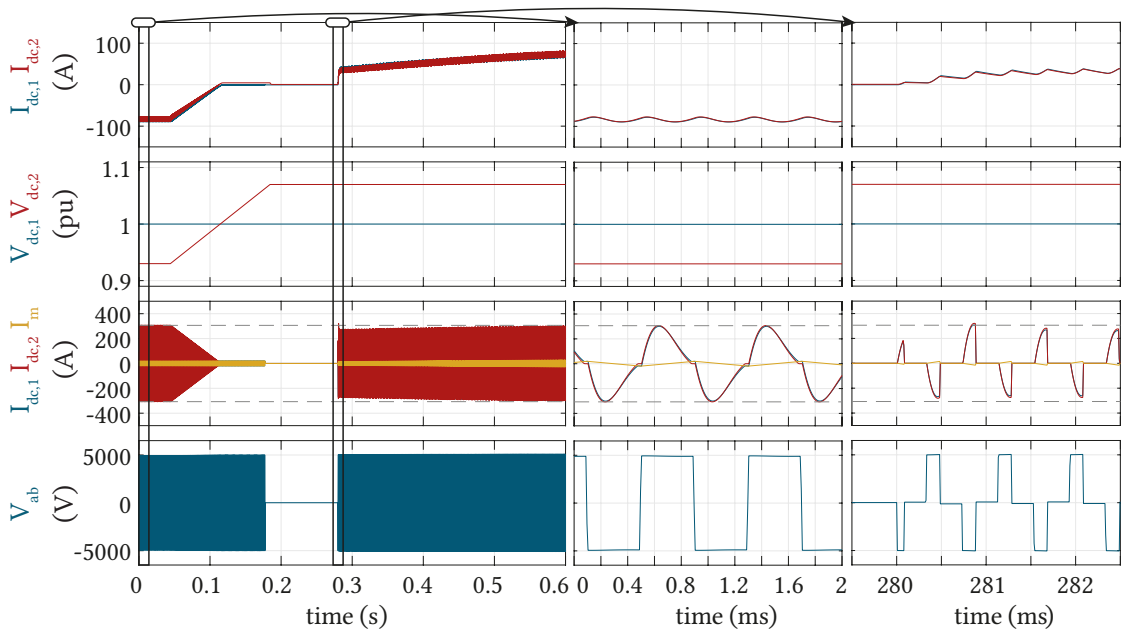


Fig. 8.7 RT simulation results of the MV DCT with idle mode, power reversal, and soft start. Standalone test with two voltage sources to validate the power reversal. At first, the DCT operates in the forward direction as shown in the first zoom-in. When the processed power is below P_{th} = 10 kW the DCT turns OFF as only no-load losses are present. After a while, the voltage difference is above ΔV = 500 V, and the rate of change is slow $\Delta V' = 1/\Delta V_{ROC}|_{1\text{ms}}$ resulting in a slow soft start as shown in the second zoom-in. After the transient, the DCT operates in the backward direction.

8.2.3 System Parameters

The complete system was built with eight RT Boxes 1 and one RT Box 3, shown in **Fig. 8.3c**. This system consists of a 14-node MVDC PDN in a mesh configuration. This system has eight AFEs and eight DCTs, a total of 70 km of transmission line, and it was thoroughly designed to have DCTs in parallel, diverse inner rings, and regions with strong and weak source support.

All the converters were created following the description in the previous section. The following tables detail the data of the steady-state operation of the system. **Tab. 8.1** shows the AFEs parameters. **Tab. 8.2** shows the DCTs parameters. **Tab. 8.3** brings information about the transmission lines, and **Tab. 8.4** details the PLL, current, and voltage control loop gains.

Tab. 8.1 AFE data

AFE	1	2	3	4	5	6	7	8
Rated Power (MW)	10	1	3	1	0.5	0.5	1	2
Rated DC-Voltage (kV)	10	10	10	2.5	5	5	5	10
Rated AC-Voltage (kV)	5	5	5	1.25	2.5	2.5	2.5	5
X/R (-) : Z (%)	5:5	5:5	5:5	5:5	5:5	5:5	5:5	5:5
Switching frequency (kHz)	2	2.5	2	2.5	2.5	2.5	2	2
DC-link capacitance (mF)	2	0.2	0.6	3.2	0.8	0.8	0.8	0.5
LCL resonant frequency (Hz)	600	650	-	-	0-	0.8	0.8	0.5
Configuration	VC	S	L	L	L	L	S	L

VC = voltage controlled; S = constant power source; L = constant power load

Tab. 8.2 Parameters of the DC-Transformers

DCT	1	2	3	4	5	6	7	8
Rated Power (MW)	1	1	5	2	10	1	2	2
Rated DC-Voltage (kV)	10:10	10:10	10:2.5	5:2.5	10:10	5:5	5:2.5	5:10
Switching frequency (kHz)	2	2	2.5	2.5	2.5	2.5	2	2
Magnetizing inductance (mH)	7.8	7.8	0.3	3.1	2.5	6.3	3.9	3.9
Leakage inductance (μH)	58	58	7.4	1.6	4.3	1.2	1.6	3.1
Resonant Capacitor (μF)	88	88	441	220	800	298	360	186
Frequency ratio (-)	1.1	1.1	1.1	1.05	1.08	1.05	1.05	1.05
Quality factor (-)	0.01	0.01	0.008	0.011	0.009	0.01	0.0082	0.01
DC-link 1 capacitance (mF)	0.8	0.8	16	0.16	2	0.8	0.16	0.16
DC-link 2 capacitance (mF)	0.2	0.2	1	0.64	2	0.8	0.64	0.4

Tab. 8.3 Length of transmission lines for the DC PDN.

Line	Length	Line	Length	Line	Length	Line	Length
$l_{1,2}$	20 km	$l_{5,12}$	10 km	$l_{7,8}$	5 km	$l_{11,12}$	10 km
$l_{3,4}$	5 km	$l_{6,7}$	5 km	$l_{8,11}$	10 km	$l_{11,13}$	5 km

Cable data: $r = 17.6m\Omega$/km, $l = 268\mu H$/km, and $c = 904\mu F$/km [158]

Tab. 8.4 Details of the closed-loop control gain

AFE	1	2	3	4	5	6	7	8
PLL gains								
k_p	1	1	1	1	1	1	1	1
k_i	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05
Current control gains								
k_p	11.1	7.5	20.8	112.3	11.1	24.9	27.8	9.4
k_i	20.8	28.1	20.8	28.1	11.11	18.7	8.3	22.5
Voltage control gains								
k_p	0.6	-	-	-	-	-	-	-
k_i	40	-	-	-	-	-	-	-

8.3 Operation of the MVDC PDN

The MVDC PDN operation is initially tested under steady-state conditions using the specified data. The system is replicated in **Fig. 8.8a** for practicality. All the DSPs have been pre-loaded with the standard control structure, allowing all the necessary modifications via CAN. The code is generated with the code generation function of PLECS and flashed to the DSP. A Python code is employed to automate the initialization of RT Boxes 1 and subsequently RT Box 3, which serves as the synchronization clock for the entire system.

The system can be initiated gradually, activating one converter at a time, or simultaneously with a single main command signal. While strong transients may occur during startup, it is noted that the focus is not on the startup phase. Once the system is operational, it reaches a natural steady-state condition. **Fig. 8.8b** shows the voltage profile of the system. It can be noted that the lowest voltage is at node ⑤, which happens to be far away from the voltage source, and with a heavy load.

To evaluate the system's dynamic response, two tests were performed: i) load changes; and ii) DCT power reversal. **Fig. 8.9** shows the load step of AFE 4 at the 2.5 kV bus (Bus E). **Fig. 8.9a** shows the DC PDN with a highlight on the converters connected to this bus, and **Fig. 8.9b** shows the real-time simulation results.

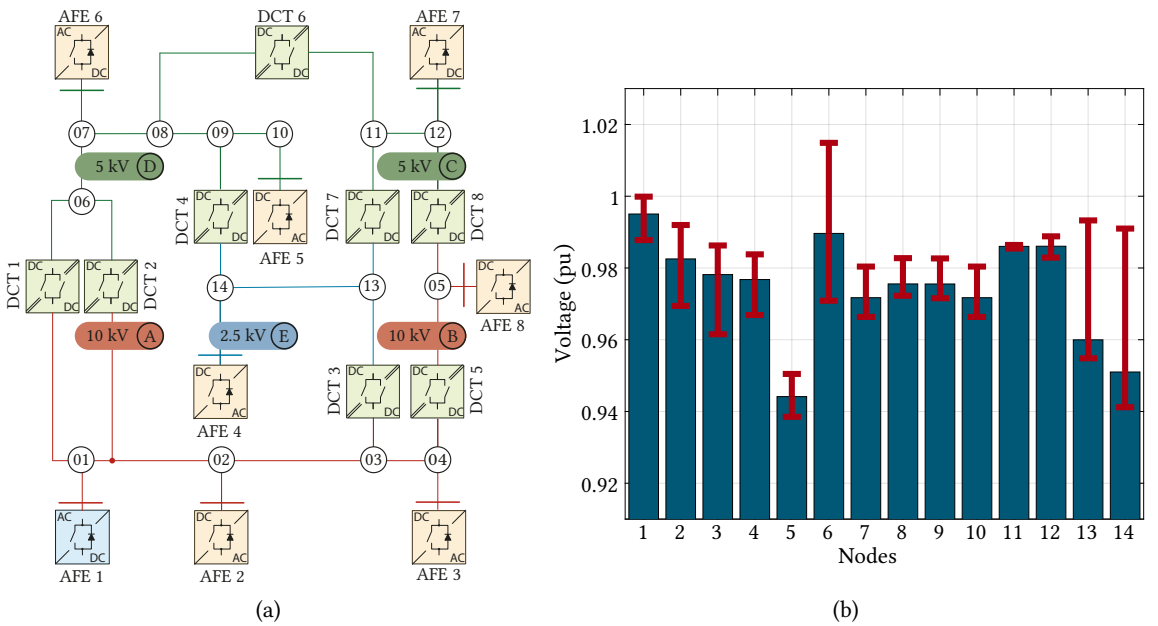


Fig. 8.8 (a) Highly meshed MVDC PDN simulated in RT-HIL. Replicated here for practicality. (b) Voltage profile of the nodes of the system. The error red bars represent the oscillation over 500 ms.

In this experiment it is possible to see that by halving the load of AFE 4, small disturbances were caused to the system, and there was no change in the natural power flow of the system. This means, no DCT has to be turned ON or OFF, no power reversal, and almost no transient disturbances.

On the other hand, a different test inverting the power of AFE 6 was performed to verify the power reversal of the DCTs. In this case, AFE 6 previously acting as a CPL becomes a power source as a generator to the DC grid.

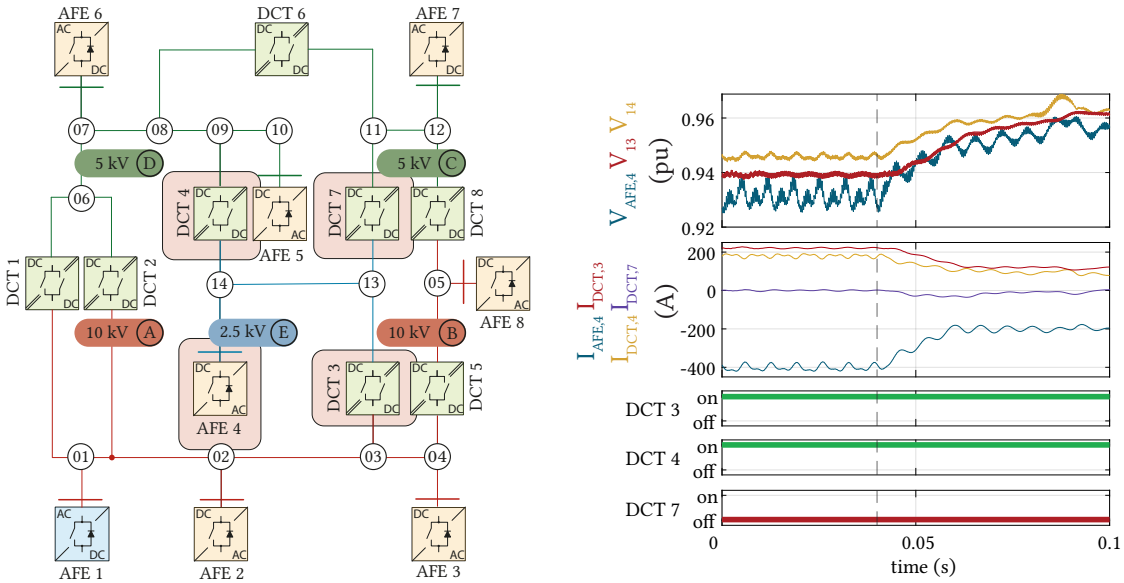


Fig. 8.9 (a) Highly meshed MVDC PDN simulated in RT-HIL, with highlights on the converters under investigation. (b) Real-time simulation results for the load step change on AFE 4. At $t = 0.04$ s, the load of AFE 4 is halved with a slew rate of $\Delta I/\Delta t = 0.015$ A/s. At steady state, only DCT 4 and DCT 7 are switching. With this test, the system remained operational with no problem, with minor transient, and the surrounding DCTs were not affected.

Fig. 8.10a shows the DC PDN with the highlighted converters under analysis, and **Fig. 8.10b** shows the real-time simulation results. In this experiment, a change in the current reference of AFE 6 occurs at $t = 0.045$ s, shifting from $i_d = -100A$ to $i_d = 100A$ with a slew rate of $\Delta I/\Delta t = 0.015A/\mu$s. Initially, both DCTs operate in parallel, each transferring half of the power. As the current changes to its new reference, bus voltages begin to rise. Eventually, the voltage difference between the two DCT terminals falls below a threshold, leading to the DCT 1 and 2 turning OFF. The noise around $t = 0.07s$ may be attributed to simulation inaccuracies. Subsequently, as the load continues injecting power into the DC bus, raising the voltage, the DCT switches ON again by detecting a voltage difference between its terminals at $t = 0.13$ s. During this transient, the voltages at the DCT terminals experience an overshoot up to $V_{DCT} = 1.1$ p.u., and the current reaches its limit at $I_{DCT} = 100$ A, before meeting the new sharing condition.

This experiment demonstrated the operability of the DCT features in real-time simulation and showed the importance of properly tuning open-loop strategies considering DCT characteristics and the system's dynamics. The conservative threshold values set for the DCT delayed the DCT operation after the reversal, leading to overvoltage. To reduce such transients, using more tightly defined reference values could be beneficial.

Finally, **Fig. 8.11** shows a extensive operational test of the DC PDN. In this figure, the DC voltage and DC current of all the AFEs are shown, along with the status and power direction. Initially, the system is in a steady-state, and a series of tests are conducted to assess the system's performance with multiple DCTs operating without centralized control.

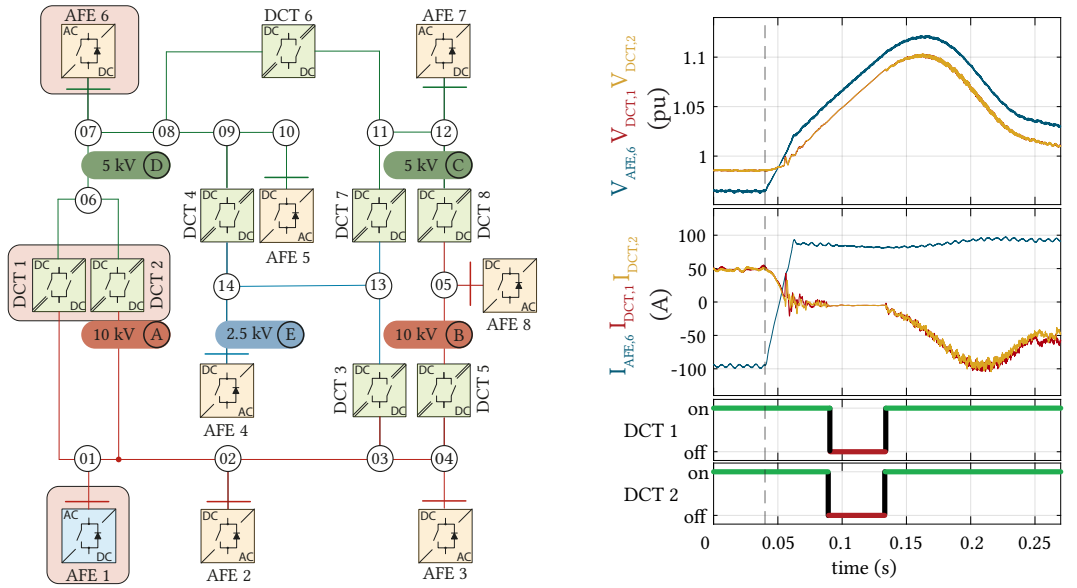


Fig. 8.10 (a) Highly meshed MVDC PDN simulated in RT-HIL, with highlights on the converters under investigation. (b) Real-time simulation results for the complete power reversal of AFE 6. At $t = 0.045$ s, the load of AFE 6 is reversed from $i_d = -100$ A to $i_d = 100$ A with a slew rate of $\Delta I/\Delta t = 0.015$ A/s. At the steady state, both DCT 1 and DCT 2 are operating in parallel. At the moment the load is reduced, the DCTs turn ON, and after a moment turn OFF to transmit the power generation to the voltage-controlled bus.

The first load test happens at time $t = 2$ s, replicating the experiment shown in **Fig. 8.9**. In this test, marked as ⓐ, the power of AFE 4 is reduced by half with a slew rate of 0.015 A/s. This results in minor transients without significant changes to the overall system. Arrows in the figure help to identify the moments of change. The next test involves completely turning off AFE 3, labeled as ⓑ. This leads to a decrease in power supplied by AFE 1, but no other changes in the system are observed.

Test ⓒ features a complete reversal of power from AFE 5, switching from a constant power load to a constant power source. This significant change disrupts the system, reversing the direction of DCT 1 and making other DCTs to adjust their the power direction. This event led to an overvoltage in some buses, reaching almost 1.3 p.u. During this transient, AFE 1 tried to control the voltage of the system, but until new power flow have completely established, some DCTs turned ON and OFF several times.

After reaching steady-state again, the AFE 7 changes from constant power source converter to voltage controlled converter. This scenario is marked as ⓓ. It can be seen that the converter starts controlling the voltage properly, and instead of providing current to the DC grid is now delivering current to the AC grid.

The final test, marked as ⓔ, involves deactivating DCT 6. This leads to a power reversal and network reconfiguration, with DCTs 4, 7, and 8 altering their status to provide a current path between Bus D and Bus C, while DCT 1 is turned off. After completing these experiments, the DC PDN eventually stabilizes into a steady-state, demonstrating the system's effective operation.

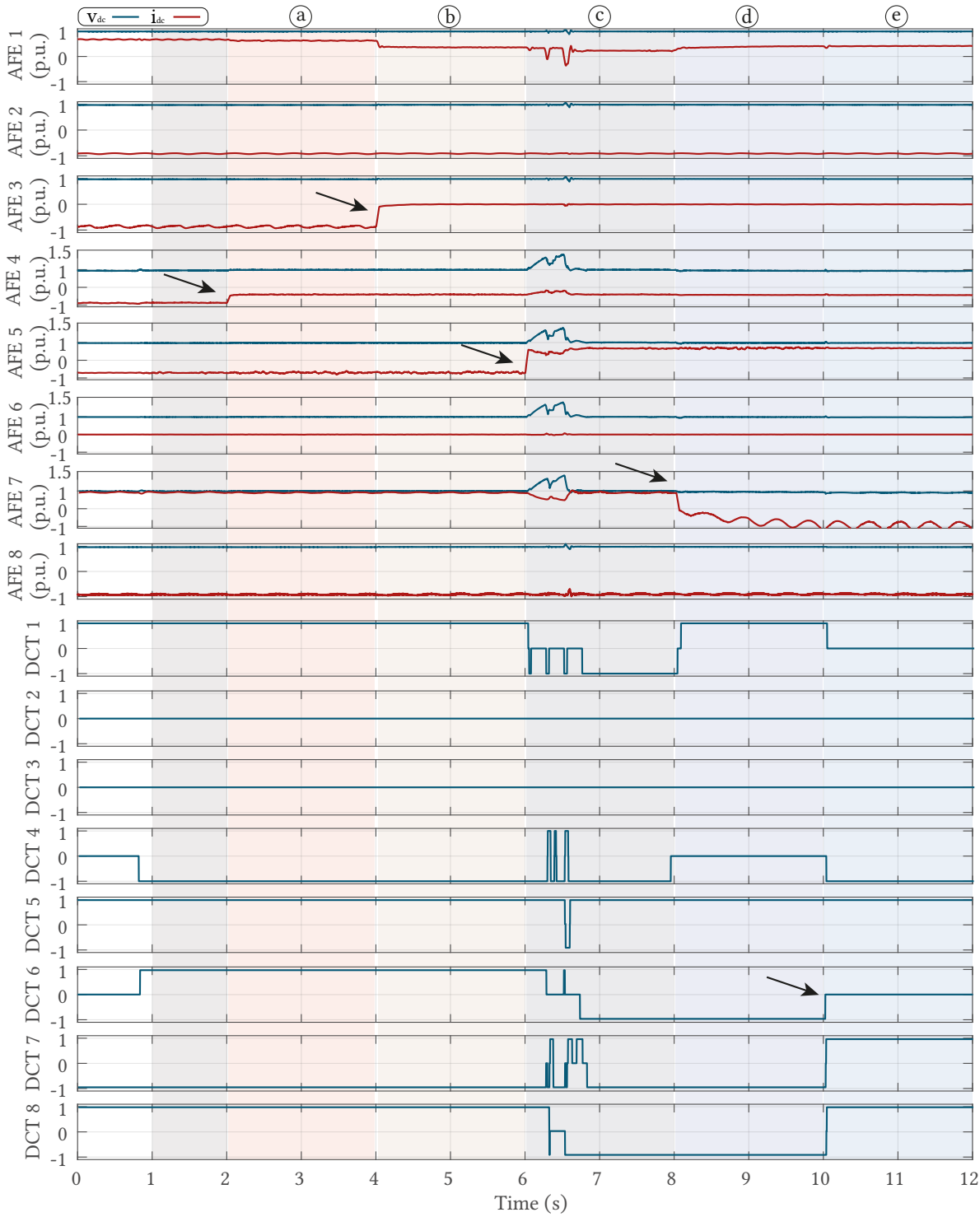


Fig. 8.11 Real-time simulation results for the DC voltage and current of all AFEs of the system and DCTs' status with the operation test. Marked with ⓐ a halved step change with a slew rate of $\Delta I/\Delta t = 0.015$ A/s on AFE 4. Marked in ⓑ, the AFE 3 is shut down. Marked in ⓒ the load of AFE 5 is reversed. Marked in ⓓ DCT 6 turns OFF. The power direction of the DCT is from higher DC voltage to lower DC voltage, besides DCT 6 which is left to right, and DCT 5 which is bottom to top.

8.4 HIL Characterization of the Nodal Impedance in DC PDN

With the real-time simulation of the multi-converter system now available, the methodology established in the previous chapter can be applied to validate and extend the outputs. The evaluation of system impedance plays a crucial role in pointing out the critical resonant frequencies of the system. Through this assessment, valuable insights can be derived, including understanding the control loop's impact on the resonances of the system and investigating the effect of AC impedance on DC nodal impedance.

The impedance measurement in RT Box is performed in the same way as performed in **Chap. 6**. For that, an ideal current source with the perturbation signal was simulated in the RT Box 1, at the converter's DC-port. The signal was generated by a 12-bit-length shift register resulting in a 4095-bit-long PRBS. The sequence was generated with a 5 kHz generation frequency, which sets the injection time to $t_{PRBS} = 0.819$ s. With this resolution, the frequency range of interest (up to 1 kHz) can be faithfully analyzed. Therefore, after recording the current and voltage of interest, performing the DFT, and plotting it in the Bode diagram, one can determine the impedance characteristic in the frequency domain. The scheme for injecting the perturbation at the AFE output and its equivalent small signal representation are shown in **Fig. 8.12a**.

To validate the impedance extraction, an AFE was first tested and compared with the small signal transfer function [161]. **Fig. 8.12b** shows real-time simulation results of the DC impedance of the AFE using the impedance measurement. It can be seen that the impedance is faithfully extracted, as is expected for the standalone simulation. The two exceptions are the effect of the DSRF-PLL around the grid frequency [189], and the very low frequencies around $f \leq 4$ Hz, due to extra resistances present in simulation. In summary, despite these two exceptions, the overall validation of impedance extraction for the AFE through real-time simulation aligns well with the anticipated outcomes of the standalone simulation.

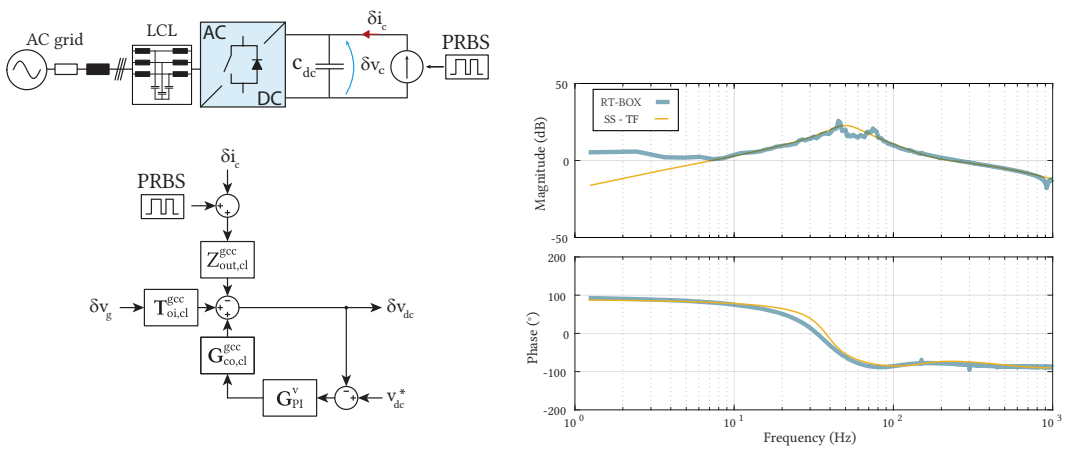


Fig. 8.12 (a) Illustration on the perturbation injection for AFE and block diagram of the small signal (SS - transfer function) modeling; where $Z^{gcc}_{out,cl}$ is the closed-loop output impedance of the grid-connected converter (GCC), G^{v}_{PI} is voltage compensator transfer function, $G^{gcc}_{co,cl}$ is current compensator transfer function, and the $T^{gcc}_{oi,cl}$ is an input-to-output transfer function. (b) The output impedance of AFE from the impedance measurement on the real-time simulation and from the small signal modeling.

8.4.1 Impact of Control on the Resonance Analysis

With the complete system operating in a steady state, the nodal impedance is verified and compared with the analytical model. The system was modeled with the methodology of **Chap. 7** and the nodal impedance is compared to the impedance extracted from the real-time simulation. The goal is to verify the RNA for a highly meshed system with a large number of DCTs.

Two converters are chosen to perform the analysis, assessing the impact of the outer control loop on the nodal impedance: AFE 1 and AFE 6, which are voltage-controlled and current-controlled converters, respectively. Thus, **Fig. 8.13** shows the comparison of the impedance extraction in the real-time simulation and the RNA, for AFE 1 and AFE 6 for different control gains.

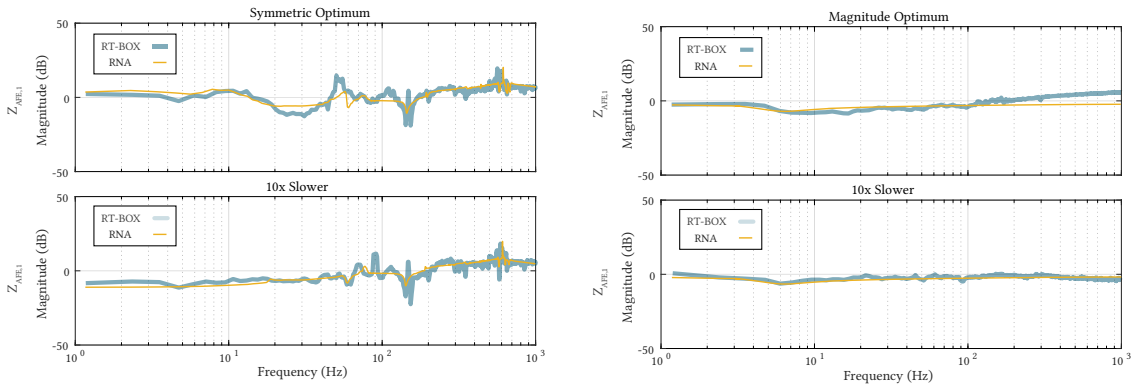


Fig. 8.13 Impact of the control dynamics on the nodal impedance with a comparison between the Nodal impedance extracted from RT Box and analytical model. (a) AFE 1 - Node 1, a voltage-controlled node with symmetric optimum tuning and with a factor of 10x slower compared to the optimum tuning. (b) AFE 6 - Node 7, a current-controlled node with magnitude optimum tuning and with a factor of 10x slower. Note that the impact of the CC tuning does not affect the RNA response once the CPL model does not include the tuning parameters.

Fig. 8.13a shows the impact of the control on the impedance of AFE 1 when connected to the DC PDN. Notably, employing a slower tuning for the outer loop control results in a reduction of impedance in the low-frequency range. The analytical model and the impedance extracted from RT Box resulted in similar results. More importantly, the resonances of the system were accurately mapped.

Similarly, **Fig. 8.13a** illustrates how the control influences the impedance of AFE 6 when connected to the DC PDN. In this case, the analytical model derived from RNA fails to capture parameter tuning differences. This limitation arises because the equivalent linearized model of the CPL does not include the CC parameter gains. Nevertheless, the model represents faithfully the level and the divergence happens at the CC bandwidth for the magnitude optimum case. Also, Node 6 exhibits the anticipated behavior of a load, aligning well with the RNA prediction and confirmed.

8.4.2 Impact of the AC Impedance on the Nodal Impedance

The AC impedance at the Point of Common Coupling (PCC) plays an important role in the system's stability and reliability. This aspect often refers to a Short-Circuit Ratio (SCR) or/and reactance-to-resistance ratio (X/R). Both values are influenced by factors such as generator, transmission line

lengths, transformer, and system configuration.

In simple words, the SCR is related to the strength of the generator in supplying short circuit current during a fault. A higher value of SCR indicates a strong source that can contribute more to the current, enhancing the stability of the system.

On the other hand, the X/R ratio is a parameter that describes the balance between the inductive and resistance components of the network. A higher value indicates a more transient-dominated response during short circuits, while the opposite leads to a more resistive response. In a strong grid, the X/R is typically X/R$\leq$ 10.

Thus, to evaluate the impact of the AC impedance on the DC impedance, three different values of X/R are selected to test the system. The impedance is calculated considering the AC transformer rated at the power of the AFE, described in **Tab. 8.1**. **Fig. 8.14** shows the considered schematic for the AC side, and the two converters under analysis.

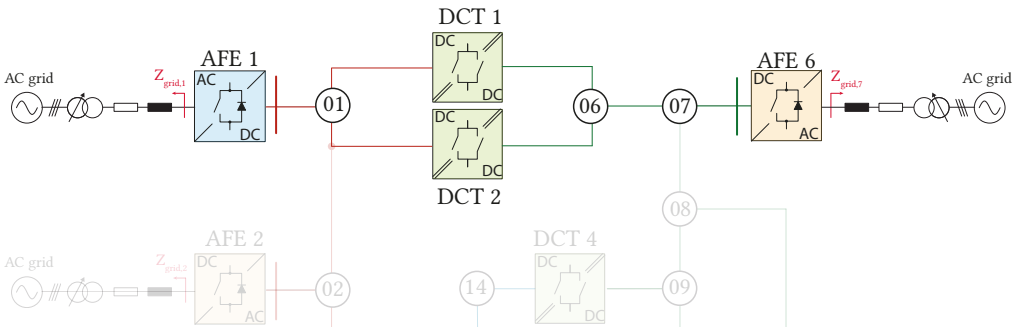


Fig. 8.14 Illustration of the considered AC grid after the LCL filter. The tests were performed with the complete system under steady state.

Fig. 8.15 shows the impedance of AFE 1 and AFE 6 extracted from RT Box for the X/R equal to 10, 5, and 1. It can be noticed that the AC impedance mostly affects the low-frequency range, as expected. For both voltage-controlled and current-controlled converters, the effect was to lower the impedance in the low-frequency range for higher values of X/R. This points out that the DC impedance is affected by the AC impedance, and for higher values of X/R, the impedance can differ from the ideal case with the strong predominately resistive grid.

Finally, it is important to note that the effect is not mapped by this proposed methodology using RNA, since the linearized model considers the perfect AC grid. Nevertheless, this effect can be investigated by using another approach for modeling the power converters, similar to the description made in [189], [190], which includes the effect of grid impedance and PLL loop. For such a case, a different methodology should be applied.

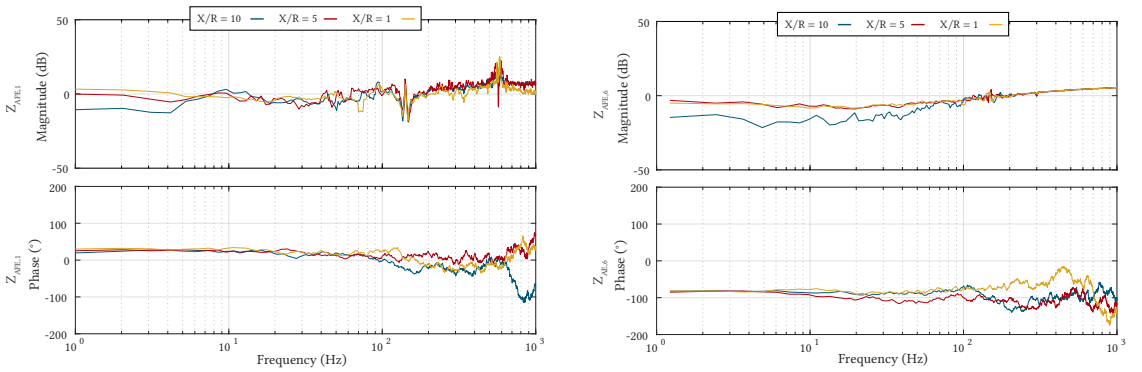


Fig. 8.15 Impact of the AC grid equivalent impedance on the nodal impedance at (a) Node 1 - voltage controlled, and (b) Node 7 - current controlled. Impedance extracted in the real-time simulation. For smaller valuer of X/R, the resistive behavior is predominant in the low-frequency range. After $f > 10$ Hz, no difference is visible for the voltage-controlled node, and after $f > 50$ Hz for the case of the current-controlled node.

8.5 Summary and Conclusion

This chapter presented the RT-HIL platform developed to explore a large and complex DC PDN with multiple DCTs. Through this real-time simulator, a highly meshed system was analyzed, and the operation of the system was verified using real controllers. The findings demonstrated the feasibility of operating such a system with the open loop-operated DCT in the system, allowing the establishment of the natural power flow.

Nonetheless, the use of real-time simulation for a large and complex system brought attention to certain limitations in the proposed methodology. The equivalent linearized model, used with the nodal matrices, lacks the inner current control loop of grid-connected converters, resulting in the loss of information within the control bandwidth. Additionally, the study showed the impact of AC impedance on the nodal impedance, which impacts the low-frequency range. This effect is not captured by the models once a perfect AC grid is considered. Lastly, while the linearization assumptions facilitate the extraction of main system resonances correctly, it becomes evident that the mismatches accumulate as the system grows in size and complexity, pointing out that a more detailed model would be necessary.

In conclusion, the RT-HIL simulation provided a means to assess a larger DC PDN with multiple DCTs and real controllers. The intended purpose of the DCT within the system was achieved and verified along with all open-loop strategies that were performed without introducing disruptive transients.

9
Summary and Future Work

This chapter concludes the thesis by summarizing its main findings. It summarizes the main contributions this thesis has brought to the field of DC systems and provides an overview of possible future research.

9.1 Summary and Overall Conclusions

This thesis focused on two crucial aspects for the broad implementation of DC PDNs in the future. The first aspect is the demonstration of the operating principles of the DCT and its essential features. This converter is responsible for connecting two DC buses, and transferring power according to the natural power flow of the system, i.e. operating as an AC transformer. This converter could enable more advanced DC PDN without adding an extra layer of control to the system.

Secondly, this thesis presented a methodology to assess the operation, stability, and planning of the DC PDNs with DCTs. The developments were adapted from the AC systems analysis tools, and adjusted for its use in a purely DC PDN with DCTs, allowing the implementation of a well-consolidated theory in the emerging system. Lastly, the methodology was tested with real-time simulations to verify the operation of the system with a large number of DCTs in the system. In the end, it proved to be possible to have such a system, mixing the dynamics of several converters to a single DC bus.

With these two parts, this thesis tackled two weak aspects in the current literature, which are the lack of tools to evaluate purely DC PDNs with DCTs, and the development of complete autonomous open loop operation of DCTs for the future DC PDNs. In this thesis, each chapter contains important information for a complete understanding of the topic.

Chap. 2 introduced the modeling and fundamental operating principles of the LLC converter, establishing the necessary modeling framework for this thesis. Firstly FHA modeling was shown, providing details about the operational principles and the soft-switching features of the LLC converter. Additionally, the dynamic equivalent model was outlined, serving a crucial role in configuring the operation of the DCT and used for the system-level studies. Lastly, the chapter showed the small-signal input impedance model, as a key parameter for scalability analysis in parallel operation.

Chap. 3 presented all the essential open-loop strategies for the reliable operation of the DCTs in DC PDNs. It covered the implementation of a soft-start strategy with a 3L operation, used to prevent MFT saturation and protect against inrush currents. Also, a comparative assessment of four distinct power reversal methods was performed, evaluating their performance and speed during the transient. These methods were based on the DC voltages, DC currents, and the resonant current of the DCT. Lastly, an idle mode was introduced to minimize unnecessary losses in the DCT when no power is being transferred to the load. While this mode could enhance operational efficiency during periods

of inactivity, it introduces a discontinuous state that could complicate the system-level analysis. All these strategies were tested in the two LV DCT prototypes.

Chap. 4 discussed the development of the MV DCT. In this chapter, the design and the construction of the MV DCT prototype were discussed, and tests to validate the static and dynamic voltage balancing of the NPC-leg were performed. The results indicate that thanks to the NPC-leg, a single symmetrizing resistor is more efficient for static voltage balancing compared to the four resistors needed for parallel balancing. Additionally, it was found that the relatively small value of the C-snubber is sufficient for dynamic voltage balancing. However, further tests under load conditions are necessary.

Chap. 5 explored the potential for scalability in terms of power increase with constant input/output voltages by connecting DCTs in parallel. Through an analysis of the input impedance, a sensitivity analysis of resonant parameters was performed, revealing that slight variations in the resonant tank could significantly impact converter characteristics. This sensitivity proved critical for achieving effective current sharing in parallel DCTs. Nevertheless, it was shown that changing the switching frequency also affected the input impedance, due to the new operating point. As a result, a solution for paralleling DCTs was suggested, consisting of operating the DCTs in parallel with different frequencies to compensate for input impedance mismatches and ensure satisfactory current sharing. The parallel operation of the DCT was tested with the two DCTs prototypes in the laboratory, and the impact of the switching frequency on the current sharing was demonstrated.

Chap. 6 detailed the methodology to analyze DC PDNs with DCTs. The methodology was developed to deal with a DC PDN with several converters in a scalable manner, for its use in the nodal notation. This approach simplified the representation of the power converter and its control loops, enabling the application of classical AC system analysis to the DC system. The methodology involves calculating the steady-state solution and frequency characteristics using nodal impedance. The chapter provided a practical demonstration of the methodology on a simple system, and the simulation in PLECS verified the analytical model.

Chap. 7 focused on the demonstration of the proposed methodology of **Chap. 6** for the DC PDN with DCTs. It investigated various aspects of the system's characteristics, such as the DCT's location in the grid, the dynamics of AC-DC converter control, and the impact of introducing an additional power converter to the system. It also evaluated the DC PDN with diverse network architectures within a dynamic power flow context. Furthermore, it presented a stability analysis using existing tools for stability assessment, demonstrating that the same tools employed in the AC system can be applied in the DC system with minimal to no adaptations.

Chap. 8 presented an RT-HIL platform developed to investigate large DC PDN. The RT-HIL, employing multiple RT-BOXES, enabled the simulation of a highly meshed MVDC PDN, with a better representation of the power converters by using real controllers. It was demonstrated that a large DC PDN with multiple DCTs and diverse sources and loads can effectively operate together when all system converters are well-designed. Moreover, it was shown that the impact of the control dynamics as well as the AC side impedance has a significant impact on the DC impedance characteristics, especially on the low frequency range. Such a conclusion is derived for this specific example and can be derived using the same methodology for other systems.

9.2 Future Work

This thesis has developed several valuable tools for researching DCTs and DC PDNs. These tools facilitate diverse studies in both power converter-level and system-level analysis, offering opportunities for further improvements and applications.

The LV DCT prototypes that have been developed can be used as a DCT in various projects in the laboratory. Improvements to the DCT features, aimed at optimizing its performance in DC PDN, can be examined. Also, experimental testing of new methods for operating and protecting the DCT, and performance comparison with other DC-DC converter is possible, among other topics. Currently, these DCTs are actively utilized in the Hyperride project [17], which delves into the operation of a hybrid AC-DC grid.

In the subject of system analysis for DC PDNs with DCTs, there is an opportunity to shift focus towards addressing the system as a power distribution problem. This opens up a broad spectrum of research areas in power system planning and operation. Possible investigations include optimal power flow control, system reconfiguration, fault analysis, multi-terminal DC grids, distance to instability, and numerous others. Clearly, each of these subjects requires specific software and models, along with well-defined objectives and metrics.

Also, the RT-HIL models offer the flexibility to integrate the MV converters into other HIL platforms in the laboratory. Specifically, the HIL model of the DCT is applied together with the MMC HIL platform developed in the laboratory to assess the control dynamics, when the MMC acts as a power supply to the DCT. The RT-HIL tests are conducted to evaluate the feasibility and challenges of the control in scenarios involving a low-resistance path between two DC ports and the low capacitance value of the DCT's DC link. This work was developed and disseminated in [191]. Future plans include utilizing the MMC as a power supply to the DCT in the laboratory.

Finally, the MV DCT serves as a versatile research platform for various projects in the area of MV DC systems. It enables research on topics such as the resonant operation of IGCTs, 2L mode operation of the 3L-NPC, medium-frequency operation, MV DCT operation, integration of new gate units, device characterization, and more. For more details of future works related to the MV DCT, the following section provides a brief overview, outlining the path toward its complete commissioning.

9.2.1 Future work of the MV DCT

In this thesis, the MV DCT prototype was assembled to test the power stages with the MFT, investigating the static and dynamic voltage balancing of the IGCTs, for the 5 kV and 5 kHz case. Although the converter is intended for 10 : 5 kV/kV operation, the complete validation of the 5 : 5 kV/kV operation is essential to address any potential problems before proceeding to test the 10 kV stack.

Throughout the tests, challenges emerged when handling faults. Despite the ability of the RC-IGCTs to withstand $20 - 30$ times the rated current, the anti-parallel diode encounters limitations in handling high di/dt. Various studies have discussed the potential benefits of soft-switching and the di/dt of the LLC topology's load current, which eliminates the need for a clamping circuit. However, issues arise in protecting the RC-IGCTs. At the moment an RC-IGCT fails in short-circuit, there is no device providing limitation for the current rate of change, only the stray inductance of the current path. This is potentially not sufficient for a control action to take place and no action is taken to prevent the complementary device from turning on. A solution for this case was suggested in [192] with the

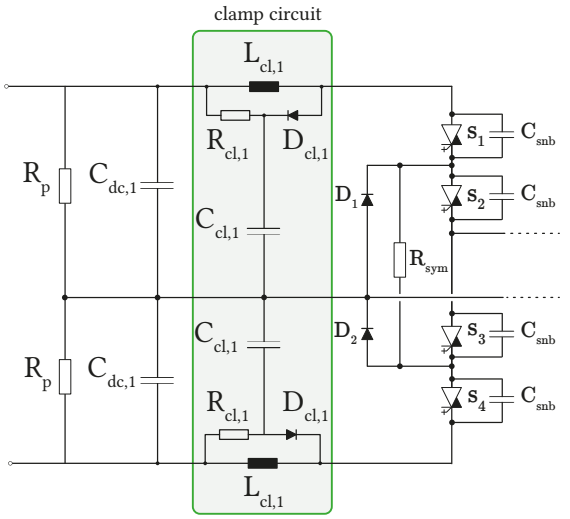


Fig. 9.1 Schematic of the NPC-leg including the clamping circuit and the dynamic and static voltage balancing strategies.

use of a gate unit including the anode-cathode voltage measurement to prevent the turn-on of the complementary RC-IGCT in the event of a short circuit. Nevertheless, this feature is not available in the ABB's gate unit, as such a gate unit is designed for hard-switching applications, including the clamping circuit.

The future tasks for the MV DCT involve three main aspects: designing the clamping circuit, re-arranging new elements in the cabinet, and completing the commissioning of the converter. The power stage schematic, incorporating the clamping circuit, is illustrated in **Fig. 9.1**. A detailed design procedure for such components can be found in [107].

After the inclusion of the clamping circuit, similar experiments performed in this thesis must be conducted. Once the commissioning phase has been completed, the MV DCT can serve various research objectives, including the characterization of 10 kV devices, MV DCT operation, acting as an interface for MVDC supplies, and other potential applications.

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