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Comparative Analysis of Unidirectional High Step-Up Converters for Medium-Voltage Applications

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Abstract

Connection of renewable energy sources to the MVDC collection grid requires an efficient, reliable and economically viable high power DC/DC converter. With these requirements in mind, the paper presents a comparative analysis of two bulk-power processing converter topologies - the Single Active Bridge (SAB) and the Phase Shifted Full Bridge (PSFB) converter from the standpoint of suitability for the application, considering power hardware design and control requirements. The aim of the work is to provide a clear summary of trade-offs between the SAB and PSFB converter without their detailed design optimization. An overview of the converters' operating principles and steady-state models is presented first, laying the foundation for the comparison through converter characteristics. Based on carefully chosen exemplary designs the advantages and drawbacks of both topologies are identified and preliminary semiconductor losses are evaluated for each case. Finally, the input voltage regulation of the converters is addressed as well as additional considerations relevant for the applications of interest.

1 Introduction

The increased presence of renewable energy sources has brought forward numerous considerations toward their integration into the grid by means of Direct Current (DC) technologies. There is now strong indication that present Alternating Current (AC) systems will be complemented or replaced by their DC counterparts not only at High Voltage (HV) levels but at Medium Voltage (MV) levels as well [1], [2]. This is particularly true for the MVDC collection grids, which are being investigated for the large solar plants [3] and wind farms [4]. Depending on the considered power levels and required distances, the shift towards MVDC collection can lead to increased system efficiency [5]. The key factor still impeding this transition is the lack of a strong business case for all involved parties.

Recent advances in the field imply that, in the near future, single wind turbine power will be approaching $20\,\mathrm{MW}$ [6]. Similar power levels can be processed by central inverters in large-scale solar plants. While the input voltage, depending on the source, is in the $(1.5-5)\,\mathrm{kV}$ range, the MVDC collection grid voltage can reach several dozens of kV in both cases, with $20\,\mathrm{kV}$ being taken as an example in this paper. This implies that the application requires a unidirectional high step-up high power DC/DC converter as the interfacing element. Fig. 1 illustrates the application and considered topological solutions on a conceptual level. The collection grid voltage is regulated by the DC/AC converter and it is assumed that maximum power point tracking and conversion from AC to DC (in case of wind turbines) is performed by the source-side converters. Consequently, it is required that the DC/DC converter regulates its input voltage.

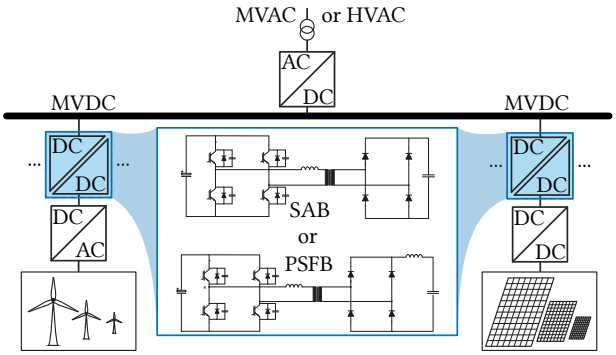

Fig. 1: Wind farm or solar plant connection to the MVDC collection grid

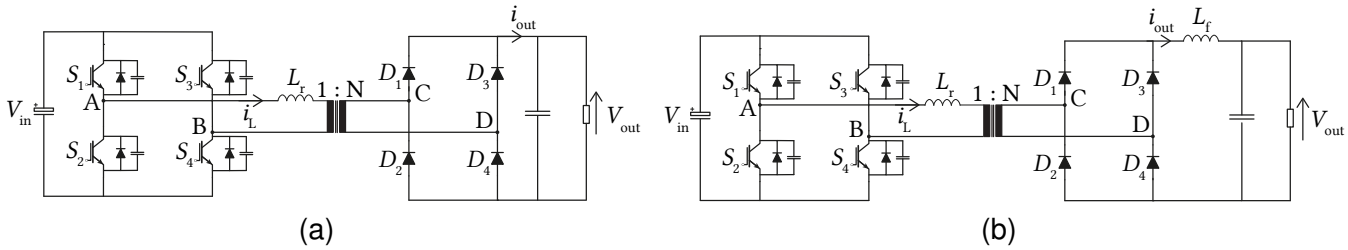

Fig. 2: Topologies analysed in this work: (a) SAB converter (b) PSFB converter

In contrast to the widely studied modular solid state transformer, the concept of monolithic (bulk-power processing) unidirectional DC/DC converters has not been extensively investigated for these applications, with few notable exceptions [7]–[15]. The lack of standardization and demand from the market has also led to a scarcity of pilot projects and demonstrators. Nonetheless, the monolithic DC/DC converter emerges as an attractive solution, potentially offering a reduction of isolation overhead and an overall more robust structure compared to the partial-power processing alternative.

In the scientific literature, bidirectional converters such as the dual active bridge and resonant converters are drawing significant attention. Although prototypes of these converters exist [16], [17], the resonant topologies present additional challenges for control in high power applications (usually requiring an additional converter to perform the control, otherwise leading to reduced efficiency), while an active rectifier introduces additional costs and complexity in the considered application, where, generally, only unidirectional power flow capabilities are required.

Among the monolithic unidirectional converters, two particularly attractive topologies, considering complexity and control requirements, are the SAB and PSFB converter. These converters have already been investigated to some extent as an interfacing element between wind [8], [9] and solar plants [15] and the power grid. Both converters offer high efficiency through soft switching as well as a comparatively simple architecture. These topologies, although well known [18], [19], have never been demonstrated nor comprehensively compared at MW-level ratings, indicating the need for further research and motivating this work.

With the presented considerations in mind, the paper is focused on an analytical comparison of the SAB and PSFB converter, based on output power and current characteristics, and semiconductor losses. Additionally, other aspects relevant for the application such as input voltage control and specific hardware requirements are addressed. It should be emphasised that the presented methodology allows a juxtaposition of the two converters without their respective optimization, strictly through appropriately selected exemplary designs. This allows the evaluation of the converters' performance based on analytical models in steady state.

2 Specifications and Designs

In Tab. 1, the overall requirements for the converter are defined. The $\pm\ 10\,\%$ variation of the input/output voltage is taken as a representative design example, considering the input voltage control requirements under output voltage and input current disturbances. The comparison is carried out for the wind farm and power grid interconnection application, with similar conclusions possible for the solar plant case as well.

The two studied toplogies are shown in Fig. 2. It can be seen that the SAB converter features only an inductor at the primary side of the Medium Frequency Transformer (MFT), while the PSFB has an additional di/dt limiting filter inductor at the output (alternatively, split and installed in both DC lines). It should be mentioned that the primary-side inductance of the PSFB is typically much smaller than

Tab. 1: General converter specifications

Description	Symbol [Unit]	Value
Input voltage	V_{in} [kV]	$5 \pm 10\,\%$
Output voltage	V_{out} [kV]	$20 \pm 10\,\%$
Output power	P_{out} [MW]	20
Sw. frequency	f_{s} [Hz]	500

the filter inductance and is usually carried out as the leakage inductance of the MFT. For the SAB, the inductor is often realized as an additional discrete component. Both the SAB and the PSFB converter can operate in two possible modes of operation - Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM).

In the analysis, three different designs, shown in Tab. 2, are considered for both converters. Each considered design conforms to the specifications from Tab. 1, enabling a fair comparison. The first and second design were oriented toward CCM and DCM operation respectively, in the entire input/output voltage range under nominal power. For the third design, the worst-case operational conditions are taken into account, without any operational mode constraints. Each design is elaborated in more detail in Section 4. It should be noted that none of the designs are optimized, and that their main purpose is to enable grounds for comparison between the SAB and the PSFB converter in terms of capability to serve the considered application.

3 Analytical Modeling

The phase-shift modulation, offering the possibility of input/output voltage or power-flow control, and being the most commonly proposed modulation strategy for both converters, is considered in the analysis. In this work, it is considered that the leg containing switches S_1 and S_2 is the leading leg, while the other leg is the lagging leg. The value of phase shift (ϕ) translates into the duty cycle (D) of the primary side voltage V_{AB}. This relation can be described as:

$$D = 1 - \frac{\phi}{\pi} \tag{1}$$

Both the SAB and the PSFB converter can operate either in CCM or DCM depending on the value of the duty cycle and other, fixed, parameters (N, $V_{\mathrm{in}}, V_{\mathrm{out}}$). If a converter operates in CCM, by decreasing the duty cycle, at some point, it enters into DCM. This point corresponds to the boundary duty cycle, which is the same for both converters and equal to the DC voltage conversion ratio ($D_{\mathrm{BCM}} = \frac{V_{\mathrm{out}}}{NV_{\mathrm{in}}}$).

In Fig. 3, the steady-state waveforms are shown for both converters operated in CCM/DCM along with conduction intervals for all semiconductor devices ("+" indicates the IGBT alone, while "-" corresponds to antiparallel diodes) during one switching cycle. It should be mentioned that the magnetizing inductance is considered to be infinite in this model which is a good approximation for the purposes of the analysis. The notation in the figure is self-explanatory. Therefore, some of the shown symbols are not explicitly explained in the text. Rather, a concise body of equations governing the operation of each converter in each operating mode is given, and comments are offered only where relevant.

Tab. 2: Exemplary converter designs

Design 1		
Parameter / Symbol [Unit]	**SAB1**	**PSFB1**
Leakage inductance / L_{r} [µH]	94.7	29.6
Filter ind. / L_{f} [mH]	n/a	2.7
Turns ratio / N	8	5.5
Nom. duty cycle / D_{nom}	0.62	0.75
Design 2		
Parameter / Symbol [Unit]	**SAB2**	**PSFB2**
Leakage inductance / L_{r} [µH]	10.74	1.79
Filter ind. / L_{f} [mH]	n/a	0.22
Turns ratio / N	5	5
Nom. duty cycle / D_{nom}	0.29	0.29
Design 3		
Parameter / Symbol [Unit]	**SAB3**	**PSFB3**
Leakage inductance / L_{r} [µH]	8.27	75.4
Filter ind. / L_{f} [mH]	n/a	9.6
Turns ratio / N	6.5	6.5
Nom. duty cycle / D_{nom}	0.59	0.82

3.1 SAB Converter

Referring to the left-hand side of Fig. 3a, the steady-state waveforms of the SAB converter operated in CCM can be described by the following equations:

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = N\frac{DT - 4t_\delta}{T} \tag{2}$$

$$I_1 = \frac{V_{\mathrm{in}} - V_{\mathrm{out}}/N}{L_r}(DT/2 - t_\delta) \tag{3}$$

$$I_2 = \tfrac{V_{\mathrm{in}} - V_{\mathrm{out}}/N}{L_{\mathrm{r}}}(DT/2 - t_\delta) - \tfrac{V_{\mathrm{out}}/N}{L_{\mathrm{r}}}(1-D)T/2. \tag{4}$$

The DCM mode operation is depicted on the right-hand side of Fig. 3a. The corresponding description can be easily derived:

$$\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = N\frac{DT}{T - 2t_\alpha} \tag{5}$$

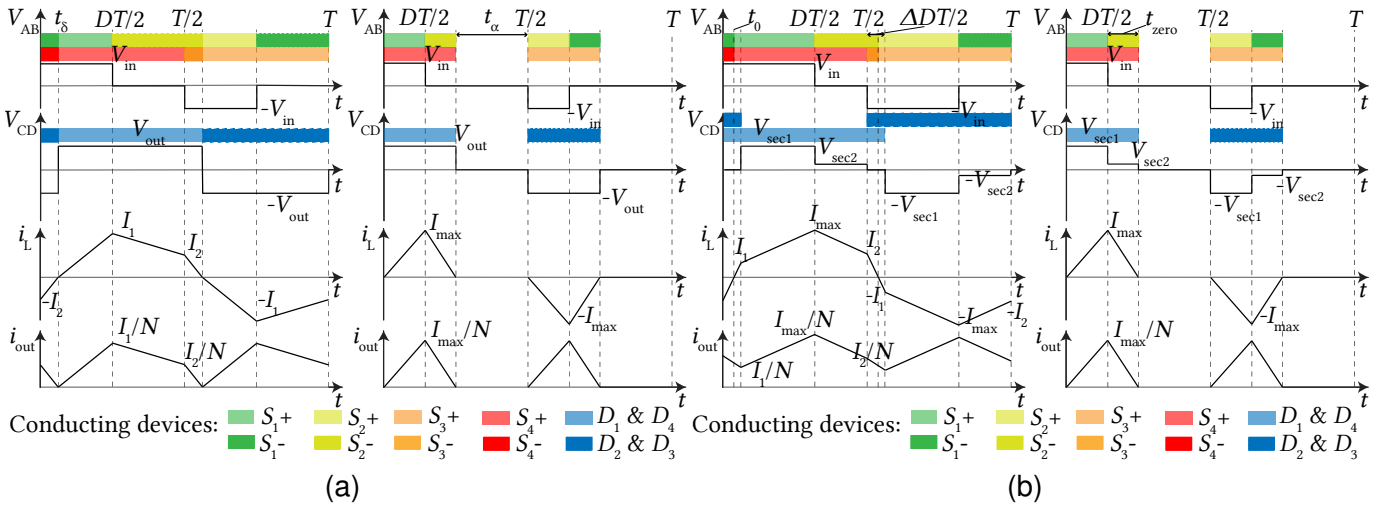

Fig. 3: Steady-state waveforms and conduction states: (a) SAB converter: CCM (left) and DCM (right) (b) PSFB converter: CCM (left) and DCM (right)

$$I_{max} = \frac{1}{L_r}(V_{in} - \frac{V_{out}}{NV_{in}})DT/2. \quad (6)$$

3.2 PSFB Converter

CCM operation of the PSFB converter is illustrated on the left-hand side of Fig. 3b. The voltage drop across L_r is always taken into account, although it is usually neglected during the $(\frac{\Delta DT}{2}, \frac{T}{2})$ interval, which is only justified if L_r is much smaller than L_f (when reflected to the primary side of the transformer). Thus, the model contains no simplifications in this sense, appreciably enhancing precision when L_r is considerable, and can be described by:

$$V_{sec1} = \frac{NL_fV_{in} + N^2L_rV_{out}}{L_f + N^2L_r} \quad (7)$$

$$V_{sec2} = \frac{N^2L_rV_{out}}{L_f + N^2L_r} \quad (8)$$

$$D_{eff} = \frac{V_{out} - V_{sec2}(1-D)}{V_{sec1}} \quad (9)$$

$$K = \frac{V_{in}\Delta D}{4L_rNf_s} + \frac{(V_{out} - V_{sec2})(1-D)}{4L_ff_s} \quad (10)$$

$$\Delta I_{out} = \frac{(NV_{in} - V_{out})D_{eff}}{2f_s(L_f + N^2L_r)} \quad (11)$$

$$I_1 = N(K - \frac{\Delta I_{out}}{2}) \quad (12)$$

$$I_2 = N(K + \frac{\Delta I_{out}}{2} - \frac{(V_{out} - V_{sec2})(1-D)}{2L_ff_s}) \quad (13)$$

$$I_{max} = N(K + \frac{\Delta I_{out}}{2}) \quad (14)$$

$$t_0 = \frac{V_{sec2}(D-1) + NV_{in}D - V_{sec1}D_{eff}}{4NV_{in}f_s}. \quad (15)$$

In the equations, f_s is the switching frequency. D_{eff} is equal to D-ΔD, and corresponds to the interval when V_{sec1} is applied at the MFT secondary. When L_f is much larger than L_r, this value becomes equal to $\frac{V_{out}}{NV_{in}}$ and is typically called the effective duty cycle of the secondary voltage. ΔI_{out} is the peak to peak ripple of the output current. While all values shown in Fig. 3b are accurately described, expression (10) also offers a good approximation of the average output current (which can be accurately expressed based on the presented model), by neglecting the change of output current slope during the duty cycle loss interval.

Equations (7) and (8) still hold true in DCM operation, shown on the right-hand side of Fig. 3b, as well as:

$$I_{max} = \frac{(NV_{in} - V_{sec1})D}{2N^2L_rf_s} \quad (16)$$

$$t_{zero} = \frac{(NV_{in} - V_{sec1})D}{2V_{sec2}f_s}. \quad (17)$$

Based on the presented steady-state analytical models and knowing the conduction states, through integration of linear segments, expressions for RMS and average currents can be derived for each semiconductor device of the converters. These expressions, although not shown, are used to obtain the converter characteristics in the following section as a basis for analysis.

4 Current Stress Comparison

In this section, the three pairs of SAB and PSFB converter designs are compared based on their output power and current characteristics. In the presented output power graphs, only the characteristics corresponding to extreme and nominal combinations of the input and output voltages are displayed, while all other characteristics fall between the shown ones. These cases are noted as: ① $(V_{\mathrm{in,min}}, V_{\mathrm{out,max}})$; ② $(V_{\mathrm{in,min}}, V_{\mathrm{out,min}})$; ③ $(V_{\mathrm{in,nom}}, V_{\mathrm{out,nom}})$; ④ $(V_{\mathrm{in,max}}, V_{\mathrm{out,max}})$; ⑤ $(V_{\mathrm{in,max}}, V_{\mathrm{out,min}})$. It should be noted that the devices within the same leg experience the same current stress, only in different half-cycles of switching. Therefore, only one device per leg is considered in the analysis. Only RMS currents are displayed, with similar conclusions being valid for average currents. Also, within current characteristics graphs, only nominal input/output voltage is shown with similar conclusions being applicable for any other input/output voltage combination.

4.1 CCM Operation

Converters SAB1 and PSFB1, defined in Tab. 2, are designed to operate in CCM at rated power in the entire input/output voltage range. It can be shown that the RMS currents on the primary side of the SAB and PSFB converters increase with the transformer turns ratio. Therefore, the turns ratio is kept as low as possible for the SAB1 and slightly above the theoretical minimum ($N_{\mathrm{min}} = \frac{V_{\mathrm{out,max}}}{N V_{\mathrm{in,min}}}$) to avoid an excessively high slew rate of the output power in CCM and/or high secondary voltage, for the PSFB1. This, nonetheless, resulted in a considerably lower required turns ratio for PSFB1 than for SAB1. The output power characteristics are shown for both converters in Fig. 4.

In Fig. 5, the current stress of the primary and secondary side devices is shown for both converters. It

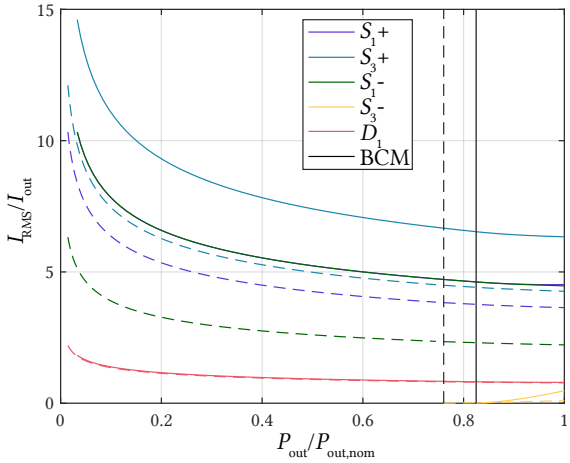

Fig. 5: Current characteristics: SAB1 - full line and PSFB1 - dashed line

can be seen that for all devices on the primary side, the PSFB1 achieves significantly lower RMS currents, while the rectifier diodes experience similar current stress.

4.2 DCM Operation

SAB2 and PSFB2, were designed to operate in DCM at rated power (hence, also at all partial power levels) for any input/output voltage combination. To make the comparison fair in this case, the same turns ratio (slightly higher than the theoretical minimum for nominal power transfer) is adopted for both converters. As a design rule, it was considered that the converters must operate in BCM (boundary mode) if the input voltage is minimal and output voltage is maximal. This rule helps to reduce the RMS currents which are drastically increased with deep DCM operation (low duty cycle for nominal power operation) and, again, provides leveled ground for the analysis. As obvious from the output power characteristics shown in Fig. 6, this resulted in identical behavior of both converters in DCM. It should be mentioned that the PSFB inductances can be selected in an infinite number of ways (as long as the total inductance reflected to one side of the

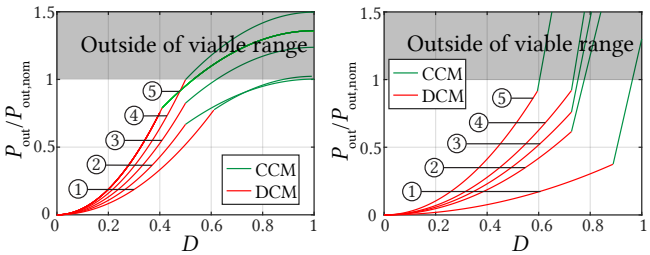

Fig. 4: Output power characteristics: SAB1 and PSFB1

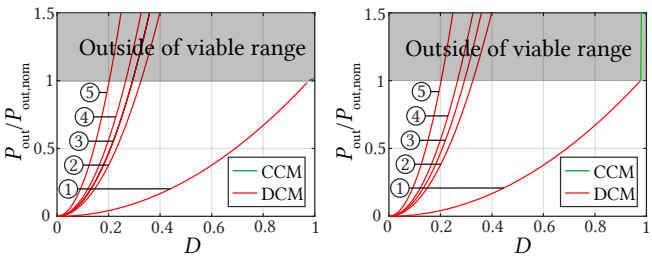

Fig. 6: Output power characteristics: SAB2 and PSFB2

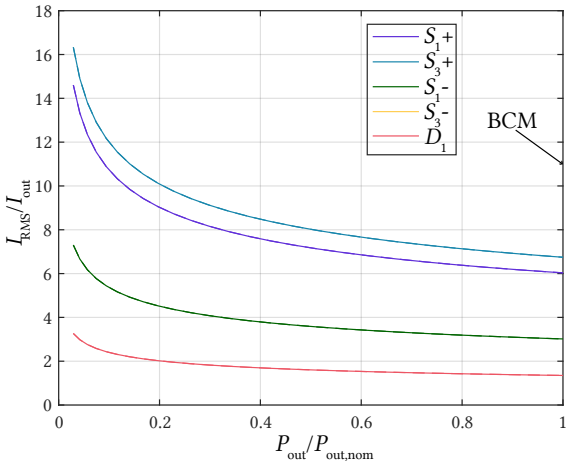

Fig. 7: Current characteristics: SAB2 - full line and PSFB2 - dashed line (coincides with the full line)

transformer remains the same) to achieve exactly the same characteristics in DCM. However, the fact that a high output filter inductance increases the voltage across the rectifier should be kept in mind.

In Fig. 7, the device RMS current stress is shown for both converters. As expected, the current stress in DCM is exactly the same for SAB2 and PSFB2. Despite this fact, the SAB converter shows clear advantages compared to the PSFB when both are designed for DCM operation. Since the SAB does not feature an output inductor, the total required inductance can be reduced by a factor of almost N^2, and the rectifier voltage is clamped to V_{out} which reduces the rectifier voltage stress.

4.3 Operation Without Mode Constraints

Converters SAB3 and PSFB3 were designed without CCM/DCM operation requirements at rated power as, considering the entire input/output voltage range operation, an optimal design is likely the one allowing a combination of CCM and DCM operation, at least for the SAB. Again, it must be emphasised that SAB3 and PSFB3 are not optimized designs. As a basis for fair comparison, in this case, the same MFT turns ratio equal to 6.5 is selected for both converters. This value of N is selected as it provides a good trade-off between forcing the SAB converter toward DCM operation, which is generally the case with low turns ratios, and CCM operation, which is achievable with higher turns ratios. For the PSFB, the additional degree of freedom originating from the additional inductance, enables CCM operation in the entire voltage range

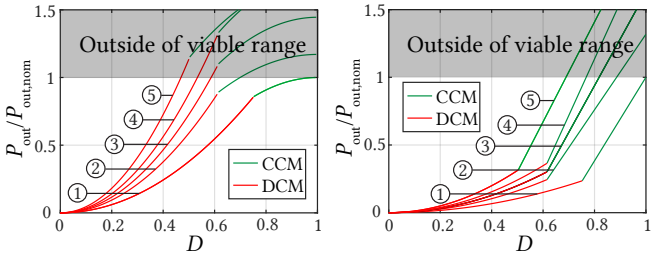

Fig. 8: Output power characteristics: SAB3 and PSFB3

even with low turns ratios. The final requirement for both converters, ensuring a fair comparison, is that nominal power is achieved at $D = 1$ when input voltage is minimal and output voltage is maximal.

Output power characteristics are shown in Fig. 8. It can be seen that, for the SAB3 converter, nominal power is reached both in CCM and in DCM for various characteristics. On the other hand, the PSFB3 output power characteristics indicate continuous operation in CCM under nominal power. It should be mentioned that the PSFB3 could have been designed differently for this comparison. The shape of the output characteristics of a PSFB converter depends on the parameter r which can be defined as the ratio of the two inductance reflected on the same transformer side ($r = \frac{L_{\mathrm{f}}}{N^2 L_{\mathrm{r}}}$). Comparing two designs, one with a high value of r, and the other with the low value of r for the same L_{r}, it is possible to observe that the second design results in a higher filter inductance which reduces the current ripple of the output current. This results also in lower RMS currents of the primary. The downside of the second design is a large variation of output power with duty cycle change in CCM. Therefore, it

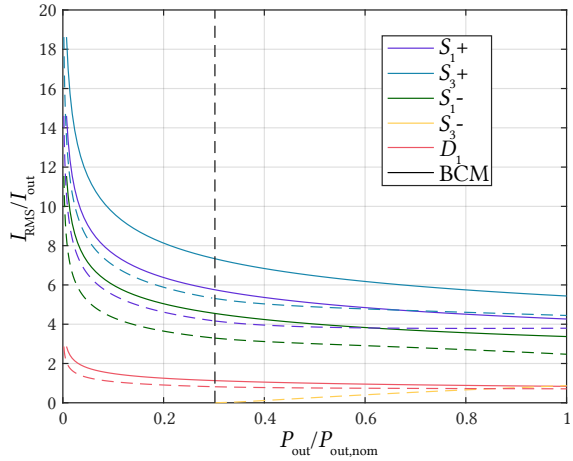

Fig. 9: Current characteristics: SAB3 - full line and PSFB3 - dashed line

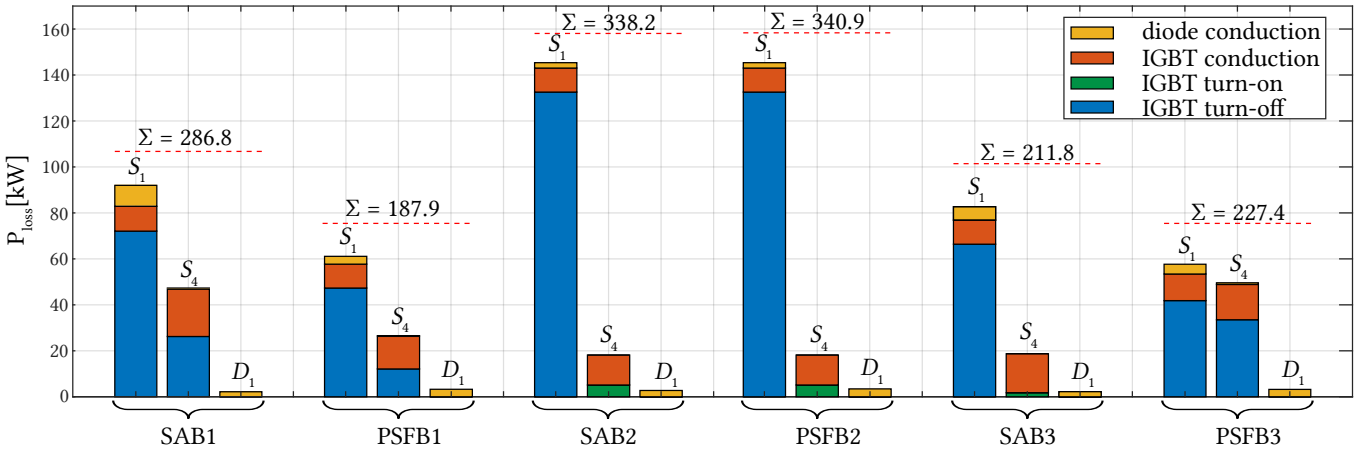

Fig. 10: Loss distribution of the 6 designs under nominal conditions: leading leg switch S_1, lagging leg switch S_4 and rectifier diode D_1. The sum represents the total losses of the converter ($\Sigma = 2P_{\mathrm{S1}} + 2P_{\mathrm{S4}} + 4P_{\mathrm{D1}}$).

can be concluded that, by increasing the factor r, it is possible to achieve lower RMS current stress and smaller output current ripple, but at a price of loose control of the output power. A conservative value of $r = 3$ was adopted for PSFB3 as a good trade-off in this sense.

In Fig. 9, it can be observed that the additional degree of freedom of the PSFB resulted in lower RMS currents in all devices. Again, a different design of the PSFB3 could have resulted in an even more obvious difference at the cost of higher slew rate of the characteristics shown in Fig. 8 (right) in CCM. From Fig. 9, it can also be seen that the PSFB3 operates mainly in CCM, but at lower power levels (around $0.3P_{\mathrm{nom}}$) enters into DCM. On the other hand, the SAB3 converter operates in DCM even at nominal power levels.

5 Semiconductor Losses

In this section, the converter designs from Tab. 2 are compared based on semiconductor losses. On the inverter side, conduction and switching losses of IGBT ($S+$), as well as conduction losses of the antiparallel diodes ($S-$) are taken into account. On the rectifier side, only conduction losses of the diodes are considered. Owing, to the soft switching properties of these converters, the reverse recovery losses of all diodes are considered negligible. The snubber circuitry related to voltage balancing and protection is not considered in this analysis, even though it is clear that addition of these elements would bring additional losses in practical design. The considered devices are 5SNA 1000G650300 ($6.5\,\mathrm{kV}/\ 1000\,\mathrm{A}$) for inverter switches and 5SDD 75Y8500 ($8.5\,\mathrm{kV}/\ 6720\,\mathrm{A}$) for the rectifier diodes. It should be mentioned that the selected devices serve only as an example for the comparison, and that the thermal and cooling aspects were not considered either.

In Fig. 10, the loss distribution is shown for each considered case. It should be pointed out that, in all cases, the devices in the same leg (leading or lagging) are subject to the same losses. Therefore, only the losses per single device position (e.g. upper switch) within the leading and lagging leg are shown. Likewise, only the losses per single rectifier diode position are displayed. It should be also mentioned that, although conduction losses of the antiparallel diodes of the lagging leg devices are low, and therefore hardly visible for SAB1 and PSFB1 converters, they still exist. The losses are, in all cases, shown for operation with nominal input and output voltages and output power. (Σ) represents the sum of all semiconductor losses for each converter.

Tab. 3 shows the required number of parallel connected IGBTs ($N\mathrm{p}$) and series connected rectifier diodes ($N\mathrm{s}$), determined based on the maximum current stress of the IGBTs ($I\mathrm{max}$) and maximum voltage across the rectifier ($U\mathrm{max}$) respectively, thus indicating the sizing rules. It is worth mentioning that the maximal voltage stress on the primary side corresponds to the input voltage, while the maximum current stress of the rectifier diodes is comparable with the peak output current which is in all cases well below the selected device ratings.

Tab. 3: The required number of used devices

Converter	Imax [kA]	Umax [kV]	Np	Ns
SAB1	14.8	20	10	4
PSFB1	9.7	25.6	7	6
SAB2	27.3	20	18	4
PSFB2	27.3	24.2	18	5
SAB3	13.6	20	9	4
PSFB3	8.6	29.4	6	6

Converters SAB1 (semiconductor efficiency $\eta = 98.59\%$) and PSFB1 ($\eta = 99.07\%$) feature a similar loss distribution with the turn-off losses (particularly of the leading leg) being dominant. As the converters are designed for CCM operation, turn-on losses do not appear, owing to the Zero Voltage Switching (ZVS) in this mode. Clearly, PSFB1 is superior to SAB1 in terms of losses and device count.

In DCM operation, converters SAB2 ($\eta = 98.34\%$) and PSFB2 ($\eta = 98.32\%$) are almost exactly the same, as explained in the previous section. The advantage of the SAB converter here comes to the fore again, this time, in the form of lower number of rectifier diodes due to lower secondary voltage stress, and slightly lower losses overall. Considering that the converters now operate in DCM, the turn-off losses of the lagging leg are zero as the current is zero at the corresponding instants owing to Zero Current Switching (ZCS) in this mode. However, the turn-on losses are present as the anti-parallel diodes of the lagging leg no longer conduct prior to IGBT turn-on. The main contributor in the losses are the leading leg turn-off losses, penalised by the high RMS current in DCM.

Without operational mode constraints, the design rules resulted in the SAB3 ($\eta = 98.95\%$) operating in DCM and PSFB3 ($\eta = 98.87\%$) in CCM for nominal input/output voltages. It can be seen that SAB3 has slightly lower losses than PSFB3. However, this is mainly a consequence of the higher required number of parallel connected devices in this converter, lowering the primary side losses. Therefore, it is again evident that the PSFB converter shows more advantages than drawbacks overall, in this comparison as well.

Comparing all six designs, it can be said that CCM operation is preferable from the standpoint of semiconductor efficiency and can lead to lower device count on the inverter side. The main disadvantage

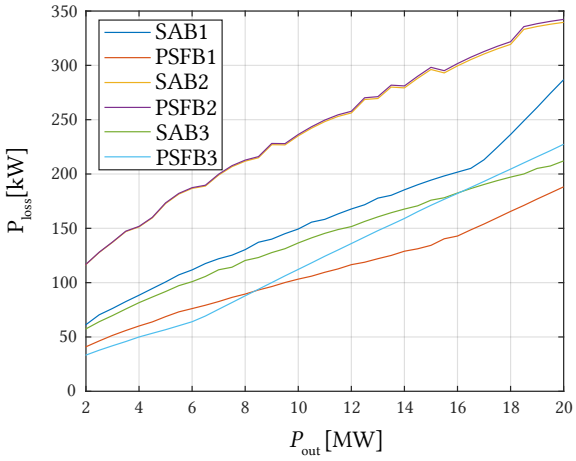

Fig. 11: Total semiconductor losses of the six converters under varying output power levels

of CCM operation of the PSFB, compared to the SAB is the higher secondary-side voltage, requiring more diodes for blocking. Therefore, it can be said that PSFB operated in CCM can lead to highest semiconductor efficiencies but at the expense of higher rectifier voltage stress.

In Fig. 11, the total losses of the six converters are shown for nominal voltages and varying output power levels, from 2MW up to 20MW. It can be concluded that, from the perspective of semiconductor losses, the PSFB converter is superior compared to the SAB converter. The only exception to this are designs for DCM operation over the entire operational range, where the SAB converter shows advantages.

6 Additional Considerations

In this section, additional considerations relevant for SAB and PSFB comparison at MW-levels are briefly addressed. The considerations are specific to the application and include feasibility of input voltage control and transient voltage suppression requirements.

6.1 Input Voltage Control

As mentioned, the DC/DC converters from Fig. 1 must regulate their input voltage under the disturbances caused by input current variation (dependant on the source power generation), and MVDC collection grid voltage fluctuations which are outside of its control.
To realize the input voltage control, only the low voltage at the input of the converter needs to be

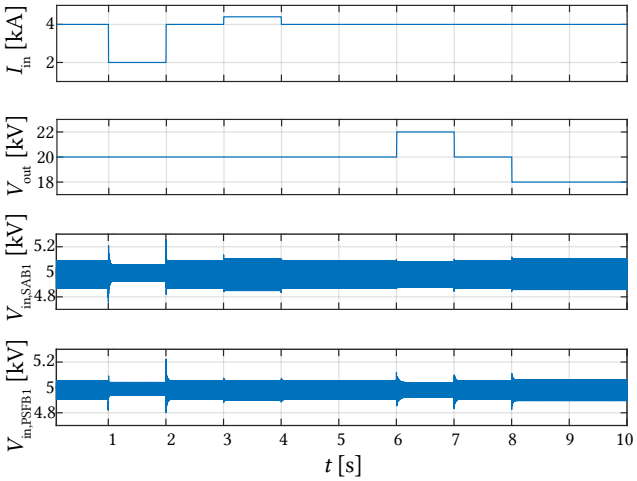

Fig. 12: Input voltage control under disturbances: SAB1 and PSFB1

measured and used as the feedback variable. The error between the wanted reference and measured value is fed to a simple PI regulator. The regulator directly controls the duty cycle of the primary side voltage. E.g. if generated power is increased, the input voltage has a tendency to increase, so in order to maintain the wanted reference, the duty cycle is increased and more current is drawn from the input capacitor. Conversely, under lower power production, the duty cycle is decreased, drawing less current from the input capacitor.

To demonstrate the feasibility of input voltage control, the above-explained controller is implemented for converters SAB1 and PSFB1. In Fig. 12, the results are shown. It can be seen that both converters can control the input voltage under varying profiles of input current and output voltage. Therefore, it is demonstrated that the control can be implemented in both cases. However, designing a PSFB converter to have a high output power variation with small duty cycle changes can lead to poor input voltage control in the described scenario as the resolution of the duty cycle variation is limited.

6.2 Additional Hardware Requirements

Unlike the SAB, the PSFB converter features an output filter inductance which can reduce the output current ripple. However, due to the existence of this inductance, in steady state operation in CCM, a voltage ringing occurs between the parasitic capacitors of the rectifier (and transformer) and the primary-side inductance. This phenomenon occurs after the duty cycle loss interval. While the maximum secondary voltage is defined by (7) in the ideal case, when the parasitic capacitance is considered it can be described by:

$$V_{\mathrm{secMAX}} = \frac{2(L_{\mathrm{f}} N V_{\mathrm{in}} + L_{\mathrm{r}} V_{\mathrm{out}})}{(L_{\mathrm{f}} + L_{\mathrm{r}})}. \qquad (18)$$

Assuming that $L_{\mathrm{f}} >> L_{\mathrm{r}}$, (7) can be approximated as NV_{in}, and (18) as $2NV_{\mathrm{in}}$. It becomes obvious that the ringing leads to an almost twofold increase of the secondary voltage, presenting itself as an inherent disadvantage of the PSFB topology. It should be emphasised that the rectifier voltage of the PSFB is inevitably higher that the rectifier voltage of the SAB (which is clamped to the grid voltage) even without considering the parasitics. The voltage ringing imposes additional requirements for the rectifier design in the case of the PSFB converter compared to the SAB converter. This issue can be addressed either by oversizing the rectifier, which may be impractical, considering the voltage levels, or by introducing additional clamping circuitry, imposing both losses and additional components.

7 Conclusion

In the paper, the SAB and PSFB converter were compared from the standpoint of current stress and semiconductor losses. It was shown that higher semiconductor efficiency can be achieved with the PSFB converter. By comparing several relevant cases, it was demonstrated that the advantages of the PSFB converter can be only utilized if the converter operates in CCM, while in DCM, the SAB is the superior topology. Several other considerations relevant for topology selection were also presented, such as the increased rectifier voltage stress of the PSFB converter and potential control issues. This makes the ultimate selection of the topology a trade-off between several presented factors.

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