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Voltage Balancing of a Split-Capacitor IGCT 3L-NPC Leg for the Resonant DC Transformer

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Abstract

This work investigates the static voltage balancing challenges in an IGCT-based LLC resonant converter with split-capacitor 3L-NPC power stages. It focuses on its operation in a two-level mode with a 50% duty cycle, especially under conditions of medium frequency switching and extremely low turn-off currents. The paper conducts a comparative analysis of two static balancing strategies: one using the parallel balancing resistors for each IGCT, and another employing a single symmetrizing resistor across the two inner IGCTs. These methods are assessed in terms of performance and losses. Additionally, it investigates how the symmetrizing resistor influences the commutation process behavior under these specific conditions. Experimental results are provided to validate the effectiveness and trade-offs of each approach.

1 Introduction

Developing high-power, medium-voltage (MV) converters presents several challenges, such as ensuring their safe and reliable operation, integrating high-voltage devices, and operating at medium frequencies. Notably, the advancement of the MV DC-DC converter design has become a focus area due to significant academic and industrial efforts, positioning it as a key enabling technology for advanced MVDC systems.

In this context, several works have been focused on developing high-power MV DC-DC converters over the years. For instance, in [1], an IGCT-based 3 MW, 600 Hz, 10 kV : 10 kV, dual active bridge (DAB) was developed. In that work, the prototype was successfully demonstrated featuring soft commutation with a turn-off current of 92 A. Another work has developed an IGCT-based 5.6 MW, 1 kHz, 5 kV : 5 kV, 3-phase DAB, where the converter's operation was tested to refine control strategies [2]. These examples highlight the success of developing DC-DC converter prototypes at the MW and MV levels. However, aiming for higher switching frequencies and lower turn-off currents, enabled by resonant operation, brings additional challenges, including the design of snubber circuits.

Other works have been investigating the development of a high-power MV LLC resonant converter, taking advantage of its intrinsic load-independent behavior, and high conversion efficiency. This converter is often referred to as a DC transformer (DCT) as an analogy to the AC transformer when operating in an open loop. In [3], and [4], the authors explored and presented the design principles, and in [5] the operation characteristics were assessed. In summary, the challenges of building high-power MV DC-DC converters come down to the design using existing technologies and costs.

In this work, an IGCT-based 1 MW, 5 kHz, 10(5) kV : 5 kV DCT is investigated. Fig. 1 shows a simplified schematic of the converter which consists of a a split-capacitor three-level (3L) NPC LLC resonant converter. The 3L operation plays a crucial role in protecting the DCT, providing soft-start and current-limiting capabilities [6]. Nevertheless, under normal operating conditions, the power stage operates in a two-level (2L) mode, with a 50% duty cycle, as shown in Fig. 1. In this case, the two upper and two lower IGCTs are effectively in series. Consequently, it is crucial to ensure both dynamic and static balancing in this configuration.

Numerous works have previously investigated the

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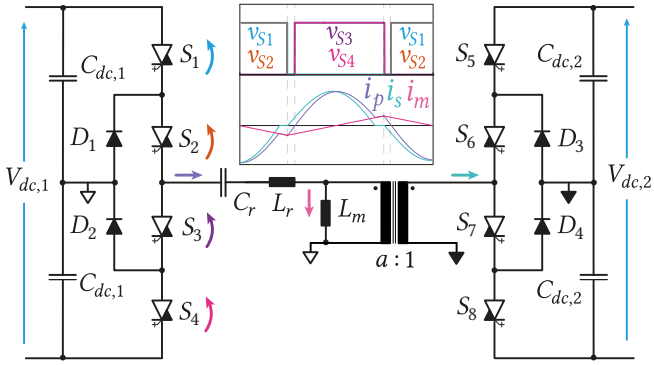


Fig. 1: 3L-NPC leg power stage of an LLC resonant converter and an illustration of the typical voltages and current waveforms for the 2L, 50% duty cycle operation.

static and dynamic voltage balancing in series-connected IGCTs [7]–[9]. These works mainly focus on hard-switched applications, which are typical in MV drives [7], [10]. Only recently there has been a shift towards investigating it in soft-switching applications, as explored in [5].

In [5], an evaluation was conducted on the resonant operation of series-connected IGCTs. That analysis highlighted the effectiveness of a low capacitance C-snubber connected in parallel - for the dynamic voltage balancing - in contrast to the conventional RCD snubber typically used in hard-switching scenarios. This simplification is primarily attributed to the soft-switching conditions (ZVS and QZCS), which reduce the energies involved during commutation. Moreover, that work examined the switching dynamics of the IGCTs under low turn-off currents scenarios (as low as 50 A) and used a parallel resistor approach for static voltage balancing.

Nevertheless, unlike the work described in [5], this study incorporates the IGCT stack within a 3L-NPC leg power stage. This setup is used in conjunction with the 1 MW medium frequency transformer (MFT) developed in [11]. The focus of the analysis is on evaluating the power stage performance with an ultra-low turn-off current of approximately 6 A, defined by magnetizing inductance of the MFT at 5 kHz operating frequency. The assessment includes tests to validate dynamic voltage balancing using the C-snubber, as well as examining the static voltage balancing.

The main contributions of this work are as follows: i) it presents a comparative assessment of two static voltage balancing strategies - parallel resistors and symmetrizing resistor; ii) it demonstrates the no-load operation of a 3L-NPC in a 2L mode for a 5 kV, 5 kHz IGCT-based DCT prototype, featuring an ultra-low turn-off current condition; and iii) it demonstrates the effective use of the symmetrizing resistor in a soft-switched 2L-operated 3L-NPC, exploring its impact on switching transients in conjunction with a low C-snubber value is used for the dynamic voltage balancing.

The paper is organized as follows: In Section II, the developed MV DCT prototype is described; Section III delves into the designs of the static voltage balancing, focusing on the parallel resistor and the symmetrizing resistor strategies, with experimental verification; Section IV presents the evaluation of the dynamic impact of the symmetrizing impact of the switches transient; and Section V, concludes this article.

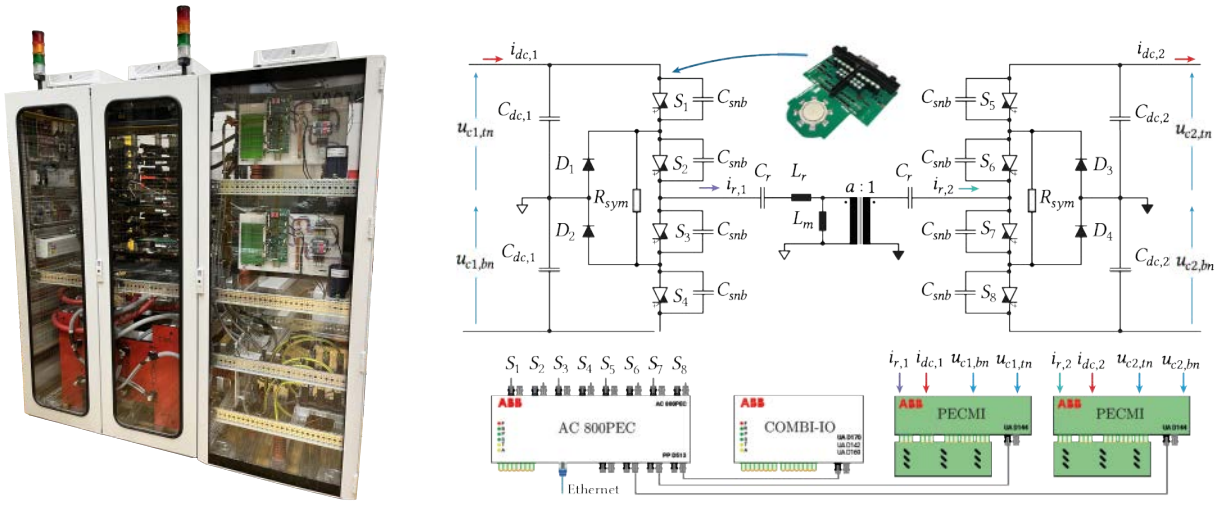
2 MV DCT prototype

The MV DCT prototype consists of a 10(5) kV : 5 kV split-capacitor 3L-NPC LLC resonant converter. In this work, only the 1:1 turns ratio configuration is investigated. The power stages operate with 4.5 kV RC-IGCTs (5SGX1445H0001), and the NP clamping diodes (5SDF0545F0001).

Fig. 2a shows the MV DCT prototype. The entire converter is fitted inside a cabinet (200 x 180 x 80 cm), excluding the deionized water cooling unit, which is externally situated and connected to the laboratory's water supply system. The integration inside the cabinet has not been optimized towards any power density-driven considerations, but only for easy of access to relevant parts. Table 1 shows the main parameters of the DCT.

The RC-IGCTs are controlled by the ABB's AC800PEC controller. Additionally, the system incorporates ABB's COMBI-IO for interfacing with different peripheral devices and ABB's PEC-MI to connect with voltage and current sensors. Fig. 2b shows the schematic of the prototype.

The MFT prototype was built with a nanocrystalline air-cooled core and hollow copper oil-insulated water-cooled windings [11]. Therefore, this prototype serves as a research platform for this study.

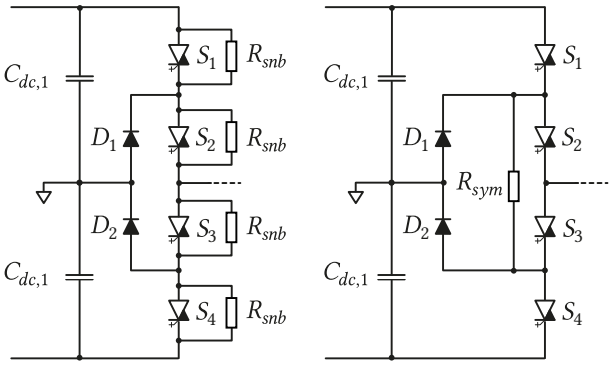


(a) (b)

Fig. 2: (a) Photo of the MV DCT prototype. (b) Schematic of the MV DCT, illustrated using the symmetrizing resistor for static voltage and a single C-snubber for dynamic voltage balancing.

Tab. 1: General information about the MV DCT

Description	Symbol (Unit)	Value
Rated power	P_n (MW)	1
DC Voltage 1	$V_\mathrm{dc,1}$ (kV)	10(5)
DC Voltage 2	$V_\mathrm{dc,2}$ (kV)	5
DC-link capacitance 1	$C_{dc,1}$ (μF)	400
DC-link capacitance 2	$C_{dc,2}$ (mF)	2.6
Leakage ind. (2:1)	L_r (μH)	42.86
Leakage ind. (1:1)	L_r (μH)	11.1
Magnetizing ind.	L_m (mH)	10.7
Resonant capacitor	C_r (μF)	61
Operating frequency	f_s (kHz)	5



(a) (b)

Fig. 3: (a) Schematic of the parallel resistor snubber. (b) Schematic of the 3L-NPC symmetrizing resistor snubber.

While the snubbers examined here are customized to meet these particular specifications, their design can be adapted for other applications.

3 Static Voltage Balancing

Unlike IGBTs that can benefit from active voltage balancing, series-connected RC-IGCTs depend on additional snubbers and balancing resistors for effective dynamic and static voltage balancing. Particularly, for static voltage balancing, the snubber is designed to ensure the switches operate safely during blocking periods.

Two known methods for static voltage balancing are evaluated, shown in Fig. 3. The first one, shown in Fig. 3a, uses the resistors in parallel with each power switch. This approach is both effective and straightforward for addressing the issue. However, it requires an individual resistor for each device, leading to increased power losses.

The second method, shown in Fig. 3b, uses a single resistor in parallel to the inner two IGCTs of the NPC-leg, solving the static voltage balancing with only one resistor, benefiting from the lower losses, as demonstrated next.

3.1 Parallel resistor

The static voltage balancing resistors ensure voltage balance across the series-connected devices

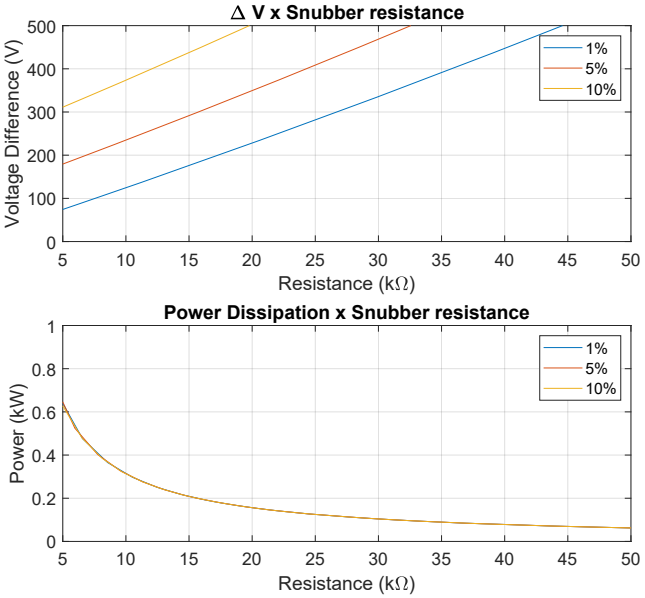


Fig. 4: Plots for the parallel resistor design. On top the expected/allowed voltage unbalance is shown and below the total corresponding power dissipation of the selected resistor is given.

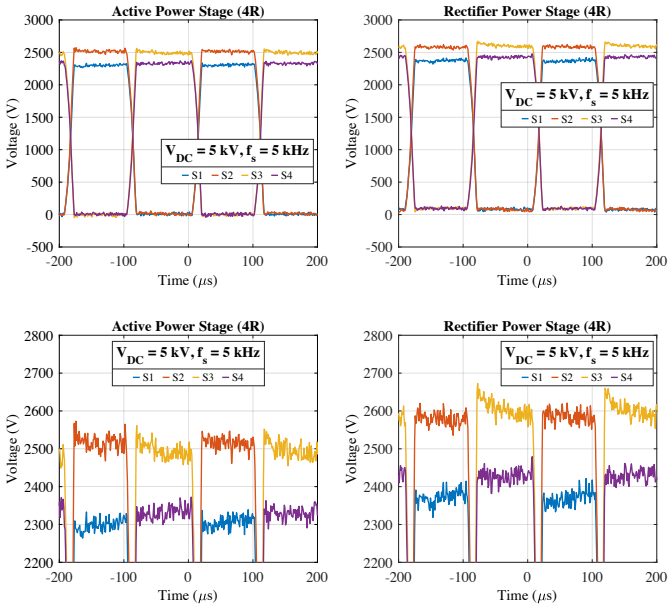


Fig. 5: Experimental waveform of the voltage across the IGCTs for the active and passive stack for the 5 kV and 5 kHz no-load operation with parallel resistor snubber.

by conducting a current greater than the maximum leakage current of these devices. Specifically, the resistors are required to carry a current that exceeds the leakage current of the RC-IGCTs when they are in the OFF state.

A sizing rule for these resistors was derived in [12], where the resistor value is sized considering the allowed voltage difference between the series connected devices, and the resistance tolerance of the resistors. This sizing rule leads to the following relationship:

$$\Delta V = \frac{V_{op} + \Delta V}{R_{snb} + \Delta R}\Delta R + I'_{leak,0}(R_{snb} + \Delta R) \quad (1)$$

where $I'_{leak,0}$ is the maximum leakage current of the devices at the operating voltage V_{op}, R_{snb} and ΔR are the values of the balancing resistor and its tolerance ($1\% \rightarrow \Delta R = R \times 0.01$), and ΔV is the maximum voltage deviation between the series connected devices. In order to correlate the leakage current with the actual operating voltage, the leakage current is,

$$I'_{leak,0} = \hat{I}_{leak,0}\sqrt{\frac{\frac{V_{op}}{n} + \frac{\Delta V}{n-1}}{V_{IGCT,0}}} \quad (2)$$

where $\hat{I}_{leak,0}$ is the maximum leakage current of the device, n is the number of series connected devices, and $V_{IGCT,0}$ is the reference voltage of the IGCT test.

Thus, this equation can be solved and the relationship between the allowed voltage deviation and the resistance value is drawn. Fig. 4 shows the resistance value versus the voltage deviation for different tolerances. At the bottom of Fig. 4, the power dissipation is shown.

From this plot, a resistor can be selected to maintain the difference between the voltages of the IGCTs below 10% of the DC-link voltage. ($\Delta V = 500$ V for the $V_{DC} = 5$ kV DC-link). Thus, resistors of $R_{snb} = 10$ kΩ can be selected with a 5% tolerance, expecting a voltage difference of $\Delta V \approx 240$ V for the demonstration in this prototype. In total, this selection leads to $P_{snb} = 4 \times 320$ W $= 1280$ W in power losses per stack.

These resistors were tested with the MV DCT prototype. The experiment was carried out by operating the DCT with the 5 kV input voltage, in a $1:1$ turns ratio configuration. The primary power stage is active with a 50% duty cycle, secondary power stage is a passive rectifier with no load. The dead time was set to $\delta = 30$ μs (mainly due to a very low turn-off current) and a C-snubber of $C_{snb} = 20$ nF was used for dynamic voltage balancing.

Fig. 5 shows the experimental waveforms for the balancing resistors, with $R_{snb} = 10$ kΩ. With this selection, a total of $P_{snb,tot} = 2 \times 1280 = 2560$ W is dissipated for the static voltage balancing, considering both stacks. This power dissipation represents 0.256% of the nominal power (1 MW).

3.2 NPC symmetrizing resistor

Taking advantage of the NPC-leg, which has the NP clamping diodes between the devices and the neutral point, a single symmetrizing resistor can be used for static voltage balancing. The resistor is positioned in parallel to the inner two IGCTs of the NPC-leg, as shown in Fig. 3b. This solution is broadly used in industrial high-power 3L-NPC inverters [13]–[17].

Differently from the simple parallel resistor strategy, which is often designed for the maximum leakage current of the device, the symmetrizing resistor needs to compensate only for the difference in leakage currents of devices. Fig. 6a illustrates the role of the clamping diode on the static voltage balancing, and Fig. 6b illustrates the role of the symmetrizing resistor.

Firstly, Fig. 6a shows an illustration when S_1 and S_2 are blocking, and the device S_2 has a higher leakage current. In this case, the voltage on S_2 will decrease and forward bias the NP clamping diode D_1, preventing the voltage of S_1 from reaching a destructive level outside of the safe operating area (SOA). Consequently, the upper NP diode provides a current path to compensate for the leakage current, and voltage S_2 is clamped to the capacitor voltage $C_{dc,2}$, approximately $V_{dc}/2$. The symmetrizing resistor is not needed in this particular scenario.

On the other hand, Fig. 6b shows the case when the device S_1 has a higher leakage current. In this case, the voltage of S_1 will decrease, while the voltage of S_2 increases. Thus, the NP diode is reverse-biased and cannot offer protection as in the previous case. Yet, this time, the symmetrizing resistor provides the current path to compensate for the leakage current, preventing voltage across S_2 from reaching destructive voltage levels.

In other words, the symmetrizing resistor compensates for the leakage current by draining extra current from S_2 to match the S_1 leakage current ($I_{leak,1} \approx I_{leak,2} + I_{Rsym}$). Hence, R_{sym} handles the difference between leakage current mismatch.

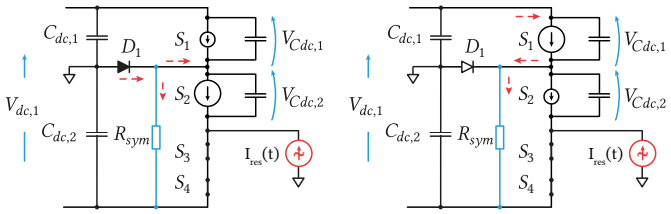


Fig. 6: (a) An illustrative example of the clamping diode acting when S_2 has a higher leakage current. (b) Example of the basic principles of the static voltage balance with an NPC symmetrizing resistor.

The current of the symmetrizing resistor should be big enough to properly compensate for the higher leakage current value of S_1. However, if the compensation is too big, the NP diode is forward biased again, and the scenario of Fig. 6a is repeated.

Consequently, following immediately this case, a simple design rule of this resistor can be derived considering the output capacitance rate of discharge and the current divider between the symmetrizing resistor and the equivalent resistance of the switch in parallel, resulting in:

$$\Delta V = \frac{R_{sym}}{R_{sym} + R_{leak,S_2}} I_{leak} \frac{T_{bk}}{C_{out}} \tag{3}$$

where ΔV is the voltage difference between both series-connected IGCTs, R_{leak,S_2} is the equivalent resistance of the switch S_2 (which is the switch in parallel with the R_{sym} for the $-V_{dc}/2$ state - similar rule can be derived with $V_{dc}/2$ and S_3), I_{leak} is the leakage surplus current of the switch S_1, C_{out} is the output capacitance of the device, and T_{bk} is the actual blocking period considering dead time of the devices, which is half of the switching period minus dead time (considering the 2L operation of the resonant converter operating principles.)

Thus, (3) relates the voltage difference between the devices and the resistance value of the symmetrizing resistance, which is affected by the capacitance value in parallel with the device. This capacitance value impacts the rate of change to discharge the

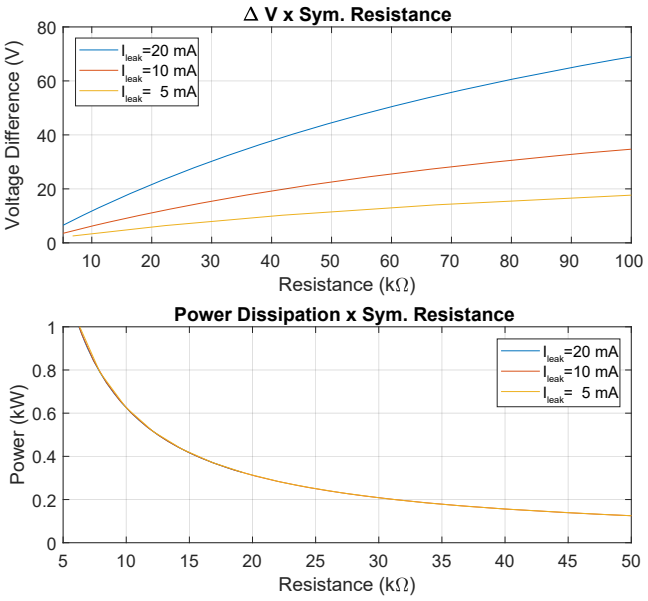


Fig. 7: Plots for the symmetrizing resistor design. On top, the maximum expected/allowed voltage unbalance during the blocking stage and below the total correspondent power dissipation of the selected resistor.

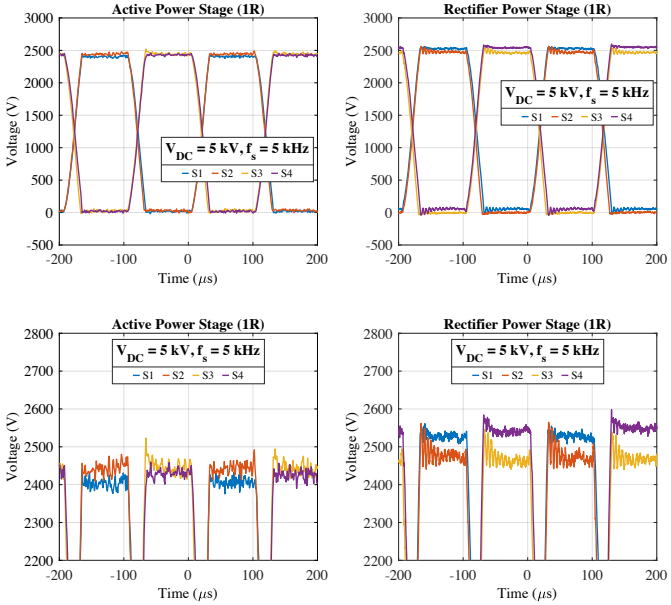


Fig. 8: Experimental waveform of the voltage across the IGCTs for the active and passive stack for the 5 kV and 5 kHz no-load operation with symmetrizing resistor snubber.

voltage with the leakage current. In (3), the capacitance is written as C_{out}, being the output capacitance of the device; however, if a snubber is included, it should be also considered for proper calculation.

Fig. 7 shows the design of the symmetrizing resistor using (3). At the bottom of Fig. 7, the power dissipation is shown for the symmetrizing resistor. This plot represents the maximum voltage deviation expected during the blocking state. The specifications of the MV DCT prototype were used for this simulation, where a switching frequency of $f_s = 5$ kHz has a switching period of $T_s = 200$ μs; hence, half a period is $T_{s,half} = 100$ μs, and with a dead time of $\delta = 30$ μs, the effective blocking period is $T_{bk} = 70$ μs. The considered C-snubber value is $C_{out} = 20$ nF. Thus, three scenarios of exceeding current of S_1, $I_{leak} = 5$ mA, $I_{leak} = 10$ mA, and the most extreme case $I_{leak} = 20$ mA, were simulated to evaluate their effect on the maximum voltage deviation.

Based on this plot, one should choose the considered worst case for designing the symmetrizing resistor. For instance, if a surplus current of $I_{leak} = 20$ mA is selected, this scenario assumes that only S_1 has leakage while S_2 is ideal. Consequently, the resistor can be chosen based on the blue curve. Alternatively, if it is assumed that the switches have similar characteristics and the surplus current is lower, opting for a higher resistor can reduce losses. It's worth noting that the C-snubber value and the blocking time influence this curve, and similar conclusions can be drawn for different sets of parameters.

Therefore, using Fig. 7, a conservative resistance value is chosen to be $R_{sym} = 20$ kΩ, for the purpose of demonstration, resulting in a power consumption of $P_{Rsym} = 320$ W per stack.

Fig. 8 shows the experimental results using the symmetrizing resistor. The total power consumption, considering both stacks is $P_{snb,tot} = 2 \times 320 = 640$ W, which represents 0.064% of the nominal power. Although the power consumption of this snubber is already much lower than the other strategy, this experiment shows that the resistance value could increase even further to reduce the losses and allow a higher voltage difference between the IGCTs.

Purely analyzing the voltage static balancing, the symmetrizing resistor is a better solution regarding performance and losses. The two solutions are compared and Tab. 2 shows the side-by-side comparison. The slightly higher values for the passive stack result from a higher DC voltage at its terminals.

Tab. 2: Comparison between R_{sym} and R_{snb}.

	Sym-R	Parallel-R
Losses per stack	340 W	1260 W
ΔV of Active stack	41 V	182 V
ΔV of Passive stack	76 V	219 V

4 Dynamic impact of the R_{sym} on the switching transients

During the 2L operation, the symmetrizing resistor is always exposed to $V_{dc}/2$, which leads to a continuous current flowing through the resistor, including during transient moments. In this sense, the current flowing through the resistor impacts the switch's transition. In general, this current is much lower than the turn-off current, which makes this effect negligible. Nevertheless, for the DCT operation, the turn-off current is already low, and with IGCT switches, this effect can be observed.

Fig. 9a shows an illustration of the impact of the symmetrizing resistor on the voltage rise time. In this example the switches $S1$ and $S2$ were conducting current and a command to turn OFF was triggered. At this moment, the dynamic behavior of the voltage across the switches can be approximated by the switches's output capacitance (including snubber if present), the two well-balanced split-capacitor DC-link as voltage sources, and a constant turn-off current during this short period.

During the voltage rise of S_1 and S_2, the R_{sym} current contributes to the total current charging the capacitor of S_1, consequently, leading to a faster transient compared to S_2. More importantly, the resistor's current returns from S_4, acting against its discharge, leading to a slower transient compared to S_3. Thus, this contribution leads to an increase in voltage imbalance.

Fig. 9b illustrates the opposite effect of the symmetrizing resistor on switches S_1 and S_4, during the complementary transition, now slowing down the discharge of S_1, and speeding up S_4.

From the simplified circuit, shown in Fig. 9a, one can notice that the impact of the R_{sym} depends on its resistance value which defines the current, the switch's equivalent output capacitance, and the turn-off current.

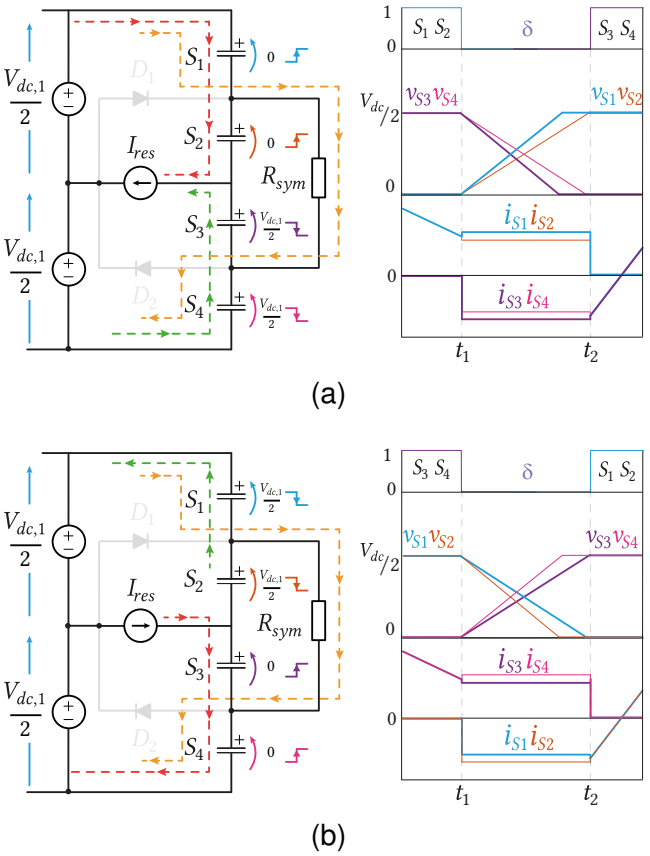


Fig. 9: Illustration with the impact of the NPC symmetrizing resistor on the switching transient, in (a) $V_{dc}/2 \rightarrow -V_{dc}/2$, and in (b) $-V_{dc}/2 \rightarrow V_{dc}/2$. The R_{sym} influences mainly the outer devices by reducing/increasing the turn-off current. During dead time, the full DC link voltage appears across $S_1 - R_{sym} - S_4$.

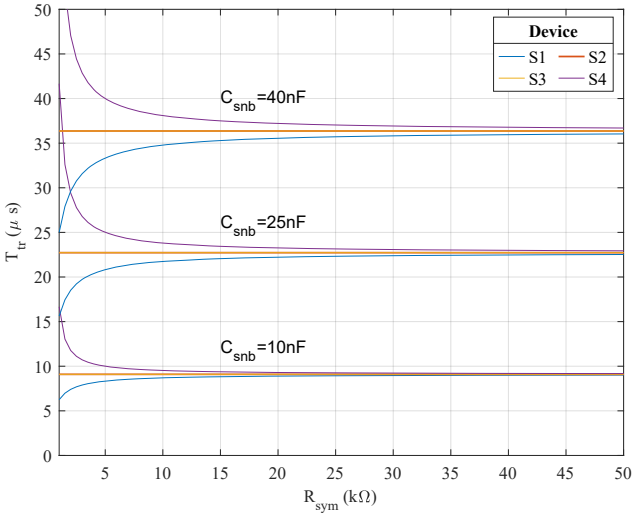


Fig. 10: Relationship between the transient response for the IGCTs and the symmetrizing resistor resistance for different snubber capacitances, considering $V_{dc} = 5$ kV, and $I_{off} = 5.5$ A, for the transition $V_{dc}/2 \rightarrow -V_{dc}/2$.

Thus, a simple equation can be derived to map its impact on the switches transients:

$$\begin{cases} i_{S1} = I_{off} \pm I_{Rsym} \\ i_{S2} = I_{off} \\ i_{S3} = I_{off} \\ i_{S4} = I_{off} \mp I_{Rsym} \end{cases} \quad (4)$$

where, $I_{Rsym} = V_{dc}/\left(2R_{sym}\right)$. The first sign represents the case with transition from high to low state ($V_{dc}/2 \rightarrow -V_{dc}/2$). Consequently, the period of the voltage transition is given by:

$$t_{tr,Sx} = \frac{C \cdot V_{dc} \cdot n}{2 \cdot i_{Sx}}, \quad (5)$$

where n is the number of series-connected devices, and i_{Sx} is the IGCT's turn off current from (4).

In this way, (5) estimate the voltage rise time, taking into consideration the R_{sym} contribution. Fig. 10 shows the transient duration of each IGCT depending on the R_{sym} resistance value, for three different capacitor snubbers, for a turn-off current of $I_{off} = 5.5$ A.

It can be seen in this plot, that for a C-snubber value of $C_{snb} = 25$ nF, and a resistor of $R_{sym} = 10$ kΩ, the switches S_2 and S_3 would take (theoretically, with the presented assumptions), approximately $t_{tr} \approx 22.73$ μs for the transition, while the switch S_1 would take $t_{tr} \approx 21.74$ μs, and finally the switch S_4 would take $t_{tr} \approx 23.81$ μs for the transition from $V_{dc}/2 \rightarrow -V_{dc}/2$. It means that switch S_3 will discharge approximately 1 μs faster than its pair (S_4), creating a voltage imbalance, and impacting the dynamic voltage balancing.

As expected, this effect is only strongly affected by low resistor values. However, these values are in the range of the required resistance to have a good compensation with low C-snubbers - which are required to allow fast voltage rise transient due to the low turn-off current. Ultimately, this is a trade-off involving the symmetrizing resistor value, the C-snubber, and the turn-off current.

To evaluate the waveforms of both stacks and the symmetrizing resistor waveforms at the same time, two Yokogawa DLM4058, 8-channel oscilloscopes were synchronized to capture the 16 waveforms at the same time. Four Cal Test Electronics CT4079-NA differential probes were used to capture the primary IGCTs voltage and the other voltages were recorded using GW Instek GDP-100 differential probe. The magnetizing current was recorded using the PEM CWT1 B/2.5/500 Rogowski coil, and the symmetrizing resistor current was recorded using the Keysight N2781B current probe.

Fig. 11 shows the complete no-load experiment showing the effect of the symmetrizing resistor on the voltage transient. The current on the symmetrizing resistor is around $I_{Rsym} \approx 0.2$ A, showing that the actual equivalent resistance value is $R_{sym} \approx 12.5$ kΩ, representing 3-5% of the turn-off current.

The total transition time is around $t_{tr} = 28$ μs. This extended duration can also be noted by visual inspection in Fig. 5 and Fig. 8, comparing the voltage shape of both strategies, where the total transition time for the parallel resistors is $t_{tr} < 20$ μs.

Furthermore, the voltage imbalance when the transient has finished while using the parallel resistor snubber is very similar to the imbalance present during the blocking state (approximately 200 V). This is a result of all the capacitors having the same current for discharging/charging. However, this is not the case for the symmetrizing resistor case, where the resistor's current contributes to increasing the voltage mismatch difference during this transient. The voltage imbalance when the first switch was completely discharged was around 290 V for the active power stage and approximately 380 V at the passive power stage.

Ultimately, this experiment showed that under these conditions, the symmetrizing resistor performed successfully the static voltage balancing, but also influenced the dynamic voltage balancing, slowing it down and increasing the voltage imbalance. Such conditions lead to the requirement for a dead time $\delta \geq 30$ μs to ensure a safe transition - representing 15% of the switching period, which is not ideal for the converter's operation.

5 Conclusion

This work detailed the challenges of operating an IGCT-based split capacitor 3L-NPC DCT at 5 kV and 5 kHz, under ultra-low turn-off current conditions. It focused on the snubber design for static

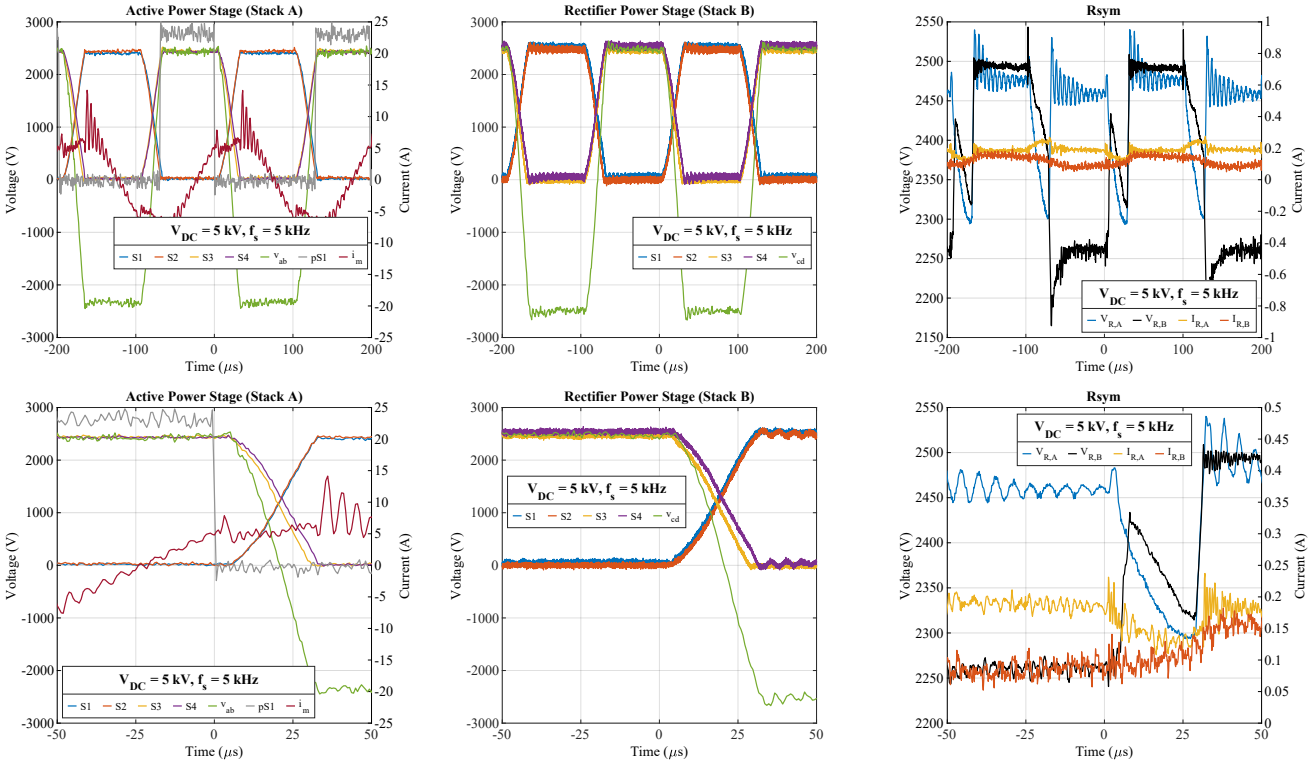


Fig. 11: Experimental waveforms for 5 kV and 5 kHz test with the voltage across the IGCTs, the voltages at the MFT terminals, the voltage across the symmetrizing resistors and their current, and the magnetizing current. The dead time was set to 30 μs and a C-snubber of 20 nF was used for the dynamic voltage balancing. The turn-off current is around $I_{off} = 5.5$ A. The total transition time is around $t_{tr} = 28$ μs.

voltage balancing, evaluating two strategies: the parallel resistor and the symmetrizing resistor.

The investigation has shown that the symmetrizing resistor snubber is as effective as the parallel resistors snubber, offering the advantage of using a single resistor compared to four in the alternative solution. Consequently, it successfully achieves static voltage balancing with lower losses.

On the downside, the symmetrizing resistor affects the voltage rise transient of the switches, which increases the dynamic voltage imbalance of the series-connected IGCTs. This effect is more critical when operating with ultra-low turn-off currents, as demonstrated with the MV DCT prototype. Nevertheless, this effect can be mitigated by using a higher resistance value and adjusting the dead time accordingly to allow safe commutation.

Consequently, additional trade-offs are required to allow the 5 kHz operation of the 3L-NPC DCT with the symmetrizing resistor such as reducing even further the C-snubber or increasing the turn-off current by adjusting the magnetizing inductance. Also, further improvements on the dynamic impact evaluation of the symmetrizing resistor could be done by assessing its impact on the 3L operation and by calculating the actual turn-off current of the IGCTs including parasite resistances and device voltage drops.

Finally, due to ongoing work in integration and commissioning, we have only included preliminary results. Comprehensive tests at full power will be detailed in subsequent reports.

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