A 16-Channel 60μW Neural Synchrony Processor for Multi-Mode Phase-Locked Neurostimulation

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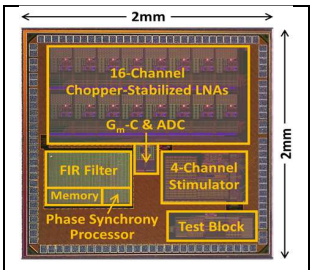
Measuring neural oscillatory synchrony facilitates our understanding of complex brain networks and the underlying pathological states. Altering the cross-regional synchrony—as a measure of brain network connectivity—via phase-locked deep brain stimulation (DBS) could provide a new therapeutic solution for various neurological [1] and psychiatric disorders [2]. This feature is missing in current neuromodulation devices and requires an accurate, energy-efficient computation of oscillatory phase and cross-regional synchrony on chip. The conventional iterative vector processing approach via CORDIC [3] can accurately extract the instantaneous phase and phase locking value (PLV) at the cost of high power consumption (400μW). As a result, it cannot be applied to large-scale (>100-CH) neuronal networks. Moreover, the latency in the pipelined CORDIC processor may hinder timely phase-locked stimulation in the absence of an excessively high clock speed. Alternatively, the PLV extractors in [4, 5] utilized simple approximation algorithms such as 1-bit quantization and local minima detection. These methods, albeit efficient, compromise PLV accuracy and cannot extract the instantaneous phase of neuronal signals. To provide an efficient, flexible, and accurate phase-locked DBS platform, this paper integrates a 16-channel low-noise AFE, an energy-efficient multi-mode phase synchrony processor, and a 4-channel neurostimulator that is locked to specific neuronal oscillatory phases (i.e., fixed or random phase, PLV or PAC). An amplitude-locked control can be further enabled through envelope and multi-band spectral energy extraction for common use cases such as epilepsy.

The SoC architecture is shown in Fig. 1. A 16-channel AFE performs low-noise conditioning of bipolar local field potentials (LFP) from two different brain regions. The 16 closed-loop chopper-stabilized LNAs followed by a shared G_m-C integrator and a 10b SAR ADC provide a good gain matching among channels, which is crucial for cross-regional biomarker extraction. Using a 16:1 multiplexer, the LNAs can be addressed in any user-defined order to allow flexible channel combinations for synchrony extraction. To save chip area, a programmable threefold FIR filter employs hardware sharing to decimate, bandpass filter (BPF), and Hilbert transform (HT) the recorded LFP signals. The BPF and HT outputs are sent to the phase synchrony processor that simultaneously extracts various neural biomarkers: instantaneous phase, amplitude envelope, PLV, phase-amplitude coupling (PAC), and spectral energy (SE). Phase locking is enabled by comparing selected biomarkers to thresholds, and the 4-channel charge-balanced stimulator is subsequently triggered.

Figure 2 presents the block diagram of the proposed lightweight phase extractor (LPE) that exploits trigonometric identities to reduce hardware complexity and overcome the power-accuracy-latency drawbacks of the conventional methods. Here, the range of complex inputs in the complex plane is identified and the inputs are confined to the [0, π/4) range. The fraction of real and imaginary components is calculated using a reciprocal LUT and a multiplier, to enable instantaneous phase approximation based on a first-order Lagrange interpolation. The resulting errors are compensated in a subsequent LUT, and the range is reconstructed to generate phase outputs in the [−π, π) range. The LPE provides 10b phase outputs normalized to [−1, 1). Figure 2 shows sub-LSB phase errors of LPE with respect to the ideal arctangent function ("atan2" in MATLAB), and the oscillatory phase of theta-band LFP measured *in-vivo* from a Long-Evans rat. For comparison, a last-bit accurate 10b unrolled CORDIC was implemented with bit-width optimization and input range reduction, similar to the LPE. The LPE achieves 30.1% and 52.4% improvements in area and power vs. CORDIC, respectively.

Building upon the proposed LPE, a phase synchrony extractor and a multi-mode phase-locked stimulation controller are implemented as depicted in Fig. 3. To improve hardware efficiency, an ℓ_∞-norm is employed to approximate the amplitude envelope in PAC/PLV, thus avoiding the use of complex Euclidean norms. Experimentally measured cross-regional PLV and PAC closely track the ideal software-based features, validating the accuracy of the proposed phase-amplitude approximators (Fig. 3). The phase synchrony processor consumes 9.69μW (including FIR) at a 0.85V supply for computing 8 PLV/PAC features, achieving >60.7% saving per feature compared to existing designs [3, 6]. To provide flexible stimulation control, the processor supports various stimulation modes by thresholding the per-sample feature (F_{SMP}, phase/amplitude @1kHz), windowed feature (F_{WIN}, PLV/PAC/SE @1-4Hz), or a combination of the two. Randomized phase locking can be further enabled using a 10b pseudo-random binary sequence (PRBS) threshold generator for synchrony disruption.



Die micrograph.

Figure 4 depicts the architecture of the 4-channel programmable neurostimulator (30-440μA). The output driver adopts a stacked H-bridge architecture with active and passive charge balancing (CB). AFE and stimulator measurement results are shown in Fig. 4. A low input-referred noise of 0.88μV_{rms} (including the ADC) was achieved in the 1-500Hz band, consuming 2.78μW/channel. The 16-channel gain matching (<0.1% mid-band) and gain programmability (53-61dB) were further demonstrated. For an intentional 50% mismatch in stimulation pulse width, the CB reduces the residual voltage to <±4mV through compensation currents and passive discharging.

Figure 5 demonstrates the 16-channel LFP recording and phase-locked stimulation in two modes, measured on three Long-Evans rats. Two custom electrode arrays (8 recording and 2 stimulation channels in each) were implanted into the infralimbic cortex (IL) and basolateral amygdala (BLA). The PSD of 16-channel input-referred LFP exhibits prominent 1/f-shaped spectra. Simultaneous recording using the SoC and a commercial device (Intan 32-ch headstage #C3314) verifies accurate measurement of LFP activity. To demonstrate the phase-locked stimulation capabilities of the SoC, stimulation was targeted at a specific phase (180°) of theta-band LFP (4-8Hz) that is known to correlate with fear- and anxiety-like behavior. Theta-band phase- and PLV-locked stimulation is further demonstrated. For both experiments, the maximum stimulation frequency was set to 6Hz, and the phase-locking detector was controlled such that phase wrapping did not trigger the stimulation.

Figure 6 shows SoC area and power breakdowns and comparison to the state-of-the-art phase synchrony processors. The 16-channel SoC occupies an area of 2.24mm^2 and consumes 60μW. To our knowledge, this work is the first SoC that integrates phase-locked stimulation while providing various stimulation modes in response to cross-regional phase- and amplitude-based neural biomarkers. This may be useful for treating a range of network-based disorders, including depression, anxiety, OCD, and movement disorders.

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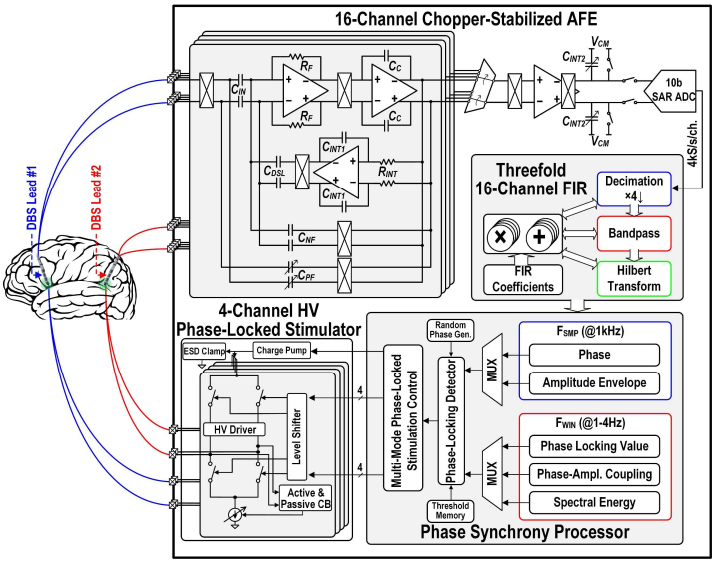


Fig. 1. Proposed 16-channel phase synchrony processor for multi-mode phase-locked neuromodulation.

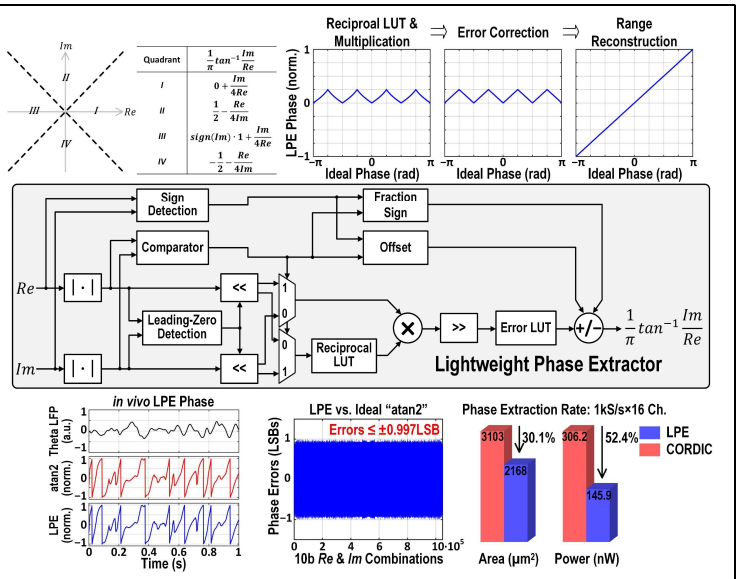


Fig. 2. Lightweight phase extraction (LPE) hardware and comparison to a CORDIC-based implementation.

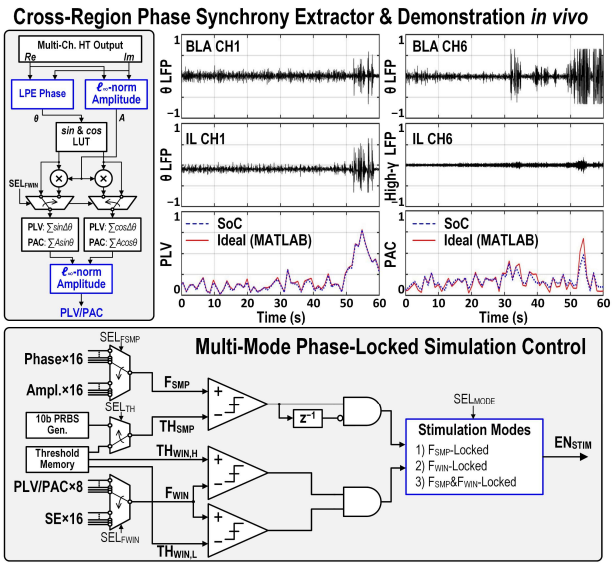


Fig. 3. Cross-regional phase synchrony extractor and multi-mode phase-locked stimulation control.

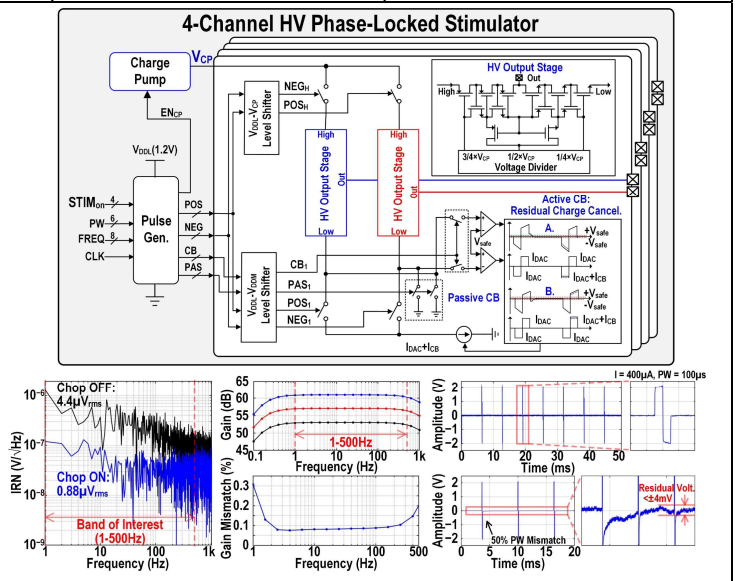


Fig. 4. Phase-locked high-voltage compliant stimulator architecture and measured AFE and stimulator performance.

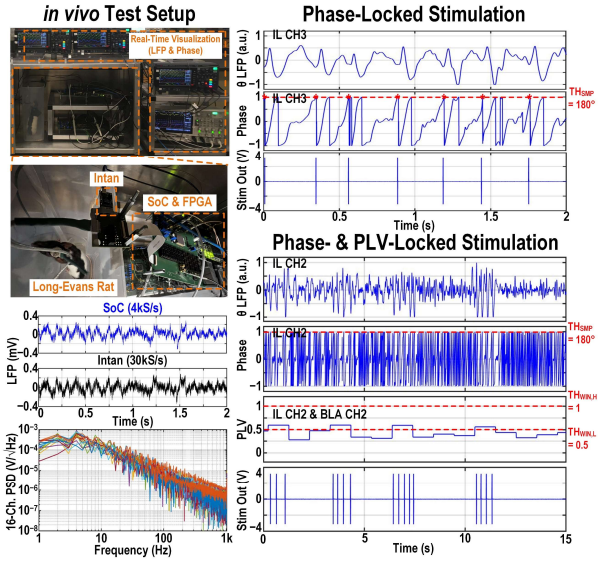
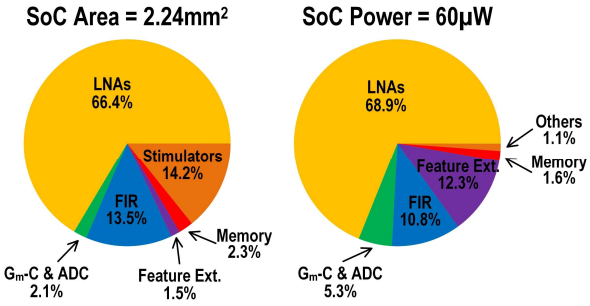


Fig. 5. Measured *in vivo* LFP recording and phase-locked stimulation on Long-Evans rats.



Comparison to the SoA Phase Synchrony Processors

Parameter	TBioCAS'19 [4]	JSSC'13 [3]	ISSCC'18 [6]	This Work
Process (nm)	180	130	130	65
Supply Voltage (V)	0.5	1.2	1.2	1.2/0.85
# Recording Ch.	-	64	32	16
# Stimulation Ch.	-	64	32	4
SoC Area/ch.† (mm²)	0.025‡	0.109*	0.237	0.14
SoC Power (μW)	0.015‡	1286*	674‡	60
PLV/PAC power (μW)	0.015 (1 PLV w/ min detect.)	400 (32 PLVs)	200.4 (65 CFC/PLVs)^	9.69 (8 PAC/PLVs)
Stimulation Modes	-	PLV thresholding	SVM Classification (PLV, CFC, SE)	Phase (fixed/random), Ampl., PLV, PAC, SE thresholding

† Estimated based on # of recording channels
* Estimated from breakdowns excluding TX
‡ Digital back-end only
^ Estimated # of feature extractions

Fig. 6. SoC area and power breakdowns and comparison to the state-of-the-art.

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