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***Abstract*—In two-stage solid-state transformers with input-series output-parallel structure, the LLC converter operating at a fixed switching frequency is a common choice for the isolated DC/DC conversion stage because it can provide a high efficiency and a fixed voltage gain. However, when applied in single-phase AC/DC conversion, the equivalent output current of the AC/DC converters contains a second harmonic current (SHC) at twice the grid frequency. The SHC causes increased ripple voltages and losses in LLC converters and should be minimized. This paper analyzes the propagation mechanism of SHC, especially the influence of both the primary and the secondary side DC link capacitors. A control method to eliminate the SHC is proposed. By adding an additional control loop, the switching frequency and voltage gain of the LLC converter are regulated dynamically to prevent the propagation of SHC. The effectiveness of the proposed control method is verified by simulations.**

***Index Terms*—solid-state transformer, LLC converter, second harmonic current, switching frequency control.**

I. Introduction

The solid-state transformer (SST) is an emerging technology that has potential in many fields, such as traction systems, renewable energy, data centers, and smart grids [1]–[5]. MVAC to LVDC conversion is one of the typical applications for SST. Due to the high input voltage, the input-series output-parallel (ISOP) structure is commonly adopted.

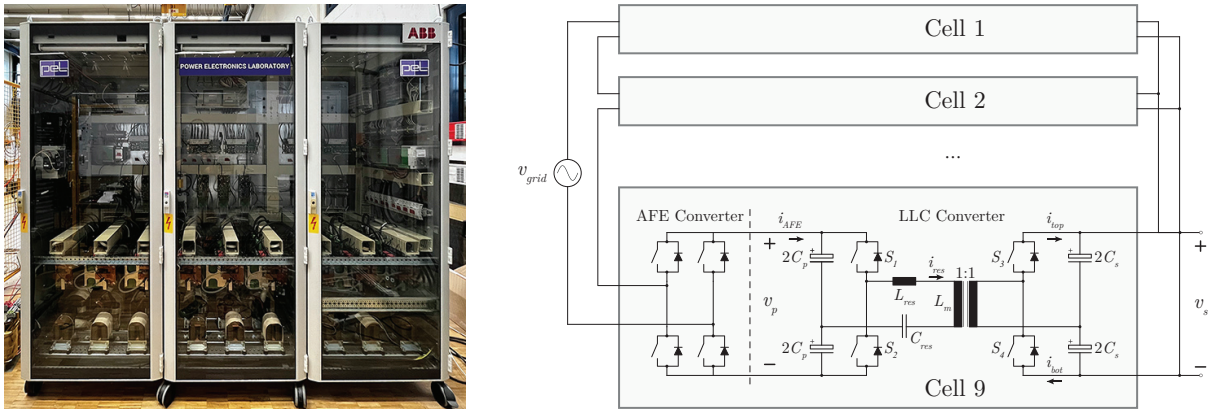
In two-stage ISOP SST, a DC/DC conversion stage that provides voltage matching and galvanic isolation is usually required. Open-loop modulated LLC converters, which operate at a fixed switching frequency that is slightly lower than the resonant frequency, can provide a load-independent voltage transfer characteristic and high conversion efficiency. These features make it suitable for the isolated DC/DC stage in SST [4]–[8]. In these applications, the LLC converter acts as a "DC transformer", often referred to as DCX, where the output voltage and power are regulated by other power stages.

For single-phase ISOP SSTs, the instantaneous power from the grid contains pulsating components at twice the grid frequency [9]. This means the equivalent output current of the AC/DC converters contains not only a DC current but also a second harmonic current (SHC). As the LLC converter operates at a fixed switching frequency and 50% duty cycle with a limited control degree of freedom, the SHC inevitably propagates to the secondary side through the LLC converter, which increases the current stress of devices and causes second harmonic ripple voltages on both the primary and secondary side DC links [10], [11].

The propagation of SHC in LLC converters has been discussed in the literature [7], [10]–[12], yet none of these analyses consider the coupling effect of DC link capacitors with the LLC converter. The equivalent dynamic model of LLC converters is established in [12] and has been applied to analyze the propagation of SHC in a three-phase SST [7]. However, the conclusion of these papers cannot be generalized to the single-phase scenario. The fluctuation of resonant current due to the SHC is discussed in [10], yet the impact of DC link capacitors is not considered. A SHC propagation model is proposed in [11]. However, this model relies on the measurement of a real converter.

Because the SHC in three-phase systems can be neutralized, various SHC suppression methods have been proposed [13]–[17]. Unfortunately, these methods are no longer valid in single-phase SSTs. The application of the active power decoupling method in single-phase SST is reported in [18], [19], but hardware modification to the SST is required in both cases. The variable frequency control of the LLC converter for SHC mitigation in a two-stage single-phase rectifier has been reported in [20]. However, this research focuses only on the control implementation, while a comprehensive analysis of this control method in terms of operating principle, parameter design, and potential benefits is still missing.

This paper first studies the behavior of SHC in LLC converters. A CLC equivalent circuit model is adopted to analyze the SHC distribution. The two operating modes of the LLC converter with different DC link capacitance are discussed. A closed-loop variable switching frequency control method of the LLC converter is proposed to prevent the propagation of the SHC to the secondary side. The principles and benefits of the proposed method are presented. The feasibility of the proposed method is verified by means of simulations using the parameters of the actual and redesigned prototype.



(a) (b)

Fig. 1. The LV PETT [4], analyzed here as an example of ISOP SST. a) prototype; b) topology.

II. The SHC in ISOP SST

The analysis of this paper is based on the low voltage power electronic traction transformer (LV PETT), which is shown in Fig. 1 and detailed described in [4]. As the LV PETT is a typical single-phase ISOP SST, the conclusion of this paper can be generalized to other similar applications.

The LV PETT contains nine cells connected in series at the AC input and in parallel at the DC output. Each cell is comprised of an H-bridge active front end (AFE) converter and an LLC converter. Since the cells are identical, the power flow is evenly distributed across the nine cells, and the SHC distribution in the SST can be simplified to the analysis of a single cell. By neglecting the losses and reactive power of the grid filter, the equivalent output current of the AFE converter i_{AFE} can be derived from the voltage v_{AC} and current i_{AC}:

$$\begin{aligned} i_{AFE} &= \frac{v_{AC} i_{AC}}{N V_P} = \frac{V_{AC} \sin(\omega_g t) I_{AC} \sin(\omega_g t - \phi)}{N V_P} \\ &= \frac{V_{AC} I_{AC}}{2 N V_P} (\cos\phi - \cos(2\omega_g t - \phi)) \\ &= I_{DC} + i_{SHC} \end{aligned} \tag{1}$$

where V_{AC} and I_{AC} represent the amplitude of v_{AC} and i_{AC}. N is the number of series-connected SST cells. As the cells are connected in series at the AC input, the grid voltage is equally shared, while the grid current is the same for all cells. ϕ is the phase angle between v_{AC} and i_{AC}. ω_g is the angular frequency of the grid. V_P is the average primary side DC link voltage.

Equation (1) shows that i_{AFE} is composed of a DC component I_{DC} and the SHC i_{SHC}, respectively expressed as:

$$\begin{aligned} I_{DC} &= \frac{V_{AC} I_{AC}}{2 N V_P} \cos\phi \\ i_{SHC} &= \frac{V_{AC} I_{AC}}{2 N V_P} \cos(2\omega_g t - \phi) \end{aligned} \tag{2}$$

For simplicity, a unity power factor where $\phi = 0$ is considered in the rest of the paper, and the amplitude of SHC I_{SHC} is equal to I_{DC}.

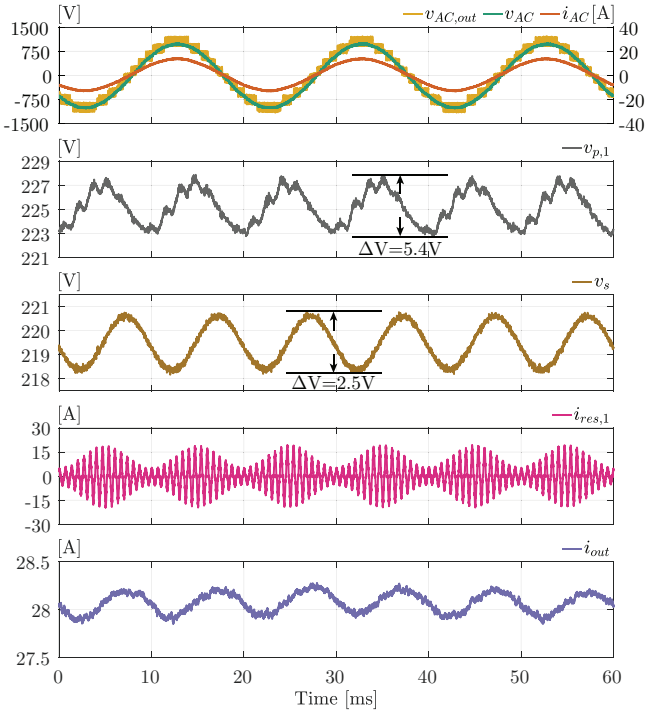


Fig. 2. Nominal operating waveform of the LV PETT at 6kW without any ripple voltage mitigation methods.

Fig. 2 shows the experimental waveform of the LV PETT at 6kW without any SHC suppression methods, which is an example of the impact of SHC on ISOP SST. The ripple voltage at 100Hz is clearly visible in the primary side DC link voltage of Cell 1 $v_{p,1}$ and secondary side DC link voltage v_s with respective values shown on the graphs. In addition, fluctuation at 100Hz can also be observed in the resonant current i_{res}, indicating the SHC propagation through the LLC converter. The experimental results are collected at a relatively low operating power due to the limitation of the power supply at the time of preparation of the paper.

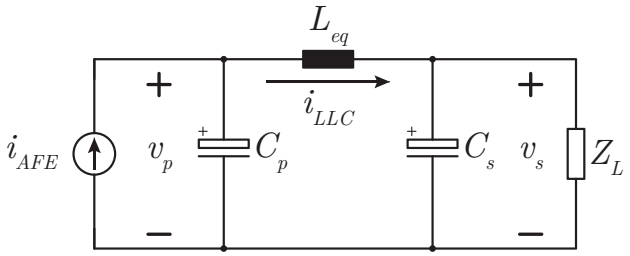


Fig. 3. The equivalent circuit of the SST cell using CLC equivalent model of the LLC converter.

III. The SHC Distribution in LLC Converters

Under normal conditions, when the power is transferred from the AC grid to the DC load, only the primary side switches S_1 and S_2 of the LLC converter are switching, while S_3 and S_4 are turned off. The resonant current i_{res} is rectified by the anti-parallel diodes of S_3 and S_4, which are i_{top} and i_{bot}, respectively. i_{LLC} is the average value of i_{top} or i_{bot} in a switching cycle, which can be expressed as:

$$i_{LLC} = \bar{i}_{top} = \bar{i}_{bot} = I_{DC,LLC} + i_{SHC,LLC} \tag{3}$$

In the CLC model, i_{LLC} is the equivalent current that flows through the LLC converter. Similar to i_{AFE}, i_{LLC} is also composed of a DC current $I_{DC,LLC}$ and the SHC $i_{SHC,LLC}$. When the losses are neglected, I_{DC} is equal to $I_{DC,LLC}$. However, i_{SHC} and $i_{SHC,LLC}$ are usually not equal.

According to the method proposed in [12], the LLC converter can be approximated by the equivalent inductance L_{eq}, which is derived using the averaged piecewise sinusoidal current [12] and can be written as:

$$L_{eq} = L_{res}\left(\frac{\pi f_{res}}{f_s}\right)^2 \tag{4}$$

where L_{res} is the resonant inductance. With this approximation, a single SST cell can be equivalent to a CLC circuit, which is shown in Fig. 3. The AFE converter is replaced by a current source i_{AFE}. Z_L represents the load impedance.

According to the CLC model, the relationship between $i_{SHC}(s)$ and $i_{SHC,LLC}(s)$ can be described by the following transfer function:

$$G_{SHC}(s) = \frac{i_{SHC,LLC}(s)}{i_{SHC}(s)} = \frac{1}{1 + \dfrac{sC_pZ_L}{1+sC_sZ_L} + s^2L_{eq}C_p} \tag{5}$$

It can be seen that the distribution of the SHC between the primary and secondary sides is mainly determined by the relationship between C_p, C_s, and L_{eq}.

TABLE I
Parameters of each LLC converter in LV PETT

DC Voltage V_{DC}	220V	Load Impedance Z_L	50Ω
Resonant Ind. L_{res}	135μH	Resonant Cap. C_{res}	60μF
Magnetizing Ind. L_m	13mH	Turns Ratio n	1
Switching Freq. f_{sw}	1500Hz	Resonant Freq. f_{res}	1768Hz
DC Cap. C_p, C_s	1-4mF	Equivalent Ind. L_{eq}	1.85mH

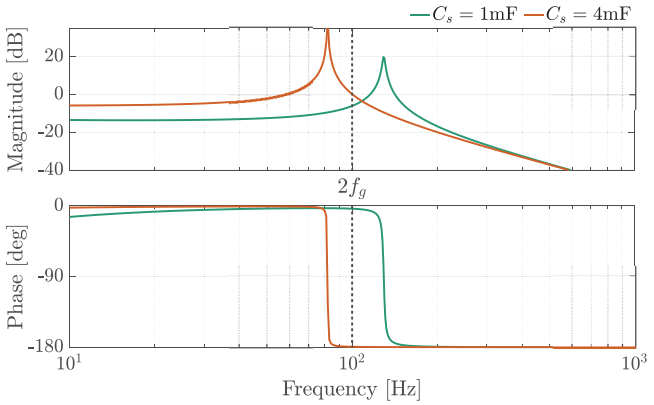


Fig. 4. Bode plot of the transfer function $G_{SHC}(s)$, with different C_s.

The LLC converter analyzed in this paper adopted the parameter from the LV PETT, which is given in Table I. Fig. 4 shows the bode plot of $G_{SHC}(s)$ with $C_p = 4$mF but different C_s. With $C_s = 1$mF, the phase delay of $G_{SHC}(s)$ at twice the grid frequency (100Hz) is almost zero. This condition is further referred to as the In-Phase Mode (IPM) of the LLC converter because $i_{SHC,LLC}$ and i_{SHC} are in phase with one another. In this case, the SHC from the grid is buffered by both C_p and C_s. On the contrary, with $C_s = 4$mF, the phase delay of $G_{SHC}(s)$ at 100Hz is approximately 180°. As $i_{SHC,LLC}$ and i_{SHC} are in anti-phase, this scenario is referred to as the Anti-Phase Mode (APM). In this case, C_p is not only buffering the SHC introduced by the AFE but also an additional SHC contribution generated by the resonance between C_s and L_{eq}.

In general, the propagation of SHC has a negative impact on the SST as it causes ripple in the output DC voltage of the SST. Furthermore, the SHC increases the current stress on the switching devices and magnetic components, reducing the overall efficiency of the SST. The variable frequency control method introduced in this paper aims to prevent the propagation of SHC and mitigate its negative influence. With different DC link capacitance, the LLC converter may operate in either IPM or APM. Due to the different SHC distribution in these two modes, the variable frequency control method has a different effect, and both cases will be introduced in the following chapters.

IV. The Variable Frequency Control Method to Eliminate SHC in LLC Converter

A. Operating Principle

According to the above analysis, the propagation of SHC in an open-loop modulated LLC converter is unavoidable. However, if the switching frequency, instead of being fixed, is regulated in response to the SHC, the propagation of SHC to the secondary side can be prevented or greatly mitigated.

Typically, variable frequency control limits the actual switching frequency between two values. The same is true in this work, but the operating range is defined differently, with

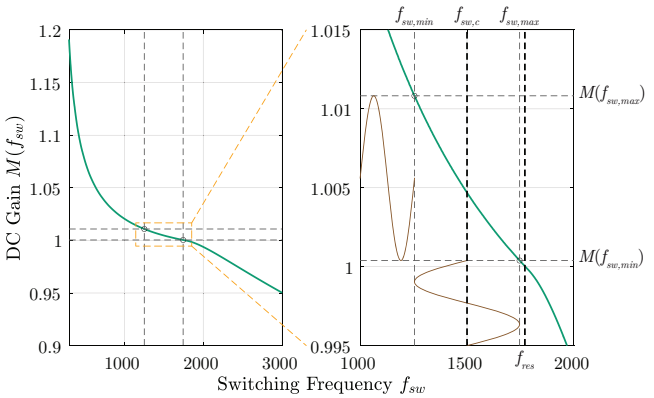


Fig. 5. The switching frequency and the corresponding voltage gain of LLC converters with variable frequency control. The parameter of the LLC converter is given in Table I, and the curves consider output power of 6kW.

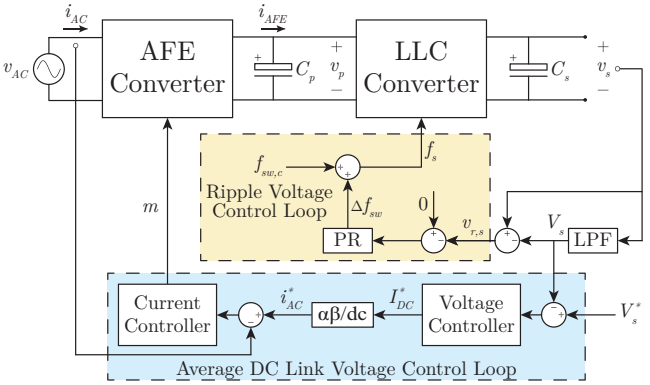


Fig. 6. Block diagram of proposed variable frequency control method based on PR controller.

a certain center frequency and frequency oscillation around it. In this case, the switching frequency of the LLC converter is expressed as:

$$f_{sw} = f_{sw,c} + \Delta f_{sw} \tag{6}$$

The frequency oscillation Δf_{sw} is generated by a closed-loop controller. The average secondary side DC link voltage V_s is regulated by the AFE converter of the SST, while the average primary side DC link voltage V_p is determined by $V_p = V_s/M\left(f_{sw,c}\right)$, where $M\left(f_{sw,c}\right)$ is the voltage gain of the LLC converter at $f_{sw,c}$. The addition of Δf_{sw} adjusts the voltage gain of the LLC converter within a half AC cycle, which further regulates the SHC distribution. In this configuration, the variable frequency control only acts on the ripple voltage, while the average DC gain of the LLC converter is fixed, which is beneficial to the stability of the SST.

When i_{SHC} is completely buffered by the primary side DC link capacitor, the primary side DC link voltage is:

$$v_p = V_P + \frac{V_{AC} I_{AC} \sin(2\omega_g t - \phi)}{4\omega_g N V_P C_p} \tag{7}$$

In this case, the second harmonic ripple voltage does not propagate to the secondary side, meaning that the secondary side voltage would be perfectly constant:

$$v_s = V_s \tag{8}$$

To achieve the desired relationship between v_p and v_s, the time varying f_{sw} should fulfill the following relationship:

$$M\left(f_{sw}\right) = \frac{v_s}{v_p} = \frac{V_s}{V_P + \dfrac{V_{AC} I_{AC} \sin(2\omega_g t - \phi)}{4\omega_g N V_P C_p}} \tag{9}$$

In a small interval close to $f_{sw,c}$, the relationship between the switching frequency and voltage gain of the LLC converter is approximately linear. As a result, the frequency oscillation Δf_{sw} is close to a sinusoidal term at twice the grid frequency. Fig. 5 presents the simulation result of the LLC converter where the variable frequency control has been applied to the SST, which demonstrates the principle of ripple voltage mitigation. The required switching frequency oscillation range and the corresponding voltage gain to suppress the ripple voltage are shown. The parameter of the LLC converter in this simulation is provided in Table I, and the SST operates with an output power of 6kW.

B. Control Implementation

The block diagram of the proposed variable frequency control method is presented in Fig. 6. The average secondary side DC link voltage V_s is regulated by the AFE converter and the DC link voltage controller of the SST. To eliminate the second harmonic ripple voltage on the secondary side DC link $v_{r,s}$, a closed-loop control method acting on $v_{r,s}$ is adopted.

Considering the controller needs to track a sinusoidal input at twice the grid frequency, a non-ideal proportional-resonant (PR) controller, synchronized to twice the grid frequency, is adopted to guarantee a zero steady-state error. To eliminate the ripple voltage, the reference signal of this controller is zero, while the output is the switching frequency oscillation Δf_{sw}. The switching frequency is generated by adding Δf_{sw} to the center frequency $f_{sw,c}$ and sent to the PWM generator of the LLC converters.

C. Parameters Design

With the proposed control method, the design of C_s does not need to consider the second harmonic ripple voltage, which usually leads to greatly reduced C_s. The design of C_p is still subject to the ripple voltage constraint. If the maximum allowed second harmonic ripple voltage on the primary side DC link $V_{rmax,p}$ is determined, the minimum required C_p can be calculated as:

$$C_{p,min} = \frac{V_{AC} I_{AC}}{2\omega_g N V_P V_{rmax,p}} \tag{10}$$

Considering the case where the voltage gain decreases monotonically with switching frequency, the minimum and

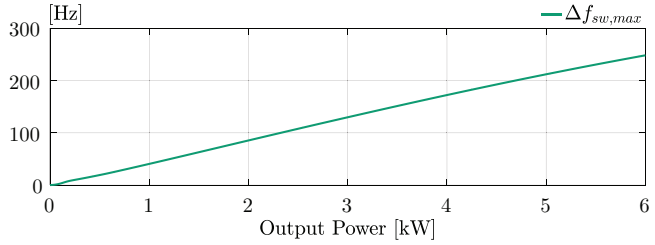


Fig. 7. Required frequency deviation $\Delta f_{sw,max}$ under different output power.

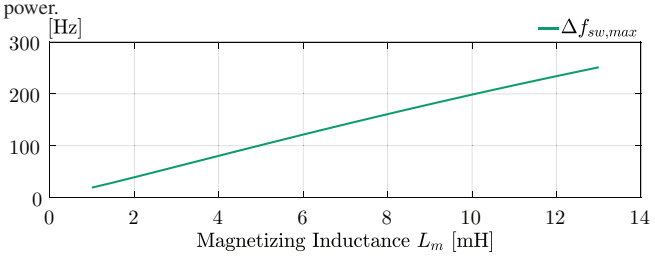


Fig. 8. Required frequency deviation $\Delta f_{sw,max}$ under different magnetizing inductance L_m. The output power is 6kW.

maximum switching frequency can be obtained by solving the following equations:

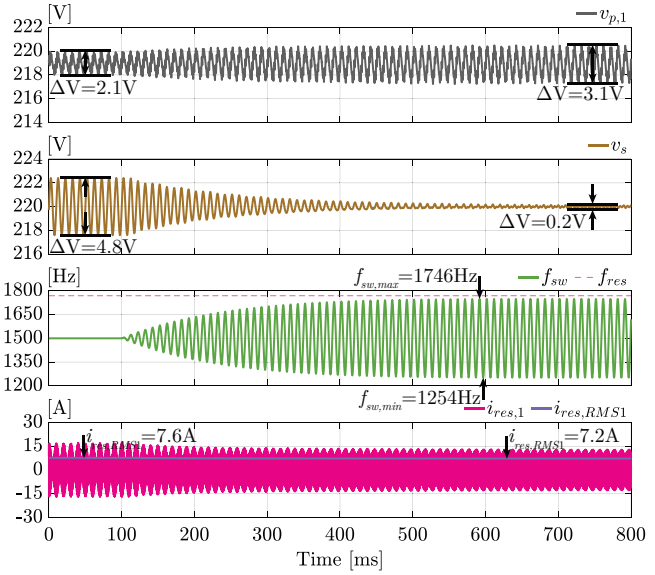
$$M\left(f_{sw,max}\right) = \frac{V_s}{V_p + V_{rmax,p}/2}$$
$$M\left(f_{sw,min}\right) = \frac{V_s}{V_p - V_{rmax,p}/2} \tag{11}$$

The sub-resonant operation, where the switching frequency is always lower than the resonant frequency f_{res}, should always be guaranteed as it is beneficial to reduce the switching losses. To keep $f_{sw,max}$ always below f_{res}, $f_{sw,c}$ should be low enough to provide enough margin between $f_{sw,c}$ and f_{res}. The maximum frequency deviation $\Delta f_{sw,max}$ is defined as:

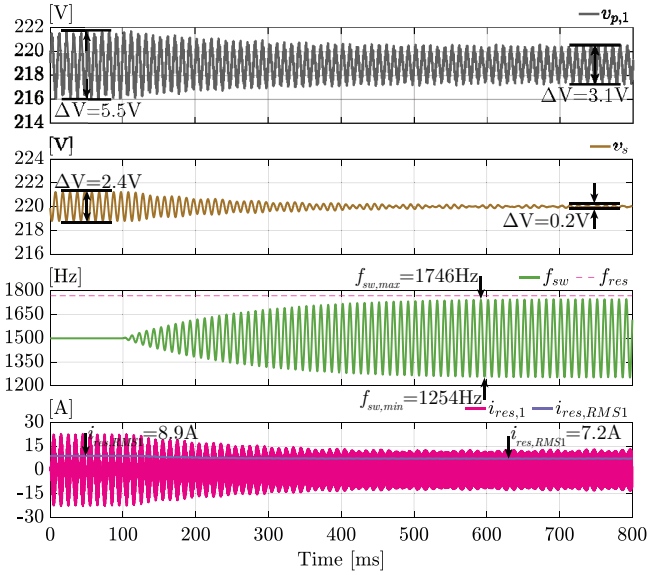
$$\Delta f_{sw,max} = f_{sw,max} - f_{sw,c} = f_{sw,c} - f_{sw,min} \tag{12}$$

For a certain SST design, $\Delta f_{sw,max}$ is related to the output power. The higher the output power, the higher the ripple voltage, and the higher $\Delta f_{sw,max}$ is required. On the other hand, the increased output power also changes the slope of the voltage gain curve, which further influences $\Delta f_{sw,max}$. Fig. 7 demonstrates the variation of $\Delta f_{sw,max}$ with output power, which considers both the two effects mentioned above. It can be seen that $\Delta f_{sw,max}$ increases linearly with the output power. Therefore, as long as $f_{sw,max} < f_{res}$ holds at the maximum output power, the sub-resonant operation can be guaranteed in the whole operating range.

If $\Delta f_{sw,max}$ is too big at the desired output power, the parameter design of the LLC converters should be adjusted to increase the slope of the voltage gain curve at $f_{sw,c}$. The slope of the voltage gain curve is mainly determined by the ratio between the magnetizing inductance L_m and resonant inductance L_{res}. In the case of a fixed L_{res}, the lower the L_m, the steeper the voltage gain curve, leading to reduced $\Delta f_{sw,max}$. Fig. 8 shows that $\Delta f_{sw,max}$ increases linearly with L_m. It is worth noting that reducing L_m reduces the required margin between f_{res} and $f_{sw,c}$ but also increases the sensitivity of the voltage gain against load fluctuation. At the same time, for sub-resonant operation, the value of L_m directly defines the turn-off current of the primary side switches, impacting the semiconductor losses. Therefore, the parameter design of L_m and $f_{sw,c}$ should consider not only the requirements of the ripple voltage control but also the performance of the entire SST.



(a)



(b)

Fig. 9. Simulation result of the SST with a) $C_s = 1$mF; b) $C_s = 4$mF. The proposed control method is enabled at $t = 100$ms.

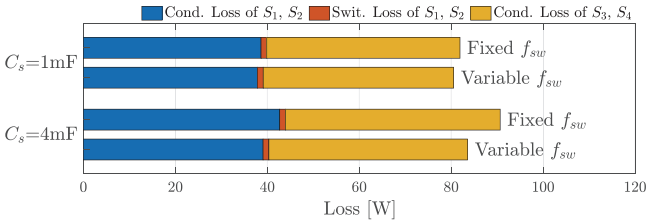


Fig. 10. Semiconductor losses of the LLC converters with and without the proposed variable frequency control method. The losses from the nine cells are added together. The output power of the SST is 6kW.

V. Simulation Results

The SST simulation model is developed in PLECS to verify the feasibility and benefits of the proposed variable frequency control method. This model adopts the topology and parameters of the LV PETT.

A. Original Resonant Tank Design

Fig. 9a shows the simulation waveform of the SST with the proposed variable frequency control method enabled at $t = 100$ms. Although the rated power of the LV PETT is 54kW, a low output power at 6kW is considered in this section. Because the SHC distribution in different cells is the same, only the waveforms of Cell 1 are provided. At the beginning, the LLC converters operate at a fixed 1500Hz switching frequency, and second harmonic ripple voltage can be observed in both the primary side DC link voltage of Cell 1 $v_{p,1}$ and the secondary side DC link voltage v_s. With $C_p = 4$mF and $C_s = 1$mF, the LLC converters operate in IPM where the SHC is buffered by both C_p and C_s.

At $t = 100$ms, the proposed control method is enabled, and a oscillation is added to the switching frequency of the LLC converters. The system reaches a new steady state in 500ms. As a result, the secondary side ripple voltage amplitude $V_{r,s}$ is reduced from 4.8V to 0.2V, indicating the SHC buffered by C_s is transferred to C_p. The primary side ripple voltage amplitude $V_{r,p1}$ is increased from 2.1V to 3.1V. In addition, the RMS value of the resonant current $i_{res,RMS1}$ is also reduced from 7.6A to 7.2A due to the removal of SHC.

If C_s is 4mF instead of 1mF, the LLC converters operate in APM where the resonance between C_s and L_{eq} introduces additional SHC. The simulation results for this situation are shown in Fig. 9b. With the variable frequency control activated at $t = 100$ms, $V_{r,s}$ reduces from 2.4V to 0.2V. $V_{r,p1}$ also reduces from 5.5V to 3.1V, because the additional SHC is eliminated and C_p only needs to buffer the SHC from the grid. $i_{res,RMS1}$ reduces from 8.9A to 7.2A.

According to the above analysis, the frequency oscillation range is only related to C_p and the output power. Therefore, although C_s is different in the two cases, the switching frequency oscillation range in the steady state is the same, which is between 1254Hz and 1746Hz. The switching frequency never exceeds the resonant frequency, which guarantees the LLC converter operates in the desired conditions.

The variable frequency control can also reduce the current stress of the LLC converter. As shown in Fig. 9a and Fig. 9b, the variable frequency control can significantly reduce the RMS value of the resonant current, leading to reduced losses of the switching devices. The simulation results of the semiconductor losses are shown in Fig. 10. S_1 and S_2 are the primary side switches of the LLC converter, while S_3 and S_4 are the secondary side switches. The IGBT model adopted in the simulation is SKM145GB066D.

The switching losses of S_1 and S_2 are almost constant in all

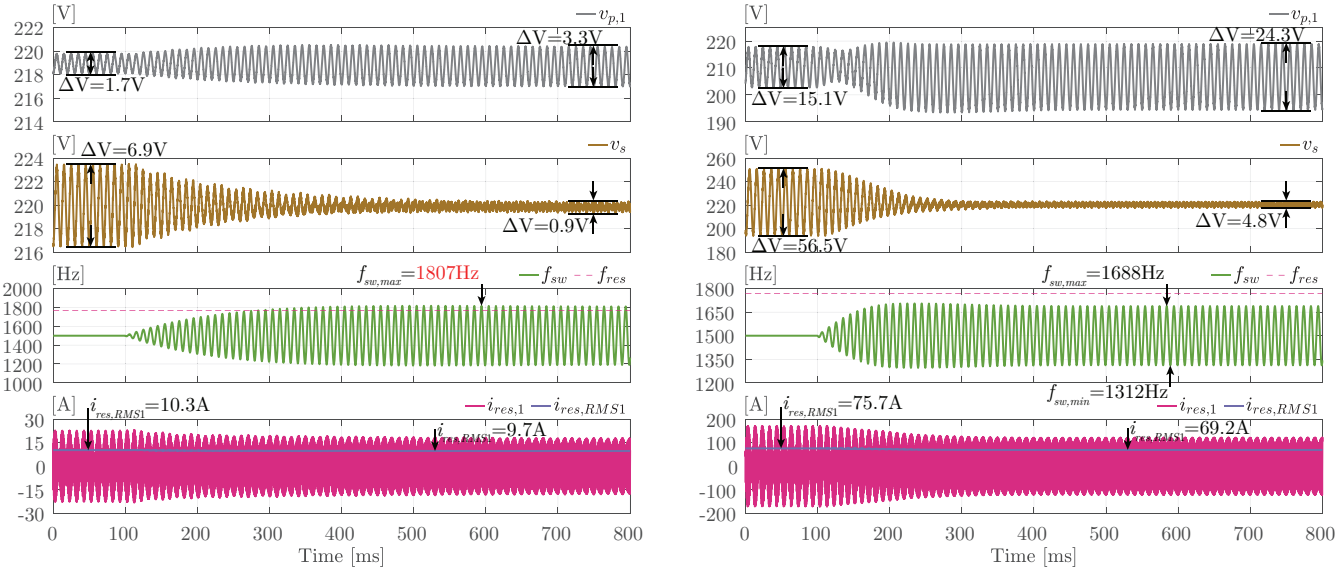


Fig. 11. Simulation result of the SST a) with 8kW output power and $L_m = 13$mH; b) with 54kW output power and L_m is reduced from 13mH to 1mH. The rest of the parameters are the same as in Fig. 9a

cases, while the switching losses of S_3 and S_4 are negligible and, therefore, not shown. As the variable frequency control can reduce $i_{res,RMS}$, a significant reduction of the conduction losses of all devices can be observed. Because the SHC transferred to the secondary side differs under different C_s, the improvement in semiconductor losses varies accordingly.

Due to the difficulty in the simulation of magnetic components, quantitative analysis of the magnetic losses is not provided. The impact of the variable frequency control on the overall efficiency of the SST should be further evaluated.

B. Modified Resonant Tank Design

In the above analysis, the output power of the SST is limited to $6\mathrm{kW}$ to guarantee the sub-resonant operation of LLC converter. According to Fig. 7, if the output exceeds $6\mathrm{kW}$, although it is already a very low output power, the required frequency deviation is still too high, and the sub-resonant operation of LLC converters cannot be guaranteed. This is because the original design of LLC converters in LV PETT only considers the open-loop operation, leading to a flat voltage gain curve at $f_{sw,c}$. Fig. 11a shows the simulation waveform of the SST at $8\mathrm{kW}$ with the original parameter from the LV PETT. The variable frequency control can still mitigate the ripple voltage, but the maximum switching frequency $f_{sw,max}$ exceeds the resonant frequency f_{res}, which means the LLC converters operate in the undesired condition.

To increase the output power of the SST while keeping the sub-resonant operation of the LLC converter, the resonant tank should be redesigned, which is in this work achieved purely by reducing the value of L_m. As a result, with the same frequency deviation, a higher voltage gain adjustment range of the LLC converter is achieved thanks to the steeper voltage gain curve. Fig. 11b presents the simulation waveform of the SST with full $54\mathrm{kW}$ output power. Because L_m is reduced from $13\mathrm{mH}$ to $1\mathrm{mH}$, a much higher ripple voltage is mitigated with even lower frequency oscillation compared to the case in Fig. 9a. However, it all comes at the cost of the stiffness of the voltage gain of LLC converters, which become more sensitive to load fluctuation.

Fig. 12 demonstrates the semiconductor loss of the LLC converters with and without the variable frequency control method and with different magnetizing inductance L_m. With $L_m = 13\mathrm{mH}$, the LLC converters have the lowest semiconductor losses, although the variable frequency control cannot be implemented, and the considerable second harmonic ripple appears on the output DC voltage. Because the reduction of L_m increases the magnetizing current peak, the current stress on devices also increases, which leads to higher losses. Once the variable frequency control is enabled, a significant reduction in the semiconductor losses can be observed. Although the losses are slightly higher than the case with large L_m, a much higher output voltage quality is achieved.

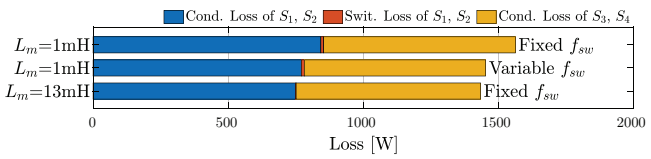


Fig. 12. Semiconductor losses of the LLC converters with and without the proposed variable frequency control method and with different magnetizing inductance L_m. The losses from the nine cells are added together. The output power of the SST is $54\mathrm{kW}$.

VI. Conclusion

Single-phase ISOP SST suffers from the SHC from the grid, which causes ripple voltage on the DC link and reduces the efficiency of the system. Especially, if the LLC converters with fixed switching frequency are adopted as the isolated DC/DC stage of the SST, the propagation of SHC to the secondary side is unavoidable.

Based on the CLC equivalent circuit, the SHC distribution in the SST is analyzed. A variable frequency control method of the LLC converter is proposed. By regulating the switching frequency and voltage gain of the LLC converters, the propagation of SHC to the secondary side is prevented, leading to reduced ripple voltage and current stress on devices. The principle and implementation of the proposed method are introduced. Simulation results verify the performance of the proposed method in the reduction of ripple voltage and semiconductor losses.

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