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***Abstract*— Dual-channel gate driver is commonly utilized in the industry for accommodating the widespread use of half-bridge power modules. As wide-bandgap devices become increasingly prevalent due to their superior switching characteristics compared with conventional silicon devices, this paper proposes a gate driver design for SiC MOSFET half-bridge module. In particular, for adapting to the case of higher voltage requirement, the proposed design includes a novel active voltage balancing circuit, which contributes to the aggregation of half-bridge module into a single device with double voltage rating. Targeting at 3.3kV/700A SiC MOSFET half-bridge power module, this paper provides a comprehensive elaboration of this gate driver, including background, conceptual design and detailed implementation. Finally, the experimental results are provided to demonstrate the operational performances.**

***Index Terms*— SiC MOSFET, dual-channel gate driver, voltage balancing, series connection.**

I. Introduction

The growing prominence of power electronics is increasingly evident in many industrial applications, particularly with the promotion and advancement of renewable energy technologies aimed for a low carbon society [1,2]. Serving as a crucial and decisive factor influencing the progress of power electronics technology, there is a continuous pursuit of breakthroughs and advancements in power electronics devices, striving for higher voltage and power ratings. While conventional Silicon devices such as IGBTs currently dominate this field, their potential for further advancement is restricted by the inherent physics of Silicon (Si) devices [3-5]. Therefore, there is a growing demand for wide band gap devices like Silicon Carbide (SiC) devices in the industrial market. The SiC MOSFET offers advantages such as higher switching speed, lower switching and conduction loss, and the ability to operate at higher temperatures. To meet the high voltage requirement in diverse industrial applications, some research groups have conducted tests on 10 kV /15 kV SiC MOSFETs [6-7]. However, these devices are currently limited to engineering samples and advanced laboratory prototypes, without any commercialization, considering prohibitively high costs. Nevertheless, commercially available SiC MOSFETs currently have a voltage rating of 3.3 kV [8], providing a more accessible option for industrial applications.

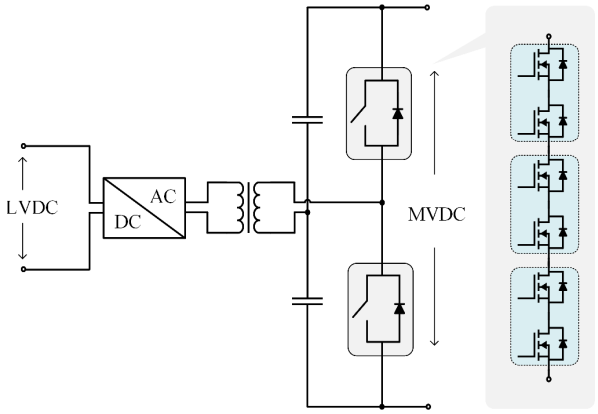

Fig. 1 Isolated DC/DC converter as the interface for interconnection of LVDC and MVDC networks, requiring HV switching stage on the MVDC side.

Recognizing the voltage limitation of a single device in meeting the high voltage requirement, many power electronics topologies have been developed to ensure compliance with the demand, which include diode-clamping multilevel converter [9], flying capacitor multilevel converter [10], modular multilevel converter [11], etc. These topologies break the blocking voltage limitation of the device, which have been serving various industrial application for several decades. Especially as the interfaces to AC distribution grid or AC motor drives, they offer the advantage of lowering the requirement of power filter due to the higher AC output voltage quality with multilevel characteristic. Nevertheless, in nowadays rising interest in DC power distribution networks to accommodate renewable energy sources or electric vehicles charging systems, compact DC/DC converters from LV (<1.5kV) to MV (>10kV) or vice versa are required. Taking one typical topology presented in Fig. 1 as an example, the above advantage of applying these multilevel topologies could not be typically benefited from, as two-level switching is typically used. Therefore,

series connection of 3.3kV SiC MOSFETs to substitute the currently unavailable high voltage device in the MV side provides an effective and only available solution, if monolithic and non-modular designs are considered.

However, a well-known challenge in series connection of power devices is the dynamic voltage imbalance issue, which is caused by the unmatched gate driver parameters and device parameters, also the difference of gate driver signal delays, etc. Compared with the series connection of conventional silicon IGBTs, the series connection of high-voltage high-power SiC MOSFETs is more challenging since the switching speed of SiC MOSFET is higher and the induced voltage imbalance could be more severe, which means the series branch becomes more vulnerable to overvoltage breakdown. Hence, it is important to apply suitable voltage balancing method for the series connection to ensure adequate voltage sharing across devices.

Consequently, this paper proposes a solution of dual-channel gate driver (GD) for high-voltage high-power SiC MOSFET half-bridge module, with the goal to make the two series connected devices inside the module aggregated into a single device with double voltage rating. Particularly, a novel active VB circuit is integrated inside this GD. Unlike the passive voltage balancing methods which suffer from notable power loss, and the existing active voltage balancing strategies which come with limited voltage balancing performance, high cost or high complexity [12-19], this approach utilizes only a few low-power BJTs, resistors, and capacitors. This simplified design provides the advantages of easy integration, low cost, and increased reliability. Targeting at 3.3kV/700A SiC MOSFET half-bridge power module, the comprehensive conceptual design and analysis of this GD is provided in this paper, followed by the hardware implementation and experimental validation.

II. Overall Structure of Dual-Channel Gate Driver

The GD serves as an essential part that realizes the interconnection between the power semiconductor module and the upstream control system. To give the illustration, its conceptual structure is depicted in Fig. 2.

Firstly, GD needs to amplify the digital switching signal to the required gate driving voltage of the power device as the basic function. Since the control system and the power devices do not share the same ground, signal isolation is required in GD design. Besides, gate driver power is generally provided by an external power supply which also does not share the same ground with the power devices, making power isolation another necessary part of GD. However, the design of signal and power isolations will introduce coupling capacitances which could induce the common mode noise during the switching transient of power device. Since high-voltage high-power SiC MOSFETs offer faster switching speed and longer transient period, the potential hazard becomes more severe when applying these devices if it is not well addressed. Therefore, in our GD design as presented in

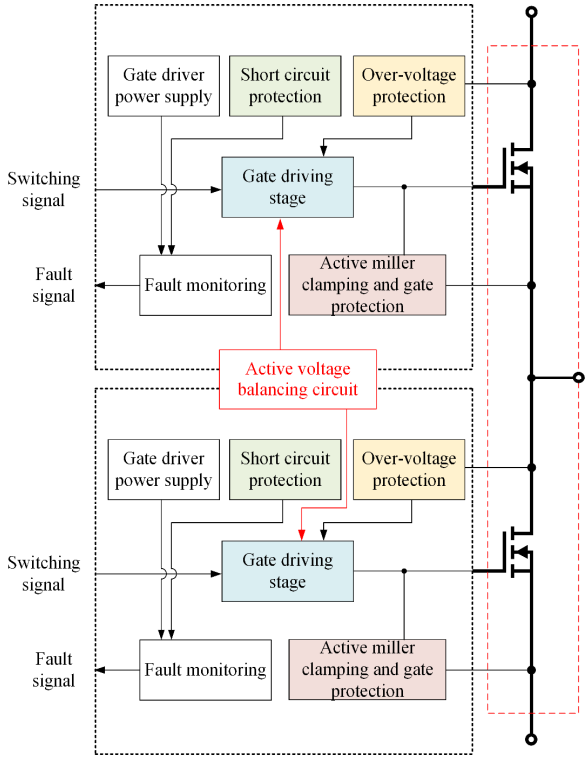

Fig. 2 Overall structure of designed GD

Fig. 3, the signal isolation is achieved by using optical fiber, which could provide galvanic isolation and theoretical zero capacitive coupling. As for the power isolation, the requirement is met by using current source loop power supply from Siebel [20]. One secondary decoupling unit DU15-24G which claims 15kV isolation voltage is used to provide sufficient power for one channel in GD. As the following parts of the output of DU15-24G, a non-isolated buck converter and a non-isolated buck-boost converter are respectively applied to generate the positive driving voltage V_{dd} (+18V) and the negative driving voltage V_{ee} (-7V) required by the gate driving stage. Besides, another non-isolated buck converter is used to generate +5V as the power supply of logic circuit inside.

In addition to the basic driving function with totem pole, protection design is also important in GD, and the corresponding hardware implementation in Fig. 2 is provided in Fig. 3 by using the same color as indication. Short-circuit protection circuit consists of the typical desaturation detection to compare the on-state voltage drop of SiC MOSFET with a threshold, and soft-shutdown to suppress the turn-off voltage overshoot when short-circuit occurs. Over-voltage protection is made of typical active voltage clamping circuit between the gate and drain terminals of SiC MOSFET, and active miller clamping and gate protection is used to prevent the damage to device from crosstalk, gate-source voltage oscillation, etc.

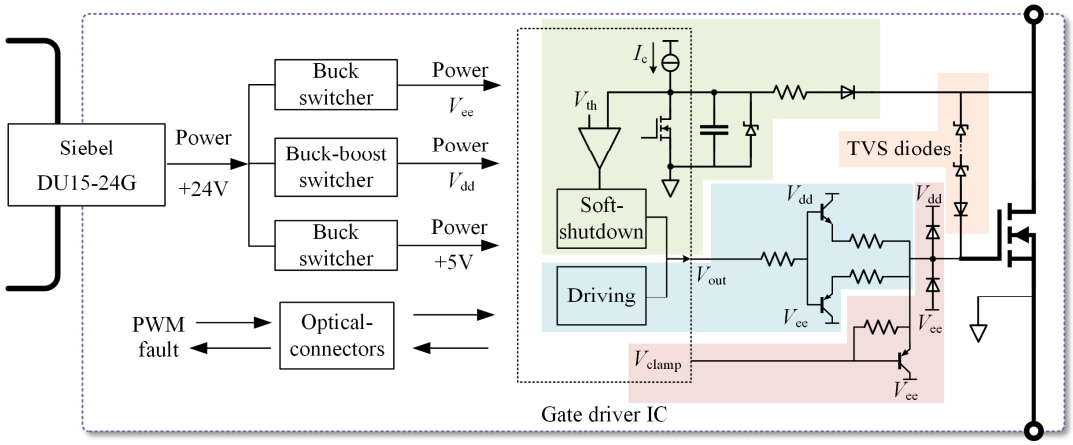

Fig. 3 Schematic of designed GD with details of the main parts (one channel is shown, with the same structure in the other channel)

Finally, for applying in high voltage case as elaborated, the two SiC MOSFETs inside the half-bridge module can be configured as series connection to switch synchronously. Generally, the static voltage imbalance caused by leakage current difference of power devices can be reduced by using parallel static voltage balancing resistors, with the value of one order less than the equivalent resistance of power device. However, the dynamic voltage imbalance can be hard to mitigate. The passive voltage balancing methods like using RC snubber will induce high power loss, moreover, the existing active voltage balancing methods still suffer from limited voltage balancing performance, high design/control complexity or high cost, which makes them not attractive in GD design [13 - 19]. Hence, a novel active voltage balancing circuit is proposed in this paper. As the key part of this GD, its working principle and hardware implementation are explained next.

III. Active Voltage Balancing Circuit

The active voltage balancing method reduces the drain-source voltage imbalance by regulating the gate driving process of series connected SiC MOSFETs, while some feedbacks about voltages across devices should be provided as the regulation criteria. Generally, delicate isolation is required to form this control loop since SiC MOSFETs have different source voltage potentials, which increases the burden of gate driver design. In our proposed method and circuit as shown in Fig. 4, the feedback detection and gate side regulation are only conducted in the upper SiC MOSFET, eliminating the necessity for the isolation.

The resistor-capacitor divider branch $R_{s1}C_{s1}$-$R_{s2}C_{s2}$, which is directly connected between the power terminal P and N of this module, is adopted to generate voltage trajectory reference v_A at the middle point A. Since R_{s1}=R_{s2} and C_{s1}=C_{s2}, v_A can be considered as one half of the voltage v_{sum} across the series connected devices if neglecting the current flowing through the resistor R_e. Due to the delay difference between gate signal *SW1* and *SW2* during the switching transient (which is regarded as the major factor causing the voltage imbalance in this analysis), the voltage v_B at the middle point B of this series branch will not be always equal to one half of v_{sum}, which also indicates the drain-source voltages (v_{ds1} and v_{ds2}) imbalance of SiC MOSFET S_1 and S_2 in this series connection.

Since the voltage difference between v_A and v_B can well reflect the degree of voltage imbalance, R_e, NPN transistor T_1 and PNP transistor T_2 are added to extract this information as the feedback. Once v_A is higher than v_B, a positive current i_e will flow through R_e and T_1; once v_A is lower than v_B, a negative current i_e will flow though T_2 and R_e. In the next state of the circuit, a positive mirror current source consisting of resistors R_1, R_2, NPN transistor T_5, PNP transistors T_3 and T_4 can amplify the positive i_e to inject compensation current i_{com} as the sourcing current into the gate side of S_1. Similarly, a negative mirror current source consisting of resistors R_3, R_4, PNP transistor T_8, NPN transistor T_6 and T_7 can amplify the negative i_e to extract i_{com} from the gate side of S_1. In this manner, once the voltage imbalance occurs during the switching transient, the current compensation will be activated immediately to regulate the gate driving

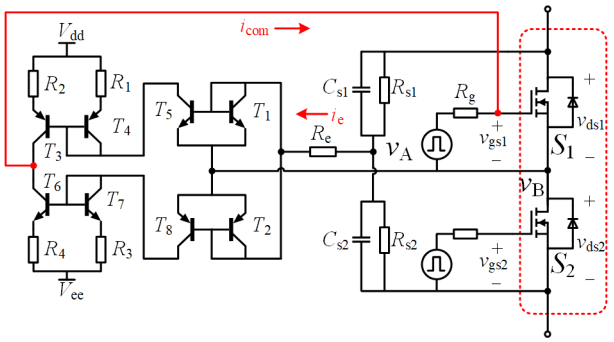

Fig. 4 Proposed active voltage balancing circuit

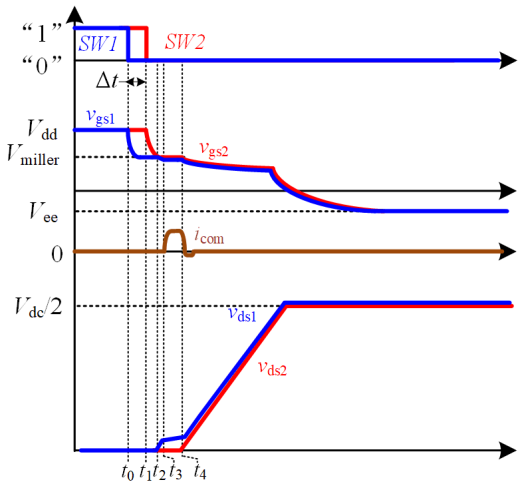

Fig. 5 Waveforms of voltage sharing with the proposed circuit

process of S_1, and to reduce the voltage imbalance. Taking the turn-off process and the case of *SW1* is faster than *SW2* as an example, the diagram of corresponding voltage sharing performance is depicted in Fig. 5, and the working detail is summarized as follows:

t_0-t_1: Before the time t_0, the gate-source voltage v_{gsi} (i=1 ,2) of S_i is equal to V_{dd} and both devices are in the on state. At t_0, *SW1* turns from "1" to "0" and v_{gs1} starts to decrease, which is accompanied with the transition of S_1 from linear region to saturation region. After a certain delay Δt, at t_1, *SW2* turns from "1" to "0" as well, and v_{gs2} starts to decrease. The voltage drop of device can be neglected in this stage, and v_{dsi} remains zero.

t_1-t_2: Both S_1 and S_2 are transiting into saturation region in this stage. It is worth noting that, for S_1, despite that v_{gs1} already reaches the Miller voltage V_{miller} as depicted, the nonlinear characteristic of Miller capacitor C_{gd1} causes that the rising of v_{ds1} can be ignored in the initial short-term period. At t_2, C_{gd1} becomes a much smaller value and v_{ds1} starts to increase dramatically. When analyzing the characteristic of S_2, the principle is the same as described. For simplicity, the dramatic rising of v_{dsi} (i=1, 2) is approximately linearized in this diagram, although a more advanced model in this stage helps to make the analysis more accurate.

t_2-t_3: Since v_{ds1} gets increased while v_{ds2} remains zero, v_A derived as $(v_{ds1}+v_{ds2})/2$ becomes higher than v_B which is equal to v_{ds2}. Theoretically, i_e becomes positive and i_{com} will be activated as the sourcing current to the gate side of S_1 immediately. However, due to the execution delay of the real circuitry (required to charge the junction capacitors, etc.), the compensation current will not be formed in time, which results in this delay stage.

t_3-t_4: After a certain delay t_d (i.e., t_3-t_2), at t_3, i_{com} will be injected into the gate side of S_1, and its magnitude can be expressed as:

$$i_{com} = t_d \cdot \frac{dv_{ds1}}{dt} \cdot \frac{R_1}{R_2} / (2 \cdot R_e) \tag{1}$$

Consequently, as the gate discharging is slowed down, the rising of v_{ds1} will get slower, which can be estimated as:

$$\frac{dv_{ds1}}{dt} = \frac{V_{miller} - V_{ee} - R_g \cdot i_{com}}{R_g \cdot C_{rss}} \tag{2}$$

At t_4, v_{ds2} starts to increase dramatically as well, and the gate compensation will be gradually disabled as dv_{ds1}/dt and dv_{ds2}/dt tend to be identical. However, due to the circuit delay, i_{com} could become negative and then gradually diverge to zero. Therefore, the compensation current should be moderate to prevent v_{ds2} from increasing significantly faster than v_{ds1}, which could result in overcompensation (where peak value of v_{ds2} becomes considerably higher than v_{ds1}). Here the principle to define the parameter choosing is given: in equation (2), dv_{ds1}/dt should remain positive to avoid S_1 returning to its linear region. Hence, the maximum allowable value of the current source can be determined using equation (4), and dv_{ds1}/dt and dv_{ds2}/dt will gradually approach each other, reducing the voltage imbalance.

Since the proposed voltage balancing circuit is composed of analogue components, once parameters are determined according to a specific case, they are not flexible to be easily changed for other cases, and the voltage balancing performance may not be optimal for all operating conditions. Therefore, the parameters of the proposed circuit are chosen in high voltage/current case where dv/dt is relatively high and the voltage imbalance could result in device failure. With the same parameters, despite that the voltage balancing performance could not be optimal when applied in low voltage/current case, the voltage imbalance can be tolerated as it is less critical compared to high voltage/current case.

IV. Hardware Prototype and Experimental Result

Since the ultimate goal of the ongoing project is to build 250kW DC/DC convert prototype as presented in Fig. 1, the current rating requirement in the MVDC side is not high, where 100A switching current can be defined as high current in this application. At the current stage, the commercially available 3.3kV/700A half-bridge power module from Mitsubishi is applied to build this prototype, and its GD is developed as shown in Fig. 6 to validate above presented concepts. The GD, placed on the top of half-bridge power module, adopts the design of two stacked PCBs, as shown in Fig. 6(a). The top PCB shown in Fig. 6(b), which is less influenced by the noise from the power side, contains voltage conversion parts which convert the Siebel gate driver power supply to required V_{ee}, V_{dd} and +5V, and some logic circuits for handling PWM signal and monitoring fault signal. The bottom PCB shown in Fig. 6(c), which is attached to the surface of this half-bridge power module, contains basic gate driving stage, active miller clamping and gate protection, over-voltage protection and short circuit protection on the top side. Besides, the active voltage balancing circuit, consists of only few low voltage and low power BJTs, resistors and capacitors, is placed on the bottom side of the bottom PCB. In this way, the parasitic inductance of routing wire is minimized to further

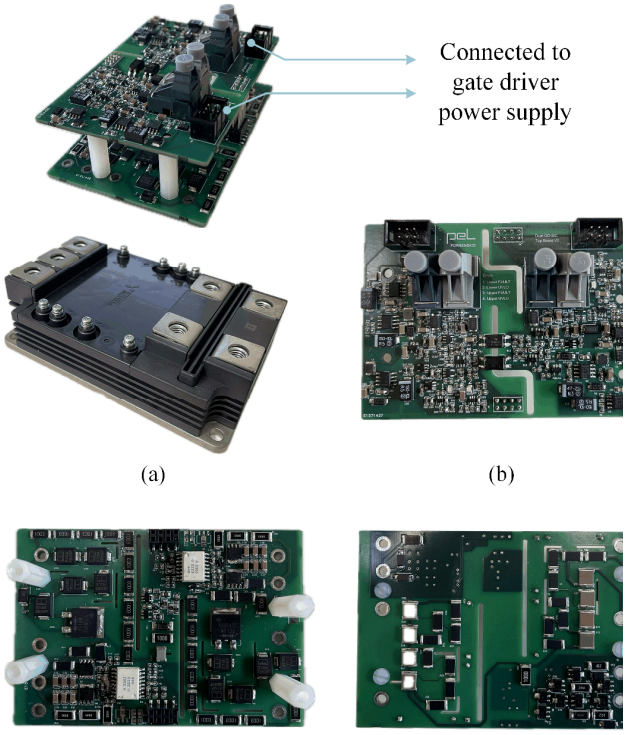

Fig. 6 (a) Two-PCB stacked GD design (b) Top PCB with voltage conversion and logic handling (c) Bottom PCB with gate driving, etc. on the top side (left figure) and active VB circuit on the bottom side (right figure)

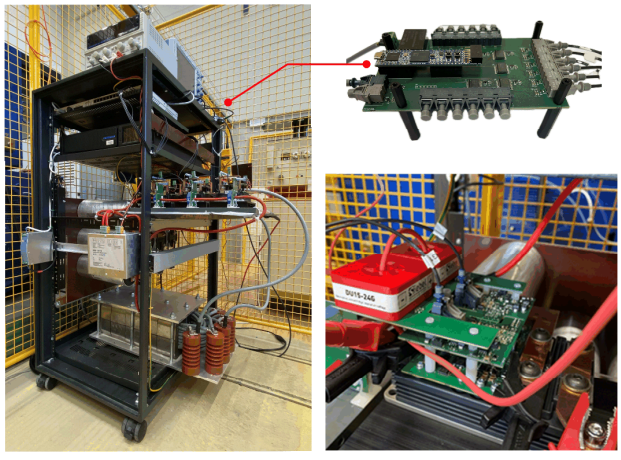

Fig. 7 (a) Double pulse test setup (b) Assembled GD with half-bridge power module for testing

enhance the voltage balancing performance of active voltage balancing circuit.

Further, the double-pulse testing setup is established as shown in Fig. 7(a), where a 10 kV variable DC power supply from Heinzinger is selected as the source, and ten 1.32 kV/ 1 mF film capacitors are connected in series as the DC-link capacitor for meeting the testing voltage and current requirement. After assembling the GD with the power module as device under test as shown in Fig. 7(b),

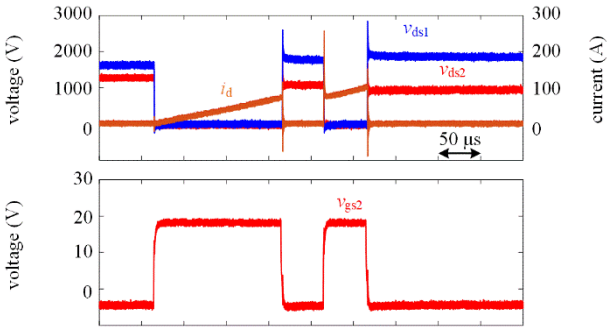

Fig. 8 Testing result by using designed GD with active voltage balancing circuit disabled in the 3000V/100A (max) case

TABLE I
KEY COMPONENTS PARAMETERS

Name	Parameters
S_i (i = 1, 2)	FMF750DC-66A
T_1, T_5, T_6, T_7	2SCR542P
T_2, T_3, T_4, T_8	2SAR542P
R_g, R_e	2.2 Ω, 50 Ω
R_1 (R_3), R_2 (R_4)	3.6 Ω, 1.2 Ω
R_{si}, C_{si} (i = 1, 2)	1 MΩ , 1.2 nF

the testing setup is placed inside a cage, and the optic-fiber communication is applied as the remote control for the safety of the operator.

Since the devices in this half-bridge power module is configured to switch synchronously as series connection, the switching signal from the controller should be distributed into several signals. Therefore, a signal distribution board based on FPGA is designed and manufactured to distribute the signals, with the capability to finely control and adjust the switching signal delays (step size of 0.25ns) by using time delay chip DS1023-25.

To validate the designed active voltage balancing circuit, its current compensation output to the gate side of upper SiC MOSFET is removed in the initial test (the red line in Fig. 4), and the natural voltage sharing performance of series connected SiC MOSFETs could be observed. As shown in Fig. 8, during the switching process, v_{gsi} (i = 1, 2) varies between -7V and +18V to turn on/off SiC MOSFET. Due to the switching signal delay difference (considered as the major factor in this experimental case), etc., a severe voltage imbalance occurs in series connection under 3kV testing voltage, as presented by v_{ds1} and v_{ds2}. As the power loop current gets higher, the induced voltage imbalance during the turn-off transient could become even worse. Therefore, it is necessary to design voltage balancing circuit to mitigate the voltage imbalance.

With the key parameters listed in Table I, the corresponding voltage sharing performance by enabling the gate current compensation is shown in Fig. 9. It is observed that, by defining the voltage imbalance degree as (v_{ds1}-v_{ds2})/ (v_{ds1}+v_{ds2}), it is greatly reduced from 33.3% to 8.3%. Moreover, the voltage v_A of the middle point of

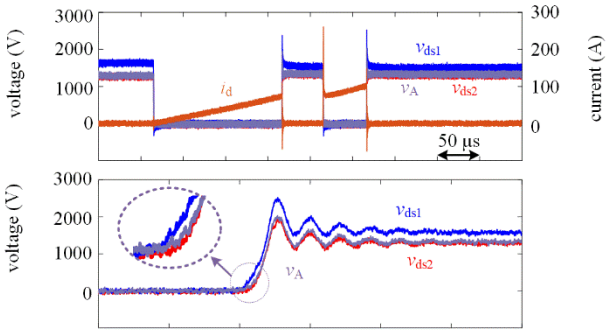

Fig. 9 Voltage sharing performance with active voltage balancing circuit enabled in the 3000V/100A (max) case

$R_{s1}C_{s1}$-$R_{s2}C_{s2}$ branch is presented, which is almost aligned with v_{ds2} during the steady state. During the turn-off transient as shown in the zoomed view in the bottom, v_A is slightly higher than v_{ds2} (v_B) to activate the gate compensation, and the voltage imbalance can be mitigated as expected.

The parameters choosing of active voltage balancing circuit is based on the 3kV/100A case in this experiment, and the effectiveness of proposed design gets validated according to the results as above. Additionally, in the experiments, the test with the same parameters under the lower voltage/current case is also conducted, and the results are shown in Fig. 10.

It is observed that, since only one set of parameters can be chosen due to its fully analogue circuit structure, the voltage balancing performance could not be as optimal when applied in the comparatively lower voltage/current case. Specifically in this case, the active voltage balancing circuit has nearly no effect for mitigating voltage imbalance since the low *dv/dt* makes the

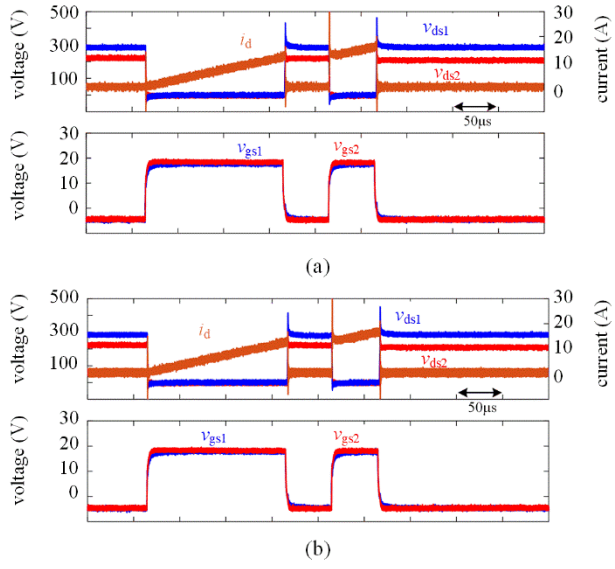

Fig. 10 Voltage sharing performance with active voltage balancing circuit (a) disabled and (b) enabled in the 600V/20A (max) case

compensation current to the gate side of upper SiC MOSFET rather small. However, since the SiC MOSFETs have much higher voltage rating (3.3kV in this design), the voltage imbalance in the low voltage/current case can be tolerated. In summary, the proposed GD with active voltage balancing capability has the potential to utilize the half-bridge module in a series connection, effectively aggregating it into a single device with double voltage rating.

V. Conclusion

In this paper, a GD with active voltage balancing circuit for series connection of SiC MOSFETs is proposed and designed, which have the capability to aggregate the half-bridge power module into a single device with double voltage rating. The active voltage balancing circuit has the advantages of simple structure, easy integration, low cost, and increased reliability. The experiments conducted on Mitsubishi half -bridge power module FMF750DC-66A, have shown that it can reduce the voltage imbalance from 33.3% to 8.3%, which validates its effectiveness. In the near future work, the active voltage balancing circuit will be combined with short circuit protection circuits to investigate its performance during the turn-off process of a short circuit, and there will be optimization efforts directed towards refining the design of the GD.

Acknowledgment

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