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Static and Dynamic Voltage Balancing for an IGCT-Based Resonant DC Transformer

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***Abstract*—This paper focuses on the operational characteristics of a medium voltage resonant DC transformer based on a split capacitor IGCT 3L-NPC leg. The study delves into both the dynamic and static balancing aspects of the 3L-NPC when operating in a two-level, 50% duty cycle mode. This particular operating condition, which skips the zero-level state and involves extra low turn-off current due to the resonant operation, presents challenges in ensuring reliable medium-frequency operation of the DC transformer. Thus, this work evaluates the behavior across various turn-off current conditions, an assessment of the dynamic balancing incorporating a low-value capacitive snubber, and the performance of the NPC symmetrizing resistor for the static voltage balancing. To validate the effectiveness of the designed snubber configurations, practical experiments are conducted using the MV prototype.**

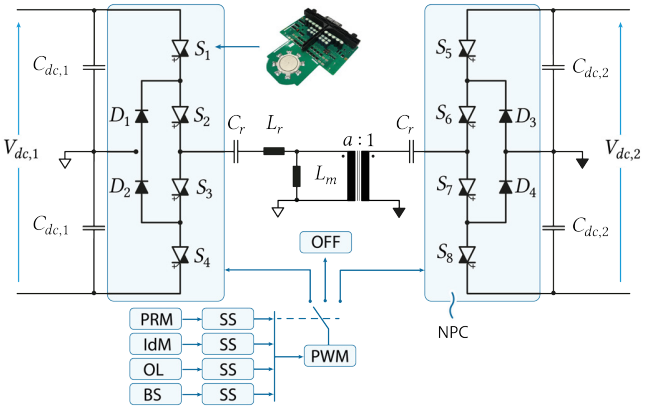
***Index Terms*—DC Transformer, Dynamic Voltage balancing, IGCT, LLC Resonant Converter, NPC, Medium voltage, MFT, Static voltage balancing.**

I. Introduction

The shift towards DC power distribution networks, enabled by power electronics technologies, is changing the nature of electrical power systems. Nowadays, DC power distribution networks (PDN) can effectively support energy transformation with distributed energy resources and energy storage, both of which are predominantly DC. This integration can be highly beneficial for future energy systems, as long as there are clear technological and economic advantages. However, one essential technology to enable a more complex DC PDN is still underdeveloped, which is the element behaving identically to the AC transformer, the DC transformer.

The DC transformer (DCT) is the converter that interconnects different power sources and loads in different voltage levels, while providing galvanic isolation. More specifically, the DC transformer, relying on the LLC converter, is capable of providing the current path between two DC buses according to the system's natural power flow, without the need for the closed-loop control system for its operation [1]. This passive behavior is possible due to the practically constant gain for any load condition for near resonant frequency operation. Thus, this converter brings the simplicity of the AC transformer to the DC systems.

However, several challenges require special attention, mainly in terms of the design using the existing technologies and costs. Works investigating high-power medium voltage LLC converters have highlighted the challenges of its operation [2] and design [3], [4].



(a)

Fig. 1. Schematic of the Split-Capacitor IGCT-based 3L-NPC resonant DCT. Developed logic for the reliable open-loop DCT operation [5], including power reversal methods (PRM), soft-start (SS), overload protection (OL), and black start (BS).

The DCT under investigation in this work is shown in Fig. 1. It consists of an IGCT-based LLC resonant converter with split-capacitor 3L-NPC power stages. The 3L operation plays a crucial role in protecting the DCT, providing soft-start and current-limiting capabilities [6]. Nevertheless, during regular operation, the power stage operates in a two-level (2L) 50% duty cycle to drive the resonant tank, where the two upper and two lower IGCTs are essentially connected in series, and both dynamic and static balancing need to be ensured.

The concept of static and dynamic voltage balancing in series-connected IGCTs has been proposed multiple times in the literature [7]–[9]. However, these proposals primarily focus on hard-switched topologies commonly employed in medium-voltage (MV) drives [7], [10]. Only recently there has been an exploration of applying these balancing techniques to soft-switching applications, as explored in [2]. In that study, the resonant operation was tested for the series connection of IGCTs. The investigation evaluated the switching behavior of the RC-IGCTs with a low turn-off current (down to 50 A), utilizing a parallel-connected C-snubber for dynamic voltage balancing and a parallel resistor for static voltage balancing.

Fig. 2. Photo of the 1 MW MV DCT prototype.

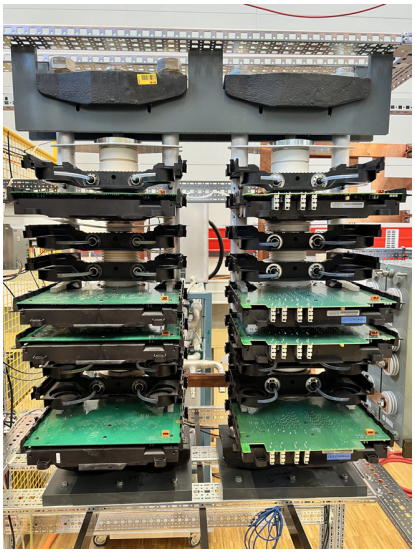


Fig. 3. 3L-NPC RC-IGCT stacks.

Thus, following the advancements presented in [2], this work incorporates the IGCT stacks into a 3L-NPC leg power stage with the developed 1 MW MFT to assess its performance. The assessment includes testing the dynamic voltage balancing using the C-snubber with an ultra-low turn-off current (lower than 20 A). Also, the single symmetrizing resistor in parallel with the inner two IGCTs is used for static voltage balancing.

This paper is organized as follows. In Section II the developed MV DCT prototype is described, providing a detailed description of the IGCTs stacks, MFT design, and the resonant capacitor selection. Section III delves into the designs of static and dynamic voltage balancing snubbers, including validation with the MV DCT prototype. Section IV presents the experimental verification of the no-load operation of the MFT. Finally, Section V provides conclusions and outlines future works.

II. MV DCT Prototype

The MV DCT prototype consists of a 10 kV : 5 kV DC-DC LLC resonant converter with split-capacitor-based 3L-NPC power stages. Fig. 2 shows the MV DCT prototype. The complete converter is fitted inside the cabinet (200 x 80 x 80 cm), besides the deionized water cooling unit which is located outside and connected to the laboratory water supply system. The integration has not been optimized.

A. 3L-NPC RC-IGCT Stacks

The RC-IGCT stack consists of a 3L-NPC leg, with the RC-IGCTs and the NP diodes, multiple heat sinks, all held by a mechanical clamp, as shown in Fig. 3. The heat sinks provide electrical, and also a thermal interface for the heat exchange between the press-pack devices and the deionized water.

TABLE I
General information about the MV DCT

Description	Symbol (Unit)	Value
Rated power	P_{n} (MW)	1
DC Voltage 1	$V_{\mathrm{dc},1}$ (kV)	10 (5)
DC Voltage 2	$V_{\mathrm{dc},2}$ (kV)	5
DC-link capacitance 1	$C_{dc,1}$ (μF)	400
DC-link capacitance 2	$C_{dc,2}$ (mF)	2.6

The primary side is supported by 10 kV RC-IGCTs, acquired as engineering samples from Hitachi Energy Semiconductors. In this work, the prototype is reconfigured for the 5 kV : 5 kV operation using the 4.5 kV RC-IGCTs (5SGX1445H0001), and the NP clamping diodes (5SDF0545F0001).

The main parameters of the MV DCT are given in Tab. I. The IGCTs are controlled by the ABB's AC800PEC controller. The setup also includes the ABB's COMBI-IO to interface various peripheral equipment and ABB's PEC-MI for interfacing voltage and current sensors.

B. 1 MW Medium Voltage MFT

Designing MFTs requires resolving a multi-physical optimization problem involving electric, magnetic, dielectric, and thermal aspects. Starting from the materials used for core and windings, as well as insulation and cooling, over the specific transformer construction type, to different methods that can be used to implement the design optimization algorithm.

The choice of the winding technologies involves the selection of its power capability, cooling strategy, and insulation method. Among diverse technologies for windings, the most common are Litz wire, foil, coaxial, and hollow/pipe conduc-

(a) (b) (c)

Fig. 4. (a) Round Cu hollow conductors inside oil vessels made of phenolic paper composite material Etronit I and B66. (b) The nanocrystalline core is made out of C-cut cores, resulting in the lower half of the core being made out of four C-cut cores together. (c) The fully assembled 1 MW MFT prototype with a 2:1 turns ratio configuration.

tors. Also, such windings are usually considered in Copper (Cu) or Aluminum (Al) material.

In particular, taking advantage of the already available deionized water cooling system in the setup, the round hollow conductor made of Cu was chosen to be the windings [11]. In this way, the winding losses are removed with water flowing inside the windings. Concerning the insulation coordination of the windings, the oil insulation was chosen as it is very effective (typically from 5kV/mm to 20 kV/mm) and has a positive influence on power density increase compared to a simpler insulation option such as air (approximately 3kV/mm). Thus, Fig. 4a shows the Cu round hollow conductors inside the oil vessel. In total four windings split into two vessels were used to allow reconfigurations of the primary and secondary windings, including the 1:1 and 2:1 turns ratio configurations.

Regarding the magnetic core, some of the most popular core materials for switched applications are the ferrite, amorphous alloy, and nanocrystalline alloy cores. The ferrite core has typically low hysteresis loss, very low eddy current loss, and relatively low cost compared with other solutions. The disadvantage is the low saturation flux density (0.3 - 0.5 T), and are typically built in small mechanical sizes. The amorphous allow on the other hand has high saturation flux density (0.5 - 1.6 T), with loss hysteresis loss, and is mechanically robust. On the downside, this material is limited in shape, has high acoustic noise, and is relatively expensive. The third option mentioned here is the nanocrystalline alloy, this material is an iron-based alloy of silicon as a thin tape with minor portions of crystal structure. This material also has low hysteresis loss, high saturation flux density (1 - 1.2 T), and lower acoustic noise. However, it can be also relatively expensive, and it is mechanically fragile. In the end, the nanocrystalline alloy core was selected due to its good magnetic properties to build the prototype. Fig. 4b shows the details of the final core assembly made out of several C-shaped pieces.

Finally, a specific MFT design comes as a solution to a multi-parameter optimization problem, selected based on a certain criterion. This could be e.g. minimal transformer weight, minimal volume, minimal material and manufacturing cost, or even a combination of different parameters expressed in the form of a cost function. Furthermore, from all the possible choices and trade-offs, the leakage and magnetizing inductance need to be designed to fulfill the specifications of the DCT application. Thus, electrical, magnetic, and thermal models need to be adapted to properly map these parameters to build the prototype as performed in [12].

TABLE II
MFT MAIN PARAMETERS

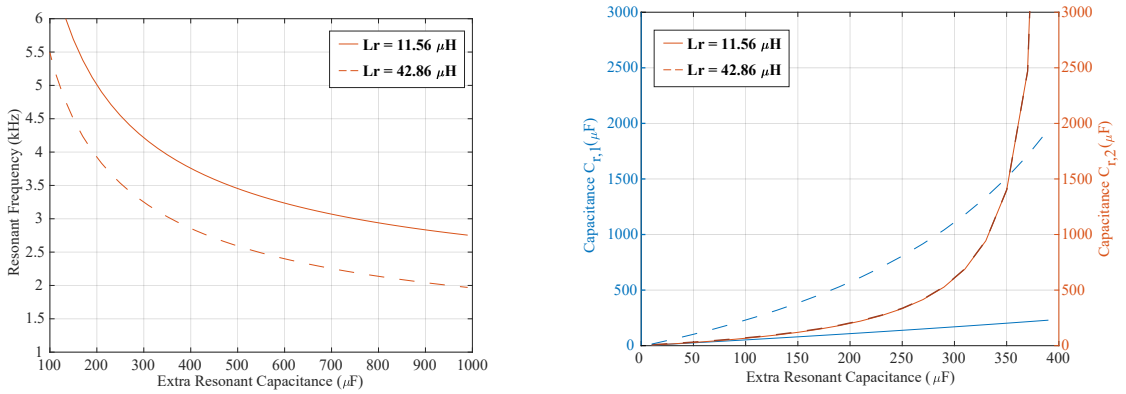
Description	Symbol (Unit)	DCT
Leakage inductance (2:1)	L_{r} (μH)	42.86
Leakage inductance (1:1)	L_{r} (μH)	11.1
Magnetizing inductance	L_{m} (mH)	10.7
Winding resistance	R_w (mΩ)	40
Operating frequency	f_{s} (kHz)	$1-5$
Inductance ratio	L_n	964

In summary, the 1 MW MFT prototype was built with a nanocrystalline air-cooled core and hollow copper oil-insulated water-cooled windings. The complete MFT is shown in Fig. 4c. The prototype was designed up to 5 kHz, and oversized in terms of maximum operational magnetic flux density to allow the operation with lower switching frequencies, down to 1kHz, without entering into saturation. Also, the winding terminations were made available at the front of the MFT, allowing the easy reconfiguration of the windings. Table II shows the main electrical parameters.

C. Resonant Tank Capacitor Selection

To complete the resonant tank, the capacitors are mounted externally. The capacitance value of the resonant capacitor directly influences the resonant frequency of the resonant tank. As DC link caps are typically much larger than resonant caps, their effect can be neglected and do not contribute to the resonant frequency. However, if the capacitance is in the same range, the DC-link capacitor must also be taken into account.

In situations where the DC-link capacitance on each side differs, such as in the case of the MV DCT prototype, each side



(a) (b)

Fig. 5. (a) Required extra capacitance considering the same value of capacitor at each side, to reach a desired resonant frequency for the two possible windings configurations. The dashed line represents the 2:1 turns ratio configuration case whereas the solid line is the 1:1 turns ratio configuration. (b) The capacitance value of each resonant capacitor considering the same equivalent capacitance at each side of the MFT. Capacitance values for the two possible windings configurations.

of the DCT has a distinct impact on the equivalent capacitance. In particular, when using the 1:1 turns ratio configuration, the capacitor on the secondary side is reflected to the primary without the turns ratio factor, which increases its impact. In the prototype, the capacitors on each side are different due to the availability of capacitors for different voltage ratings (10 kV and 5 kV.)

Consequently, to ensure smooth bidirectional operation, it becomes crucial to ensure that both sides of the resonant tank impedance loops exhibit similar impedance characteristics. This requires calculating the equivalent capacitance for each side and any additional required capacitance (resonant capacitor) should be incorporated accordingly.

Using the schematic of Fig. 1, the equivalent capacitance of the primary and secondary sides can be calculated according to the following:

- Primary side

$$C_1 = \frac{(C_{dc,1} + C_{dc,1}) \times C_{r,1}}{(C_{dc,1} + C_{dc,1}) + C_{r,1}} = \frac{2C_{dc,1} \times C_{r,1}}{2C_{dc,1} + C_{r,1}} \quad (1)$$

- Secondary side

$$C_2 = \frac{(C_{dc,2} + C_{dc,2}) \times C_{r,2}}{(C_{dc,2} + C_{dc,2}) + C_{r,2}} = \frac{2C_{dc,2} \times C_{r,2}}{2C_{dc,2} + C_{r,2}} \quad (2)$$

where C_1 and C_2 are the equivalent capacitance of each side of the MFT. Now, the total equivalent capacitance, reflected to the primary, can be written as:

$$C_{tot} = \frac{C_1 \times C_2'}{C_1 + C_2'} = \frac{C_1 \times \frac{C_2}{a^2}}{C_1 + \frac{C_2}{a^2}} \quad (3)$$

Then, solving for C_{tot}, it results in (4). With the C_{tot}, one can find the value of the resonant capacitor for the desired resonant frequency. Furthermore, to select a combination of resonant capacitors which would result in the same equivalent capacitance for each side of the MFT, i.e. $C_1 = C_2$, a second equation is created.

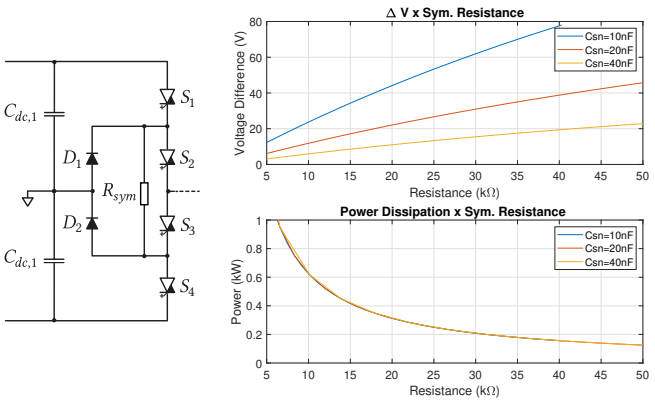
$$C_1 = C_2 \rightarrow \frac{2C_{dc,1} \times C_{r,1}}{2C_{dc,1} + C_{r,1}} = \frac{2C_{dc,2} \times C_{r,2}}{2C_{dc,2} + C_{r,2}} \quad (5)$$

In this way, (4) and (5) create a system of equations to find the combination of the resonant capacitors to have the same total equivalent capacitance for each side.

Fig. 5a shows the required resonant capacitance value to realize a specific resonant frequency considering the parameters of the MV DCT prototype described in Table I and Table II. With this plot, any combination of extra capacitors added to the resonant tank that results in this specific capacitance would meet the requirement for the resonant frequency.

However, if it is desired to have the same equivalent capacitance value for each side of the MFT (i.e. $C_1 = C_2$), each resonant capacitor needs to combine and compensate the DC-link capacitance, detailed in Table I. Thus, Fig. 5a shows the possible combinations for low values of extra resonant capacitance for the two possible MFT configurations under analysis. To fulfill this requirement, the extra capacitance on the secondary side needs to be much higher due to the already high capacitance values of the DC-link. After a requirement of $C_x = 350$ μF of extra capacitance, the capacitance value for the secondary becomes too high, making its practical realization more challenging.

$$C_{tot} = \frac{2C_{dc,1}2C_{dc,2}C_{r,1}C_{r,2}}{2C_{dc,1}2C_{dc,2}C_{r,2} + 2C_{dc,2}C_{r,1}C_{r,2} + 2C_{dc,1}2C_{dc,2}C_{r,1}a^2 + 2C_{dc,1}C_{r,1}C_{r,2}a^2} \quad (4)$$



(a) (b)

Fig. 6. (a) Schematic of the 3L-NPC with symmetrizing resistor. (b) Pertinent plots for the symmetrizing resistor design. On top of the expected/allowed voltage unbalance and below the total correspondent power dissipation of the selected resistor.

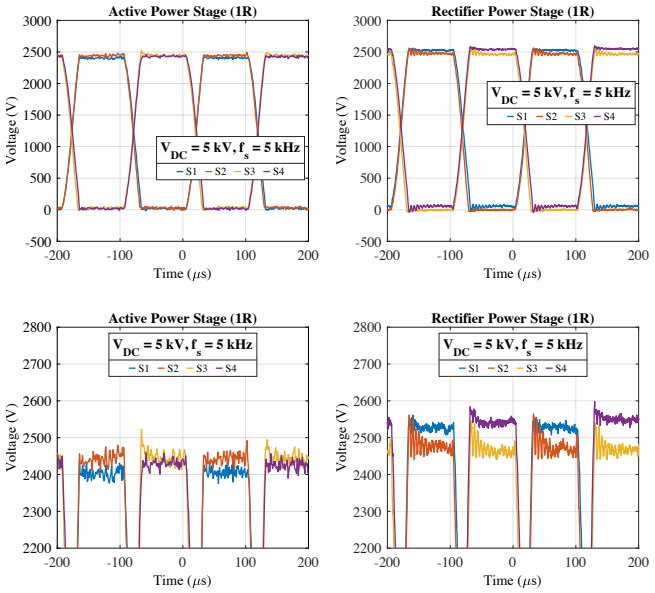


Fig. 7. Experimental waveform of the voltage across the IGCTs for the active and passive stack for the 5 kV and 5 kHz no-load operation with NPC symmetrizing resistor snubber. The dead time was set to 30μs and a C-snubber of 20nF was used for dynamic voltage balancing.

Ultimately, it can be seen that the total resonant capacitance to realize 5 kHz resonant frequency is around $C_x = 200$ μF for the $1:1$ turns-ratio configuration and around $C_x = 125$ μF for the $2:1$ turns-ratio configuration.

III. Design of Snubbers

In contrast to IGBTs, which can take advantage of active voltage balancing, series-connected IGCTs rely on passive snubbers and balancing resistors to ensure both dynamic and static voltage sharing. Therefore, the NPC symmetrizing resistor is used for the static voltage balancing, and a C-snubber is used for the dynamic voltage balancing.

A. NPC Symmetrizing Resistor

Taking advantage of the NPC-leg, which has the NP clamping diodes between the devices and the neutral point, a single symmetrizing resistor can be used for static voltage balancing. The resistor is positioned in parallel to the inner two IGCTs of the NPC-leg, as shown in Fig. 6a. This solution is broadly used in 3L-NPC inverters [13]–[17]. Differently, from the simple parallel resistor strategy [18], which is often designed for the maximum leakage current of the device, the symmetrizing resistor needs to compensate only for the leakage difference of the devices.

A simple design rule of this resistor can be derived considering the output capacitance rate of discharge and the current divider between the symmetrizing resistor and the equivalent parallel switch, resulting in:

$$\Delta V = \frac{R_{sym}}{R_{sym} + R_{leak,S_2}} \hat{I}_{leak,0} \frac{T_s}{C_{out}} \tag{6}$$

where ΔV is the voltage difference between both series-connected IGCTs, R_{leak,S_2} is the equivalent resistance of the switch S_2 (which is the switch in parallel with the R_{sym} for the $-V_{dc}/2$ state - similar rule can be derived with $V_{dc}/2$ and S_3), $\hat{I}_{leak,0}$ is the peak leakage current of the device, and C_{out} is the output capacitance of the device.

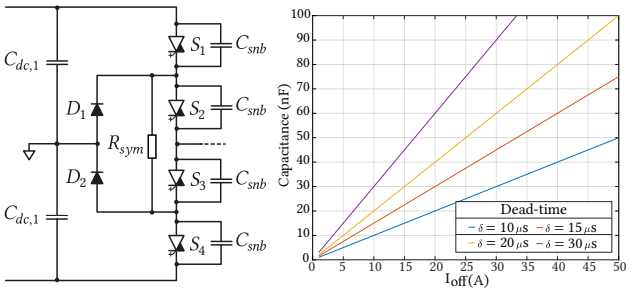
Thus, (6) relates the voltage difference between the devices and the value of the symmetrizing resistance depending on the capacitance value in parallel with the device. This capacitance value impacts the rate of change to discharge the voltage with the leakage current. In (6) this capacitance is written as C_{out}, being the output capacitance of the device; however, if a snubber is included, it should be considered for proper calculation.

Fig. 6b shows the design of the symmetrizing resistor using (6). At the bottom of Fig. 6b, the power dissipation is shown for the symmetrizing resistor. Using this plot, the resistance value is chosen to be $R_{sym} = 20$ kΩ resulting in a power consumption of $P_{Rsym} = 320$ W per stack.

This resistor was tested with MV DCT prototype for the $1:1$ turns ratio configuration, supplying the primary side to a 5 kV power supply with the secondary side connected and no-load. Fig. 7 shows the experimental results for the voltage across the IGCTs during the 2L operation with 5 kV and 5 kHz. It can be seen that in this case, the voltage unbalance was mitigated by the snubber. The voltage difference of the active side was approximately 40 V, while for the rectifier side was 76 V. The total power dissipation represents 0.064% of the nominal power (1 MW).

B. Dynamic Voltage Balancing

The dynamic voltage balancing is designed to ensure safe operation during the switching transitions. The sizing of the snubber for the series connected IGCTs is affected by both the maximum acceptable dynamic voltage imbalance, and by the expected turn-off current level.



(a) (b)

Fig. 8. (a) Schematic of the 3L-NPC with symmetrizing resistor with C-snubber. (b) Maximum snubber capacitance vs turn-off current for different dead times.

With the low turn-off current, the voltage rise time increases drastically. Further, the sum of the gate unit delay and voltage rise becomes in a comparable range of the available switching period of 200 μs. Nevertheless, compared to the usual RCD snubber required for hard-switching applications, the soft-switching conditions bring the possibility to simplify this circuit. Firstly, as the switching transients happen with ZVS, there is no danger linked to the discharge of the snubber capacitance into the device about to turn ON. Consequently, a purely capacitive snubber is enough for this application bringing advantages such as size, cost, and efficiency. Fig. 8a shows the capacitor snubbers in parallel with the IGCTs.

In this way, the capacitor snubber should be designed to have the transitions as fast as possible. Assuming that the IGCT output capacitance is negligible, the maximum snubber capacitance can be found by:

$$C_{snb,max} = \frac{i_{off} \cdot t_{dt} \cdot n}{4V_{dc}} \tag{7}$$

where i_{off} is the IGCT turn off current, t_{dt} is the dead-time, V_{dc} is the DC voltage and n the number of series connected IGCTs. Fig. 8b shows the relationship between the maximum capacitance value and turn-off current for different dead times. This plot shows the maximum capacitance value, for a given current to perform a safe ZVS. If this criterion is not fulfilled, the ZVS will be lost and extra losses due to partial shoot-through will appear [19].

In this way, knowing that the worst case scenario has a turn-off current of $I_{off} \approx 10$ A, a $C_{snb} = 20$ nF was selected to ensure the dynamic voltage balance of the stack. With this capacitance and this turn-off current, the dead time needs to be set as $\delta \geq 20$ μs, therefore, a $\delta = 25$ μs was used.

Fig. 9 shows the switching transition of the IGCTs using a $C_{snb} = 20$ nF snubber, for different turn-off currents. The blue waveform is the 5 kV, 5 kHz operation. For this case, it can be seen that the turn-off current is $I_{off} \approx 8$ A, which results in a transition time of 19μs. The voltage mismatch after the first IGCT is turned on is around 350 V. This experiment verified that the low turn-off current leads to a very slow transition, consequently, requiring a very conservative dead time. A dead

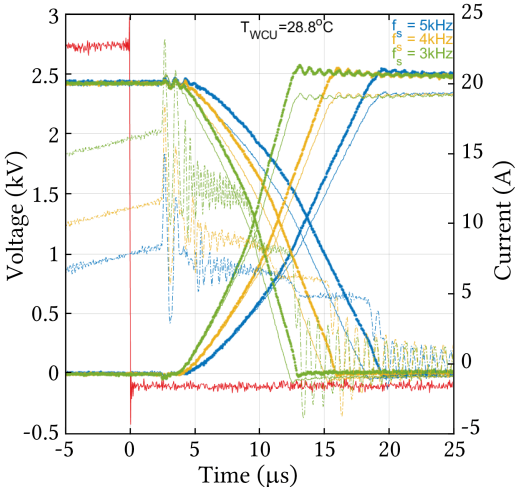


Fig. 9. Experimental waveforms for the 2L transition with a $C_{snb} = 20$ nF snubber, with different switching frequencies. The strong line represents the outer device (S_1 and S_4), and the light line the inner device (S_2 and S_3). The solid lines are the voltages over the IGCTs and the dash-dotted lines are the currents. The red pulse is the turn-off signal.

time of $\delta = 25$ μs consists of 12.5% of the switching period, which is not ideal for the converter operation.

Therefore, lower switching frequencies were tested to evaluate the switching transient with higher turn-off currents. The switching frequencies of $f_s = 4$ kHz and $f_s = 3$ kHz were tested and the experimental waveforms are also shown in Fig. 9, in yellow and green, respectively. For the case of $f_s = 4$ kHz the turn-off, the current is $I_{off} \approx 11$ A, resulting in approximately 16 μs for the transition, and a voltage imbalance of 300V. Lastly, for $f_s = 3$ kHz, the turn-off current is $I_{off} \approx 17$ A, and the transition period is 13μs. This operation led to a voltage imbalance of 250V.

As expected, with a lower switching frequency, which results in a higher turn-off current, and due to the value of magnetizing inductance, the transition duration is shorter. Further, a lower value of the snubber capacitor could be used in an attempt to speed up the transition even more. The minimum required capacitance value to achieve dynamic voltage balance is such that all IGCTs possess the same equivalent parallel capacitance, which includes the device output capacitance and snubber capacitance.

Finally, the dynamic voltage balancing with a C-snubber was validated for the no-load operation with the two 3L-NPC.

IV. MFT No-Load Experimental Validation

After validating the operation of the power stacks, a preliminary no-load test was conducted to evaluate the MFT thermal performances. Numerous thermocouples (TCs) were added to accessible locations within the core, windings, and oil vessels. The test schematic is shown in Fig. 10.

Fig. 11 shows the experimental results for a 12 h no-load DCT operation. The locations of the TCs measuring the air temperatures in the inner vessel cylinder are indicated

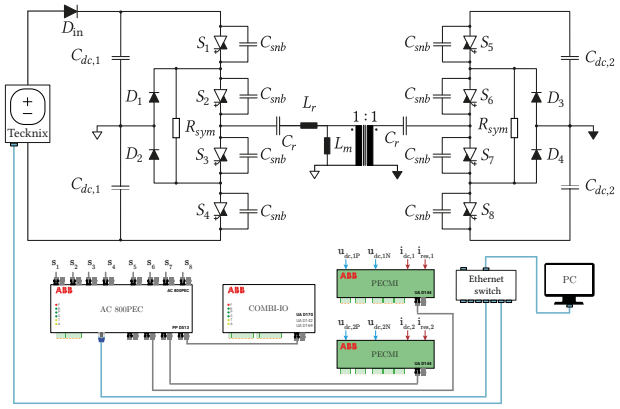


Fig. 10. Test setup for evaluating the no-load operation of the DCT.

in the top left corner of Fig. 11a. Temperature T_{out} shows the ambient temperature inside the closed DCT cabinet. As expected, the two air temperatures within the enclosed space between the vessel's inner walls and the core leg, top and bottom parts, $T_{ac,Lin}$ and $T_{ac,Rin}$ are the highest, whereas the other two temperatures, $T_{a,Lin}$ and $T_{ac,Rin}$, outside of the core, are notably lower. The discrepancy in values between the latter two temperatures is presumably due to the measurement uncertainty of the employed K-type TCs.

Various core temperatures are presented in Fig. 11b. Thereby, the letters in the subscript mark the location of the TC. It can be differentiated between F/B/R, front, back, and right, and T/B, which stands for top and bottom. In pairs, the following temperatures were observed with the help of attached TCs:

- $T_{c,FT}$ and $T_{c,FB}$: temperatures at the top and bottom of the frontal vertical core surface (the one facing the termination panel);
- $T_{c,BT}$ and $T_{c,BB}$: temperatures at the top and bottom of the back vertical core surface;
- $T_{c,F}$ and $T_{c,B}$: front and back core surface temperatures measured close to the air gap
- $T_{c,RT}$ and $T_{c,RB}$: temperatures measured 3 cm inside of the core (between two sets) at the top and bottom on the right core side;

It can be observed that the temperatures measured at the top tend to be higher than the ones measured at the bottom. This trend can be nicely followed for three location pairs, namely, at the front and back surfaces, as well as inside the core. As anticipated, the temperatures are higher within the core than on the surface, due to worse cooling conditions.

The notches that are visible in most of the core temperature measurements are due to seizing operation in half an hour intervals. This was done with the idea of observing the difference in measurements owing to the presence of a magnetic field during operation, which, depending on the location of the TCs can introduce errors due to induced voltages.

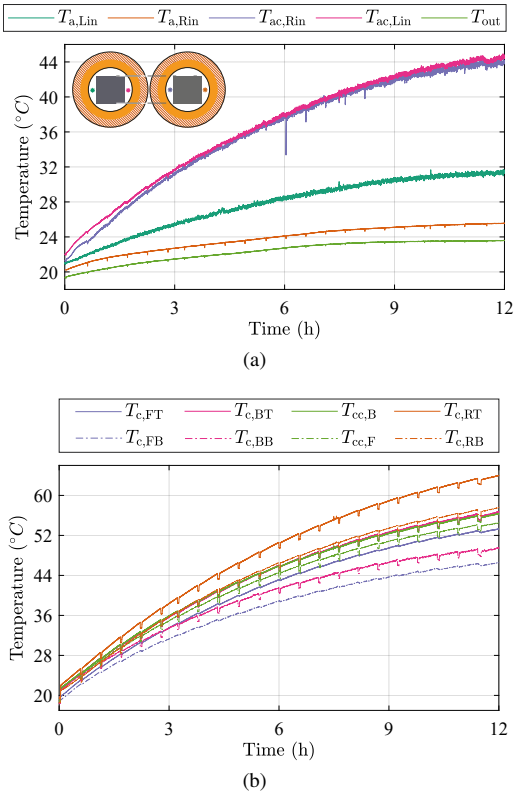


Fig. 11. Measured temperatures of (a) the air around and between the inner vessel walls and the core and (b) at the core surface and inside of the core.

Finally, with this test, the temperature of the core could be verified, proving that the air-cooling approach was well-designed and sufficient.

V. Conclusion

In this work, the performance of an IGCT-based split capacitor 3L-NPC DCT was evaluated, focusing on both static and dynamic voltage balancing. The first step involved calculating and experimentally validating the efficacy of the NPC symmetrizing resistor. This method, thanks to the NP clamping diodes, significantly reduces snubber losses compared to the conventional approach for series-connected IGCTs, which typically uses parallel resistor snubbers.

For the dynamic voltage balancing, a low capacitance value of the C-snubber was analyzed for the switching transient during the 2L operation of the 3L-NPC. Findings indicated that the low current levels result in slow switching transients, requiring a long dead time. This extended dead time consequently diminishes the effective pulse delivered to the resonant tank. These conditions led to further investigation into different switching frequencies, showing improved transients with higher turn-off currents, which could be an option for IGCT-based DCTs.

Finally, due to the ongoing integration and commissioning work, only preliminary results are included here, and full power tests will be subsequently reported.

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