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Le vent se lève,
il faut tenter de vivre.
—Paul Valéry

To my family.
To all my friends.
To this unforgettable and invaluable journey.

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Abstract

In the past decades, a significant increase of the transistor density on a chip has led to exponential growth in computational power driven by Moore's law. To overcome the bottleneck of traditional von-Neumann architecture in computational efficiency, efforts are being dedicated to the development of alternative architectures that can seamlessly integrate computation and memory, such as in-memory computing. However, it still remains challenging in a suitable material system to fully harness the potential of this architecture. A noteworthy direction in this pursuit is the exploration of large-area 2D circuits based on two-dimensional (2D) materials and their heterostructures, leveraging their extraordinary properties such as the nano-scale thickness, outstanding electrical properties, and mechanical robustness. This motivates this thesis work to develop a scalable method of 2D material synthesis and exploit them as a promising platform for next-generation electronic devices.

To this end, the first part of this thesis work explores the chemical vapor deposition (CVD) growth and electrical properties of individual TMDC materials. First, 2-inch wafer-scale monolayer MoS_2 film is synthesized on a sapphire substrate. Several growth parameters, like the usage of NaCl and the etching-gas (O_2 and H_2), are studied to achieve a continuous and uniform film with a high crystalline quality. The 2-inch MoS_2 film is then used as active channel material in in-memory computing devices and proved its potential to extend Moore's law. Second, large-area NbS_2 single crystals are synthesized by CVD method. The growth morphologies are studied by changing the amount of Nb precursor, growth temperature and H_2S :Ar ratio. Depending on the thickness of NbS_2, a transition takes place from a metallic 3R-phase to a superconducting 2H-phase. A Berezinskii-Kosterlitz-Thouless (BKT) superconducting transition is observed in the CVD-grown 2H-phase NbS_2 below the transition temperature (T_c) of 3 K, opening up new possibilities for scalable and practical applications of superconductors in electronic and quantum devices.

The second part of this thesis work focuses on developing synthesis method and studying the electrical properties of MoS_2-NbS_2 heterostructures. First, MoS_2-NbS_2 lateral heterostructures is grown by "one-step" MOCVD route with the monolayer MoS_2 substitutionally doped with Nb atoms, which results in a p-type transport performance. A high current on/off ratio of around 10^4 is observed in the heterojunction. By performing temperature-dependent electrical measurements, DFT and quantum transport simulations, the band structure through the NbS_2-

MoS_2 heterojunction is studied. Second, NbS_2-MoS_2 patterned heterostructures is produced by a “two-step” route, combining MOCVD and sulfurization. The heterojunction is used as an active channel material with novel 2D contacts to develop field-effect transistors, in-memory devices and wafer-scale 2D circuits. Compared to pristine MoS_2, the heterostructure performs a lower contact resistance and Schottky barrier height, resulting in a significant enhancement of the memory window and current on/off ratio. The synthesis of MoS_2-NbS_2 heterostructures enables the creation of tailored 2D materials with enhanced electrical properties, showcasing their potential to revolutionize electronic and quantum device technologies.

Key words : two-dimensional materials, transition metal dichalcogenides, molybdenum disulphide, niobium disulphide, metal-organic chemical vapor deposition, TMDC heterostructure, FET devices, floating-gate memories, 2D circuits, in-memory computing.

Résumé

Au cours des dernières décennies, l'augmentation significative de la densité des transistors sur les puces électroniques a conduit à une croissance exponentielle de la puissance de calcul conformément à la loi de Moore. Pour surmonter le manque d'efficacité de l'architecture traditionnelle de von Neumann en matière de calcul, des efforts sont consacrés au développement d'architectures alternatives qui peuvent pleinement intégrer le calcul et la mémoire, telles que l'informatique en mémoire. Cependant, il reste encore à trouver un système de matériau approprié pour exploiter pleinement le potentiel de cette architecture. L'exploration de circuits de grande surface basés sur des matériaux bidimensionnels (2D) et leurs hétérostructures, tirant parti de leurs propriétés extraordinaires telles que l'épaisseur nanométrique, les propriétés électriques exceptionnelles et la résistance mécanique, constitue une orientation importante dans ce domaine. Cette thèse est motivée par le développement d'une méthode évolutive de synthèse de matériaux 2D et leur exploitation comme plateforme prometteuse pour les dispositifs électroniques de prochaine génération.

À cette fin, la première partie de ce travail de thèse explore la croissance par dépôt chimique en phase vapeur (CVD) et les propriétés électriques de différents dichalcogénures de métaux de transition (TMDC). Tout d'abord, un film de MoS_2 monocouche à l'échelle d'une plaque de 2 pouces est synthétisé sur un substrat de saphir. Plusieurs paramètres de croissance, comme l'utilisation de NaCl et le gaz de gravure (O_2 et H_2), sont étudiés pour obtenir un film continu et uniforme de haute qualité cristalline. Le film de MoS_2 est ensuite utilisé comme matériau de canal actif dans les dispositifs de calcul en mémoire et a prouvé son potentiel pour prolonger la loi de Moore. Deuxièmement, des monocristaux de NbS_2 de large surface sont synthétisés avec la méthode CVD. Les morphologies de croissance sont étudiées en changeant la quantité de précurseur Nb, la température de croissance et le ratio H_2S :Ar. Une transition d'un polytype métallique 3R à un polytype supraconducteur 2H est observée en fonction de l'épaisseur de NbS_2. La transition supraconductrice Berezinskii-Kosterlitz-Thouless (BKT) se produit dans le NbS_2 en phase 2H obtenu par dépôt en phase vapeur en dessous de la température de transition T_c de 3 K, ce qui ouvre de nouvelles possibilités d'applications pratiques et évolutives des supraconducteurs dans les dispositifs électroniques et quantiques.

La deuxième partie de ce travail de thèse se concentre sur le développement d'une méthode de synthèse et l'étude des propriétés électriques des hétérostructures MoS_2-NbS_2. Tout d'abord,

les hétérostructures latérales MoS_2-NbS_2 sont produites par la méthode MOCVD en une seule étape, la monocouche MoS_2 étant dopée de manière substitutive avec des atomes de Nb, ce qui entraîne un comportement de transport de type p. L'hétérojonction présente une caractéristique de transfert de type p avec un rapport de courant on/off élevé d'environ 10^4. La structure de bande à travers l'hétérojonction MoS_2-NbS_2 est étudiée par des mesures électriques dépendant de la température, par DFT et par des simulations de transport quantique. Deuxièmement, des hétérostructures NbS_2-MoS_2 modelées par lithographie sont produites par une voie en deux étapes, combinant MOCVD et sulfuration. L'hétérojonction est utilisée comme matériau de canal actif avec de nouveaux contacts 2D pour développer des transistors à effet de champ, des dispositifs en mémoire et des circuits 2D à grande échelle. Par rapport au MoS_2 seul, l'hétérostructure présente une résistance de contact et une hauteur de barrière Schottky plus faibles, ce qui se traduit par une amélioration significative de la fenêtre de mémoire et du rapport entre les courants on/off. La synthèse des hétérostructures MoS_2-NbS_2 permet de créer des matériaux 2D sur mesure avec des propriétés électriques améliorées, démontrant leur potentiel pour révolutionner les technologies des dispositifs électroniques et quantiques.

Mots clefs : matériaux bidimensionnels, dichalcogénures de métaux de transition, disulfure de molybdène, disulfure de niobium, dépôt chimique en phase vapeur de composés organométalliques, hétérostructure TMDC, dispositifs FET, mémoires à grille flottante, circuits bidimensionnels, informatique en mémoire

Contents

Acknowledgements **i**

Abstract (English/Français) **v**

List of figures **xiii**

List of tables **xv**

1 Introduction **1**
1.1 Context and objectives of this work . . . 1
1.2 Outline of the thesis . . . 3

2 Van der Waals heterostructures based on 2D TMDCs **5**
2.1 Graphene and beyond . . . 5
2.1.1 Graphene . . . 5
2.1.2 Hexagonal boron nitride . . . 6
2.1.3 Black phosphorus . . . 6
2.1.4 Transition metal dichalcogenides . . . 7
2.1.5 2D oxides . . . 7
2.2 Two-dimensional transition metal dichalcogenides . . . 8
2.2.1 Crystal structure . . . 8
2.2.2 Electrical band structure . . . 9
2.3 Van der Waals heterostructures . . . 12
2.3.1 Improve performance of electronic devices . . . 13
2.3.2 Applications on optoelectronic devices . . . 13
2.3.3 Moiré patterns . . . 15
2.4 Synthesis routes of 2D TMDC heterostructures . . . 15
2.4.1 Exfoliation and heterostructure assembly . . . 17
2.4.2 Chemical vapor deposition . . . 18

3 Experimental techniques **27**
3.1 Introduction . . . 27
3.2 Material synthesis by MOCVD . . . 28
3.3 Material characterization . . . 29
3.3.1 Atomic force microscope . . . 29

3.3.2 Raman spectroscopy . . . 30
3.3.3 Photoluminescence spectroscopy . . . 31
3.3.4 X-ray photoelectron spectroscopy . . . 32
3.3.5 Aberration-corrected high-resolution scanning transmission electron microscopy . . . 33
3.3.6 Energy dispersive X-ray spectroscopy . . . 34
3.4 Device fabrication . . . 35
3.4.1 Device structures . . . 35
3.4.2 Transfer methods . . . 36
3.4.3 Photolithography . . . 38
3.4.4 Laser writer lithography . . . 39
3.4.5 Electron beam lithography . . . 40
3.4.6 Etching techniques . . . 40
3.4.7 Metal deposition and lift-off . . . 41
3.4.8 Atomic layer deposition . . . 42
3.5 Electrical measurements . . . 42
3.5.1 Electrical transport measurements . . . 42
3.5.2 Superconductivity measurements . . . 44
3.5.3 Memory characterization . . . 45

4 Wafer-scale monolayer MoS_2 grown by MOCVD 49
4.1 Introduction . . . 49
4.1.1 State of art: synthesis of 2D monolayer MoS_2 . . . 49
4.1.2 Outline of this chapter . . . 50
4.2 2-inch monolayer MoS_2 growth with tube furnace MOCVD . . . 50
4.2.1 Growth process . . . 50
4.2.2 Optimization of growth process . . . 52
4.2.3 Characterization of MOCVD-grown monolayer MoS_2 film . . . 55
4.3 Applications of MOCVD-grown monolayer MoS_2 . . . 56
4.3.1 Logic-in memories . . . 56
4.3.2 Artificial neural networks . . . 57
4.3.3 Vector–matrix multiplication processor . . . 59
4.4 Conclusion . . . 60

5 Superconducting 2D NbS_2 grown epitaxially by CVD 61
5.1 Introduction . . . 61
5.1.1 2D metallic TMDCs . . . 61
5.1.2 State of art: electrical properties and synthesis of 2D NbS_2 . . . 61
5.1.3 Outline of this chapter . . . 63
5.2 2D NbS_2 single crystals grown by CVD . . . 63
5.2.1 Growth process . . . 63
5.2.2 Growth morphologies under different conditions . . . 64
5.3 Thickness dependent phase transition of CVD-grown NbS_2 . . . 66

5.3.1 Correlation between phase transition and flake thickness 66
5.3.2 Electrical transport in 2D NbS_2 with different phase structures 68
5.4 Further studies and conclusion 70
5.4.1 Superconductivity of 2H-phase NbS_2 70
5.4.2 Conclusion 72

6 P-type doping in NbS_2-MoS_2 lateral heterostructures grown by MOCVD 73
6.1 Introduction 73
6.1.1 State of art: electrical properties and synthesis of p-type MoS_2 73
6.1.2 2D metal-semiconductor TMDC heterostructures 74
6.1.3 Outline of this chapter 74
6.2 2D NbS_2-MoS_2 lateral heterostructures grown by MOCVD 75
6.2.1 Growth process 75
6.2.2 Characterization of lateral heterostructures 76
6.3 P-type Nb-doped monolayer MoS_2 77
6.3.1 Characterizations of Nb doping in MoS_2 78
6.3.2 Electrical transport of monolayer MoS_2 doped with Nb 80
6.4 P-type NbS_2-MoS_2 heterojunctions 81
6.4.1 Atomistic and electronic structures of NbS_2-MoS_2 heterojunction 81
6.4.2 Transport properties of p-type NbS_2-MoS_2 heterojunctions 84
6.5 Further studies and conclusion 85
6.5.1 Schottky barrier height extraction 85
6.5.2 Conclusion 87

7 2D circuits enabled by patterning TMDC heterostructures 89
7.1 Introduction 89
7.1.1 2D materials: an ideal platform for in-memory computing 89
7.1.2 2D metal-semiconductor heterostructures: properties and synthesis . . 90
7.1.3 Outline of this chapter 90
7.2 Production of NbS_2-MoS_2 patterned heterostructures 91
7.2.1 Synthetic process 91
7.2.2 Optical characterizations 91
7.3 Electrical transport characterization of NbS_2-MoS_2 patterned heterostructures 93
7.3.1 Device structure 93
7.3.2 Transport behavior and Schottky barrier height extraction 94
7.4 Floating-gate memories based on NbS_2-MoS_2 patterned heterostructures . . . 95
7.4.1 Device structure 95
7.4.2 Memory device Programming 96
7.4.3 Retention time and endurance testing 97
7.5 Conclusion 99

8 Conclusion and outlook **101**
8.1 TMDC materials produced by MOCVD method 101
8.1.1 Summary of the results 101
8.1.2 Perspective for future research 102
8.2 TMDC heterostructures produced by CVD method 102
8.2.1 Summary of the results 102
8.2.2 Perspective for future research 103

Bibliography **105**

List of Abbreviations and Symbols **121**

List of Publications **127**

Curriculum Vitae **131**

List of Figures

2.1 A library of 2D materials 6
2.2 TMDC crystal structures 8
2.3 Electrical band structures of semiconducting TMDCs 10
2.4 Electrical band structures of metallic TMDCs 11
2.5 Production of van der Waals heterostructures 13
2.6 Optoelectronic applications of van der Waals heterostructures 14
2.7 Moiré patterns in van der Waals heterostructures 16
2.8 Mechanical exfoliation and assembly method to produce TMDC flakes and van der Waals heterostructures 17
2.9 A schematic illustration of chemical vapor deposition for TMDC thin layer. . . . 19
2.10 Lateral growth and epitaxial growth in CVD growth of TMDC. 20
2.11 Strategies to promote CVD growth of TMDCs. 22
2.12 Control of lateral and vertical heterostructure growth. 25
2.13 "One-step" and "two-step" growth route of TMDC heterostructures by CVD. . . 26

3.1 Schematic of the home-built MOCVD system for material synthesis 28
3.2 Material characterization techniques: AFM, Raman and PL 31
3.3 Material characterization techniques: XPS, STEM and EDS 33
3.4 Device structures employed for electrical characterizations 36
3.5 Process flow of material transfer via PMMA and water capillary 37
3.6 Process flow of material transfer assisted by PMMA and thermal-release tape . 38
3.7 Process flow of photolithography 39
3.8 Process flow of metal deposition and lift-off 41

4.1 Process flow of MOCVD growth of monolayer MoS_2 film 51
4.2 MoS_2 growth dependence of Mo precursors in MOCVD 52
4.3 Na-assisted MOCVD growth of MoS_2 film 53
4.4 Etching-gas confined MOCVD growth of MoS_2 film 54
4.5 Characterizations of MOCVD-grown monolayer MoS_2 film 55
4.6 Logic-in memory based on MOCVD-grown MoS_2 film 57
4.7 Artificial neural networks based on MOCVD-grown MoS_2 film 58
4.8 Vector–matrix multiplication processor based on MOCVD-grown MoS_2 film . . 59

5.1 Atomic structures of NbS_2 with different polytype stackings 62

5.2 Schematic illustration of CVD system for NbS_2 growth. 64
5.3 Optical micrographs of as-grown NbS_2 flakes under different growth conditions 65
5.4 AFM images of as-grown NbS_2 showing the growth direction 65
5.5 Thickness dependent phase transition of NbS_2 67
5.6 Transport properties of NbS_2 with different phases 69
5.7 Superconductivity in 2H-phase NbS_2 71

6.1 MOCVD growth process of NbS_2-MoS_2 lateral heterostructures 76
6.2 Characterization of NbS_2-MoS_2 lateral heterostructures 77
6.3 STEM and EDX analysis of Nb doped-MoS_2 79
6.4 Raman and PL spectrum of Nb doped-MoS_2 79
6.5 Electrical transport of Nb doped-MoS_2 80
6.6 QM modeling of the NbS_2-MoS_2 lateral heterostructure with Nb doping 81
6.7 Projected density of states of the Nb doped-MoS_2 interfaces 83
6.8 Transport properties of p-type NbS_2-MoS_2 heterojunction 84
6.9 Schottky barrier height extraction of Nb-doped NbS_2-MoS_2 heterojunction . . 86

7.1 Schematic illustration of process flow to produce NbS_2-MoS_2 patterned heterostructures 91
7.2 Optical characterizations of NbS_2-MoS_2 patterned heterostructures 92
7.3 Device structure of FET based on NbS_2-MoS_2 patterned heterostructures 93
7.4 Transport behavior and Schottky barrier extraction of NbS_2-MoS_2 patterned heterostructures 95
7.5 Device structure of floating-gate FET based on NbS_2-MoS_2 patterned heterostructures 96
7.6 Memory programming of floating-gate FET based on NbS_2-MoS_2 patterned heterostructures 97
7.7 Retention time and endurance testing of floating-gate FET based on NbS_2-MoS_2 patterned heterostructures 98

List of Tables

6.1 Work functions of the Nb doped-MoS_2 with different doping levels. 82

1 Introduction

1.1 Context and objectives of this work

Driven by Moore's law, the quantity of transistors integrated into a single chip is rapidly increasing every few years, resulting in an exponential growth in computational power in the past decades. Particularly, in recent years, the rapid development of emerging artificial intelligence technologies, such as machine learning and the Internet of Things, has been producing a substantial surge of unstructured data in digital systems, posing higher challenges to modern computing. However, digital computing systems still currently rely on the von Neumann architecture by using the separate processing unit and memory, requiring data to be constantly transferred between these components. This leads to higher energy expenses for computing, as well as increased latency due to the need for continuous data movement, causing a bottleneck in terms of computational speed and efficiency. Consequently, the exploration of a new generation of high-energy-efficient computing and storage architecture has become a pressing topic.

Nowadays, a novel architecture based on the integration of computation and storage, known as "compute-in-memory" architecture, is gradually gaining attention. This approach aims to perform computations directly within the memory devices by exploiting the Kirchhoff and Ohm laws, acting as accelerators for resource-demanding tasks like machine learning and signal processing algorithms. Despite various material platforms have been examined for in-memory computing, none has managed to overcome all the challenges involved in its realization. Therefore, the search for a suitable material platform for the development of scalable, reliable, and energy-efficient in-memory computing is still ongoing, to address the escalating demand for sustainable and resource-conscious technological solutions.

In this context, two-dimensional (2D) materials perform outstanding electrical and mechanical properties with nano-scale thickness, as well as the ability to enhance and tune properties by forming van der Waals heterostructures, which is considered as promising material platform for the next-generation electronic devices. Detailed introduction is available in **Chapter 2**. Although these 2D materials and their heterostructures can be obtained by mechanical

exfoliation and assembly, further industrial applications in scalable and integrated devices are hindered by a limited lateral size, random shape and thickness. Chemical vapor deposition (CVD) and its advanced versions (MOCVD, LPCVD, PECVD) have been explored to synthesize layered materials with a large area and controllable thickness, which makes it a versatile and crucial technique for synthesizing 2D materials and facilitating their industrial applications.

The overall goal of this thesis is to achieve large-area growth of TMDC materials and their heterostructures by CVD method, investigate their electrical properties through fabricating electronic devices, and further exploit them in integrated 2D circuits for in-memory computing applications. This doctoral thesis starts from the exploration of large-area growth of monolayer MoS_2 film on a 2-inch sapphire substrate, which will be further discussed in **Chapter 4**. Several growth parameters are studied to achieve the continuous and uniform growth of the film, and promote the crystalline quality examined by several characterization techniques. Collaborating with my colleague, Dr. Guilherme Migliato Marega, the 2-inch MoS_2 film is further applied in in-memory computing devices and proved its potential to extend Moore's law. Next, CVD growth of NbS_2 single crystals is investigated in **Chapter 5**, with a further characterization of its electrical properties and the superconductivity. In **Chapter 6**, "one-step" CVD growth of MoS_2-NbS_2 heterostructures is demonstrated with the monolayer MoS_2 substitutionally doped with Nb atoms, resulting in a p-type transport behavior, which is imperative for the development of complementary logic applications based on MoS_2. Furthermore, in **Chapter 7**, "two-step" growth of patterned MoS_2-NbS_2 heterostructures is explored by combining MOCVD and sulfurization, which provides a flexible and versatile approach to produce TMDC heterostructures used for wafer-scale integrated 2D circuits.

1.2 Outline of the thesis

This thesis is organized into seven main chapters, which aim to address the state-of-art of TMDC van der Waals heterostructures (**Chapter 2**), the experimental techniques (**Chapter 3**), and the research results (**Chapter 4-7**) as well as the general conclusions and outlook (**Chapter 8**). To provide a guideline of this doctoral thesis, the organizational structure of the thesis with their main topic in each chapter is briefly outlined in this section.

- **Chapter 2** gives a general introduction on two-dimensional (2D) transition metal dichalcogenides (TMDCs) and their van der Waals (vdw) heterostructures, which includes an overview of 2D material family, and a particular focus on the crystal structure, electrical band structure and applications of 2D TMDCs and their vdw heterostructures. Furthermore, a literature review on the synthesis methods of 2D TMDC materials and their heterostructures is provided to address the fundamental principles used in later chapters.

- **Chapter 3** presents a detailed information on the experimental techniques used in this thesis, including the material synthesis and characterization, device fabrication and electrical measurements.

- **Chapter 4** demonstrates the synthesis of 2-inch wafer-scale monolayer MoS_2 by MOCVD method and its applications in in-memory computing devices, including logic-in-memory device, artificial neural networks and vector–matrix multiplication processor. The results shown in this chapter were published in the following peer-reviewed papers:

  - Migliato Marega, G., Ji, H.G., Wang, Z.. Pasquale, G., Tripathi, M., Radenovic, A. & Kis, A. *A large-scale integrated vector–matrix multiplication processor based on monolayer molybdenum disulfide memories.* **Nature Electronics (2023)**, 6, 991–998.

  - Migliato Marega, G., Wang, Z., Paliy, M., Giusi, G., Strangio, S., Castiglione, F., Callegari, C., Tripathi, M., Radenovic, A., Iannaccone, G. & Kis, A. *Low-Power Artificial Neural Network Perceptron Based on Monolayer MoS_2.* **ACS Nano (2022)**, 16 (3), 3684–3694.

  - Migliato Marega, G. Zhao, Y., Avsar, A., Wang, Z., Tripathi, M., Radenovic, A. & Kis, A. *Logic-in-memory based on an atomically thin semiconductor.* **Nature (2020)**, 587 (7832), 72–77.

- **Chapter 5** demonstrates epitaxial CVD growth of 2D NbS_2 single crystals and continuous transition from a metallic 3R-polytype to superconducting 2H-polytype with respect to its thickness. The results shown in this chapter have been published in the following peer-reviewed paper:

  - Wang, Z., Cheon, C.Y., Tripathi, M., Migliato Marega, G., Zhao, Z., Ji, H.G., Macha, M., Radenovic, A., & Kis, A. *Superconducting 2D NbS_2 Grown Epitaxially by Chemical Vapor Deposition.* **ACS Nano (2021)**, 15 (11), 18403-18410.

- **Chapter 6** demonstrates the one-step simultaneous MOCVD synthesis of NbS_2-MoS_2 lateral heterostructures with p-type Nb substitutional doping of monolayer MoS_2. The results presented in this chapter were published in the following peer-reviewed paper:

  - Wang, Z., Tripathi, M., Golsanamlou, Z., Kumari, P., Lovarelli, G., Mazziotti, F., Logoteta, D., Fiori, G., Sementa, L., Migliato Marega, G., Ji, H.G., Zhao, Z., Radenovic, A., Iannaccone, G., Fortunelli, A. & Kis, A. *Substitutional p-Type Doping in NbS_2–MoS_2 Lateral Heterostructures Grown by MOCVD*. **Advanced Materials (2023)**, 35 (14), 2209371.

- **Chapter 7** demonstrates a two-step method, by combining MOCVD and sulfurization, to produce TMDC metal-semiconductor patterned heterostructures, and employ them in field-effect transistors, in-memory devices and 2D circuits. The results shown in this chapter produce the following to-be-submitted paper:

  -Wang, Z., Migliato Marega, G., Collete, E., Radenovic, A., & Kis, A. *Wafer-Scale Integrated 2D Circuits Enabled by Patterning TMDC Metal-Semiconductor Heterostructures.* **In preparation**.

- **Chapter 8** gives a summary of the results in this doctoral thesis and discusses further possibilities and challenges for next-generation electronic devices based on 2D TMDC heterostructures.

2 Van der Waals heterostructures based on 2D TMDCs

In this chapter, a general introduction will be given on two-dimensional (2D) transition metal dichalcogenides (TMDCs) and their van der Waals (vdw) heterostructures. Due to breadth and complexity of this field, it's hard to give a comprehensive description within this chapter. Thus, we will focus on the material systems and physical phenomena most relevant to this thesis work. First of all, a 2D material family will be introduced to show its evolution and state of development since the discovery of graphene. Afterwards, a literature review of 2D TMDCs and their vdw heterostructures will be provided in the next two sections, to discuss their structure, electrical properties and perspective of further applications. In the last section, synthesis routes to obtain 2D TMDCs and their heterostructures will be discussed to emphasize the motivation of this thesis work and highlight the principles used in the later chapters.

2.1 Graphene and beyond

2.1.1 Graphene

First discovered in 2004[1], graphene, a 2D material composed of a single layer of carbon atoms arranged in a honeycomb lattice[2], performs many extraordinary physical properties, such as outstanding mechanical robustness[3] and remarkable electrical conductivity[4]. In particular, due to its nature of zero-bandgap semi-metal[5], the charge carriers in graphene move ultra-fast, leading to a high mobility, which makes graphene a highly conductive 2D material and an essential component of many vdW heterostructures[6]. Additionally, graphene shows partial optical and electrostatic transparency with a tunable work function[7] because of its atomic thickness and finite density of states, making it a crucial platform to build complex vdW heterostructure devices. For instance, Bernal-stacked bilayer graphene, the simplest vdW heterostructure, with four pseudospin flavors, exhibits unique properties and allows the introduction of a bandgap when subjected to a vertical electric field[8]. In contrast, non-Bernal stacked bilayer graphene behaves like two individual monolayers[9], highlighting the nuanced character of layer interactions, which heavily relies on their stacking orientation.

In addition, graphane [10] and fluorographene [11], which is used as chemical alterations of graphene, can significantly impact the electronic properties by changing sp^2 hybridization into sp^3 tetrahedral bonds. Unfortunately, graphane is difficult to be used for making heterostructures because of it degrading, and only crystals of fluorographene with poor electronic performance have been reported so far.

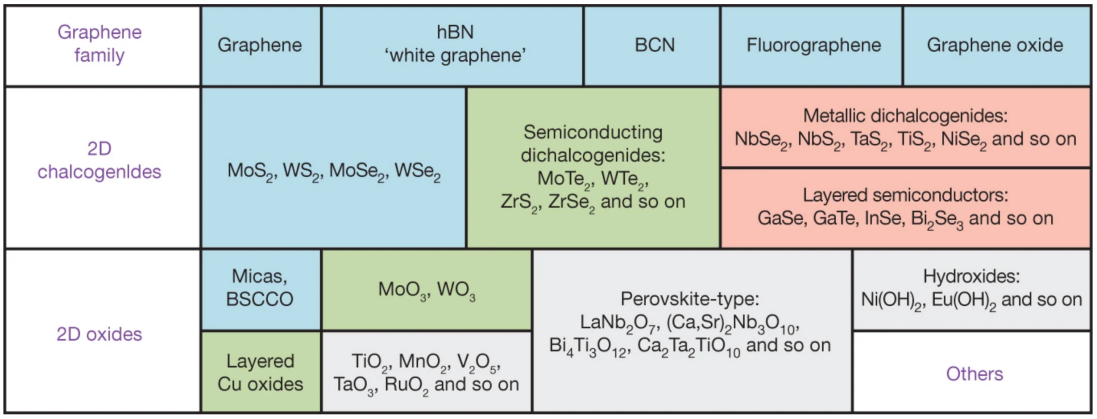

Figure 2.1: A library of 2D materials. The blue, green, and pink shaded regions mark out the air-stable, air-sensitive, and air-unstable materials. The gray shaded region marks out the materials which are successfully exfoliated from their bulk counterpart but lack further information. Reprinted with permission of Nature Publishing Group from ref. [12].

2.1.2 Hexagonal boron nitride

Hexagonal boron nitride (h-BN) is one of the member in 2D material family, which shows a hexagonal lattice arranged by boron and nitrogen atoms and is often referred to as "white graphene" due to the similar structure. In contrast to the high conductivity of graphene, h-BN behaves as a good insulator due to its intrinsic covalent bonding. Like other 2D materials, single or few layer h-BN can be also obtained by mechanical exfoliation from bulky crystals, making it widely used as ultra-flat insulating substrates[13], defect-free dielectrics and atomically thin tunnelling barriers[14]. Furthermore, h-BN shows high resistance on both mechanical manipulation and chemical interactions, which enables it an ideal material for sample encapsulation[9] with an atomically smooth surface free of dangling bonds and charge traps.

2.1.3 Black phosphorus

Black phosphorus is a semiconducting material which can be exfoliated into its 2D form as thin flakes or monolayer (phosphorene). Black phosphorus shows a layer dependent bandgap which can be tuned from 0.33 eV (bulk) to 1.5 eV (monolayer) as well as a high carrier mobility of up to 1000 $cm^2V^{-1}s^{-1}$ [15], [16], [17], which makes it a promising candidate for a platform in optoelectronic devices. Moreover, due to its orthorhombic and wavelike

structure, phosphorene displays highly anisotropic properties in both the optical and transport properties. For instance, it exhibits a lower optical absorption threshold for linearly polarized light along the armchair direction compared to the perpendicular direction[18]. Additionally, anisotropic properties in optical conductivity and Raman spectra have been noted[19], which provides a swift method for determining the lattice orientation of phosphorene.

2.1.4 Transition metal dichalcogenides

Transition metal dichalcogenides (TMDCs), the main class of materials studied in this thesis work, consist of a large array of layered materials which have the general chemical formula MX_2, where M represents a transition metal atom such as molybdenum (Mo), tungsten (W), or niobium (Nb), and X represents a chalcogen atom such as sulfur (S), selenium (Se), or tellurium (Te). They show a broad range of electronic properties, from insulating or semiconducting to metallic or semi-metallic, which arises from the progressive filling of the non-bonding d bands by the transition metal electrons [20]. In semiconducting TMDCs, such as MoS_2, $MoSe_2$, WS_2 and WSe_2, they display an indirect-to-direct bandgap transition with layer number decreasing from bulk to monolayer [21], [22], in the range of 1–2 eV with the measured carrier mobility generally in the order of 100 $cm^2V^{-1}s^{-1}$ at room temperature [23], [24], [25], [26]. In addition, these layered materials also show unusual electrical properties like valley polarization[27], [28], valley Hall effect [29], and superconductivity [30], [31], making these materials increasingly attractive. To fully investigate the properties of TMDC materials and employ them in industrial fields, several synthesis methods have been developed to obtain the thin flakes or even wafer-scale film of TMDCs, which will be further introduced in Section 2.4.

2.1.5 2D oxides

Apart from the 2D materials mentioned in above subsections, there is another group comprises numerous oxides, including lead oxide and lead salts (like PbO, $Pb_2O(SO_4)$, Na_2PbO_2), phosphorus oxides and phosphates, transition metal oxides (like MoO_3, WO_3), and perovskite-like crystals such as BSCCO and $Sr_2Nb_3O_{10}$ [32], [33], [34], [35]. In contrast to the majority of other 2D materials, the layers in 2D oxides are commonly connected by week covalent bonds, oxygen bridges, or intercalating elements, and are typically nonstoichiometric owing to the existence of oxygen vacancies[20]. Moreover, layered oxides typically exhibit a polycrystalline structure, which limits the crystal quality obtained by mechanical exfoliation methods. Most of the studies on 2D oxides are focused on their applications as battery cathode materials (Mo and V oxides) [36], superconductors (copper and cobalt layered oxides) [37], [38] and passivating layers (phosphorus oxide) [39], [40]. In addition, quantum confinement effects are expected to result in unique properties of 2D oxides compared to their 3D counterparts [41], including lower dielectric constants and larger bandgaps, and the potential for exhibiting charge density waves [42].

2.2 Two-dimensional transition metal dichalcogenides

2.2.1 Crystal structure

Transition metal dichalcogenides (TMDCs), the main material group studied in this thesis work, are one of the most important members in the family of 2D materials. As mentioned in subsection 2.1.4, they share the same chemical formula of MX_2, where M represents a transition metal atom (Mo, W, Nb, etc.) and X represents a chalcogen atom (S, Se, or Te). Up to now, different layered TMDC materials have been discovered, as presented in Figure 2.2a.

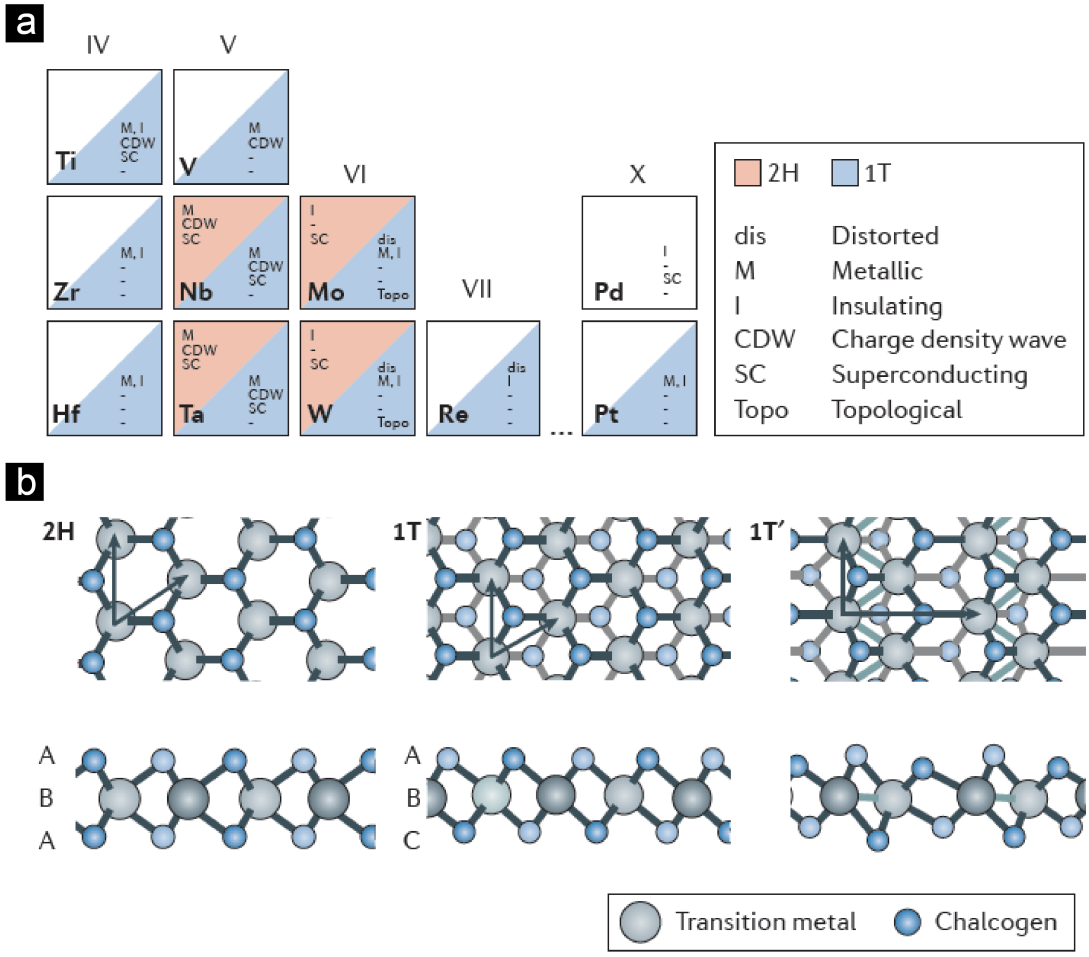

Figure 2.2: TMDC crystal structures. (a) Periodic table of known layered TMDCs, arranged based on the involved transition metal element, and marked with their existing structural phases and observed electronic phases. (b) Schematic of top and side views of single layers of TMDCs in their trigonal prismatic (2H), distorted octahedral (1T) and dimerized (1T') phases. Reprinted with permission from ref. [43].

Each individual layer of TMDCs is composed of one portion of metal atoms (M) and two portions of chalcogen (X) atoms, connected by a strong covalent bonding. These three-

atomic layers are stacked together by a weak van der Waals interaction in different stacking orders, resulting in different phase structures, as demonstrated in Figure 2.2b. The 2H phase exhibits an ABA stacking configuration, where chalcogen atoms locate at identical position A in different atomic layers and aligned on top of each other in the orthogonal direction. In comparison, the 1T phase displays an ABC stacking order, where chalcogen atoms in different atomic layers are not aligned. Depending on various TMDC materials, either the 2H or 1T phase can stably exist at room temperature. In addition, different crystal structures show distinctive electrical performance. For example, 3R-phase NbS_2 is metal, while 2H-phase NbS_2 shows superconductivity, which will be further discussed in this thesis work in Chapter 5.

2.2.2 Electrical band structure

Transition metal dichalcogenides (TMDCs) exhibit diverse electronic properties depending on their varied chemical compositions and structural phases, which results from the gradual occupation of the non-bonding d bands by the transition metal electrons [20]. TMDCs composed of group VI transition metals, such as molybdenum (Mo) and tungsten (W) combined with sulfur (S) and selenium (Se), usually behave as semiconductors in their thermodynamically stable 2H phase. When composed of group V transition metals, such as NbS_2, $NbSe_2$, TaS_2, these TMDCs show metallic behavior at room temperature.

Semiconducting TMDCs

In semiconducting TMDCs, one of their unique properties is indirect-to-direct band gap transition as shown in Figure 2.3a. In bulk or multilayer TMDCs, the conduction band minimum (CBM) is located halfway between the K and Γ points, while the valence band maximum (VBM) is located at the Γ point. When the layer number decreases, the interactions between bonding and anti-bonding states of out-of-plane L_z=0 orbitals from other layers are reduced [44], leading to a direct band gap transition at the K point in monolayer TMDCs. For example, both simulation and experimental results have observed an increased bandgap of MoS_2 with decreasing layer number [45], [21], [46], resulting in a higher photoluminescence intensity. Various layer numbers with varied band structures show significant different contrast under the dark field of an optical microscope, which helps to distinguish between monolayer and multilayer crystals during mechanical exfoliation. Moreover, this unique band structure offers monolayer TMDCs attractive optical properties, making them suitable for applications in optical or optoelectronic devices.

In addition, the absence of inversion symmetry in monolayer semiconducting 2H-TMDCs leads to a spin splitting of the electronic bands driven by the spin-orbit interaction. The degeneracy of the conduction and valence band extrema at points K and K' is lifted due to the lack of time-reversal invariant momenta. This effect is especially prominent in the valence band [48], which can be explained by the fact that the spin-orbit interaction is a relativistic effect which intensifies with the increasing mass of elements. The spin splitting of bands at K

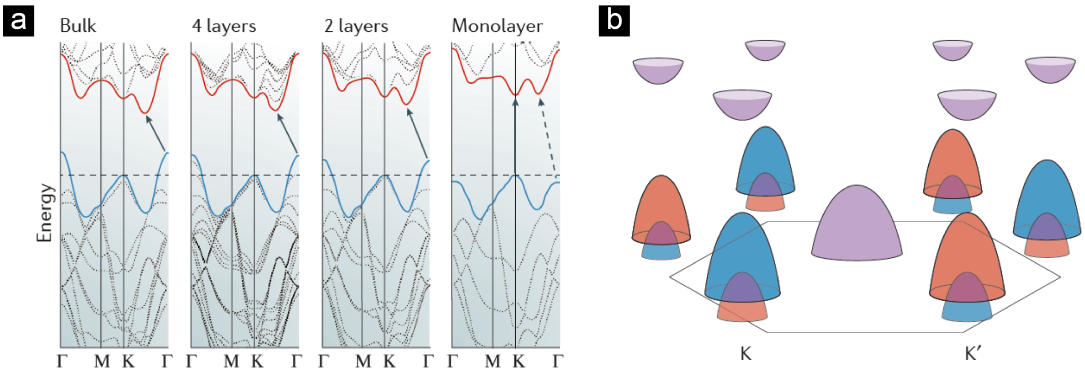

Figure 2.3: Electrical band structures of semiconducting TMDCs. (a) Simulation results of the band structure of 2H-MoS2 with a decreasing layer thickness. Reprinted with permission from ref. [45] (b) Schematic of the band structure of monolayer 2H-MoS_2, illustrating the spin splitting of the bands at the *K* and *K*' points on the corners of the Brillouin zone. Up and down spin polarization is presented by orange and blue colours, respectively. Reprinted with permission from ref. [47].

and *K*' is opposite due to time-reversal symmetry, resulting in a different energy for a specific spin orientation at the *K* and *K*' valleys [43]. The spin-valley coupling property of TMDCs is depicted in Figure 2.3b, indicating that the valley polarization of charge carriers automatically converts into their spin polarization [49]. This spin-valley locking effect of monolayer TMDCs, especially $MoSe_2$ and WSe_2 with a large spacing energy [48], makes them attractive in the applications of next-generation optoelectronic, spintronic and valleytronic devices [50], [51], [52], [53].

Metallic TMDCs

In addition to semiconducting TMDCs, some components of TMDCs exhibit metallic performance at room temperature. Most of these materials consist of transition metal atoms in V group, such as Nb and Ta, and the others are certain structural phases of VI group TMDCs, such as 1T'- and 2H-$MoTe_2$. The metallic properties of these TMDCs is attributed to a partially filled d-band of the transition metal atoms, which provides a high density of states near the Fermi level, leading to good electrical conductivity. The chalcogen atoms contribute to the electronic structure of the material through their p-orbitals, which hybridize with the d-orbitals of the transition metal atoms. The good conductivity and layered structure make metallic TMDCs an ideal 2D contact to reduce the contact resistance and improve the performance of electronic devices.

One of the interesting phenomena in metallic TMDCs is their charge density wave (CDW) phases, as presented in Figure 2.4, which relies heavily on the chemical composition and structural phase of the material. For example, according to first-principles calculations, monolayer 2H-$NbSe_2$ exhibits a charge-density wave (CDW) phase with a distinct periodicity of 4×1, in contrast to the $3 \times 3 \times 1$ periodicity observed in the bulk material [55], [54].

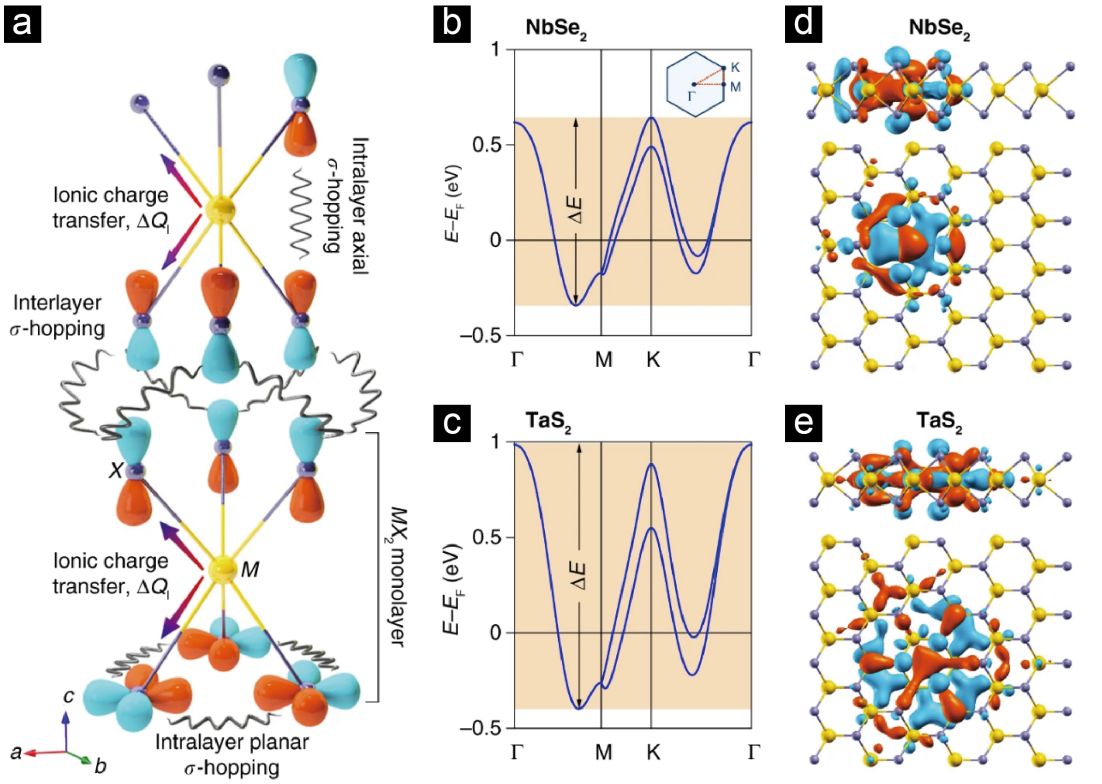

Figure 2.4: Electrical band structures of metallic TMDCs. (a) Schematic illustration showing the charge transfer channels, including intralayer ionic charge transfer, intralayer covalent bonding, and interlayer σ-hopping. (b, c) Electronic band structure of monolayer $NbSe_2$ and TaS_2 calculated by first-principles. The inset of (b): the Brillouin zone and its high syemmety k-points. (d, e) Side and top views of the computed real-space distributions of Wannier orbitals associated with the topmost valence bands in monolayer $NbSe_2$ and TaS_2. Positive regions of the electronic wave functions are schemed in orange and negative regions in blue, respectively. Reprinted with permission from ref. [54].

The calculation results further suggest that this monolayer CDW phase offers a larger gain in electronic energy, leading to a higher transition temperature. Experimental results also demonstrate a significant increase in the CDW transition temperature of 2H-$NbSe_2$ from bulk (T_{CDW} = 33 K) to monolayer (T_{CDW} = 145 K) [56]. Compared to 2H-$NbSe_2$, first-principles calculations for the isostructural 2H-$TaSe_2$ indicate the same periodicity of 3 × 3 for both bulk and monolayer forms [57]. Some other metallic TMDCs, like 2H and 1T phases of TaS_2, 1T-$TiSe_2$, also shows rich and diverse CDW performance [58], [54]. However, the underlying theory to fully explain the CDW behavior of TMDCs remains a challenging and complex area of research. For example, one of the most-known theory is driven by Fermi surface nesting [59], but ongoing debate is risen regarding its employment in TMDCs. Another mechanism has been proposed related to strong electron-phonon interactions with high values at the CDW wave vector [60], but it's far from reaching a consensus. Furthermore, the coexistence of CDW and superconductivity indicates that many-body effects play a crucial role in these

materials [20].

Another important behavior of metallic TMDCs is superconductivity. It is worth noting that almost all bulk TMDCs with a CDW state in their phase diagram also show superconductivity, such as the 2H phase of $NbSe_2$, TaS_2 and $TaSe_2$ [61], [62], [63], [64], except 2H-NbS_2, which displays superconductivity without CDW [65]. Moreover, the superconductivity of TMDCs persists in their 2D limit [43]. For example, monolayer 2H-$NbSe_2$ displays superconductivity with a critical temperature (T_c) of 3 K [66], which is lower than that of the bulk (T_c = 7 K). The superconductivity in 2D TMDCs can be explained by the interaction between spin–orbit coupling and Cooper pairing [67], [68]. The monolayer 2H phase of TMDCs exhibits spin splitting of the *K* and *K*' valleys, which can be considered as an out-of-plane Zeeman field. This spin-valley coupling is consistent with Cooper pairing, allowing for the existence of a superconducting state characterized by an Ising-like polarization of spins in the out-of-plane direction. However, due to the difficulty of synthesis and fast degrading rate in air, most work are done in theoretical side up to now, while 2D superconducting TMDCs still remain not fully studied in experimental side.

2.3 Van der Waals heterostructures

Due to the weak van der Waals interaction, 2D materials with few- to mono- layers can be obtained from their bulk crystals. Reversely, this interaction makes it possible to assemble individual layer structures in a desired order to construct synthetic materials. Currently, the most versatile method to construct van der Waals heterostructures is to mechanically stack individual layers on top of the others. Considering a large number of available 2D crystals, this method shows its advantages on creating a substantial variety of heterostructures without limit of lattice- or crystal orientation-matching. The interfaces obtained in this way are atomically flat and free of contamination [69] due to a "self-cleansing" mechanism [70]. To obtain heterostructures, there are also chemical methods by growing the components from bottom to top, such as chemical vapor deposition (CVD) and molecular beam epitaxy (MBE). Although limited by the lattice matching compared to mechanically stacking, these chemical methods offer several advantages: precise control over layer thickness, higher quality interfaces, larger area coverage and high scalability, which shows potential for industrial applications.

Due to the freedom of combining 2D materials and their various electronic properties, a numerous variety of layered structures with desired properties can be created, like insulating, semiconducting, conducting, superconducting and magnetic. In this section, we mainly focus on the electronic properties and applications of TMDC van der Waals heterostructures, while further discussion on their synthesis routes will be available in later section.

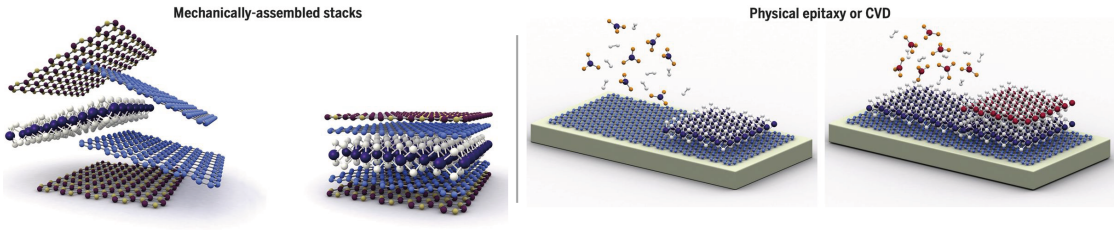

Figure 2.5: Production of van der Waals heterostructures. Schematic showing van der Waals heterostructures can be produced by mechanically assembled stacks (left) or large-scale growth method (right), like CVD and physical epitaxy. Reprinted with permission from ref. [20].

2.3.1 Improve performance of electronic devices

As mentioned as previous section, 2D semiconducting TMDCs have been widely used in electronic devices based on field-effect transistors due to their high carrier mobility and direct bandgap in monolayer. However, their performance is still subject to limitations imposed by both intrinsic and external factors. On one hand, the electrode contact induces surface states between the contact metal and semiconductor pinned close to the Fermi level, resulting in large contact resistances [71]. Intrinsically, the nature of 2D semiconductors which consist of atomic-scale thickness and pristine van der Waals surfaces poses challenges in minimizing contact resistance and fabricating ideal metal-semiconductor junctions with traditional 3D metals. [20]. Recent theoretical calculations [6] and experiment results [72], [73] have shown that Fermi level pinning can be weakened by 2D metal-semiconductor junctions. By introducing 2D contact, the Schottky barrier can be tuned and these heterostructures exhibit lower contact resistance and improved performance compared to conventional 3D metal-semiconductor contacts. Moreover, precise control of the metal-TMDC interface and the doping level of the TMDC material can further enhance the performance of the resulting devices. For instance, the doping level of TMDCs can be adjusted by doping with impurities or by gating to achieve the desired electronic properties [74]. On the other hand, the encapsulation of TMDCs in h-BN has proven to be a practical method to explore their intrinsic properties. Thanks to the air-tight encapsulation with atomically smooth surface, the utilization of h-BN prevents the 2D materials from oxidization and degrading [75], as well as environmental or substrate-induced disorders [76], thereby increasing transport mobility [77] and reducing optical linewidths [78].

2.3.2 Applications on optoelectronic devices

Due to their unique properties, such as layer-dependent band structure and strong light-matter interaction, TMDCs and their heterostructures have arisen increasing attention to develop the next-generation optoelectronic devices. Although optoelectronic applications of TMDC heterostructures are not our main topic in this thesis work, here we would like to give a listing summary on it to highlight the potential of TMDC heterostructures.

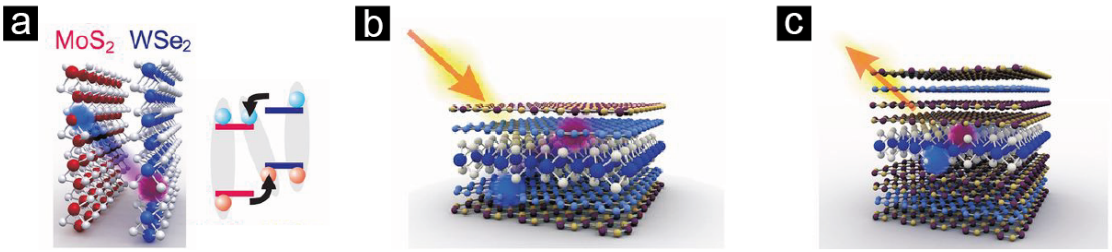

Figure 2.6: Optoelectronic applications of van der Waals heterostructures. (a) Indirect excitons observed in a MoS_2/WSe_2 heterostructure, where photoexcited electrons from WSe_2 are gathered in MoS_2, and photoexcited holes from MoS_2 are gathered in WSe_2. (b-c) TMDC heterostructures designed for photovoltaic applications and light-emitting diodes, respectively. Reprinted with permission from ref. [20].

- **Photodetector.** Photodetectors based on TMDC heterostructures have attracted significant attention in recent years due to their high sensitivity, fast response time, and broad spectral range [33]. One of the advantages of TMDC heterostructures is their large density of states [79], which leads to a high absorption coefficient and a high photodetection efficiency. Moreover, the layer-dependent band structure [21] of TMDCs enables precise control over the spectral response of these devices. By stacking different TMDCs with complementary band gaps, a broad spectral range can be covered, from visible to near-infrared wavelengths [80].

- **Exciton device.** Exciton devices built by TMDC heterostructures have shown extraordinary properties in optoelectronic field, including long lifetime, large binding energy, and high quantum efficiency [81]. Indirect excitons can be realized by combining TMDCs with different work functions, such as MoS_2/WSe_2 [82] and $MoSe_2/WSe_2$ [28], [83] heterostructures, leading to the accumulation of photoexcited electrons and holes in different layers. Such excitons usually have long lifetimes [83], with a tunable binding energy by changing the layer distance of semiconductors. In addition, by using p- and n-doped materials, atomically sharp p-n junctions can be created [84], which significantly enhances quantum efficiency by a fast carrier separation.

- **Light-emitting diode.** A vertical heterostructure consisting of a monolayer TMDC sandwiched between highly conductive transparent electrodes can serve as an efficient light-emitting diode (LED) device. In this arrangement, charge carriers are injected from the electrodes directly into the 2D material, avoiding the need for synthesizing p- and n-type materials in traditional LEDs [20]. To enhance the radiative recombination of electrons and holes in TMDCs, two to three layers of h-BN are usually used as additional tunnel barriers to increase the dwell time of the carriers [85]. Additionally, by controlling the interlayer distance and band alignment of the TMDCs, the emission wavelength can be precisely tuned [85], making it a promising platform for tunable LEDs.

2.3.3 Moiré patterns

2D TMDC layers can be easily stacked vertically to form heterostructures due to their van der Waals interaction, which offers a new degree of freedom in the form of the twist angle. When overlaying two layers of periodic lattice structures with a slight difference, a new intricate periodic pattern is created, called moiré pattern, as can be seen in Figure 2.7a.

The difference can come from the slightly mismatched lattice constant δ or a twist angle θ between their crystallographic axes. By adjusting lattice constants and the orientations, it allows precise control over the moiré pattern's characteristics, including its periodicity and symmetry.

The properties of the moiré pattern can be dramatically different from the individual layer, which is due to the significantly modified electronic dispersion by the moiré-induced periodic potential. For example, strongly correlated phenomena, including topological insulating phases [89], magnetism [90], [91] and superconductivity [92], [93], [94], can be induced or modulated by the delicate tuning of moiré-induced effects. Furthermore, moiré patterns is increasingly attractive to explore their applications of moiré excitons in quantum materials and nanoelectronics. The moiré excitons are the excitons trapped in the moiré potential minimum, which shows lower kinetic energy than the moiré potential. Notably, they show energy scales that are distinguishable from the typical intralayer or interlayer excitons observed in 2D materials. It has been demonstrated by reproducing the Hubbard model in 2D with moiré-trapped interlayer excitons [95] that quantum simulators can be realized by creating superlattices with tailored properties, enabling the creation of quantum dots [96], valleytronic devices [97], and even new platforms for quantum computation [98]. The periodic potential wells created by the moiré can act as an array of localizing wells for single carriers and excitons, which offers prospects for the development of novel optoelectronic devices with tailored functionalities [99].

2.4 Synthesis routes of 2D TMDC heterostructures

To further characterize the novel properties of 2D TMDC heterostructures and propel their utilization in next-generation electronic and optoelectronic devices as discussed in previous sections, it is crucial to develop a robust synthesis approach to produce TMDC heterostructures with a controllable and scalable manner, which strongly depends on a large-scale production of individual TMDC layers. Nowadays, two types of synthesis routes are mainly used in the 2D materials, the top-down method (exfoliation [1]) and the bottom-up method (such as chemical vapor deposition (CVD) [100], physical vapor deposition (PVD) [101], molecular-beam epitaxy (MBE) [102]). Among all these methods, mechanical exfoliation stands out as the easiest and widely used for different materials, while CVD method is considered as the most promising for industrial applications because of its large-scale produciblity and high controllability. In this section, the two most common used methods for synthesizing TMDC heterostructures will be discussed. Firstly, mechanical exfoliation and assembly method will be briefly introduced to

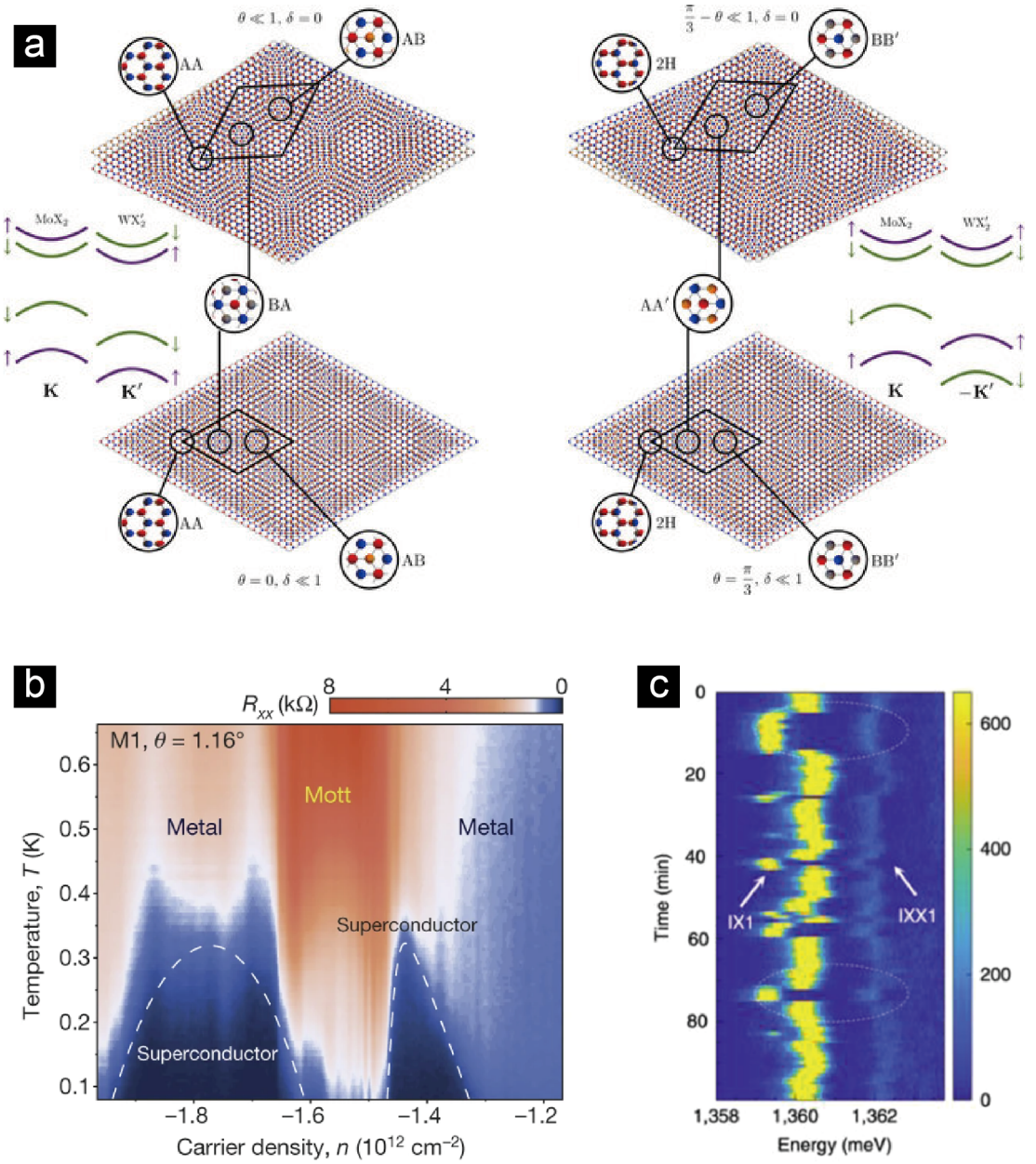

Figure 2.7: Moiré patterns in van der Waals heterostructures. (a) Moiré patterns formed by TMDC bilayers and band alignment. Reprinted with permission from ref. [86]. (b) Superconducting and insulating regimes in twisted bilayers of graphene. Reprinted with permission from ref. [87]. (c) Time-resolved PL emission of localized interlayer excitons and biexcitons in $MoSe_2/WSe_2$ heterobilayer. Reprinted with permission from ref. [88].

address their advantages and disadvantages compared to CVD and MOCVD method. Subsequently, we will focus on the CVD and MOCVD method which is mostly relevant to this thesis work, discussing about its growth mechanism and recent progresses about the acquisition of high-quality large-area TMDC crystals and heterostructures.

2.4.1 Exfoliation and heterostructure assembly

Exfoliation

To produce TMDC heterostructures, individual layers should be first obtained by exfoliation method from their bulky crystals, which was used to isolate the very first graphene samples [1]. The mechanism of exfoliation method is simple: by using mechanical forces or specific chemical reagents, a bulk crystal is easily decomposed in thin flakes with different thickness (down to single layer), due to the weakly van der Waals interactions between neighboring layers. The bulk crystals used for exfoliation can be natural minerals (such as graphite and MoS_2), or synthetic grown crystals (such as WSe_2 and $MoSe_2$). The process of mechanical exfoliation is shown in Figure 2.8a and can be explained as follows: Firstly, a piece of clean and sticky tape is gently pressed onto the surface of the TMDC crystal, peeling off a few thin flakes of the TMDC crystal. To get further thinner flakes (few layers or even single layer), the tape can be folded onto the clean regions and peeled off for several times. Afterwards, the exfoliated TMDC layer is then carefully transferred onto the target substrate by pressing down the tape and slowly striping off. The thin flakes obtained by mechanical exfoliation method usually maintain a high crystal quality similar as their bulk counterpart, thus making it the primary way for proof-of-concept and fundamental studies of the intrinsic properties of pristine TMDCs.

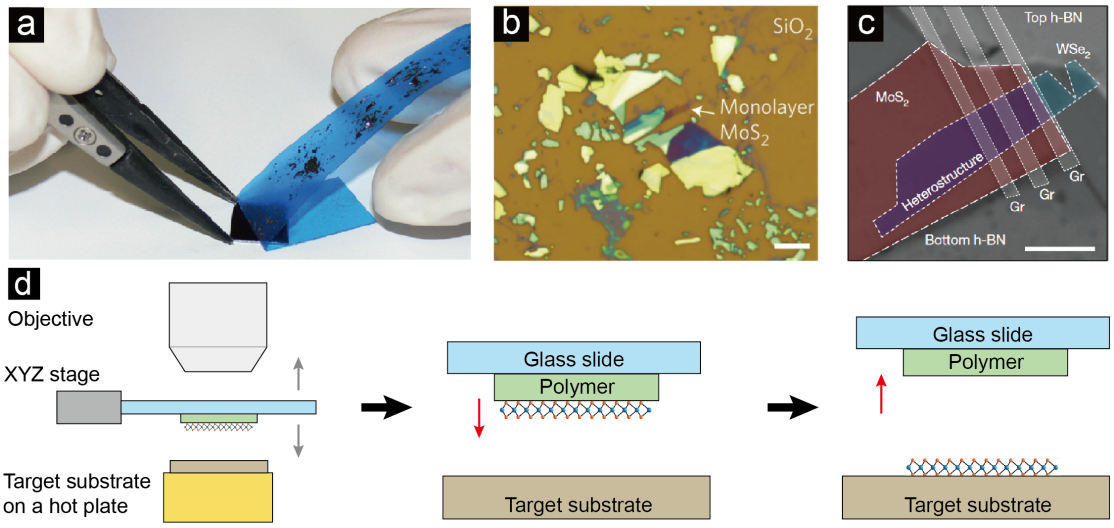

Figure 2.8: Mechanical exfoliation and assembly method to produce TMDC flakes and van der Waals heterostructures. (a) The process of mechanical exfoliation showing the step of removing tape and peeling off excess bulk materials, leaving TMDC thin flakes on the target substrate. (b) Optical microscope image of MoS_2 crystals on SiO_2 substrate, produced by mechanical exfoliation method. Scale bar: 10 μm. Reprinted with permission from ref. [103]. (c) Optical microscope image of h-BN/MoS_2/WSe_2/h-BN heterostructure produced by mechanical exfoliation method. Scale bar: 5 μm. Reprinted with permission from ref. [104]. (d) Graphic representation of the individual steps of the transfer method based on PDMS.

However, as demonstrated in Figure 2.8b, a random collection of MoS_2 flakes with various thickness are produced by this method, with only a minimal part of them being monolayers. Therefore, the main disadvantage of this method lies in the small size, random shapes, low yield, and uncontrollable thickness of the flakes. Some attempts have been tried to improve the yield and reproducibility of this technique. For example, gold-assisted exfoliation [105], [106] has been developed by using forma bond of gold atoms with the topmost layer of material which is stronger than the van der Waals interactions inside the material, allowing selective peel-off of the topmost layer. The size of the gold-assisted exfoliated flakes can reach up to few millimetres. Nevertheless, the technique is slow and not scalable for large scale production, which significantly limits its further application in industry.

Heterostructure assembly

As the inverse process of material exfoliation, van der Waals heterostructures can be obtained through the stacking of different monolayers. This approach provides significant flexibility for combining diverse compounds and creating varied heterostructures, given the absence of constraints associated with lattice matching and epitaxial growth alignment. Owing to the superior flexibility and high quality of exfoliated monolayers, assembly remains the predominant method for acquiring TMDC heterostructures in contemporary research studies. However, it is challenging to achieve a clean interface due to the residues during the transfer process. Additionally, the fabrication of lateral heterostructures still remains a significant obstacle, primarily attributed to the specific lattice alignment requirements. The limitations associated with the random shape and small size of exfoliated flakes further constrain the heterostructures obtained through this assembly method, as discussed in the "Exfoliation" subsection.

Over the years, several techniques have been reported for assembling monolayer flakes into heterostructures, and the most common one is transfer technique. Since this approach is not our main focus in this thesis, a brief explanation will be provided to introduce the main idea. To stack monolayer flakes precisely on top of each other and obtain vertical heterostructures, a microscope is placed on the topmost of the transfer setup to check the flake position and make sure a precise alignment. Then a substrate carrying the flake with polymer film for transfer can be aligned on top of the target substrate, and moved down slowly until attaching to the target. Finally, the flake sticks to the target and the empty polymer film is removed. A schematic is shown in Figure 2.8d.

2.4.2 Chemical vapor deposition

As discussed in the previous subsection, although TMDC thin flakes and their heterostructures can be obtained by mechanical exfoliation and assembly, further application in industry is limited by the small size, random shapes, and non-scalable production method. In comparison, chemical vapor deposition (CVD) and its advanced version, metal-organic chemical vapor deposition (MOCVD) are considered as a scalable method to grow TMDC materials and their

heterostructures with a high crystalline quality and controllable layer number. To address more clearly, this subsection will first give an overall explanation on the growth configuration and growth optimization of single material growth, and then focus on the technique and mechanism of achieving TMDC heterostructures.

2.4.2.1 Single TMDC layer growth

Growth configuration and mechanism

Taking CVD growth of MoS_2 thin layer as an example, Figure 2.9 demonstrates the configuration of growth process in a hot-wall tube furnace. The two precursors, MoO_3 powder and sulfur powder, are placed in Zone 1 of the tube furnace and evaporated at a temperature. Then the precursors are mixed thoroughly and carried into Zone 2 of the tube furnace by carrier gas, where chemical reactions take place and the product deposits on the surface of the substrate. The above chemical reactions can be described as the following formula:

$$MoO_3(s) + S(s) \rightarrow MoO_{(3\text{-}x)}(s) + SO_x(g) \tag{2.1}$$

$$MoO_{(3\text{-}x)}(s) + S(s) \rightarrow MoS_2(s) \tag{2.2}$$

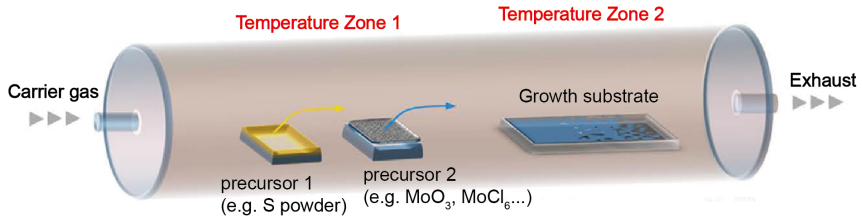

Figure 2.9: A schematic illustration of chemical vapor deposition for TMDC thin layer. The CVD setup includes a hot-wall tube furnace with two temperature zones, one for heating up and evaporating the precursors, and the other for reaching the growth temperature. Reprinted with permission from ref. [107].

Although CVD has become the most common method to synthesize large-area TMDC thin layer, there is still some limitations for further scalable applications because of the powder-based growth configuration. For example, the evaporation rate of the powder precursors varies when the growth process goes on, causing a non-stable precursor supply. In addition, variations in the distance between the source and substrates can lead to differences in nucleation density, resulting in non-uniformity on a wafer scale. To solve this problem, metal-organic

chemical vapor deposition (MOCVD) is employed by using gaseous precursors, allowing for a stable precursor supply by controlling the gas flow. Accordingly, the precursors of MOCVD growth of MoS_2 film can be the vapor phase $Mo(CO)_6$ and H_2S or diethyl sulfide ($(C_2H_5)_2S$). The gaseous precursors are carried into the tube furnace directly, decompose to MoO_x and S, and have chemical reaction at high temperature, resulting in a uniform deposition of the product on the substrate.

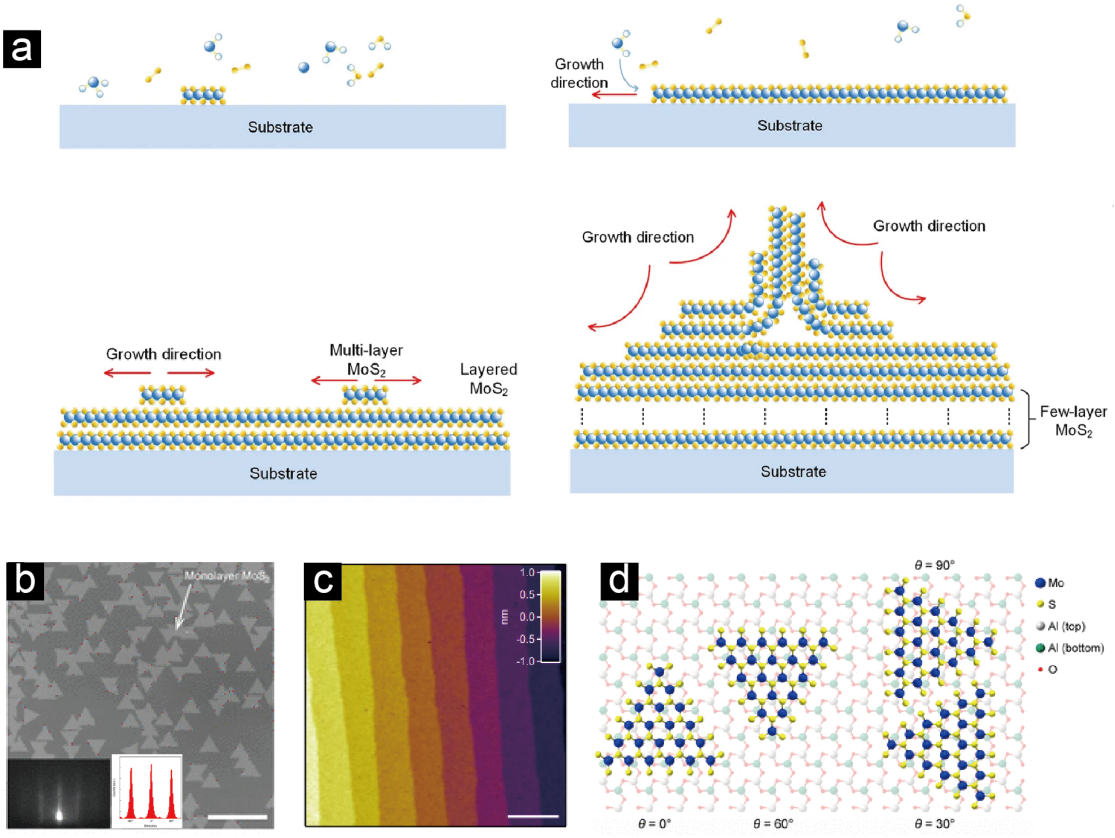

Figure 2.10: Lateral growth and epitaxial growth in CVD growth of TMDC. (a) Illustration for the nucleation stage and crystal growth stage in CVD growth of TMDC, as well as two different growth directions: lateral growth and vertical growth. (b) Optical microscopy image showing as-grown monolayer MoS_2 grains on the sapphire, with the corresponding reflection high-energy electron diffraction (RHEED) pattern and orientation histogram shown in the insets. The scale bar: 50 μm. (c) AFM image showing an atomically smooth terrace on the sapphire surface after annealing in air. (d) Schematic illustration of the lattice match between the MoS_2 crystals and the underlying sapphire substrate, controlling an epitaxial growth. Reprinted with permission from ref. [108] and [74].

In general, CVD or MOCVD process can be comprised as the following two stages: the nucleation stage and the crystal growth stage. In the first stage, as shown in the top-left panel of Figure 2.10a, the intermediate or reaction products, such as $MoO_{(3-x)}$ or gaseous MoS_2 are absorbed and diffuse on the substrate, initiating the formation of nucleation centers. At

these nucleation sites, atoms or molecules from the precursors come together to form small clusters of MoS_2. With additional precursor supply, nucleation density increases all over the substrate, which is related to the vapor concentration of two precursors and the gas flow rate. Following nucleation, the crystal growth stage involves the expansion of the initially formed MoS_2 islands. During this stage, additional precursor molecules continue to adsorb onto the existing nuclei, leading to the elongation and coalescence of MoS_2 domains. The lateral growth (top-right panel of Figure 2.10)occurs in a direction parallel to the substrate surface, resulting in the enlargement of the MoS_2 flakes, whereas vertical growth (bottom-right panel of Figure 2.10) occurs atop each layer, contributing to an increased thickness. The lateral or vertical growth process depends on energetically favorable positions and may be influenced by factors such as temperature, precursor concentrations, and the choice of substrate. Control over these parameters is essential for achieving uniform and large-area coverage of MoS_2 during the lateral growth stage.

In addition to maintaining a lateral growth, epitaxy also plays a crucial role in achieving large-area MoS_2 film with improved electronic and structural properties, which guides crystal orientation towards a singular direction and minimizes the adverse effects arising from grain boundaries. It has been reported that highly aligned MoS_2 flakes can be grown on an atomically flat sapphire substrate [74] achieved by pre-annealing process (the as-grown MoS_2 flakes and the terrace steps are shown in Figure 2.10 b and c, respectively), which is attributed to a favorable lattice alignment between the substrate and MoS_2 induced by the the strong van der Waals interaction (schematic illustrated in Figure 2.10d). Moreover, temperature serves as a critical factor in epitaxial growth on the kinetics of the process. Specifically, it governs the energy available to the crystals, enabling them to undergo rotational motions and ultimately attain the lowest energy state. This thermal energy plays a pivotal role in dictating the speed and efficiency of crystal formation, ensuring that the crystals align with the substrate lattice during epitaxial growth.

Strategies to promote CVD growth of TMDCs

In the synthesis of TMDC materials through CVD or MOCVD methods, various strategies have been explored to enhance the lateral size of TMDC single crystals and achieve uniform growth of monolayer continuous films. For example, researchers have utilized alkali metal halides (e.g. NaCl, KI) to promote the crystal growth of monolayer TMDCs, which is reported to efficiently suppress nucleation [109] and enhance the lateral growth of single domains. Moreover, alkali metal halides also serve as catalysts to enhance the efficiency and speed of TMDC growth in CVD processes. As demonstrated by DFT-calculated energy diagrams shown in Figure 2.11a, the highest energy barrier for chemical reactions is reduced from 0.53 to 0.29 eV by introducing Na as a growth promoter [22], which allows for a substantial decrease in growth temperature. Additionally, halide elements (F, Cl, Br, and I) induce further catalytic reactions, forming intermediate products like MoO_2Cl_2, which also attributes to the decrease of the required energy barrier and reaction temperature.

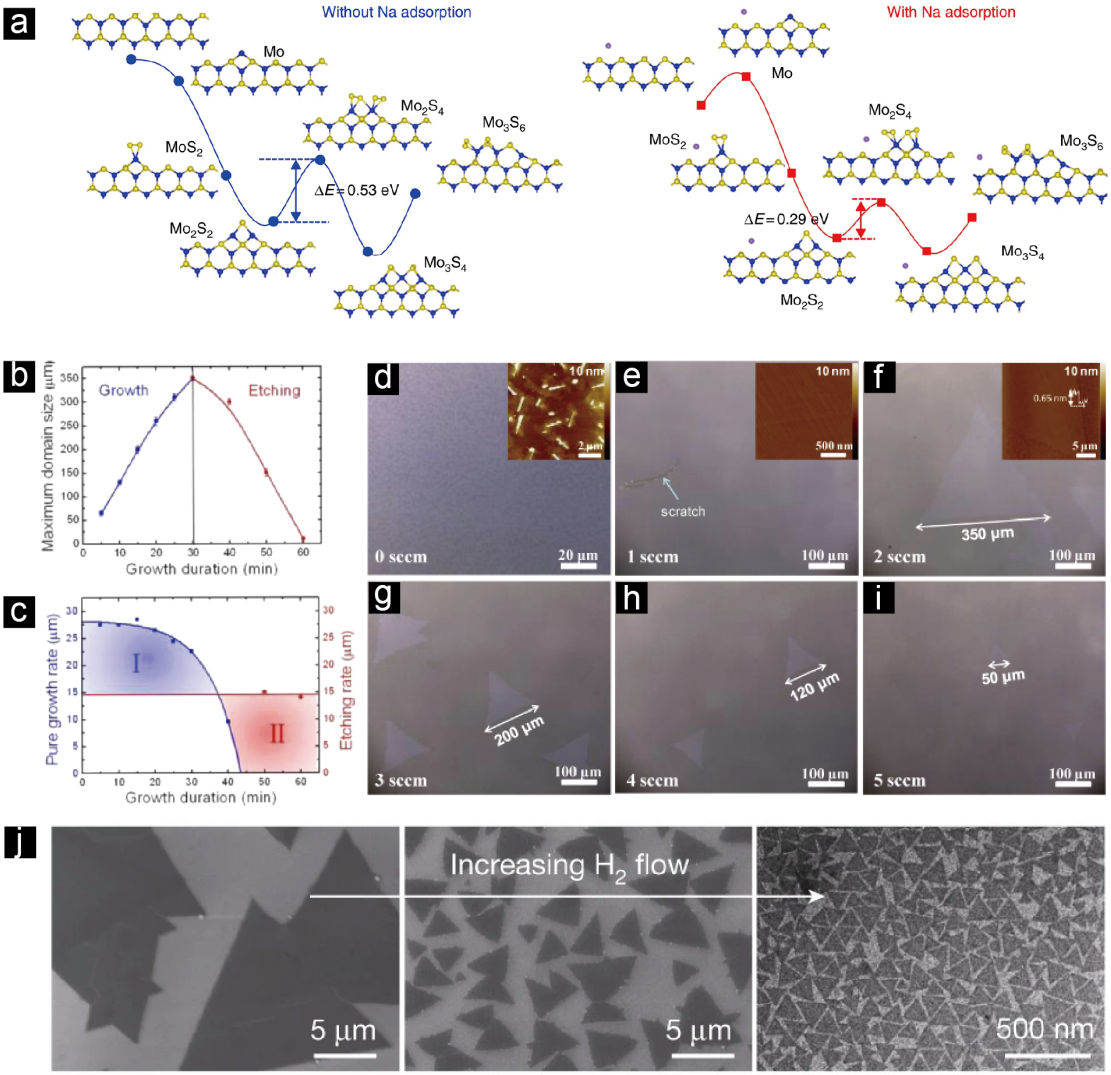

Figure 2.11: Strategies to promote CVD growth of TMDCs. (a) DFT-calculated energy diagrams for MoS_2 growth, indicating a lower highest energy barrier with Na absorption. (b) Evolution of the size of single-crystal MoS_2 domains as a function of the growth duration with effect of oxygen. (c) Dependence of pure growth rate and etching rate of MoS_2 domains on the growth duration with effect of oxygen. (d-f) Optical images of MoS_2 grown on sapphire for 30 min with O_2 flow rate ranging from 0 to 5 sccm. (j) Grain size variation of monolayer MoS_2 depending on the hydrogen flow rate. Reprinted with permission from ref. [22], [110] and [111].

In addition, oxygen and hydrogen gases are also utilized to promote the CVD growth of TMDC monolayers. As shown in Figure 2.11b-f, a small amount of O_2 allows for a significant enhancement in the grain size. O_2 assists as a chemical etchant to reduce nucleation density by removing unsteady nuclei, and also prevents poisoning effect of the MoO_3 precursor to ensure a high chemical activity. However, as can be seen in Figure 2.11b, c, and g-i, an

excessive amount of O_2 or exposure time may over-etch the as-grown crystals, resulting in a reduced crystal size. Similarly, a small amount of H_2 helps to eliminate carbon contamination generated during the growth process by reacting with carbon to form organic gases and accelerates the growth of MoS_2 by promoting the vaporization of precursors during CVD growth. However, a discernible trend emerges when the gas flow is further increased, indicating a pronounced decrease in monolayer MoS_2 size and the emergence of bilayer MoS_2 (shown in Figure 2.11j). This can be attributed to the dual effects of H_2. On one hand, as a chemical reducing gas, H_2 exerts desulfurization and etching effects on MoS_2 flakes, resulting in a diminished domain size. On the other hand, the primary reactant, MoO_x, can undergo further reduction to elemental Mo by H_2, which does not readily react with S and is consequently deposited directly onto the substrate, impeding lateral growth and leading to the growth of multilayered MoS_2 flakes instead of monolayers. Therefore, a careful trade-off needs to be explored to find the optimal flow rate of O_2 or H_2.

2.4.2.2 TMDC heterostructure growth

Control of lateral and vertical heterostructure growth

Based on the arrangements of the different layers, TMDC heterostructures are classified as lateral (in-plane direction) and vertical heterostructures (stacked on top of each other). Both lateral and vertical TMDC heterostructures offer a platform for designing materials with enhanced and tunable properties, enabling the development of novel electronic and optoelectronic devices. Thus, it is essential to understand the mechanism and manage a precise control of lateral and vertical heterostructure growth by CVD method.

The deterministic growth of lateral and vertical heterostructures can be explained by the classical nucleation kinetics model during the second layer growth [112], as illustrated in Figure 2.12a. The first compound grow spontaneously on the growth substrates, while the vapor reactants for the growth of the second compound selectively deposit into the facet edges of the first compound, and serve as preferential nucleation sites. The outcome of whether the edge nuclei expend onto the surface of the first compound (leading to vertical growth as panel 1) or the substrate surface (resulting in lateral growth as panel 2) is determined by the associated nucleation rate R:

$$R = \exp\left(-\frac{\Delta G^*}{kT}\right) \times \exp\left(-\frac{\Delta G_m^*}{kT}\right) \tag{2.3}$$

where ΔG_m is the thermal activation energy for atomic migration into the nucleus. The critical free energy barrier for nucleation ΔG^* can be expressed by the following equation:

$$\Delta G^* = \frac{\pi t(\gamma_{c,\text{edge}})^2}{L\Delta T / T_m - (\gamma_c + \gamma_{cs} - \gamma_s)/t} \tag{2.4}$$

where r and t are the radius and the thickness of the nucleus. γ_s, γ_c, $\gamma_s c$, and $\gamma_{c,edge}$ correspond to the surface energy of the substrate, surface energy of nucleus of monolayer crystals, interfacial energy between the substrate and the nucleus, and surface energy of nucleus edge of the monolayer crystals, respectively, and T_m is the melting temperature of monolayer crystal, ΔT is the difference between the melting temperature and the growth temperature.

Thus the nucleation rate R is highly related to the growth temperature, and can be maxmized at a certain temperature, as shown in Figure2.12c. When the associated nucleation rate is higher on the surface of the first compound than that on the growth substrate at certain growth temperature, heterostructures tend to grow vertically to maintain the lowest energy state, as illustrated in Figure 2.12d. Conversely, if the nucleation rate is lower, lateral heterostructures are more likely to form as demonstrated in Figure 2.12e.

"One-step" and "two-step" growth route

To achieve TMDC heterostructures, two main growth routes are distinguished based on whether the samples are taken out of the chamber between the growth of two compounds: "one-step" and "two-step" growth route.

In the one-step growth route, all precursors required for the synthesis of TMDC heterostructures can be introduced into the growth reactor without opening the chamber. The sequence of the growth can be controlled by either adjusting various growth products at different growth temperatures or switching the gaseous precursor supply. For example, as demonstrated in Figure 2.13a, the precursors for both MoS_2 and WS_2 growth are placed in the tube furnace at one time. The difference in their nucleation and growth rates gives rise to sequential growth of MoS_2 and WS_2. The optical microscope image in Figure 2.13c presents the morphology of the as-grown heterostructure: monolayer MoS_2 is grown in the center, while monolayer WS_2 is grown around MoS_2, forming an in-plane heterostructure. The "one-step" route provides a practical and effective approach to achieve continuous growth while maintaining high chemical reactivity at the interface. Moreover, it ensures an oxygen-free environment throughout the entire growth process, leading to a residue-free interface and a low defect concentration.

In the two-step growth route, following the growth of the first compound, the as-grown sample is taken out of the growth chamber to facilitate alterations such as changing the precursor or implementing additional processes like spin-coating, lithography, or sulfurization. Subsequently, the modified sample is re-loaded into the growth chamber to undergo the second CVD process. A representative example of this "two-step" growth approach is illustrated in Figure 2.13b and the as-grown samples are presented in Figure 2.13d and e. Although the interface quality may not reach the same level as that in "one-step" growth, this method allows

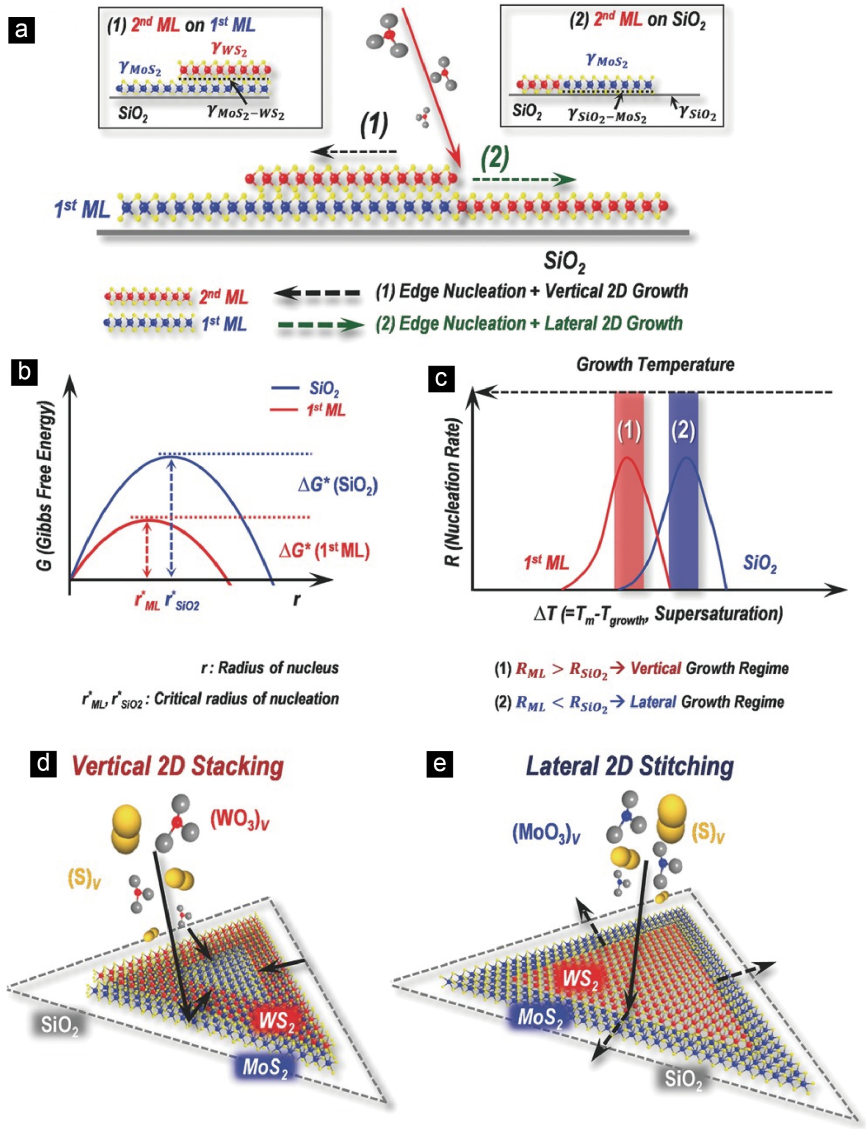

Figure 2.12: Control of lateral and vertical heterostructure growth. (a) The 2D nucleation kinetics model for the lateral and vertical heterostructure growth. (b) The energy barrier for 2D nucleation of the second compound on SiO_2 substrate and on the surface of the first compound. (c) The correlation between the 2D nucleation rate and the growth temperatures deduced from (b). (d,e) The schematic illustration of vertical and lateral heterostructure growth. Reprinted with permission from ref. [112].

for the creation of more complex heterostructures.

In this thesis work, considerable amount of efforts have been devoted to explore the growth recipes of TMDC heterostructures, which also includes the investigation of using "one-step" route in Chapter 6 and "two-step" route in Chapter 7 and will be further discussed in later chapters.

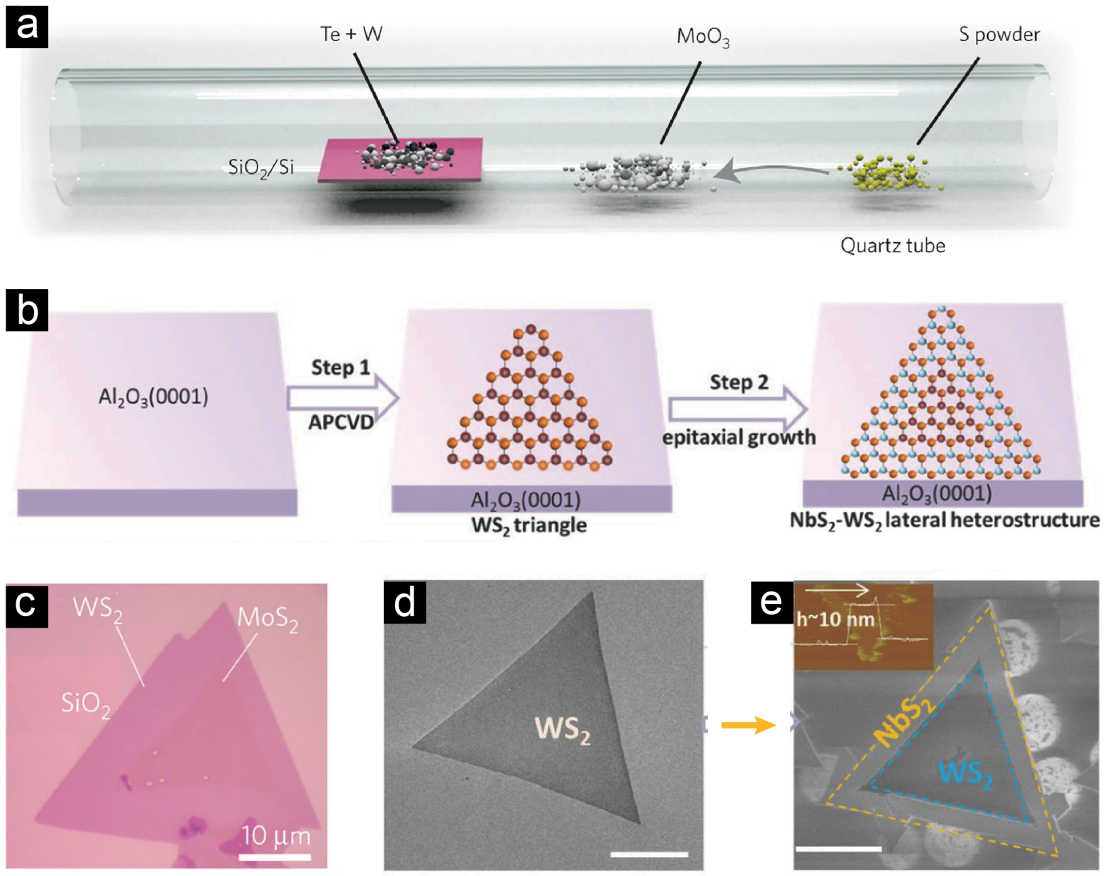

Figure 2.13: "One-step" and "two-step" growth route of TMDC heterostructures by CVD. (a) Schematic of the CVD process for MoS_2-WS_2 heterostructures by one-step growth route. (b) Process flow of "two-step" CVD route to grow WS_2-NbS_2 heterostructures. (c) Optical microscope image of as-grown MoS_2-WS_2 heterostructures obtained by the "one-step" growth route shown in (a). (d-e) Optical microscope images of WS_2 crystal and WS_2-NbS_2 heterostructure obtained by the two steps during the growth of heterostructures shown in (b). Scale bar: 25 μm. Reprinted with permission from ref. [113] and [114].

3 Experimental techniques

3.1 Introduction

Comparing to traditional bulky semiconductors, the properties of two-dimensional (2D) semiconductors are extremely sensitive to the environment, and their device performance can be significantly influenced by the material and interface quality. To obtain high-quality 2D materials and improve their device performance, a significant amount of time and effort are devoted to optimize the synthesis of 2D materials and handle various techniques for material characterization, device fabrication, and electrical measurement. Therefore, a complete overview of these methods is given in this chapter.

In Section 3.2, the main material synthesis method in this thesis work, metal-organic chemical vapor deposition (MOCVD) is demonstrated, with a detailed description on its configuration. Detailed growth parameters are further discussed in later chapters. In Section 3.3, several material characterization techniques are presented, including the atomic force microscope (AFM), Raman spectroscopy, photoluminescence spectroscopy (PL), X-ray photoelectron spectroscopy (XPS), high-resolution scanning transmission electron microscope (STEM), and energy dispersive X-ray spectroscopy (EDS). These techniques are frequently employed in later chapters to examine the surface morphology, the material quality, the chemical composition and the lattice structure, which provides fundamental information on our as-grown materials. The following Section 3.4 illustrates the device structures utilized in this thesis and discusses the process flow to fabricate the electronic devices, including material transfer methods, patterning with lithography techniques, etching techniques, and metal and dielectric deposition methods. In the last Section 3.5, the techniques and instruments employed in this thesis for the electrical measurements are described, including electrical transport measurements, superconductivity measurements, and memory characterizations. The measurement results with further analysis and discussion is available in later chapters.

3.2 Material synthesis by MOCVD

Although two-dimentional (2D) transition metal dichalcogenide (TMDC) materials can be simply obtained by the top-down exfoliation method due to the weak van der Vaals force, the irregular shape and uncontrollable thickness of the obtained flakes as well as the poor yield and unscalable production process still hinder their scaling and industrial application. In comparison, the bottom-up chemical vapor deposition (CVD) method is controllable and scalable, expected to synthesize the 2D TMDC materials in a large-area scale with homogeneous shapes and thicknesses. In particular, as the advanced technology of CVD, metal-organic chemical vapor deposition (MOCVD) method based on all-gas precursors shows higher controllability and uniformity of the growth process and as-grown materials. In this thesis work, CVD and MOCVD are used as main synthesis methods to produce the samples we study (e.g., MoS_2 in Chapter 4 and Chapter 7, NbS_2 in Chapter 5, NbS_2-MoS_2 lateral heterostrutures in Chapter 6). The CVD and MOCVD growth is carried out in a tube-based horizontal reactor built up in our laboratory, which will be depicted in this section.

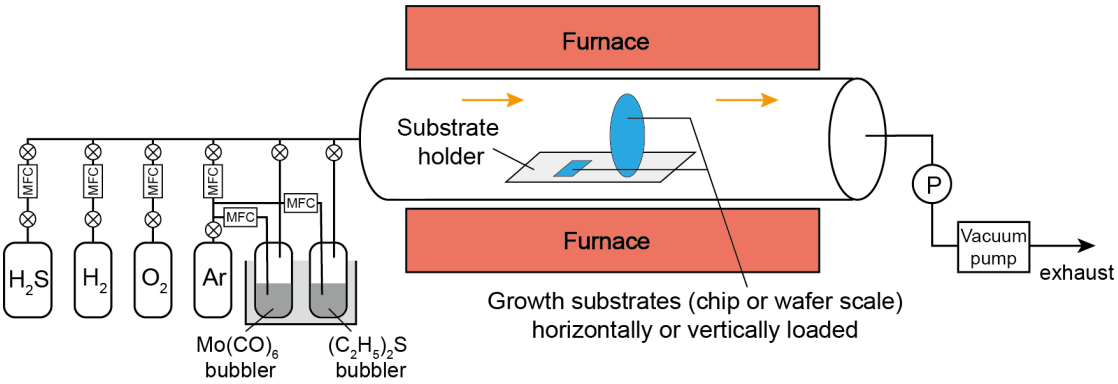

Figure 3.1: Schematic of the home-built MOCVD system for material synthesis. The system is controlled by LabView and consists of three main parts from the left to the right: the precursor inlet part, the middle growth part, and the waste disposal part.

The configuration of our home-built MOCVD system is schematically illustrated in Figure 3.1. The system is controlled by Labview and consists of three main parts: the precursor inlet part, the middle growth part, and the waste disposal part. In the first part, the two precursors, molybdenum hexacarbonyl ($Mo(CO)_6$, Sigma Aldrich supplies) and diethyl sulfide ($(C_2H_5)_2S$, Sigma Aldrich supplies) are stored inside the bubbler cylinders in a water bath, where the temperature can be maintained at the setpoint to keep a stable vapor rate of the precursor, and carried by Argon (Ar) to the MOCVD furnace reactor. Alternatively, hydrogen sulfide (H_2S, Multigas supplies) can be also introduced to the MOCVD furnace reactor as sulfur precursor. In addition, a small amount of oxygen (O_2) or hydrogen (H_2) can also be added into the reactor for an etching-gas confined growth (discussed in detail in Section 4.2.2). The flow rate of each gas is controlled by a separate mass flow controller (MFC). The middle growth part is built by a Carbolite tube furnace (0-1100 °C) and a quartz tube (4-inch in diameter and 1.3 m in length). A 2-inch c-plane sapphire wafer or a c-plane sapphire chip is used as the growth substrate and

annealed at 1000 °C in the air before growth to achieve an atomically smooth surface. The growth substrates can be loaded vertically or horizontally on a boat-shape quartz holder in the middle of the furnace. Prior to growth, the substrate is treated in 3 wt% potassium hydroxide (KOH, Sigma Aldrich supplies) solution to obtain a hydrophilic surface and spin-coated with NaCl solution (concentration of 0.05-0.3 mol/L in DI water, Sigma Aldrich 99.5%) to suppress the nucleation and accelerate the growth. The growth reaction takes place at 850-950 °C lasting for around 30 minutes. In the waste disposal part, a vacuum pump is connected between the tube reactor and the exhaust ventilation to fully pump out the remaining air before growth and the reaction residues after growth. The tube reactor is kept at atmospheric pressure during the growth process, with the growth temperature and gas flow controlled automatically by LabView. Since the growth parameters are different for various materials, further details about the parameter optimizations and growth results are discussed in later chapters.

3.3 Material characterization

To evaluate the quality of the as-grown materials and to further optimize the growth parameters, several material characterization techniques are employed before device fabrication and electrical measurements to pursue a good performance. For example, the as-grown materials are first observed under an optical microscope (Olympus BX51M) to briefly check the size, shape, thickness and overall uniformity. Subsequently, atomic force microscope (AFM) is utilized to precisely measure the sample thickness, surface morphology and identify any possible cracks or residues. Some optical characterization techniques, such as Raman spectroscopy, photoluminescence (PL), and X-ray photoelectron spectroscopy (XPS) can also be used to further assess the chemical components, elemental composition, doping level and lattice strain. Lastly, high-resolution scanning transmission electron microscopy (HR-STEM) and energy dispersive X-ray spectroscopy (EDS) are conducted to examine the atomic structure and elemental distribution. Here in this section, the working principles and instruments of each technique we use to characterize our materials will be described in the following subsections, while the measurement results will be discussed in later chapters.

3.3.1 Atomic force microscope

Atomic Force Microscopy (AFM) is a versatile technique used to examine surfaces at the nanoscale level. It is based on the principle of detecting the force between a cantilever and a sample surface, as schematically shown in Figure 3.2a. The cantilever, typically made of silicon (Si) or silicon nitride (Si_3N_4) and coated with a thin layer of metal, is mounted on a flexible beam and positioned above the sample surface. During scanning, the cantilever is brought into contact with the surface using a feedback loop, which maintains a constant force between the cantilever tip and the surface. As the cantilever scans across the surface, the deflection of the cantilever is measured by a laser reflected off the back of the cantilever. The deflection is proportional to the force between the tip and the surface, which is utilized to

generate an image of the surface topography. Additionally, AFM can be employed to measure other physical properties of a surface, including elasticity, adhesion, and friction, by analyzing the force-distance curve obtained during the scanning process.

In 2D material field, AFM is widely used to precisely measure the thickness of 2D crystals to determine the number of atomic layers. Due to the fragility of 2D materials, non-contact mode AFM is particularly useful because it allows for a precise measurement of the material thickness without causing any damage. In this mode, the cantilever is positioned above the sample surface at a distance larger than the thickness of the 2D material. The oscillation frequency of the cantilever is adjusted to be close to the resonance frequency of the cantilever in order to achieve maximum sensitivity. As the cantilever scans across the surface, the amplitude and frequency of the oscillation tend to change due to the interaction between the cantilever and the sample, which triggers the feedback loop system to adjust the tip height to maintain a constant oscillation amplitude. The thickness of the 2D material can be determined by analyzing the change in frequency and amplitude of the oscillation, which is proportional to the distance between the cantilever and the surface.

Figure 3.2b shows an exemplary AFM image of an as-grown NbS_2 flake on top of a sapphire substrate, with a corresponding height profile showing a thickness of around 1.5 nm (2 layers). In this thesis work, all AFM data are acquired on the Asylum Research Cypher AFM in the LANES laboratory, using Si tips with a nominal resonant frequency around 70 kHz (Olympus AC240TS).

3.3.2 Raman spectroscopy

Raman spectroscopy is a powerful and non-destructive technique for studying the vibrational and structural properties of materials. It has been used as a convenient tool to measure the layer numbers and characterize the doping and strains in 2D materials. As described in the upper panel of Figure 3.2c, Raman spectroscopy relies on the interaction between the scattered light and the target sample, where the scattered light provides information about the vibrational modes of the material. When a sample is irradiated with a monochromatic light source, some of the photons interact with the vibrational modes of the material, causing a shift in the energy of the scattered photons. The Raman spectrum of the material is obtained by measuring the intensity of the scattered light at different frequencies, which provides a unique fingerprint of the material.

In TMDCs, the Raman spectrum is particularly informative due to the presence of the E_{2g} mode, which is related to the in-plane vibrations of the metal and chalcogen atoms in the material. The intensity and line width of E_{2g} peak provide information about the degree of strain, defects, and doping in the material, making Raman spectroscopy a powerful tool for studying the properties of TMDCs. In addition to the E_{2g} mode, TMDCs exhibit several other peaks in the Raman spectrum, as shown in the bottom panel of Figure 3.2 such as A_{1g} and 2LA modes, which are related to the out-of-plane vibrations of the chalcogen atoms and

the interlayer coupling between the layers, respectively. These modes are also sensitive to the crystal structure and defects in the material, and their intensity and width line provide valuable information about the properties of the material.

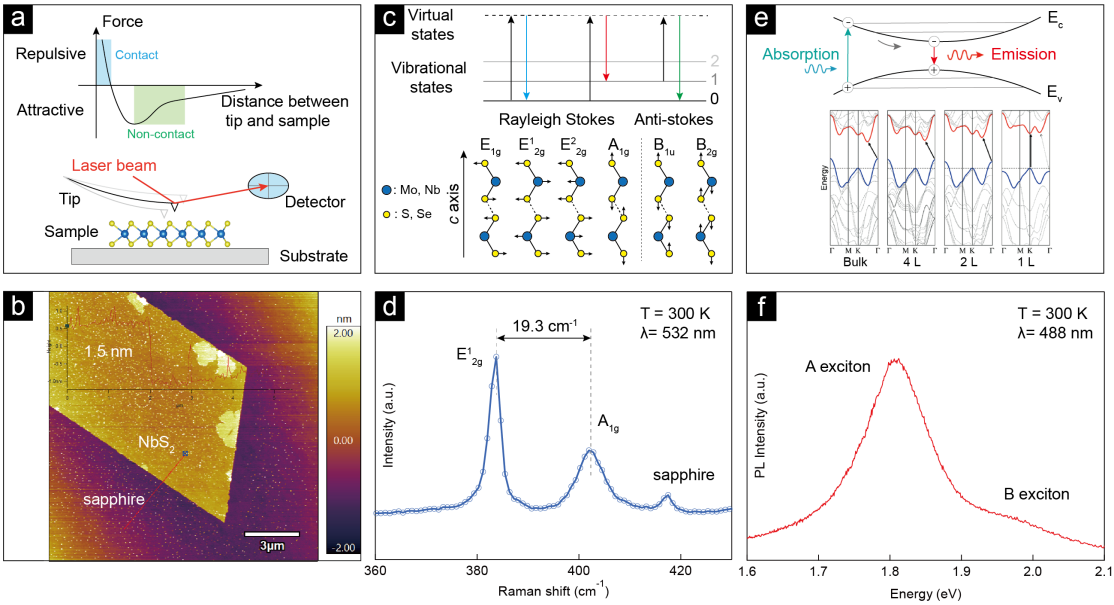

Figure 3.2: Material characterization techniques: AFM, Raman and PL. (a) A force-distance graph and a working schematic showing the interaction between tip and sample when AFM working. (b) An exemplary topography image and height profile on an as-grown NbS_2 sample measured by AFM microscope. (c) Interactions with the incident laser by Raman spectroscopy and typical lattice vibration modes of TMDC materials. (d) An exemplary Raman spectrum of monolayer MoS_2 on the sapphire substrate. (e) Top: a schematic showing photon-electron interactions during PL spectroscopy. Bottom: calculated band structure of bulk, quadrilayer, bilayer and monolayer MoS_2, reproduced from ref.[45]. (f) An exemplary PL spectrum of monolayer MoS_2 on sapphire substrate. The signal of sapphire background has been removed.

Figure 3.2d demonstrates exemplary Raman spectra acquired on monolayer MoS_2 film grown on a sapphire substrate. The distance between the two typical peaks, $E^1{}_{2g}$ and A_{1g} peak, is around 19.3 cm^{-1}, indicating the nature of monolayer of our MoS_2 film. Raman measurements presented in this thesis work are carried out using a commercial Renishaw inVia Qontor confocal Raman microscope with a 532 nm laser, 3000 gr/mm grating, and a Master Renishaw CCD detector. The parameters are slightly different for various substrates to obtain a strong signal with low noise. In general, we use an excitation power of 1-5 mW, the exposure time of 5-20 s, and the accumulation of 5-10 cycles.

3.3.3 Photoluminescence spectroscopy

Photoluminescence (PL) spectroscopy is a handy and instructive technique used to investigate the optical properties of materials by measuring the emission of light from excited states. As shown on the top of Figure 3.2e, the material absorbs photons from the excitation light with

higher energies ($h\nu$) than the bandgap energy (E_g) and the electrons get excited from the valence band to the conduction band, which creates electron-hole pairs (excitons). These excitons then recombine, emitting a photon with an energy equal to the bandgap of the material, which can be detected and analyzed to gain insights into the electronic and structural properties of the material.

In the field of 2D TMDCs, PL has been a very useful technique for identifying monolayer crystals owing to their unique property of an indirect-to-direct bandgap transition from bulk to monolayer materials, demonstrated on the bottom of Figure 3.2e. In addition, by measuring the wavelength and intensity of the emitted light, PL spectroscopy can provide valuable information about the optical properties of TMDCs, such as their bandgap energies, exciton dynamics, and defects.

Figure 3.2f shows an exemplary PL spectrum of an as-grown monolayer MoS_2 film on a sapphire substrate, where the signal of the sapphire background has been removed. Two distinct emission peaks are visible from the spectrum, designated as the A-exciton originated from the ground state and B-exciton from a higher spin-orbit split state. In this thesis work, we conduct the PL spectroscopy at room temperature by using the same instrument of Raman spectroscopy as described in Section 3.3.2. The only differences are the usage of the laser wavelength (488 nm) and a sparser grating (600 gr/mm) for a wide spectra range.

3.3.4 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is a widely used analytical technique that provides information on the chemical and electronic properties of a material, based on the excitation of electrons in the material using a beam of X-rays, as depicted in Figure 3.3a. The electrons from the atoms in the topmost layers of the material can be ejected by the X-rays (referred as photo-electrons) and their energy can be detected by a spectrometer, which provides information about the chemical composition of the material.

In 2D materials, such as graphene, transition metal dichalcogenides (TMDCs) and black phosphorus, XPS is a powerful tool to investigate their surface chemistry and electronic structure. For example, XPS spectrum provides information on the types and concentrations of elements present in the surface layer of the material, which can be used to determine the quality and purity of the material. XPS can also give information on the valence band and core level electronic structure of the material, which can be used to determine the electronic properties of the material, such as the bandgap energy, work function and charge transfer. Furthermore, XPS can be used to characterize defects and impurities of 2D materials, which has a significant impact on the electronic properties of the material.

Figure 3.3b shows an exemplary XPS spectrum acquired on an as-grown NbS_2 sample on top of a sapphire substrate. The full-range spectrum shows the binding energy, the number of detected electrons and its electron configurations for each atom, from which chemical

compositions can be analyzed by further fitting. In this thesis work, the XPS measurements are carried out by the Surface characterization center at EPFL, using a PHI VersaProbe II scanning XPS microprobe (Physical Instruments AG, Germany) with a monochromatic Al Kα X-ray source of 24.8 W power and a beam size of 100 μm.

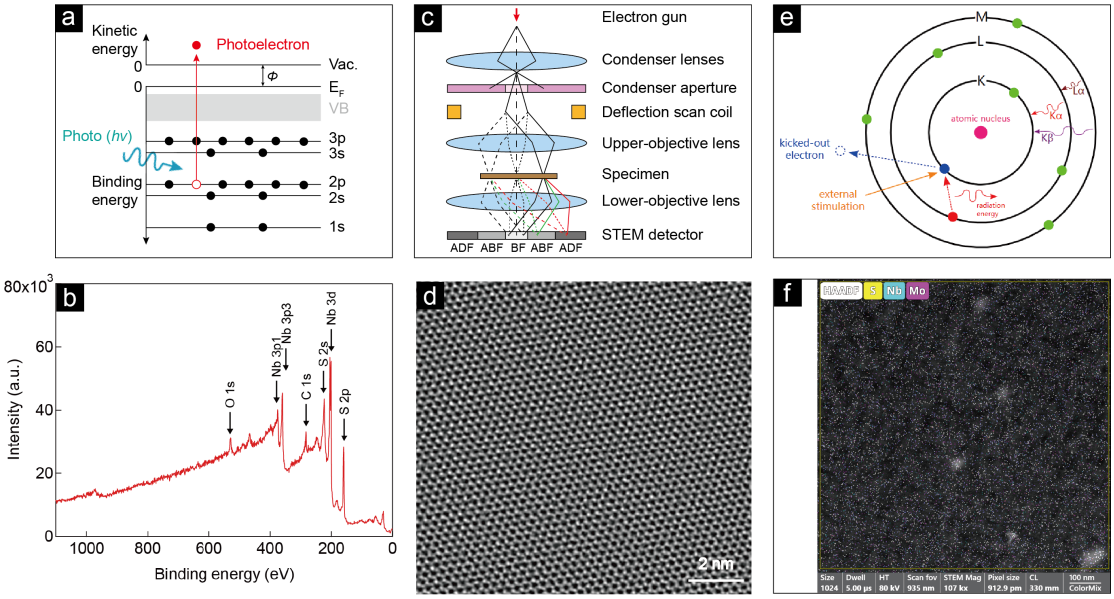

Figure 3.3: Material characterization techniques: XPS, STEM and EDS. (a) A schematic showing the photoelectric effect as XPS working. (b) An exemplary full-range XPS spectrum of an as-grown NbS_2 sample on a sapphire substrate. (c) A simplified STEM configuration showing the main components and optical path diagram. (d) An exemplary STEM image of monolayer MoS_2 film transferred on TEM grid. (e) A schematic demonstrating the X-ray emission process when EDS working. (f) An exemplary EDS mapping of Nb-doped monolayer MoS_2 showing the elemental distribution. The figure in panel e is reproduced from ref. [115].

3.3.5 Aberration-corrected high-resolution scanning transmission electron microscopy

The high-resolution scanning transmission electron microscope (HR-STEM) employs a highly focused electron beam to obtain images of atomic-scale resolution, enabling it to resolve the atomic structure of materials. The HR-STEM comprises several components working in tandem to produce high-resolution images, as illustrated in Figure 3.3c, including an electron source, an electron lens, a specimen stage and a detector. When acquiring STEM images, the electron source generates a highly focused electron beam, which then passes through the electron lens and focuses onto the specimen. As the beam passes through the specimen, it interacts with the atoms in the material, causing the electron scattering in different directions. The scattered electrons are then detected by the detector, and the resulting pattern is used to construct an image of the material.

As an example, an STEM image of monolayer MoS_2 film is displayed in Figure 3.3d, showing its lattice structure with a 2H stacking. In this thesis work, STEM measurements are conducted by using a double aberration-corrected FEI Titan Themis, equipped with a X-FEG, Super-X EDS detector and a Wein-type monochromator, operated at 80 kV acceleration voltage. The as-grown samples are transferred to a silicon nitride TEM grid by PMMA-assisted wet transfer technique as explained in Section 3.4.2. Afterwards, the grid is immersed in hot acetone and annealed in high vacuum for 6 hours at 250 °C to remove the polymer residue. All STEM measurements are performed by using the parameters as follows: The beam convergence half-angle is set to 20 mrad which collects angles between 49.5-198 mrad. The microscope is conducted at an accelerating voltage of 80 kV, ensuring it remains below the threshold for electron-beam-induced knock-on damage to the samples. The electron probe current is set to 20 pA. To avoid sample drift, images are collected at different regions using a quicker scan with 512×512 pixels and 8 µs dwell times. Inverse fast Fourier transform filtering is applied to magnified images to improve contrast and emphasize atomic structures. The HR-STEM imaging and analysis in this thesis are mainly performed by Dr. Mukesh Tripathi from LANES group.

3.3.6 Energy dispersive X-ray spectroscopy

Energy dispersive X-ray spectroscopy (EDS) is a non-destructive method widely used for determining the elemental composition of materials, which relies on the detection and analysis of X-rays generated when high-energy electrons bombard the sample. As shown in Figure 3.3e, the electrons generated in the electron gun are accelerated towards the sample and collide with the atoms on the surface of the sample, generating X-rays related to the energy levels of the detected samples. The emitted X-rays are then detected and analyzed by a detector, separated by their energy levels. The resulting spectrum of X-rays displays unique peaks of the elements present in the sample and their relative abundances.

An EDS mapping of Nb-doped MoS_2 is shown in Figure 3.3f, from which a uniform elemental distribution can be observed. The composition of each element can be analyzed by further fitting the spectrum. In this thesis work, EDS measurements are performed in both Titan Themis and FEI Talos TEM by Dr. Mukesh Tripathi from LANES group. The as-grown samples are transferred to a silicon nitride TEM grid by PMMA-assisted wet transfer method (Section 3.4.2) followed by being immersed in hot acetone and annealed in a high vacuum for 6 hours at 250 °C to remove the polymer residue. The intensities of STEM-EDS elemental maps and spectrum are recorded by using Nb Lα, Mo Kα, and S Kα X-ray emissions, respectively. Velox software, ThermoFisher Scientific is used to process the EDS spectrum and elemental mapping data.

3.4 Device fabrication

After the synthesis and characterization of as-grown materials, we transfer them to the Si/SiO_2 substrate for device fabrication and further electrical measurements. Due to their nature of atomic thickness, 2D materials are fragile and sensitive to surface residues and interface states. Therefore, specific techniques are required to maintain a high cleanness and reduce possible damages during device fabrication process. In this section, the device structures for different purposes of electrical measurements are introduced first. Several techniques used for device fabrication are depicted in later subsections, including transfer methods, photolithography, etching techniques, electron beam lithography, dielectric deposition, metal deposition and lift-off.

3.4.1 Device structures

To study the transport behavior of our MOCVD-grown materials, field-effect transistors (FETs) are fabricated after transferring the materials onto Si/SiO_2 substrate, as schematically shown in Figure 3.4a, showing a cross section view of a FET device fabricated based on monolayer MoS_2. Monolayer MoS_2 is used as an active channel material, with a Si substrate as backgate and a layer of 270 nm-thick SiO_2 as tunnel blocking oxide. Corresponding optical microscope images of two-probe and four-probe FETs are demonstrated in Figure 3.4c-d, respectively, for different purposes of electrical measurements. In addition, floating-gate (FG) FETs are also fabricated in this thesis work to employ our materials on in-memory computing and artificial neural networks. The device geometry and optical microscope image of a FGFET based on NbS_2-MoS_2 heterostructure are presented in Figure 3.4b and e, respectively. The device configuration may change according to various materials and purposes of measurements, which will be further depicted in later chapters.

Taking the FGFET device (Figure 3.4b) as an example, the detailed process flow of fabrication can be described as follows. First, the as-grown material is transferred from sapphire onto the Si/SiO_2 substrate (Subsection 3.4.2). Afterwards, the material is patterned to the desired shape and size by using laser writer lithography (Subsection 3.4.4) or electron beam lithography (Subsection 3.4.5) depending on the needed accuracy and etching techniques (Subsection 3.4.6). Eventually, a stack of 2 nm titanium (Ti) and 80 nm gold (Au) is deposited on top of the material as electrode contacts by using laser writer lithography (Subsection 3.4.4) or electron beam lithography (Subsection 3.4.5), metal deposition and lift-off (Subsection 3.4.7). Before above fabrication process, the Si/SiO_2 substrate is sequentially deposited by a stack of 2 nm chromium (Cr) and 40 nm platinum (Pt) as local gate (Subsection 3.4.7), 30 nm SiO_2 as blocking oxide by atomic layer deposition (ALD) (Subsection 3.4.8), 5 nm platinum (Pt) as floating gate (Subsection 3.4.7) and 7 nm SiO_2 as tunnel oxide (Subsection 3.4.8).

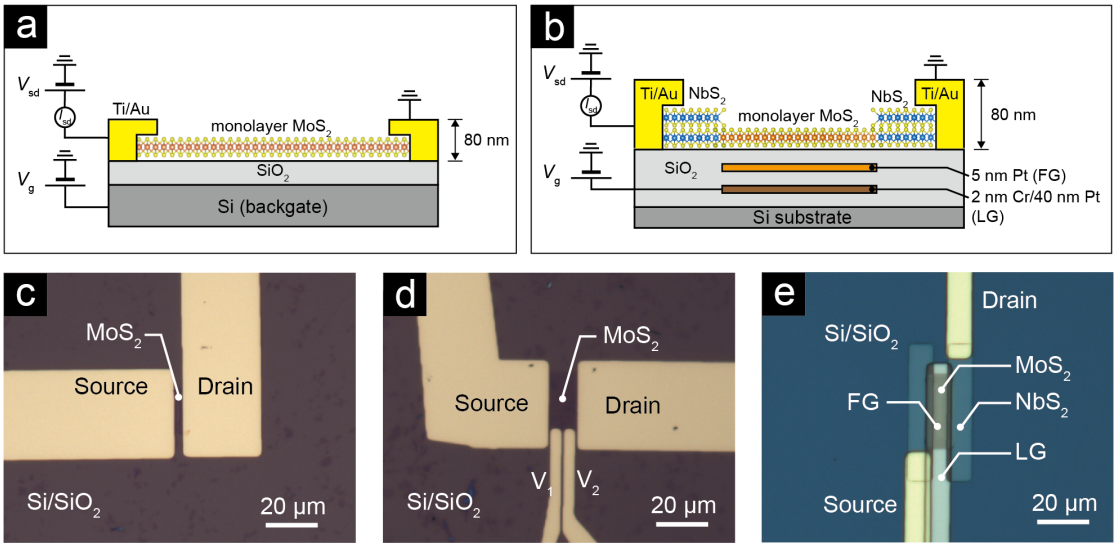

Figure 3.4: Device structures employed for electrical characterizations in this thesis work. (a) The configuration of a two-probe field-effect transitor (FET) based on monolayer MoS_2. (b) The device geometry of a floating-gate FET based on NbS_2-MoS_2 heterostructure. (c-d) The optical microscope images of a two-probe and a four-probe field-effect transitor (FET) based on monolayer MoS_2, respectively. (e) The optical microscope image of a floating-gate FET based on NbS_2-MoS_2 heterostructure.

3.4.2 Transfer methods

Wet transfer via PMMA and water capillary force

To transfer the as-grown sample from sapphire to Si/SiO_2 substrate, the sample is first spin-coated with polymethyl methacrylate (PMMA) at a speed of 2000 rpm for 60 s and baked on a hot plate for drying at 180 °C for 5 min, creating a stack of PMMA, as-grown sample and sapphire substrate. The purpose of this step is to add a relatively thicker film on top of the sample for protection so that it can more easily withstand the following steps. It is noted that PMMA A2 is used for MoS_2 transfer, while PMMA A4 (denser than PMMA A4) is used for NbS_2 transfer because of a stronger interaction between NbS_2 and sapphire substrate. Afterwards, the stack is diced into smaller pieces with PMMA at the edges scratched away, cleaned with IPA and dried with Nitrogen (N_2). The stack is then immersed in DI water for 10 min, which facilitates film detachment in later process when water penetrates the interface between the sample and sapphire substrate. The stack is picked out and slowly re-immerse into water with the degree between the chip and water surface around 45° (Figure 3.5 step 4). In this way, the gap between the film of PMMA/as-grown sample and sapphire substrate can be slowly opened by the capillary force at the interface, leading to a gradual detachment of the thin film. After detachment, the film is floating on the water surface and can be fished up by a target substrate (Si/SiO_2). Subsequently, the film holding by the target substrate is heated at 65 °C for 30 minutes to remove water and promote the adhesion to the target substrate. Finally, the PMMA film can be removed by immersing the sample in acetone overnight. An additional

annealing process in high vacuum at 250 °C for 6 h is applied to further enhance the interface quality by eliminating remaining polymer residues and moisture.

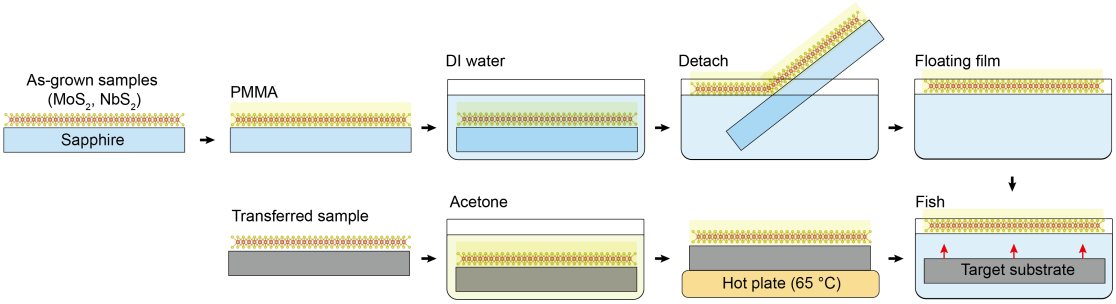

Figure 3.5: Process flow of material transfer via PMMA and water capillary. A schematic showing each step when transferring as-grown samples from sapphire substrate to another target substrate with assistance of PMMA and water capillary.

Thanks to the high flexibility of the thin PMMA film, this wet transfer method (process flow shown in Figure 3.5) is mostly used in this thesis work when transferring an as-grown sample (NbS_2 flakes in Chapter 5 and NbS_2-MoS_2 heterostructures in Chapter 6) completely without damage or cracks to a Si/SiO_2 substrate or a TEM grid. However, the capillary force of water is difficult to control by determining the degree when re-immersing, making the method not efficient and kind of tricky. Moreover, the method works well for flakes up to micrometer scale but has difficulties when transferring wafer-scale continuous film. This method is developed by my colleagues, Dr. Jing Zhang and Dr. Yanfei Zhao in LANES group, and further improved by Zhenyu Wang.

Semi-dry transfer assisted by PMMA and thermal-release tape

As discussed in the previous transfer method, the wet transfer method shows a low efficiency and its bottleneck when transferring wafer-scale continuous film. Thus, a new transfer technique assisted with thermal-release tape is developed to satisfy the need of continuous film transfer in a more controllable way, as demonstrated in Figure 3.6 and described below.

The preparation steps of semi-dry transfer is similar to the one we presented above in wet transfer. The sample (in a chip or wafer scale) is first spin-coated with PMMA at a speed of 2000 rpm for 60 s and heated at 180 °C for 5 min for drying. Afterwards, the sample can be diced to small chips or keep its original size according to the size of target substrate, with the edges of PMMA layer scratched away followed by cleaning with IPA and drying with N_2. Instead of immersing to water directly, a thermal-release tape (shrink at 135 °C) is covered on top of the PMMA layer to create a stack of tape/PMMA/sample/sapphire, followed by removing bubbles using a flat tweezer. Then the stack is left in wafer for around 10 min, letting water go into the gap between the film and sapphire substrate, and the sapphire substrate can be detached gently by a tweezer in water, leaving the film of PMMA and sample on the tape because of their stronger adhesion. Subsequently, the tape attached with the film is slowly put on the target substrate with removing bubble with a flat tweezer as before. The sample is then

baked on a hot plate at 55 °C for 1 hour to improve the adhesion. To remove the tape from the sample, the hot plate is heated up to 135 °C, at which temperature the thermal-release tape shrinks and PMMA film with the sample remains on the target substrate. Finally, the sample can be cleaned by removing PMMA film in acetone overnight and annealing in high vacuum at 250 °C for 6 h.

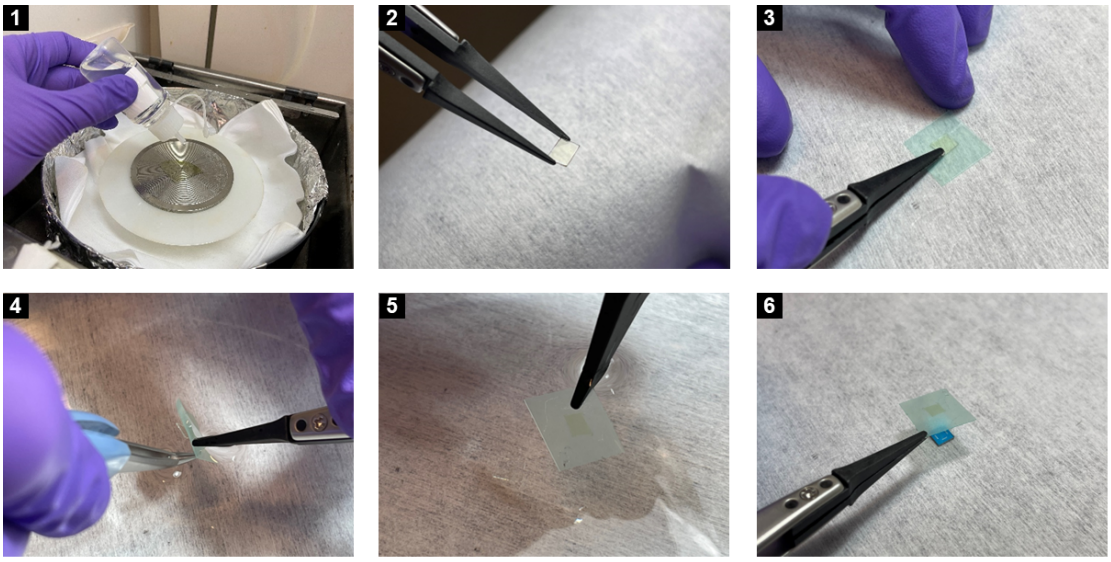

Figure 3.6: Material transfer assisted by PMMA and thermal-release tape. Sequential pictures showing the transfer process assisted by PMMA and thermal-release tape.

Compared to wet transfer method via water capillary, this method assisted with thermal release tape shows its advantage in transferring chip-scale or wafer-scale continuous film, enabling the scalable applications on integrated devices of TMDC materials, such as logic-in memories and artificial neural networks based on monolayer MoS_2 (Chapter 4) and NbS_2-MoS_2 heterostructures (Chapter 7). This method is well developed by my colleague Dr. Guilherme Migliato Marega, and further optimized by Zhenyu Wang.

3.4.3 Photolithography

Photolithography is a fundamental technology used to transfer a pattern from a mask onto a substrate using light, which enables the production of micrometer-scale and even more complex electronic devices. To do photolithography, as illustrated in Figure 3.7, the substrate is first coated with a layer of photoresist and then exposed to light through a mask, which contains a desired pattern of the features. A positive resist leads to a higher solubility of the exposed region in the developer, and for the negative one, the unexposed regions are soluble. After exposure, the photoresist is developed to remove the areas that were made more or less soluble by the exposure. In this way, the desired patterns are transferred from the masks to the substrate followed by etching or deposition of material.

Although the traditional photolithography with a mask is not a main technique used in this thesis work, its advanced techniques share a similar working principle (Figure 3.7), laser writer lithography (Subsection 3.4.4) and electron beam lithography (Subsection 3.4.5), are mostly used in our process flow of device fabrication, which will be discussed in later subsections.

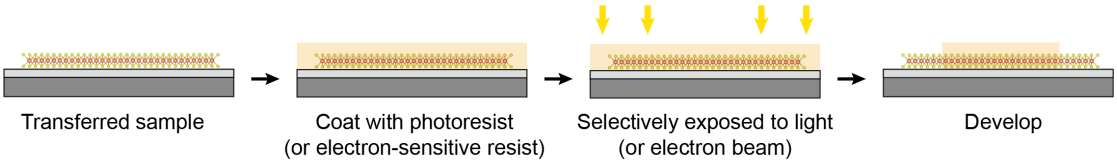

Figure 3.7: Process flow of photolithography. Schematics showing the photolithography process to make pattern mask with resist on a sample. A similar working principle is shared with laser writer lithography (Subsection 3.4.4) and electron beam lithography (Subsection 3.4.5).

3.4.4 Laser writer lithography

Laser writer lithography is a high-resolution lithography technique with an accuracy of several micrometers to tens of nanometers, which is commonly used to produce patterns for microelectronic devices on large scales. In this thesis work, laser writer lithography is used to prepare patterns of photoresist masks on substrate before material etching and metal deposition. The process begins with a Si/SiO_2 substrate (chip or wafer scale) coated with positive double layers of photoresists, 0.4 μm of LOR 5A (poly(methyl methacrylate-co-methacrylic acid), PMMA-co-MMA) on the bottom and 1.1 μm of AZ 1512 HS (bis(4-dimethylaminophenyl)phenylmethanone novolac resin) on the top. Here, the bottom LOR 5A layer is spin-coated at a speed of 5000 rpm for 60 s and baked at 180 °C for 4 min, and the top AZ 1512 HS layer is spin-coated at a speed of 5000 rpm for 60 s and baked at 100 °C for 90 s. Since LOR 5A is more sensitive to the laser irradiation, the bottom layer tends to be slightly over-exposed, resulting in an undercut structure, which prevents the material depositing on the walls of the pattern and facilitates the lift-off of excess metals in later process. A laser beam with a wavelength of 405 nm and a dose of 60 mJ/cm^2 is then selectively exposed the photoresist layers to create the desired pattern. After exposure, the photoresists are developed by AZ 726 MIF (2,1,4-diazonaphthoquinone novolac resin, no dilution needed) for 45 s to remove the areas that were exposed by the laser, followed by rinsing in DI water to clean the developer residue. The resulting pattern in the photoresist is then produced on the substrate by etching or deposition of materials (Subsection 3.4.6 and Subsection 3.4.7). The double layers of photoresists can be removed by immersing the sample in dimethyl sulfoxide (DMSO) overnight.

Compared to traditional photolithography techniques introduced in Subsection 3.4.3, laser writer lithography benefits from the ability to create higher resolution patterns and the ability to create patterns on non-planar surfaces. It also shows the advantage of being a direct-write technique, which means that patterns can be created on a substrate without the need for a mask. The laser writer lithography of this thesis work is carried out in Center of Micro-

NanoTechnology (CMi) at EPFL, with the Sawatec SM-200, coater and hotplates for i-line photoresist coating, and Heidelberg Instruments MLA150-2, i-line photoresist laser writer for exposure.

3.4.5 Electron beam lithography

Electron beam lithography (EBL) is another advanced lithography technique widely used to pattern a very precise structure in semiconductor devices. Compared to photolithography (Subsection 3.4.3) and laser writer lithography (Subsection 3.4.4), EBL writes patterns much more slowly but possesses an ultra-high resolution of several nanometers, which makes it an alternative for making patterns on nanometer scales.

Working with the similar principle as photolithography, EBL employs a focused electron beam to scan and write the patterns over the substrate covered an electron-sensitive resist layer. Here in our process flow, we use a double-layer positive resist of 150 nm-thick MMA EL6 (methyl methacrylate) on the bottom and 80 nm-thick PMMA (polymethyl methacrylate) A2 on the top to obtain a undercut structure for later easier lift-off process. It is noted here that the bottom MMA EL6 layer is spin-coated at a speed of 4000 rpm for 60 s and baked at 180 °C for 5 min, and the top PMMA A2 layer is spin-coated at a speed of 1500 rpm for 60 s and baked at 180 °C for 5 min. Upon exposure, the small precise patterns are exposed using a beam current of 1 nA with a minimum pixel size of 5 nm, while the big rough ones are exposed using a high current of 100 nA and 50 nm pixel size to shorten the exposure time. The dose is set to 900 μC/cm^2 in both cases. After exposure, the resist layers are developed by a 3:1 mixture solution of 2-propanol (IPA) and DI water for 2 minutes, which is kept at 4 °C for a smooth and sharp development, and rinsed with pure IPA to remove the residue. The desired pattern is then drawn on the substrate followed by later etching or deposition process (Subsection 3.4.6 and Subsection 3.4.7). The resist layers can be cleaned by immersing the sample in acetone overnight. In this thesis work, the spin-coating process is done in LANES laboratory, while the EBL exposure is performed in Center of Micro-NanoTechnology (CMi) at EPFL, using the Raith EBPG5000+ electron beam lithography system with acceleration voltage of 100 kV.

3.4.6 Etching techniques

To obtain a regular geometry for device fabrication, it is sometimes necessary to etch away excess 2D materials. In this thesis work, two types of etching techniques are employed, including oxygen (O_2) plasma etching and xenon difluoride (XeF_2) chemical etching, depending on the thickness of 2D materials and their substrate. The first technique, O_2 plasma etching, is more convenient and safe to use, but it may damage the protecting polymer masks due to its non-selective etching, leading to a risk of exposing the underlying materials to plasma irradiation. Thus, this technique is suitable for brief etching of very thin layer materials (monolayer or bilayers) with a thick polymer resists. In comparison, XeF_2 chemical etching is extremely selective, which reacts with TMDC crystals and is non-reactive with the photoresists, therefore

not causing damage to the protecting layer. However, XeF_2 is very harmful to the human body, so a purging and pumping procedure is required when loading and unloading the samples. In addition, due to its isotropic etching directions (both vertical and horizontal), thick crystals may have over-etched shapes compared to the desired patterns. Si and SiO_2 are also reactive with XeF_2, which may cause some etching to the substrate.

Before the etching process, laser writer lithography or electron beam lithography (Figure 3.7) is adopted to make pattern mask on resist layer. The O2 plasma etching is carried out in LANES laboratory, using the PICO low-pressure plasma system from Diener electronic. The O_2 plasma is generated with a 30 sccm of O_2 flow by scattering a 300 W RF power in a 6-inch-diameter vacuum chamber, where the exposed monolayer material is removed within 30 seconds. The XeF_2 chemical etching is performed in Center of Micro-NanoTechnology (CMi) at EPFL, using the SPTS Xactix X4-XeF_2 Silicon etching system. After loading the sample, the chamber is automatically pumped and purged with nitrogen (N_2) to remove the remaining air and moisture. The etching process consists of 5 cycles of XeF_2 vapor supply, separated by pumping the chamber down to 20 mTorr. Each cycle lasts for 30 s with the chamber pressure kept at 1 Torr. After etching, the chamber is pumped and purged again to eliminate any XeF_2 residues.

3.4.7 Metal deposition and lift-off

The Ti/Au electrode contact, the Cr/Pt local gate and the Pt floating gate in this thesis work as shown in Figure 3.4 are deposited in an ultrahigh vacuum chamber (10^{-7} mbar) by using the Leybold Optics LAB 600H electron beam evaporator in Center of Micro-NanoTechnology (CMi) at EPFL. The target wafers are placed facing down at the top of the chamber, in a rotating holder to achieve homogeneous deposition. The metals are placed in a crucible at the bottom of the chamber, which is around 1 meter distance from the wafer holder. During deposition process, the metal is melted by a high-energy electron beam and evaporated into gaseous phase, resulting a deposition on the whole wafers. To realize precise control of the thickness, the thickness of the deposited metal is continuously monitored by a quartz oscillator.

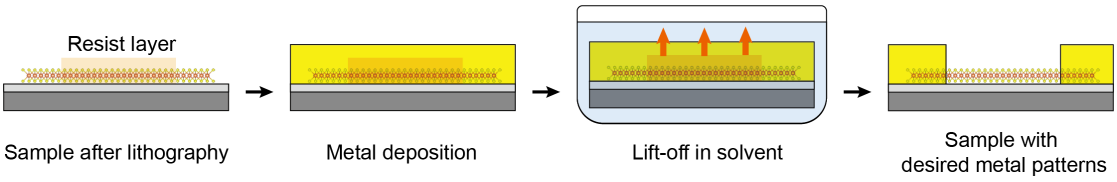

Figure 3.8: Process flow of metal deposition and lift-off. Schematics explaining the metal deposition and lift-off process to make metal patterns on a sample after lithography. The lithography process has been shown in Figure 3.7.

After deposition, the wafers are immersed in certain solvent for lift-off process to remove the resist layer and excess metals. Dimethyl sulfoxide (DMSO) is employed for removing the double-layer resists of LOR 5A/AZ 1512 HS in laser writer lithography (Subsection 3.4.4), while

acetone is used for removing the PMMA/MMA resist layers in electron beam lithography (Subsection 3.4.5). A schematic describing the metal deposition and lift-off process is shown in Figure 3.8.

3.4.8 Atomic layer deposition

Atomic layer deposition (ALD) is a thin-film deposition technique that enables precise control of material thickness and composition at the atomic level. ALD involves sequential and self-limiting surface reactions between gaseous precursors and a substrate, relying on the saturation of reactive sites on the substrate surface to ensure uniform deposition and precise control of film thickness. When ALD working, two or more gaseous precursors are alternatively exposed to the substrate surface, reacting in a self-limiting manner to form a single atomic layer. The process repeats for multiple cycles to achieve the desired film thickness and composition.

In this thesis work, high-k dielectric, silicon oxide (SiO_2), is used as the insulator material to achieve effective modulation of the electric field within the semiconducting channel. The dielectric layer is grown by ALD using the JETFIRST 200 Rapid Thermal Processing machine in Center of Micro-Nanotechnology (CMi) at EPFL. During deposition, the two precursors, bis(tertiary-butylamino)silane (BTBAS) and water (H_2O) are sequentially pulsed into the reactor (heated up to 300 °C) and react on the surface of the sample. The reactor pressure is kept between 4 to 8 mbar and the thickness of the deposited layer is controlled by counting the pulse numbers. After deposition, nitrogen (N_2) is used to purge and pump the gas line and the reactor to remove excess precursors.

3.5 Electrical measurements

In this section, the electrical measurement techniques employed in this thesis work are depicted, including the electrical transport measurements based on a field effect transistor, the superconductivity measurements based on a four-terminal device, and the memory and circuit characterizations based on floating-gate field effect transistors and 2D circuits. In each subsection, the measurement setup and parameters are described in detail, while the results and analysis will be further discussed in later chapters.

3.5.1 Electrical transport measurements

The most common geometry for transport measurements is a two-probe field-effect transistor (FET), as shown in Figure 3.4 a and c. In this thesis work, Si substrate is used as back gate to control the carrier concentration, and Ti/Au electrodes are deposited on top of the semiconductor as source and drain contacts to measure its conductivity or resistivity. While applying the gate voltage (V_g) and source-drain voltage (V_{sd}), the source-drain current can be

measured by an ampere meter as source-drain current (I_{sd}). The total resistance (R_{tot}) and conductance of the FET can be easily extracted by the following equation:

$$R_{tot} = \frac{1}{G_{tot}} = \frac{V_{sd}}{I_{sd}} \tag{3.1}$$

Considering the geometry of two-probe FETs, this total resistance includes the sheet resistance of 2D materials (R_{2D}) and the contact resistance (R_c) at the source and drain electrodes, which can be extracted by:

$$R_{tot} = R_{2D} + 2 \times R_c \tag{3.2}$$

Due to the absence of dangling bonds at the surface, the formation of a robust interface bond between 2D materials and the contact metals is impeded, resulting in a large contact resistance. In addition, surface contamination, like polymer residues during fabrication, moisture and O_2 in air, can also impair the contact quality. Thus, it is imperative to eliminate the impact of contact resistance to accurately determine the sheet conductivity of 2D materials and calculate the carrier mobility.

One typical solution is to measure the device in a four-probe FET geometry, as illustrated in Figure 3.4d. Comparing to two-probe FETs, two more electrodes are fabricated at the edge of the semiconductor channel, with a small area contacting the material. In this way, the contact resistance is avoided by applying the source-drain current (I_{sd}) through the channel and measuring the voltage drop between probe 1 and 2 (V_{12}), with the gate voltage (V_g) tuning the conductivity of the semiconductor. Therefore, the sheet resistance or conductance measured by the four-probe configuration can be calculated by the following formula:

$$R_{2D} = \frac{1}{G_{2D}} = \frac{V_{12}}{I_{sd}} \tag{3.3}$$

And the contact resistance can be also extracted by using the equation 3.2.

Another important parameter to determine the performance of a FET device is the field effect mobility (μ_{FE}), which indicates the moving rate of charge carriers under an electric field (E), with the unit of $cm^2V^{-1}s^{-1}$. The two-probe field effect mobility in 2D materials can be calculated using the following equation:

$$\mu_{FE} = \frac{L}{W \times C_i \times V_{sd}} \times \frac{dI_{sd}}{dV_g} \tag{3.4}$$

where μ_{FE} is the field-effect mobility, L is the channel length, W is the channel width, C_i is the capacitance per unit area of the insulating layer, V_{sd} is the source-drain voltage, and dI_{sd} / dV_{g} is the slope of the output characteristics curve. While using the same formula to calculate field-effect mobility in four-probe measurements, the source-drain voltage, V_{sd}, is replaced by the voltage drop between probe 1 and 2 (V_{12}), and L represents the channel length between the two small probes.

In this thesis work, the electrical transport measurements on the FET devices are performed in a Janis Research 10 K closed cycle refrigerator in LANES laboratory, where the instruments are integrated and controlled by LabView software. Before loading the sample, the fabricated devices are annealed in a high vacuum tube furnace at 200 °C for 6 hours to remove the polymer residues and improve the contact adhesion. Then the device is installed onto a specific chip holder which fits the sample space inside Janis chamber, where the contact electrodes of the device can be wire-bonded. Afterwards, the sample is loaded into Janis chamber, followed by another in-situ annealing at 110 °C for 6 hours in high vacuum to remove moisture and O_2 absorbed on the surface. The temperature of the sample space can be controlled ranging from 10 K to 450 K by Lakeshore 336. When doing two-probe measurements, Agilent E5270B is used as the voltage source and ampere meter to apply source-drain voltage (V_{sd}) and gate voltage (V_{g}), and meanwhile measure the source-drain current (I_{sd}) and leakage current (I_{g}). For four-probe measurements, an additional Keithley 2000 voltmeter is used to measure the voltage drop V_{12}.

3.5.2 Superconductivity measurements

The CVD-grown NbS_2 crystals in Chapter 5 show a 3R to 2H phase transition dependent on their thickness, resulting in a metal to superconductor transition. To study their electrical behavior, especially superconductivity, four-terminal devices are fabricated on the NbS_2 flakes (Section 3.4), sharing a similar geometry as shown in Figure 3.4d to avoid contact resistance, where the source-drain current (I_{sd}) is applied through the two big electrodes and the voltage drop between the two small probes are measured as V_{12}. The resistance between the two probes can be calculated by:

$$R = \frac{V_{12}}{I_{\mathrm{sd}}} \tag{3.5}$$

When superconductivity occurs, the voltage drop between the two probes (V_{12}) should be

measured as zero, resulting in a zero resistance.

In this thesis work, NbS_2 devices are measured in a ICE Oxford Cryogen Free Continuous Flow Cryostat system in LANES laboratory, with the instruments integrated and controlled by LabView software. To eliminate the polymer residues and strengthen the contact adhesion, the devices are annealed at 200 °C for 6 hours in high vacuum tube furnace after fabrication process, followed by being wire-bonded onto a specific chip holder to fit the sample space inside ICE Cryostat chamber. The sample is immersed in a liquid helium (He) environment with a base temperature around 1.3 K, and the temperature of the sample space can be controlled within a range of 1.3 K to 260 K by Lakeshore 336. Temperature dependent four-probe longitudinal resistance (R_{xx}) are measured using SR860 lock-in amplifier with an AC probe current (I_{AC}) set at 100 nA and a frequency of 13.3 Hz. DC voltage-current (V-I) characteristics are measured by applying a constant DC current using a Keithley 2636B sourcemeter, while the DC voltage is measured with a Keithley 2182A nanovoltmeter. Four-probe differential resistance (dV_{AC}/dI_{AC}) is measured using the lock-in amplifier with AC probe current (I_{AC}) set at 100 nA and a frequency of 13.3 Hz, while simultaneously sweeping the DC current. An out-of-plane magnetic field can be applied on the sample by American Magnetics, Inc. Model 430, Power Supply Programmer.

3.5.3 Memory characterization

Hysteresis Measurement

Hysteresis behavior is a key characteristic of floating gate memory devices studied in this thesis work, which refers to the lag or delay in a system's response to changes in its input. When a programming voltage is applied, electrons are injected into the floating gate, increasing its negative charge and shifting the threshold voltage to a lower value. Conversely, when an erase voltage is applied, electrons are removed from the floating gate, decreasing its negative charge and shifting the threshold voltage to a higher value.

To investigate this behavior, a two-probe floating gate field-effect transistor (FGFET) is fabricated based on our 2D materials, as schematically shown in Figure 3.4b. 2D semiconductor used as active channel material is transferred on a Si/SiO_2 substrate, where 5 nm Pt is deposited as a floating gate and a stack of 2 nm Cr and 40 nm Pt is deposited as a local gate, with SiO_2 as dielectric layers. Ti/Au is deposited on the top of the material as electrode contacts to apply source-drain voltage.

Hysteresis behavior can be characterized by measuring the output current (I_{sd}) as a function of the gate voltage (V_g) while applying a source-drain voltage (V_{sd}). The gate voltage is swept from a minimum to a maximum value and then back again, while the current is continuously measured. Due to variations in the internal built-in charge storage at different gate voltages, the threshold voltage of a floating gate memory device changes in both the forward and reverse paths, which leads to the appearance of a memory window (V_{TH}) in the device characteristics,

indicating the delay in the device's response to changes of the applied gate voltage and a data storage range without causing damage to the device. Other information such as I_{ON}/I_{OFF} ratio and slew rate can also be extracted from this curve.

Furthermore, to study the *I-V* characteristics of the memory devices, the source-drain current (I_{sd}) is measured while sweeping the source-drain voltage (V_{sd}). Differing from the traditional FET, an additional step is necessary before each measurement to set a constant initial charge in the floating-gate voltage, where the device is first reset at a voltage (V_{reset}) ramping from 0 V. Afterwards, the gate voltage is ramped up to a programming voltage ($V_{g,\,program}$) to write the memory and then reduced to a read voltage ($V_{g,\,read}$) which is kept constant during each measurement. In this way, the *I-V* curves show the output characteristics of the memory device under various programming voltages.

Retention time

In a floating gate memory device, the charge stored in the floating gate determines the threshold voltage of the device. Over time, the charge can leak out due to various physical mechanisms, causing the threshold voltage to shift and potentially leading to data loss. Retention time is an important parameter which characterizes the data storage ability of a floating gate memory device, defined as the period of time over which a memory device can retain its programmed state within an acceptable range of threshold voltage variation.

In this thesis work, memory elements are employed as mainly programmable resistances, so we use the evolution of source-drain conductance values (G_{sd}) instead of the threshold voltage (V_{TH}) to analyze the retention time. Prior to the measurements, the device is first reset at a voltage (V_{reset}) ramping from 0 V to set a constant initial charge in the floating gate among each measurement. Subsequently, a programming voltage ($V_{g,\,program}$) is applied by ramping gate voltage to write the memory and then reduced to a read voltage ($V_{g,\,read}$) which is kept the same value during various measurements. From this moment, the source-drain current (I_{sd}) is recorded as a function of time with a constant source-drain voltage applied.

Since the retention time usually lasts for years or even tens of years at room temperature, it's very time-consuming to measure the actual value of retention time. One practical way is to test the sample at an elevated temperature and calculate the equivalent retention time at room temperature by using the following Arrhenius model:

$$A_f = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_n} - \frac{1}{T_e}\right)\right] \tag{3.6}$$

where A_f is the acceleration factor, E_a is the activation energy (A typical activation energy is 0.8 eV for effects related to charge loss when no voltage is applied to the device), k is Boltzmann's constant (8.617×10^{-5} eV/K), T_n is the temperature of the normal environment and T_e is the elevated temperature. The conductance exhibits a faster degrading rate at the elevated

temperature (t_e) and the retention time can be recorded straightforwardly. An acceleration factor A_f can be calculated by the Arrhenius model, which means that if the data lasts for t_e at the elevated temperature, it would last A_f times longer at room temperature, corresponding to the equivalent retention time at room temperature.

Endurance test

Endurance is a crucial parameter which shows the capability of a floating gate memory device to withstand repeated program and erase operations without failure, defined as the number of cycles that these operations can be performed before causing damage to the device or significant changes in its performance. In this thesis work, the endurance of memory is measured by applying programming/erasing (P/E) cycles and then recording the source-drain current (I_{sd}) after each pulse at a constant source-drain voltage (V_{sd}) and read voltage ($V_{g,\,read}$). Each P/E cycle consists of a 100 ms +11.5 V pulse for the erase operation, and a 100 ms -11.5 V pulse for the program operation.

In this thesis work, the above memory characterizations on the FGFET devices are conducted in a Janis Research 10 K closed cycle refrigerator in LANES laboratory. Before measuring, the device is first annealed in a high vacuum tube furnace at 200 °C for 6 hours to enhance contact adhesion and eliminate polymer residues, and then installed onto a specific chip holder allowing for wire-bonding of the contact electrodes, which fits the sample space inside Janis chamber. Afterwards, the sample is loaded into Janis chamber and undergoes another in-situ annealing at 110 °C for 6 hours in high vacuum to remove moisture and O_2 absorption. The temperature of the sample space can be controlled by Lakeshore 336 within a range of 10 K to 450 K. During measurements, Agilent E5270B is utilizedd as the voltage source and ampere meter to apply source-drain voltage (V_{sd}) and gate voltage (V_g), while simultaneously measuring the source-drain current (I_{sd}) and leakage current (I_g).

4 Wafer-scale monolayer MoS_2 grown by MOCVD

4.1 Introduction

4.1.1 State of art: synthesis of 2D monolayer MoS_2

Since the first isolation of graphene in 2004 [1], significant attention has been focused on 2D material exploration and nanoscale device fabrication. Among these 2D materials [12], TMDCs are considered as a promising material platform for realizing scaled semiconducting devices and circuits due to their unique band structures[3] and extraordinary properties [116], [43]. In particular, monolayer molybdenum disulfide (MoS_2) possesses a large direct bandgap of 1.8 eV [21] and shows a strong ability to modulate the semiconducting channel with a high on/off current ratio of 10^8 [23], which reveals its potential to develop next-generation electronics [117], [118], [119], [120], [121] and realize the extension of Moore's law in advanced technological nodes [122], [123]. To fully exploit its appealing properties and advance its industrial applications, it is necessary to develop a scalable and reproducible method to synthesize high-quality monolayer MoS_2 on a wafer scale.

Due to the weak van der Waals interactions between neighboring layers, TMDC flakes can be easily obtained by mechanical exfoliation from their bulk crystals [103]. However, further applications in industry are limited by the small size, random shapes, and uncontrollable thickness of the flakes. Alternatively, chemical vapor deposition (CVD) has been widely used for synthesizing semiconducting TMDCs with a large domain size and controllable thickness [100], [74], [124], [125]. Solid-phase precursors are usually utilized in CVD process, such as sulfur (S), molybdenum oxide (MoO_3) and tungsten oxide (WO_3), whose evaporation rate is difficult to be controlled stably during the whole process, resulting in a non-uniform growth. In addition, the distance between the source and substrate makes significant difference in nucleation density, also causing a nonuniformity in wafer-scale growth. As an advanced version of CVD technique, metal-organic chemical vapor deposition (MOCVD) ensures a stable precursor supply by using gaseous precursors, such as $Mo(CO)_6$, $W(CO)_6$, diethyl sulfide ($(C_2H_5)_2S$) and H_2S), enabling a wafer-scale uniformity and precise layer number control [126], [127], [128].

4.1.2 Outline of this chapter

In this chapter, we will demonstrate the synthesis of 2-inch wafer-scale monolayer MoS_2 by MOCVD method and its applications in logic-in-memory computing and artificial neural networks. In Section 4.2.1, we demonstrate the growth process of 2-inch monolayer MoS_2 using a home-built quartz tube furnace. To achieve monolayer growth, we optimize several growth parameters (Section 4.2.2), adopt the sodium (Na) assisted MOCVD growth and the etching-gas confined MOCVD growth to decrease the nucleation density and promote the lateral growth of the crystals. In Section 4.2.3, we perform atomic force microscopy (AFM), Raman spectroscopy, Photoluminescence (PL), aberration-corrected scanning transmission electron microscopy (STEM) to characterize the MOCVD-grown monolayer MoS_2. In Section 4.3, we further apply our 2-inch monolayer MoS_2 to logic-in-memory computing, artificial neural networks and vector–matrix multiplication processor, from which we believe that these results pave the way for the future industrial application of 2D materials.

The main ideas and methods in this chapter are developed by Zhenyu Wang and Prof. Andras Kis, with most experiments and analysis performed by Zhenyu Wang, while the work in some subsections is performed in close and fruitful collaboration with my colleagues in LANES and LBEN laboratory, as listed below. In Section 4.2.1 about the MOCVD growth process, the CVD setup is improved together with Dr. Michal Macha with supervision of Prof. Aleksandra Radenovic. In Section 4.2.2 about the optimization of MOCVD growth, the experiments and analysis are performed with initial assistance of Dr. Jing Zhang and Dr. Yanfei Zhao. In section 4.2.3 about the characterizations of MOCVD-grown MoS_2 film, STEM measurements and analysis are performed by Dr. Mukesh Tripathi. In section 4.3 about the applications of MOCVD-grown monolayer MoS_2 film, the device fabrication and electrical measurements are performed by Dr. Guilherme Migliato Marega with MoS_2 film produced by Zhenyu Wang.

The results in this chapter are published in **Nature**, 2020 (doi: 10.1038/s41586-020-2861-0), **ACS Nano**, 2022 (doi: 10.1021/acsnano.1c07065) and **Nature Electronics**, 2023 (doi: 10.1038/s41928-023-01064-1), respectively. Thus, there is considerable overlap between these three articles [117], [129], [130] and this chapter.

4.2 2-inch monolayer MoS_2 growth with tube furnace MOCVD

4.2.1 Growth process

Our wafer-scale growth of continuous monolayer MoS_2 films was performed in a 4-inch home-built quartz tube furnace, as introduced in Figure 3.1. 2-inch sapphire ($Al_2O_3(0001)$) wafers were annealed at 1000 °C for 6 h before growth process, which helps to produce atomically ultra-smooth surfaces of sapphire [74]. Then the wafers were pre-treated with 3 wt.% KOH to make the surface hydrophilic and spinning-coated with sodium molybdenum (Na_2MoO_4) and sodium chloride (NaCl). Na_2MoO_4 provides molybdenum (Mo) precursor at the beginning of the growth and promotes the initial nucleation. NaCl helps to enlarge domain size by

decreasing the nucleation density [109] and accelerate growth rate by reducing the energy barrier [22], which will be discussed in detail in Section 4.2.2. After these preparation steps, the sapphire wafer was vertically carried by a quartz boat and loaded into the quartz tube furnace for MOCVD growth. To remove the remaining air and create an inert atmosphere, the entire chamber was pumped into vacuum and purged with argon (Ar) gas several times. Molybdenum hexacarbonyl ($Mo(CO)_6$) and diethyl sulfide ($(C_2H_5)_2S$) and H_2S) were used as Mo and S gaseous precursors during growth process, respectively. The precursors were stored inside a bubbler whose temperature was maintained at 25 °C. Small amount of hydrogen (H_2) and oxygen (O_2) were mixed with Argon (Ar) as carrier gases, for steady evaporation and balancing the growth rate by etching effect [110], [131], which will be also discussed in detail in Section 4.2.2.

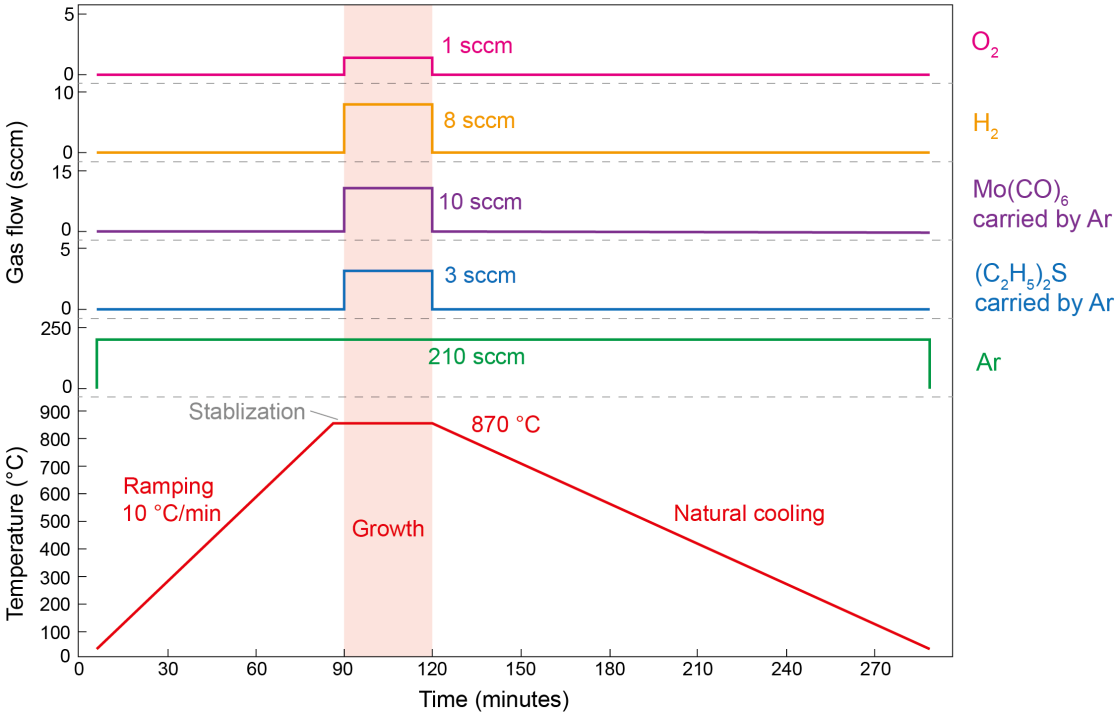

Figure 4.1: An exemplary process flow of MOCVD growth of monolayer MoS_2. All growths are carried out at atmospheric pressure and at a temperature of 870 °C, with a carrier Ar flow of 210 sccm, while the gas flow rate of O_2, H_2 and the precursors are slightly varied among different growth runs. The $Mo(CO)_6$ and $(C_2H_5)_2S$ precursors are carried by Ar gas from a bubbler, which is constantly kept at 25 °C in a water bath.

Figure 4.1 presents a typical process flow of MOCVD growth of monolayer MoS_2, with temperature and gas flow controlled by a LabVIEW program. The furnace was first heated to 870 °C with a Ar gas flow of 210 sccm and stabilized for 5 min. Growth started when $Mo(CO)_6$ and $(C_2H_5)_2S$ and H_2S precursors were carried into the chamber by 10 sccm and 3 sccm of Ar flow, respectively. With continuous precursor supply, monolayer island domains extend to a large area and finally immerge in a continuous film. The growth process lasts for 30 min at atmospheric pressure and at a temperature of 870 °C. Immediately after the growth, the gas

supply of $Mo(CO)_6$, $(C_2H_5)_2S$ and H_2S, O_2 and H_2 was cut off, while Ar continued flowing to remove the residue during the natural cooling down until room temperature. In later sections, to optimize the growth conditions, possible changes are made to the flow rate of $Mo(CO)_6$, $(C_2H_5)_2S$ and H_2S, O_2 and H_2, and the concentration of Na_2MoO_4 and NaCl.

4.2.2 Optimization of growth process

To obtain a continuous and uniform MoS_2 monolayer growth on a 2-inch sapphire wafer, we optimized several growth parameters in this section. Our MoS_2 film is grown in the layer-by-layer growth mode [108], which is ideal for uniform layer control over the large scale [111]. The layer-by-layer growth of MoS_2 film was observed only when we applied a low flow rate of $Mo(CO)_6$, as shown in Figure 4.2a-b. The growth at a higher flow rate of $Mo(CO)_6$ will lead to a mixture of monolayer and multilayer regions, as shown in Figure 4.2c. Therefore, it's preliminary and necessary to keep a low partial pressure of Mo vapor over the entire process to get a uniform monolayer growth.

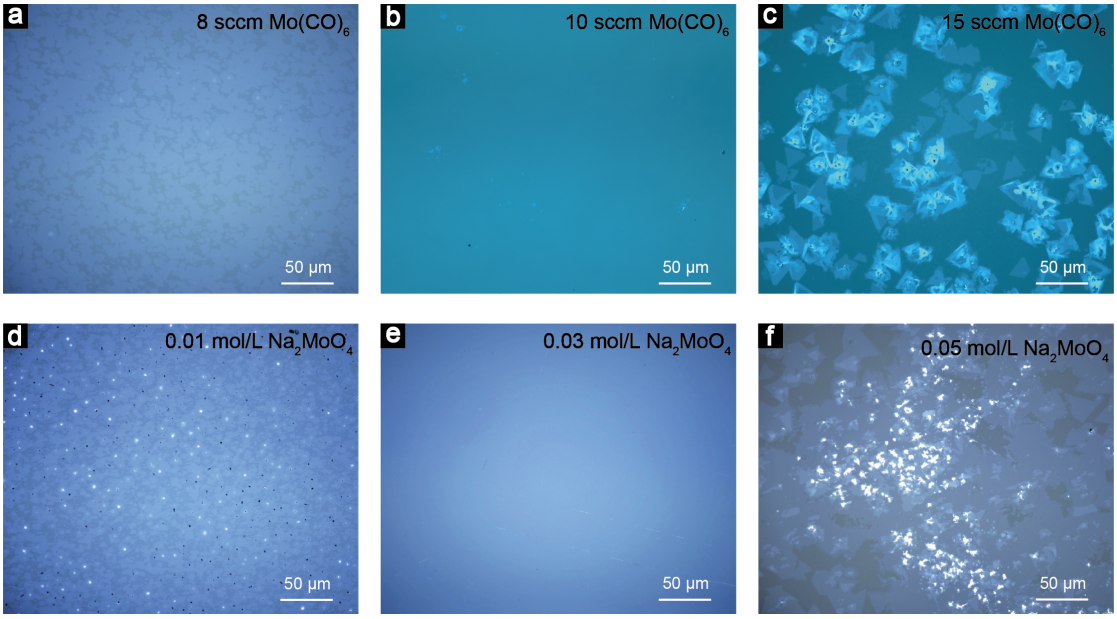

Figure 4.2: MoS_2 growth dependence of Mo precursors in MOCVD. The optical microscope images of MoS_2 film grown by MOCVD with a $Mo(CO)_6$ flow rate of (a) 8 sccm, (b) 10 sccm and (c) 15 sccm, and with a Na_2MoO_4 concentration of (d) 0.03 mol/L, (e) 0.01 mol/L and (f) 0.05 mol/L, respectively. The other parameters were kept identical except the unique variable factor among each growth run. A higher coverage was observed with increasing amount of $Mo(CO)_6$ or Na_2MoO_4 but multilayer growth dominates when excessive Mo precursors were applied.

We spin-coat Na_2MoO_4 on the substrate before loading, as described in Section 4.2.1. Tiny flakes or nucleus of MoS_2 generated from the initial growth provide positions with high chemical potential energy on the substrate, which promotes deposition of MoS_2 crystals

produced from the gaseous precursors. From our experimental results, no MoS_2 was observed on the wafer after growth without pre-coated Na_2MoO_4, even if increase the gas flow of $Mo(CO)_6$, indicating Na_2MoO_4 plays a necessary role on precursor deposition. An increasing Na_2MoO_4 concentration enlarges the coverage of MoS_2 film but excessive concentration leads to a multilayer growth, as shown in Figure 4.2d-f. Thus, 0.03 mol/L Na_2MoO_4 gives the best growth results according to our optimized recipe.

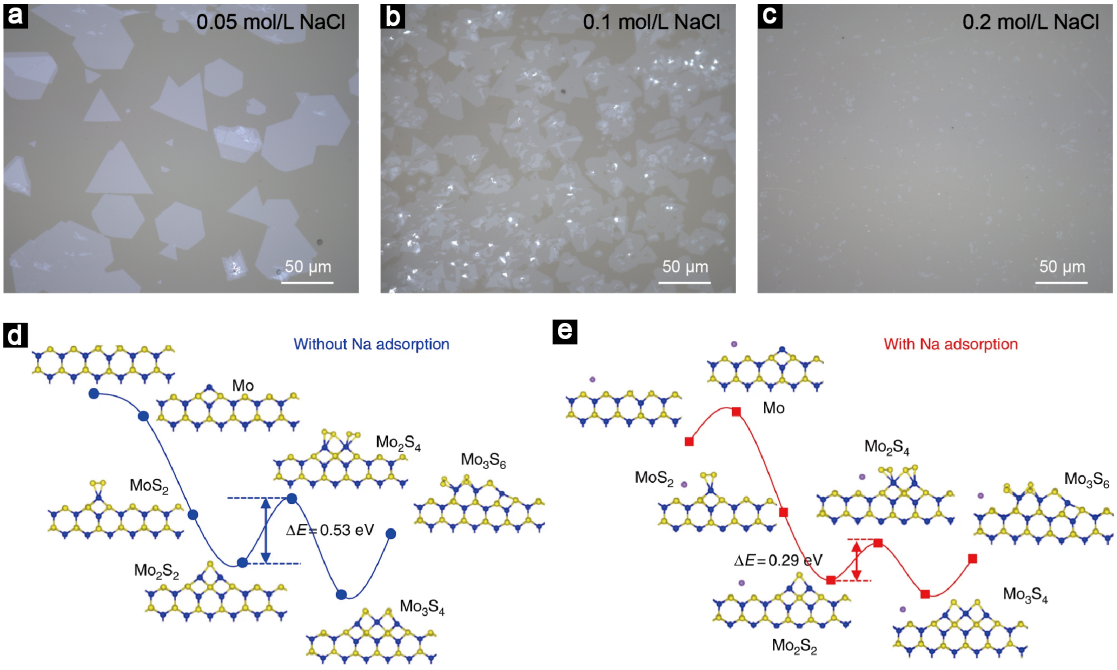

Figure 4.3: Na-assisted MOCVD growth of MoS_2 film. (a-c) The optical microscope images of MoS_2 film grown by MOCVD with a NaCl concentration of 0.05 mol/L, 0.1 mol/L and 0.2 mol/L, respectively. The other parameters were kept the same among each growth run. (d-e) The catalytic effect of Na in accelerating the growth of monolayer MoS_2, reproduced from [22].

Figure 4.3a-c show the effect of pre-coated NaCl concentration on film coverage. Growth of monolayer triangular flakes is dominant when lower NaCl concentrations are used. With incorporation of NaCl, nuclear density decreases and molybdenum oxychloride is formed [132], which has a lower melting point and higher chemical reactivity, accelerating growth rate and enlarger domain size. With 0.2 mol/L NaCl, MoS_2 grow to large domains and subsequently merge into continuous film.

The usage of alkali-based compounds in the MOCVD growth of MoS_2 was first reported by [111], and several following works also showed similar results [109], [22], [132]. The underlying reason for its promotion effect was revealed by Yang et al. [22] and Song et al. [132], where sodium (Na) serves as the reaction catalyst and decreases the energy barrier required for the formation of an intermediate product (Figure 4.3e-f). The highest energy barrier is reduced from 0.53 eV to 0.29 eV with Na as the catalyst, leading to a 17 times higher growth rate for the S-terminated edges.

During growth process, a small amount of O_2 is used for an etching-gas confined growth and the results are presented in Figure 4.4a-c. Tiny flakes with high nucleation density were observed when no O_2 was introduced. When increasing O_2 gas flow, a larger domain size and a higher coverage were achieved with a suppressed nucleation density. Due to the strong etching effect, 1 sccm of O_2 was chosen as the optimal flow rate to get a stable monolayer growth. The mechanism of O_2 confined growth can be explained as follows [110]. Unstable nuclei are removed by reacting with O_2 and thus the nucleation density of MoS_2 is substantially decreased to enable large domain growth. Meanwhile, the usage of O_2 prevents MoO_2 from chemically reducing to Mo, which requires a much higher energy barrier to form MoS_2.

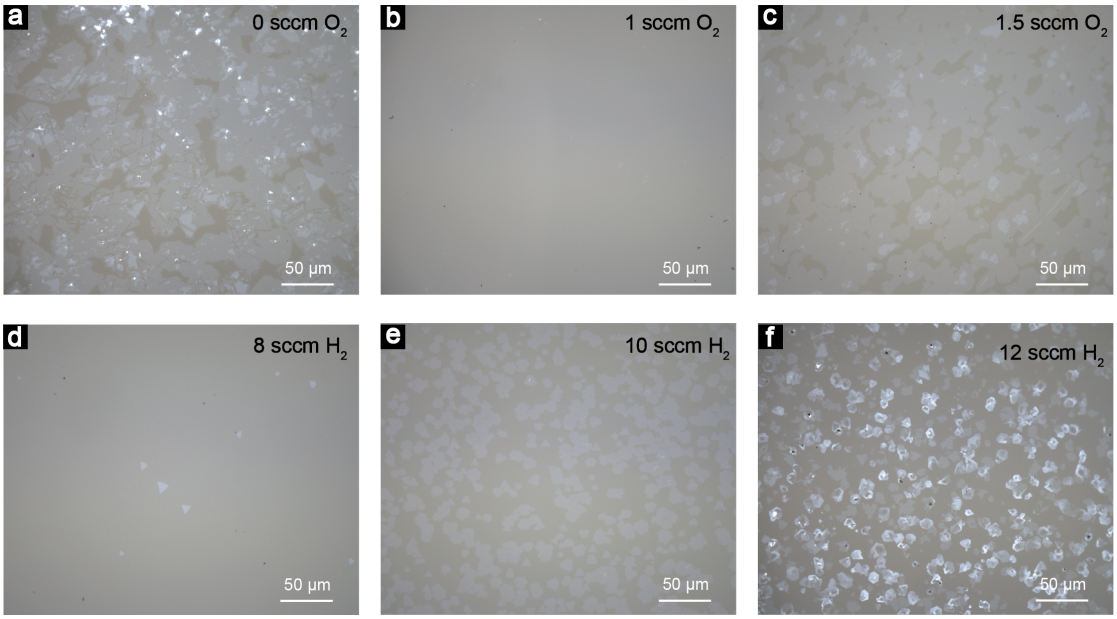

Figure 4.4: Etching-gas confined MOCVD growth of MoS_2 film. The optical microscope images of MoS_2 film grown by MOCVD with a O_2 flow rate of (a) 0 sccm, (b) 1 sccm and (c) 1.5 sccm, and with a H_2 flow rate of (d) 8 sccm, (e) 10 sccm and (f) 12 sccm, respectively. The other parameters maintained the same except the unique variable factor among each growth run.

Since $(C_2H_5)_2S$ precursor is used in our MOCVD process, which easily generates carbon contamination, H_2 is also introduced to the growth chamber to remove carbon contamination[26]. However, an obvious tendency to smaller monolayer-MoS_2 grain size and emergence of bilayer-MoS_2 were observed with an excessive H_2 gas flow in previous works [133], [111], also shown by our experimental results in Figure 4.4d-f. On one hand, H_2 is a chemical reducing gas which has desulfurization and etching effect to MoS_2 flakes. On the other hand, the main reactant, MoO_x can be further reduced to Mo by H_2, which is difficult to react with sulfur precursors and deposited on the substrate directly. This will block the lateral growth and affect the continuity of the film, resulting in a growth of multilayer MoS_2. Thus, an optimal H_2 flow rate was explored as 8 sccm in our growth recipe, which effectively removes carbon contamination and get good quality and uniformity of monolayer MoS_2.

4.2.3 Characterization of MOCVD-grown monolayer MoS_2 film

To examine the quality of our as-grown MoS_2 film, AFM, Raman spectroscopy, PL, and aberration-corrected STEM are used in this section for characterization.

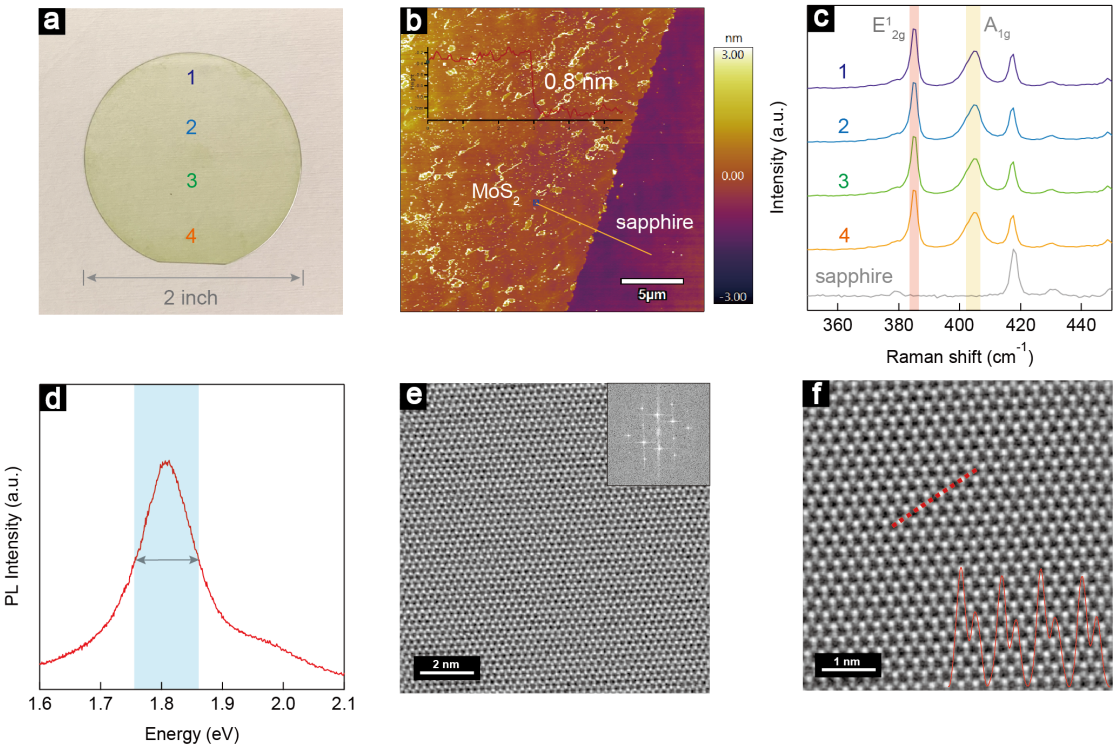

Figure 4.5: Characterizations of MOCVD-grown monolayer MoS_2 film. (a) The optical microscope image of a typical as-grown MoS_2 film on a 2-inch sapphire wafer. (b) AFM image of an as-grown MoS_2 film on a sapphire substrate, with a height profile showing the thickness of 0.8 nm. (c) Room-temperature Raman spectra obtained on different regions of the MoS_2 film shown in (a) and a bare sapphire substrate as comparison. (d) PL spectrum acquired at room temperature of as-grown MoS_2 film on sapphire. The signal from sapphire background has been removed.(e) STEM image showing a large region of monolayer MoS_2. Inset: FFT image showing the crystalline monolayer MoS_2 structure. (f) A magnified filtered STEM image taken from (e) showing the 2H crystal structure of monolayer MoS_2, with the intensity line profiles taken along the dashed line.

Figure 4.5a shows the photograph of typical as-grown MoS_2 film (greenish yellow) on a 2-inch sapphire wafer. Figure 4.5b displays the atomic force microscope (AFM) image as well as its corresponding height profile of the MoS_2 film on a sapphire substrate, which indicates a thickness of 0.7 nm for monolayer MoS_2 with a smooth surface. Figure 4.5c demonstrates the room-temperature Raman spectra collected from different positions on the MoS_2 film. All the Raman spectra demonstrate two typical peaks at 383 cm^{-1} ($E^1{}_{2g}$) and 402 cm^{-1} (A_{1g}), confirming the monolayer nature of MoS_2 and a uniform growth all over the wafer. PL spectrum of as-grown MoS_2 on sapphire (presented in Figure 4.5d) measured at room temperature exhibit a strong emission from the A exciton at 1.83 eV with a narrow full width at half-maximum

(FWHM), which shows the characteristic of the direct band gap of monolayer MoS_2 [21].

To further study the atomic structure, as-grown monolayer MoS_2 film was transferred onto a transmission electron microscopy (TEM) grid and aberration-corrected scanning TEM (STEM) measurements were performed on it and demonstrated in Figure 4.5. Atomically resolved STEM image in Figure 4.5e shows a large contamination-free region of monolayer MoS_2, with its corresponding fast Fourier transform (FFT) amplitude spectrum in the inset displaying the crystalline monolayer MoS_2 structure. A magnified filtered STEM image in Figure 4.5f shows the 2H crystal structure of monolayer MoS_2. The intensity line profile at bottom right was taken along the dashed line in the image, and show the peak positions of Mo atoms and S atoms.

4.3 Applications of MOCVD-grown monolayer MoS_2

4.3.1 Logic-in memories

Emerging data-intensive applications in the fields, such as machine learning and the Internet of Things, are driving the need to develop energy-efficient electronic hardware. Compared with von Neumann architectures, which uses separate processing and storage units, in-memory computing uses the same basic device structure for logic operations and data storage [134], [135], [136], and considered a promising candidate to reduce the energy cost of data-centered computing. The success of this approach depends strongly on identifying an ideal material system suitable for such device designs. 2D materials such as semiconducting TMDCs, could be an ideal material system for such architecture due to their exceptional electrical and mechanical properties, as discussed in Section 4.1.

In this section, we use our MOCVD-grown MoS_2 film as an active channel material for developing logic-in-memory devices and circuits based on floating-gate field-effect transistors (FGFETs). Figure 4.6a shows an optical micrograph of a fabricated memory array based on FGFETs. Each FGFET has a local Cr/Pd (2 nm/80 nm) bottom gate and a thin-film Pt floating gate (5 nm thickness), with HfO_2 deposited for both blocking and tunnel oxides (30 nm and 7 nm thick, respectively). The conductance of our FGFETs can be precisely and continuously tuned, allowing us to use them as building blocks for reconfigurable logic circuits. Logic-in-memory units can be connected in parallel to execute more complex operations, and the signal can be transferred to the next set of units, creating a structure like a field-programmable gate array. Figure 4.6b demonstrates two-input logic-in-memory unit cell capable of acting as a universal logic gate as well as the concept of a three-input cell, which increases the functionality that can be implemented compared to a two-input structure. As a proof of concept, three-input cell operating in one of its possible states, three-input NAND is displayed in Figure 4.6c.

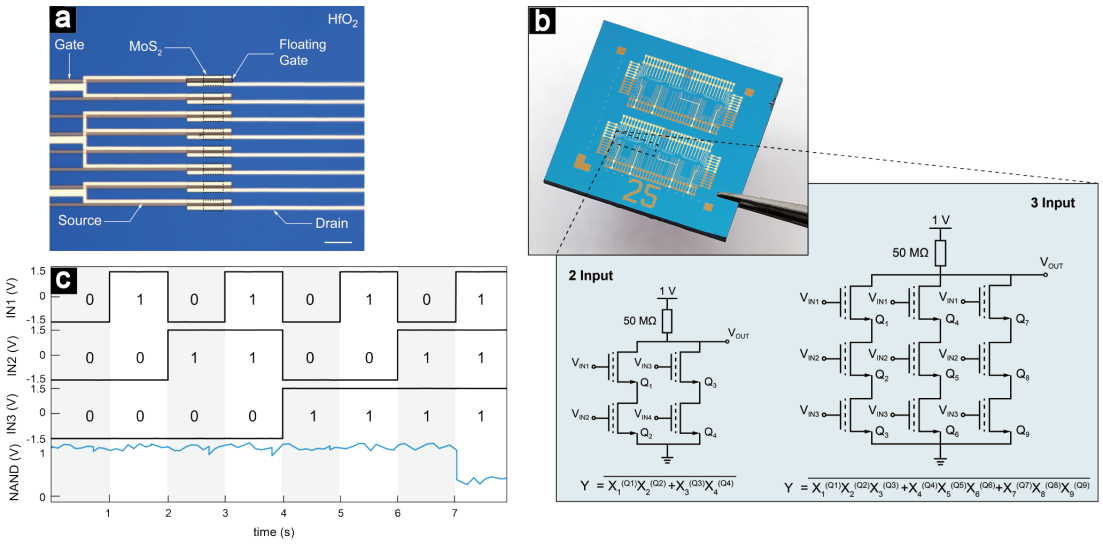

Figure 4.6: Logic-in memory based on MOCVD-grown MoS_2 film (a) Optical image of the fabricated floating-gate memory array, comprising eight memory cells (boxed). Scale bar, 10 μm. (b) Top left, photograph of a fabricated 12 mm by 12 mm die with logic-in-memory cell arrays. The boxed area contains two-input and three-input logic-in-memory cells, and their schematics are shown below with Y the output logic function. (c) Time traces showing stability of the output voltage for the NAND operation of the three-input unit cell.

4.3.2 Artificial neural networks

Modern processors perform many functions needed for the operation of our electronic devices, which increases the consumption of computing energy by transferring data between the memory and the processor. As introduced in Section 4.3.1, this data transfer bottleneck can be avoided by performing computation directly in the memories' physical layer, instead of the separation of processing and memory units in the von Neumann architecture. This type of in-memory processing satisfies the architecture to realize energy efficiency of processors for specialized data-driven applications, such as artificial neural networks (ANN).

In this section, we demonstrate an in-memory, general purpose processor based on an array of floating-gate memories with MOCVD-grown monolayer MoS_2 as an active channel. Figure 4.7a presents the three-dimensional schematic and the cross sectional view of our floating-gate memory array, with the optical micrograph of a fabricated memory array shown in Figure 4.7b. Wafer-scale, continuous and large-grain monolayer MoS_2 grown using MOCVD is transferred on top of a stack of bottom gate and floating gate, and contacted using titanium-gold (Ti/Au) as drain-source electrodes. The devices have a channel length and width of 1 and 12.5 μm, respectively. Individually addressable devices are connected in parallel for performing in memory the multiply-accumulate (MAC) operations using Kirchoff laws for summation and Ohm's law for multiplication, as schematic in Figure 4.7a inset.

As a proof of concept, we demonstrate an artificial neural network based on a circuit com-

posed of seven memory devices connected in parallel. We perform digit classification of artificially generated inputs containing noise, corresponding to a seven-segment LCD display, as presented in Figure 4.7c. This display configuration was widely used in the past where spurious signal variations cause a noisy representation of numbers that standard classification methods have difficulty of classifying. To perform a robust figure classification, we present the schematics of the one-layer perceptron network in Figure 4.7d with a SoftMax activation function in the output layer. The dot-product operation is performed in memory while the nonlinear function is implemented numerically in the acquisition system. Figure 4.7e presents a sample of the acquired output signal after the physical multiplication-accumulation operation without the SoftMax function and with the digital gain used for scaling the physical values to the abstract numbers of the neural network. We achieve a maximum accuracy of 91.5%, compared to the 95.5% accuracy estimated in the software model, classifying up to 10000 numbers/s. This measurement is performed with 4-bit precision programming and an input signal with added white noise having a standard deviation $\sigma = 0.1$.

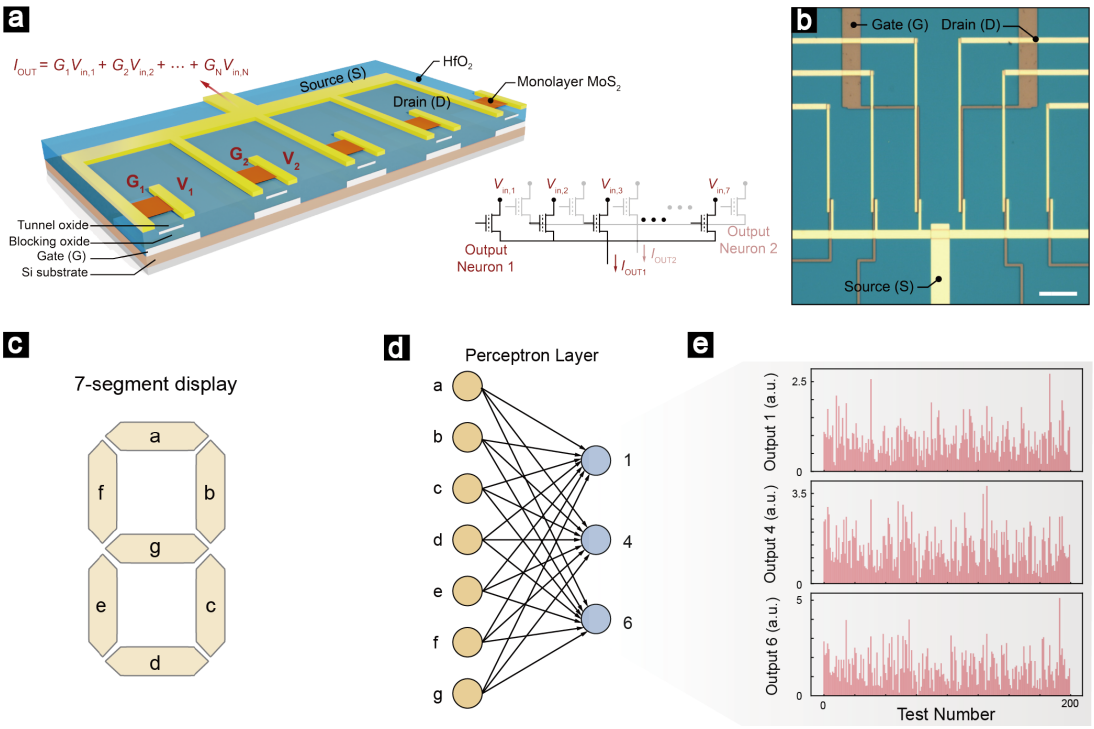

Figure 4.7: Artificial neural networks based on MOCVD-grown MoS_2 film (a) 3D schematic representation of the MoS_2 memory device array and the corresponding circuit schematic for the multiplication-accumulation operation. (b) Optical image of an array of memories connected in parallel. scale bar: 50 μm.(c) Representation of a seven-segment display. (d) One-layer perceptron network for seven-segment figure classification. (e) Sample of inference operations after different test signals are sent to the input layer and measured in one of the neurons.

4.3.3 Vector–matrix multiplication processor

As shown in Subsection 4.3.1 and 4.3.2, floating-gate field-effect transistors based on MoS_2 have been used in logic-in-memory and in-memory computing as well as the main building blocks of perceptron layers. In this subsection, we demonstrate another application of MOCVD-grown MoS_2 in an integrated 32 × 32 vector–matrix multiplier with 1,024 FGFETs.

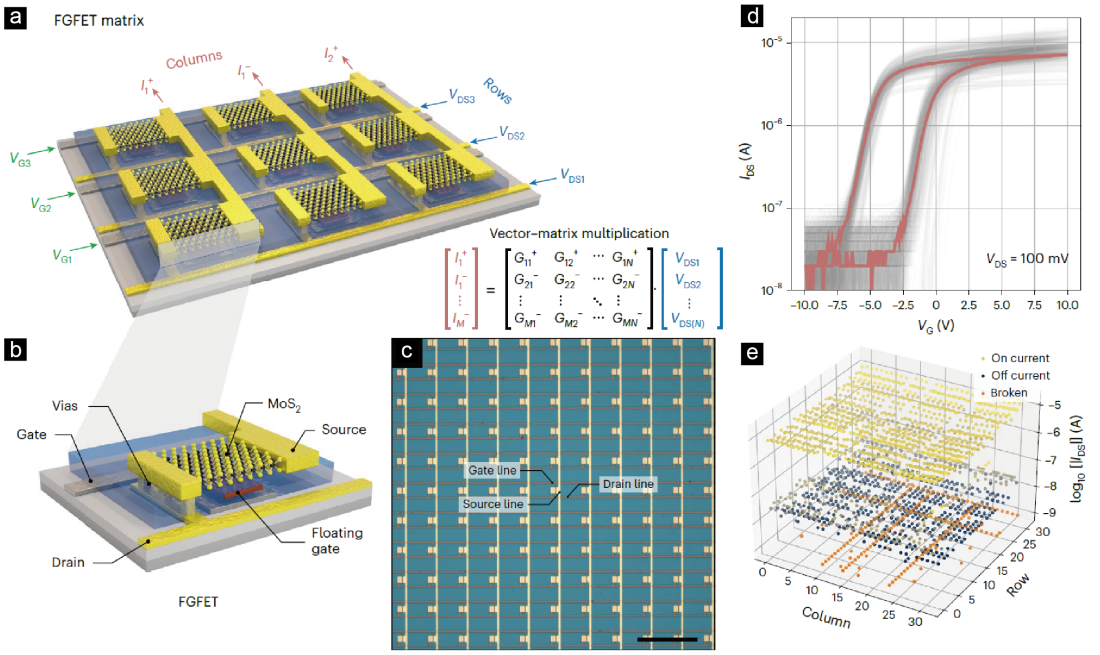

Figure 4.8: Vector–matrix multiplication processor based on MOCVD-grown MoS_2 film (a) Three dimensional illustration of vector–matrix multiplication processor by connecting the FGFETs. The inset shows the correspondence between signals and vector–matrix multiplication (b) Cross section of the FGFET device based on MOCVD-grown monolayer MoS_2. (c) Optical image of the memory matrix configuration. Scale bar: 500 μm. (d) I_{DS} versus V_G hysteresis curves of the 851 working devices; the red curve highlights the behaviour of one of the 851 memory devices. (e) Three dimensional plot shows the mapping of the ON and OFF currents on the 32 × 32 chip taken at V_{DS} = 100 mV.

Figure 4.8 a and b illustrate the structure of the memory matrix and an individual FGFET, respectively. The use of a matrix configuration allows a denser topology and directly corresponds to performing vector–matrix multiplications. The memories are controlled by the local gates made by 2 nm/40 nm Cr/Pt and the floating gates made by a 5 nm Pt layer. 30 nm HfO_2 and 7 nm HfO_2 are deposited as block oxide and tunnel oxide, respectively. Wafer-scale MOCVD-grown MoS_2 is transferred on top of the gate stack and etched to form the transistors' channels, with a stack of 2 nm/60 nm Ti/Au patterned and evaporated on the top as the drain–source contacts.

The I_{DS} versus V_G curves of each FGFET device in Figure 4.8d shows a high yield (83.1%) and low device-to-device variability, which are prerequisites for practical applications. Further-

more, Figure 4.8e shows a good distribution of the ON and OFF current distribution over the entire memory matrix. The processor carries out vector–matrix multiplications and illustrates its functionality by performing discrete signal processing.

4.4 Conclusion

In this chapter, 2-inch wafer-scale monolayer MoS_2 is synthesized by MOCVD method. The optimization of growth parameters to achieve continuous and uniform monolayer is discussed in detail, including the amount of Mo precursors, the effect of NaCl, and etching-gas confinement. Several characterization techniques, such as AFM, Raman, PL and STEM, are then employed on the as-grown MoS_2 film to confirm a high crystal quality and a nature of monolayer growth. Furthermore, the 2-inch monolayer MoS_2 is used as active channel material to develop logic-in memory devices, artificial neural networks and vector–matrix multiplication processor, opening the way to the realization of energy-efficient circuits based on 2D materials for machine learning, the Internet of Things and non-volatile computing.

5 Superconducting 2D NbS_2 grown epitaxially by CVD

5.1 Introduction

5.1.1 2D metallic TMDCs

Semiconducting two-dimensional (2D) transition metal dichalcogenides (TMDCs) have been heavily studied owing to their layer-number dependent bandgap [45] and outstanding performance as field-effect transistors [23] and optoelectronic devices [104]. In contrast to semiconducting TMDCs, metallic TMDCs (e.g., NbS_2, $NbSe_2$) are attracting great attention in the context of realizing 2D metal-semiconductor junctions with semiconducting TMDCs [71], [137] with the aim of lowering contact resistance by weakening Fermi level pinning [6]. They are expected to be ideal 2D metal electrodes thanks to their van der Waals (vdW) interaction and small lattice mismatch with other TMDCs [12], enhancing electrical performance compared to conventional 3D metal electrodes. Additionally, these metallic TMDCs hold interesting low-temperature properties such as superconductivity [65],[138] magnetism [139] and charge density waves (CDW) [140], [141], where superconducting TMDCs could be used to observe Andreev reflection in 2D systems [142], [143] and realize Josephson junctions [144].

5.1.2 State of art: electrical properties and synthesis of 2D NbS_2

Among metallic TMDCs, 2H-NbS_2 is a peculiar case in that it is the only superconductor with no CDW instabilities observed experimentally [65]. This is unusual if compared with other isostructural and isoelectronic 2H-$NbSe_2$ and 2H-TaS_2, where superconductivity coexist with CDW order. Theoretical work, however, points out 2H-NbS_2 is on the verge of CDW order in the 2D limit [145] or even close to spin density wave instabilities [146] possibly induced by magnetic impurities [147]. This makes 2D NbS_2 an appealing material platform to explore quantum phase transitions. These interesting electronic properties and their potential device applications motivate the development of methods to synthesize 2D metallic and superconducting NbS_2.

Niobium disulfide (NbS_2) mainly exists in two polytypes: rhombohedral (3R) and hexagonal (2H), which exhibit distinct electrical properties. Figure 5.1 illustrates the atomic structures of NbS_2 with 3R and 2H polytype stacking. Each layer is composed of a single 1H layer where the Nb atoms are coordinated in a trigonal prismatic shape, while adjacent layers interact via the van der Waals force and maintain the interlayer distance of around 0.7 nm [148]. The two polytypes are distinguished by relative rotation and atom alignment between the neighboring planes [149]. In 3R-NbS_2, metallicity has been confirmed with a minimum resistance at around 30 K [150]. On the other hand, superconductivity can be observed in 2H-NbS_2 bulk below a transition temperature (T_c) of 6 K [65]. These two phases can be selectively grown in bulk by changing the sulfur pressure [151], whereas reports on control over the polytypes in the few-layer limit are rare.

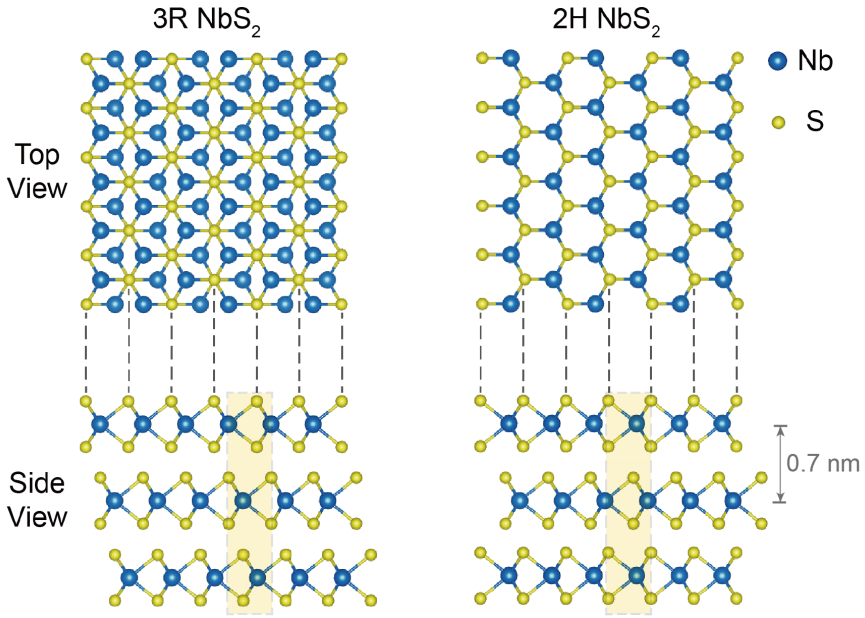

Figure 5.1: Atomic structures of NbS_2 with different polytype stackings. Side and top views of atomic structures of NbS_2 with 3R-polytype stacking and 2H-polytype stacking.

Although 2D NbS_2 can be obtained by mechanical exfoliation from bulk crystals [152], [153], the flakes are usually several µm in size with little control over the thickness. In recent years, several attempts of growing NbS_2 using CVD have been reported [150], [114], [154]. Nevertheless, only 3R-phase metallic NbS_2 has been grown, with a limited domain size and lack of precise layer number control. Growing large-grain and superconducting 2H-phase NbS_2 with controllable thickness has not been reported yet, hindering exploration of 2D superconducting properties and further applications in electrical devices.

5.1.3 Outline of this chapter

Here in this chapter, we demonstrate epitaxial CVD growth of 2D NbS_2 single crystals and continuous transition from a metallic 3R-polytype to superconducting 2H-polytype with respect to its thickness (Section 5.2). The growth process is presented in detail in Section 5.2.1, followed by the growth morphologies induced by growth temperature and H_2S:Ar ratio (Section 5.2.2). In the optimized growth recipe, our NbS_2 flakes have a rectangular shape with a large grain size exceeding 500 μm and are highly-aligned by quasi van der Waals epitaxy with atomically smooth sapphire surface. In Section 5.3, we show that the flake thickness can be tuned from 1.5 nm to 10 nm by different NaCl concentrations, resulting in a thickness-dependent phase tansition. The thickness-dependent phase transition was clearly observed from Raman and aberration-corrected scanning transmission electron microscopy (STEM) study (Section 5.3.1, which is further confirmed by transport measurements for different phases (Section 5.3.2). Furthermore, we demonstrate the observation of BKT-type superconductivity in layered 2H-NbS_2 below a transition temperature of 3 K in Section 5.4, where the conclusion of this chapter is made.

This article was the result of a close and extremely constructive collaboration between the author and Dr. Cheol-Yeon Cheon, who contributed equally to the results of the electrical measurements. Dr. Mukesh Tripathi also contributed to the project by performing STEM measurements and analaysis shown in Section 5.3.1.

The results in this chapter have been published in "*Superconducting 2D NbS_2 Grown Epitaxially by Chemical Vapor Deposition*", **ACS Nano** 2021 15 (11), 18403-18410. Thus, there is considerable overlap between this article [31] and this chapter.

5.2 2D NbS_2 single crystals grown by CVD

5.2.1 Growth process

2D NbS_2 was grown using a home-built CVD reactor schematically presented in Figure 5.2. C-plane sapphire was used as the growth substrate and was annealed in air for 6 h prior to growth, resulting in a clean surface with atomically smooth step terraces [155], which is crucial for achieving epitaxial growth [74]. A solution of niobium chloride ($NbCl_5$) in isopropanol (IPA) was used as the precursor, while 0.3 mol/L sodium chloride (NaCl) solution in deionized water was used to reduce nucleation density [109] and the reaction energy barrier [22]. Both solvents were spin-coated on top of sapphire substrate before loading into the chamber. Afterwards, a sapphire wafer was loaded into the quartz chamber and covered with another bare sapphire wafer, which promotes the growth of larger crystals by localizing the $NbCl_5$ vapor and reducing the flow rate of H_2S near the substrate. The reactor tube was purged with argon to remove residual oxygen and humidity before growth.

During the whole growth process, hydrogen disulfide (H_2S) with a flow rate of 35 sccm was

delivered to the chamber by using argon as a carrier gas. The growth procedure lasts for 30 min at a temperature of 950 °C and atmospheric pressure. As soon as the growth is finished, the chamber is allowed to cool down naturally. H_2S flow was kept with a flow rate of 5 sccm until the furnace reached a temperature of 150 °C to reduce sulfur vacancies. In later sections, to optimize the growth conditions, possible changes are made to the growth temperature and the flow rate of H_2S.

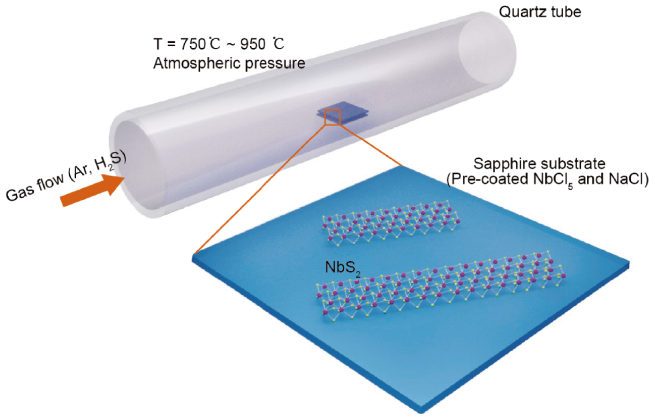

Figure 5.2: Schematic illustration of the hot-wall CVD system for NbS_2 growth. In the chamber, a bare wafer was placed on top of the sapphire wafer, which was spin-coated with NaCl and $NbCl_5$ solutions.

5.2.2 Growth morphologies under different conditions

Temperature induced morphology transition

Optical micrographs of CVD-grown NbS_2 crystals are shown in Figure 5.3. As can be seen from the figure, the shape and thickness of NbS_2 flakes show a clear trend, changing from thick triangles to thin rectangles with increasing temperature. In addition, all the rectangular NbS_2 flakes are perfectly aligned to the same direction at high temperature shown in Figure 5.3c.

The different crystal morphologies and the orientation of rectangular NbS_2 can be explained by the temperature-dependent strong interaction between NbS_2 and the sapphire substrate [156]. At the early stages of growth, nucleation takes place on the surface of sapphire with an initial random orientation of the crystallites [157]. For relatively low growth temperatures (e.g., 750 °C), the small crystallites do not have enough thermal energy to explore the energy landscape by rotation before they grow to big crystals. As a result, NbS_2 crystals with a small domain size and a random orientation are observed. We also observe a higher nucleation density under these conditions because of weak thermal etching. On the other hand, at higher growth temperatures (850 °C and 950 °C), the orientation of the grown NbS_2 is determined by the underlying sapphire. This could be related to the orientation of step edges on the atomically smooth sapphire surface. AFM images of rectangular NbS_2 crystals from the sample shown in Figure 5.3c are presented in Figure 5.4 which clearly show that the long edges of the NbS_2

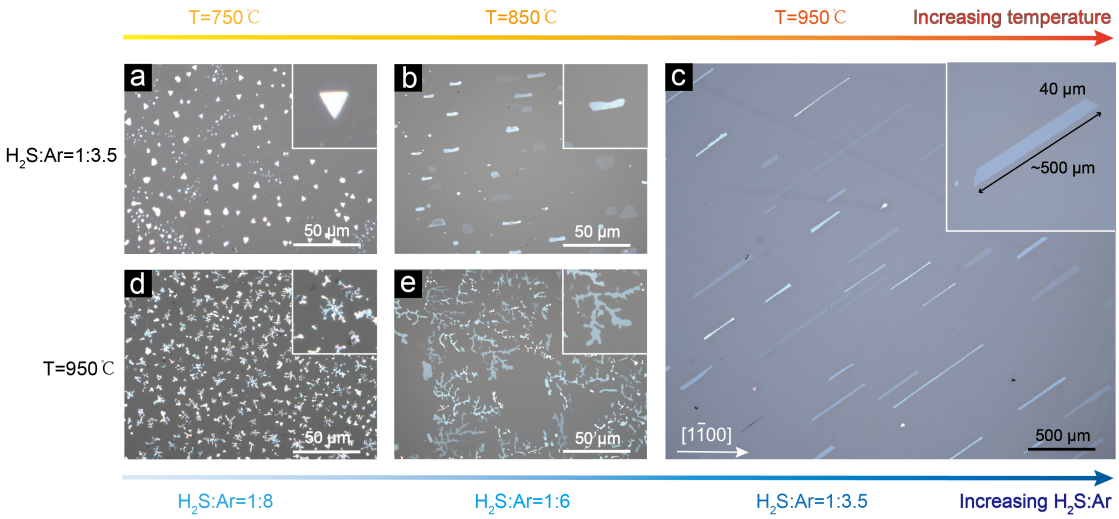

Figure 5.3: Optical micrographs of as-grown NbS_2 flakes under different growth conditions. A clear trend from thick triangular to thin rectangular, dendritic to regular shaped NbS_2 flakes was observed with increasing growth temperature and higher H_2S:Ar value, respectively.

crystal are oriented along the step edges on the surface of sapphire. In addition, we note that the smaller triangular NbS_2 crystals both on sapphire and on the NbS_2 thin film are epitaxially aligned along the [1-100] axis of the underlying c-plane sapphire, which can be explained by van der Waals interaction with the underlying substrate [158].

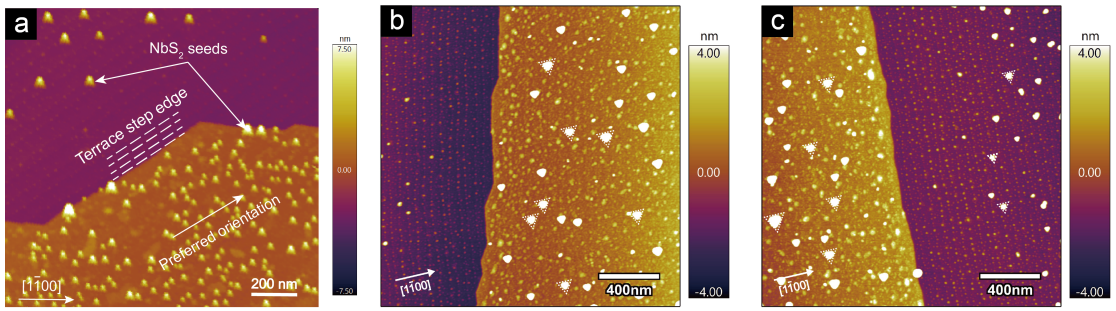

Figure 5.4: AFM images of as-grown NbS_2 on a sapphire substrate showing the growth direction NbS_2 seeds are epitaxially aligned along the [1-100] axis of c-plane sapphire, while the preferred growth orientation of rectangular NbS_2 flakes is determined by the terrace step edges.

Flow ratio of H_2S and Ar induced morphology transition

Growth morphologies can be also modulated by the gas flow ratio of H_2S and Ar. Dendritic NbS_2 crystals were observed in Figure 5.3d and e with a relatively lower value of H_2S:Ar compared to that in Figure 5.3c. The morphology transition induced by the gas flow ratio can be explained by the growth rates of different edge terminations [159]. In our case, the $NbCl_5$ precursor is reduced by H_2S and tiny NbS_2 seeds emerge at the early stage of growth. Along

the edges of these tiny seeds, Nb and S atoms are exposed to the reactor atmosphere on zigzag edges [159] with high chemical reactivity. They encounter atoms diffusing on the surface in random collisions and new chemical bonds are formed to achieve the most energetically stable structure [160]. Assuming that the spin-coated $NbCl_2$ provides the same amount of Nb precursor, the probability of meeting and bonding with free atoms depends on the partial pressure of H_2S. When the sulfur supply rate is at an insufficient level (e.g., H_2S : Ar = 1:8), S-terminated edges have much higher possibility to meet free Nb atoms, which leads to a higher growth rate of S-terminated edges than Nb-terminated edges. The difference in growth rates causes the dendritic shapes shown in Figure 5.3d and e. As H_2S increases to a saturated level (e.g., H_2S : Ar = 1:3), both S and Nb-terminated edges have enough opportunity to bond with free atoms, resulting in similar growth rates of these two type of edges. As a consequence, crystals grow with regular shapes and sharp edges as shown in Figure 5.3c.

It is notable that in our optimal growth condition, as shown in Figure 5.3c, rectangle-shaped NbS_2 flakes are grown with a large domain size having a typical length exceeding 500 μm and a width of around 40 μm, which is significantly larger than those in previous reports [150], [114], [148].

5.3 Thickness dependent phase transition of CVD-grown NbS_2

In this section, We demonstrate that our CVD-grown rectangular NbS_2 crystals can have both 3R and 2H-phase structures, depending on the thickness. Atomic force microscopy (AFM), Raman spectroscopy and aberration-corrected STEM are further conducted to investigate the correlation between the phase transition and thickness. Furthermore, to compare their electrical performance, electrical transport measurements are carried out in 2D NbS_2 with different phase structures.

5.3.1 Correlation between phase transition and flake thickness

Changing the $NbCl_2$ concentration allows us to control the thickness of rectangular NbS_2 crystals in the 1.5 nm to 10 nm range, corresponding to 2-16 layers. A histogram of the thickness distribution of as-grown NbS_2 crystals for different pre-coated $NbCl_5$ concentrations is shown in Figure 5.5a, indicating that a higher $NbCl_5$ concentration leads to a higher dominant thickness. In Figure 5.5b, we show an AFM image of a rectangular NbS_2 single crystal with a thickness of 10 nm. A smooth surface and sharp edge can be clearly seen, indicating that our NbS_2 samples have a high crystallinity and good quality.

Figure 5.5c shows the room-temperature Raman spectra acquired from as-grown rectangular NbS_2 crystals with various thicknesses on sapphire substrate. The blue curve presents the Raman spectrum from 3 nm-thick NbS_2 showing two characteristic peaks at 348 cm^{-1} (E_2) and 389 cm^{-1} (A_1), which corresponds with the 3R-phase NbS_2 [161]. The orange curve on the other hand, collected from 10 nm-thick NbS_2 is characterized by peaks located at 340

cm^{-1} (E^1_{2g}) and 379 cm^{-1} (A_{1g}), in agreement with the spectral signature of the 2H-phase NbS_2 [161]. Data from the 4 nm-thick NbS_2 (purple curve) shows a mixture of Raman spectra for both 3R-phase and 2H-phase, indicating the transition between 2H and 3R occurs around this thickness.

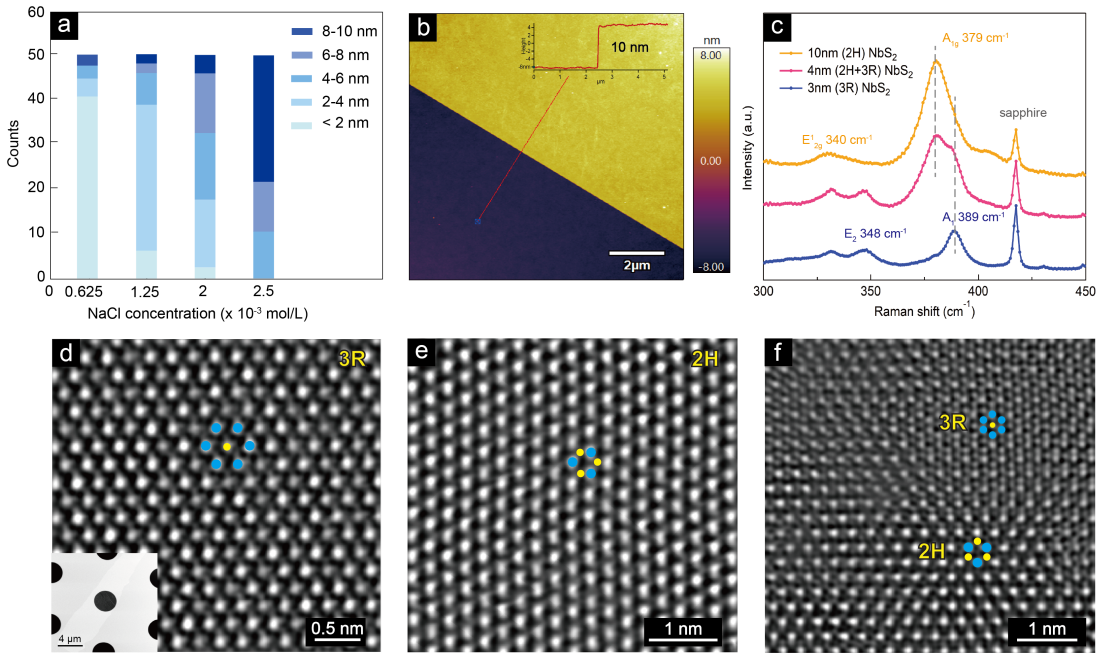

Figure 5.5: Thickness dependent phase transition of NbS_2. (a) Histogram for the thickness distribution of as-grown NbS_2 grains for different precoated $NbCl_5$ concentrations. (b) AFM image of an NbS_2 flake transferred onto a Si/SiO_2 substrate showing a thickness of 10 nm. (c) Raman spectra at room temperature for as-grown NbS_2 flakes on sapphire substrate. (d-f) STEM images of NbS_2 flakes with (d) 3R-polytype stacking, (e) 2H-polytype stacking and (f) a mixture of 3R-polytype stacking and 2H-polytype stacking. Inset of (d): A low magnification ADF-STEM image of a NbS_2 flake transferred onto a TEM grid.

The atomic structures of different phases and stackings can be directly visualized by employing aberration-corrected STEM. We show in Figure 5.5d-f high-resolution high annular angular dark field (HAADF)-STEM images obtained from transferred NbS_2 samples to distinguish different atomic structures and stacking arrangements with various thicknesses. The inset of Figure 5.5d shows a low-magnification HAADF image of a rectangular NbS_2 crystal transferred onto a TEM grid. The HAADF intensity is proportional to the square of the atomic number (Z^2), allowing Nb and S atoms to be directly distinguished based on the contrast of individual atomic columns. In Figure 5.5d, bright hexagonal rings (Nb atoms) with darker spots (S atoms) in the center are displayed, indicating that the Nb atoms mismatch slightly without any rotation between adjacent layers (illustrated in the left channel of Figure 5.1), corresponding to a 3R-polytype stacking. On the other hand, equal intensity of each Nb atom in Figure 5.5e reveals that they are aligned to each other with opposite direction between adjacent layers (illustrated in the right channel of Figure 5.1), and that 3 Nb atoms can be found around

a single S atom, suggesting a 2H-polytype stacking. Additionally, a mixture of 3R and 2H polytype stacking is observed in Figure 5.5f. S line defects are visible close to the interfaces of different stackings, whereas S vacancies are present everywhere in the image.

5.3.2 Electrical transport in 2D NbS_2 with different phase structures

In order to characterize the electrical transport properties of CVD-grown NbS_2 crystals with different phases, multiterminal devices were fabricated after the crystals have been transferred onto a Si/SiO_2 substrate. Afterwards, the samples were spin-coated with PMMA polymer and put on a hot plate at 180 °C for 5 min. Electro-beam lithography was used to pattern the electrodes. Finally, a stack of 2nm/80nm thick Ti/Au was deposited by e-beam evaporation for the electrodes, followed with a lift-off process with acetone to remove the PMMA layer. Between the fabrication steps, samples were kept in the inert Ar environment inside a glovebox to prevent sample degradation in air. Figure 5.6a displays an optical micrograph of a Hall bar device based on a 10 nm-thick NbS_2 crystal.

To examine the relationship between the thickness-dependent structural phase and its transport properties, temperature dependence of four-probe longitudinal resistance (R_{xx}) was measured at zero magnetic field, with results for three representative thicknesses (3 nm, 4 nm, and 10 nm) shown in Figure 5.6b. Inset shows the magnified view in the 1.5 K - 10 K temperature range. For the sample with a thickness of 3 nm (blue curve), the resistance linearly decreases as the temperature is lowered, indicating its metallic property ($dR/dT>0$), consistent with previous predictions [162]. However, its resistance starts to slightly increase below 20 K where the resistance minimum is observed. Similar observations of this low-temperature resistance minimum were reported in CVD grown 3R-phase NbS_2 [150], [148], which is attributed to electron scattering at defect or excess Nb sites. From the device, we do not observe the superconducting transition above our experimental base temperature (1.4 K). These electrical properties agree well with the metallic nature of the 3R-phase NbS_2. On the other hand, for the 2H-phase sample with a thickness of 10 nm (shown as orange curve), the resistance drops sharply to zero at around 3 K, indicating the superconducting transition. The superconducting transition critical temperature (T_c) is 2.6 K, which corresponds to the temperature at which the resistance becomes half of the normal-state resistance R_N, $R(T_c) = 0.5\ R_N$.

At the intermediate thickness (4 nm) between the 2H and 3R phase of NbS_2 (shown as the purple curve), interestingly, the resistance drops sharply at around 3 K but remains at a relatively high value (around 150 Ω) down to the base temperature of 1.4 K. This feature could be explained by the presence of mixed 2H and 3R phases where metallic 3R-phase and superconducting 2H-phase domains coexist. Notably, this 4 nm-thick device shows metallic behavior at high temperatures but with a slower resistance change (dR/dT) than that of the other 2H and 3R devices. This leads to a lower residual resistance ratio (*RRR*) of around 1.5, defined as the ratio between the resistance at T = 300 K and the normal-state resistance above the superconducting transition temperature of the 2H phase, at T = 10 K, which is lower than

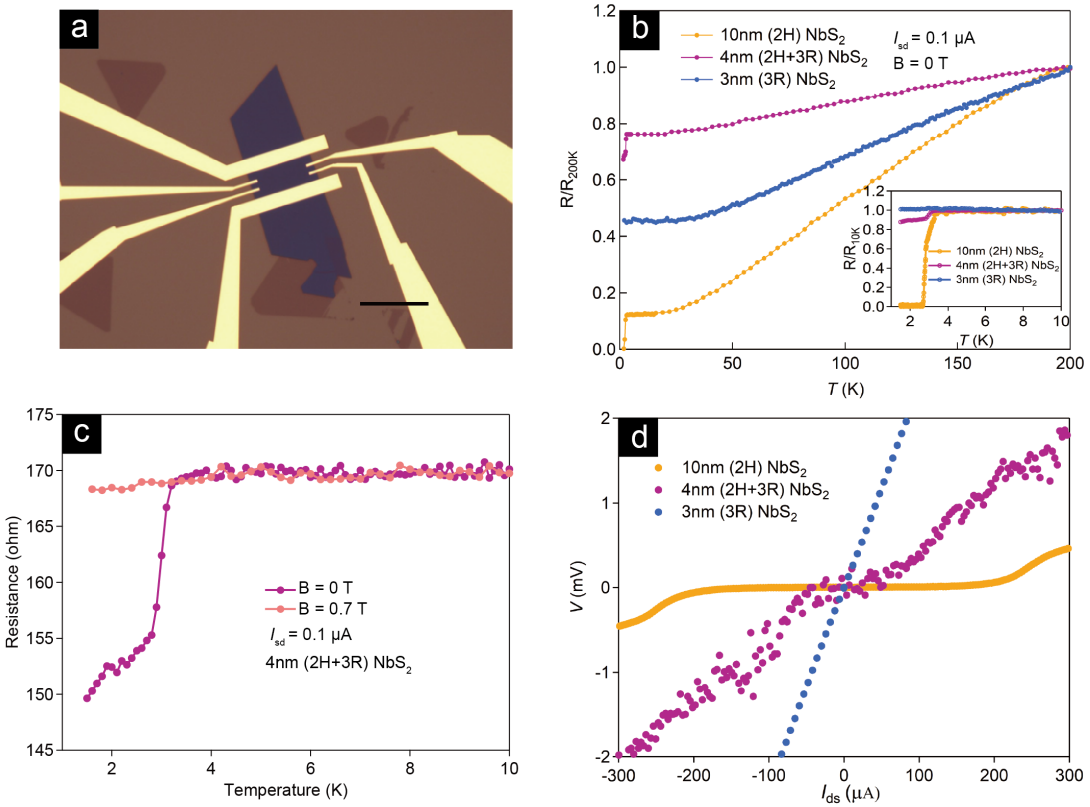

Figure 5.6: Transport properties of NbS_2 with different phases. (a) Optical micrograph of a NbS_2 device fabricated on Si/SiO_2 substrate with a flake thickness of 10 nm. Scale bar length: 25 μm. (b) Zero-field cooled resistance as a function of temperature for NbS_2 devices with different thicknesses. An AC current of 0.1 μA is used to probe the resistance. Inset: a zoomed-in temperature dependence of resistance from 1.4 K to 10 K. (c) Resistance as a function of temperature for 4nm-thick NbS_2 with and without out-of plane magnetic field (0.7 T). Drain-source AC current (I_{sd}) was kept at 0.1 μA during the measurement. (d) *V*-*I* characterization of NbS_2 devices with different thicknesses at the base temperature of 1.4 K.

that of the 3 nm-thick 3R-phase (around 3.3) and 10 nm-thick 2H phase (around 11). Since *RRR* is commonly used as an indicator of the crystalline quality of a superconductor [163], [164], a smaller *RRR* in 4 nm-thick NbS_2 indicates the existence of additional structural disorder, which we attribute to sulfur point and line defects between 2H and 3R phases, as confirmed by the STEM results in Figure 5.5f. Magnetic field cooling suppresses this sharp resistance drop (shown in Figure 5.6c), which further supports the hypothesis that the resistance drop is related to the superconducting transition of the 2H domains.

Figure 5.6d displays four-probe DC *V*-*I* characteristics for NbS_2 with different structural phase at the base temperature (1.4 K). A linear curve was obtained for the 3 nm-thick 3R-phase NbS_2 sample, whereas a strong non-linear curve was obtained for the 10 nm-thick 2H-phase NbS_2, consistent with a Berezinskii-Kosterlitz-Thouless (BKT) type superconducting phase transition. Compared to single-phase samples, the *V*-*I* curve of the 4nm-thick sample shows

a weak non-linear curve (a possible combination of 2H and 3R-phase signal) but with a larger noise, which could be related to contributions from line defects separating the two phases. These results, consistent with Raman and STEM results, provide additional evidence that transition from the metallic 3R-polytype to the superconducting 2H-polytype takes place in our thickness-controlled CVD-grown NbS_2 crystals.

5.4 Further studies and conclusion

5.4.1 Superconductivity of 2H-phase NbS_2

To further study the superconductivity of CVD-grown 2H NbS_2 crystals, both four-probe DC and AC transport measurements were performed in this section. Figure 5.7a shows the temperature dependence of resistance (R_{xx}) of the device shown in Figure 5.6a at various out-of-plane magnetic fields B, applied perpendicularly to the 2D crystal plane. In the presence of the magnetic field, we define the critical temperature T_c as the temperature at which the resistance decreases to 80% of the normal resistance value. As the amplitude of the magnetic field increases, the critical transition temperature decreases and the resistance change becomes more gradual. A metallic behavior without resistance drop was obtained above the magnetic field of 0.6 T, indicating that superconductivity is completely suppressed by the magnetic field. Figure 5.7b shows the magnetic field-dependent transition, B_{c2} vs T_c/T_{c0} phase diagram where B_{c2} is the upper critical field and T_{c0} the critical temperature at zero magnetic field. We find a linear relation between B_{c2} and T_c, which is a typical feature of 2D superconductors [75], [165]. It can be fitted with a model from the linearized Ginzburg-Landau(GL) theory [166],

$$B_{c0}(T) = \frac{\phi_0}{2\pi\xi_{GL}(0)^2}\left(1 - \frac{T}{T_c}\right) \tag{5.1}$$

where $\xi_{\mathrm{GL}}(0)$ is zero-temperature coherence length, and ϕ_0 is magnetic flux quantum. From the fitted result, we get $\xi_{\mathrm{GL}}(0)$ = 25 nm, which is larger than the probed sample thickness (10 nm). This indicates that the 2D superconducting transition should follow the BKT type transition.

Figure 5.7c shows the four-probe DC I-V characteristics as a function of temperature for the 6 nm-thick 2H-phase NbS_2 device. At 3.5 K, linear Ohmic behavior was obtained with the constant slope of resistance around 3 Ω, which is equal to the metallic normal-state resistance. As the temperature decreases, the curve becomes non-linear and a critical current gap is observed at which the probe voltage is close to zero. The V-I curves plotted on a logarithmic scale (shown in the Figure 5.7d) display a clear transition from a V-I linear dependence to a power-law dependence ($V \propto I_\alpha$) indicating the BKT transition. We estimate the BKT transition temperature (T_{BKT}) to be 3 K at the value of α = 3 for our 6 nm-thick NbS_2 crystal. Fitted α

values as a function of temperature can be found in the Figure 5.7e. The data presented above provides further evidence that our CVD-grown 2H NbS_2 exhibit the features expected from a 2D superconductor.

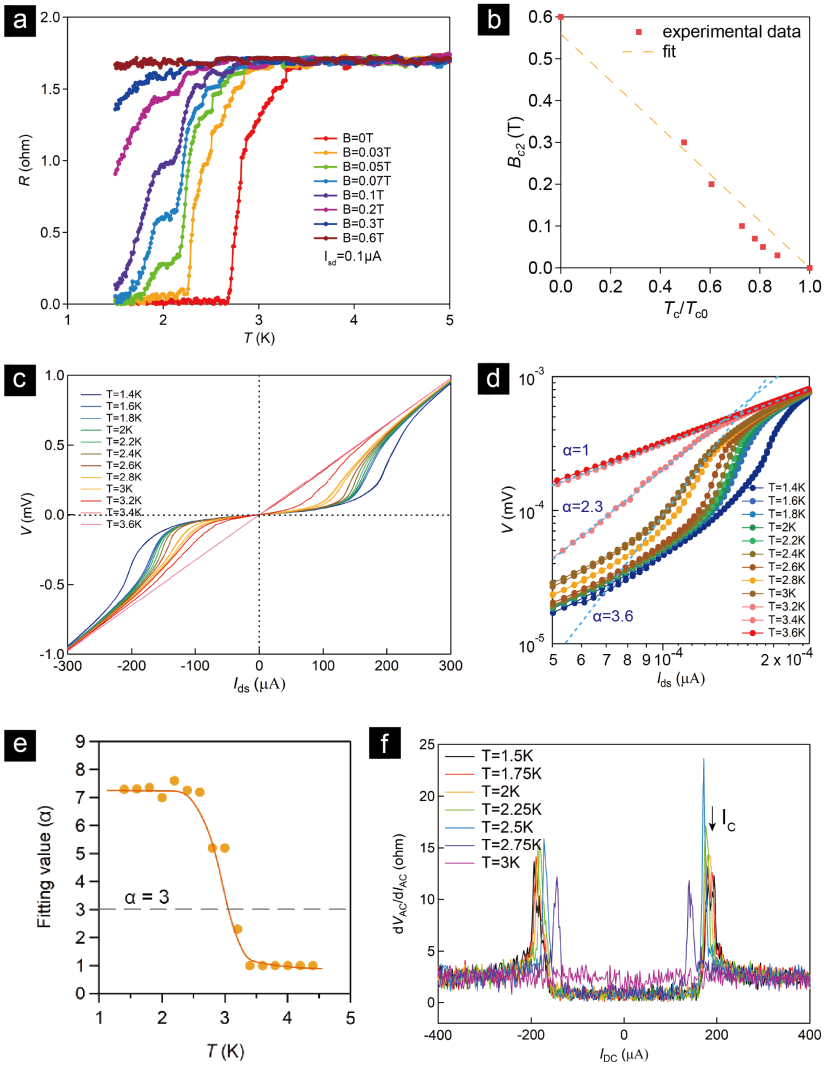

Figure 5.7: Superconductivity in 2H-phase NbS_2. (a) Electrical resistance of the device shown in Figure 5.6a at various out-of-plane magnetic fields B. (b) Corresponding B vs T_c/T_{c0} diagram from the data shown in (a) with its fitting result. (c) V-I characterization for 6 nm-thick NbS_2 device from the base temperature to 3.6 K. (d) V-I curve in (c) replotted on a logarithmic scale showing $V \propto I_\alpha$ behavior, consistent with an expected BKT model. (e) Power-law dependence ($V \propto I_\alpha$) of the fitting parameter α as a function of temperature from the data shown in (d). Gray dashed line corresponds to α =3, where the BKT transition temperature (T_{BKT}) is estimated to be 3 K for our 6 nm-thick grown NbS_2 flake. (f) Differential resistance at zero magnetic field as a function of source-drain bias current at different temperatures for the 6 nm-thick NbS_2 device.

To further investigate the superconducting critical current, AC differential resistance as a

function of DC drain-source current was measured at fixed temperatures ranging from 1.5 K to 3 K as shown in Figure 5.7f. Resistance peaks sharply at the critical current (190 μA at 1.5 K) which indicates the transition from the normal resistive state to the superconducting zero-resistance state. The critical current gradually decreases with an increasing temperature and disappears above 3K as the sample becomes metallic.

5.4.2 Conclusion

In this chapter, we demonstrate a CVD method to synthesize 2D NbS_2 single crystals with a large size, controllable thickness and epitaxial orientation. The thickness-dependent structural transition from metallic 3R-phase to superconducting 2H-phase was first observed in CVD-grown NbS_2 and was confirmed by Raman spectroscopy, aberration-corrected STEM as well as transport measurements. The CVD-grown 2H-phase NbS_2 behaves as a 2D superconductor, with BKT-type superconducting transition occurring below 3 K. Our work demonstrates a practical approach to phase-controllable growth of 2D TMDC superconductors and provides the platform for their widespread use in mesoscopic devices.

6 P-type doping in NbS_2-MoS_2 lateral heterostructures grown by MOCVD

6.1 Introduction

6.1.1 State of art: electrical properties and synthesis of p-type MoS_2

Semiconducting two-dimensional (2D) transition metal dichalcogenides (TMDCs) have been extensively investigated for next-generation nanoelectronics and optoelectronics because of their atomic scale thickness [23], layer-dependent band structure [167] and favorable electrical properties [43]. Among them, monolayer molybdenum disulfide (MoS_2) is most widely studied due to its strong photoluminescence [45] (PL) and high stability [43]. Monolayer MoS_2 with a large intrinsic bandgap of 1.8 eV [21] and a high on/off current ratio of 10^8 in n-type FET devices [23] behaves as an n-type semiconductor which is attributed to the electron doping by sulfur vacancies [168], [169]. Moreover, MoS_2-based integrated nanoelectronics are emerging rapidly in recent years, such as in-memory devices [117] and artificial neural networks (ANN) [170], which highlights their potential to extend Moore's law in advanced technologies [122], [123]. Complementary logic applications based on MoS_2 are desirable for the realization of a platform for low energy-consuming and high effective computing, which requires the reliable synthesis of p-type MoS_2 [171].

Unlike the conventional n-type MoS_2, which is predominantly studied for its semiconducting properties, p-type MoS_2 exhibits a positive charge carrier concentration attributed to the incorporation of p-type dopants, making it an attractive candidate for complementary metal-oxide-semiconductor (CMOS) technology. The electrical performance of p-type MoS_2 is a crucial factor in determining its potential applications in electronic devices. On one hand, p-type MoS_2 shows high hole mobility, which has been reported to be in the range of 20-200 $cm^2V^{-1}s^{-1}$. This high mobility is attributed to the reduced scattering of holes due to the absence of midgap states in p-type MoS_2, differing from n-type MoS_2, which has midgap states resulting from the presence of sulfur vacancies. On the other hand, p-type MoS_2 exhibits a higher carrier concentration compared to n-type MoS_2, with reported values of up to 1×10^{18} cm^{-3}. The high carrier concentration of p-type MoS_2 is a consequence of the efficient doping of p-type impurities during the synthesis process, which leads to a higher density of holes in

the valence band.

Several methods have been reported to achieve p-type doped MoS_2, such as plasma treatment [172], [173], [174], charge transfer [175], [176] and contact engineering [171], [176]. However, these non-intrinsic p-type doped MoS_2 were limited to monolayer thicknesses and their further applications are hindered by the complicated process and low controllability [177], showing that the synthesis of high-quality and controllable p-type doped monolayer MoS_2 remains a challenge. Recently, some attempts have been reported to introduce substitutional metal doping with Nb atoms inside MoS_2 lattice structure by chemical vapor deposition (CVD) [177], [178], [179], realizing charge transfer by electron occupation of metal d-orbitals [180], [181]. Nevertheless, these p-type MoS_2 FET devices shows a low on/off ratio and carrier mobility because of their large contact resistance related to strong Fermi level pinning on metal contacts.

6.1.2 2D metal-semiconductor TMDC heterostructures

As mentioned in Chapter 2, 2D metal-semiconductor (M-S) junctions based on TMDC heterostructures are expected to result in a reduced contact resistance due to weakened Fermi level pinning and modulation of the Schottky barrier [6]. Furthermore, the interface of these 2D M-S heterostructures is one of the crucial factors determining their performance, requiring comprehensive characterization, such as identifying geometrical distortions, interfacial coupling and electronic states [182]. Although TMDC heterostructures can be obtained using the transfer technique thanks to van der Waals interactions [12], CVD growth is scalable towards large area growth, layer number control, high reproducibility as well as low residue concentration [183]. Several examples of lateral and vertical TMDC heterostructures grown by CVD have been reported, including semiconductor-semiconductor heterostructures (e.g. MoS_2/WS_2 [113], $MoS_2/MoSe_2$ [184]) and metal-semiconductor heterostructures (e.g. NbS_2/WS_2 [114]).

6.1.3 Outline of this chapter

Here in this chapter, we demonstrate the one-step simultaneous MOCVD synthesis of NbS_2-MoS_2 lateral heterostructures with p-type Nb substitutional doping of monolayer MoS_2. In Section 6.2, a "one-step" MOCVD method to synthesize NbS_2-MoS_2 lateral heterostructure is demonstrated (Section 6.2.1), with a comprehensive characterization of the lateral heterostructures by Atomic force microscopy (AFM), Raman spectroscopy, Photoluminescence (PL), aberration-corrected scanning transmission electron microscopy (STEM) (Section 6.2.2).

In Section 6.3, we demonstrate that our MOCVD-grown monolayer MoS_2 is substitutionally doped with Nb dopants resulting a p-type behaviour. Raman spectroscopy, PL, STEM combining with energy-dispersive X-ray spectroscopy (EDX) are used to confirm the substitutional Nb doping (Section 6.3.1). Field-effect transistors (FETs) are fabricated to study the electrical transport performance of the p-type MoS_2 (Section 6.3.2).

In Section 6.4, density-functional theory (DFT) simulations are performed (Section 6.4.1) to calculate the band structures of Nb-doped MoS_2 and reveal the Fermi level alignment at the interface with the critical role of doping. And FET device based on our heterojunction is fabricated and exhibits a p-type transfer characteristic with an current on/off ratio of 10^4 (Section 6.4.2). In Section 6.5, we further carry out temperature-dependent I-V characterization and self-consistent quantum transport simulations to extract the Schottky barrier height (SBH) at the interface of the p-type heterojunction, where the conclusion of this chapter is made.

The main ideas and methods in this chapter are developed by Zhenyu Wang and Prof. Andras Kis, with most experiments and analysis performed by Zhenyu Wang, while the work in some subsections is performed in close collaboration with my colleagues in LANES laboratory as well as Prof. Alessandro Fortunelli's group from CNR-ICCOM and Prof. Giuseppe Iannaccone's group from University of Pisa for simulation results, as listed below. STEM measurements and EDX spectroscopy shown in Section 6.2.2 and Section 6.3.1 are performed by my colleague Dr. Mukesh Tripathi. The QM simulations and modelling shown in Section 6.4.1 are performed by Prof. Alessandro Fortunelli's group from CNR-ICCOM. The numerical simulations of transport shown in Section 6.5.1 are performed by Prof. Giuseppe Iannaccone's group from University of Pisa.

The research findings presented in this chapter have been published in the paper: "*Substitutional P-type Doping in NbS_2-MoS_2 Lateral Heterostructures Grown by MOCVD*", **Advanced Materials**, 2023, 35 (14), 2209371. Thus, there is considerable overlap between the paper [185] and this chapter.

6.2 2D NbS_2-MoS_2 lateral heterostructures grown by MOCVD

6.2.1 Growth process

Our NbS_2-MoS_2 lateral heterostructures were synthesized by sequentially growing each component on a c-plane sapphire wafer in a home-build MOCVD system, as schematically shown on Figure 6.1a. Since NbS_2 requires a higher growth temperature than MoS_2 according to our previous results [109], [31], the quartz tube was first heated to 850 °C with temperature maintained for 10 min for monolayer MoS_2 growth. During this time, molybdenum hexacarbonyl ($Mo(CO)_6$) and hydrogen sulfide (H_2S) precursors were simultaneously introduced into the growth tube. Subsequently, the precursor supply was turned off and the tube was continuously heated until 950 °C. Monolayer MoS_2 on sapphire substrate was in turn employed for the preparation of heterostructures. H_2S flow was resumed, reacting with the pre-coated $NbCl_5$ and resulting in NbS_2 growth. Initial nucleation of NbS_2 preferably takes place at the edges of as-grown MoS_2 due to its high chemical reactivity. NbS_2 growth continues outward onto the surface of sapphire owing to its lower Gibbs free energy comparing to the surface of MoS_2 [112], resulting in lateral NbS_2-MoS_2 heterostructures. Typical as-grown NbS_2-MoS_2 lateral heterostructures are shown in Figure 6.1b, characterized by MoS_2 triangles with a lateral size of

around 30 µm and surrounded by NbS_2 with a width of around 5 µm. Notably, the successive growth of both components without air exposure prevents the oxidation of as-grown MoS_2 edges, which is essential for the formation of high-quality lateral heterostructures.

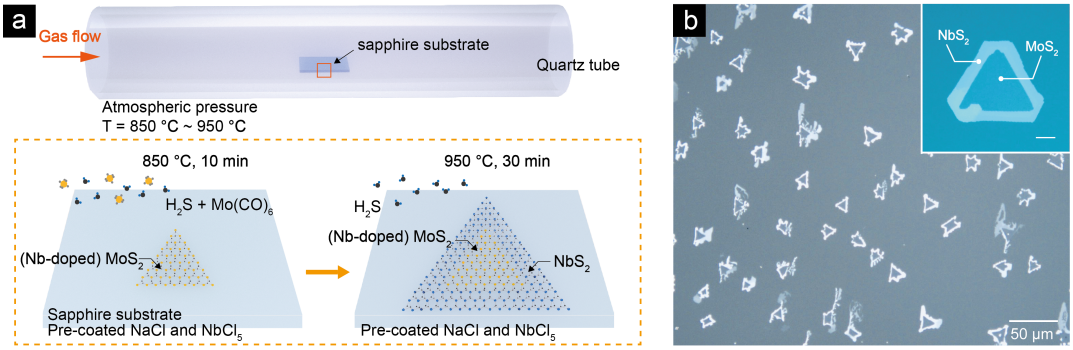

Figure 6.1: MOCVD growth process of NbS_2-MoS_2 lateral heterostructures. (a) Schematic illustration of the MOCVD process for NbS_2-MoS_2 lateral heterostructure growth. (b) Optical micrograph of as-grown NbS_2-MoS_2 lateral heterostructures grown on sapphire. Inset: Zoomed-in image presenting a MoS_2 triangle surrounded by NbS_2. Scale bar: 10 μm.

6.2.2 Characterization of lateral heterostructures

Figure 6.2a shows the AFM image of an as-grown NbS_2-MoS_2 lateral heterostructure on the sapphire substrate, indicating a smooth surface with a thickness of 3 nm for NbS_2 and a height of 0.7 nm for monolayer MoS_2. By controlling the different growth parameters, we were able to tune the thickness of NbS_2 within the heterostructures between 3 nm and 10 nm. Figure 6.2b presents the Raman spectra obtained from different regions of the heterostructure acquired at room temperature. The Raman spectrum from the central region (orange curve) contains two typical peaks at 383 cm^{-1} (E^1_{2g}) and 402 cm^{-1} (A_{1g}), confirming the monolayer nature of MoS_2. The peripheral region shows peaks in the Raman spectrum (red curve) located at 340 cm^{-1} (E^1_{2g}) and 379 cm^{-1} (A_{1g}), in agreement with the vibration modes of NbS_2. Raman intensity maps corresponding to the characteristic modes of NbS_2 and MoS_2 are shown in Figure 6.2c. Uniform signals indicate uniform chemical distribution and the clear boundaries can be seen between the NbS_2 and MoS_2 regions, confirming the formation of in-plane heterostructures without alloying.

To investigate the atomic structure and interface of the heterostructure, aberration-corrected annular dark field (ADF)-STEM imaging was performed with images shown in Figure 6.2d-e. Due to varying thickness, few-layer NbS_2 shows stronger contrast in comparison to monolayer MoS_2. Magnified and filtered image shows a clear and sharp interface between the two materials. Moreover, the fact that NbS_2 is vertically stacked in a hexagonal lattice arrangement (2H-phase) with no visible defects in the individual regions suggests a high crystalline quality

of our heterostructure samples. A relative orientation angle of around 30° is estimated from their atomic lattice structure of the heterostructure, which can be further confirmed from the corresponding fast Fourier transformation (FFT) image shown in the inset. Geometric phase analysis (GPA) of the corresponding ADF-STEM image shows compressive in-plane strain along the interface with MoS_2 (see Figure 6.2f). Distribution of strain is observed clearly along the interface, which is attributed to the lattice mismatch and layer variations of the two compounds.

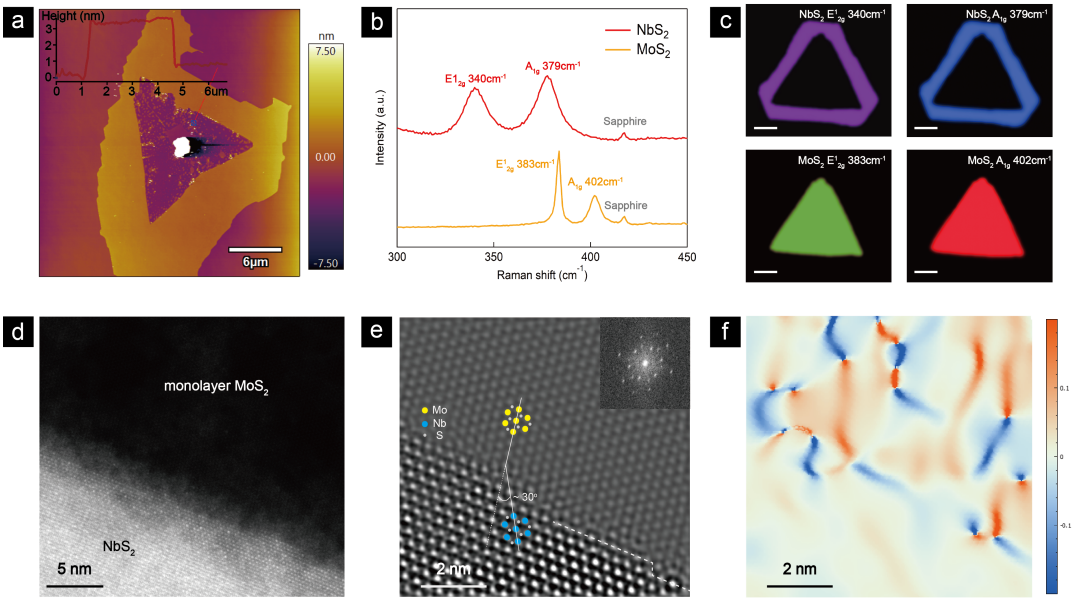

Figure 6.2: Characterizations of NbS_2-MoS_2 lateral heterostructures. (a) AFM image and its corresponding height profile of as-grown NbS_2–MoS_2 lateral heterostructure. The thicknesses of NbS_2 and MoS_2 are around 3 nm and 0.7 nm, respectively. (b) Raman spectra at room temperature for NbS_2-MoS_2 lateral heterostructures on sapphire. The red curve was measured on peripheral NbS_2, while the orange curve was taken on central MoS_2. (c) Raman mapping images based on the intensity of the typical modes on NbS_2 region and MoS_2 region from the heterostructure sample. Scale bar: 10 μm. (d-e) STEM images taken on the interface of NbS_2-MoS_2 lateral heterostructure. The darker side shows monolayer MoS_2, while the brighter sides correspond to few-layer NbS_2. Inset of (e): Corresponding FFT of the ADF-STEM image. The separated diffraction spots indicate the in-plane growth of the heterostructure. (f) 2D strain mapping of NbS_2-MoS_2 heterostructure for in-plane (ϵ_{xx}) direction, which is analysed from the corresponding image shown in (e).

6.3 P-type Nb-doped monolayer MoS_2

Our monolayer MoS_2 in the heterostructures was substitutionally doped with Nb atoms during the MOCVD process. Nb dopants were introduced from pre-coated $NbCl_5$ into MoS_2 lattice

in the period when the MoS_2 nuclei grow larger to crystals, which corresponds to the 850 °C/10 min stage shown in Figure 6.1a. Notably, the substitutional doping (together with MoS_2 growth) and heterostructure interface formation (together with NbS_2) take place at different stages and temperatures of the growth process, independently of each other.

6.3.1 Characterizations of Nb doping in MoS_2

STEM and EDX analysis

A typical ADF-STEM image in Figure 6.3a shows the perfect atomic lattice structure of monolayer MoS_2. Several sulfur vacancies, a common defect in TMDCs, can be observed. The fast Fourier transform (inset) pattern from the corresponding image further confirms the high-quality growth. In principle, different atoms can be identified directly from their atomic contrast because of the relation between ADF intensity and the Z number (Z^2). However, since Nb and Mo differ from each other with only one Z number in the periodic table, it is not straightforward to distinguish them in ADF-STEM images. Therefore, inverse fast Fourier transition (IFFT) method was used to identify Nb dopants in MoS_2 [186], as shown in Figure 6.3b. Nb atoms are highlighted with yellow circles in Figure 6.3a and can be seen as bright dots at the corresponding location in Figure 6.3b. Sulfur vacancies (V_s) are also visible as black dots in Figure 6.3b.

In addition, to extract the doping concentration precisely, EDX spectroscopy was further employed in the MoS_2 region as shown in Figure 6.3c-d. Elemental mapping and spectrum from the corresponding region show the spatial distribution of S, Mo and Nb atoms. Although the K and L edge energies for Nb and Mo are very close, peak deconvolution can be used to separate them, highlighting the uniform distribution of the three elements within the measured region showing an atomic concentration of S > Mo > Nb. Average Nb dopant concentration extracted from the EDX is 1.5%.

Raman and Photoluminescence spectrum

Figure 6.4a compares Raman spectra acquired from the Nb-doped MoS_2 and pristine MoS_2 on sapphire substrate. Both of the characteristic peaks ($E^1{}_{2g}$ and A_{1g}) show a separation of around 20 cm^{-1}, indicating the monolayer nature of the pristine MoS_2 and Nb-doped MoS_2. The Raman signals of Nb-doped MoS_2 show a blue-shift compared with the pristine MoS_2, consistent with previous literature [177]. The same location of sapphire signals confirms that the shift is not due to noise. The shift of Raman spectra depends on the coexistence of strain and charge doping [187], [188]. In our case, the blue shift of Raman signals can be explained by growth-induced tensile strain and reduced electron-phonon scattering, which results from the distorted lattice and hole injection due to the substitutional Nb-doping [177], respectively.

Figure 6.4b presents PL spectra of Nb-doped monolayer MoS_2 and pristine monolayer MoS_2, as well as their corresponding fitting curves. A strong PL peak located at around 1.80 eV was observed in pristine monolayer MoS_2, in-line with its direct band gap nature [45]. Compared

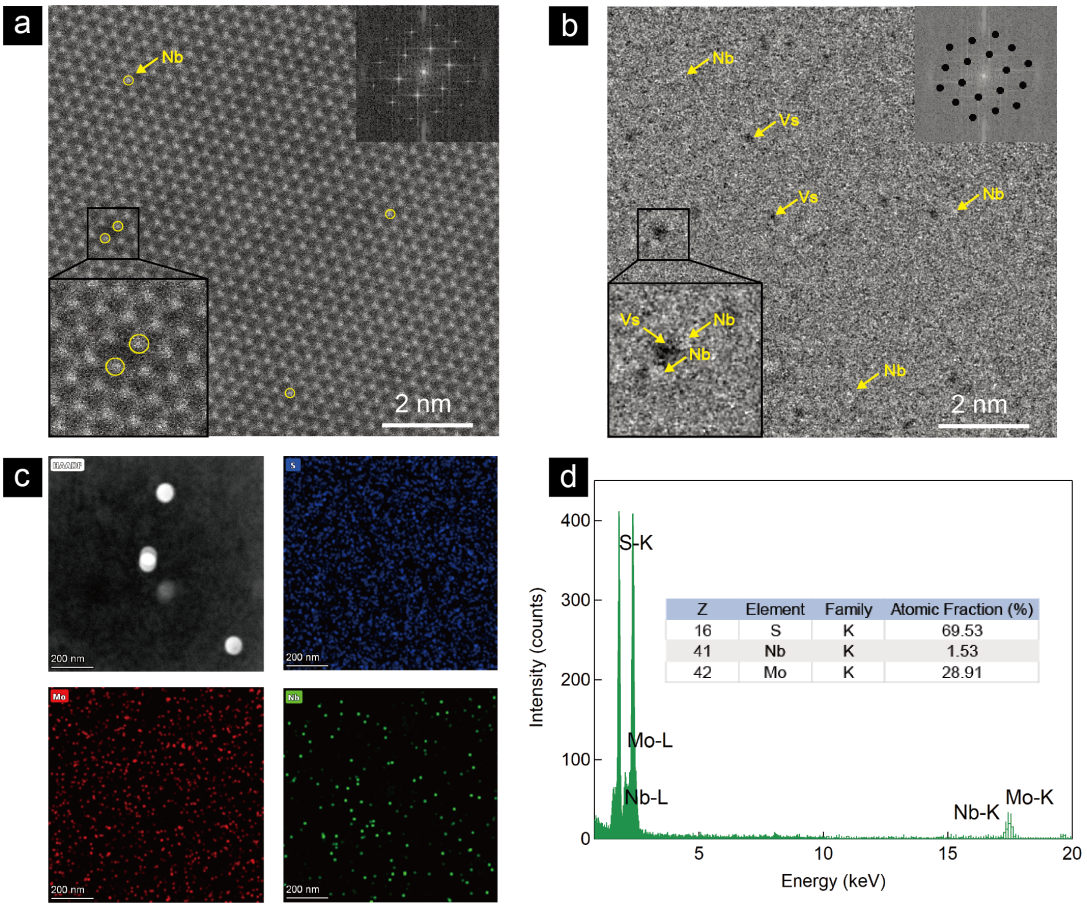

Figure 6.3: STEM and EDX analysis of Nb doped-MoS_2. (a-b) ADF-STEM image of the Nb-doped MoS_2 film and inverse fast Fourier transform (IFFT) filtered image, respectively. Top-right insets show the corresponding FFT images.

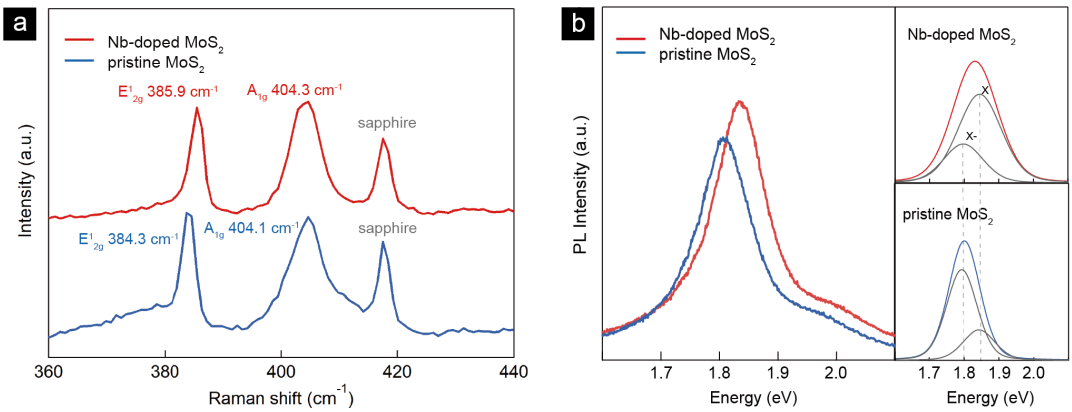

Figure 6.4: Raman and PL spectrum of Nb doped-MoS_2. (a-b) Raman and PL spectrum of Nb-doped MoS_2 comparing with pristine MoS_2 on sapphire substrates measured at room temperature.

with pristine MoS_2, the Nb-doped monolayer MoS_2 shows a blue-shifted PL peak with enhanced intensity, which is consistent with previous results on p-type doping MoS_2 [177], [189]. To explain the spectral changes, the PL peaks can be considered as a combination of the trion (X^-) peak at around 1.79 eV and the exciton (X) peak at around 1.85 eV, as shown by the gray curves. In pristine MoS_2, the PL spectra are dominated by the trion (X^-) peak because of the strong electron doping [190]. With Nb doping, the exciton (X) peak becomes dominant due to the reduced electron density and a suppressed electron concentration.

6.3.2 Electrical transport of monolayer MoS_2 doped with Nb

To examine electrical transport properties of our Nb-doped MoS_2, transfer characteristics were studied on multiple samples with different doping concentrations with results shown in Figure 6.5a. Notably, a stack of Ti/Au was utilized as conventional 3D contact on a channel of our MoS_2. The variation of Nb dopant concentration is due to different amounts of spin-coated $NbCl_2$ precursor during growth, which shows a range of 0.9% to 4.6% according to our EDX analysis. A clear transition from n-type to p-type is visible from the transfer curves, as the Nb dopant concentration increases. Pristine MoS_2 shows a n-type behavior, while 0.9% Nb-doped MoS_2 shows both p-type and n-type behavior, and 1.5% Nb-doped MoS_2 shows a p-type behavior. In particular, in 1.5%Nb-doped MoS_2 sample, a typical p-type behavior with an on/off ratio of 1×10^3 and field-effect mobility of around 1.43 $cm^2V^{-1}s^{-1}$ was observed. The mobility is lower than that of pristine MoS_2, which can be attributed to the increased structure distortion because of substitutional Nb doping in MoS_2. Nevertheless, in a sense of material discovery, p-type MoS_2 achieved by substitutional doping is already an advancement comparing to pristine MoS_2. The I-V characteristic exhibits linear behavior within the measured range, as depicted in Figure 6.5b.

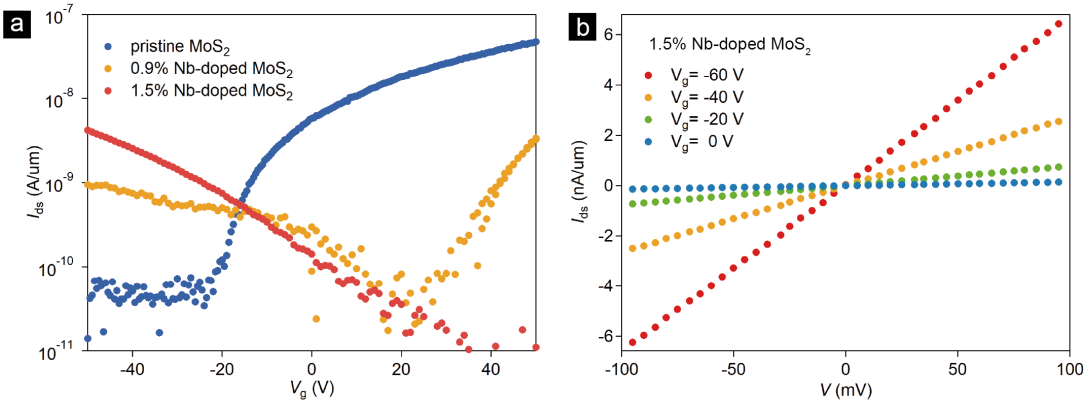

Figure 6.5: Electrical transport of Nb doped-MoS_2. (a) Transport properties of Nb-doped MoS_2 with various doping concentrations. A stack of Ti/Au is utilized as electrode contact. Source-drain voltage was fixed at 200 mV during the measurement. (b) I-V curves of 1.5% Nb-doped MoS_2 under various back-gate voltages at room temperature.

6.4 P-type NbS_2-MoS_2 heterojunctions

6.4.1 Atomistic and electronic structures of NbS_2-MoS_2 heterojunction

To shed theoretical insight into the heterojunction between metallic NbS_2 and p-type Nb-doped monolayer MoS_2, first-principle calculations were performed based on DFT. Density of states (DOS) and the band structure for the heterojunction are shown in this section.

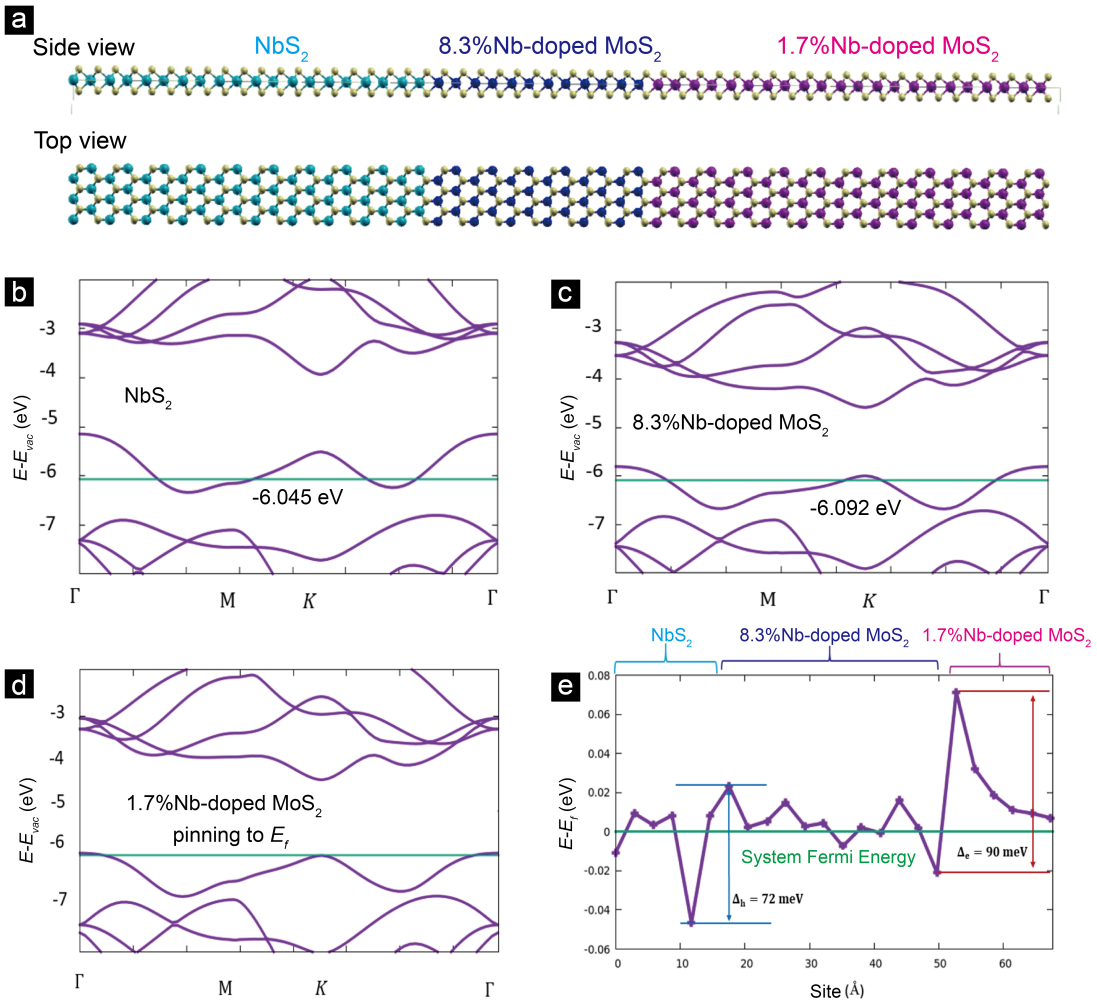

Figure 6.6: QM modeling of the NbS_2-MoS_2 lateral heterostructure with Nb doping. (a) Atomistic depictions in side and top views. (b-d) Band structure of the pure fragments, aligned as derived from the analysis of the electrostatic potential in the scattering system. (e) Profile of local Fermi-energy or local top of the valence band profile along the transmission direction derived from a fragment analysis of the electrostatic potential on metal atoms [191], with a highlighted potential jump at the buffer-phase/MoS_2 junction of 90 meV.

To model the NbS_2-MoS_2 lateral heterostructure at the Quantum-Mechanical (QM) level, we exploit the VCA (Virtual Crystal Approximation). The VCA is an approach to studying defected, disordered or alloyed systems, in which a crystal in its primitive periodicity is substituted in

part or in total with fictitious or virtual atoms (chemical elements) that interpolate between the behavior of real atoms (chemical elements). The VCA has been shown to lead to accurate results within the rigid band approximation.

To use VCA, we define "mixed" chemical elements composed of a given percentage of Nb and Mo elements. This allows us to rapidly analyze the structural and electronic properties of phases with Mo/Nb mixed composition. From this analysis, we create our QM structural model: a reasonably large unit cell (depicted in Figure 6.6a) made of (i) pure NbS_2, (ii) a Nb-doped MoS_2 buffer, and (iii) a slightly Nb-doped core/pristine MoS_2 (the Nb-doping content is around1.5% at the experimental level, set to 1.66% for convenience in the simulations). The buffer phase (ii) is introduced to mediate the 5% lattice mismatch between MoS_2 (3.19 Å at the DFT level) and NbS_2 (3.35 Å). Its doping level is set to 8.3%, as this doping is energetically the most stable, i.e., it has the minimum gradient of total energy and work function with respect to the lattice parameter.

Table 6.1: Work functions of the Nb doped-MoS_2 with different doping levels.

MoS_2	Work Function (TVB)	$Nb_{0.05}Mo_{0.95}S_2$	Work Function	$Nb_{0.25}Mo_{0.75}S_2$	Work Function
$a_y(a_{y\ MoS2})$	5.811939149 eV	$a_y(a_{y\ MoS2})$	5.9671202 eV	$a_y(a_{y\ MoS2})$	6.081930841 eV
$a_y(a_{y\ mid1})$	5.781925544 eV	$a_y(a_{y\ mid1})$	5.9371582 eV	$a_y(a_{y\ mid1})$	6.086986986 eV
$a_y(a_{y\ ave})$	5.75585326 eV	$a_y(a_{y\ ave})$	5.9117304 eV	$a_y(a_{y\ ave})$	6.092351383 eV
$a_y(a_{y\ mid2})$	5.729959984 eV	$a_y(a_{y\ mid2})$	5.88699017 eV	$a_y(a_{y\ mid2})$	6.09030485 eV
$a_y(a_{y\ NbS2})$	5.706176874 eV	$a_y(a_{y\ NbS2})$	5.86832532 eV	$a_y(a_{y\ NbS2})$	6.089847737 eV
$Nb_{0.5}Mo_{0.5}S_2$	Work Function	$Nb_{0.75}Mo_{0.25}S_2$	Work Function	NbS_2	Work Function
$a_y(a_{y\ MoS2})$	6.13604642 eV	$a_y(a_{y\ MoS2})$	6.087034861 eV	$a_y(a_{y\ MoS2})$	5.99782726 eV
$a_y(a_{y\ mid1})$	6.15643007 eV	$a_y(a_{y\ mid1})$	6.115360023 eV	$a_y(a_{y\ mid1})$	6.024071026 eV
$a_y(a_{y\ ave})$	6.17815938 eV	$a_y(a_{y\ ave})$	6.142211191 eV	$a_y(a_{y\ ave})$	6.045384714 eV
$a_y(a_{y\ mid2})$	6.19483337 eV	$a_y(a_{y\ mid2})$	6.158581548 eV	$a_y(a_{y\ mid2})$	6.064316963 eV
$a_y(a_{y\ NbS2})$	6.20451544 eV	$a_y(a_{y\ NbS2})$	6.172364855 eV	$a_y(a_{y\ NbS2})$	6.074000674 eV

As a technical note, we use the experimental definition of doping content, i.e., the percent of Nb out of the total number of atoms, while in VCA it is customary to use the x-atomic percent as the definition of the fictitious element. For clarity, 1.5% Nb-doping in core/pristine MoS_2 in the main text corresponds to x = 0.045 in the VCA (for computational convenience, we set x = 0.05 in the simulations, corresponding to 1.67%-global-doping), while 8.3% Nb-doping in the buffer phase in the main text corresponds to x = 0.25 in the VCA.

The VCA analysis of the pure phases confirms the dependence of band structure on lattice parameters [192]. Moreover, a fragment analysis [191] of the system, illustrated in Figure 6.6e, leads us to two further conclusions. First, the top of the valence band (TVB) of semiconducting MoS_2 is pinned to the Fermi level of the system. Second, there are two localized barriers in the electrostatic potential at the NbS_2/8.3%Nb-doped-MoS_2/1.7%Nb-doped-MoS_2 junctions of 72

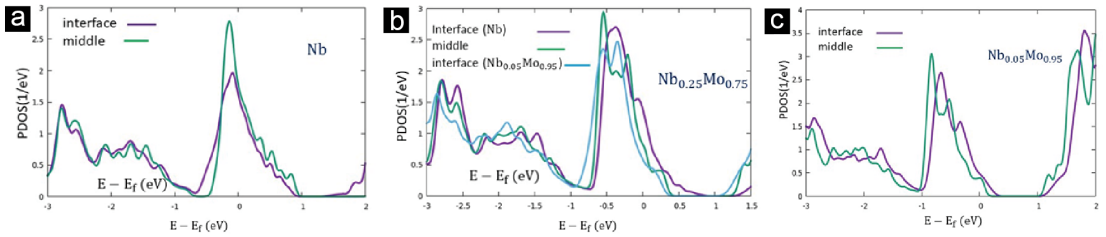

Figure 6.7: Projected density of states of the Nb doped-MoS_2 interfaces. Projected Density of States (PDOS) of selected metal atoms at the interface or in the middle of each fragment in the scattering region: (a) Nb atoms, (b) $Nb_{0.25}Mo_{0.75}$ (corresponding to 8.3% Nb-doping) and (c) $Nb_{0.05}Mo_{0.95}$ (corresponding to 1.7% Nb-doping).

meV and 90 meV, which suggest a suppression of transmission at the heterojunctions, despite the uncertainty in the values of these barriers due to the deformation of the band structure following the formation of charge dipoles at the interface. In synthesis, QM modeling predicts that the lattice and electronic mismatch at the NbS_2-MoS_2 lateral heterostructure is overcome by Nb doping into MoS_2 (as produced by growing NbS_2 in excess of Nb onto pre-prepared MoS_2 flakes and evidenced by EDX and ADF-STEM measurements) mediating structurally and electronically the NbS_2-MoS_2 transformation, and giving rise to a p-type NbS_2-MoS_2 heterojunction, also possessing good electrical transport properties.

In Table 6.1 we report the work function of minimal unit cells as a function of the (fixed) vertical lattice parameter y. In detail, we fix the lattice parameter y, we DFT-relax the other lattice parameter and the atomic coordinates, and we calculate the system work function on the so-relaxed geometry. Two main conclusions are apparent from the simulation results. (1) The work function has a non-monotonous behavior as a function of x, with a maximum for x around 0.50. (2) The system with x = 0.25 is the most stable, i.e., it has the least variation of the work function (and accordingly of total energy, not shown) as a function of geometrical constraints: the work function stays at around 6.08/6.09 eV varying by only 1 hundredth of an eV in the whole range of the y-lattice-parameter between that of relaxed pure MoS_2 (3.19 Å at the DFT-optimized level) and that of relaxed pure NbS_2 (DFT-optimized value is around 3.35 Å). The $Nb_{0.25}Mo_{0.75}S_2$ phase (corresponding to 8.3% Nb-doping) is thus optimally suited to mediating and relaxing epitaxial mismatch in the NbS_2-MoS_2 lateral heterostructure. Incidentally, note that the work function of pure NbS_2 never goes beyond the TVB of MoS_2 at any level of compressive strain.

Finally, in Figure 6.7 we plot the Projected Density of States (PDOS) on selected metal atoms as derived from the DFT analysis of the composite NbS_2/8.3% Nb-doped MoS_2/1.7% Nb-doped MoS_2 system, illustrating the deformation of the band structure following the formation of charge dipoles at the interface.

6.4.2 Transport properties of p-type NbS_2-MoS_2 heterojunctions

To characterize the transport performance of our MOCVD-grown NbS_2/p-type MoS_2 lateral heterostructures, FET devices based on the heterojunctions were fabricated on Si/SiO_2 substrate (shown in the insets of Figure 6.8b-c), where NbS_2 is used as a 2D contact comparing to the devices with conventional 3D contact shown in Figure 6.5.

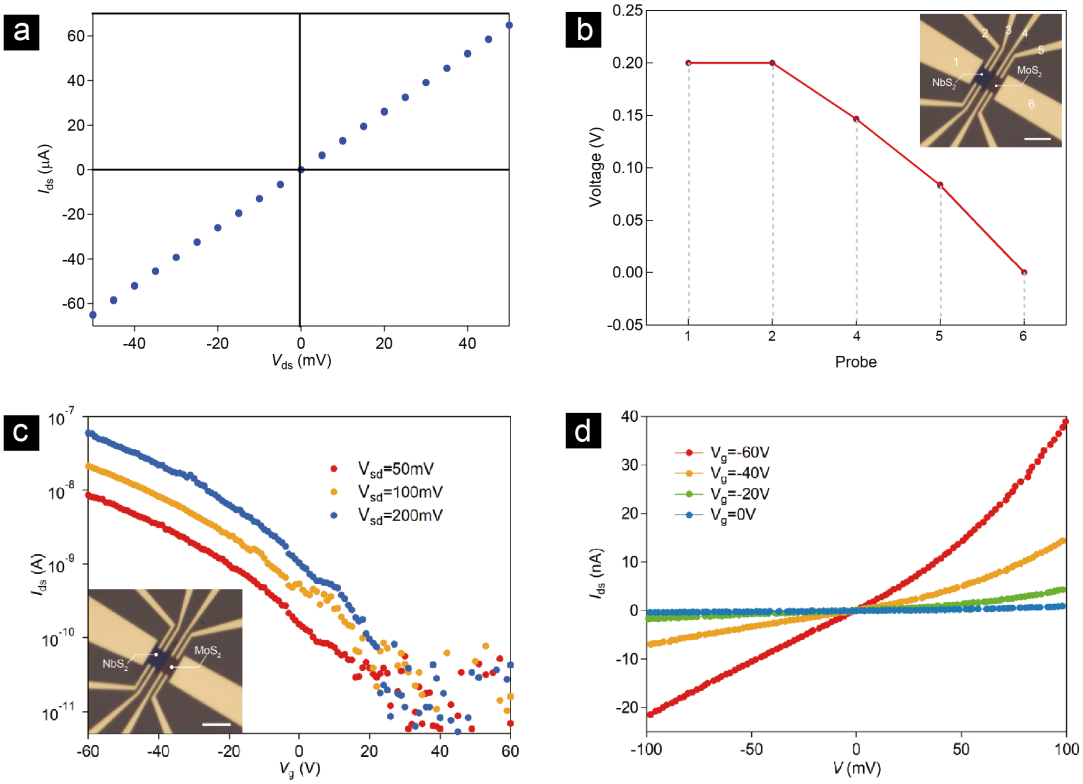

Figure 6.8: Transport properties of p-type NbS_2-MoS_2 heterojunction. (a) Room-temperature I-V characterization of NbS_2 in the heterostructure. Metallic behaviour with a total resistance (R_{tot}) of 770 Ω was confirmed by the linear I-V curve. (b) Voltage potential measured from different probes on the device shown in the inset. Source-drain voltage is fixed at 0.2 V between Probe 1 and Probe 6, while back-gate voltage is 60 V during the measurement. (c) Room-temperature transfer characteristic for the FET device based on the NbS_2-MoS_2 lateral heterojunction, shown in the inset. Scale bar: 10 μm. Back-gate voltage V_g is applied to the substrate with a bias voltage ranging from 50 mV to 200 mV. P-type behavior is demonstrated from the transfer curves. (d) Four-probe I-V characterization of an NbS_2-MoS_2 lateral heterojunction at room temperature for different values of back-gate voltage.

A linear I-V curve confirms metallic behavior of our NbS_2 at room temperature with a total resistance (R_{tot}) of 770 Ω(see in Figure 6.8a). Figure 6.8b presents the voltage potential measured from different probes on the device shown in the inset. Source-drain voltage is fixed at 0.2 V between Probe 1 and Probe 6, while back-gate voltage is 60 V during the measurement. A negligible voltage drop is observed in NbS_2 channel compared to the MoS_2 channel. Figure

6.8c demonstrates the room-temperature transfer characteristic curves collected from the FET devices shown in the bottom-left image with a Nb doping concentration of 1.5%. A typical p-type behavior with an on/off ratio of 1×10^4 was observed and the four-probe field-effect mobility is calculated to be 1.46 $cm^2V^{-1}s^{-1}$, defined as

$$\mu = \frac{dI_{ds}}{dV_g} \cdot \frac{L}{W \cdot C_i \cdot V} \tag{6.1}$$

where L and W are the channel length and width between two voltage probes, respectively, while C_i is the capacitance between Nb-doped MoS_2 channel and the back gate per unit area). The four-probe I-V curves in Figure 6.8d present the output characteristics of the NbS_2-MoS_2 lateral heterojunction at room temperature. A non-symmetric current rectification behavior is visible from the I-V curves, indicating the presence of a Schottky contact at the heterointerface.

6.5 Further studies and conclusion

6.5.1 Schottky barrier height extraction

To study the Schottky barrier height (SBH) at NbS_2/p-type MoS_2 junction, temperature-dependent transport measurements were carried out under various gate voltages, as shown in Figure 6.9a. In order to obtain an accurate estimate of the barrier, we fit the measurement data with the results of quantum transport simulations of the heterojunction. We use the following transport model to perform our simulation: NbS_2 and MoS_2 monolayers were described by a nearest-neighbor, two-orbital tight-binding Hamiltonian. The Hamiltonian parameters were calibrated to obtain the best agreement with the DFT band structures of the uncoupled materials in the energy range of interest for transport phenomena. This model leaves as free parameters the hopping amplitude between the monolayers at the heterointerface and the height of the Schottky barrier in flat-band conditions. The value of both these quantities was iteratively adjusted in order to obtain the best fit of the I_{sd}-V characteristics. The value t_{IF} of the hopping amplitude considered in simulations also accounts for the cumulative effect of the defects and disorder localized at interface, which is otherwise assumed ideal in our model. We extimated t_{IF} around 2×10^{-6} eV, a very small value, which suggests a strongly defective interface in addition to the localized barriers already observed in Figure 6.6e.

The cross-section of the simulated device is sketched in Figure 6.9b. The simulation domain in the transport direction is restricted to a neighborhood of the heterointerface. For a given I_{sd} current, the voltage drop over this region is smaller than the experimentally measured V, due to the presence of a residual parasitic sheet resistance R_s associated to the 5 µm-long MoS_2 region between the heterojunction and the voltage contact. In order to map the source-to-drain bias over the simulation region into V, and thus, obtain results directly comparable with

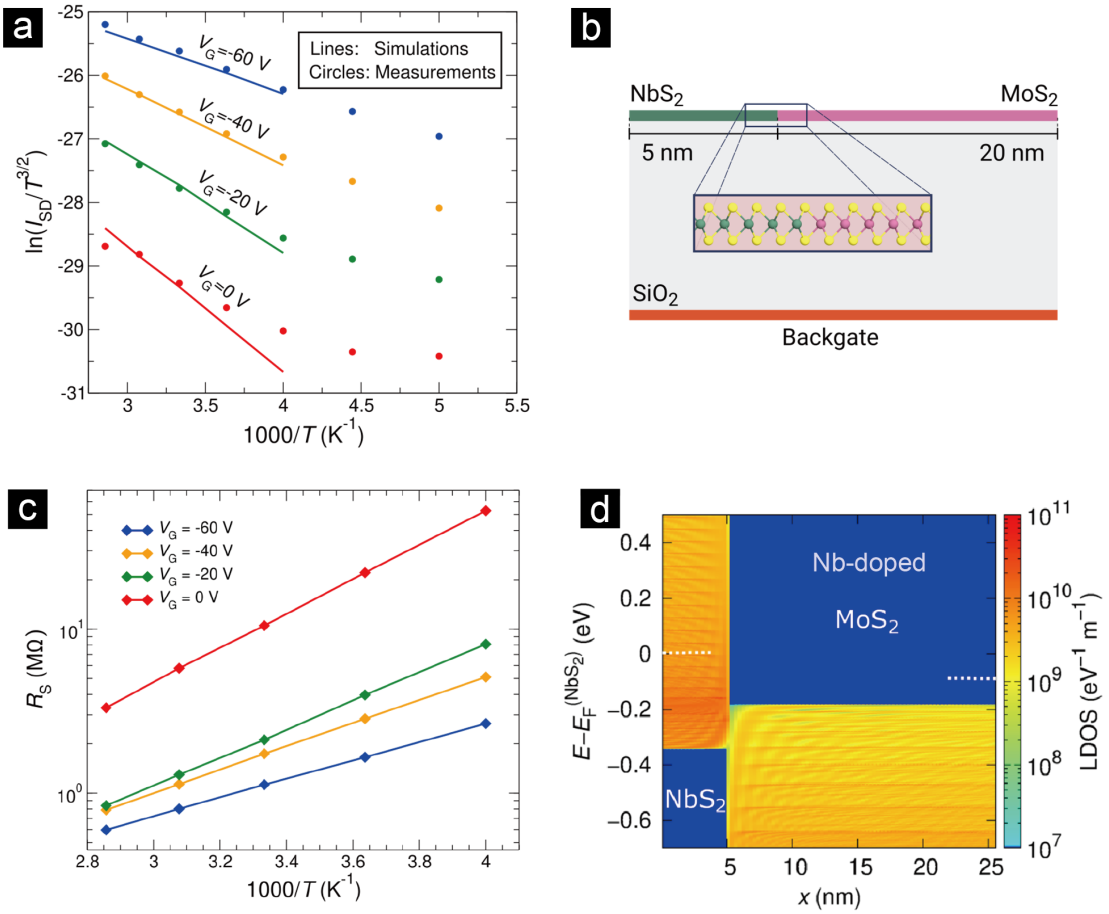

Figure 6.9: Schottky barrier height extraction of Nb-doped NbS_2-MoS_2 heterojunction. (a) Comparison of the Arrhenius plots obtained from measurements (dots) and simulations (lines). The probe voltage was fixed to 100 mV during the measurement. (b) Sketch of the simulated device (not to scale). (c) Sheet resistance R_s extracted from simulations as a function of temperature. (d) Colormap of the density of states along the device close to flat-band conditions. The dotted lines denote the Fermi level at the NbS_2 and MoS_2 contacts.

the experimental data, we estimated R_s from the I_{sd}-V measurements at room temperature by means of the Cheung method [193]. The dependence of R_s on the temperature was modeled by assuming

$$R_s \propto \exp\left(\frac{\Delta E_v}{k_B T}\right) \tag{6.2}$$

where the distance ΔE_v between the top of the valence band and the Fermi level in the MoS_2 was estimated from the simulation of the metal/SiO_2/MoS_2 stack in equilibrium conditions. It is shown in Figure 6.9c for different values of V_g.

To take into account the substitutional doping due to Nb atoms, MoS_2 was assumed to be p-doped with a concentration of 6×10^{12} cm^{-2}. This value is in reasonable agreement with the doping levels extracted from the EDX data shown in Figure 6.3c-d. Furthermore, a uniform density of states $D_{it} = 3.4\times10^{13}$ cm^{-2} was included in the MoS_2 band gap to model the presence of traps at the interface with SiO_2. The simulation results for the Arrhenius plot are compared with the corresponding experimental data in Figure 6.9a. The plots show that our numerical model closely reproduces the dependence of the current on both the back-gate voltage and the bias voltage, for temperatures sufficiently close to 300 K and higher. The deviations of the experimental Arrhenius curves from the exponential behavior for temperatures no larger than 50 K are likely due to disorder-induced fluctuations of the Schottky barrier height along the NbS_2-MoS_2 interface [194]. This effect is not taken into account in our simulations. Figure 6.9d shows the local density of states along the device close to flat band conditions. According to the map, the corresponding Schottky barrier height turns out to be ${\Phi^{FB}}_B = 230$ meV.

6.5.2 Conclusion

In summary, one-step MOCVD method is utilized to synthesize NbS_2-MoS_2 lateral heterostructures with Nb dopants present in monolayer MoS_2 in this chapter. A visible interface and high quality of the as-grown heterostructures were prove by detailed characterization. Due to the increased hole concentration from Nb doping, monolayer MoS_2 shows a p-type transfer characteristic with a high current on/off ratio of around 10^4. A detailed compositional model of the heterojunction interface, describing the transition between the pure lattice-mismatched phases of NbS_2 and MoS_2 through a buffer phase of 8.3% Nb-doped MoS_2 was derived through DFT simulations. Furthermore, a value of 230 meV for the Schottky barrier height at the NbS_2-MoS_2 interface was estimated by fitting the electrical measurements with the results of self-consistent quantum transport simulations. Our work makes an instructive combination of substitutional doped TMDC materials and 2D metal-semiconductor heterostructures, which paves a prospective way to designing innovative nano-scale devices and CMOS-like 2D circuits.

7 2D circuits enabled by patterning TMDC heterostructures

7.1 Introduction

7.1.1 2D materials: an ideal platform for in-memory computing

The initial von Neumann architecture [195], with separate processing and storage units, has imposed limitations on the ability of modern processors to meet the growing demand [196] for high-performance and low-consumption computation required by emerging data-intensive applications [117]. Therefore, a highly energy-efficient hardware is urgently desired to maintain a sustainable development of these applications, such as machine learning [197], [198] and the Internet of Things. Among these new-generation architectures [195], [199], [200], [201], in-memory computing shows a prominent advantage, as it performs computation directly in the physical layer of memories [134], [135], [136] by combining Kirchhoff's and Ohm's laws, making it a highly desirable solution to avoid the bottleneck of data processing [129].

To fully harness the potential of this architecture, many material systems have been explored for in-memory computing [202]. Among them, semiconducting two-dimensional (2D) transition metal dichalcogenides (TMDCs) have been attracting great attention due to their atomic scale thickness [23], layer-dependent band structure [167] and favorable electrical properties [116], [43]. In particular, monolayer molybdenum disulfide (MoS_2) is most widely investigated and presents ideal semiconducting behavior with a large direct bandgap of 1.8 eV [21] and a high current on/off ratio of 10^8 in n-type field-effect transistor (FET) [23]. Furthermore, integrated nanoelectronics based on MoS_2 have been rapidly emerging in recent years, such as in-memory devices [117], [203], [204], [205] and artificial neural networks (ANN) [129], indicating monolayer MoS_2 a prospective material candidate for low energy-consuming and high effective computing.

7.1.2 2D metal-semiconductor heterostructures: properties and synthesis

However, the device performance is still hindered by the large contact resistance between semiconductor channel and conventional electrode contacts, making it a challenge to satisfy the requirements of scalable applications and advanced technologies. 2D metal-semiconductor (M-S) junctions based on TMDC heterostructures [12] are expected to reduce contact resistance by weakening Fermi level pinning and modulating the Schottky barrier [6]. These lateral and vertical TMDC heterostructures [114], [185], [206], [207] can be obtained using chemical vapor deposition (CVD) or metal-organic CVD method, resulting in a high-crystallinity growth and precise control of layer number but a limited scalability for integrated device design [208]. In comparison, some other attempts, like sulfurization [209], [210], [211], [212], benefit from a large-area growth and high reproducibility but still struggle in improving crystal quality and achieving monolayer growth. The success of this approach strongly depends on identifying an optimal technique to produce high-quality and easily integrable TMDC heterostructures.

7.1.3 Outline of this chapter

Here in this chapter, we demonstrate a versatile and scalable method, by combining metal-organic chemical vapor deposition (MOCVD) and sulfurization, to produce TMDC metal-semiconductor heterostructures with high growth quality and high application flexibility, and employ them in in-memory devices and 2D circuits. In Section 7.2, synthetic process of NbS_2-MoS_2 patterned heterostructures will be demonstrated by using the "two-step" route, and several optical characterizations will be conducted to examine the growth quality. In Section 7.3, field-effect transistors (FETs) are fabricated by using MoS_2 as an active channel material and NbS_2 as 2D contacts. By introducing 2D NbS_2 contact, the contact resistance and Schottky barrier height are suppressed compared to pristine MoS_2 FETs, leading to a significant enhancement of the mobility and on/off current ratio. In Section 7.4, we demonstrate the application of floating-gate memories using patterned heterostructures, showing a larger memory window than that of pristine MoS_2. Furthermore, a precise and continuous modulation of the conductance of the FGFETs can be realized by tuning the gating voltages, with a stable data storage capability. The research findings in this chapter support the material platform of 2D TMDC metal-semiconductor heterojunctions for the next generation of in-memory processors, enabling machine learning implementations like deep neural networks to fully exploit this architecture.

The main ideas and methods in this chapter are developed by Zhenyu Wang, Dr. Guilherme Migliato Marega and Prof. Andras Kis. Most experiments and analysis are performed by Zhenyu Wang, while the work in some subsections is performed in close collaboration with my colleagues in LANES laboratory, as listed below. The fabrication of memory devices in Section 7.4 is mainly performed by Zhenyu Wang, with help of Dr. Guilherme Migliato Marega and Eloi Collette. Memory device measurements in Section 7.4 are performed with great assistant of Dr. Guilherme Migliato Marega and Eloi Collette.

The research findings presented in this chapter produce the following to-be-submitted paper: "*Wafer-Scale Integrated 2D Circuits Enabled by Patterning TMDC Metal-Semiconductor Heterostructures*", **in preparation**.

7.2 Production of NbS_2-MoS_2 patterned heterostructures

7.2.1 Synthetic process

Our NbS_2-MoS_2 patterned heterostructures were produced by a "two-step" route, combining metal-organic chemical vapor deposition (MOCVD) and sulfurization, which is shown as the schematic in Figure 7.1. Firstly, 2-inch wafer-scale monolayer MoS_2 film was grown by MOCVD on a sapphire substrate by the method shown in Section 4.2.1 and transferred onto a Si/SiO_2 substrate by thermal-release tape method shown in Section 3.4.2. Subsequently, photolithography and dry etching technique were utilized to pattern MoS_2 channels. Afterwards, photolithography was applied again to make Nb patterns and a layer of 3nm-thick Nb was evaporated to prepare for NbS_2 growth. Finally, the sample was sulfurized in a quartz tube at 400 °C for 1 h with a H_2S flow rate of 30 sccm and a Ar flow rate of 100 sccm to produce NbS_2 and obtain heterostructures. This approach can be extended to produce other TMDC heterostructures which consist of monolayer semiconductor and few-layer metal.

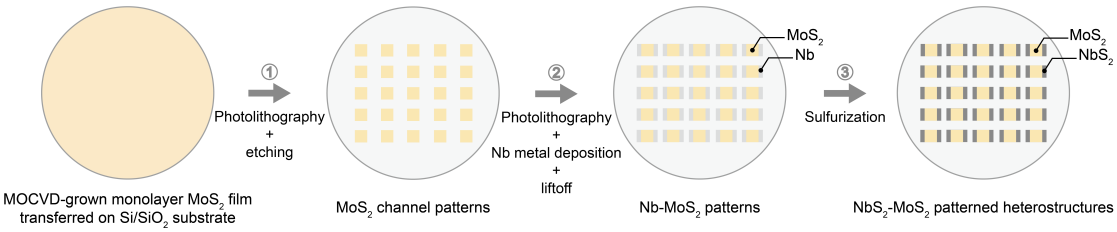

Figure 7.1: Schematic illustration of process flow to produce NbS_2-MoS_2 patterned heterostructures. The process flow of producing NbS_2-MoS_2 patterned heterostructures includes: MOCVD growth of monolayer MoS_2, photolithography and dry etching step to make MoS_2 channels, photolithography and metal deposition step to make Nb patterns and sulfurization, as illustrated from left to right.

7.2.2 Optical characterizations

Figure 7.2a shows the AFM image of a NbS_2 sample on a Si/SiO_2 substrate after sulfurization, which indicates a smooth surface with a thickness of 12 nm. The Raman spectra in Figure 7.2b present strong signals located at 335 cm^{-1} ($E^1 1_{2g}$) and 388 cm^{-1} (A_{1g}), in agreement with the vibration modes of 2H-phase NbS_2, verifying a good quality of our sulfurized NbS_2. Figure 7.2c demonstrates XPS spectra (shown as orange dots) with corresponding fitting curves (shown as blue and red curves) of the sulfurized NbS_2 samples. Identical peaks for Nb^{+4} and Nb^{+5} states are visible in the fitting curves, verifying the exist of Nb^{+4} and Nb^{+5} chemical bonds generated from sulfurization. There are no metallic Nb signals observed on our NbS_2 samples, indicating

a complete sulfurization without Nb residue.

To check the quality of MOCVD-grown monolayer MoS_2 after sulfurization process, AFM and Raman spectra were performed on the MoS_2 region in the heterostructure. Figure 7.2d demonstrates the AFM image of monolayer MoS_2 on sapphire substrate showing a smooth surface and a thickness of 0.7 nm. Figure 7.2e shows the Raman spectra obtained on MoS_2 region in the heterostructures before and after sulfurization. Both of the spectrum perform two sharp peaks at 383 cm^{-1} ($E^1{}_{2g}$) and 402 cm^{-1} (A_{1g}), confirming the nature and good quality of monolayer MoS_2, indicating there is no oxidization or Nb doping after sulfurization. A typical optical micrograph of NbS_2-MoS_2 patterned heterostructures is demonstrated in Figure 7.2f, from which we can see rectangular MoS_2 channels with a width of 5 μm and sulfurized NbS_2 patterns with a width of 10 μm.

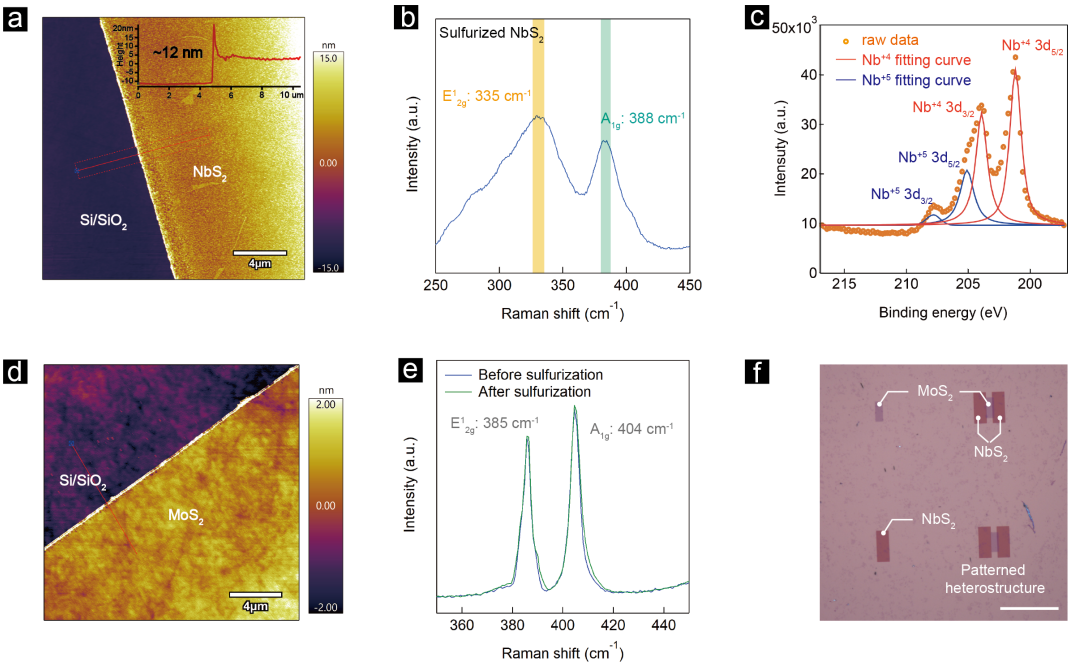

Figure 7.2: Optical characterizations of NbS_2-MoS_2 patterned heterostructures. (a) AFM image and its corresponding height profile of sulfurized NbS_2 in the heterostructure. (b) Raman spectra at room temperature for NbS_2 samples sulfurized on a Si/SiO_2 substrate. (c) XPS spectra and its corresponding fitting curves of sulfurized NbS_2. (d) AFM image of monolayer MoS_2 in the heterostructure after sulfurization. (e) Room-temperature Raman spectra obtained on MoS_2 region in the heterostructures before and after sulfurization. (f) Optical micrograph of NbS_2-MoS_2 patterned heterostructures on Si/SiO_2 substrate. Scale bar: 50 μm.

7.3 Electrical transport characterization of NbS_2-MoS_2 patterned heterostructures

7.3.1 Device structure

To examine the electrical performance, FET devices were fabricated based on our NbS_2-MoS_2 patterned heterostructures. Structural schematic of a 2-probe FET device is shown in Figure 7.3a and an optical micrograph is presented in the left panel of Figure 7.3b. The patterned heterostructure was produced on a Si/SiO_2 substrate as demonstrated in the previous part, where monolayer MoS_2 serves as transistor channel and NbS_2 is used as novel 2D contact. Si substrate is used as back gate, while a Ti/Au stack is utilized as source/drain electrodes connecting with NbS_2. To avoid contact resistance during the electrical measurements, 4-probe FETs were also fabricated as shown in the right panel of Figure 7.3b. The voltage potential measured from different probes on the device is demonstrated in Figure 7.3c, from which a negligible voltage drop was observed on NbS_2 region compared to MoS_2 channel. In addition, room-temperature I-V characterization of sulfurized NbS_2 in the inset of Figure 7.3c shows liner curve with a total resistance (R_{tot}) of 600 Ω. Both of the above results indicate a metallic behavior of sulfurized NbS_2, serving as 2D contact for the MoS_2 channel.

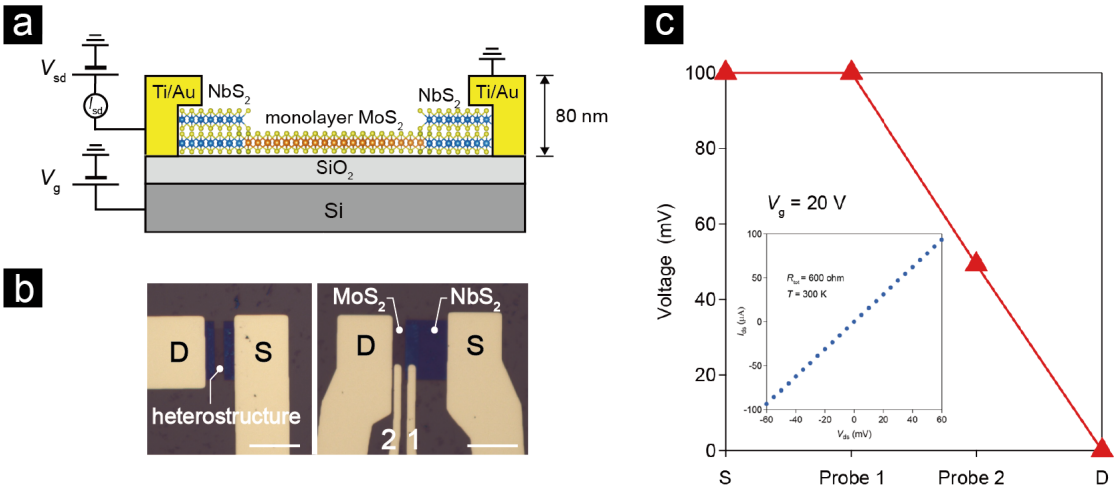

Figure 7.3: Device structure of FET based on NbS_2-MoS_2 patterned heterostructures. (a) Schematic of 2-probe FET device structure fabricated using NbS_2-MoS_2 patterned heterostructures. (b) Optical micrograph of a 2-probe FET (left) and a 4-probe FET (right) fabricated using NbS_2-MoS_2 patterned heterostructures. Scale bar: 20 μm. (c) The voltage potential measured from different probes on the device shown in the right panel of (b). Inset: I-V characterization of sulfurized NbS_2 at room temperature, showing a metallic behaviour with a total resistance (R_{tot}) of 600 Ω.

7.3.2 Transport behavior and Schottky barrier height extraction

Figure 7.4a presents the gating characteristics of the transistor with 2D NbS_2 contact shown in the right panel of Figure 7.3b as well as a MoS_2 transistor with conventional 3D Ti/Au contact for comparison. A typical behavior of n-type channel can be observed for the both devices, while the heterostructure exhibits an on/off ratio of 10^6 and four-probe field-effect mobility of around 38.5 $cm^2V^{-1}s^{-1}$, which is defined as

$$\mu = \frac{dI_{ds}}{dV_g} \cdot \frac{L}{W \cdot C_i \cdot V_{ds}} \tag{7.1}$$

where L and W are the channel length and width between two voltage probes, respectively, while C_i is the capacitance between MoS_2 channel and the back gate per unit area, and V_{12} is the voltage measured between the two probes. The mobility value of the heterostructure is higher than that of pristine MoS_2 (5.8 $cm^2V^{-1}s^{-1}$). Figure 7.4b demonstrates four-probe output characteristics of the same devices in Figure 7.4a, where a linear I-V curve with a higher on-state current was observed for the heterostructure compared to pristine MoS_2. Together with the data in the inset of Figure 7.4b showing the two-probe I-V characterization of the transistors, we can calculate the contact resistance of the heterostructure with 2D NbS_2 contact as a value of 0.9 $M\Omega \bullet \mu m$, which is less than half of the value (2.1 $M\Omega \bullet \mu m$) for pristine MoS_2 with conventional 3D Ti/Au contact.

To study the Schottky barrier height (SBH), temperature-dependent transport measurements were carried out under various gate voltages, and the corresponding Arrhenius plots for NbS_2-MoS_2 heterojunction (2D contact) are shown in Figure 7.4c. The SBH values under each gate voltage can be extracted by using the 2D thermionic emission equation and shown in Figure 7.4d:

$$I_{SD} = A_{2D} T^{3/2} \exp\left(-\frac{q}{k_B T}(\phi_B - \frac{V}{n})\right) \tag{7.2}$$

where A_{2D} is the 2D equivalent Richardson constant, T is the temperature, q is the electronic charge, k_B is the Boltzmann constant, ϕ_B is the Schottky barrier height value, V is the probe voltage across the interface and n is the ideality factor. The effective SBH of NbS_2-MoS_2 heterojunction was obtained as a value of 123 meV under flat-band bias condition as presented in Figure 7.4d, which is lower than that of MoS_2-Ti interface.

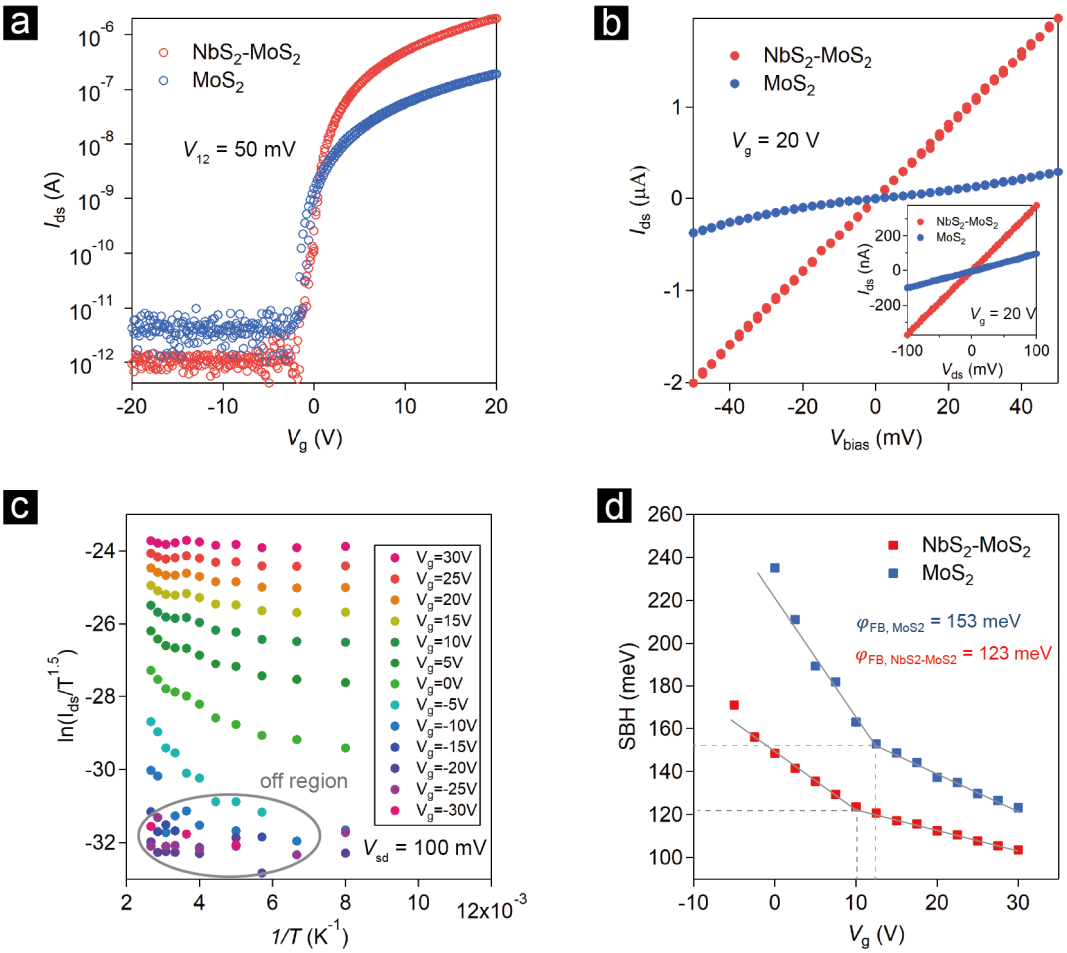

Figure 7.4: Transport behavior and Schottky barrier extraction of NbS_2-MoS_2 patterned heterostructures. (a) Room-temperature transfer characteristic for the FET devices based on pristine MoS_2 and NbS_2-MoS_2 patterned heterostructures, respectively. (b) Four-probe *I-V* characterization of pristine MoS_2 and NbS_2-MoS_2 patterned heterostructures at room temperature, respectively. Inset: Two-probe *I-V* characterization of pristine MoS_2 and NbS_2-MoS_2 patterned heterostructures at room temperature, respectively. (c) $ln(I_{ds}/T^{1.5})$ versus $1/T$ at different back-gate voltages in the temperature range from 125 K to 350 K for NbS_2-MoS_2 heterojunction. The probe voltage was fixed at 100 mV during the measurement. (d) The extracted Schottky barrier height values from the data in (c) and the flat-band SBH for MoS_2-Ti interface and NbS_2-MoS_2 heterojunction, respectively.

7.4 Floating-gate memories based on NbS_2-MoS_2 patterned heterostructures

7.4.1 Device structure

We demonstrate floating-gate memories based on our NbS_2-MoS_2 patterned heterostructures, where monolayer MoS_2 and sulfurized NbS_2 are used as the transistor channel and 2D contact,

respectively. Figure 7.5a and b show the side-view schematic of the floating-gate memory structure and its optical micrograph. Our memory devices use Si substrate as back gate and a 5nm-thin Pt layer as floating gate. Both blocking and tunnel oxides (270 nm and 7 nm thick, respectively) consist of SiO_2 to achieve effective modulation of the electric field within the semiconducting channel.

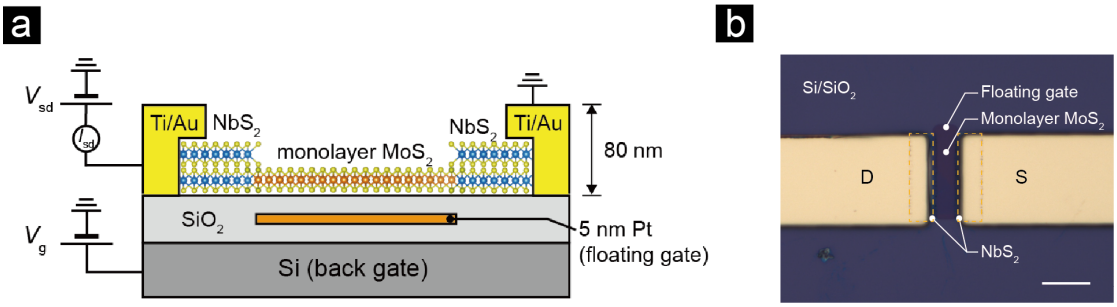

Figure 7.5: Device structure of floating-gate FET based on NbS_2-MoS_2 patterned heterostructures. (a),(b): Side-view schematic and optical micrograph of the floating-gate memory device based on NbS_2-MoS_2 patterned heterostructures, respectively. Scale bar: 10 μm.

7.4.2 Memory device Programming

Room-temperature gating characteristic of our memory device based on the heterostructure is presented by the red curve in Figure 7.6a, with a comparison showing the transport behavior of pristine MoS_2 (blue curve). A memory window of 13.8 V can be estimated from the total shift of the memory threshold voltage in our NbS_2-MoS_2 sample, which is slightly larger than that of pristine MoS_2 (12 V). Notably, the heterostructure shows an on/off ratio of 10^7, two orders higher than the value of pristine MoS_2, which is attributed to lower contact resistance and Schottky barrier height as we demonstrated in the previous part. Supplementary Figure S5 shows temperature-dependent gating characteristics of our memory device based on the heterostructure. A lower on-state current and a narrower memory window were observed with the temperature decreasing from 300 K to 10 K, verifying the floating-gate memory behavior controlled by the amount of charge stored in the charge trapping layer.

To retrieve the memory state of the device, we applied a constant voltage ($V_{g\,(read)}$) to the gate and measured the drain-source current after programming with different gate biases. A linear behavior of the output characteristics is demonstrated in Figure 7.6b, indicating ohmic-like contacts. Figure 7.6c illustrates various states of normalized conductance over time, showing the capacity of setting the channel conductance through programming voltages and the stability within one-hour range.

By applying short potentiative and depressive pulses, we can control the device conductance states to the desired level. In Figure 7.6d, the conductance of the memory device can be also continuously set by applying a number of pulses. Linear control over the conductance was achieved when applying potentiative pulses (-10 V amplitude, 10 ms duration and 1 s rest

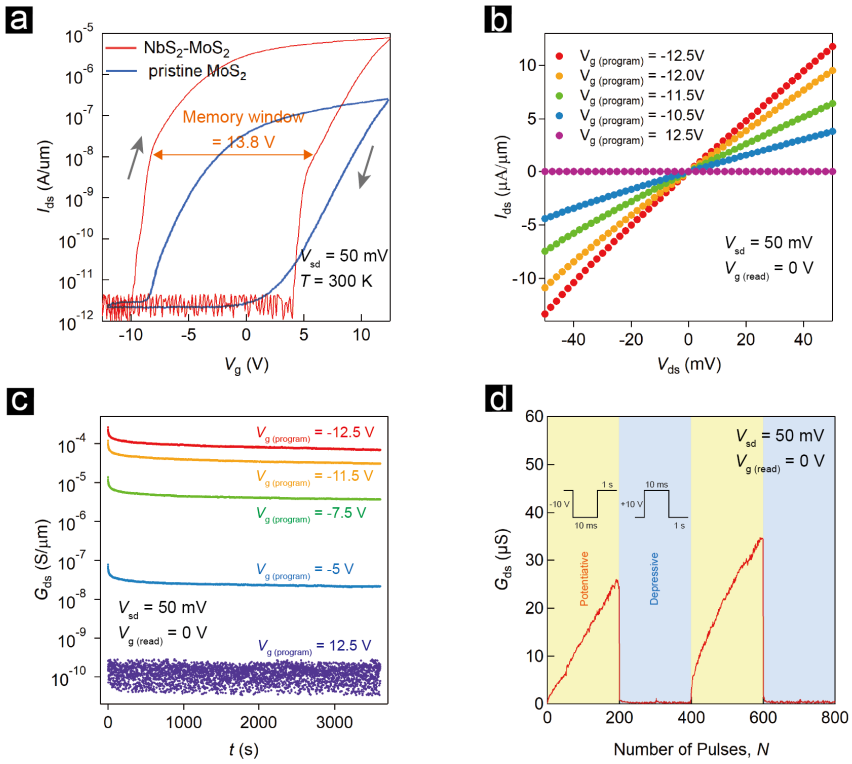

Figure 7.6: Memory programming of floating-gate FET based on NbS_2-MoS_2 patterned heterostructures. (a) Transfer characteristics of the floating-gate FETs fabricated with NbS_2-MoS_2 heterostructure (red curve) and pristine MoS_2 (blue curve) collected for two distinct directions of gate voltage sweep (indicated by grey arrows) at room temperature. (b) Output characteristics of the floating-gate FETs based on NbS_2-MoS_2 patterned heterostructures after having been programmed with different programming voltages. (c) The conductance over time of a memory device which is programmed by different gate voltages. (d) The device conductance as a function of number of pulses, showing a continuous control and linear evolution of the conductance by applying voltage pulses to the gate.

time) to the gate, while the device was reset by using depressive pulses (+10 V amplitude, 10 ms duration and 1 s rest time).

7.4.3 Retention time and endurance testing

To examine the ability of data storage of our floating-gate memory devices, we first recorded the drain-source conductance G_{sd} verse time at room temperature with a $V_{g\ (read)}$ = 0 V after having been programmed by $V_{g\ (program)}$ = +12.5 V and $V_{g\ (program)}$ = -12.5 V, respectively, as the red curves show in Figure 7.7a. The conductance value remained stable over 10 h without loss of data, indicating a strong data storage capability. Moreover, we tested our sample at elevated temperature (425 K) to calculate the equivalent retention time at room temperature by using Arrhenius model:

$$A_f = \exp\left(\frac{E_a}{k}\left(\frac{1}{T_n} - \frac{1}{T_e}\right)\right) \tag{7.3}$$

where A_f is the acceleration factor, E_a is the activation energy (A typical activation energy is 0.8 eV for effects related to charge loss when no voltage is applied to the device), k is Boltzmann's constant (8.617×10^{-5} eV/K), T_n is the temperature of the normal environment and T_e is the elevated temperature. As demonstrated by the blue curves in Figure 7.7a, the conductance exhibits a faster degradation rate at high temperature but the data can still be stored over 18.2 h. An acceleration factor of 8973 can be calculated by the Arrhenius model, which means that if the data lasted for 18.2 h at 425 K, it would last 8973 times longer at 300 K, or about 19 years.

Endurance test was performed in our memory device to examine its re-programmability, as presented in Figure 7.7b. Drain-source current was plotted as a function of the number of program/erase (P/E) cycles. In each P/E cycle, there is a 100-ms +11.5 V pulse for the erase operation and a 100-ms -11.5 V pulse for the program operation. Remarkably, our memories demonstrate remarkable durability and inherent robustness, enduring over 63,000 programming pulses before failure occur, displaying a credible non-volatile performance.

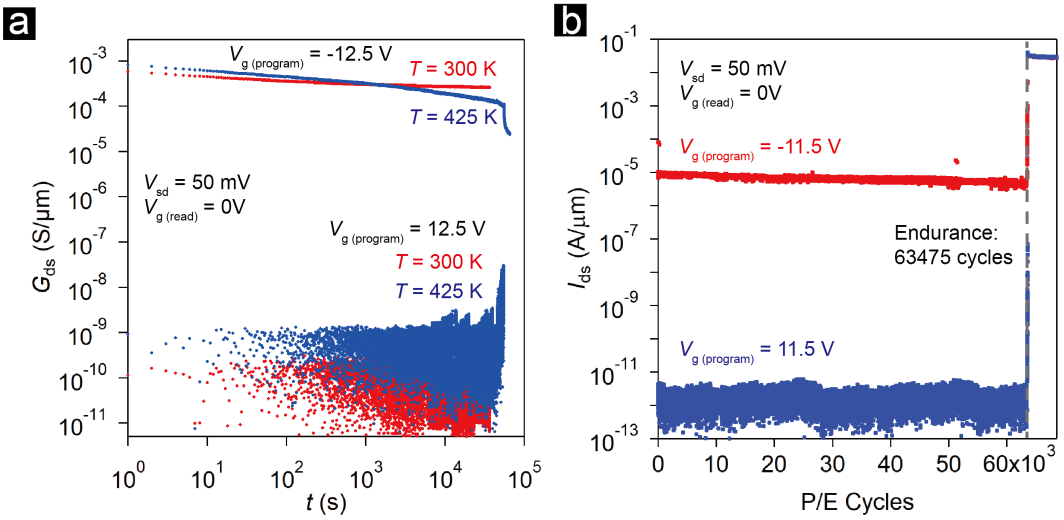

Figure 7.7: Retention time and endurance testing of floating-gate FET based on NbS_2-MoS_2 patterned heterostructures. (a) Two-state retention time at different temperatures, showing the drain–source conductance (G_{ds}) over time. Red curve and blue curve show the data obtained at 300 K and 425 K, respectively. Data storage shows a faster degrading rate at high temperature. (b) Endurance test of a floating-gate memory device, showing output current (I_{ds}) as a function of the number of program/erase (P/E) cycles. The device lose its memory ability after 63475 cycles.

7.5 Conclusion

In conclusion, we demonstrate our exploration of producing NbS_2-MoS_2 patterned heterostructures by a "two-step" route and using them as an active channel material with novel 2D contacts to develop FETs, in-memory devices and 2D circuits. Compared to pristine MoS_2, the heterostructure shows a lower contact resistance and Schottky barrier height, resulting in a significant improvement of the memory window and on/off current ratio. Moreover, we realize a precise and continuous modulation of the conductance of our FGFETs, enabling us to use them as building blocks for reconfigurable logic circuits in the future. Our findings provide a versatile approach to produce 2D TMDC heterostructures and highlight their potential for the development of next-generation low-power electronics and 2D circuits.

8 Conclusion and outlook

Two-dimensional (2D) materials are considered as promising material platform for the next-generation electronic devices due to their outstanding electrical and mechanical properties with nano-scale thickness, as well as the ability to enhance and tune properties by forming van der Waals heterostructures. Thus, it is essential to develop a versatile and scalable method of synthesizing 2D materials and their heterostructures with a large scale and high quality. In this thesis work, we first explore the growth condition of large-scale production of individual 2D materials by using metal-organic chemical vapor deposition (MOCVD) method, and realize the wafer-scale growth of continuous monolayer MoS_2 film and epitaxial growth of large-size NbS_2 single grains. With a success of the synthesis method, we employ the MOCVD-grown monolayer MoS_2 film in in-memory computing devices, realizing a large-scale integration, and study the superconductivity performance of CVD-grown 2H-NbS_2 at low temperature. Furthermore, we explore the synthesis route of NbS_2-MoS_2 heterostructures by using "one-step" and "two-step" route based on CVD method, and achieve NbS_2-MoS_2 heterostructures in both grain and wafer scale. We also study the electrical properties and band structure of the heterostructures in both experimental and theoretical term, and explore the possibility to integrate them in in-memory computing devices.

In the next sections, the main results of these topics and the further research directions will be discussed in light of the entire thesis work.

8.1 TMDC materials produced by MOCVD method

8.1.1 Summary of the results

In Chapter 4, we explore the optimization of MOCVD growth conditions to achieve uniform and continuous monolayer MoS_2 film on a 2-inch sapphire wafer, including the amount of Mo precursors, the effect of NaCl, and etching-gas confinement. To examine the crystal quality and confirm the monolayer nature, several characterization techniques are performed on the as-grown MoS_2 film, such as AFM, Raman, PL and STEM. Moreover, the MOCVD-grown

monolayer MoS_2 is employed as active channel material to develop logic-in memory devices, artificial neural networks and vector–matrix multiplication processor, proving the possibility to realize energy-efficient 2D circuits based on 2D materials for in-memory computing.

In Chapter 5, we demonstrate a synthesis route of 2D NbS_2 single crystals by CVD method. The as-grown NbS_2 shows a large size, controllable thickness and epitaxial orientation. By applying various growth parameters, such as temperature and the gas flow ratio of H_2S and Ar, different morphologies of as-grown NbS_2 crystals are observed. We also find that our CVD-grown NbS_2 crystals show thickness-dependent transition between 3R and 2H-phase structures, which is further confirmed by Raman spectroscopy, STEM and electrical transport measurements. Furthermore, the CVD-grown 2H-phase NbS_2 shows superconductivity and take place BKT-type superconducting transition below 3 K.

8.1.2 Perspective for future research

In the context of future research on MOCVD-grown MoS_2, one of the promising directions is to further scale up the production of single-layer MoS_2 and to achieve wafer-scale MoS_2 single crystal by refining growth techniques. This scalability is crucial to meet the demands of high-density integrated circuits in industrial applications, which impacts the device reliability and performance. Concurrently, it is essential to develop semiconductor technologies, such as circuit architecture, interconnectivity, and fabrication processes, to exploit wafer-scale MoS_2 on higher-dimensional integrated applications. This comprehensive approach, combining scalable production, circuit design and fabrication, will transform MOCVD-grown MoS_2 into high-performance integrated circuits, driving innovation in the semiconductor industry.

Regarding future research on CVD-grown NbS_2, one prospective direction involves the pursuit of wafer-scale production of superconducting NbS_2 by CVD or MOCVD method, which is imperative for its practical applications and facilitating its integration into large-scale electronic devices. Another direction is to enhance the superconducting properties of NbS_2 through precise control of growth parameters and the introduction of novel doping techniques. This can contribute to the development of superconducting devices with improved performance and efficiency in the field of quantum technologies, energy storage applications electronics and advanced sensing technologies.

8.2 TMDC heterostructures produced by CVD method

8.2.1 Summary of the results

In Chapter 6, we use "one-step" MOCVD method to synthesize NbS_2-MoS_2 lateral heterostructures, and find that the monolayer MoS_2 is substitutionally doped with Nb atoms. Several characterization techniques, such as AFM, Raman spectroscopy, PL, aberration-corrected STEM and EDX, are used to examine the interface and confirm the high-quality lateral het-

erostructure growth and substitutional Nb doping. Due to the increased hole concentration from Nb doping, the FET device based on the heterojunction exhibits a p-type transport behavior with a high on/off current ratio of around 10^4. A compositional model through DFT simulations of the heterojunction interface is demonstrated to calculate the band structures of Nb-doped MoS_2 and reveal the Fermi level alignment at the interface with the critical role of doping. Furthermore, by fitting the electrical measurements with the results of self-consistent quantum transport simulations, the Schottky barrier height at the NbS_2-MoS_2 interface is estimated to be a value of 230 meV.

In Chapter 7, we show a scalable method of producing NbS_2-MoS_2 patterned heterostructures by a "two-step" route. The heterostructures are utilized as an active channel material with novel 2D contacts for the development of field-effect transistors, in-memory devices and 2D circuits. Compared to pristine MoS_2, the heterostructure show a larger memory window and higher on/off current ratio, which can be attributed to a weakened contact resistance and Schottky barrier height. Moreover, the conductance of the FGFET can be precisely and continuously controlled by gating voltages, making it a promising building block for reconfigurable logic circuits.

8.2.2 Perspective for future research

This thesis work has explored the electrical properties of TMDC heterostructures and their applications in 2D circuits as discussed above. Here are several perspective directions for the future research of TMDC heterostructures synthesized by CVD or MOCVD method:

In terms of material synthesis, first of all, continued efforts should be dedicated to refining and optimizing the CVD or MOCVD growth methods for a larger scale production. Enhancements in scalability, reproducibility, and control over the heterostructure interface are imperative for broader applications. Secondly, exploration of novel TMDC combinations, such as different TMDC combinations and hybrid heterostructures by combining TMDCs with other 2D materials or even traditional semiconductors, will broaden the scope of potential applications in electronic devices and circuits. Strain engineering and surface modification is also promising for tailored electronic and chemical properties. Furthermore, it is crucial to develop advanced characterization techniques to gain deeper insights into the structural and electronic properties of TMDC heterostructures. Techniques such as in-situ monitoring during growth and advanced spectroscopy methods can provide a more comprehensive understanding of the heterostructure interfaces.

With regard to device development, it is promising to explore the integration of TMDC heterostructures into three-dimensional architectures by stacking multiple 2D layers or by combining them with 3D materials. Such an approach shows the potential to study unique electronic and optical properties, offering opportunities for the design of multifunctional devices. Additionally, it is important to investigate strategies for addressing the challenges related to large-scale production, integration into existing technologies, and compatibility

with standard semiconductor processes, in order to scale up TMDC heterostructure devices for practical industrial applications.

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List of Abbreviations and Symbols

Symbol	Meaning
μ	Mobility
μ_{FE}	Field effect mobility
μm	Micrometre
μs	Microsecond
Ω	Ohm
θ	Twist angle
δ	Lattice constant
$\Delta \mathrm{E_v}$	distance between the top of the valence band and the Fermi level
ΔG_m	Activation energy for atomic migration
ΔG^*	Critical free energy barrier for nucleation
ΔT	Difference between melting temperature and growth temperature
γ_c	Surface energy of nucleus
$\gamma_{c,edge}$	Surface energy of nucleus edge
γ_s	Surface energy of substrate
$\gamma_s c$	Interfacial energy between substrate and nucleus
$\xi_{\mathrm{GL}}(0)$	Zero-temperature coherence length
ϕ_0	Magnetic flux quantum
ϕ_B	Schottky barrier height
$\Phi^{\mathrm{FB}}{}_{\mathrm{B}}$	Schottky barrier height at flat band condition
π	Pi
ρ	Electric resistivity
σ	Electric conductivity
ε	Dielectric constant
ε_0	Vacuum dielectric constant
^{o}C	Degree celsius
$(C_2H_5)_2S$	Diethyl sulfide
Å	Angstrom
2D	Two-dimensional
A	Ampère
$\mathrm{A_{2D}}$	Two-dimentional equivalent Richardson constant
AC	Alternating current

ADF	Annular dark field
A_f	Acceleration factor
AFM	Atomic force microscope
ALD	Atomic layer deposition
Al_2O_3	Aluminum oxide
Ar	Argon
Au	Gold
B	magnetic field
B_{c2}	Upper critical field
BKT	Berezinskii-Kosterlitz-Thouless
Br	Bromine
BTBAS	Bis(tertiary-butylamino)silane
CBM	Conduction band minimum
CDW	Charge density wave
C_i	Capacitance per unit area of the insulating layer
Cl	Chlorine
CMOS	Complementary metal-oxide-semiconductor
CO_2	Carbon dioxide
Cr	Chromium
CVD	Chemical vapour deposition
DC	Direct current
DES	Diethyl sulfide
DFT	Density functional theory
DI water	Deionized water
DMSO	Dimethyl sulfoxide
E_a	Activation energy
EBL	Electron beam lithography
EDS	Energy dispersive X-ray spectroscopy
eV	Electronvolt
F	Fluorine
FET	Field-effect transistor
FFT	Fast Fourier transform
FGFET	Floating-gate field-effect transistor
FWHM	Full width at half-maximum
G_{ds}	Drain-source conductance
GL	Ginzburg-Landau
GPA	Geometric phase analysis
gr	Grating
G_{tot}	Total conductance
H_2	Hydrogen
H_2O	Water
H_2S	Hydrogen sulfide

HAADF	High-angle annular dark filed
hBN	Hexagonal boron nitride
HfO_2	Hafnium Oxide
HRSTEM	High-resolution scanning transmission electron microscope
Hz	Hertz
IFFT	Inverse fast Fourier transition
I_{in}	Input current
I_{on}	On-state current
I_{off}	Off-state current
IPA	Isopropanyl alcohol
J	Joule
K	Kelvin
KI	Potassium iodide
KOH	Potassium hydroxide
L	Channel length
LED	Light-emitting diode
LPCVD	Low pressure chemical vapor deposition
MBE	Molecular beam epitaxy
MFC	Mass flow controller
min	Minute
MMA	Methyl methacrylate
Mo	Molybdenum
MoO_3	Molybdenum oxide
$Mo(CO)_6$	Molybdenum hexacarbonyl
MOCVD	Metal-organic chemical vapour deposition
MoS_2	Molybdenum disulfide
$MoSe_2$	Molybdenum diselenide
mrad	Milliradian
N_2	Nitrogen gas
NaCl	Sodium chloride
Na_2MoO_4	Sodium molybdate
Nb	Niobium
NbS_2	Niobium disulfide
$NbSe_2$	Niobium diselenide
nm	nanometer
O_2	Oxygen
P/E	Programming/Erasing
PECVD	Plasma-enhanced chemical vapor deposition
Pd	Palladium
PDOS	Projected density of states
PDMS	Polydimethylsiloxane
PL	Photoluminescence

PMMA	Poly(methyl methacrylate)
Pt	Platinum
PVD	physical vapor deposition
RHEED	Reflection high-energy electron diffraction
q	Electronic charge
QM	Quantum-Mechanical
rpm	Revolutions per minute
R_{2D}	Sheet resistance of 2D materials
R_c	Contact resistance
R_N	Normal-state resistance
RRR	Residual resistance ratio
R_s	Residual parasitic sheet resistance
R_{Tc}	superconducting-state resistance
R_{tot}	Total resistance
R_{xx}	Longitudinal resistance
SBH	Schottky barrier height
sccm	Standard cubic centimeters per minute
Se	Selenide
SEM	Scanning electron microscopy
Si	Silicon
Si_3N_4	Silicon nitride
SiO_2	Silicon dioxide
STEM	Scanning transmission electron microscopy
T_{BKT}	BKT transition temperature
T_c	Superconducting transition critical temperature
T_{c0}	Critical temperature at zero magnetic field
T_e	elevated temperature
TEM	Transmission electron microscopy
Ti	Titanium
t_{IF}	hopping amplitude
T_m	melting temperature
TMDC	Transition metal dichalcogenide
T_n	Temperature of the normal environment
V	Volts
V_{12}	Voltage drop between probe 1 and 2
VBM	Valence band maximum
VCA	Virtual crystal approximation
vdW	Van der Waals
V_{ds}	Drain-source voltage
V_{erase}	Erasing Voltage
V_{prog}	Programming voltage
V_{read}	Reading voltage

V_{TH}	Threshold voltage
V_g	Gate voltage
V_s	Sulfur vacancy
W	Tungsten
$W(CO)_6$	Tungsten hexacarbonyl
WO_3	Tungsten trioxide
WS_2	Tungsten disulfide
WSe_2	Tungsten diselenide
XeF_2	Xenon difluoride
XPS	X-ray photoelectron spectroscopy

List of Publications

Publications relevant to this thesis

1. Wang, Z., Marega, G.M., Collete, E., Radenovic, A. & Kis, A. *Wafer-Scale Integrated 2D Circuits Enabled by Patterning TMDC Metal-Semiconductor Heterostructures*, **in preparation**.

2. Wang, Z., Tripathi, M., Golsanamlou, Z., Kumari, P., Lovarelli, G., Mazziotti, F., Logoteta, D., Fiori, G., Sementa, L., Marega, G.M., Ji, H.G., Zhao, Y., Radenovic, A., Iannaccone, G., Fortunelli, A. & Kis, A. *Substitutional p-type doping in NbS_2-MoS_2 lateral heterostructures grown by MOCVD*. **Advanced Materials (2023)**, 35 (14), 2209371. doi:10.1002/adma.202209371.

3. Wang, Z., Cheon, C.-Y., Tripathi, M., Marega, G.M., Zhao, Y., Ji, H. G., Macha, M., Radenovic, A. & Kis, A. *Superconducting 2D NbS_2 grown epitaxially by chemical vapor deposition*. **ACS Nano (2021)**, 15 (11), 18403–18410. doi:10.1021/acsnano.1c07956.

4. Migliato Marega, G., Ji, H.G., Wang, Z., Pasquale, G., Tripathi, M., Radenovic, A. & Kis A. *A large-scale integrated vector–matrix multiplication processor based on monolayer molybdenum disulfide memories*. **Nature Electronics (2023)**, 6, 991–998. doi:10.1038/s41928-023-01064-1

5. Migliato Marega, G., Wang, Z., Paliy, M., Giusi, G., Strangio, S., Castiglione, F., Callegari, C., Tripathi, M., Radenovic, A., Iannaccone, G. & Kis, A. *Low-power artificial neural network perceptron based on monolayer MoS_2*. **ACS Nano (2022)**, 16 (3), 3684–3694. doi:10.1021/acsnano.1c07065.

6. Migliato Marega, G. Zhao, Y., Avsar, A., Wang, Z., Tripathi,M., Radenovic, A. & Kis, A. *Logic-in-memory based on an atomically thin semiconductor*. **Nature (2020)**, 587 (7832), 72–77. doi:10.1038/s41586-020-2861-0.

Other publications

1. Zhao, Y., Tripathi, M., Čerņevičs, K., Avsar, A., Ji, H.G., Marin, J.F.G, Cheon C.-Y., Wang, Z., Yazyev, O.V. & Kis, A. *Electrical spectroscopy of defect states and their hybridization in monolayer MoS_2*. **Nature Communications (2023)**, 14, 44. doi:10.1038/s41467-022-35651-1.

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3. Piacentini, A., Marian, D., Schneider, D.S., Marín, E.G., Wang, Z., Otto, M., Canto, B., Radenovic, A., Kis, A., Fiori, G., Lemme, M.C. & Neumaier, D. *Stable Al_2O_3 encapsulation of MoS_2-FETs enabled by CVD grown h-BN*. **Advanced Electronic Materials (2022)**, 8 (9), 2200123. doi:10.1002/aelm.202200123

4. Zhang, M., Lihter, M., Chen, T.-H., Macha, M., Rayabharam, A., Banjac, K., Zhao, Y., Wang, Z., Zhang, J., Comtet, J., Aluru, N. R., Lingenfelder, M., Kis, A. & Radenovic, A. *Super-resolved optical mapping of reactive sulfur-vacancies in two-dimensional transition metal dichalcogenides*. **ACS Nano (2021),** 15 (4), 7168-7178. doi:10.1021/acsnano.1c00373.

5. Schneider, D.S., Reato, E., Lucchesi, L., Wang, Z., Piacetini, A., Bolten, J., Marian, D., Marin, E.G., Radenovic, A., Wang, Z., Fiori, G., Kis, A., Iannaccone, G., Neumaier, D. & Lemme, M.C. *MoS_2/graphene lateral heterostructure field effect transistors*. **Device Research Conference (DRC) (2021)**, pp 1-2. doi: 10.1109/DRC52342.2021.9467156.

6. Piacentini, A., Schneider, D., Otto, M., Canto, B., Wang, Z., Radenovic, A., Kis, A., Lemme, M.C, & Neumaier, D. *Low hysteresis MoS_2-FET enabled by CVD-grown h-BN encapsulation*. **Device Research Conference (DRC) (2021)**, pp 1-2. doi:10.1109/DRC52342.2021.9467236.

7. Erbas, B., Rubio, C.A., Liu, X., Pernollet, J., Wang, Z., Bertsch, A., Penedo, M., Fantner, G., Banerjee, M., Kis, A., Boero, G. & Brugger, J. *Combining thermal scanning probe lithography and dry etching for grayscale nanopattern amplification*. **Microsystems & Nanoengineering (2023), accepted**.

8. Liu, X., Erbas, B., Rubio, C.A., Rivano, N., Wang, Z., Jiang, J., Bienz, S., Kumar, N., Sohier, T., Penedo, M., Banerjee, M., Fantner, G., Zenobi, R., Marzari, N., Kis, A., Boero, G. & Brugger, J. *Dielectric topography engineering induced strain enhances mobility of MoS_2 FETs*, **submitted**.

9. Wells, R., Diercks, N.J., Boureau, V., Wang, Z., Zhao, Y., Nussbaum, S., Esteve, M., Caretti, M., Johnson, H., Kis, A., Sivula, K. *Composition-tunable transition metal dichalcogenide nanosheets via a scalable, solution-processable method*, **submitted**.

10. Marega, G. M., Ottesen, A., Wang, Z., Ji, H.G., Radenovic, A. & Kis, A. *Memristors based on floating-gate memories using monolayer MoS_2*, **in preparation**.

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- Material synthesis and characterization of wafer-scale semiconductors, superconductors and their heterostructures by MOCVD method.
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- Prepared polycrystalline ferroelectric lead-free thin films by sol–gel/spin-coating method
- Explored the effect of alloying on the structural and ferroelectric characteristics

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VOLUNTEERING AND OUTREACH

Enterprise Visit "Material Science in Acoustic Devices" *Dec 2017-Jan 2018*

Team leader and organizer (team of 20) *Goertek Company, Shandong, China*

- Contact the company for the visit and sponsor
- Host a seminar with the research team of the company

PRIZES, AWARDS, FELLOWSHIPS

National Scholarship for Outstanding Overseas Students *Chinese Ministry of Education, Jul 2023*

Academic and Research Excellence Scholarship *Tsinghua University, Oct 2018*

Prize of the First 3D printing Contest in Beijing *Tsinghua University, Nov 2017*

PUBLICATIONS IN PEER-REVIEWED SCINETIFIC JOURNALS

As First Author/Equal Contribution

- **ACS Nano**, 2021, 15 (11), 18403–18410. Superconducting 2D NbS2 Grown Epitaxially by Chemical Vapor Deposition. LINK
- **Advanced Materials**, 2023, 35 (14), 2209371. Substitutional P-Type Doping in NbS2–MoS2 Lateral Heterostructures Grown by MOCVD. LINK

As Co-author

- **Nature**, 2020, 587 (7832), 72–77. Logic-in-Memory Based on an Atomically Thin Semiconductor. LINK
- **ACS Nano**, 2022, 16 (3), 3684–3694. Low-Power Artificial Neural Network Perceptron Based on Monolayer MoS2. LINK
- **Nature Electronics**, 2023, 6, 991–998. A Large-Scale Integrated Vector–Matrix Multiplication Processor Based on Monolayer Molybdenum Disulfide Memories. LINK
- **ACS Nano**, 2021, 15 (4), 7168–7178. Super-Resolved Optical Mapping of Reactive Sulfur-Vacancies in Two-Dimensional Transition Metal Dichalcogenides. LINK
- **Advanced Materials**, 2022, 34 (48), 2108469. Zero-Bias Power-Detector Circuits Based on MoS2 Field-Effect Transistors on Wafer-Scale Flexible Substrates. LINK
- **Nature Communications**, 2023, 14 (1), 44. Electrical Spectroscopy of Defect States and Their Hybridization in Monolayer MoS2. LINK
- **Advanced Electronic Materials**, 2022, 8 (9), 2200123. Stable Al2O3 Encapsulation of MoS2-FETs Enabled by CVD Grown h-BN. LINK

CONFERENCE PROCEEDINGS

- **Flatland Beyond Graphene 2023** (200+ attendees) *Oct 2023, Prague, Czeck Republic*
  Talk: "Substitutional P-type Doping in NbS2–MoS2 Lateral Heterostructures Grown by MOCVD"
- **10 Years of Material Science in 2Ds** (50+ attendees) *May 2023, Madrid, Spain*
  Presentation: "2D Superconducting NbS_2 and p-type NbS_2-MoS_2 heterostructures grown by CVD."
- **Graphene Flagship Core 3 - WP3 Enabling Materials Meeting** *Oct 2022, Gran Canaria, Spain*
  Presentation: "Floating-gate memories enabled by NbS_2-MoS_2 patterned heterostructures."

SKILLS

- **Languages:** Mandarin (Native), English (Professional, C1/C2), French (Fluent, B1)
- **Data Analysis:** Origin, Igor pro, image analysis with ImageJ
- **CAD:** DesignCAD Express, Solidworks, Klayout
- **Text and Graphics:** Office, LaTeX, Blender, Adobe Illustrator, Adobe Photoshop
- **Fabrication:** 5-year experience in device designment, e-beam lithography (EBL), laser writer lithography, photolithography, dry and wet etching, thin films deposition (ALD, etc)
- **Characterization:** Electrical measurements, Atomic force microscopy (AFM), Scanning electron microscopy (SEM), Raman and photoluminescence spectroscopy
- **Industrial Standards:** Cleanroom ISO 5-7, chemical hazards, cryogenic and high vacuum systems
- **Softskills:** Project management, team leading and collaboration, technical writing, public speaking,
- **Social Media:** 3-year experience in photography and video editing, 40,000 followers in social medias including Instagram, Tiktok.