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# A Wireless Power Conversion Chain with Fully On-chip Automatic Resonance Tuning System for Biomedical Implants

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**ABSTRACT** This paper presents a wireless power conversion system designed for biomedical implants, with integrated automatic resonance tuning. The automatic tuning mechanism improves power transfer efficiency (PTE) by finely tuning the resonant frequency of the power link and maximizing the rectified voltage. This adjustment ensures robust and reliable remote powering, even in the face of environmental changes and process variations, while also minimizing tissue exposure to power. On-chip switched array capacitors are connected in parallel with the resonant capacitor, and the system identifies the optimal switched capacitor combination for the highest rectified voltage by iterating over each of them. The proposed system is implemented and fabricated in standard 180 nm CMOS technology, with a total area of 0.339 mm<sup>2</sup>, and its operation is verified. The measurement results demonstrate that this system provides tolerance up to mismatches equivalent to 75 pF capacitance variation in LC tank,  $\pm 15\%$  LC variation in this design. The system offers a PTE enhancement from 9.1% to 30.2% in case of high LC variation, and the tuning control consumes 154.7  $\mu$ W of power during resonance tuning. Moreover, the power conversion chain delivers an optimized rectified voltage along with a regulated voltage of 1.8 V.

**INDEX TERMS** Automatic resonance tuning, biomedical implants, inductive link, power conversion chain, rectifier, wireless power transmission (WPT).

## I. Introduction

Implanted medical devices have been extensively studied for various monitoring and therapeutic applications. Among all challenges, powering the devices is crucial for the functioning of all subsequent modules. Wireless power transmission (WPT) for battery and battery-less devices is preferred due to a lower risk of infection and few limitations to patients' daily activity. Different wireless powering methods have been studied, and inductive powering stands out for its higher power transfer efficiency (PTE) and capability of half-duplex data transmission over a single inductive link [1]–[5]. An adequately high PTE is required to reduce the energy dissipated into the tissue for safety reasons, and maximizing PTE is commonly achieved by estimating the load of the secondary unit and matching the quality factors of both the primary and secondary stages [6].

Some studies have been devoted to finding a theoretically optimal circuit. For instance, authors in [6] have analyzed the optimal resistive loading while researchers in [7] have proposed optimal resonant load transformation on resonators with any fixed loading impedance. The resonance capacitor is connected in series with the inductor, and additional components are added in parallel with the resonator [8]. All component values can be calculated from the optimal quality factors. However, even with a careful design, variations in distance, temperature and other factors are inevitable. This discrepancy may cause a deviation of the resonating frequency from the designed value and a mismatch between the primary and secondary resonance frequency, diminishing the PTE. The mismatches observed in the WPT system can be classified into three distinct categories: (a) LC variations, which assume a constant

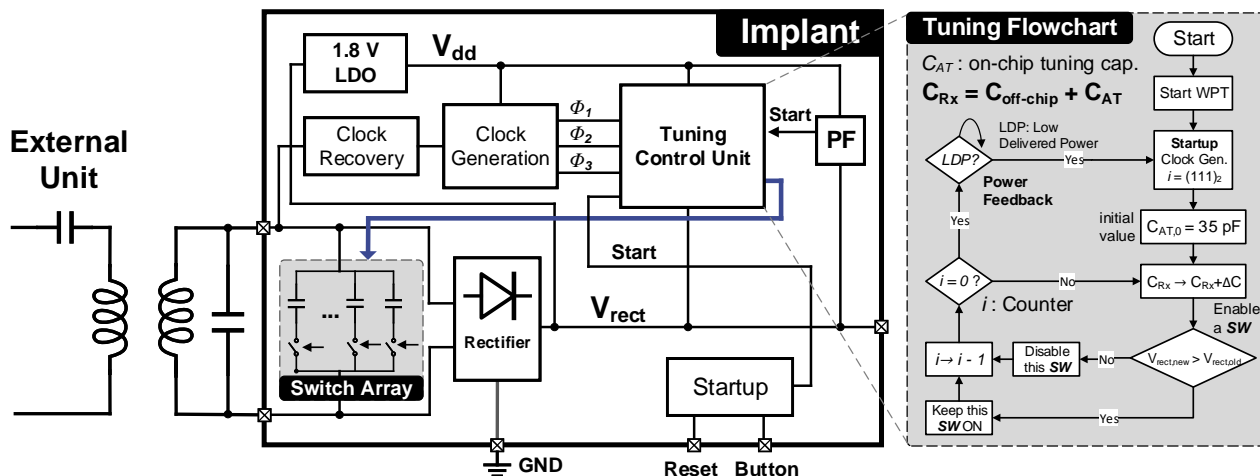


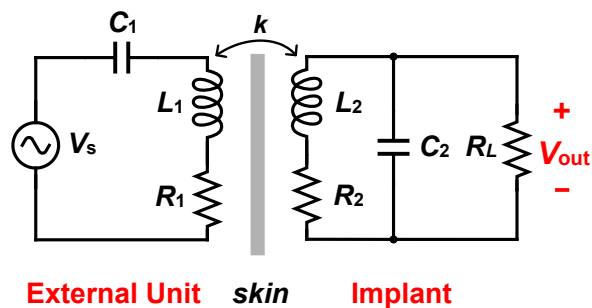
FIGURE 1. Block diagram of the proposed automatic resonance tuning system and its flowchart of the tuning algorithm, inductive link, and wireless power conversion chain including the rectifier and 1.8 V low-dropout (LDO) voltage regulator.

inductance resulting in capacitor variations, (b) variations in distance, and (c) angular misalignments. These three mismatches have notable implications for wireless power transfer and the corresponding coupling coefficient. Precise tuning and wireless power transfer are achieved at a specific coupling coefficient ( $k$ ). Each of these mismatches can indeed influence the coupling coefficient ( $k$ ). For example, an increase in coil distance leads to a decrease in  $k$ , and angular misalignment has a considerable impact on reducing  $k$ . Consequently, these mismatches influence the resonance frequency and can be addressed by developing a tuning system. A summary is presented in the following paragraphs with some tuning system examples on the primary or secondary side, most of which involve a tuning capacitor.

There are different types of automatic tuning systems, classified based on the tuning method (SAR [9], [10] and monotonic sweeping [11]–[15]) and the detection target (rectified voltage/current or swing amplitude). Monotonic sweeping utilizes a counter and control logic to adjust the resonance capacitor dynamically, while SAR logic employs a specific method for automatic tuning. In systems with battery chargers, the rectified current can be used as the detection target, enhancing efficiency through a current sensor [15]. Alternatively, instead of monitoring the rectified voltage, the swing amplitude can be observed to reduce delays associated with stabilizing the voltage and charging the rectifier's output capacitor. The design of the tuning system at the external unit (primary side) is more investigated as it is generally not implanted and can carry more functional units, with few considerations on its size and power dissipation. Earlier designs started with air-coupled inductive links, some of which require direct communication between the primary and secondary. Authors in [16] have equipped both the primary and secondary with Freescale's MC1322 which includes a microcontroller unit (MCU), an analog-to-digital converter (ADC), and a radio. During the tuning process, the

MCU of the primary firstly sets a frequency and the MCU at the secondary performs a measurement of power and sends it to the primary with the same link as transmitting other data; the primary MCU is programmed with an algorithm that searches for the optimal resonance frequency with new and prior power measurements, and will reset the frequency; the above steps repeat until maximum power on the load is reached. This design is not favored for implantable medical devices (IMDs) due to their excessive size and power consumption. Apart from physical tuning capacitors, more studies have turned their focus to switched capacitor banks or matrices where the MCU or logic circuits directly control the status of the switches. A capacitor matrix is introduced in [17] for magnetic coupling, in which a capacitor matrix is connected in series with the primary coil and another matrix connected in parallel. A current monitor measures the current from the primary driver and the MCU controls the switches with their impedance-matching algorithm. A binary search for the optimal capacitor set is adopted, so the size and quantity of the capacitor matrix should be carefully designed for a trade-off between resolution and tuning time. There are a lot more trials presented and studied in [18], [19].

Since the size and power of an MCU are concerns for implanted devices, more implementations are based on custom circuits specific to the tuning function. In [20], a real-time capacitor compensation scheme is described, where the current phase-out of the secondary coil is detected by a dual-edge sampler and the resonant coupling capacitor is gradually compensated by switching binary-weighted capacitors. Though this implementation is claimed to be faster than binary search as the capacitance variation is restricted to 25%, the power and clock of the secondary coil seem to come from external sources, which is unrealistic for practical IMDs. Authors in [10] control the switches through successive approximation register (SAR) logic and corresponding start-up circuits. Instead of binary-weighted



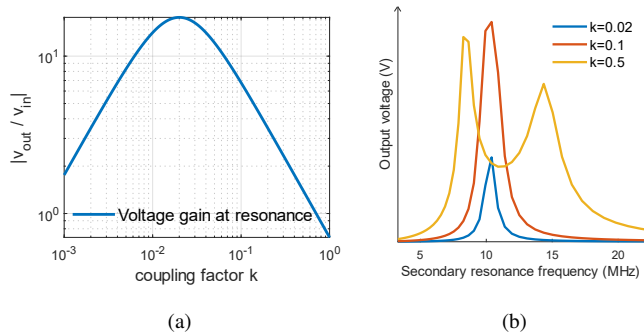
**FIGURE 2.** Schematic of an inductive link in a series-parallel configuration.

capacitors, multiple switched capacitor units are connected to higher bits from the SAR logic, for a more uniform layout and easy monitoring of the parasitic capacitance. It is deduced that the two clock signals are used both to drive the SAR logic and to control the switches of the variation sensor described in [10]. In addition, several authors have explored active compensation methods in recent research, including those discussed in [21]–[24], which involve adaptively tuning a capacitor bank to compensate for resonance variations.

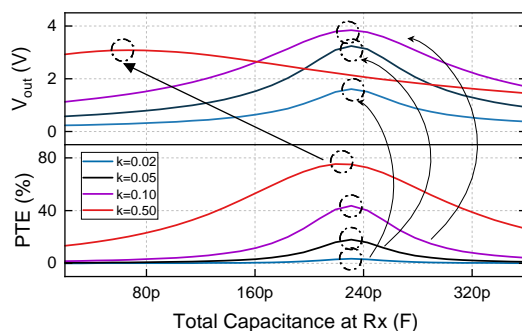
This paper presents a 13.56 MHz automatically tuned wireless power conversion chain for biomedical implants, as shown in Fig. 1. An enduring problem encountered by wirelessly powered IMDs, specifically concerning variations in resonance at the secondary, is effectively tackled through the designing of a counter-based automatic resonance tuning technique which demonstrates a compensation dynamic range of 6 control bits. The whole system is also capable of providing tolerance up to mismatches equivalent to 75 pF capacitance (in LC tank) variation while consuming only 154.7  $\mu$ W of power during resonance tuning. Furthermore, the performance of the tuning system has been validated with regard to its ability to handle variations in distance and angular misalignment. Section II of this paper investigates the properties of an inductive link and Section III provides an explanation of the design of each module and their related simulation results. Section IV presents the silicon verification through measurement results. Finally, Section V presents the conclusion.

## II. Properties of inductive links

The schematic of the simplified diagram of an inductive link is shown in Fig. 2. Coil design involves a critical coupling coefficient that determines the maximum voltage gain between resonators in the series-parallel topology. If this coupling coefficient exceeds a critical value, voltage gain decreases, and instability may occur due to energy transfer back to the primary coil. It should be noted that strong coupling is not guaranteed in real biomedical applications. Derivations of the voltage gain  $|v_{out}/v_{in}|$  have been studied in the frequency domain in [6] and the transfer function is



**FIGURE 3.** (a) Calculated gain at resonance with sweeping coupling factor; (b) qualitative simulated output voltage with sweeping coupling.



**FIGURE 4.** PTE, output voltage and its derivative with respect to the total tuning capacitance  $C_t$ .

expressed as

$$\frac{v_{out}}{v_{in}} = \left( \frac{(1/k)L(j\omega)}{1 - L(j\omega)} \right) \left( \frac{1}{j\omega\sqrt{L_1L_2}} \right) \left( \frac{R_L}{j\omega C_2 R_L + 1} \right) \quad (1)$$

where  $\omega$ ,  $L_{1,2}$ ,  $C_{1,2}$ ,  $k$ , and  $R_L$  are the operating frequency, primary and secondary inductors and capacitors, coupling coefficient, and load resistance. If the circuit with its feedback effect is modeled as a closed loop system [6], the loop transmission  $L(j\omega)$  is defined as

$$L(j\omega) = \frac{(j\omega)^2 k^2 L_1 L_2}{Z_1 Z_2} \quad (2)$$

The impedance of the primary and secondary resonators is simplified as

$$Z_{1,2} = \frac{(j\omega)^2 + j\omega \frac{\omega_c}{Q_{1,2}} + \omega_c^2}{j\omega/L_{1,2}} \quad (3)$$

where  $\omega_c$  is the resonance frequency and  $Q_{1,2}$  is the quality factor of the inductors.

Though the formula for the maximum PTE has been derived in [6] with matched load resistance, it is not exploited because of the fixed load from the rectifier in this system. The theoretical gain at resonance with respect to the coupling factor  $k$  is plotted in Fig. 3(a). As mentioned, critical coupling is defined as the coupling at which the gain is maximized and the corresponding coupling factor is denoted as  $k_c$ . With a coupling factor  $k < k_c$ , calculation and

**TABLE 1.** Denotation of signals in the auto-tuning system.

Denotation	Definition
$V_+, V_-$	AC signal coming from the inductive link.
$V_{rect}$	rectified voltage.
$V_{in+}, V_{in-}$	input voltages of the latched comparator used in the tuning control unit.
$V_{CMP+}$	output of the latched comparator, $V_{CMP+} = 1$ when $V_{in+} > V_{in-}$ .
$\Phi_1$ to $\Phi_3$	clock with same period but different duty cycles.
$SW(\bar{5}:0)$	control signals to the switched capacitors.
$C_{SW}(\bar{5}:0)$	six switched capacitors.
$\overline{RST}_{in}$	universal reset of the DFFs from external.
$C_{prev}$	storage capacitor of the rectified voltage.

simulation of a sweeping frequency demonstrate a unique peak while with  $k > k_c$ , a saddle shape is observed with a lower voltage gain at resonance, with simulations plotted in Fig. 3(b). Such separation of peak voltage gains is defined as the frequency splitting phenomenon, which has been utilized in some research for communication regardless of lower PTE [25]. Since the auto-tuning system in this paper should maximize PTE, the operating frequency is set close to the primary and secondary resonance frequency. To account for any mismatch between these frequencies, we model the deviation by sweeping the resonance capacitance  $C_2$  (or  $C_{RX}$ , depicted in Fig. 2) around its optimal value. In Fig. 4, we present the PTE, output voltage, and the derivative of the output voltage concerning the tuning capacitance to evaluate the system's performance under varying tuning conditions. The design in [10] utilizes the curve of the derivative of the output voltage with respect to the resonance capacitance, which is positive when the capacitance should be enlarged and vice versa. Regarding the monotonically increasing derivative curve for stronger coupling, either the  $k$  value is unrealistically large and such a case can be solved by limiting the tuning time, as proposed in [10]. A closer consideration is made of the peak of the PTE and the tuning capacitance at the locations where the derivative crosses zero. The PTE difference between the two peaks decreases as coupling becomes weak. Since no reference voltage is engaged and loose coupling is focused in this work, the output voltage is maximized as an approximation to maximizing the PTE.

### III. System Architecture

The flowchart of the auto-tuning algorithm that effectively maintains the rectifier voltage within a designated range, even when exposed to different types of external disturbances to the WPT link, and ensuring PTE is illustrated in the right box of Fig. 1. Moreover, Table 1 summarizes the denotations and Fig. 5 demonstrates the composition of the auto-tuning system. The secondary resonance frequency is adjusted by activating or deactivating the six switched capacitors.

An active rectifier is designed to convert AC power from an external wireless power source into DC power. The active rectifier is modified from [26] and features a self-biasing bulk to the cross-coupled PMOS transistors, as shown in Fig. 6. Additionally, the rectifier comprises two common-gate comparators, with two NMOS switches that function as active diodes. To address the delays associated with active diodes and mitigate issues such as multiple pulsing and reverse current, dynamic switched-offset biasing is employed in the implementation of comparators. This approach utilizes a push-pull structure and introduces auxiliary bias current to the predefined DC offset, thereby enhancing the slew rate and enabling instantaneous switching off of the comparators. This technique helps compensate for diode delays and ensures efficient and reliable operation of the system. Moreover, to provide the necessary power supply for the auto-tuning system, a 1.8 V low-dropout voltage regulator (LDO) is designed, as illustrated in Fig. 7(a). The LDO is composed of an error amplifier, a voltage reference generator, a PMOS pass transistor, a feedback loop, and a frequency compensation circuit to ensure stability. Furthermore, a power feedback control unit, as shown in Fig. 7(b), is designed to trigger automatic tuning in the event of coil misalignment, achieved through the generation of two control bits denoted as low and high delivered power (LDP and HDP).

The control unit is composed of a comparator, a three-bit down counter, a one-hot decoder, six duplicated processing units, and a clock recovery and divider module, as shown in Fig. 5. The start-up and termination of the control unit are regulated by the counter and an input signal  $\overline{BTN}$ , which is a pulse in imitation of a button press to start tuning coming from the implanted microcontroller. The above modules and their functionality are explained in further Sections.

#### A. Capacitor bank

Six switched capacitors are connected in parallel with the resonance capacitor, whose total capacitance is 30% of the ideal resonance capacitance  $C_{2,opt}$  at the secondary to compensate for a bidirectional 15% LC variation. To do so, and in order to achieve resonance at 13.56 MHz for an implant coil with an inductance of 0.6  $\mu$ H, a capacitor range of 69 pF is necessary. In this system, the overall capacitor coverage is designed to be 75 pF, which adequately meets this requirement. It is important to note that there exists a trade-off between tuning time and tuning accuracy, as well as the maximum output voltage achieved after tuning. In order to achieve a balance between these factors, a tuning resolution of 5 pF is set, allowing for a reasonable tuning time and energy consumption. Bidirectional tuning is achieved by inserting inverters before the switched capacitor at the indices of 5, 3 and 0, which is not shown in the diagram. A switched capacitor structure is utilized, as illustrated in Fig. 5 in the red rectangle.

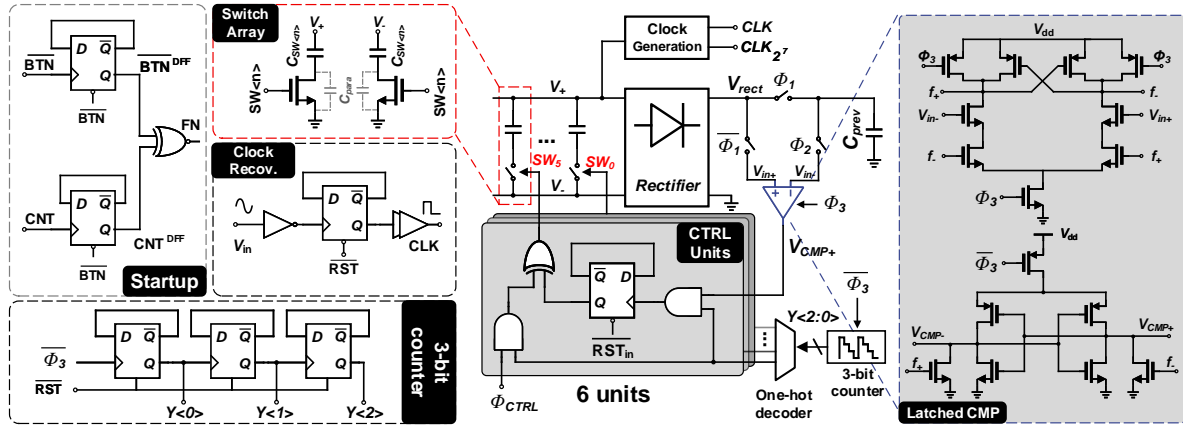


FIGURE 5. Block diagram of the proposed automatic resonance tuning system including the logic control units, switch array, and active rectifier.

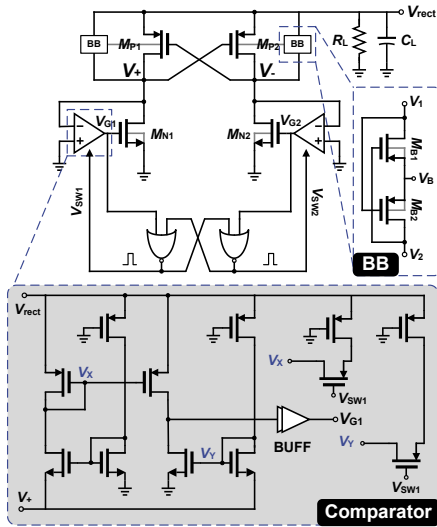
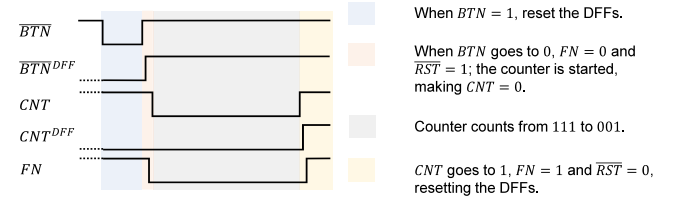


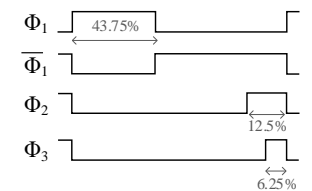
FIGURE 6. Schematic of the active rectifier and the common-gate comparator.



(a)

Y		Sel						
(2)	(1)	(0)	(5)	(4)	(3)	(2)	(1)	(0)
1	1	1	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0
...	...	...	...	...	...	...	...	...
0	1	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

(b)



(c)

FIGURE 8. (a) Startup waveform; (b) truth table of the one-hot decoder; and (c) clock signals  $\Phi_1$  to  $\Phi_3$ .

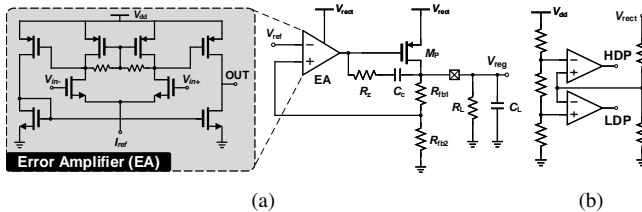
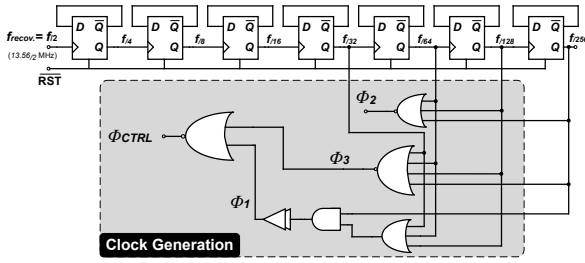


FIGURE 7. Schematic of the (a) 1.8 low-dropout (LDO) voltage regulator and (b) power feedback control.

### B. Start-up and termination

The circuit of the start-up and termination module is shown in Fig. 5 in the top left box with a finished signal ( $FN$ ). Recall that some DFFs are reset by  $RST$  and this signal is generated as  $RST = RST_{in} \cdot FN$ . The waveform of all signals involved in Fig. 8(a) demonstrates its functionality when the universal reset  $RST_{in}$  is high: (1) the button signal is turned ON via the implanted microcontroller and the DFFs

in this module is reset, making a high  $FN$  and in turn  $RST$ , resetting all DFFs in the clock recovery, clock divider and counter; (2) the button is released and  $BTN^{DFF}$  goes high,  $FN$  and  $RST$  are inverted and the counter started, making the  $CNT$  signal going low; (3) the counter counts from 111 to 010 with all six switched capacitors iterated; (4) the counter counts to 001, inverting  $CNT$ ,  $CNT^{DFF}$  and  $FN$ , which will reset the DFFs in other modules apart from the processing unit. The counter is disabled and  $CNT$  is kept high at termination, which leads to a high  $RST$  that resets the counter. The auto-tuning system is restarted solely at the arrival of the  $BTN$  pulse that enables the counter. The three-bit down counter and one-hot decoder activate the six processing units one by one and regulate the termination of tuning. The counter is implemented by three DFFs reset by  $RST$  in sequences with a three-bit output  $Y\langle 2:0 \rangle$ . These three bits are then decoded to six one-hot selection signals  $Sel\langle 5:0 \rangle$ , only one of which is high. The truth



**FIGURE 9.** Schematic of the clock generation unit using the recovered clock.

table of  $Y\langle 2 : 0 \rangle$  and  $Sel\langle 5 : 0 \rangle$  is shown in Fig. 8(b). For example,  $Sel\langle 4 \rangle$  is generated by  $Sel\langle 4 \rangle = Y\langle 2 \rangle \cdot Y\langle 1 \rangle \cdot \bar{Y}\langle 0 \rangle$ . The selection signals are connected with the processing unit with AND gates, guaranteeing that the control signal for a switched capacitor is only modified during the specific period. When the counter state is at 001 or 000, the signal  $CNT$  transits from zero to one from  $CNT = \bar{Y}\langle 2 \rangle \cdot \bar{Y}\langle 1 \rangle$ , which engages the termination of the auto-tuning system.

### C. Clock recovery and divider

A square wave is recovered from the AC signal through an inverter, a D flip-flop (DFF) and a buffer as shown in Fig. 5 in the clock recovery box. The clock divider implemented by a sequence of DFFs provides clocks with multiples of the recovered square wave and clock signals used in the control unit are generated by combining some of them, as shown in Fig. 9. The signal  $RST$  combines the universal reset  $RST_{in}$  with a termination signal and will be introduced in the next Section. Denoting the clock from the  $n$ th DFF (among 7 DFFs) of the clock recovery and divider sequence as  $CLK_{2^n}$ , where  $2^n$  indicates its period being  $2^n$  times the AC signal period,  $\Phi_1$  to  $\Phi_3$  are generated as

$$\begin{aligned} \Phi_1 &= (CLK_{2^{N-1}} + CLK_{2^{N-2}} + CLK_{2^{N-3}}) \cdot CLK_{2^N} \\ \Phi_2 &= \frac{CLK_{2^N} + CLK_{2^{N-1}} + CLK_{2^{N-2}}}{2} \\ \Phi_3 &= \frac{CLK_{2^N} + CLK_{2^{N-1}} + CLK_{2^{N-2}} + CLK_{2^{N-3}}}{4} \end{aligned}$$

where  $N = 8$ , each with a duty cycle of 43.75%, 12.5% and 6.25%, as shown in Fig. 8(c). Fluctuations when ANDing the clocks can be observed due to the delay of the DFF. For example,  $CLK_{2^N}$  goes low later than clocks with a smaller period going high, creating a short duration during which both signals are high. This does not have any negative impacts on the system's operation.

### D. Control unit

The control unit applies the following strategy. In each of the six periods, the control signal of a switched capacitor is inverted and the rectified voltage before and after this change are compared; if the new rectified voltage is higher, this change is recorded and kept by the processing unit, as illustrated in the flowchart. The clocked comparator is implemented as depicted in Fig. 5 in the blue box [27].

The working scheme of the control unit is explained with an example in Fig. 10 that includes comparator signals and connected tuning capacitances. Also, the first two periods of this transient simulation are split into Phases (1a) to (2d) and the variations in the signals are summarized in Fig. 10. Such operation is repeated until all six switched capacitors are iterated.

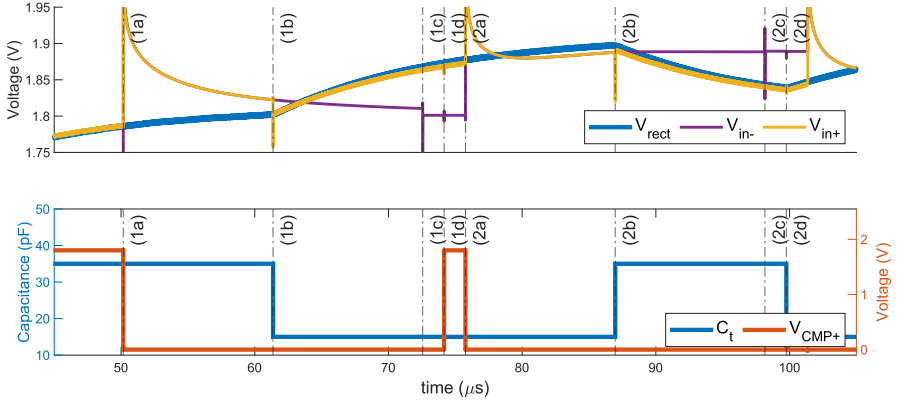
With an operating frequency of 13.56 MHz, the off-chip inductors and capacitors at the primary and secondary sides are set to  $L_1 = 1.2 \mu\text{H}$ ,  $C_1 = 115 \text{ pF}$ ,  $L_2 = 0.6 \mu\text{H}$  and  $C_{2,opt} = 195 \text{ pF}$  (in parallel with an on-chip 35 pF). The switched capacitors  $C_{SW}\langle 5 : 0 \rangle$  are 20 pF, 20 pF, 10 pF, 10 pF, 10 pF, 5 pF and an initial connected tuning capacitance is selected at 35 pF by inserting an inverter to  $SW\langle 5 \rangle$ ,  $SW\langle 3 \rangle$  and  $SW\langle 0 \rangle$ . Binary-weighted capacitors are avoided to reduce the step at each capacitance change. A buffer consisting of two inverters at the output of each processing unit eliminates the fluctuations and drives the large transistors of the switch capacitors. The number of DFFs in the clock chain is  $N = 8$ , leading to a waiting time of  $9.6 \mu\text{s}$  between inverting the switching and comparison. The period of the  $\Phi_1$  is  $18.8 \mu\text{s}$  and the time required for tuning is  $153.6 \mu\text{s}$ .

The control unit's power during tuning in simulation is  $9.2 \mu\text{W}$  and  $5.8 \mu\text{W}$  after tuning. The simulation results of the system performance at  $k = 0.1$  is summarized in Fig. 11 with an LC variation of  $\pm 15\%$  compensated. It should be noted that LC variation is modeled solely by capacitance variation. Fig. 12 demonstrates the transient simulation when the coupling factor  $k = 0.1$  and the resonance capacitance is 390 pF and 320 pF. Compared to the case without tuning ( $V_0$ ), the rectified voltage of the auto-tuning system is significantly enhanced and the change of connected tuning capacitance matches the deviation of  $C_2$  from its ideal value. The obtained control signal  $SW\langle 5 : 0 \rangle$  is in correspondence of  $C_2$ , for example,  $SW\langle 5 : 0 \rangle = 000000$  for  $C_2 = 390 \text{ pF}$ ,  $SW\langle 5 : 0 \rangle = 000100$  for  $C_2 = 380 \text{ pF}$  and  $SW\langle 5 : 0 \rangle = 111110$  for  $C_2 = 330 \text{ pF}$ . Comparable results on inductance variation are anticipated because the optimal resonance frequency within the tuning range is always achieved by adjusting tuning capacitors. Fig. 13 shows the simulated power consumption breakdown of the logic unit of the proposed system. The clock generation in the logic unit and rectifier in the system account for the majority of the power consumption. The overall power consumption of the logic unit and switch array is  $113.6 \mu\text{W}$ . The simulated end-to-end PTE with 0.1 coupling coefficient is 25.9%, delivering 6.8 mW to the load.

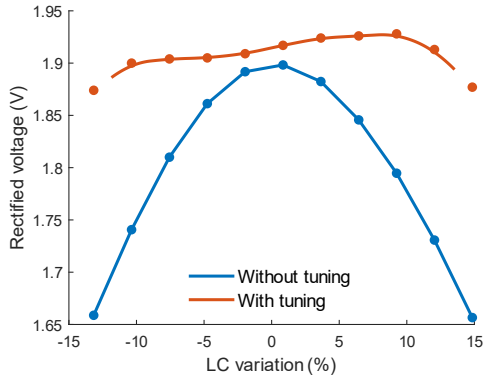
## IV. Measurement Results

The proposed automatic tuning system and wireless power conversion chain are designed and fabricated in a 180 nm standard CMOS technology. The system comprises a total area of  $0.339 \text{ mm}^2$ , with a core area of  $0.1 \text{ mm}^2$  (excluding pads). The floorplan of the control units and on-chip

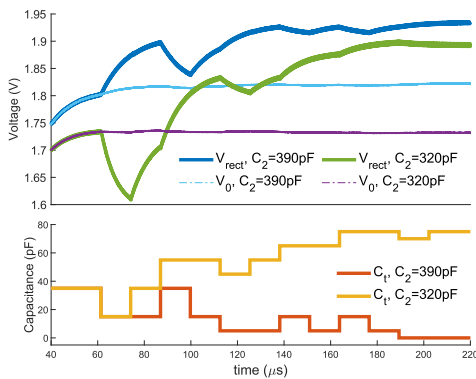
Phase	Variations in the control unit signals
(1a)	Auto-tuning is enabled and $\Phi_1 = 1$ ; the storage capacitor $C_{prev}$ is connected to rectified voltage $V_{rect}$ ; counter counts to 111 and the selection signal $Sel(5) = 1$ .
(1b)	$\Phi_1 = 0$ and the storage capacitor is disconnected; the rectified voltage is connected to the positive input of the comparator; the control signal $SW(5)$ is inverted and the connected tuning capacitance changes.
(1c)	$\Phi_2 = 1$ and the storage capacitor is connected to the negative input of the comparator.
(1d)	$\Phi_3 = 1$ and comparison is made; $V_{in+} > V_{in-}$ and $V_{CMP+}$ goes high and the output of the DFF in the 5th processing unit is inverted.
(2a)	Same as (1a) except that the counter counts to 110 and $SW(4) = 1$ .
(2b)	Same as (1b) except that $SW(4)$ is inverted.
(2c)	Same as (1c).
(2d)	Comparison is made and $V_{in+} < V_{in-}$ ; the output of the DFF in the 4th processing unit is not inverted and the connected tuning capacitance is recovered to the state at (2a).



**FIGURE 10.** Simulation of the rectified voltage  $V_{rect}$ , input voltages of the comparator  $V_{in-}$  and  $V_{in+}$ , total tuning capacitance  $C_t$  and output voltage of the comparator  $V_{CMP+}$  with  $C_2 = 390$  pF and  $k = 0.1$ .

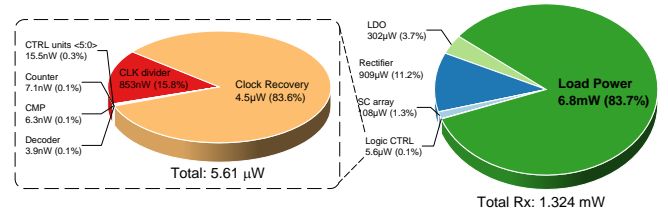


**FIGURE 11.** Simulation results of the rectified voltage without tuning and after auto-tuning at  $k = 0.1$ .

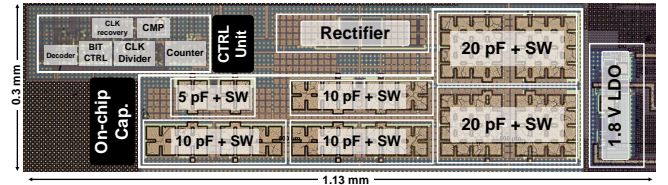


**FIGURE 12.** Transient simulation of the rectified voltage with tuning ( $V_{rect}$ ), rectified voltage without tuning ( $V_0$ ) and total added tuning capacitance  $C_t$  at  $k = 0.1$ .

capacitors can be seen in Fig. 14. Printed circuit board (PCBs) have been developed to validate the prototype design, encompassing both the inductive link and implanted unit, as illustrated in Fig. 15. Furthermore, an off-chip capacitor, with

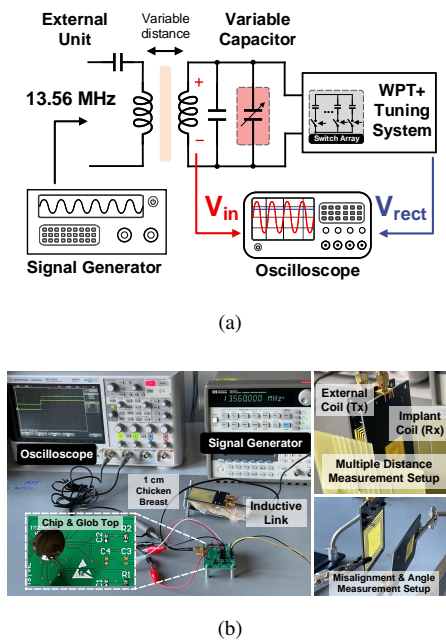


**FIGURE 13.** Simulation of power consumption breakdown of the proposed wireless power conversion chain and automatic resonance tuning system, delivering 6.8 mW to the load while the receiver circuit dissipates 1.324 mW (total Rx).

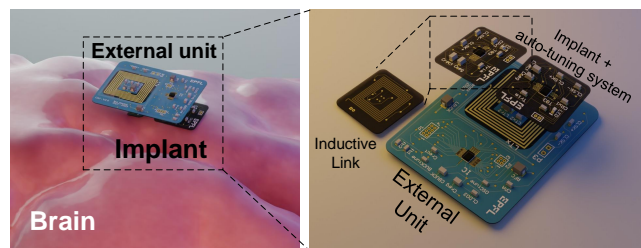


**FIGURE 14.** Die photograph of the proposed automatic tuning system fabricated in a standard 180 nm CMOS process with an area of 1.13 mm×0.3 mm.

a value of 40 nF is required for the output of the rectifier ( $C_{prev}$  in Fig. 5). Fig. 15(a) shows the connection of the system including the inductive link and the fabricated chip for measurements. Given the requirement for implantation of the Rx coil within a limited outer diameter (in the range of 10 mm), a trade-off arises between the coil's quality factor and the number of turns per layer (fill ratio), assuming a constant outer diameter. Consequently, it is crucial to optimize the design of the implant coil in order to fulfill these specific requirements. The inductive link comprises a Tx coil (1.2  $\mu$ H with a 43 mm outer diameter) and implant coil (600 nH with a 13.6 mm outer diameter) at Rx, separated by 5-20 mm in the air or 1 cm of chicken breast. To enhance the PTE, an additional coil resonator can be used at the external unit. For the purpose of brain implant applications, the outer dimension of the Rx



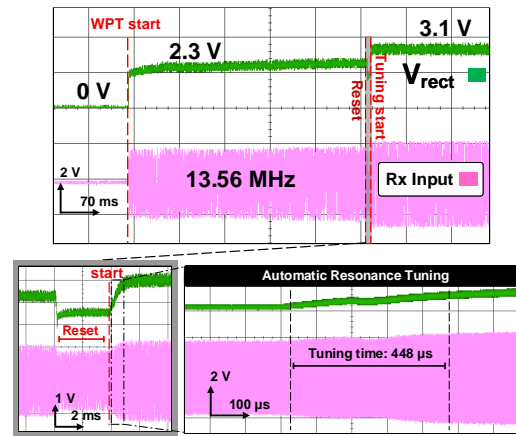
**FIGURE 15.** (a) Schematic and (b) photo of the experimental setup in air and 1 cm of chicken breast with external and implant coils along with the multiple distance and angular misalignment setups.



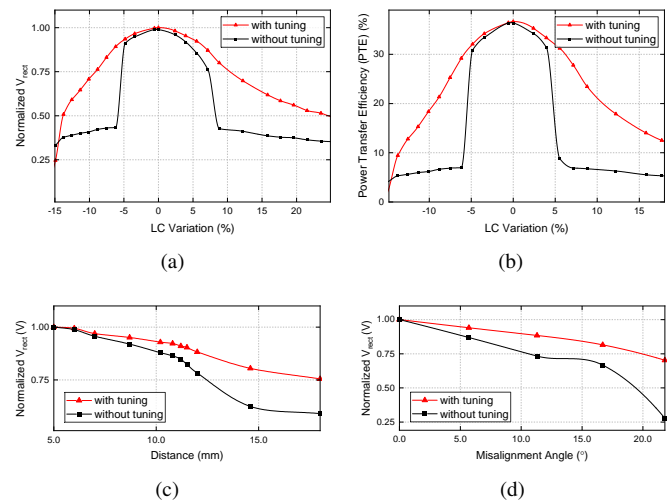
**FIGURE 16.** Conceptual implementation of the fabricated IC and the PCB prototypes.

coil is specified as 13.6 mm. Experimental characterization has been conducted utilizing transient voltage analysis and distance or angular misalignment sweep using the setup shown in Fig. 15(b). The implementation of the fabricated IC and the PCB prototypes and their conceptual view of its usage are shown in Fig. 16.

The rectified voltage, which is harvested and obtained, is measured by performing a transient analysis. To demonstrate this, different LC combinations with positive and negative variations in the resonance frequency are evaluated. The measured results of the transient received input sine voltage and the rectified voltage after tuning are shown in Fig. 17. The tuning time and the required time to have a stable rectified voltage depend on the parasitic capacitors and the value of the rectifier output capacitance. It should be noted that an internal overvoltage protection circuit has been integrated within the chip to safeguard its circuits against potential damage resulting from high received voltages. The tuning process is initiated by utilizing a pre-defined voltage



**FIGURE 17.** Measured results of transient received input sine voltage and the rectified voltage after starting WPT and resonance tuning.



**FIGURE 18.** Measurement results of (a) the normalized  $V_{rect}$  and (b) PTE without and with tuning in different LC tank variations, at no LC variation, and the rectified voltage versus (c) distance and (d) angular misalignment.

node (BTN that is intended to be controlled by an implanted microcontroller), and the rectified voltage ( $V_{rect}$ ) is captured. Subsequently, the system behavior is observed by enabling and disabling the tuning process using the reset button. Fig. 18(a),(b) shows the effect of the automatic tuning system on the received rectified voltage (normalized) and the PTE (4.8 mW power delivery in case of no LC variation) with the LC variation (mismatch the resonance capacitor with the ideal value), which can be observed by the slope in  $V_{rect}$  when tuning is achieved. The rectified voltage decreases significantly by approximately 7% from one extreme to the other in the absence of tuning, while this issue is enhanced by the tuning system. Also, it is observed that for a 7% variation, assuming a consistent load, the delivered power to the load are 1.07 mW and 3.69 mW without and with tuning, respectively, leading to a PTE increase from 9.1% to 30.2%. Additionally, following a -14.5% LC variation, the rectified voltage decreases and becomes insufficient for the



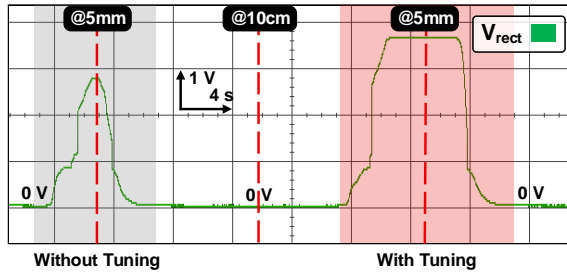


FIGURE 19. Measurement results of the transient rectified voltage with and without automatic tuning by Tx-Rx coil distance variation 0-10 cm.

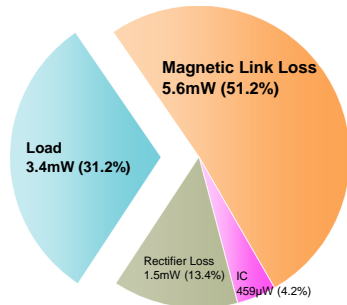


FIGURE 20. Measurement results of the power consumption breakdown.

wireless powering units. Hence, the auto-tuning system fails to operate, leading to a more drastic reduction in the rectified voltage compared to the version without tuning. Fig. 18(c) displays the relationship between the harvested voltage and distance with and without the tuning system. To measure the misalignment, a setup is configured to adjust angular misalignment at various distances. Fig. 18(d) illustrates the angular misalignment tolerance of up to 20 degrees at a distance of 10 mm in the automatically tuned system. The coils are symmetrical, and there is no sensitivity for the Z-axis misalignment and the sensitivity for the X- and Y-axis misalignment is similar.

The transient response of the rectified voltage under distance variation, both with and without tuning, is illustrated in Fig. 19. In this experimental setup, the Tx coil remains in a fixed position while the Rx coil is gradually displaced from a considerable distance of 10 cm to a much closer proximity of 5 mm. Subsequently, the tuning system is activated, and the entire procedure is replicated under this new condition. To ensure consistent and uniform motion in both scenarios, a twisting screw jack is employed, which maintains a constant speed throughout the displacement process. The tuning control unit consumes  $154.7 \mu\text{W}$  including the switch array and clock generation units and the overall system delivers 3-10 mW power with the maximum end to end PTE of 51% (at  $k=0.1$ ) and 31.2% (at  $k=0.05$ ). The measured power consumption breakdown (at  $k=0.05$ ) is shown in Fig. 20. The measured S-parameters of the coils, both without and with tuning, are shown in Fig. 21(a), obtained using a network analyzer. Furthermore, Fig. 21(b) and (c) show

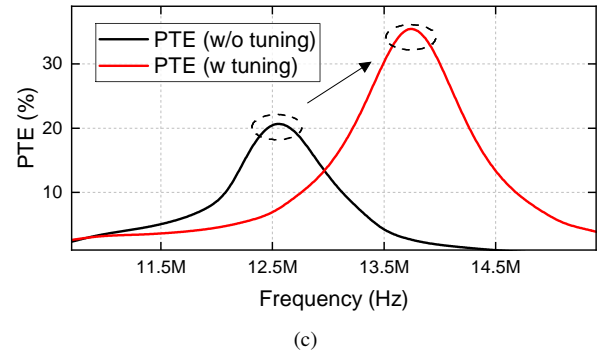
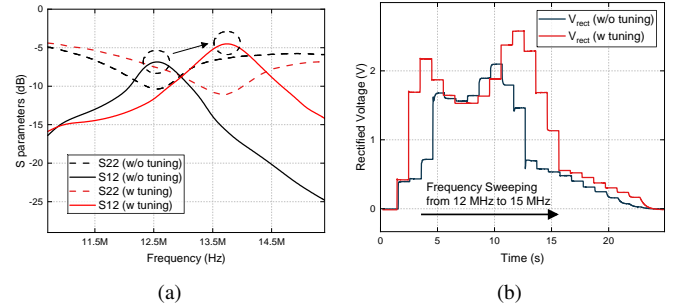


FIGURE 21. Measurement results of the coils connected to a network analyzer (a) s-parameter with and without tuning, (b) the rectified voltage during the frequency sweeping, and (c) power transfer efficiency.

the measured rectified voltage and PTE captured during frequency sweeping by the network analyzer.

Table 2 summarises the overall automatic resonance tuning system and its wireless power conversion unit performance. The key performances of the proposed auto-tuning system are compared to the state-of-the-art tuning systems and compensation techniques in Table 3, including their wireless power conversion performance along with the tuning method and resolution. The automatic tuning systems are categorized based on the tuning method (SAR and monotonic sweeping) and the detection target (rectified voltage/current or swing amplitude). The proposed wireless power conversion chain and automatic tuning system present an efficient on-chip solution in terms of both power and time for wireless powering and integrated compensating for wide  $\pm 15\%$  LC tank variations in biomedical implants.

## V. Conclusion

This paper proposes a power conversion chain with an integrated automatic resonance tuning system for wirelessly powered biomedical implants to deliver wireless power while maximizing power transfer efficiency under different link variations. The wireless power conversion chain incorporates an active rectifier and a low-dropout voltage regulator and switched array capacitors to optimize power delivery by adjusting the resonant capacitance and maximizing the delivered power to the load. The implemented system demonstrates feasibility with a size of  $0.339 \text{ mm}^2$ . Measurement results show tolerance for mismatches up to

**TABLE 2. Performance summary**

CMOS Technology		TSMC 180 nm
Chip Area		0.339 mm <sup>2</sup>
<b>Wireless Power Transmission 1 External + 1 Implant</b>		
Coil Distance		5-20 mm
Inductive Link: L <sub>Tx</sub> — L <sub>Rx</sub>		1.2 μH — 0.6 μH
Resonance Capacitor C <sub>Tx</sub> —C <sub>Rx</sub>		115 pF — 230 pF
<b>Wireless Power Conversion Unit</b>		
Operation Frequency		13.56 MHz
Rectifier	Max. VCR — Max. PCE	90 % — 80.1 %
	Load Cap.	40 nF
LDO 1.8 V	Output Voltage	1.8 V
	Power Dissipation	302 μW
<b>Automatic Resonance Tuning System</b>		
Total On-Chip Cap.		75 pF
Resolution		5 pF
Number of Tuning Bits		6 switches
Tuning Method		Monotonic Sweep
Tuning Range		±15%
Power Consumption		154.7 μW
Operation Frequency		53 kHz

±15% in LC tank variation, with low power consumption (154.7 μW) during resonance tuning. The PTE is enhanced depending on the LC variation and load power. For instance, it elevates power delivery from 0.52 mW to 2.34 mW, leading to a PTE increase from 9.1% to 30.2% in cases of high LC variation. The power conversion chain delivers an optimized rectified voltage and maintains a regulated voltage of 1.8 V, confirming the practicality and effectiveness of the proposed system for enhancing IMD performance.

## REFERENCES

- [1] M. J. Karimi, A. Schmid, and C. Dehollain, "Wireless Power and Data Transmission for Implanted Devices via Inductive Links: A Systematic Review," *IEEE Sensors Journal*, vol. 21, no. 6, pp. 7145–7161, 2021.
- [2] G. Namgoong, W. Park, and F. Bien, "A 13.56 MHz Wireless Power Transfer System With Fully Integrated PLL-Based Frequency-Regulated Reconfigurable Duty Control for Implantable Medical Devices," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 16, no. 6, pp. 1116–1128, 2022.
- [3] C. Huang, T. Kawajiri, and H. Ishikuro, "A 13.56-MHz Wireless Power Transfer System With Enhanced Load-Transient Response and Efficiency by Fully Integrated Wireless Constant-Idle-Time Control for Biomedical Implants," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp. 538–551, 2018.
- [4] M. Kim, H.-S. Lee, J. Ahn, and H.-M. Lee, "A 13.56-MHz Wireless Power and Data Transfer System With Current-Modulated Energy-Reuse Back Telemetry and Energy-Adaptive Voltage Regulation," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 2, pp. 400–410, 2023.
- [5] Y. Park, S.-T. Koh, J. Lee, H. Kim, J. Choi, S. Ha, C. Kim, and M. Je, "A Wireless Power and Data Transfer IC for Neural Prostheses Using a Single Inductive Link With Frequency-Splitting Characteristic," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 6, pp. 1306–1319, 2021.
- [6] M. W. Baker and R. Sarpeshkar, "Feedback Analysis and Design of RF Power Links for Low-Power Bionic Systems," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, no. 1, pp. 28–38, 2007.
- [7] R.-F. Xue, K.-W. Cheng, and M. Je, "High-Efficiency Wireless Power Transfer for Biomedical Implants by Optimal Resonant Load Transformation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 4, pp. 867–874, 2013.
- [8] M. J. Karimi, C. Dehollain, and A. Schmid, "Power Feedback Control Unit for Closed-Loop Wirelessly Powered Biomedical Implants," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 5, pp. 1674–1678, 2023.
- [9] H. Lyu and A. Babakhani, "A 13.56-MHz -25-dBm-Sensitivity Inductive Power Receiver System-on-a-Chip With a Self-Adaptive Successive Approximation Resonance Compensation Front-End for Ultra-Low-Power Medical Implants," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 1, pp. 80–90, 2021.
- [10] P. Gosselin, R. Puddu, A. Carreira, M. Ghanad, M. Barbaro, and C. Dehollain, "A CMOS automatic tuning system to maximize remote powering efficiency," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017, pp. 1–4.
- [11] H. Xu, U. Bihl, J. Becker, and M. Ortmanns, "A multi-channel neural stimulator with resonance compensated inductive receiver and closed-loop smart power management," in *2013 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2013, pp. 638–641.
- [12] H.-M. Lee and M. Ghovanloo, "A Power-Efficient Wireless Capacitor Charging System Through an Inductive Link," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 10, pp. 707–711, 2013.
- [13] H.-M. Lee, K. Y. Kwon, W. Li, and M. Ghovanloo, "A Power-Efficient Switched-Capacitor Stimulating System for Electrical/Optical Deep Brain Stimulation," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 1, pp. 360–374, 2015.
- [14] B. Lee, M. Kiani, and M. Ghovanloo, "A Triple-Loop Inductive Power Transmission System for Biomedical Applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, no. 1, pp. 138–148, 2016.
- [15] D. Ye, Y. Wang, Y. Xiang, L. Lyu, H. Min, and C.-J. R. Shi, "A Wireless Power and Data Transfer Receiver Achieving 75.4% Effective Power Conversion Efficiency and Supporting 0.1% Modulation Depth for ASK Demodulation," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 5, pp. 1386–1400, 2020.
- [16] V. J. Brusamarello, Y. B. Blauth, R. de Azambuja, I. Muller, and F. R. de Sousa, "Power Transfer With an Inductive Link and Wireless Tuning," *IEEE Transactions on Instrumentation and Measurement*, vol. 62, no. 5, pp. 924–931, 2013.
- [17] Y. Lim, H. Tang, S. Lim, and J. Park, "An Adaptive Impedance-Matching Network Based on a Novel Capacitor Matrix for Wireless Power Transfer," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4403–4413, 2014.
- [18] R. W. Porto, V. J. Brusamarello, L. A. Pereira, and F. R. de Sousa, "Fine Tuning of an Inductive Link Through a Voltage-Controlled Capacitance," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 4115–4124, 2017.
- [19] H. Kennedy, R. Bodnar, T. Lee, and W. Redman-White, "A Self-Tuning Resonant-Inductive-Link Transmit Driver Using Quadrature Symmetric Delay Trimmable Phase-Switched Fractional Capacitance," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 6, pp. 1694–1706, 2018.
- [20] S. Lee, J. Yoo, H. Kim, and H.-J. Yoo, "A dynamic real-time capacitor compensated inductive coupling transceiver for wearable body sensor network," in *2009 Symposium on VLSI Circuits*, 2009, pp. 42–43.
- [21] S. O'Driscoll, A. S. Y. Poon, and T. H. Meng, "A mm-sized implantable power receiver with adaptive link compensation," in *2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 2009, pp. 294–295, 295a.
- [22] M. Stoopman, S. Keyrouz, H. J. Visser, K. Philips, and W. A. Serdijn, "Co-Design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 3, pp. 622–634, 2014.
- [23] Y. An, X. Li, X. Feng, H. Xu, and Y. Zhuang, "High Sensitivity RF Energy Harvesting System with Self-calibrate Network," in *2023*

**TABLE 3. Comparison of automatic resonance tuning systems in the literature**

	ISCAS' 13 [11]	TBCAS' 16 [14]	ISCAS' 17 [10]	JSSC' 20 [15]	TBCAS' 21 [9]	This Work
CMOS Tech. ( $\mu\text{m}$ )	0.35	0.35	0.180	0.065	0.18	<b>0.18</b>
Power frequency (MHz)	13.56	13.56	13.56	13.56	13.56	<b>13.56</b>
Silicon Measurement	No	Yes	No	Yes	Yes	<b>Yes</b>
Tuning Method	Monotonic sweeping	Monotonic sweeping	SAR	Monotonic sweeping	SAR	<b>Monotonic sweeping</b>
Tuning Resolution	0.51 pF	0.5 pF	0.48 pF	2 pF	0.38 pF	<b>5 pF</b>
# of Tuning bits	3-bit	on-chip: 5-bit 0-16 pF off-chip: 5-bit 15-480 pF	4-bit	6 control bits, 0-128 pF	6 control bits, 0-24 pF	<b>6 control bits, 0-75 pF</b>
Detection Target	Rectified Current	Swing Amplitude	Rectified voltage	Rectified Current	Swing Amplitude	<b>Rectified voltage</b>
Operation frequency		26.4 kHz	26.5 kHz	100 kHz	5 kHz	<b>39 kHz</b>
Rx coil inductance		0.6 $\mu\text{H}$	4.59 $\mu\text{H}$	7.45 $\mu\text{H}$	6.36 $\mu\text{H}$	<b>0.6 <math>\mu\text{H}</math></b>
Outer diameter	2.92 $\mu\text{H}$	34 mm		22 mm	12.1 mm	<b>13.6 mm</b>
LC Variation Tolerance	-	6.9%	$\pm 11\%$ (overall 22%)	128 pF	24 pF	<b><math>\pm 15\%</math> (overall 30%)</b>
Max. $\Delta\text{C}$ coverage		16 pF	7.2 pF			<b>75 pF</b>
Tx-Rx Distance (mm)	-	20 mm	-	-	20 mm	<b>5-20 mm</b>
Rx Power		Tuning: 224 $\mu\text{W}$			Total Rx: 64.6* $\mu\text{W}$	<b>Tuning: 154.7 <math>\mu\text{W}</math></b>
Consumption (mW)		Total: 7.84* mW				<b>Total Rx: 1.95 mW</b>
Rx Efficiency (%)	-	80.3*	-	-	46.4	<b>64</b>
Delivered Power (mW)	-	32	0.85	10	0.03	<b>3-10</b>
Silicon Area ( $\text{mm}^2$ )	-	2.54	0.126	-	0.17*	<b>0.339</b>
Rectifier Type & PCE	-	Active PCE: 76.2%	Passive	Active PCE: 75.4%	Passive	<b>Active PCE: 80.1%</b>

\*: Calculated value

- IEEE/MTT-S International Microwave Symposium - IMS 2023*, 2023, pp. 875–878.
- [24] S.-H. Lee, Y.-W. Jeong, S.-J. Park, and S.-U. Shin, "A Rectifier-Reusing Bias-Flip Energy Harvesting Interface Circuit With Adaptively Reconfigurable SC Converter for Wind-Driven Triboelectric Nanogenerator," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 8, pp. 8022–8031, 2023.
- [25] J. Pan, A. A. Abidi, W. Jiang, and D. Marković, "Simultaneous Transmission of Up To 94-mW Self-Regulated Wireless Power and Up To 5-Mb/s Reverse Data Over a Single Pair of Coils," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 4, pp. 1003–1016, 2019.
- [26] Y. Lu and W.-H. Ki, "A 13.56 MHz CMOS Active Rectifier With Switched-Offset and Compensated Biasing for Biomedical Wireless Power Transfer Systems," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, no. 3, pp. 334–344, 2014.
- [27] M. Abbas, Y. Furukawa, S. Komatsu, J. Y. Takahiro, and K. Asada, "Clocked comparator for high-speed applications in 65nm technology," in *2010 IEEE Asian Solid-State Circuits Conference*, 2010, pp. 1–4.



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