SPAD Developed in 55 nm Bipolar-CMOS-DMOS Technology Achieving Near 90% Peak PDP

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***Abstract*—We present a single-photon avalanche diode (SPAD) developed in 55 nm bipolar-CMOS-DMOS (BCD) technology, which achieves high photon detection probability (PDP) while its breakdown voltage is lower than 20 V. To enhance the PDP performance, the SPAD junction is optimized with lightly-doped-drain and high-voltage-well layers which are provided in the BCD process. In addition, the dielectric layers over the SPAD are properly etched to reduce multilayer reflections so that the photon collection efficiency can be maximized. The SPAD achieves a peak PDP of 89.4% at 450 nm wavelength with the excess bias voltage of 7 V, while its breakdown voltage is 16.1 V. At the same bias condition, the device shows a dark count rate (DCR) of 38.2 cps/μm^2. It also achieves a timing jitter of 55 ps at 940 nm with the 7 V excess bias. This new high-performance SPAD implemented in such an advanced node BCD technology operating at a low breakdown voltage is expected to have a major impact on several single-photon applications, especially biomedical sensing and imaging.**

***Index Terms*—Avalanche photodiode (APD), bipolar-CMOS-DMOS (BCD) technology, detector, electronic photonic integration, fluorescence correlation spectroscopy (FCS), fluorescence lifetime imaging microscopy (FLIM), frontside illumination (FSI), Geiger-mode avalanche photodiode (G-APD), high-volume manufacturing, integrated optics device, integration of photonics in standard CMOS technology, optical sensing, optical sensor, photodetector, photodiode, photomultiplier, photon counting, photon timing, semiconductor, sensor, silicon, single-photon avalanche diode (SPAD), single-photon counting, single-photon imaging, standard CMOS technology.**

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I. Introduction

SINGLE-PHOTON avalanche diodes (SPADs) are devices in high demand for various applications, especially in biomedical practices [1], [2]. They could replace photomultiplier tubes (PMTs) thanks to their compactness and high sensitivity in tomography applications such as near-infrared optical tomography (NIROT) [3] and time-of-flight positron emission tomography (ToF-PET) [4]. They also play a key role in fluorescence-lifetime imaging microscopy (FLIM) [5], fluorescence correlation spectroscopy (FCS) [6], and Raman spectroscopy [7]–[11].

SPADs fabricated in CMOS technology are of great interest due to such advantages as low-cost fabrication, mass production, and monolithic integration capability with circuitry. Furthermore, with the technology scaling down, the advantages of CMOS-SPADs are becoming more pronounced in terms of pixel resolution, footprint, and functionality. Many attempts have therefore been made to develop SPADs based on advanced CMOS technologies [12]–[13]. As technology nodes scale, however, the doping concentrations of implants typically increase, which presents a challenge for the development of CMOS-SPADs as it narrows the width of the depletion region, resulting in a higher dark count rate (DCR) and lower photon detection probability (PDP) [13], [14].

To address this problem, Gramuglia *et al.* [15] and Keshavarzian *et al.* [16] reported a SPAD based on 55 nm bipolar-CMOS-DMOS (BCD) technology. The BCD technology provides deeper and/or lower-doped layers compared to CMOS technology, and this facilitates the implementation of SPADs with very low DCR and high PDP at higher excess bias voltages (V_E). Also, the BCD technology makes high-voltage transistors available to designers, thus enabling pixels that allow for a high excess bias voltage [16]. One downside of the BCD-SPAD is the relatively high breakdown voltage (V_B), typically over 30 V, which results in higher power consumption and limits its applicability range.

Another approach is to use backside-illuminated (BSI) CMOS image sensor (CIS) technology with 3D stacking. While the recent reports by Shimada *et al.* [17] and Morimoto *et al.* [18] demonstrated excellent SPAD performance based on 90 nm BSI CIS processes, the BSI 3D stacking approach may not be appropriate for cost-effective applications. Furthermore, until now, both of these approaches have been commonly unavailable from a foundry.

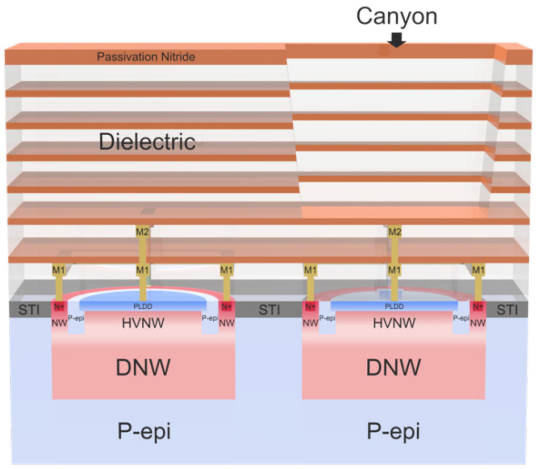

Fig. 1. Cross-sections of the BCD-SPADs.

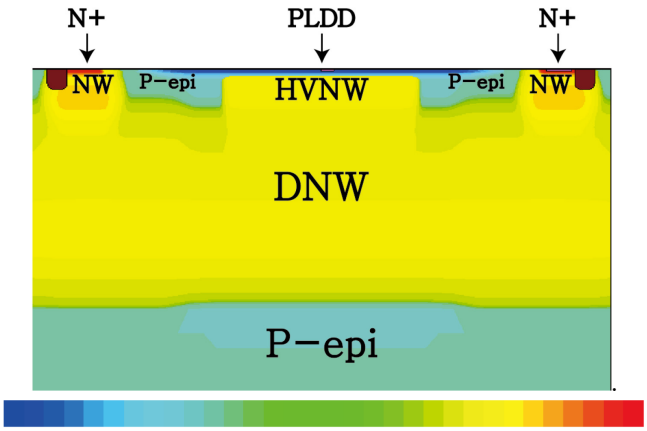

Fig. 2. Doping-concentration profile of the BCD-SPADs.

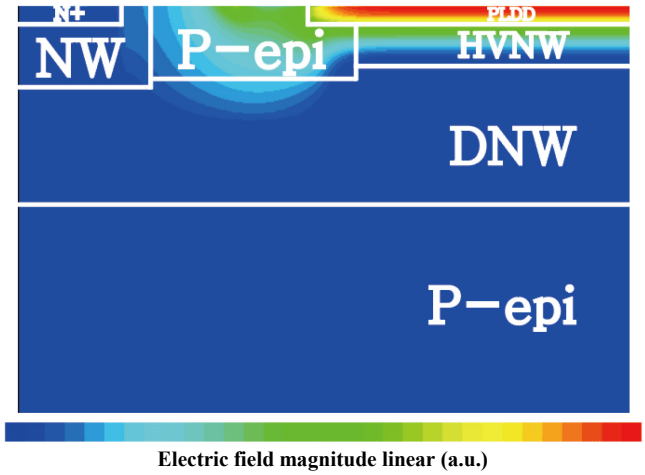

Fig. 3. E-field profile of the BCD-SPAD obtained with TCAD simulation.

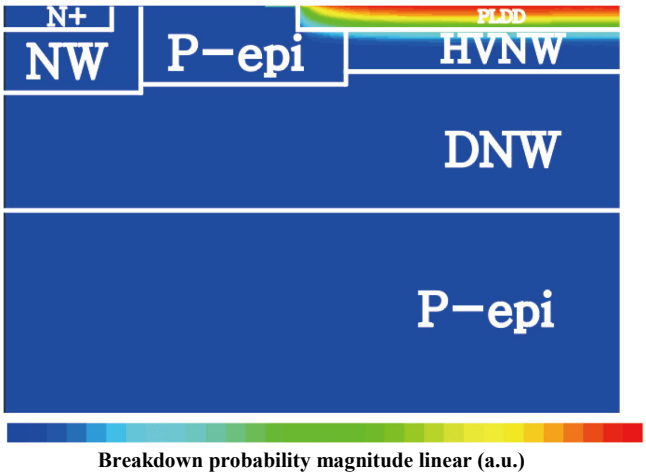

Fig. 4. The breakdown probability profile of the BCD-SPAD obtained with TCAD simulation.

In this paper, we present a SPAD fabricated in 55 nm BCD technology. In order to achieve high performance while maintaining the V_B less than 20 V, the junction is formed with P-type lightly-doped-drain (PLDD) and high-voltage N-well (HVNW) layers. In addition, the dielectric layers above the SPAD are properly etched away to reduce the multilayer reflection. The resulting SPAD achieves outstanding performance in terms of PDP, DCR, and timing jitter with a low breakdown voltage of 16.1 V.

II. Device Structure and Simulation

A. Device Structure

Fig. 1 shows cross-sections of two SPAD configurations Both SPADs have the identical device structure, where PLDD and HVNW layers form a 9 μm diameter PN junction and a total diameter of 14.4 μm as shown in Fig. 2. Both layers are standard in this technology, and the merits of using such layers are: (i) the PLDD generates less implantation-induced defects, enabling low-noise SPAD operation, and (ii) the HVNW provides a proper depletion region with the PLDD layer, which is wide enough to prevent band-to-band tunneling but, at the same time, not so wide as to significantly increase the breakdown voltage. To prevent premature edge breakdown, the SPADs are designed in a round shape and a P-epi guard ring with a width of 2 μm is implemented at the edge of the junction. A lightly-doped deep N-well (DNW) is used for the cathode connection, and it also makes the absorption region larger and consequently increases the PDP. To maximize the SPAD detection efficiency further, a few of the SPAD's dielectric layers above the multiplication and guard-ring regions are etched away, thus forming a *canyon*. We implemented two SPADs with and without the canyon. By comparing their performance, the effect of the canyon can be clearly demonstrated.

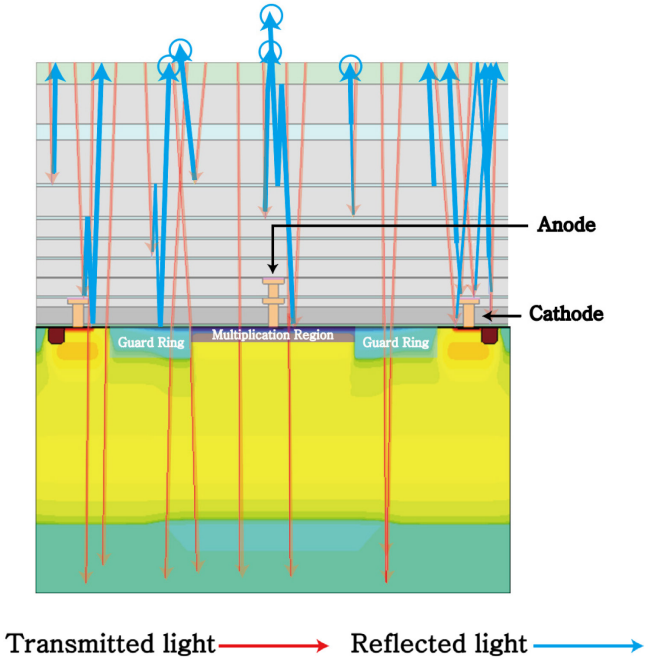

Fig. 5. Simplified raytracing result of the BCD-SPAD without the canyon obtained with TCAD simulation.

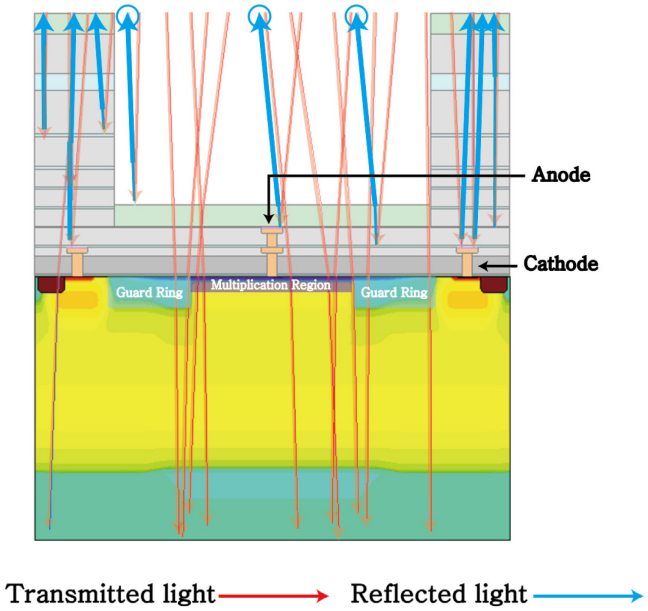

Fig. 6. Simplified raytracing result of the BCD-SPAD with the canyon obtained with TCAD simulation.

B. TCAD Simulation

In order to check the SPADs' E-field profile, TCAD simulation using Okuto's avalanche breakdown model was performed when the V_B and V_E were 16 V and 7 V, respectively [19]. As can be seen in Fig. 3, the E-field strength at the edge of the junction is reduced by the P-epi guard ring.

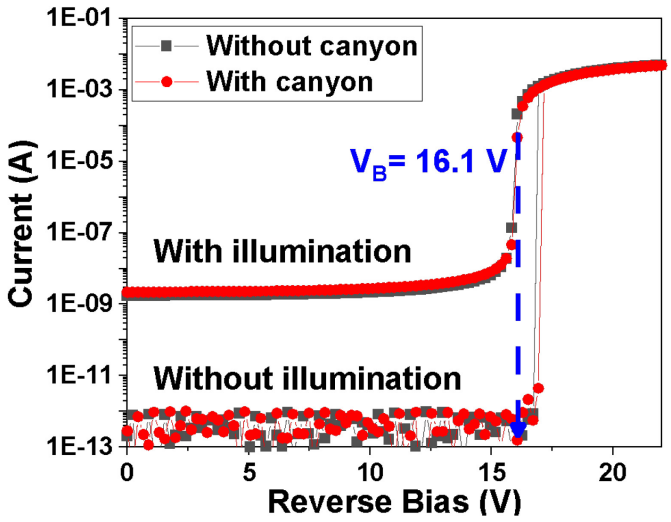

Fig. 7. I-V characteristics of the BCD-SPADs under dark and illumination conditions.

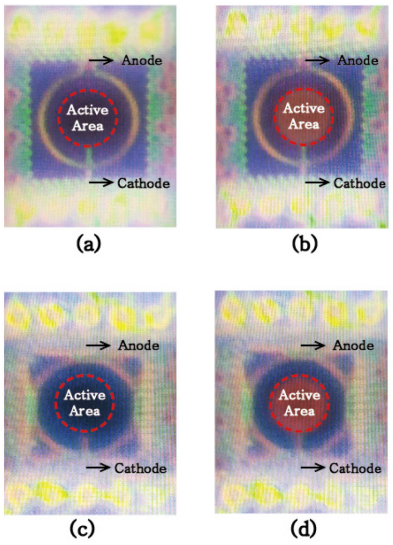

Fig. 8. Results of light emission tests of BCD-SPADs: (a) SPAD without the canyon before V_B, (b) SPAD without the canyon at V_E = 3 V, (c) SPAD with the canyon before V_B, (d) SPAD with the canyon at V_E = 3 V.

Therefore, we are able to avoid the premature edge breakdown phenomenon and form a high and uniform E-field at the planar PLDD/HVNW junction. In addition, the simulation to check the breakdown probability of the device was conducted using the McIntyre model as shown in Fig. 4 [20]. With the shallow junction, it is expected that the proposed devices achieve high PDP at 400~500 nm which corresponds to about 0.1 to 1 μm penetration depth of photons inside silicon. Finally, the effects of the canyon etch were investigated using ray-tracing simulations. In these simulations, the transmitted and reflected light is represented by the reddish and bluish arrows, respectively. The several dielectric layers on top of the non-

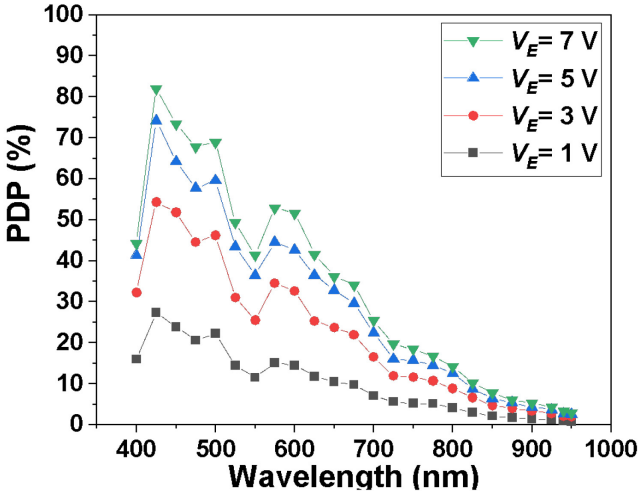

Fig. 9. PDP of the BCD-SPAD without canyon as a function of the wavelength at four different excess bias voltages.

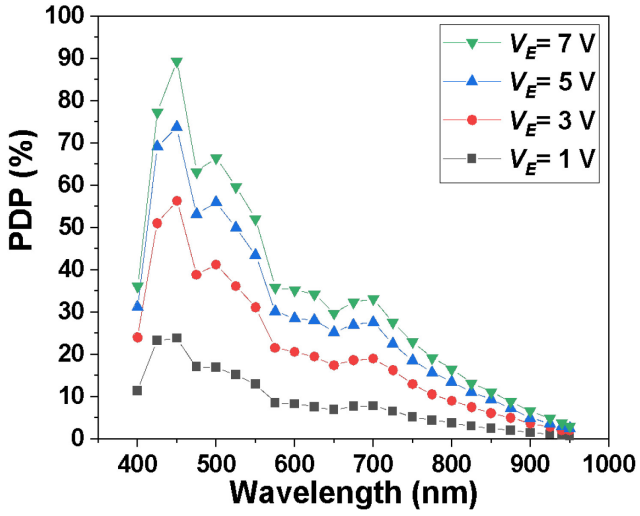

Fig. 10. PDP of the BCD-SPAD with canyon as a function of the wavelength at four different excess bias voltages.

canyon-etched SPAD result in many reflections as shown in Fig. 5. On the other hand, the light reflections are reduced in the SPAD with the canyon etch as can be seen in Fig. 6. The simulation results indicate that more photons reach the active region with the canyon etch, thereby leading to a higher PDP.

III. Experiment Results

A. I-V Characteristics

Fig. 7 shows the I-V characteristics of the fabricated BCD-SPADs with and without illumination measured using a semiconductor device analyzer at room temperature. As both SPADs are based on the same front-end-of-line (FEOL), they

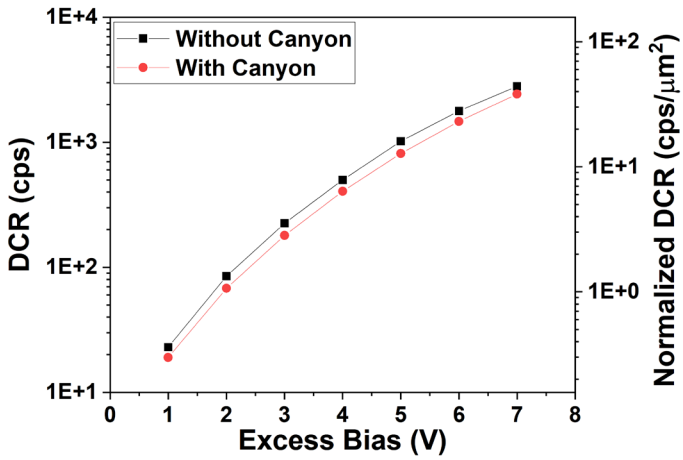

Fig. 11. DCR of the BCD-SPADs as a function of excess bias.

show similar results, small dark currents and high avalanche multiplication. Thanks to the high doping concentration of the PLDD, both SPADs have a low V_B of about 16.1 V, matching well with our expectations from the TCAD simulation. In addition, the dark currents of both SPADs increase at a higher voltage than the V_B under illumination, which indicates the number of dark carriers is relatively low [4].

B. Light Emission Test

Light emission tests of both SPADs are conducted to confirm the suppression of premature edge breakdown as shown in Fig. 8. The light-emitting area indicates the avalanche multiplication region when a higher excess bias than its V_B is applied. Therefore, the test results clearly demonstrate that a high E-field, over the critical E-field of silicon, is uniformly formed in the planar junction of both SPADs. Moreover, as the edge of the junction is not brighter than the center, the devices don't exhibit any premature edge breakdown, which was expected from TCAD simulation results shown in Figs. 3 and 4.

C. Photon Detection Probability

The PDP measurements were performed from 400 nm to 950 nm in 25 nm steps for the two SPADs at V_E = 1, 3, 5, and 7 V as displayed in Figs. 9 and 10, respectively. The tests were based on the continuous light technique at room temperature [21]. In the setup for these measurements, coherent and uniform light was illuminated to the SPAD and a reference photodiode by using an integrating sphere and a monochromator. The optical intensity of the reference photodiode was then measured for calculating the number of photons impinging on the SPAD. The SPAD was quenched with an external passive quenching resistor of 100 kΩ and the outputs were monitored by the oscilloscope. The dead time was about 2.5 μs, with which it was checked that the SPADs do not suffer from any afterpulsing.

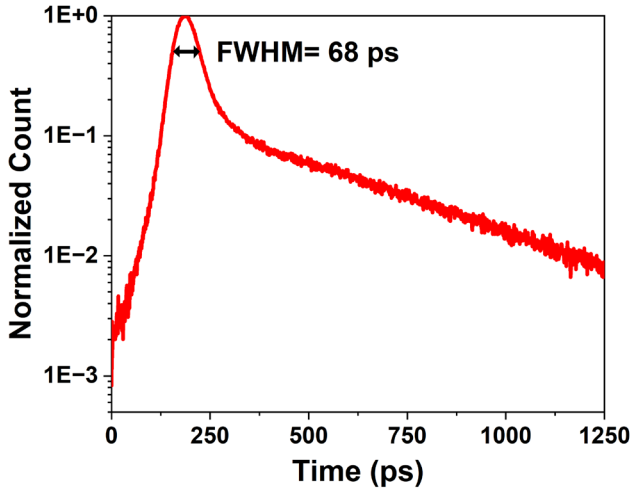

Fig. 12. Timing jitter of the BCD-SPAD without canyon.

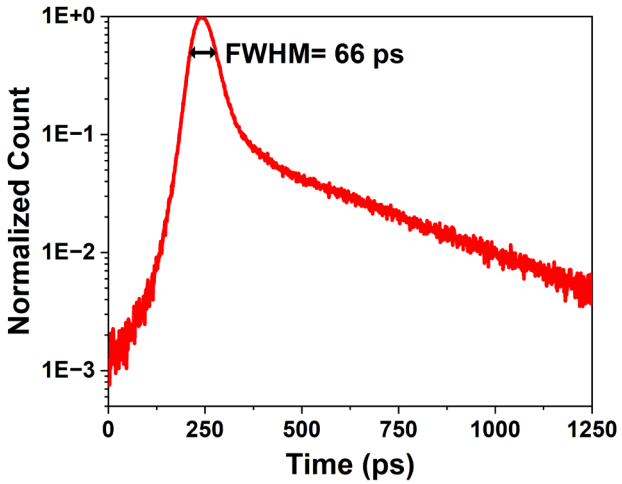

Fig. 13. Timing jitter of the BCD-SPAD with canyon.

As both SPADs are based on a shallow junction, they have a peak PDP at around 450 nm. Moreover, the presence of fewer dielectric layers allows more photons to reach the silicon with fewer reflections, as expected with the simulations in Fig. 5 and Fig. 6, and therefore near 90% peak PDP is achieved with canyon etching when V_E is 7 V, while the default structure shows about 82% peak PDP at the same bias condition.

D. Dark Count Rate

DCR is comprised of primary and secondary pulses. Thermally generated carriers and tunneling are dominant components in primary pulses, while the secondary pulses, known as afterpulses, are avalanches caused by the release of trapped carriers [22]. That is to say, the DCR of a SPAD is mainly affected by the FEOL and should not be affected by the canyon implementation.

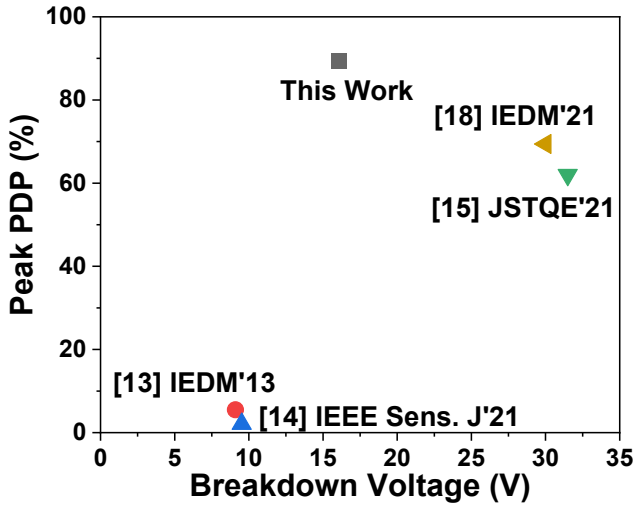

Fig. 14. Peak PDP vs V_B comparisons of SPADs fabricated in 90 nm or more advanced processes.

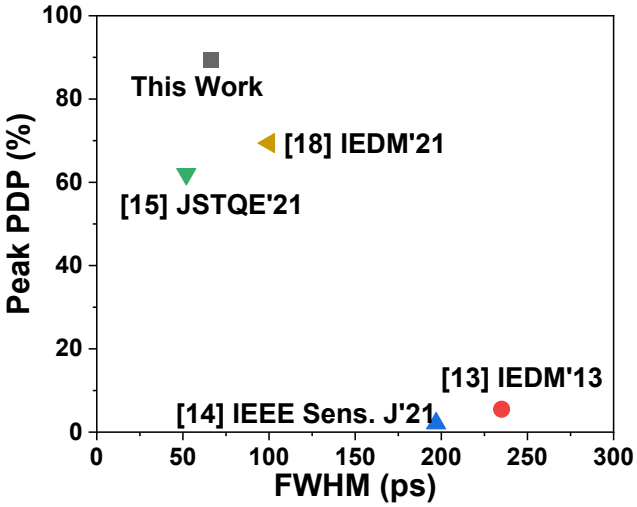

Fig. 15. Peak PDP vs timing jitter (FWHM) comparisons of SPADs fabricated in 90 nm or more advanced processes.

DCR measurements were conducted with a passive quenching resistor of 100 kΩ and an oscilloscope. As can be seen in Fig. 11, the DCR difference between the SPADs with and without canyon etch is almost negligible, and therefore it can be concluded that the canyon etch process over the SPAD does not influence its noise performance. The SPADs show very low DCR, about 0.03 cps/μm^2, at V_E = 1 V so that it can be operable at a higher V_E to increase its PDP performance. When V_E is increased to 7 V, the DCR is about 40 cps/μm^2.

E. Timing Jitter

The timing jitter performance is an important factor for bio-medical applications that requires precise sensing such as ToF PET [23]. The timing jitter is the statistical fluctuation in

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH SPADS FABRICATED IN 90 NM OR MORE ADVANCED PROCESSES

	This work		[13]	[14]	[15]	[17]	[18]
	Without Canyon	With Canyon					
Technology	55 nm FSI BCD	55 nm FSI BCD	65 nm FSI CMOS	65 nm FSI CMOS	55 nm FSI BCD	90 nm BSI CIS	90 nm BSI CIS
Active Junction	PLDD/HVNW	PLDD/HVNW	N+/PW	N+/PW	DPW/BNW	n/a	n/a
Guard Ring	P-epi GR	P-epi GR	Modified NW	NW	Virtual GR	n/a	n/a
Active Area	63.6 μm^2	63.6 μm^2	64 μm^2	100 μm^2	60.8 μm^2	n/a	n/a
V_B	16.1 V	16.1 V	9.1 V	9.52 V	31.5 V	22 V	30 V
V_E	7 V	7 V	0.4 V	0.3 V	7 V	3 V	2.5 V
Normalized DCR	44 cps/μm^2	38.2 cps/μm^2	15.6 kcps/μm^2	138 kcps/μm^2	2.6 cps/μm^2	19 cps/pix	0.044 cps/μm^2
Peak PDP @ wavelength	82% @ 425 nm	89.4% @ 450 nm	5.5% @ 425 nm	2.1% @ 440 nm	62% @ 530 nm	n/a	69.4%* @ 510 nm
PDP at 940nm @ V_E	3.64% @ 7 V	3.94% @ 7 V	0.3% @ 0.25 V	0.2% @ 0.3 V	4.2% @ 7 V	20.2%* @ 3V	24.4%* @ 2.5 V
Timing Jitter @ λ, V_E	68 ps @ 940 nm, 7 V	66 ps @ 940 nm, 7 V	235 ps @ 637 nm, 0.4 V	197 ps @ 685 nm, 0.3 V	52 ps @ 780 nm, 3 V	137 ps @ 940 nm, 3 V	100 ps @ 940 nm, 2.5 V

*PDE with microlens on the top of the SPAD

time between the absorption of the photon and its corresponding avalanche breakdown [22]. It is dominated by carrier transit time, such as drift, diffusion, and avalanche multiplication time [24]. The timing jitter performance of the SPADs was measured using the time-correlated single-photon counting (TCSPC) technique at V_E = 7 V with a 940 nm picosecond pulsed laser having a 30 kHz repetition rate. Both SPADs have excellent timing jitter performance, about 66 ps FWHM, including the jitter of the laser and laser driver as shown in Figs. 12 and 13. Both show almost identical jitter values because they share a common SPAD structure. The timing jitter could be decreased further with integrated circuitry as well as an optimized setup [25].

IV. DISCUSSIONS

The proposed devices are compared with state-of-the-art SPADs fabricated in 90 nm processes and below in Figs. 14 and 15. The previously-reported SPADs that have lower V_B than the present SPAD reported in this paper suffer from very low peak PDP as well as very high DCR [13], [14]. Compared to the SPADs which have higher V_B, our SPAD still exhibits higher peak PDP and lower or comparable timing jitter [15], [17], [18]. We further improve the detection efficiency of our SPAD without sacrificing other performance characteristics. Therefore, the proposed SPAD achieves the highest peak PDP with excellent timing jitter performance in spite of the reduced V_B, while showing reasonable DCR performance. Table I lists the performance summary of the SPADs and shows the performance comparisons with the state-of-the-art SPADs.

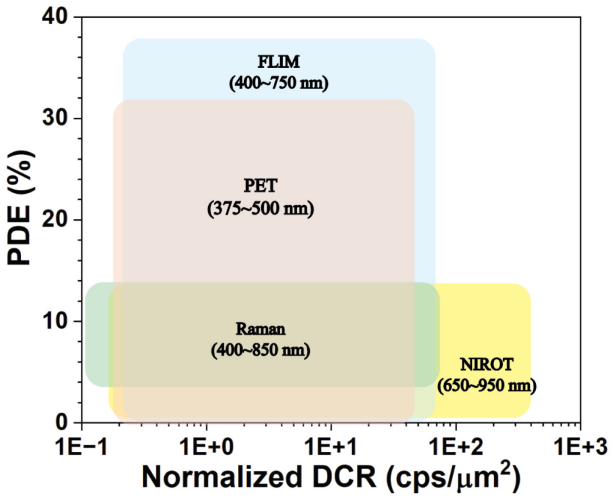

Fig. 16. Different biomedical applications and their requirements [26]–[31].

The demonstrated SPAD can be an excellent candidate for several biomedical applications, where high PDP, low timing jitter, and low V_B are required. For example, the high PDP of the proposed SPAD at around 450 nm is greatly beneficial to PET applications. In addition, the low timing jitter can substantially improve the sensitivity and resolution of ToF-PET systems. Other biomedical applications such as FLIM and time-domain Raman spectroscopy also require such a high PDP in the visible wavelength range. Moreover, as the

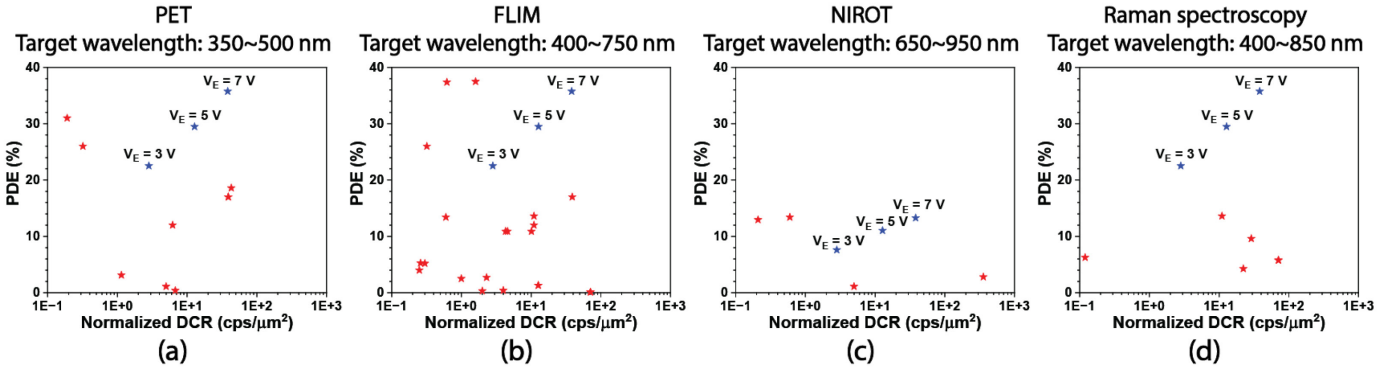

Fig. 17. Peak performance and target wavelength of typical CMOS/BCD-based SPAD sensors for biomedical applications reported in [25]–[30]. For the proposed SPAD we used different excess bias voltages and a fill factor of 40%, assuming no microlenses were used. (a) Reported PET applications vs SPAD at 450 nm, (b) Reported FLIM applications vs SPAD at 450 nm, (c) Reported NIROT applications vs SPAD at 700 nm, (d) Reported Raman spectroscopy applications vs SPAD at 450 nm.

proposed device achieves reasonable NIR efficiency with the use of lightly-doped DNW, it's expected that the SPAD can be also utilized in NIROT applications. In addition, the low V_B offers an advantage to biomedical equipment in terms of power management and consumption, which is expected to play a major role in portable diagnostic and surgical systems.

Many multi-pixel SPAD sensors targeted at biomedical applications are actually co-integrated with the corresponding quench/recharge and data acquisition circuits. Therefore, the overall pixel efficiency, also called photon detection efficiency (PDE), is defined as PDE = PDP × fill factor (FF). Fig. 16 shows the PDE and normalized DCR range of typical CMOS/BCD-based SPAD sensors for biomedical applications [26]–[31]. The fill factor of the SPAD is determined by the ratio of the active area of the SPAD to the total area of the device. With an active area diameter of 9 μm and a total diameter of 14.4 μm, the fill factor of the device is about 40%. Also, as shown in Fig. 17, the sensors in different biomedical applications are compared to the peak performance of the proposed SPAD at different excess bias voltages, taking into account a FF of 40%. Considering the various target wavelengths of each technology, the non-identical peak performance of the SPAD is used for the comparison. For PET, FLIM, and Raman spectroscopy, the SPAD's performance at 450 nm, where the device has the maximum efficiency in their target wavelengths, is compared to the SPAD sensors as can be seen in Fig. 17. (a), (b), and (d). On the other hand, the performance at 700 nm is used to compare NIROT's sensors. Although an ideal sensor would be placed in the top left corner of the plot, the proposed SPAD can be optimized in terms of the PDP and DCR according to each application by adjusting its excess bias voltage. It should thus be able to satisfy the demanding requirements of most biomedical applications.

V. Conclusion

We have demonstrated and characterized high-performance SPADs based on 55 nm BCD technology. With the use of layers available in BCD technology, the SPAD structure is optimized for low-noise and high-efficiency operation with a low V_B. In order to enhance its efficiency, we use canyon etch to reduce multilayer reflections. The resulting SPAD has a V_B of 16.1 V, peak PDP of 89.4% at 450 nm, DCR of 38.2 cps/μm^2, and timing jitter of 66 ps at V_E = 7 V. It's expected that the proposed SPAD has a great potential for several biomedical applications.

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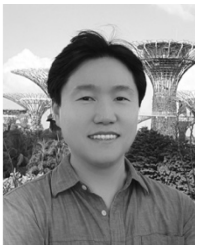

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