Doping Engineering for PDP Optimization in SPADs Implemented in 55-nm BCD Process

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***Abstract*—We introduce a new family of single-photon avalanche diodes (SPADs) with enhanced depletion regions in a 55-nm Bipolar-CMOS-DMOS (BCD) technology. We demonstrate how to systematically engineer doping profiles in the main junction and in deep p-well layers to achieve high sensitivity and low timing jitter. A family of sub 10 μm SPADs was designed and fully characterized. With the increase of the well-defined depletion region, the breakdown voltages of three variants are 17.1, 20.6, and 23.0 V, respectively, the peak PDP wavelengths are 450 nm, 540 nm, and 640 nm, respectively. The timing jitter below 50 ps (FWHM) at 5 V excess bias voltage are achieved in SPAD1 and SPAD2. SPAD3 shows a high PDP over a wide spectral range, with a peak PDP of 41.3% at 640 nm, and 22.3% at 850 nm, and the timing jitter 96 ps at 3 V excess bias voltage. The proposed SPADs are suitable to low-pitch, large-format image sensors for high-speed, time-resolved applications and quantum imaging.**

***Index Terms*—Single-photon avalanche diode (SPAD), BCD, doping engineering, single-photon imaging, quantum imaging.**

I. Introduction

SINGLE-photon avalanche diodes (SPADs) in monolithic CMOS technology [1] have been receiving great attention in recent years for scientific, industrial, and consumer applications, such as time-of-flight (TOF) sensing [2]–[4] , low-light photon counting and imaging [5], [6], biomedical imaging [7], [8], quantum random number generation (QRNG) [9]. However, CMOS SPADs using advanced technology nodes, below 180 nm, tend to have limited photon detection probability (PDP) in a small range of wavelengths and generally low sensitivity in near-infrared (NIR) spectral range, due to narrow depletion regions available in these technologies [10].

Significant improvements in NIR and an overall wide spectral range has recently been achieved in submicron CMOS technologies [10]–[14] and the use of electrical microlensing [15], also known as charge focusing [16], has been shown to be useful to improve PDP. Electrical microlensing consists of forcing photo-generated carriers to drift towards the multiplication region by gradual doping profiles or non-vertical electric fields. However, wide and deep depletion regions appear to be the most effective means to improve NIR PDP. For instance, Webster *et al.* have achieved over 40% PDP from 410 nm to 760 nm at high excess bias by burying the multiplication region in 130 nm CMOS technology. Niclass *et al.* have used fully depleted SPAD structures in 180 nm CMOS technology achieved PDP of 64.8% and 24% at 610 nm and 850 nm, respectively at moderate excess bias.

Recently, advanced backside illuminated (BSI) 3D stacking technologies have emerged with high fill factor, making high NIR PDP SPAD sensors possible. A BSI charge-focusing SPAD achieved a PDE (photon detection efficiency) of 24.4% at the wavelength of 940 nm with optical microlenses and a dedicated light trapping technique [6]. Another work reported a PDE of 21.8% for only 2.5 µm pitch with an optimized gapless microlens and pyramid surface for diffraction (PSD) [17]. The PDE of 36.5% at 940 nm, the world's highest value so far, was achieved by combining dual diffraction and 2x2 on-chip lens [18]. However, the BSI technology typically is high cost, and requires long delivery time.

In this paper, we report on a new family of frontside-illuminated (FSI) SPADs with a pitch of 8.5 µm characterized by fully depleted main junction and 3 different depletion DPW layers, with the potential of being miniaturized further. We first demonstrate how to systematically engineer the doping profile of the main junction and of the deep p-well layers, and then fully characterize the impact of doping engineering in small SPADs. The proposed structures are called SPAD1, SPAD2, and SPAD3, where SPAD1 and SPAD2 are optimized for timing jitter, with less than 50 ps (FWHM) at 5 V excess bias voltage, while SPAD3 was red and NIR enhanced, with a comparably low timing jitter.

II. SPAD Structure and Simulation

Fig. 1(a) shows the cross-section of the FSI SPAD family in 55 nm BCD process. The SPAD is based on a shallow N-well (NW) and P-well (PW) junction. The pitch is 8.5 µm. All the SPADs presented in this study were designed and realized in a round shape with an avalanche diameter of 4.4 µm, achieving a fill factor of 21%. Based on the achieved results, a parameter optimization can be performed to achieve a higher fill factor in future generations. Fig. 1(b) shows the doping profile versus

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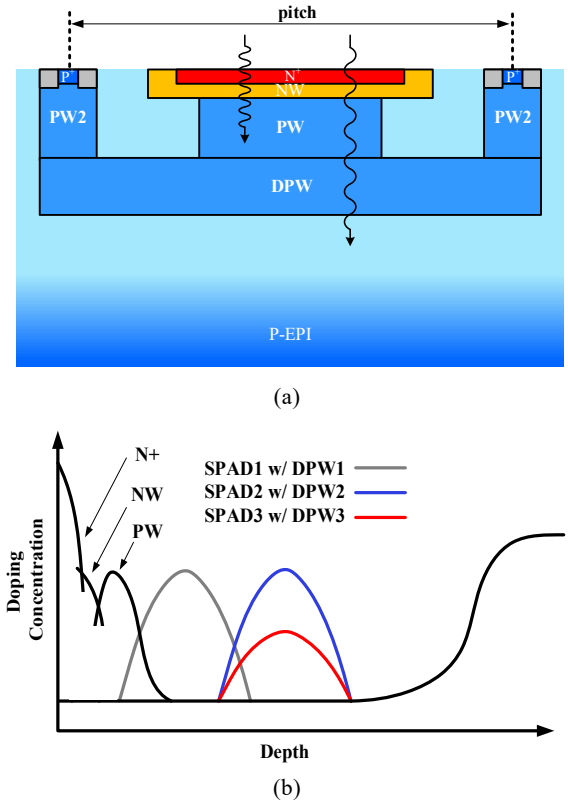

Fig. 1. (a) Simplified cross-section of the proposed SPAD. The structure is based on shallow NW and PW layers. Three different DPW layers are also implemented. All 3 SPADs have the same drawn avalanche area and pitch. (b) The simplified doping profile versus depth below silicon surface. Layers DPW1-3 are used in SPAD1-3, respectively.

depth below surface. The substrate features a gradient of p-type doping in the epitaxial layer, and the SPAD incorporates three different deep P-well (DPW) layers below the junction.

Doping engineering is employed in both the main junction and deep p-well layers. Fig. 2 shows simulations of the relative electric field, as well as the depletion layer boundaries. For the main junction, the avalanching junction is engineered through shallow NW and PW layers and optimized to achieve a high avalanche gain and wide depletion region. Significant efforts are dedicated to fine-tuning the fully depleted PW layer to achieve a higher breakdown probability. For the different DPW layers, the depletion region can be well defined in depth, while photo-generated carriers in the depletion region can quickly drift towards the avalanching junction.

III. Results and Discussion

A. I-V Characteristics

The static current/voltage curves of the proposed SPADs were measured using a semiconductor analyzer, revealing extremely low dark current levels in the pA range for all three variants. The current-voltage curves with illumination are shown in Fig. 3(a).

With different DPW layers, the corresponding breakdown voltages are 17.1, 20.6, and 23.0 V, respectively. This means that the breakdown voltage is related to both the main junction

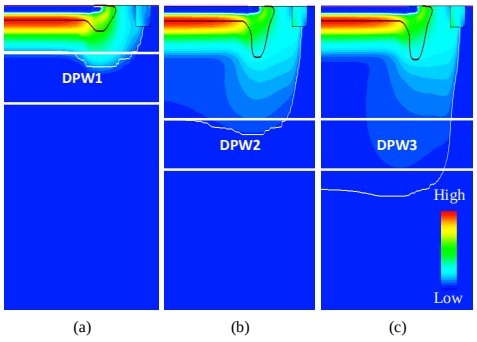

Fig. 2. Simulation results depicting the electric field as well as the depletion layer boundaries for SPAD1 (a), SPAD2 (b), and SPAD3 (c) at 3V excess bias voltage. The junction is engineered to achieve a wide depletion region.

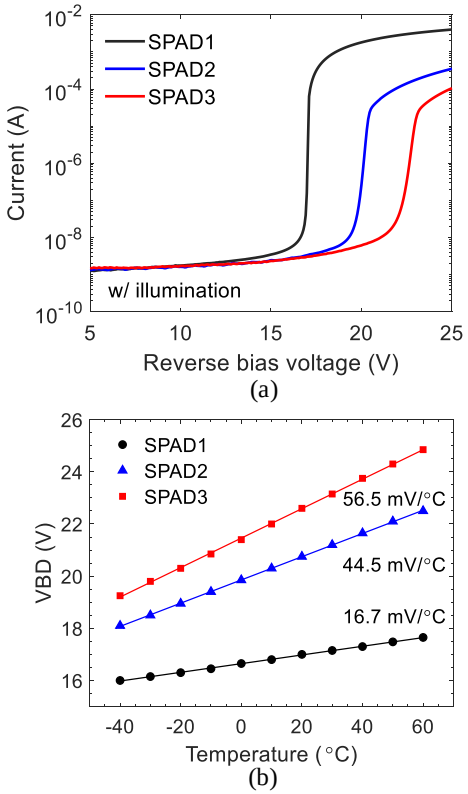

Fig. 3. (a) SPADs current as a function of reverse bias voltage with illumination. (b) Breakdown voltage as a function of temperature for 3 different SPADs.

and the DPW layers for miniaturized fully depleted SPAD. Besides, it is clearly shown that SPAD2 and SPAD3 achieve lower photo-current above the breakdown voltage. Fig. 3(b) shows the breakdown voltage as a function of temperature from -40 ℃ to 60 ℃. The extracted temperature coefficients are 16.7, 44.5, and 56.5 mV/℃, respectively. With a thicker depletion region, the temperature coefficients grow larger [19].

B. Dark Count Rate

The dark count rates (DCRs) of 8 samples for each SPADs were measured at room temperature. Fig. 4(a) shows the

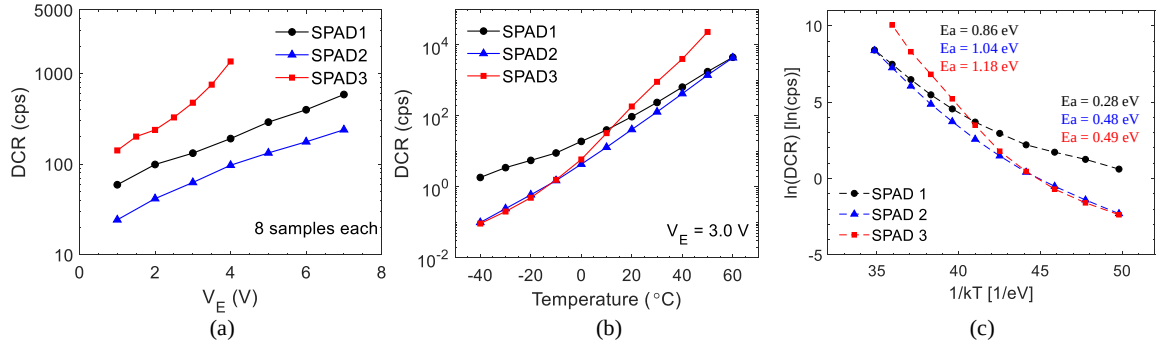

Fig. 4. (a) Median DCR at room temperature. The data is obtained by measuring 8 dies. (b) Temperature dependence of DCR for 3 different SPADs. Measurements were taken from one SPAD sample each from -40 ℃ to 60 ℃. (c) Arrhenius plot of the DCR for 3 different SPADs at the excess bias voltage of 3 V.

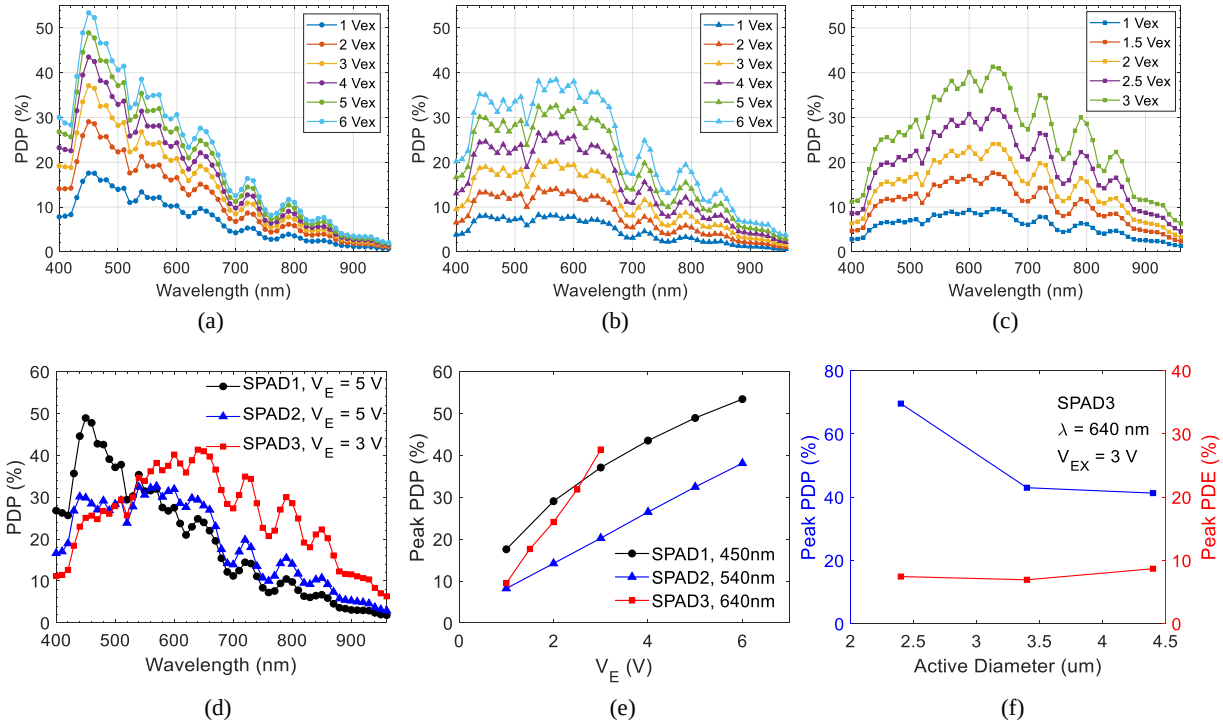

Fig. 5. Measured PDP as a function of wavelength for SPAD1 (a), SPAD2 (b), and SPAD3 (c) from 400 nm to 960 nm with the step of 10 nm. (d) PDP comparison as a function of wavelength for 3 different SPADs. (e) PDP as a function of excess bias voltage at the peak wavelength for 3 different SPADs. (f) Peak PDP and PDE as a function of draw active diameter of SPAD3. The guard ring width is same during the scaling. The PDP is calculated based on the draw active area.

median DCR as a function of the excess bias voltage. The median DCR of SPAD1 is 132 cps and 290 cps at 3 V and 5 V excess bias voltage, respectively. This can be further reduced through optimizing the guard ring to decrease the electitric field in the junction edge. It is clear that SPAD2 shows the best DCR performance, with the median DCR of 62.3 cps and 132.2 cps at 3 V and 5 V excess bias voltage, respectively. The median DCR of SPAD3 is 474.2 cps at 3 V excess bias voltage. SPAD3 shows the worst DCR performance, due to deep-level traps in the wide depletion region. The temperature dependence of DCR at 3 V excess bias voltage is shown in Fig. 4(b), whereas SPAD2 and SPAD3 show a strong temperature dependence. As the thermal generation is the main source of dark count rate, activation energies can be extracted from the temperature dependence [20]. The Arrhenius plot for 3 different SPADs is shown in Fig. 4(c). At high temperature, where SRH (Shockley-Read-Hall) effect is the dominant, the corresponding activation energies of the SPAD family is 0.86, 1.04, 1.18 eV, respectively. With the temperature cooling down, the tunneling mechanism becomes more important. The the corresponding activation energies of the SPAD family is 0.28, 0.48, 0.49 eV, respectively

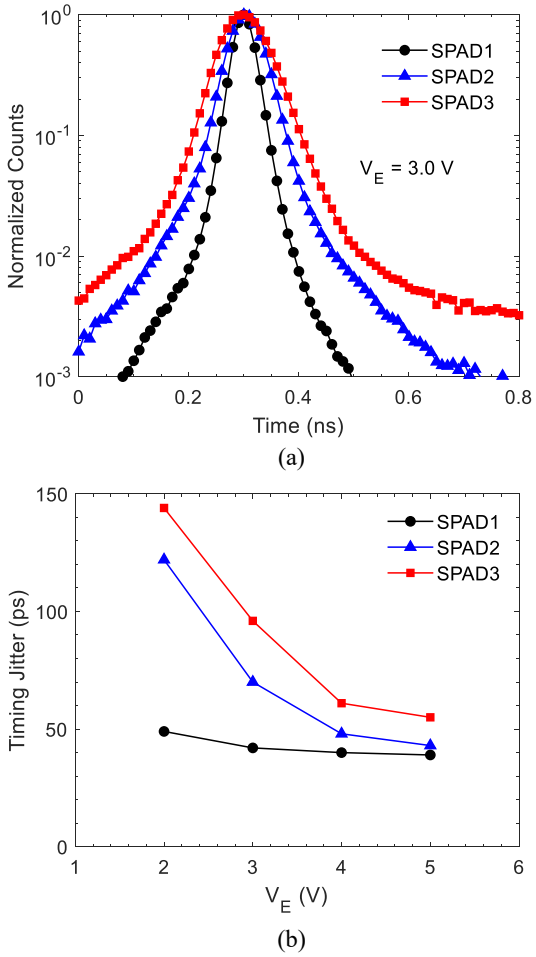

Fig. 6. (a) Timing jitter response for an 850 nm laser at 3 V excess bias voltage. The jitter of the laser is 32 ps. (b) Timing jitter (FWHM) as a function of excess bias voltage.

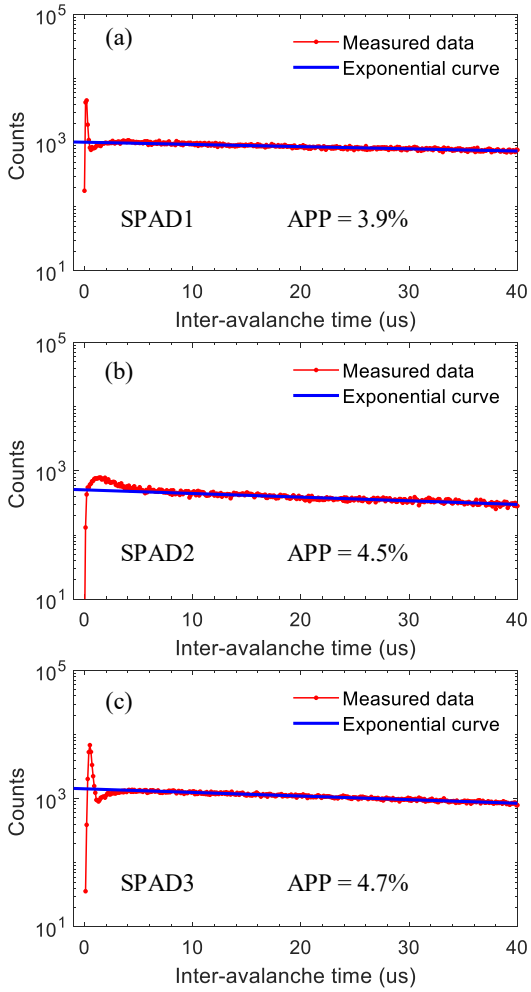

Fig. 7. Afterpulsing probability: measured inter-avalanche time histogram at room temperature. (a)-(b) SPAD1 and SPAD2 at 5 V excess bias voltage. (c) SPAD3 at 3 V excess bias voltage. The dead time of each SPAD was 100 ns.

C. Photon Detection Probability

PDP measurement was taken at room temperature with 10 nm interval using the continuous light technique [21]. The calculated PDP is based on the draw avalanche area. Fig. 5 shows the measured PDP results from 400 nm to 960 nm with the step of 10 nm for all the SPADs. With the different DPW layers, it is clearly shown that the peak PDP wavelengths are observed to be 450 nm, 540 nm, and 640 nm, respectively. SPAD1 achieves peak PDP of 48.9% at 450 nm, 6.7% at 850 nm, and 2.4% at 940 nm at 5 V excess bias voltage. SPAD2 achieves peak PDP of 32.4% at 540 nm, 10.7% at 850 nm, and 3.7% at 940 nm at 5 V excess bias voltage. Thanks to the wider depletion region, SPAD3 shows a high PDP over a wide spectral range, with peak PDP of 41.3% at 640 nm, 22.3% at 850 nm, and 8.3% at 940 nm at 3 V excess bias voltage. This broad spectral response from visible to NIR holds great potential for a diverse applications. The peak PDP as a function of excess bias voltage is shown in Fig. 5(e). The peak PDP of SPAD3 shows the strongest dependence on excess bias voltage. The miniaturization of SPAD plays a crucial role in the development of large-format image sensors. During the pitch scaling down, same guard ring width is maintained. However, the reduction in SPAD pitch presents challenges in accurately evaluating the avalanche area through light emission test, and the process mismatch can have a higher impact. Fig. 5(f) shows the peak PDP and PDE of SPAD3 as a function of draw active diameter. The minimum active diameter is 2.4 μm, the corresponding pitch is 6.5 μm. We can see that the peak PDE decreases only a bit during the pitch scaling from 8.5 μm to 6.5 μm. The lateral charge collection by drift-diffusion can help enhance the sensitivity thanks to the fully depleted structure.

D. Timing Jitter

A dedicated printed circuit board equipped with a fast comparator was utilized to evaluate the timing jitter. A low threshold voltag,which was close to the baseline of the output pulse, was applied to detect the SPAD signal at the onset of the avalanche phenomenon. Fig. 6(a) shows the timing jitter at 3 V excess bias voltage with an 850-nm laser source (NKT Photonics PiL085X). The jitter of the laser is 32 ps. The evolution of jitter as a function of the excess bias voltage

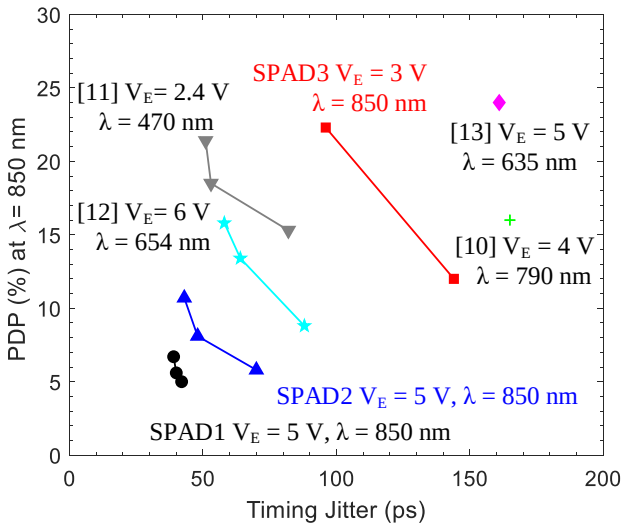

Fig. 8. Performance comparison of the N-on-P SPADs in monolithic CMOS technologies. PDP at 850 nm versus timing jitter at similar excess bias voltages is reported.

is shown in Fig. 6(b). A timing jitter of 42, 70, and 96 ps (FWHM) is achieved at 3 V excess bias voltage, respectively. The timing jitter at same excess voltage increases clearly with the expansion of the depletion region, because the timing fluctuation of the photo-generated carriers upward towards the avalanching area will be dominant.

E. Afterpulsing Probability

Under constant low light condition, the distribution of inter-avalanche time follows poisson statistics. An afterpulse can be triggered by trapped carriers during recharging. The measured afterpulsing probability (APP) is shown in Fig. 7. A high threshold voltage of the comparator, which was close to the peak of the output pulse, was applied to detect the output pulse. The dead time is about 100 ns.The afterpulsing probability of SPAD1 and SPAD2 was measured to be 3.9%, and 4.5% at 5 V excess bias voltage. The measured afterpulsing probability of SPAD3 was 4.7%. Due to the lack of integrated quench and recharge circuits, a large number of carriers maybe trapped after an avalanche. Thus, the measured afterpulsing probability was significantly overestimated.

IV. State-of-the-Art Comparison

Fig. 8 shows the PDP and timing jitter comparison of the proposed SPADs with the previously reported N-on-P type SPADs in CMOS technology. The proposed SPAD1 and SPAD2 show less than 50 ps timing jitter at 5 V excess bias voltage. The proposed SPAD3 shows a high PDP at 850 nm, while keeping a low timing jitter at 3 V excess bias voltage. Table 1 shows the overall performance of the developed SPADs and comparison with the state-of-the-art SPADs.

V. Conclusion

We demonstrate the role of doping engineering to widen the depletion region in small SPADs with a pitch of 6.5 μm to 8.5 μm implemented in a 55-nm BCD process. To demonstrate it practically, a family of SPADs was designed, realized, and fully characterized in this technology. The doping profiles of the avalanching junction layers were optimized to achieve red- and NIR-enhanced sensitivity. Experimental evaluation of the proposed SPADs revealed that the PDP peak wavelength can be improved with a wider and deeper depletion region, thereby achieving a high PDP over a wide spectral range, with a peak PDP of 41.3% at 640 nm, and 22.3% at 850 nm, and the timing jitter 96 ps at 3 V excess bias voltage. The technique is suitable for small-pitch SPADs and large-format image sensors, with multi-megapixel resolution, both operating in frontside- and backside-illuminated modes.

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH N-ON-P FRONT-SIDE ILLUMINATED SPADS IN CMOS TECHNOLOGY.

Parameter	This work (SPAD1)	This work (SPAD2)	This work (SPAD3)	[10]	[11]	[12]	[13]	[14]
Structure	Shallow NW/PW	Shallow NW/PW	Shallow NW/PW	N+/PW	Deep NW/epi	Deep NW/epi	Deep NW/PW	Deep NW/PW
Technology (nm)	55	55	55	180	90	130	180	180
Pitch (μm)	8.5	8.5	8.5	N/A	N/A	N/A	25	N/A
Avalanche area (μm^2)	15.2	15.2	15.2	78.5	32.1	50.2	206.9	220
Fill Factor (%)	21	21	21	N/A	N/A	N/A	33.1	35
VBD (V)	17.1	20.6	23.0	19.7	14.9	20	20.5	20.0
VE (V)	5	5	3	4	2.4	6	5	5
DCR (cps/μm^2)	19.1	8.7	31.2	30	~4.6	0.36 (V_E = 2 V)	0.6	1.7
PDP Peak (%)	48.9 @450 nm	32.4 @540 nm	41.3 @640 nm	36 @600 nm	44 @690 nm	45.2 @560 nm	64.8 @610 nm	47 @570 nm
PDP (%) @ 850 nm	6.7	10.7	22.3	16	21.4	15.8	24	20
PDP (%) @ 940 nm	2.4	3.7	8.3	N/A	10.1	5.7	8.8	9.7
Afterpulsing probability (%)	3.9[a]	4.5[a]	4.7[a]	50[a]	0.38	0.98	0.49	N/A
Dead time (ns)	100[a]	100[a]	100[a]	750[a]	23	35	24.9	N/A
Timing Jitter (ps) FWHM	39 @850 nm	43 @850 nm	96 @850 nm	165 @790 nm	51 @470 nm	58 @654 nm	161 @635 nm	N/A

[a] This value is significantly overestimated with huge parasitic capacitance due to the lack of integrated circuit.

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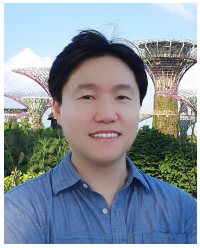

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