A 0.32 × 0.12 mm^2 Cryogenic BiCMOS 0.1–8.8 GHz Low Noise Amplifier Achieving 4 K Noise Temperature for SNWD Readout

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***Abstract*— A significant number of cryogenic low-noise amplifiers (cryo-LNAs) are required for the readout of superconducting nanowire detector (SNWD) arrays. It is desirable to have compact cryo-LNAs in place so that the size of the readout circuitry for the SNWD array can be reduced. In this study, we first examined the bandwidth, linearity, and noise requirements of the cryo-LNA for SNWD readout. After that, the design and implementation of a wideband silicon–germanium (SiGe) BiCMOS cryo-LNA were described in detail. The LNA features two cascode stages with resistive shunt–shunt feedback for wideband input impedance matching. The capacitive peaking techniques and emitter inductive degeneration via a slab inductor were utilized to increase the bandwidth without compromising the layout's compactness. To ensure the amplifier works well at cryogenic temperatures, we modified the model parameters from the foundry-provided models based on the device's reported cryogenic test data. The measurement results at 3.6 K demonstrate that the cryo-LNA, occupying a core size of only 0.03 mm^2, achieves a noise-equivalent temperature (NET) of 4–10 K and an average gain of 30.5 dB in the frequency band from 0.1 to 8.8 GHz, under a power consumption of 8.2 mW. We successfully integrated this LNA with a quantum sensor array on a printed circuit board (PCB) and obtained favorable test results, demonstrating the potential application of LNAs for reading large-scale SNWDs.**

***Index Terms*— BiCMOS, cryogenic temperatures, low-noise amplifiers, SiGe heterojunction bipolar transistor (HBT), superconducting single-photon detectors, timing jitter.**

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I. Introduction

SIGNIFICANT progress has been achieved in the field of superconducting nanowire detectors (SNWDs) since their initial demonstration [1]. The SNWDs offer high-speed single-photon detection capabilities across a wide range of wavelengths from ultraviolet to infrared, with high detection efficiency (DE), low noise, and precise photon timing. Alongside advancements in device physics, detector design, and applications [2], efforts have been made to translate high-performance SNWD devices into complete systems that provide users with access to their capabilities ranging from mass spectrometry, molecular ultraviolet–visible (UV–VIS)/infrared (IR) spectroscopy, and even dark matter detection [3], [4]. Improvements in the low-loss optical coupling, enhanced readout circuits, and optimized device designs have enabled the realization of detector systems that exhibit high system DE, high maximum count rates, low noise, and low timing jitter [5]. Various engineering approaches have been employed to overcome these challenges, each offering advantages and tradeoffs regarding implementation complexity, performance, and scalability. Consequently, integrating the readout front end alongside the SNWD arrays within the cryostat is anticipated, using the same printed circuit board (PCB) or package. This approach minimizes the interconnects between room temperature (RT) and cryogenic temperature (CT) environments. Primarily, applications requiring many cryogenic low-noise amplifiers (cryo-LNAs) with low noise, small area, and low power consumption are targeted.

One approach to designing a cryo-LNA with a noise-equivalent temperature (NET) of a few degrees kelvin is to use III–V InP or GaAs high-electron-mobility transistors (HEMTs). However, for the large-scale SNWD readout scenarios, LNAs are only a part of the readout electronics, and more complex digital-to-analog mixed circuits, such as clocks, time-to-digital converters (TDCs), and multiplexers, are expected to be realized in the same system-on-chip (SoC) to improve the integration and reliability. In this fully integrated readout envision, III–V cryo-LNA is possibly a less suitable option. Thus, people are turning to radio

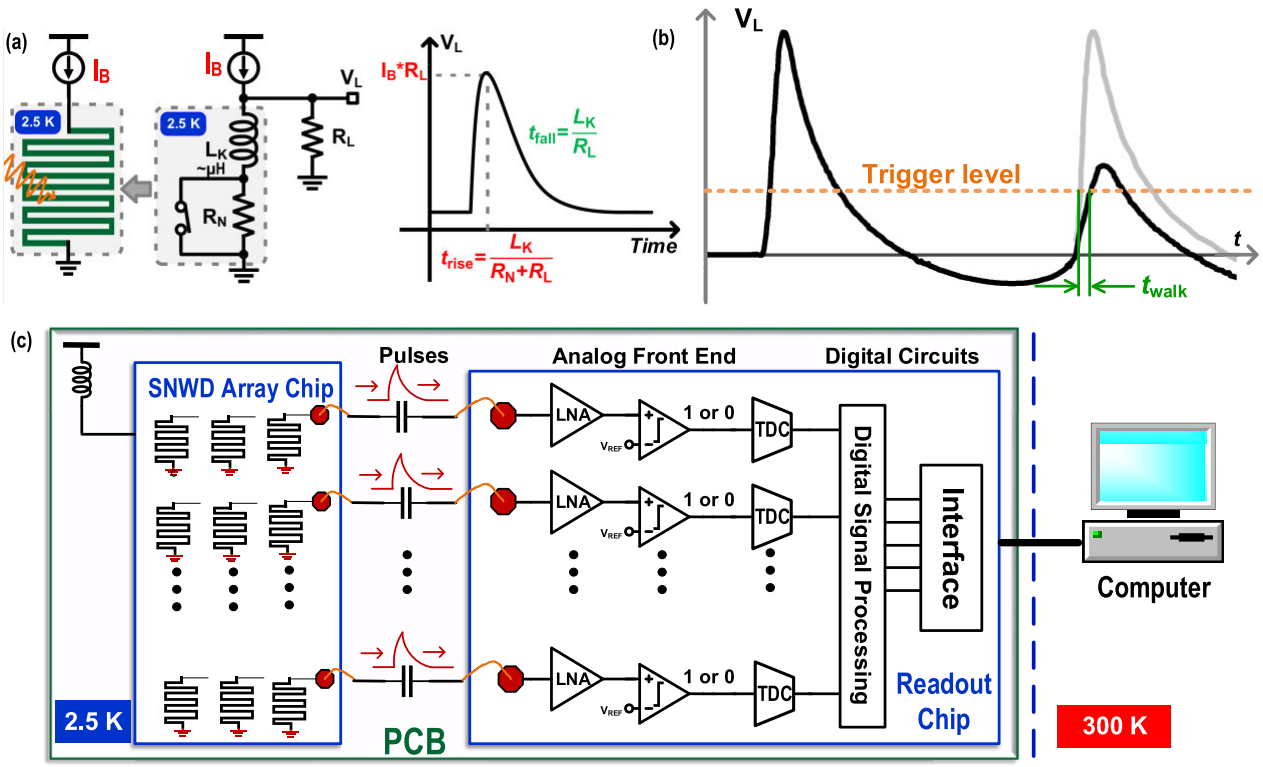

Fig. 1. (a) SNWD device, together with its model and output voltage pulse. (b) Time walk error of the SNWD. (c) Scheme for access of SNWD array.

frequency (RF) CMOS processes for cryo-LNA implementations [6], [7]. However, these LNAs often need several tens of milliwatts of power consumption, while the measured NET can be easily larger than 10 K at 4 K ambient temperature. Therefore, in our cryo-LNA implementation, we used a SiGe BiCMOS process, which is quite versatile, allowing the design of digital/analog mixed-signal building blocks (using the MOSFETs) and low-noise RF building blocks using the SiGe heterojunction bipolar transistors (HBTs). Apart from the noise performance, unlike depletion-mode III–V HEMTs, SiGe HBTs implemented in BiCMOS support single-polarity biasing, simplifying biasing. This advantage becomes significant when scaling up the number of interfaced SNWDs. Furthermore, HBT's $1/f$ noise is much lower than that of a field-effect transistor (FET); thus, up-down conversion processes become more robust.

Cryogenic SiGe HBT LNAs have found diverse applications in SNWD readout, radio astronomy, quantum computing, and terahertz microwave kinetic inductance detector systems [6], [7], [8]. However, many of these LNAs have relied on large-area inductors or off-chip matching elements to ensure reliable operation, which resulted in low reliability and reproducibility. To ensure low-power operation, sub-mW C-band cryogenic HBT LNAs with an exceptionally low collector–emitter voltage ($V_{CE} \approx 0.2$ V) have been developed explicitly for superconducting transmon qubit readout applications [7]. It is important to note that such low V_{CE} values can degrade linearity notably [9]. In the context of SNWD readout, nonlinearities in the readout cryo-LNA response can distort the shape and timing of the amplified signal. This distortion can affect the accuracy of photon counting or timing measurements performed using the SNWD. In the case of ultra-thick SNWDs readout or amplitude multiplexed readout of SNWDs [10], [11], [12], the detectors' output current might reach tens to over 100 μA. Consequently, this leads to an input voltage of the readout LNA as high as ~2 mW to ~5 mV (~−41 to −33 dBm). Thus, it is crucial to have an amplifier with high linearity to preserve the fidelity of the detected photon signal.

This work describes a compact and low-noise cryo-LNA with reasonable linearity aiming for SNWD readout. After the introduction, Section II will discuss the influence of cryo-LNA's performance on the SNWD readout timing jitter to conclude the specifications of the LNA. Section III will analyze and design the wideband cryo-LNA. Then, Section IV illustrates the implementation and the measurement results, while the SNWD readout result using the designed LNA is given in Section V. We conclude our article in Section VI.

II. SNWD Readout Front End: Specifications

An SNWD typical readout circuit is schematically shown in Fig. 1(a). The SNWD is biased with a current source I_b through a bias tee. Neglecting the high-order nonlinearity, the detector can be modeled by an inductance L_k representing the kinetic inductance of the superconducting nanowire, which is in series with a variable resistor whose resistance is 0, while the nanowire is superconductive and $R_N \approx 1$–2 kΩ when the detector absorbs a photon or particle. This shift in resistance causes a voltage pulse at the output of SNWD, and the rising

time of the pulse can be written as

$$t_R \approx \frac{L_k}{R_N + R_L} \tag{1}$$

where R_L is the load resistance of the detector. Given the low intrinsic timing jitter of the SNWD, this voltage pulse can accurately time tag the photon or particle hit. The performance of the readout electronics will degrade the SNWD system timing jitter (J_T), a statistical figure that represents the deviation of the real response voltage pulse from the ideal arrival time. Here, we will discuss the influence of the noise figure, bandwidth, and linearity on J_T.

The critical current in typical SNWD designs is a few tens of microamperes, which implies that the output amplitude of the output pulse (A_P) is around 1 mV. It is, therefore, advantageous (though not strictly required) to employ a cryogenic amplifier circuit to increase the signal amplitude, making it processable by subsequent readout electronics, typically consisting of comparators with a constant threshold (V_{TH}) to define the timing mark for the TDC and the digital back end. The noise of the LNA adds jitter to the output voltage pulse, thus lowering the low timing jitter. According to the small-signal perturbation theory [13], the timing jitter caused by the noise of the LNA at the output of the LNA can be expressed as [5]

$$J_{\text{LNA}} \approx \frac{\sigma_{\text{LNA}}}{K} \times 2.355. \tag{2}$$

K is the slope of the rising edge of the pulse and σ_{LNA} is the LNA's root-mean-square (rms) noise voltage at its output port. K is determined by t_R and A_P, which is set by I_B (the bias current of the SNWD) and the gain of the LNA and is further affected by its bandwidth. Taking these factors into consideration, (2) can be expressed as

$$J_{\text{LNA}} \approx \frac{\text{NF} \cdot \sigma_i \cdot t_{R\_\text{LNA}}}{I_B \cdot R_L} \times 2.355 \tag{3}$$

where t_{R_LNA} is the rising time of the pulse at the output of the LNA. When L_k is tiny, the detector output pulse is extremely sharp ($t_R \sim$ 50–100 ps), and the amplifier's bandwidth (BW) is the limiting factor in achieving a minimal t_{R_LNA} and, thus, low J_{LNA}. σ_i is the rms noise voltage at the input port of the LNA. If only the effect of thermal noise is considered

$$\sigma_i = \sqrt{4 \cdot k \cdot T_{\text{AMB}} \cdot \text{BW} \cdot R_S} \tag{4}$$

where k is Boltzmann's constant, T_{AMB} is the ambient temperature of the LNA, and R_S is the input port resistance. If the kinetic inductance L_k is small, then the limitation to achieve a small t_{R_LNA} is the bandwidth of the LNA, which can be expressed as $t_{R\_\text{LNA}} = 0.35/\text{BW}$. Thus, we can rewrite (3) as

$$J_{\text{LNA}} \approx \frac{\text{NF}}{I_B \cdot R_L} \cdot \sqrt{\frac{4 \cdot k \cdot T_{\text{AMB}} \cdot R_S}{\text{BW}}} \times 0.824. \tag{5}$$

The above equation shows that to reduce the deterioration of the SNWD system timing jitter by the LNA's noise, we need a small $\text{NF}/\sqrt{\text{BW}}$ and low operating temperature of the LNA and the detector. Our SNWD samples were biased at 5–20 μA with R_N = 1–2 kΩ. Since the typical rising time of the output pulses from the detectors is 100–400 ps, we set the LNA's objective bandwidth >6 GHz in order to effectively capture the rising edge. To guarantee the timing jitter of SNWD with the cryo-LNA reaches <15 ps, we can readily obtain that the NF of the LNA should be better than 0.15 dB in the worst scenario.

For leading-edge-technique-based photon counting methods used in the SNWD readout, a comparator with a constant threshold voltage (V_{TH}) is used to define the timing mark for the TDC. V_{TH} has to be reasonably high to prevent false triggering due to noise. For the high-count-rate scenario, the pulse amplitude is varied due to the long reset time of the SNWDs [14]. The performance of the leading-edge technique is limited by the significant timing error (also known as time walk error) caused by the varied amplitude, as shown in Fig. 1(b). The time walk is inversely proportional to the slope of the leading edge. Thus, a steeper rising edge results in a smaller time walk error under the same varying amplitude. Therefore, we must preserve the detector pulses' steep rising edge up to the LNA. This further emphasizes the significance of extending the amplifier's bandwidth.

The linearity of the amplifier used in the readout circuitry, which is often expressed in terms of output 1-dB compression point ($P_{1\ \text{dB}}$) and third-order intermodulation point (OIP3), is also crucial since it determines how accurately the amplified signal represents the original input. Any nonlinearities in the amplifier's response can distort the shape and timing of the amplified signal. This distortion impacts the accuracy of photon counting or timing measurements performed using the SNWD. Furthermore, the nonlinear amplifier restricts the dynamic range, compressing the amplified pulse signal. This can lead to inaccurate readings or loss of information, especially when dealing with high-count-rate photon signals or in applications where a wide range of photon fluxes must be detected. Assuming the output pulse amplitude of the LNA V_O = 70 mV, which is sufficiently larger than V_{TH} =~50 mV, the average output $P_{1\ \text{dB}}$ can be calculated as approximately −7 dBm with a load of 50 Ω. To achieve extremely low power consumption, the HBTs were used to construct the two-stage cryo-LNAs, and those HBTs were biased closely to the forward region with a low collector–emitter voltage (V_{CE} = 0.2–0.4 V) [9], [10]. This design approach sacrifices too much linearity, making it inappropriate for SNWD readout electronics.

Some important applications, such as dark matter detection and space-based astronomy, quantum imaging, and mass spectrometry [3], generally require large detector arrays. Positioning the LNA in close proximity to the SNWD shortens the signal path, thereby reducing signal loss and minimizing the risk of external interferences, such as electromagnetic interference and thermal noise, negatively impacting the timing jitter caused by the interconnection. Thus, a proposed scheme is illustrated in Fig. 1(c), where the SNWD array chip is mounted side-by-side with the readout integrated circuits and connected by bonding wires at cryogenic temperatures. This imposes compactness in the area for the LNA to decrease the cost. Moreover, the crucial tradeoff between jitter and power consumption when scaling up the number of pixels is arising.

TABLE I
LNA NOISE FIGURE BUDGET CALCULATION

Parameters	Specifications
Operating Temperature	<4.2 Kelvin
Bandwidth	0.1~6 GHz
Noise Figure (Equivalent Noise Temperature)	<0.15 dB (10 Kelvin)
Power Consumption	<10 mW
Area	<1 mm^2
Output P1 dB (Output IIP3)	>-7 dBm (>2 dBm)

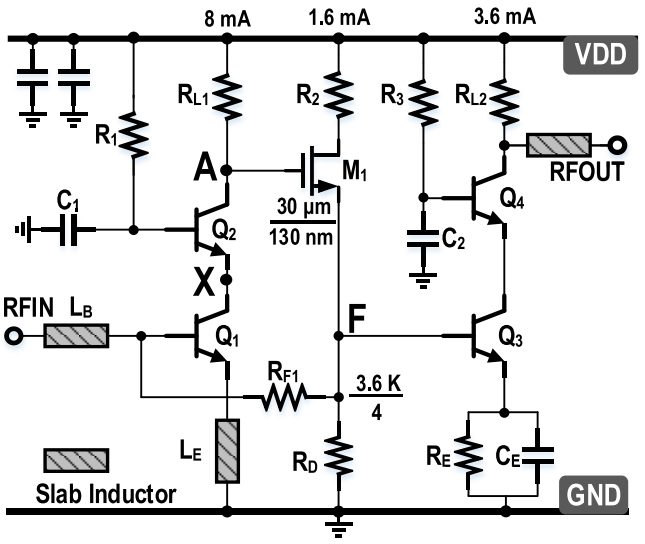

Fig. 2. Topology of the BiCMOS wideband low-noise amplifier.

In this study, the cool power budget of the cryostat is ~0.9 W, and it is intended that 32 detectors will be accessed concurrently; therefore, the power consumption of a single readout channel is approximately 28 mW. Considering that the comparator, TDC, and digital back-end blocks are expected to consume a significant amount of power, we allocated 10 mW to the cryo-LNA. From all of the above analysis, we listed the main objective specifications of the LNA in Table I.

III. CRYO-LNA DESIGN

Fig. 2 depicts the SiGe BiCMOS LNA structure. It is a variant of the conventional Meyer topology [15]. A single shunt feedback is applied to scale down the input impedance by around a factor of the loop gain so as to achieve wideband impedance matching. We used the cascode structures as the primary amplification core in our design for robust stability and enhanced single-stage gain. In the meantime, we eliminated the global feedback between the input and the output stages of a Meyer amplifier to reduce the gain loss caused by the feedback loops. To set the transistors' quiescent bias properly, relying on a single supply voltage, a source follower (SF) was added between the 1st and 2nd stages. We opt for a MOSFET instead of an HBT as a buffer due to its lower gate–source offset voltage ($V_{GS} \approx 0.5$ V) compared to the base–emitter offset voltage ($V_{BE} \approx 0.75$ V). This allows us to increase the resistive load R_{L1}, enhancing the gain of the first stage to suppress the noise of the output stage. As the temperature is lowered to CT (approximately 4 K in our design), a higher junction voltage is required to overcome the potential barrier at the B-C junction and enable forward biasing of both Q_1 and Q_3. In addition, incorporating resistive feedback is critical in maintaining stable voltages at nodes A and F, compensating for temperature and supply voltage variations. This is essential to ensure that the transistors remain correctly biased and the LNA functions effectively, even in cryogenic environments. To achieve this, we extracted the static SPICE models based on the findings presented in [16]. These models were carefully investigated to ensure that the circuit maintains the required biasing conditions at CT. Fig. 3 illustrates the anticipated static voltages at CT. It demonstrates that maintaining V_{DD} above 1.65 V results in voltage at the source of M_1 (V_F) exceeding 0.95 V, thereby enabling proper biasing of the amplifying HBTs Q_1 and Q_3 in the first and second stages within the forward active region, as well as M_1 of the SF buffer, in the saturation region. Thus, the resistive feedback biasing system retains the quiescent operating points of the LNA, even when the operating temperature decreases to 4 K. The low-power LNA designs described in [9] and [17] operate with a low collector-to-emitter voltage ($V_{CE} = 0.2$ V) to be able to reach lower supply voltages. However, this reduction in V_{CE} causes bipolar transistors to operate in the deep saturation region, which can adversely impact the linearity of the LNA. As mentioned in Section I, ensuring linearity is crucial for keeping the shape and timing of the amplified signal when readout of the ultra-thick SNWDs or readout using amplitude multiplexed technique. In the presented design, the transistors Q_1 and Q_3 are biased with a collector-to-emitter voltage (V_{CE}) of approximately 0.8 V at RT and 0.95 V at CT to enhance the amplifier's linearity. A higher V_{CE} also results in a lower collector–emitter transconductance (g_o) and thus noise. The simulated static current of every stage and the total LNA current consumption at CT are highlighted in Fig. 3(b). With a significant increase in transconductance by approximately five times at CT, the current consumption of the first and second stages could be effectively reduced from 8 to 2.8 mA and from 3.6 to 1.5 mA, respectively. This reduction in current consumption necessitated a supply voltage of 1.8 V, leading to V_F of approximately 1 V at CT.

The small-signal equivalent circuit of the LNA is illustrated in Fig. 4, which is used to analyze the LNA's scattering parameters and noise figure. By considering the circuit component values and the extracted small-signal parameters obtained from SPICE simulations, as shown in Tables I and II, respectively, one can derive the dc gain of the amplifier. According to the current–voltage feedback theory, the overall LNA voltage gain at dc can be expressed as [18]

$$A_{\text{total,DC}} = \frac{G_{m3} R_{F1} R'_{L2}}{R_s \left(1 + \frac{R_{F1} + R_{\text{in0}}}{G_m \beta_1 R'_D R_{L1}}\right)}. \quad (6)$$

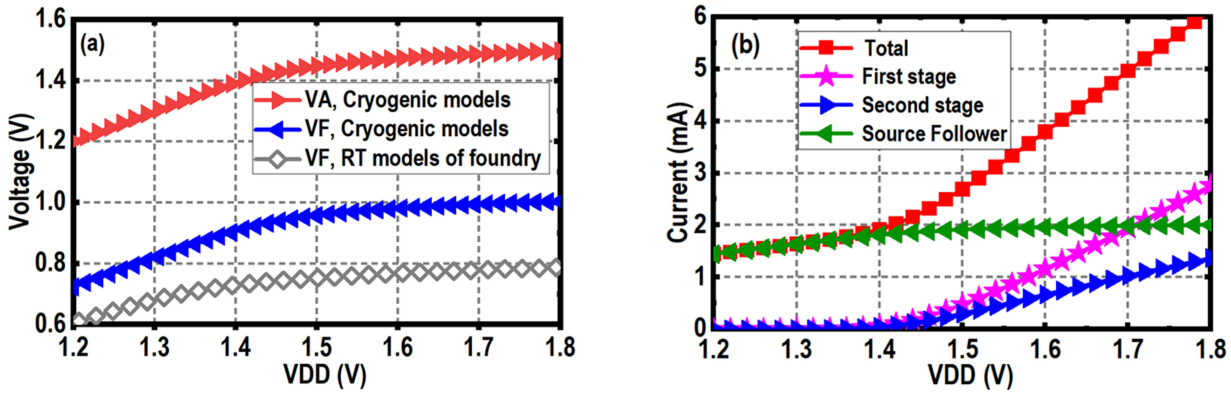

Fig. 3. Anticipated statics of the voltage and current variation versus the supply voltage using the cryogenic static models. (a) Voltages. (b) Currents.

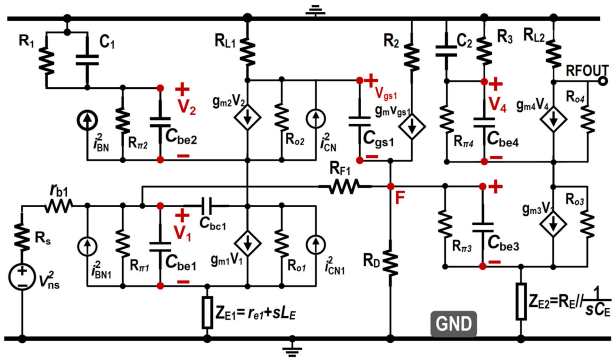

Fig. 4. Small-signal models for noise and scatter parameter analysis.

TABLE II
SMALL-SIGNAL MODEL PARAMETERS ADAPTED FOR CIRCUIT DESIGN AT CT

	Q_1					Q_2		Q_3		Q_4		M_1	
Para.	C_{be1} (fF)	C_{bc1} (fF)	g_{m1} (mS)	r_{e1} (Ω)	r_{b1} (Ω)	C_{be2} (fF)	g_{m2} (mS)	C_{be3} (fF)	g_{m3} (mS)	C_{be4} (fF)	g_{m4} (mS)	C_{gs} (fF)	gm (mS)
RT	271	66	280	1.6	3.2	65	212	150	123	67	120	23	20
CT	152	42	350	1.1	2	25	252	106	215	47	200	12	70

The effective transconductance of transistor Q_3 is denoted as $G_{m3} = g_{m3}/(1 + g_{m3}R_E)$. The equivalent dc gain of the source follower is $G_m R'D = g_{m3}R'D/(1 + g_{m3}R_E)$. Furthermore, the approximate equivalent input resistances for stages 1 and 3 are expressed as $R_{\text{in0}} \approx R_{\pi 0} + \beta_1 r_e$ and $R_{\text{in3}} \approx R_{\pi 0} + \beta_3 R_E$, respectively. Finally, the equivalent load resistances are given by the following expressions:

$$R'_{L2} = R_{L2}//R_{\text{Load}} \tag{7}$$

$$R'_D = R_D//R_{F1}//R_{\text{in3}}. \tag{8}$$

The input resistance is expressed as

$$R_{\text{in}} = \frac{R_{F1}R_{\text{in0}}}{R_{\text{in0}} + R_{F1} + G_m\beta_1 R'_D R_{L1}}. \tag{9}$$

Assume that the dc gain of the source follower is close to 1, and the input impedance can be expressed as

$$R_{\text{in}} \approx \frac{R_{F1}}{1 + \left(\frac{R_{F1}}{\beta_1} + R_{L1}\right)\cdot\frac{1}{r_e + r_b}} \approx \frac{R_{F1}(r_e + r_b)}{R_{L1}}. \tag{10}$$

To achieve input impedance matching ($S_{11} < -10$ dB) across the entire frequency range of operation without a significant circuit size increase, a small inductive emitter-degenerated slab inductor (L_E) was employed. In addition, double capacitive zero peaking structures were implemented to broaden the bandwidth. These structures were constructed implicitly by R_D and the parasitic capacitance at node F (C_F) and explicitly by $R_E - C_E$. By incorporating these design elements, the LNA achieves improved input impedance matching and a wider bandwidth while minimizing circuit size.

The small-signal circuit parameters are calibrated using the extracted and measured device characteristics given in [7] and [19] in order to examine the behavior of the LNA at CT. In essence, we found the scale factors of the parameters when the operating temperature decreased from 300 to 4 K RT to CT. We then adjusted the room temperature small-signal parameters by applying these scale factors while taking the transistor sizes into consideration, and the altered circuit parameters are presented in Table II. Substituting these parameters into the small-signal equivalent circuits leads to the simulated results displayed in Fig. 5, which illustrates a notable enhancement in the gain of the LNA, along with an expanded bandwidth achieved through the improved −3-dB cutoff frequency. This improvement can be attributed primarily to the lower parasitic capacitance of the device and the high quality factor of the capacitive peaking RC tanks at CT. While S_{11} experiences a slight degradation, it remains below −10 dB. The degradation is primarily observed at low frequency due to the decrease in r_{e1} and r_{b1} (Fig. 4) at CT, as depicted in (10) and Table II. Under the initial assumption that the high gain of the first stage (>14 dB) renders the noise from the second stage negligible, we can analyze the noise figure of the LNA by considering only the noise contribution of the first stage and the feedback network. Neglecting the impact of $R_{\pi i}$ and R_{oi}, we can express the noise factor (F) of the LNA using

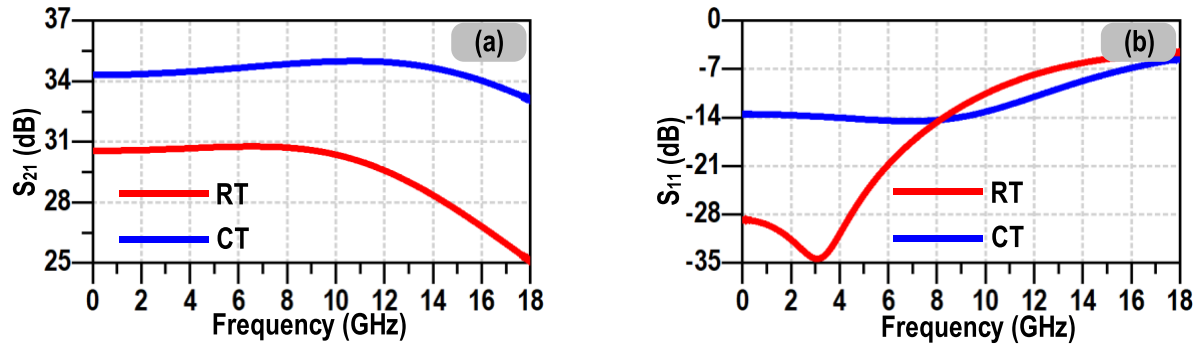

Fig. 5. Simulated scattering parameters of the LNA. (a) S21. (b) S11.

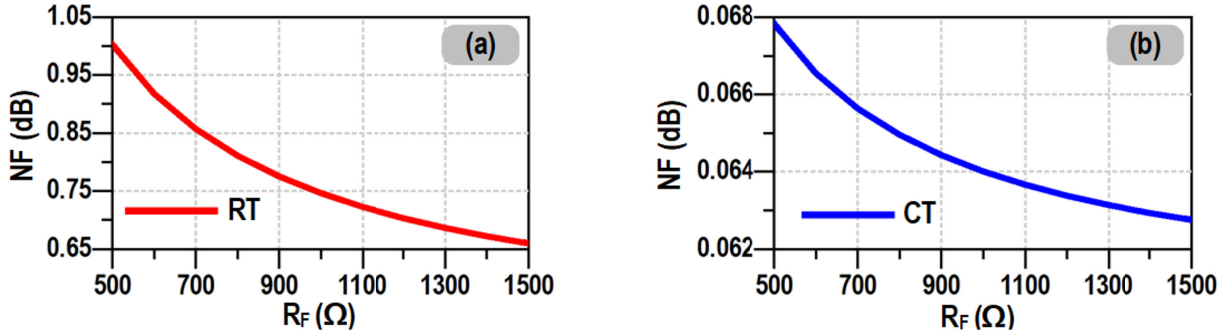

Fig. 6. Influence of R_F on NF at (a) RT and (b) CT.

the following equation:

$$F = 1 + \frac{T_{A,\mathrm{LNA}}}{T_{A,S}}\left(\frac{R_X}{R_s} + \frac{R_X R_s}{R_F^2} + \frac{R_s}{R_F} + \frac{g_{m1}R_s(|\beta(j\omega)|+1)}{2|\beta(j\omega)|^2}\right) \tag{11}$$

where $T_{A,S}$ represents the ambient temperature of the source and $T_{A,\mathrm{LNA}}$ is the ambient temperature of the LNA. The term R_X corresponds to the frequency-dependent current gain of Q_1 and is given by $(r_{e1} + r_{b1} + 1/g_{m1}) \cdot \beta(j\omega)$. To achieve a balance between S_{11} and F for room temperature (RT) operation, it is crucial to appropriately set the value of R_F. However, as the operating temperature decreases from the reference temperature of 290 to 4 K, the coefficient in the second term of (11) $T_{A,\mathrm{LNA}}/T_{A,S}$ scales down by approximately a factor of 18.6 dB, which can effectively suppress the noise contribution of the feedback resistor R_{F1}. Consequently, the noise induced by the resistive feedback network becomes less significant at cryogenic temperatures than at room temperature, as depicted in Fig. 6. Note that, for this LNA, we did not try to achieve the input noise matching over a wide bandwidth, relying on some inductors and capacitors to construct a matching network, which in fact sacrifices some of the noise performance in exchange for better low-frequency impedance matching and keeping the circuit area small.

IV. Implementation and Measurement of the Cryo-LNA

The LNA was designed on the IHP 130-nm BiCMOS process. Two concerns motivated using this process. For one thing, this process has been used to design cryogenic LNA with excellent noise performance under low power consumption. For another thing, we were able to obtain sufficient device cryogenic temperature test data from various literature to compute the cryogenic circuit simulation model. The current density of Q_1 ($48 \times 0.9 \times 0.07$ μm) at CT was set to around 0.9 mA/μm^2 to optimize the noise performance. A smaller area of Q_2 was set to lower the parasitic capacitance introduced at node X, thus reducing its noise contribution. The second stage was designed for a current density of 1.7 mA/μm^2, offering an optimum gain with minimized power. Since HBTs have a high ac current gain ($\beta \approx 800$), small-emitter degenerated resistors and inductors affect Z_{IN} significantly. Therefore, the implicit intrinsic emitter resistor of Q_1 (r_{e1}) was set to 1.2 Ω and a slab inductor with a low inductance ($L_E = 38$ pH) was used. Given the considerable impact of bonding wires, we laid out nine ground pads on the chip besides the ground-signal-ground (GSG) pads while designing a larger power supply pad to support multiwire bonding. This compact design results in a core area of 0.03 mm^2, and Fig. 7(a) shows that, including the GSG pads, the total area is 280×480 μm. The LNA's scattering parameters (both at RT and CT) and noise figure at RT were measured on-chip using the Lakeshore CRX-4K probe station, and the SOLT method was applied for calibration, where the calibration kit files are different for RT and CT. For testing the noise performance at CT, the chip was mounted on a Rogers 5880 substrate using bonding wires [Fig. 7(b)] and secured inside a brass cavity [Fig. 7(c)]. In order to minimize the influence of the bonding wires, we designed a rectangular hole in the PCB to place the LNA die so that the bonding

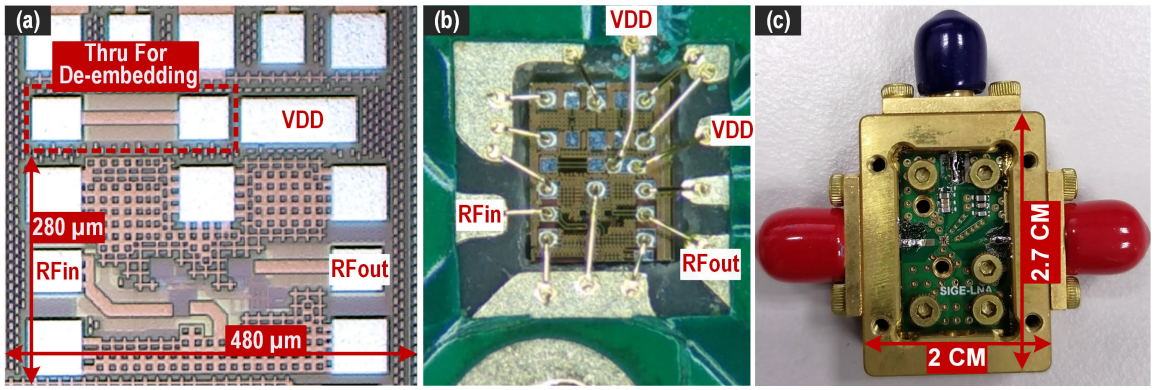

Fig. 7. (a) Fabricated LNA die micrograph. (b) Macro photograph of the wire bonding scheme. (c) Photograph of the LNA module.

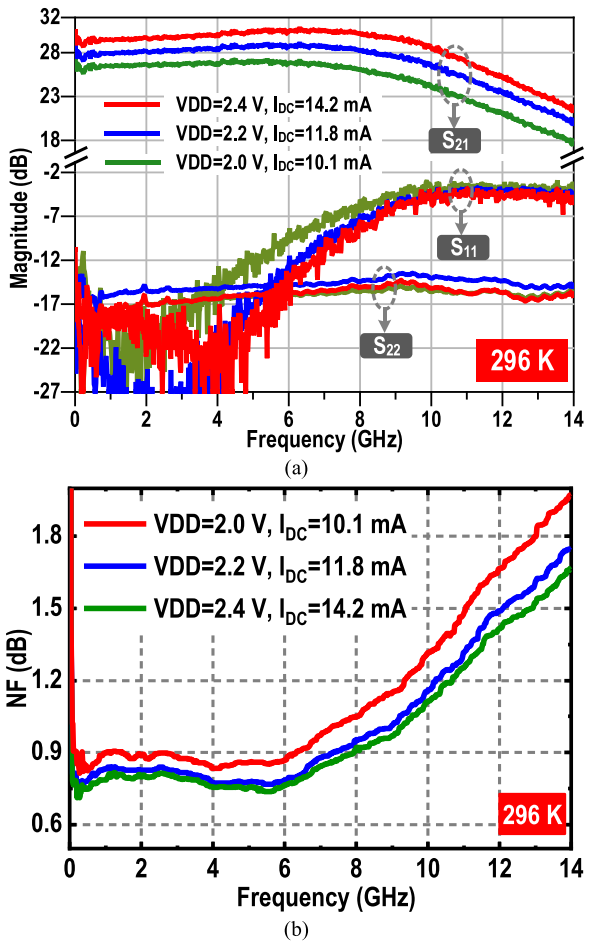

Fig. 8. On-chip measured results of (a) S-parameters and (b) NF of the LNA at 296 K.

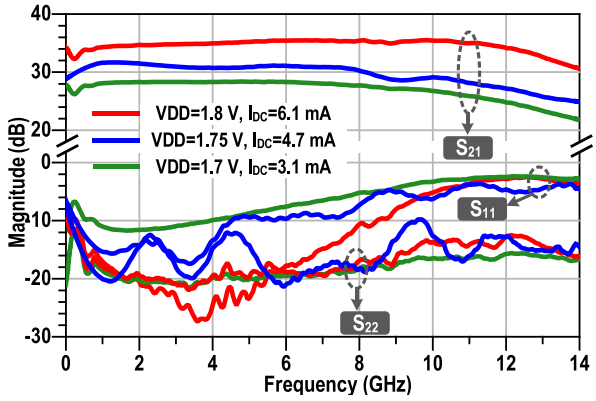

Fig. 9. On-chip measured S-parameter of the LNA at 3.6 K.

pads and the surface of the PCB are on the same level, which effectively reduces the length of the bonding wires. Also, the input and output microstrip lines are designed to be 50 Ω and are guaranteed to be as short as possible to avoid the impact introduced by the PCB.

Fig. 8(a) shows the on-chip measured S-parameters of the LNA at RT under various biasing conditions (V_{DD} = 2/2.2/2.4 V). The LNA's gain improves as the supply voltage (V_{DD}) increases. Specifically, for V_{DD} = 2.2 V, the S-parameter values show that S_{21} is greater than 28 dB with a maximum in-band variation of 2 dB, and S_{11} is less than −9 dB for frequencies below 8 GHz. This resistive port impedance can ensure the proper reset of the SNWD, thus effectively preventing any latching of the detector [20]. Fig. 8(b) illustrates the on-chip measured NF as a function of frequency at RT for three different voltage supplies. The plot demonstrates that the LNA maintains sub-1-dB NF (on-chip testing results) up to a frequency of 8 GHz under 2.4-V supply voltage. The cryogenic S-parameters were measured on-chip under different supply voltages, 1.7/1.75/1.8 V, and the results are shown in Fig. 9. As the supply voltage V_{DD} increases, the input matching improves, decreasing S_{11}. As described in (9) and Table II, at CT, the combined resistance of $(r_{b1} + r_{e1})$ decreases, resulting in a slight decrease in the input resistance (R_{in}) and leading to a higher S_{11} value. However, for higher values of V_{DD}, the current gain of Q_1 (β_1) increases sufficiently to compensate for this effect, resulting in improved impedance matching. Under typical biasing conditions of V_{DD} = 1.8 V and I_{DC} = 6.1 mA, the LNA demonstrated excellent input impedance matching (S_{11} < −10 dB) across the frequency range of 0.1–8.8 GHz. This indicates a significant improvement in input impedance matching at CT.

The NET measurement at CT was performed using the cold attenuator method [21], following the same biasing conditions.

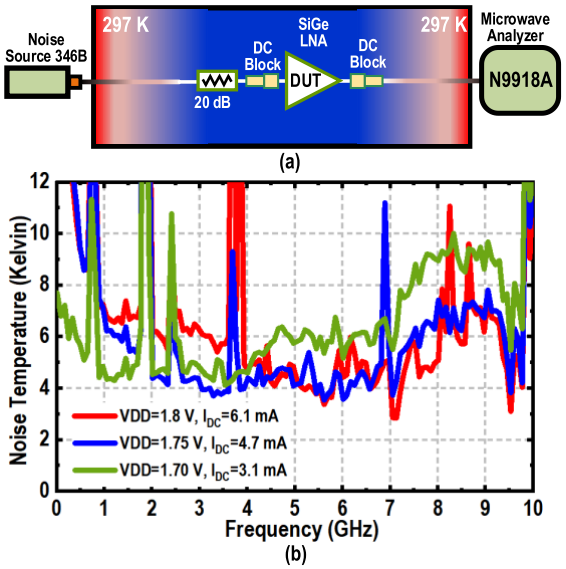

Fig. 10. (a) Setup to evaluate the NT of the LNA at 3.6 K. (b) Results.

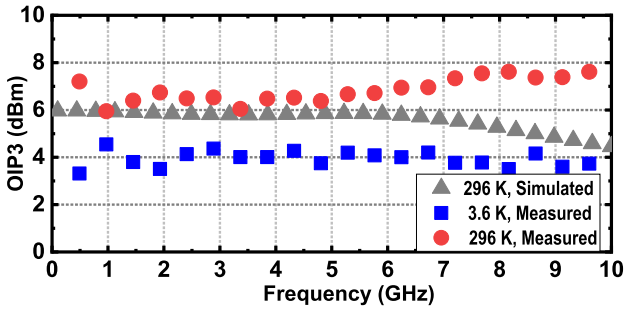

Fig. 11. OIP3s under $V_{DD} = 2.2$ V at 296 K and $V_{DD} = 1.8$ V at 3.6 K.

The experimental setup is depicted in Fig. 10(a), through the Keysight 346B as the cold/hot noise source and isolating the thermal noise with a 20-dB commercial attenuator. The effects of cables, attenuators, and adaptors were deembedded to obtain accurate noise temperature values. The LNA achieves an average NET of 5 K from frequency 0.1 to 6 GHz under $V_{DD} = 1.7$ V. As V_{DD} increases, the noise temperature degrades at low frequencies (<2 GHz) but improves at higher frequencies. The uncertainty of the NET mainly results result from: 1) the insertion loss (IL) of the attenuator errors; 2) the average physical temperature of the coaxial from the RT to the cryogenic sample holder of the cryostat (125 ± 25 K); 3) the noise excess-noise ratio (ENR) of Keysight 346B (15 ± 0.17 dB); 4) the physical temperature variations of the 20-dB attenuator (3.6 ± 0.1 K) and the noise source (296 ± 0.5 K); and 5) the port impedance mismatch. We can calculate the uncertainty of the NET test results as ∼±1.482 K.

The output third-order intercept point (OIP3) was measured using two-tone signals with 1-MHz spacing, and the results are plotted in Fig. 11. The output $P_{1\ dB}$ results at RT and CT were shown in Fig. 12, where $P_{1\ dB} > -7$ dBm in the operating band under 1.8-V power supply. The LNA's linearity at cryogenic temperatures is worse than that at room temperature

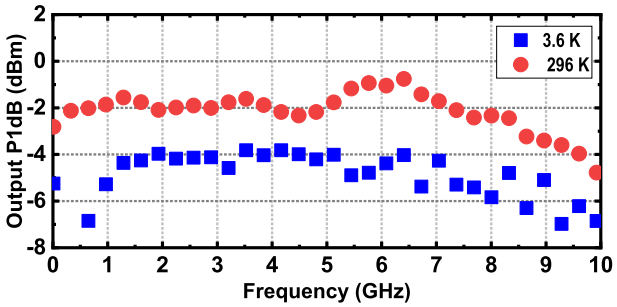

Fig. 12. OIP3s under $V_{DD} = 2.2$ V at 296 K and $V_{DD} = 1.8$ V at 3.6 K.

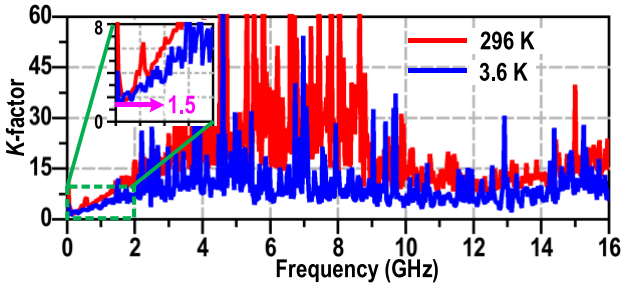

Fig. 13. K factors under $V_{DD} = 2.2$ V at 296 K and $V_{DD} = 1.8$ V at 3.6 K.

due to the significant increase in the slope of the collector current versus base voltage at CTs. However, it still reaches the design objectives and satisfies the SNWD readout application. The measurement of the K-factor allows for the assessment of the stability of the LNA. LNAs generally tend to be more susceptible to instability at lower frequencies. The LNA stability analysis is shown in Fig. 13, with a minimum value of 1.5 at about 100 MHz, suggesting that the cryogenic LNA is unconditionally stable at both CT and RT. Table III compares the LNA and the current state-of-the-art of the cryo-LNAs on CMOS process [23], [24], [25], InP HEMT process [26], [27], [28], [29], as well as on SiGe BiCMOS process [6], [26], [30], [31], [32]. The cryo-LNA demonstrates good performance in parameters, including operational bandwidth, input and output return loss, and circuit area. Moreover, $P_{1\ dB}$ is high enough to linearly amplify the SNWD output pulse to greater than 150 mV. Consequently, the LNA output can be fed directly to the comparator without further amplification.

V. Applications Results

A. SNWD Design

The proposed detector designed by Single Quantum (SQ) consists of a detector array comprising 32 pixels. Each pixel is connected to two sides, sharing a single ground. Each pixel in this configuration occupies an area of 20 × 20 μm. The nanowire within each pixel has a width of 100 nm, a thickness of 10 nm, and a meander pitch 8 (p) of 200 nm. Fig. 14 shows the die micrograph of such design.

First, the LNA is introduced into the 3.4 K stage, being closed to the detector and consequently demonstrating enhancements in various parameters through cooling, as illustrated in Section III. Subsequently, an investigation into the impact of different design parameters, such as noise

TABLE III
CRYOGENIC LNA PERFORMANCE COMPARISON

Ref.	Freq. (GHz)	T_{AMB}	NT (K)	Gain (dB)	S_{11} (dB)	OIP3 (dBm)	P_{1dB} (dBm)	VDD (V)	Power (mW)	Biasing Voltage No.	Offchip Comp.	Die area (mm^2)	Tech.
JSSC'21 [24]	4.6-8.2	4 K	15.8-46.8	39~44.8	<5.8	-3~0	-11.5~-9.5	1.4	39	4	NO	0.72	40nm CMOS
RFIC'22 [25]	5.9~8.4	4.1 K	37~40	10~13.4	<4	NG	NG	NG	2.57	2	NO	NG	14nm FinFET
RFIC'22 [26]	4.2~9.2	16 K	4.5~21.5	31.4~35	<-5.6	-6~2*	NG	0.8	21	3	NO	0.23	22nm FDSOI
EDL'20 [27]	4~8	5 K	4.1	20	NG	NG	NG	NG	0.112	NG	YES	NG	0.1 μm InP HEMT
TMTT'23 [28]	4~6	4 K	2	23.1	<-8.9	NG	-23.2	NG	0.2	4	YES	NG	0.1 μm InP HEMT
TMTT'18 [29]	0.3~14	4 K	3.5	41.6	<-5	NG	NG	0.8	12	2	YES	1.5	0.1 μm InP HEMT
TMTT'21 [30]	8~18	10 K	5~9.3	29.6~32.8	<-5	NG	NG	NG	19.6	6	NO	2.5	0.1 μm mHEMT
IMS'18 [31]	2~4	7 K	3.3~4	28	<-6.5	NG	NG	0.65	3	3	NO	0.6	130nm SiGe BiCMOS
IMS'19 [6]	0.4~1.2	16 K	3.3	30	<-7	NG	~-20	0.7/0.5	6.6	4	YES	1.32	130nm SiGe BiCMOS
IMS'17 [26]	4-8	18 K	8	26	<-7	NG	NG	0.4	1	3	YES	0.45	130nm SiGe BiCMOS
IMS'21 [32]	0.1~3	15 K	4.6~6	27~32	NG	NG	NG	0.4/0.2	0.96	4	YES	0.63	130nm SiGe BiCMOS
IMS'17 [33]	0.3-3	16 K	2.3	22	<-3	NG	NG	NG	32	3	YES	0.6	130nm SiGe BiCMOS
This work	**0.1~8.8**	3.6 K	4~10.5	**33~36**	**<-10**	3~5	-6.7~-3.8	1.75	8.2	1	NO	0.038	130nm SiGe BiCMOS

*IIP3 at RT.

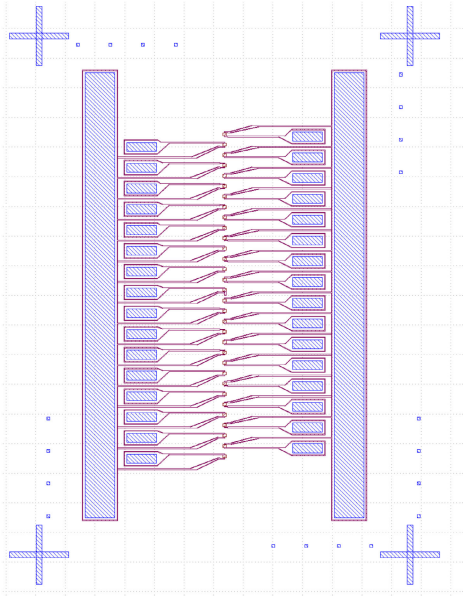

Fig. 14. Die micrograph of the 32-pixel SNWD array. Each pixel occupies an area of 20 × 20 μm in the center. On each side: 16 signal pads and a common large ground pad.

figure and bandwidth, is conducted to validate the analysis in Section II. A comparative study is carried out between the proposed design and a state-of-the-art cryogenic commercial LNA (CITLF1), focusing on jitter. Finally, a compact prototype that combines the SNWD and the SiGe LNA on a single PCB and operates at the lowest achievable temperature is validated.

B. SNWD Modeling

We modified the SPICE model proposed in [22] to integrate it into the SiGe low-noise amplifier (LNA) design framework. This adjustment ensured that the parameters elaborated in Section II resulted in an optimized pulse shape, consequently leading to an ideal balance between jitter and power. The bias current is set to 21 μA for the simulation and the measurements conducted at 3.4 K.

In Fig. 15, the experimental setup at cryogenic temperatures is depicted. The SNWD is mounted in a PhotonSpot cryogenic system, operated using a Cryomech PT415 pulse tube. The SNWDs are cooled to 880 mK and exposed to the laser beam via free-space coupling through ultraviolet windows. Mounted on the 4 K stage, the SiGe LNA and a commercial bias-tee (ZFBT-4R2G+) are coupled to the detector via short high-frequency cryogenic cables. This configuration minimizes pickup noise and heat transfer in contrast with the RT readout that is commonly used.

Fig. 16 illustrates that, in this context, the pulse rise time is primarily constrained by the detector's rise time of 350 ps due to the dimensions of the SNWD (20 × 20 μm). Notably, the cooling process proves more effective in minimizing noise power rather than significantly enhancing the rise time. For smaller detectors, as detailed in the upcoming analysis, exploiting the extended bandwidth of the proposed LNA can potentially drive jitter to even lower levels. At a temperature of 3.4 K, the LNA's gain experiences an enhancement, leading to a substantial increase in the signal-to-noise ratio (SNR). The pulse dead time, inherently dependent on the LNA's input impedance, shows minimal alteration. This highlights the stability of the LNA's input impedance even post-cooling, thereby ensuring a passive and accurate reset for the SNWD.

C. Timing Jitter

The setup in Fig. 17 is used for the timing jitter characterization of the SNWD pulse after the amplification through the SiGe LNA. A 40-GS/s, 13-GHz oscilloscope allows

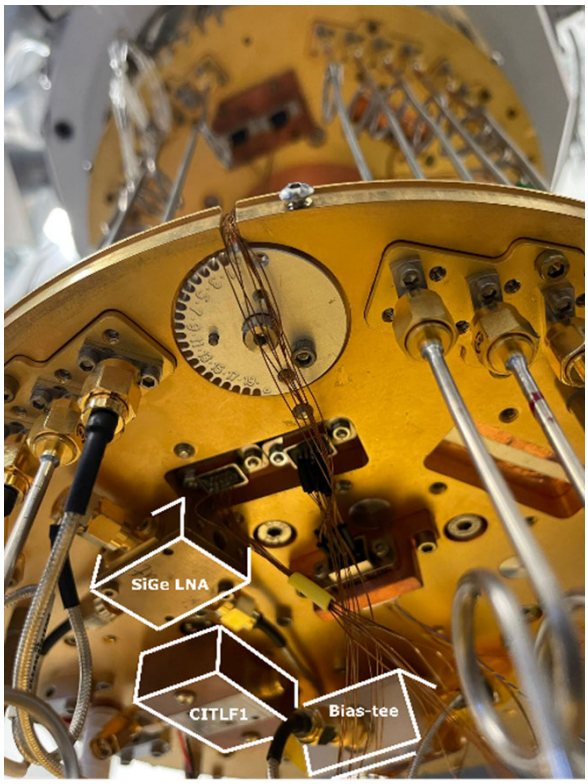

Fig. 15. Proposed SiGe CLNA, the commercial CLNA, and the bias-tee all mounted on the 3.4 K stage of the PhotonSpot cryogenic system.

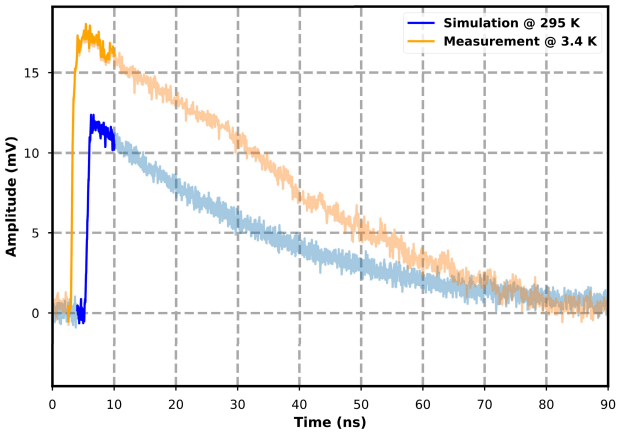

Fig. 16. Simulated chain output is represented in blue, using the SNWD Specter model on Cadence Virtuoso environment at 295 K. It is compared to the measured pulse at 3.4 K, visualized in orange.

us to determine the timing jitter of the detection chain. This evaluation consists of the accumulation of time difference between two triggers: detected photons through the entire chain containing the SNWD and LNA from one side and through the fast photodiode (Newport InGaAs) from another. The reference photodiode has a timing jitter significantly inferior to the detector's one, rendering it negligible for analytical purposes. The femtosecond pulsed laser (OneFive Origami 10, NKT) generates 150-fs width pulses at 1030-nm wavelength. One path of the generated emissions directly reaches the reference photodiode, while another beam portion undergoes second-harmonic generation (SHG) to convert it

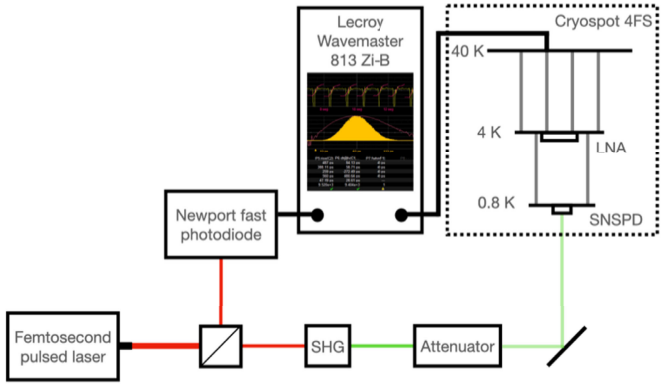

Fig. 17. Optical test setup of the characterization of the total chain jitter by means of time-correlated single-photon counting (TCSPC) acquisition.

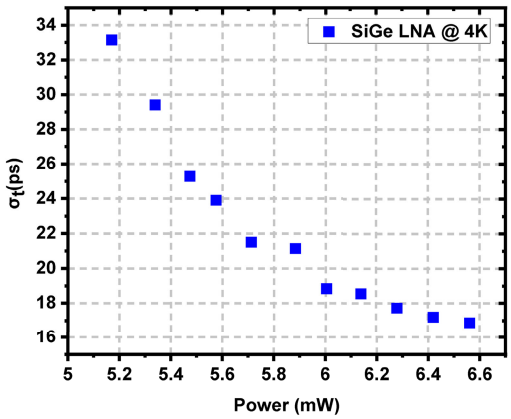

Fig. 18. Full chain jitter characterization when coupling the SNWD to the SiGe LNA at 4 K as a function of the LNA power consumption.

to 515 nm. This SHG-converted signal is subsequently attenuated before reaching the SNWD, ensuring operation within the single-photon regime.

Fig. 18 shows that the total standard deviation exhibits a quadratic decrease as LNA power increases under the assumption of constant bandwidth and output rise time. Given that the LNA's bandwidth remains unaltered during the power increment, this observation is consistent with (5), which illustrates the impact of noise factor reduction on timing jitter. A balance becomes crucial between the static power consumption of the LNA and the desired contribution to the timing jitter. An alternative approach to further decrease the LNA's jitter contribution involves maintaining a constant minimal noise factor while broadening its bandwidth. In the subsequent measurement, we emulate variations in bandwidth by coupling the LNA with a high-speed oscilloscope having a variable bandwidth, enabling an examination of its influence on the overall jitter.

The trace in black shows the excepted LNA jitter that is a product of the integrated thermal noise and the output pulse rise time. The first one ($\sqrt{\mathrm{BW}}$) increases much faster than the rise time (1/BW) as a function of the system bandwidth. One should mention that only the value of the solid line corresponds to the displayed jitter values, and all the dashed lines are normalized for demonstration purposes. The plot shows that for large detectors, where the output

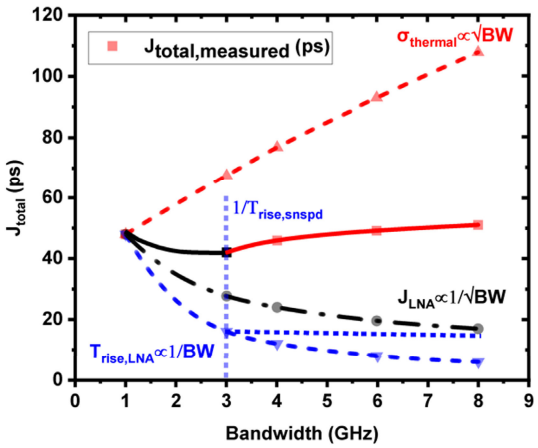

Fig. 19. Accumulated jitter across the entire chain (solid), measured at 3.4 K, is compared with the LNA jitter profile outlined in (5) (dashed).

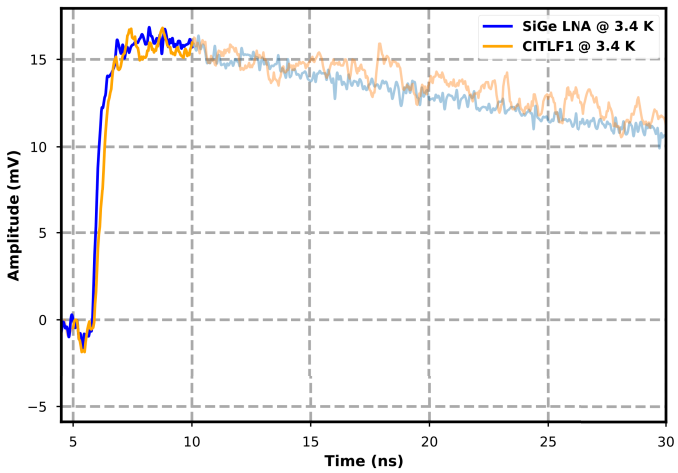

Fig. 20. Output pulse shapes measured at 3.4 K showing the effect of the LNA bandwidth on the rise time.

rise time is instead limited by $L_k/(R_L + R_N)$, increasing the LNA's bandwidth beyond the inverse of the SNWD's rise time increases the overall jitter. In our specific case, the SNWD has an intrinsic rise time of 350 ps, equivalent to an optimal bandwidth of approximately 3 GHz. The jitter measurement shown by the solid line in Fig. 19 shows that an inflection point of the jitter curve occurs around 3 GHz. In the proposed LNA design, the bandwidth is 6 GHz, and the rise time constraint is pushed toward the detector's side instead of the more commonly known scenario. One can rewrite (5) as

$$J_{\mathrm{LNA}} \approx \frac{\mathrm{NF}}{I_b \cdot R_L} \cdot \frac{\sqrt{\mathrm{BW}}}{\mathrm{BW}_{\mathrm{opt}}} \cdot \sqrt{4 \cdot k \cdot T_{\mathrm{AMB}} \cdot R_S} \times 0.824 \qquad (12)$$

where BW is the LNA bandwidth and $\mathrm{BW}_{\mathrm{opt}}$ is the optimal system bandwidth that can be approximated to $\min\{(R_L + R_N)/L_k, \mathrm{BW}\}$. It is essential to mention that, considering the detector's size, its contribution to jitter is not negligible. Consequently, the total measured jitter arises as a quadratic combination of the LNA and SNWD contributions.

A comparison is made between the SiGe LNA and a state-of-the-art commercial SiGe cryogenic LNA CITLF1 [23], which features a −3-dB cutoff frequency of 1.5 GHz, along with a noise temperature that linearly increases from 4 K at 1 GHz to 6.5 K at 3 GHz. Both amplifiers are mounted in the 4 K stage, as shown in Fig. 15. The pulse shapes of the respective amplifier outputs are presented in Fig. 20. Notably, the SiGe LNA exhibits a rise time of 350 ps, primarily constrained by the detector size. Conversely, the CITLF1 showcases a rise time of 600 ps, predominantly limited by bandwidth. The results of the jitter characterization for the same SNWD device, biased at approximately 21 μA, are illustrated in Fig. 21. The commercial amplifier shows a full-width at half-maximum (FWHM) of 54 ps, requiring a nominal power of 26.5 mW at 4 K. In contrast, the proposed SiGe design achieves an FWHM value of 42 ps while consuming only 6.5 mW at 4 K. This is because the bandwidth of the CITLF1 is lower than the optimal bandwidth in (12), which is 3 GHz, despite its low noise figure.

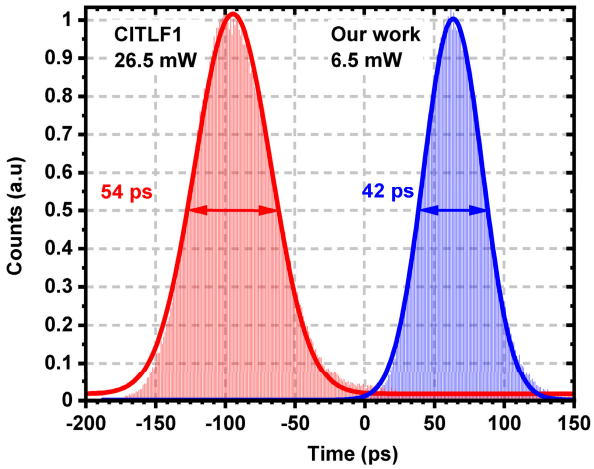

Fig. 21. Total chain jitter measured by means of time-correlated single-photon counting (TCSPC) acquisition method using the same SNWD. This measurement highlighted the low-power and low-jitter contribution of the proposed SiGe LNA, comparison to the commercial SiGe amplifier CITLF1.

D. Scalability Test

The SNWDs and the SiGe LNAs were integrated on the same PCB. The prototype PCB was designed using the RO4350 substrate, which offers reduced signal loss. The dimensions of the PCB are 65 × 32 mm, as illustrated in Fig. 22. It is mounted within the base shielded stage, with all signals (SNWD bias, amplifier supply, and pixel outputs) transmitted via coaxial cables to the output. The PCB features eight pixels, with integrated SiGe LNAs and the SNWD die. The bottom left image displays the wire-bonded compact SiGe LNA die, which is double-bonded to enhance stability. The bottom-right image showcases the wire-bonded Single Quantum SNWD die connected to the prototype PCB.

In the first scenario, a pixel with low critical current (I_c) was used, and the SNWD was positioned at a considerable distance from the amplifier supply connector. Conversely, a high critical current SNWD was used in the second scenario, and the SNWD was placed near the supply connector, specifically Pixel 1. Operating the amplifiers at low supply voltages minimizes device heating and ensures amplifier stability. However,

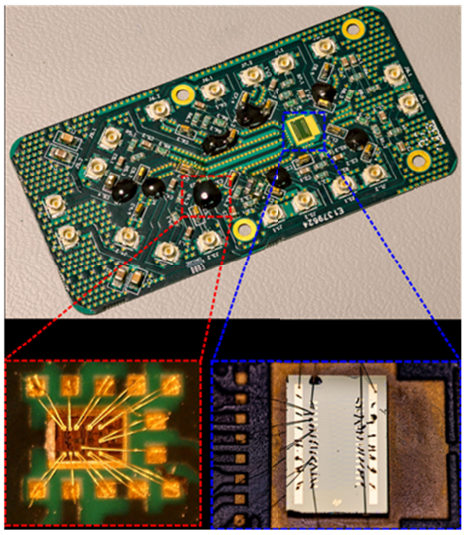

Fig. 22. Cryogenic prototype PCB for the integration. Top: eight pixels PCB with integrated SiGe LNAs and the SNWD die. Bottom left: wire-bonded compact SiGe LNA die with double bonding to enhance stability. Bottom right: single quantum SNWD die wire-bonded to the prototype PCB.

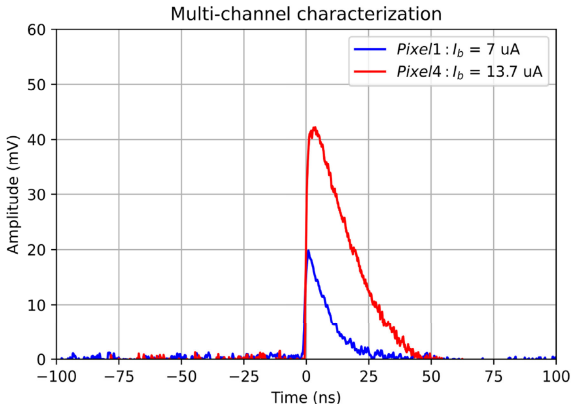

Fig. 23. Cryogenic integration prototype outputs using $V_{DD} = 1.65$ V for two extreme cases, Pixels 1 and 4.

TABLE IV

SNWD CHARACTERIZATION RESULTS AT 3.8 K WHEN COUPLED TO THE SiGe LNA ON THE SAME PCB

Pixel number	I_c (μA)	R_{SNWD} (×10^6 Ω)
1 #	9.0	0.076
4 #	15.1	9.3

increasing the distance between the pixel and the supply connector may introduce a voltage drop, potentially reducing amplifier gain. It is crucial to assess this effect, particularly for Pixel 4. The critical current measured under these conditions was 13.7 μA for Pixel 4 and 8.7 μA for Pixel 1. The two pixels characteristics are summarized in Table IV. To further increase the LNA gain, a line driver is employed at RT, and the resulting pulses are depicted in Fig. 23. The pulse waveforms demonstrate that the SNWD operates appropriately and does not exhibit latching even when positioned close to the SNWD. However, due to the variation in critical current among the array pixels, there may be some deviation in the amplitudes of the output pulses. This deviation can lead to time-walk effects, especially in high-timing resolution applications. As mentioned in the previous sections, this effect is minimized by making the rise time faster and will be more predominant when large arrays of detectors are explored. When scaling up the number of pixels, crosstalk is a concern. However, we mitigate potential interference between neighboring readout lines by avoiding capacitive coupling. In addition, rapid SNSPD reset within the 100-ps range effectively limits thermal crosstalk, preventing temperature rise that could impact the performance of adjacent SNWD pixels.

VI. CONCLUSION

This study presents a comprehensive analysis of the design and implementation of a cryogenic BiCMOS SiGe LNA. The LNA incorporates two cascode stages: a CMOS interstage common-source buffer and a resistive shunt–shunt feedback. The measurement results demonstrate that the LNA achieves an average NET of ∼5 K and >10-dB input and output return loss over the frequency range of 0.1–8.8 GHz with a power consumption of 8.2 mW. The cryo-LNA features: 1) an ultrawide operational bandwidth; 2) a compact footprint; 3) a single power supply voltage; 4) a reasonably low NET; and 5) a high $P_{1\ dB}$, which renders it well suited for readout of large-scale SNWD array. To achieve optimal readout performance tailored to specific applications, we analyzed the impact of low-noise amplifier (LNA) specifications on the readout timing jitter of the SNWDs. The analysis was experimentally verified by utilizing the designed wideband cryo-LNA, as well as a commercial LNA with a narrower bandwidth. Furthermore, the integration of the cryogenic SiGe LNA dies in close proximity to the SNWDs was also demonstrated. The measurement results suggest that this integration, without any adverse effects on normal behavior and reset mechanism for the detectors, can enhance the timing performance of the entire detection chain.

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