X-HEEP: An Open-Source, Configurable and Extendible RISC-V Microcontroller for the Exploration of Ultra-Low-Power Edge Accelerators

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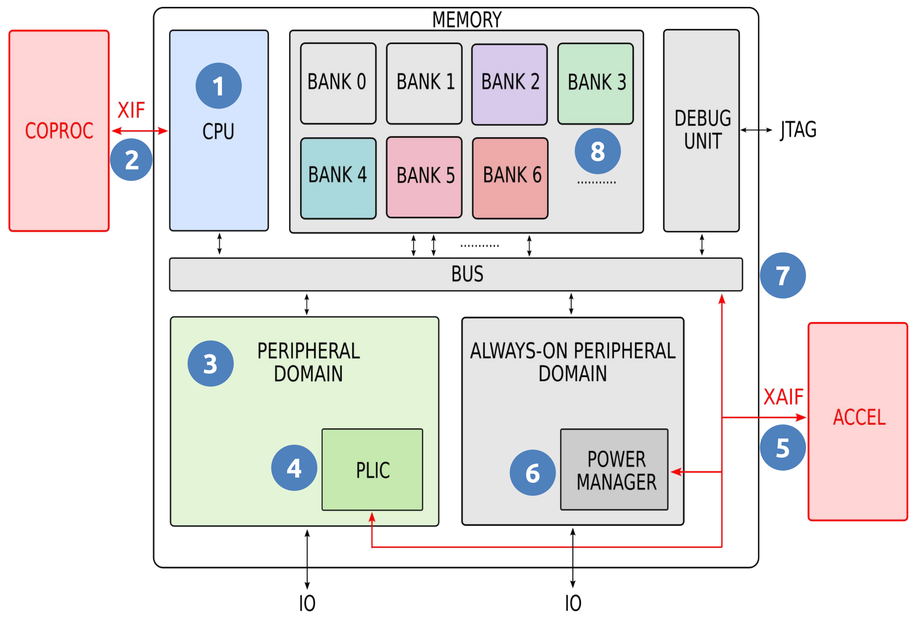
X-HEEP: eXtendible Heterogeneous Energy Efficient Platform

Configurable and Extendible Architecture



1 **Configurable RISC-V core:**

- cv32e20 [1]
- cv32e40p [2]
- cv32e40x [3]

2 **XIF:** configurable interface to plug in coprocessors

3 **Configurable peripherals:**

- DMA
- GPIO
- UART
- I2C
- SPI
- ...

4 **PLIC:** configurable platform interrupt controller

5 **XAIF:** configurable interface to plug in accelerators

6 **Configurable power manager:**

- Clock-gating
- Power-gating
- RAM retention

7 **Configurable bus topology:**

- One-at-a-time
- Fully-connected

Configurable bus addressing:

- Contiguous
- Interleaved

8 **Configurable number of memory banks**

[1] Low-power, 32-bit, in-order RISC-V core with a 2-stage pipeline that implements RV32[E|I][M]C instruction set architecture.
[2] High-performance, 32bit, in-order RISC-V core with a 4-stage pipeline that implements RV32IMFC[Xpulp] instruction set architecture.
[3] High-performance, 32-bit, in-order RISC-V core with a 4-stage pipeline that implements the RV32[I,E][M|Zmmul][A]Zca_Zcb_Zcmp_Zcmt[Zba_Zbb_Zbs|Zba_Zbb_Zbc_Zbs]ZicntrZihpmZicsrZifencei[X] instruction set architecture and offers extensions through the CORE-V-XIF interface.

Design Flow Support

CONFIGURATION → SystemVerilog templates

Automatic tools to configure the RTL code of X-HEEP thanks to customizable parameters

SW IMPLEMENTATION → HAL and FreeRTOS

- Includes an hardware abstraction layer (HAL) for easy access to peripherals' functionalities
- Supports FreeRTOS to enable concurrent execution and enhance resource management

SIMULATION AND HW IMPLEMENTATION → FuseSoC

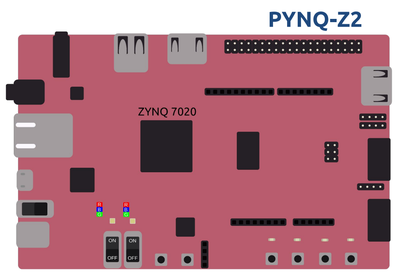
Automatic tool to generate the required script to simulate and implement the design

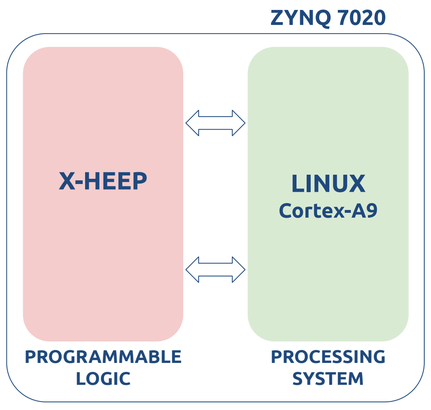
Supported tools:

- **Simulation:** Verilator, Questasim, etc.
- **ASIC:** Design Compiler, Innovus, etc.
- **FPGA:** Vivado, etc.

FPGA: Fully-virtualized Platform for Healthcare Applications

Implementation and Features





IMPLEMENTATION → Zynq 7020 on Pynq-Z2 board

X-HEEP implemented on the programmable logic side communicates with the Linux system on the processing system side

FULL VIRTUALIZATION → No off-board I/O connectivity required

All peripherals virtualized under Linux

Examples: JTAG virtualized towards Linux GPIOs, **UART** virtualized towards a Linux serial port, **FLASH** virtualized on the board DRAM, etc.

ESTIMATIONS → Performance and energy

- **Performance estimation** through dedicated performance counters
- **Energy estimation** based on TSMC 65nm CMOS technology

USER INTERACTION → Jupyter notebook

Dedicated Python class to support interaction through Jupyter notebook

Useful Links

Open-source Repositories

X-HEEP | FPGA-HW | FPGA-SW

X-HEEP → Main repository of X-HEEP

https://github.com/esl-epfl/x-heep

FPGA → Repositories of the FPGA emulation platform

https://github.com/esl-epfl/x-heep-femu

https://github.com/esl-epfl/x-heep-femu-sdk

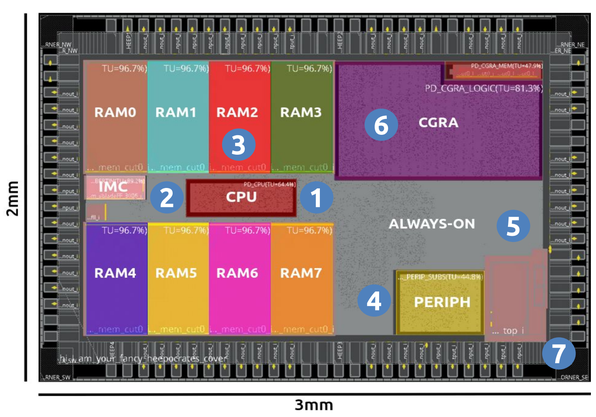
HEEPOCRATES: X-HEEP-based Chip for Healthcare Applications

Post-PnR Layout and Silicon Characterization

1 **cv32e20 core**

2 **In-memory computing (IMC) accelerator [4]**

3 **8 x 32 KB of SRAM banks**



Tech	TSMC 65 nm LP CMOS
Area	6 mm2
Voltage range	0.8 V – 1.2 V
Freq range	32 kHz – 470 MHz
Power range	230 uW – 48 mW

4 **All available peripherals in place**

5 **Fully-connected bus with contiguous addressing**

7 **12 power domains**

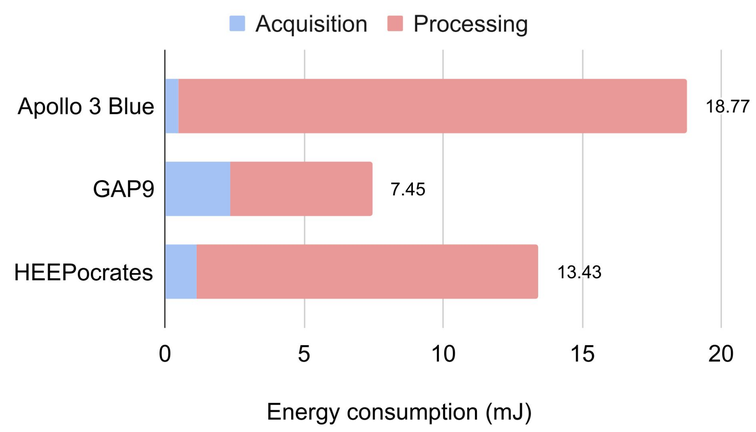
6 **Coarse-grained reconfigurable array (CGRA) accelerator [5]**

[4] William Andrew Simon, Yasir Mahmood Qureshi, Marco Rios, Alexandre Levisse, Marina Zapater, and David Atienza. 2020. Blade: an in-cache computing architecture for edge devices. IEEE Transactions on Computers, 69, 9, 1349–1363.
[5] Loris Duch, Soumya Basu, Rubén Braojos, David Atienza, Giovanni Ansaloni, and Laura Pozzi. 2016. A multi-core reconfigurable architecture for ultra-low power bio-signal analysis, 416–419.

Energy Consumption

APPLICATION → EEG Seizure Detection [6]

Convolutional neural network (CNN) used to detect seizures in electroencephalography (EEG) signals.



[6] Catalina Gómez, Pablo Arbeláez, Miguel Navarrete, Catalina Alvarado-Rojas, Michel Le Van Quyen, and Mario Valderrama. 2020. Automatic seizure detection based on imaged-eeg signals through fully convolutional networks. Scientific reports, 10, 1, 1–13.