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Fourier-Based Harmonic Control of Plug-and-Play Active Filters for Input-Series/Output-Parallel Solid-State Transformers

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***Abstract*—Solid-State Transformers with Input-Series/Output-Parallel configuration represent a convenient solution for AC/DC conversion, thanks to their scalability and modularity. As known, each module of the ISOP converter is affected by a second-order harmonic ripple caused by a local single-phase AC/DC conversion. This ripple can be neutralized by installing active filters, removing the need to oversize the DC-bus capacitances. However, standard controls for such active filters are based on measuring the AC side electrical variables, which can make them impractical to be installed in pre-existing configurations. This work presents a control algorithm for active filters that does not require any external measurement, and that is therefore suited for a Plug-and-Play installation in a pre-existing ISOP converter, without additional sensoring or control hardware modifications. To comply with the complex dynamics generated in the ISOP configuration, the proposed approach is based on a real-time Fourier decomposition, that allows precise and selective real-time control of the second-order harmonic using standard proportional-integral controllers and a decoupling network. The approach is particularized and validated experimentally with a single-phase ISOP SST, showing satisfactory performances.**

***Index Terms*—Input-Series/Output-Parallel (ISOP), Solid-State Transformer (SST), Active filters, Second-Order Harmonic suppression, Fourier-based harmonic control.**

I. Introduction and Background

SOLID State Transformers (SSTs) are a promising solution for efficient, reliable, and flexible power conversion in various applications, including renewable energy integration, industrial uses, and traction [1]–[5]. They combine the benefits of conventional power transformers (e.g., voltage/current scaling, galvanic insulation, etc...) with enhanced controllability and increased flexibility offered by power electronics. The Input-Series/Output Parallel (ISOP) SST architecture has gained significant attention due to its scalability and modularity, being able to offer high voltage ratings at the primary side and high current ratings at the secondary side by properly combining multiple identical conversion modules [1].

An ISOP SST can be conveniently employed for AC/DC conversion, and in this case each module typically incorporates a dedicated single-phase AC/DC conversion stage. However, as known, their operation introduces a power oscillation at twice the AC line frequency [6], that could adversely affect the DC-bus voltage of each module. In single-phase configurations, this may even propagate to the secondary side of the overall converter [4], [5], [7].

The mitigation of the second-order harmonic can be achieved through large capacitor banks or LC trap filters, but these solutions would lead to increased system bulkiness, impacting size, weight and power density of the SST. An alternative solution is represented by Active Power Filters (APFs): additional conversion structures purposely designed and controlled to counteract the second-order harmonic ripple [6], [8]–[10]. In presence of active filters, the DC bus capacitors of the ISOP SST modules do not need to be sized for the second-order harmonic ripple suppression, and therefore they can be reduced to improve the system compactness [7]. While the use of active filters has found applications in both single-level [6], [8]–[10] and multilevel converters [11], [12], their employment for SST configurations is still very limited.

Conventional control algorithms employed in active filters rely on locally neutralizing the power ripple generated by the AC/DC conversion stage. This is typically achieved by computing the ripple based on the AC line voltage and current measurements [7], while additional closed-loop controls are only used as a slow steady-state support for the feed-forward action [8], [9], [11]. However, this requires all active filters to have access to AC line measurements, which may be inconvenient for installations into a pre-existing system.

This work investigates the development of a closed-loop control algorithm for the active filters that would be entirely based on internal variables, without any need for external measurements or communication. This would make the active filters suitable for a plug-and-play implementation on a pre-existing ISOP SST. The solution provided in this work is an harmonic controller based on a real-time Fourier decomposition. Compared to other control strategies for active filters including a closed-loop resonant control [8], [11], with the proposed approach the second-order harmonic variables of the system can be analyzed through their time-varying coefficients and, similarly to a dq transformation in a three-phase AC system, they can be decoupled and independently controlled as DC variables. Therefore, both the dynamic performances and the stability margins of the second-order harmonic controller can be easily assessed through simple and known tools of control theory. This helps in simplifying the tuning of the controllers, which is especially beneficial in ISOP SST configurations because of the complex dynamics arising from the coupling of multiple modules [13].

II. Mathematical Model

A. Equivalent Model of an ISOP SST Module

The analyzed architecture is an ISOP SST composed of N identical modules, as represented in Fig.1. Each module comprises a single-phase AC/DC stage, a DC-bus capacitor, an isolated DC/DC stage and an active filter.

To guarantee a proper dynamic control of the second-order harmonic, the mathematical model of the DC-bus equivalent behavior of an ISOP SST cell must be established.

By focusing on a single cell, and by applying Kirchhoff's voltage law, the dynamic of the DC-bus voltage v_{DC} is:

$$C_{DC}\frac{\mathrm{d}v_{DC}}{\mathrm{d}t} = i_{AC/DC} - i_{DC/DC} - i_{APF} \tag{1}$$

where $i_{AC/DC}$ is the current injected into the DC bus by the AC/DC conversion stage, $i_{DC/DC}$ is the current absorbed by the DC/DC conversion stage, and i_{APF} is the current absorbed by the active filter (as represented in Fig.1).

In the linear approximation, both $i_{AC/DC}$ and $i_{DC/DC}$ can be replaced by their Norton equivalents, characterized by a current source and an equivalent shunt impedance. In this case, it is important to point out that the Norton equivalent of both the AC/DC and of the DC/DC conversion stages are characterized by a current source that includes a second-order harmonic component. Indeed, for an ISOP configuration, a second-order harmonic current component could not only be introduced by the AC/DC conversion stage of the same module, but can be also propagated from other modules through the DC/DC interfaces [13]. Similarly, the equivalent shunt impedance of the Norton equivalents should not be limited to the parameters of a single module, but should also consider the contribution of the other SST modules.

Finally, in the equivalent circuit, the active filter can be modeled as a controllable current source. Through a proper control, its aim is to neutralize the ripple voltage generated on the DC bus, mimicking the effect of a trap filter.

By grouping the modeled current sources and impedances, (1) can be analyzed in the Laplace domain as:

$$V_{DC}(s) = Z_{DC}(s)\cdot\left[I_{DC}(s) - I_{APF}(s)\right] \tag{2}$$

where $Z_{DC}(s)$ and $I_{DC}(s)$ are the equivalent impedance and the equivalent current source seen at the DC bus terminals of the module. They take into account the contribution of both the DC bus capacitor (whose impedance is $Z_{C_{DC}}(s) = 1/sC_{DC}$) and of the Norton equivalents of the other conversion stages. Fig.1 shows a simplified scheme on how to derive the equivalent circuit corresponding to (2).

B. Dynamic Model of Time-Varying DC-Bus Harmonics

To analyze the dynamic evolution of specific harmonic components of interest, the variables in (1) can be expressed as Fourier series in a moving time window of width T_0.

As an example, the DC-bus voltage can be decomposed as:

$$\begin{aligned} v_{DC}(t) &= v_{DC}^{\langle 0\rangle}(t) + \cdots \\ &\cdots + \sum_{h=1}^{+\infty}\left[v_{DC,\mathrm{c}}^{\langle h\rangle}(t)\cos(h\omega_0 t) + v_{DC,\mathrm{s}}^{\langle h\rangle}(t)\sin(h\omega_0 t)\right] \end{aligned} \tag{3}$$

where $\omega_0 = 2\pi f_0 = 2\pi/T_0$ denotes the fundamental angular frequency of the Fourier decomposition, $v_{DC}^{\langle 0\rangle}$ is the moving average of v_{DC}, while $\left\{v_{DC,\mathrm{c}}^{\langle h\rangle}, v_{DC,\mathrm{s}}^{\langle h\rangle}\right\}$ denote the instantaneous value of the cosine and sine components of the h-th order harmonic of v_{DC}, respectively.

The coefficients of the time-varying Fourier decomposition (3) are expressed through the Fourier integrals in the moving time window $[t - T_0, t]$:

$$v_{DC}^{\langle 0\rangle}(t) = \frac{1}{T_0}\int_{t-T_0}^{t} v_{DC}(\tau)\,\mathrm{d}\tau \tag{4}$$

$$v_{DC,\mathrm{c}}^{\langle h\rangle}(t) = \frac{2}{T_0}\int_{t-T_0}^{t} v_{DC}(\tau)\cos(h\omega_0\tau)\,\mathrm{d}\tau \tag{5}$$

$$v_{DC,\mathrm{s}}^{\langle h\rangle}(t) = \frac{2}{T_0}\int_{t-T_0}^{t} v_{DC}(\tau)\sin(h\omega_0\tau)\,\mathrm{d}\tau \tag{6}$$

and the magnitude of the h-th order harmonic component can be computed from the sine and cosine components as:

$$v_{DC}^{\langle h\rangle}(t) = \sqrt{\left(v_{DC,\mathrm{c}}^{\langle h\rangle}(t)\right)^2 + \left(v_{DC,\mathrm{s}}^{\langle h\rangle}(t)\right)^2} \tag{7}$$

The same time-moving Fourier decomposition as in (3)-(7) can be also applied to i_{DC} and i_{APF}.

When the system is in steady-state operating conditions with period T_0, the results of (4)-(7) are constant, and coincide with the coefficients of a classic Fourier analysis of periodic signals. However, in dynamic conditions, these coefficients are time-varying signals, which can be analyzed through standard tools of linear system analysis.

By choosing $T_0 = T_{AC}$, the second-order harmonic of interest is found by setting $h = 2$. Then, by applying the frequency shift properties of the Laplace transform, the dynamic relationship between the time-varying coefficients of the DC-bus voltage (i.e., $\left\{v_{DC,\mathrm{c}}^{\langle 2\rangle}, v_{DC,\mathrm{s}}^{\langle 2\rangle}\right\}$) and the time-varying

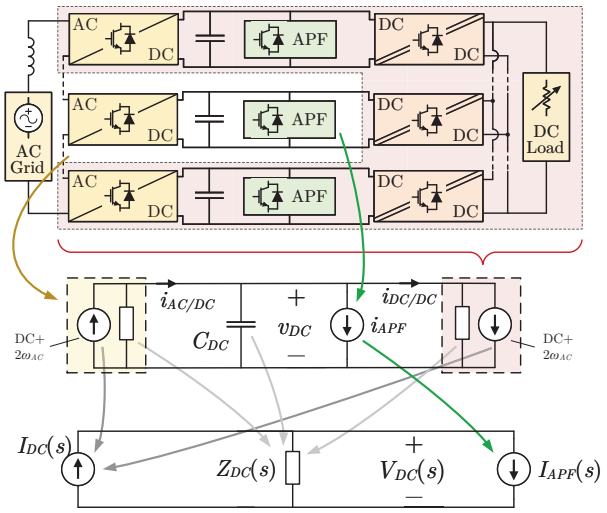

Fig. 1. Procedure to derive the equivalent DC-bus circuit of an ISOP module. The circuit needs to explicitly consider both the effect of the AC/DC conversion stage and of the mutual interaction with the other SST modules, that propagates through the DC/DC conversion stage.

coefficients of the DC-bus currents (i.e., $\{i^{\langle 2\rangle}_{DC,\mathrm{c}}, i^{\langle 2\rangle}_{DC,\mathrm{s}}\}$ and $\{i^{\langle 2\rangle}_{APF,\mathrm{c}}, i^{\langle 2\rangle}_{APF,\mathrm{s}}\}$) is represented in the Laplace domain by the coupled two-inputs/two-outputs system:

$$\begin{bmatrix} V^{\langle 2\rangle}_{DC,\mathrm{c}}(s) \\ V^{\langle 2\rangle}_{DC,\mathrm{s}}(s) \end{bmatrix} = \begin{bmatrix} Z^{\langle 2\rangle}_{DC,\mathrm{cc}}(s) & Z^{\langle 2\rangle}_{DC,\mathrm{cs}}(s) \\ Z^{\langle 2\rangle}_{DC,\mathrm{sc}}(s) & Z^{\langle 2\rangle}_{DC,\mathrm{ss}}(s) \end{bmatrix} \cdot \begin{bmatrix} I^{\langle 2\rangle}_{DC,\mathrm{c}}(s) - I^{\langle 2\rangle}_{APF,\mathrm{c}}(s) \\ I^{\langle 2\rangle}_{DC,\mathrm{s}}(s) - I^{\langle 2\rangle}_{APF,\mathrm{s}}(s) \end{bmatrix} \quad (8)$$

with the equivalent harmonic impedances defined as:

$$Z^{\langle 2\rangle}_{DC,\mathrm{cc}}(s) = Z^{\langle 2\rangle}_{DC,\mathrm{ss}}(s) = \frac{Z_{DC}(s - \mathrm{j}2\omega_0) + Z_{DC}(s + \mathrm{j}2\omega_0)}{2} \quad (9)$$

$$Z^{\langle 2\rangle}_{DC,\mathrm{sc}}(s) = -Z^{\langle 2\rangle}_{DC,\mathrm{cs}}(s) = \frac{Z_{DC}(s - \mathrm{j}2\omega_0) - Z_{DC}(s + \mathrm{j}2\omega_0)}{2\mathrm{j}} \quad (10)$$

This approach allows analyzing the dynamic behavior of the second-order harmonic component as the evolution of voltages and currents in a coupled 2×2 system and, similarly to the effect of a rotational transformation in a three-phase AC system, makes the steady-state variables to be constant, which is advantageous for analysis and control purposes.

III. The Fourier-Based Harmonic Controller

Through (8), the dynamic evolution of the second-order harmonic of the DC-bus voltage can be analyzed through the corresponding cosine and sine coefficients $\{v^{\langle 2\rangle}_{DC,\mathrm{c}}, v^{\langle 2\rangle}_{DC,\mathrm{s}}\}$. Then, the neutralization of the second-order harmonic ripple is aimed at driving $v^{\langle 2\rangle}_{DC,\mathrm{c}} \to 0$ and $v^{\langle 2\rangle}_{DC,\mathrm{s}} \to 0$ by acting on the harmonic currents $i^{\langle 2\rangle}_{APF,\mathrm{c}}$ and $i^{\langle 2\rangle}_{APF,\mathrm{s}}$ of the APF, while the currents $i^{\langle 2\rangle}_{DC,\mathrm{c}}$ and $i^{\langle 2\rangle}_{DC,\mathrm{s}}$ behave as constant disturbances. Since all these components are driven to constant values, it becomes feasible to analyze and control them using established tools of control theory. This offers the advantage of conveniently specifying dynamic performance characteristics, such as time constants, overshoot limits, and stability margins.

The proposed control algorithm is based on decoupling the mutual interaction between $v^{\langle 2\rangle}_{DC,\mathrm{c}}$ and $v^{\langle 2\rangle}_{DC,\mathrm{s}}$, in a way that they would behave as the voltage of the ideal DC-bus capacitor C_{DC}, which can be regulated through standard Proportional-Integral (PI) controllers. This is implemented as follows.

Thanks to the symmetry properties (9)-(10), the impedance matrix in (8) is always invertible, and it is possible to define an admittance matrix for the second-order harmonic as:

$$\begin{bmatrix} Y^{\langle 2\rangle}_{DC,\mathrm{cc}}(s) & Y^{\langle 2\rangle}_{DC,\mathrm{cs}}(s) \\ Y^{\langle 2\rangle}_{DC,\mathrm{sc}}(s) & Y^{\langle 2\rangle}_{DC,\mathrm{ss}}(s) \end{bmatrix} = \begin{bmatrix} Z^{\langle 2\rangle}_{DC,\mathrm{cc}}(s) & Z^{\langle 2\rangle}_{DC,\mathrm{cs}}(s) \\ Z^{\langle 2\rangle}_{DC,\mathrm{sc}}(s) & Z^{\langle 2\rangle}_{DC,\mathrm{ss}}(s) \end{bmatrix}^{-1} \quad (11)$$

Then, by defining the currents

$$\begin{bmatrix} I^{\langle 2\rangle}_{dist,\mathrm{c}}(s) \\ I^{\langle 2\rangle}_{dist,\mathrm{s}}(s) \end{bmatrix} = sC_{DC} \cdot \begin{bmatrix} Z^{\langle 2\rangle}_{DC,\mathrm{cc}}(s) & Z^{\langle 2\rangle}_{DC,\mathrm{cs}}(s) \\ Z^{\langle 2\rangle}_{DC,\mathrm{sc}}(s) & Z^{\langle 2\rangle}_{DC,\mathrm{ss}}(s) \end{bmatrix} \cdot \begin{bmatrix} I^{\langle 2\rangle}_{DC,\mathrm{c}}(s) \\ I^{\langle 2\rangle}_{DC,\mathrm{s}}(s) \end{bmatrix} \quad (12)$$

and by computing the reference currents for the APF as

$$\begin{bmatrix} I^{\langle 2\rangle}_{APF,\mathrm{c}}(s) \\ I^{\langle 2\rangle}_{APF,\mathrm{s}}(s) \end{bmatrix} = \frac{1}{sC_{DC}} \cdot \begin{bmatrix} Y^{\langle 2\rangle}_{DC,\mathrm{cc}}(s) & Y^{\langle 2\rangle}_{DC,\mathrm{cs}}(s) \\ Y^{\langle 2\rangle}_{DC,\mathrm{sc}}(s) & Y^{\langle 2\rangle}_{DC,\mathrm{ss}}(s) \end{bmatrix} \cdot \begin{bmatrix} I^{\langle 2\rangle}_{eq,\mathrm{c}}(s) \\ I^{\langle 2\rangle}_{eq,\mathrm{s}}(s) \end{bmatrix} \quad (13)$$

the overall system (8) for the second-order harmonic control can be rewritten as:

$$\begin{bmatrix} V^{\langle 2\rangle}_{DC,\mathrm{c}}(s) \\ V^{\langle 2\rangle}_{DC,\mathrm{s}}(s) \end{bmatrix} = \frac{1}{sC_{DC}} \cdot \begin{bmatrix} I^{\langle 2\rangle}_{dist,\mathrm{c}}(s) - I^{\langle 2\rangle}_{eq,\mathrm{c}}(s) \\ I^{\langle 2\rangle}_{dist,\mathrm{s}}(s) - I^{\langle 2\rangle}_{eq,\mathrm{s}}(s) \end{bmatrix} \quad (14)$$

The system (14) describes the dynamics of two decoupled DC-buses, with identical DC-bus capacitance C_{DC}, subject to the (constant) disturbances $i^{\langle 2\rangle}_{dist,\mathrm{c}}$ and $i^{\langle 2\rangle}_{dist,\mathrm{s}}$, and controllable through the equivalent currents $i^{\langle 2\rangle}_{eq,\mathrm{c}}$ and $i^{\langle 2\rangle}_{eq,\mathrm{s}}$.

As also previously mentioned, the regulation of $v^{\langle 2\rangle}_{DC,\mathrm{c}}$ and $v^{\langle 2\rangle}_{DC,\mathrm{s}}$ to zero can be simply achieved through standard PI controllers. The reference currents $i^{\langle 2\rangle *}_{eq,\mathrm{c}}$ and $i^{\langle 2\rangle *}_{eq,\mathrm{c}}$ can be computed from the relationship:

$$I^{\langle 2\rangle *}_{eq,\mathrm{c}}(s) = -\big(K_P + K_I/s\big) \cdot \big(0 - V^{\langle 2\rangle}_{DC,\mathrm{c}}(s)\big) \quad (15)$$

$$I^{\langle 2\rangle *}_{eq,\mathrm{s}}(s) = -\big(K_P + K_I/s\big) \cdot \big(0 - V^{\langle 2\rangle}_{DC,\mathrm{s}}(s)\big) \quad (16)$$

and the parameters of the PI controllers can be easily chosen with any well-known tuning technique to achieve the desired performances in the time and frequency domain.

Then, the corresponding harmonic current components $i^{\langle 2\rangle *}_{APF,\mathrm{c}}$ and $i^{\langle 2\rangle *}_{APF,\mathrm{s}}$ can be reconstructed via (13), and the overall APF reference current i^{*}_{APF} is obtained as:

$$i^{*}_{APF} = i^{\langle 2\rangle *}_{APF,\mathrm{c}} \cos(2\omega_0 t) + i^{\langle 2\rangle *}_{APF,\mathrm{s}} \sin(2\omega_0 t) \quad (17)$$

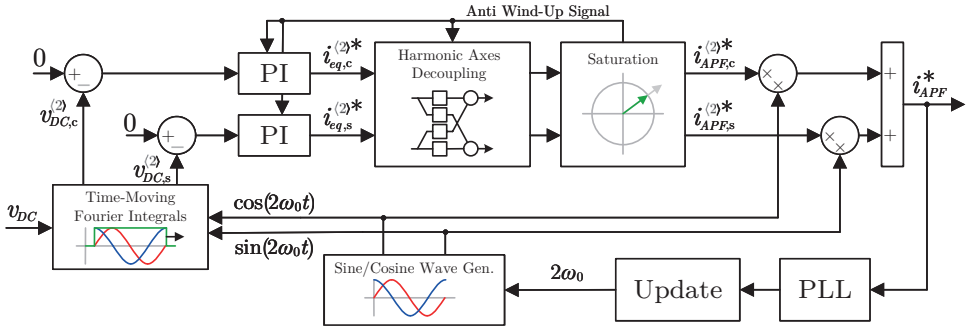

Fig. 2. Schematic block diagram of the proposed Fourier-based harmonic controller.

Overall, the reference i^*_{APF} is only computed based on the measurement and processing of the DC-bus voltage v_{DC}. It can be finally applied by using a low-level controller, which depends on the adopted active filter topology.

The block diagram of the proposed Fourier-based second-order harmonic controller is represented in Fig.2. Additional implementation details are discussed in the following.

A. Automatic Frequency Synchronization

The proposed controller, to guarantee proper selectivity, should have a precise knowledge of the harmonic frequency $2\omega_{AC}$. However, for a Plug-and-Play active filter, this information cannot be acquired in real-time from the measurements on the AC side of the system, but should instead be automatically estimated only from the DC-side measurement. Therefore, a feedback loop should be included in the controller with the aim to drive $(2\omega_0) \rightarrow (2\omega_{AC})$.

A simple solution would be to implement a Phase-Lock-Loop (PLL) algorithm on the second-order harmonic of the DC-bus voltage v_{DC} itself, in a way to automatically estimate the frequency component of interest. However, since the controller is aimed at the neutralization of $v^{\langle 2\rangle}_{DC}$, the estimation of $2\omega_{AC}$ from v_{DC} would quickly be hampered by the active filter itself, and would easily fail.

Therefore, the solution adopted in this work consists in estimating the frequency from the output i^*_{APF} of the controller, which in steady-state conditions would be a sinusoidal waveform oscillating at $2\omega_{AC}$, and would provide an increasingly closer approximation of i_{DC}. This implementation is represented in the block diagram of Fig.2. To avoid dynamic interactions between the PLL and the Fourier-based controller, the frequency $2\omega_0$ is updated with a much slower rate compared to the closed-loop dynamics of $v^{\langle 2\rangle}_{DC}$.

B. Distortion-free Circular Saturation

As in any closed-loop control algorithm, the computed reference current i^*_{APF} should be limited to comply with the maximum capabilities of the active filter itself. Therefore, a saturation algorithm should be included in the controller itself.

However, if a simple saturation is applied to the output i^*_{APF} itself, the resulting steady-state output would be non-sinusoidal, and the active filter would introduce additional undesired harmonic components to the DC-bus. Additionally, the resulting signal would be difficult to process to implement proper anti wind-up strategies for the PI controllers.

Therefore, in the proposed approach, the saturation has been implemented on the coefficients $i^{\langle 2\rangle *}_{APF,\mathrm{c}}$ and $i^{\langle 2\rangle *}_{APF,\mathrm{s}}$. With the aim to limit the magnitude $i^{\langle 2\rangle *}_{APF}$ to a specific limit $i^{\langle 2\rangle *}_{APF,max}$, the corresponding coefficients have been processed as:

$$\begin{aligned} &\text{if} \quad \left(i^{\langle 2\rangle *}_{APF} > i^{\langle 2\rangle *}_{APF,max}\right) \quad \text{then:} \\ &\quad i^{\langle 2\rangle *}_{APF,\mathrm{c}} \rightarrow i^{\langle 2\rangle *}_{APF,\mathrm{c}} \cdot \left(i^{\langle 2\rangle *}_{APF,max} / i^{\langle 2\rangle *}_{APF}\right) \\ &\quad i^{\langle 2\rangle *}_{APF,\mathrm{s}} \rightarrow i^{\langle 2\rangle *}_{APF,\mathrm{s}} \cdot \left(i^{\langle 2\rangle *}_{APF,max} / i^{\langle 2\rangle *}_{APF}\right) \\ &\text{with} \quad i^{\langle 2\rangle *}_{APF} = \sqrt{\left(i^{\langle 2\rangle *}_{APF,\mathrm{c}}\right)^2 + \left(i^{\langle 2\rangle *}_{APF,\mathrm{s}}\right)^2} \end{aligned} \tag{18}$$

In this way, the saturated output will have the same phase angle as the non-saturated reference.

Using a circular saturation on the sine and cosine coefficients of i^*_{APF} automatically guarantees a distortion-free output, and also allows to use the difference between the saturated and non-saturated outputs $i^{\langle 2\rangle *}_{APF,\mathrm{c}}$ and $i^{\langle 2\rangle *}_{APF,\mathrm{s}}$ to implement standard anti wind-up strategies. The circular saturation is shown in the corresponding block of Fig.2.

IV. Experimental Setup

A. The Power Electronics Traction Transformer

The structure analyzed in this work is a single-phase ISOP SST based on the low voltage prototype of the Power Electronic Traction Transformer (PETT) described in [4] and represented in Fig.3. This converter, conceived as a low voltage SST demonstrator for railway applications, is currently used as a research platform to analyze and improve the design and the control of ISOP SST converters.

The circuit architecture of the PETT, schematically represented in Fig.IV-A), is composed of $N = 9$ identical modules, each of which includes a non-isolated AC/DC conversion stage and a galvanically isolated DC/DC conversion stage.

In the considered setup, the isolated DC/DC conversion stages are realized with an LLC Series Resonant Conversion

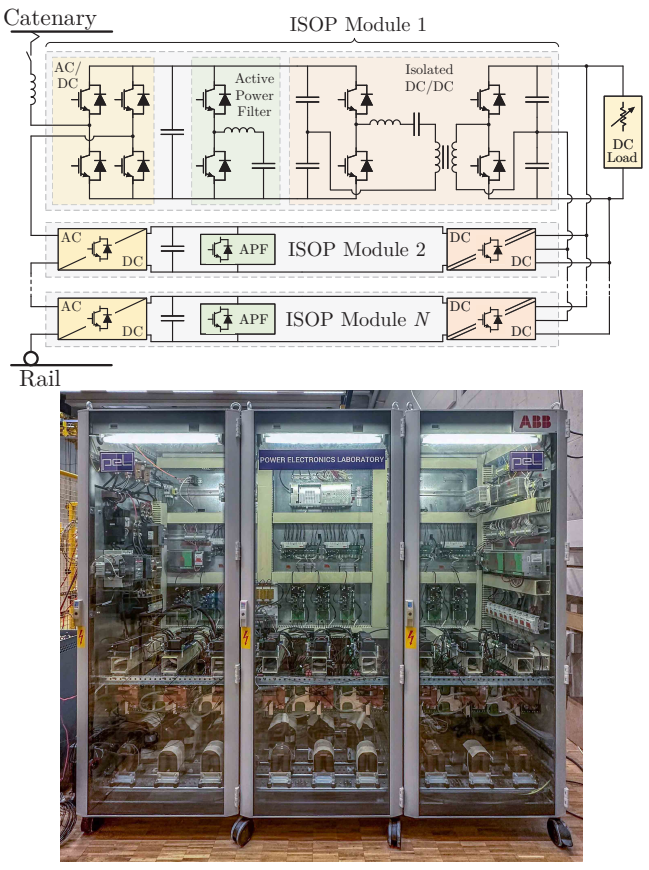

Fig. 3. The Power Electronics Traction Transformer (PETT), analyzed as example of an ISOP SST: Top) Circuit Topology; Bottom) Experimental setup.

(SRC) architecture, implemented with a half-bridge leg and a split-capacitor. The primary-side half-bridge legs are operated in open-loop with a 50% duty-cycle modulation at a frequency slightly lower than the resonance frequency of the LLC tank, in order to achieve soft-switching operation [4]- [5].

The AC/DC conversion stages are based on a full-bridge architecture. The AC grid current is controlled in closed-loop by modulating the AC/DC stages in a way to absorb, with unitary power factor, a desired power from the AC grid, with the aim to stabilize the DC-bus voltage on the secondary side of the overall ISOP converter. A phase shift pulse width modulation is implemented to control the full-bridge converters. With this technique, by shifting the carrier of the 9 modules by $1/9$ of their period, it is possible to improve the harmonic content of the equivalent voltage generated on the AC side, despite the relatively low switching frequency ($317\,\mathrm{Hz}$). At the same time, the switching harmonics generated by the AC/DC converters on the DC-bus currents of the 9 modules, once combined at the parallel output of the ISOP structure, cancel one another, meaning that the switching harmonics do not propagate to the secondary side of the SST [4], [5].

A Buck-type active filter has been implemented in the considered setup [7], with the aim to locally neutralize the introduced second-order harmonic ripple. Fig.IV-B shows the circuit topology and a picture of one of the units realized and installed into the PETT.

The parameters of the system are summarized in Table I. As described in [7], the presence of the active filter allowed the reduction of the DC-bus capacitance of each ISOP module from the initial value of $4\,\mathrm{mF}$ to a final value of $375\,\mu\mathrm{F}$. Indeed, thanks to the active filters, the DC-bus capacitance does not need to be sized for the suppression of the second-order voltage harmonic ripple, and is instead only subject to the switching harmonics produced by the conversion stages.

The control algorithm developed for the active filters in [7] was based on the direct compensation of the second-order harmonic current generated locally by each AC/DC conversion stage. As also previously mentioned, this approach, despite being simple and intuitive, requires each active filter to access information regarding the AC voltage and current of the SST, thus needing additional sensing equipment or communication interfaces between the conversion structures. It has therefore been replaced by the proposed Fourier-based control algorithm, in a way to test the potential use of the active filter as a Plug-and-Play solution.

TABLE I
USED PARAMETERS OF THE PETT.

Parameter		**Value**
Power	P	$8\,\mathrm{kW}$
AC Grid Voltage (RMS)	$V_{AC,RMS}$	$800\,\mathrm{V}$
AC Grid Frequency	f_{AC}	$50\,\mathrm{Hz}$
Number of ISOP Modules	N	9
Primary DC Voltage (single module)	V_{DC}	$220\,\mathrm{V}$
Primary DC Capacitance (single module)	C_{DC}	$375\,\mu\mathrm{F}$
Secondary DC Voltage	$V_{DC,out}$	$220\,\mathrm{V}$
Secondary DC Capacitance (equivalent)	$C_{DC,out}$	$20\,\mathrm{mF}$
LLC Resonant Inductance	L_{res}	$135\,\mu\mathrm{H}$
LLC Resonant Capacitance	C_{res}	$60\,\mu\mathrm{F}$
LLC Magnetizing Inductance	L_{mag}	$13\,\mathrm{mH}$
LLC Transformation Ratio	N_1/N_2	1
AC/DC Switching Frequency	$f_{AC/DC}$	$317\,\mathrm{Hz}$
DC/DC Switching Frequency	$f_{DC/DC}$	$1.5\,\mathrm{kHz}$
Active Filter Apparent Power	S_{APF}	$1\,\mathrm{kVA}$
Active Filter Inductance	L_{APF}	$200\,\mu\mathrm{H}$
Active Filter Capacitance	C_{APF}	$360\,\mu\mathrm{F}$
Active Filter Capacitor Voltage	V_C^*	$160\,\mathrm{V}$
Active Filter Switching Frequency	$f_{sw,APF}$	$10\,\mathrm{kHz}$

B. Low-level control of the Buck-type Active Filter

The proposed Fourier-based harmonic control algorithm provides a reference current i^*_{APF} to be absorbed from the DC-bus, based on the measured DC-bus voltage v_{DC}. Therefore, it is independent of the specific architecture of the active filter. The control of the current i_{APF} is instead depending on the specific architecture of the active filter, and can be regarded as part of a low-level control algorithm.

The low-level control algorithm of the Buck-type is schematically represented in Fig.IV-B, and is based on the regulation of the overall energy stored in C_{APF}, which is realized through the control of its voltage v_C. To be more specific, the controller features a cascaded scheme, with an outer control loop regulating the capacitor voltage v_C and an inner control loop regulating the inductor current i_L. The outer control loop compares the measured voltage v_C to the reference voltage v_C^* and computes, through a Proportional-Integral-Resonant (PIR) controller, a reference current i_L^* for the inductor, that is then tracked by the inner loop, which is also based on a PIR architecture, with the voltage v_C added as a feedforward term. The output of the current controller is a voltage reference u^*_{APF}, which is applied through a Pulse Width Modulation (PWM) technique.

The reference voltage v_C^* has been computed as:

$$v_C^* = \sqrt{{V_{C0}^*}^2 + \left(v_{DC}\cdot i'^*_{APF}\right)/\left(\omega_{AC} C_{APF}\right)} \tag{19}$$

where V_{C0}^* is the rated offset voltage for the buck capacitor, while the current i'^*_{APF} defined as the 90° shifted version of the current i^*_{APF} expressed in (17), which can be directly computed from the coefficients $i^{\langle 2\rangle *}_{APF,\mathrm{c}}$ and $i^{\langle 2\rangle *}_{APF,\mathrm{s}}$ as:

$$i'^*_{APF} = i^{\langle 2\rangle *}_{APF,\mathrm{s}} \cos\left(2\omega_0 t\right) - i^{\langle 2\rangle *}_{APF,\mathrm{c}} \sin\left(2\omega_0 t\right) \tag{20}$$

In this way, by neglecting the conversion losses and the energy stored in L_{APF}, the equivalent current absorbed in steady-state conditions from the DC-bus is approximately equal to:

$$\begin{aligned} i_{APF} &= \frac{p_{APF}}{v_{DC}} \approx \frac{1}{v_{DC}}\cdot\frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{1}{2} C_{APF}\, {v_C^*}^2\right) \approx \\ &\approx \frac{1}{v_{DC}}\cdot\frac{\mathrm{d}}{\mathrm{d}t}\left(\frac{1}{2\omega_{AC}}\, v_{DC}\, i'^*_{APF}\right) \approx \frac{1}{2\omega_{AC}}\cdot\frac{\mathrm{d}i'^*_{APF}}{\mathrm{d}t} \approx \\ &\approx i^{\langle 2\rangle *}_{APF,\mathrm{c}} \cos\left(2\omega_0 t\right) + i^{\langle 2\rangle *}_{APF,\mathrm{s}} \sin\left(2\omega_0 t\right) \approx i^*_{APF} \end{aligned} \tag{21}$$

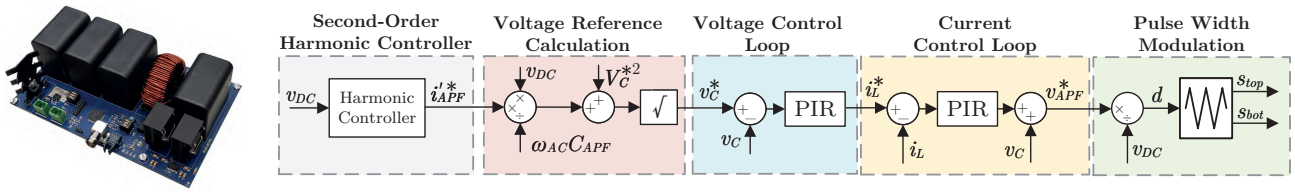

Fig. 4. Buck-type active filter implemented in PETT. Left) Hardware prototype; Right) Control block diagram.

C. Tuning

To implement the harmonic axes decoupling (13), it is necessary to estimate the equivalent impedance seen from one active filter unit at the corresponding DC-bus. As discussed in Section II, this impedance does not only consist of the DC-bus capacitance, but needs to take into account also the equivalent contribution of all the other modules of the ISOP converter, that can propagate through the LLC conversion stage [13].

The theoretical impedance Z_{DC} seen from one module of the PETT, and the corresponding impedances $Z_{DC,\mathrm{cc}}$ and $Z_{DC,\mathrm{sc}}$ are represented in Fig.5. They have been computed from the analysis of the equivalent circuit described in [13].

The equivalent impedances $Z^{\langle 2\rangle}_{DC,\mathrm{cc}}$ and $Z^{\langle 2\rangle}_{DC,\mathrm{sc}}$ have been also estimated in the real experimental setup for the low frequency operation (which corresponds to the equivalent behavior of Z_{DC} close to 100 Hz). This has been done by applying a step change in the second-order harmonic current components $\{i^{\langle 2\rangle}_{APF,\mathrm{c}}, i^{\langle 2\rangle}_{APF,\mathrm{s}}\}$ injected by one active filter and observing the corresponding response of $\{v^{\langle 2\rangle}_{DC,\mathrm{c}}, v^{\langle 2\rangle}_{DC,\mathrm{s}}\}$. The results are shown in Fig.6. In this case, the current perturbation has been injected while the active filters of all the other SST modules were already functioning based on the open-loop control algorithm developed in [7]. The results are in line with the theoretical analysis.

The PI controllers have then been tuned to achieve a closed-loop behavior of a first-order system with a time constant of around $\tau \approx 100\,\mathrm{ms}$ (i.e., around 10 periods of the second-order harmonic oscillation at 100 Hz). Thanks to the harmonic axes decoupling, the equivalent impedance used for the control is the same impedance of the ideal DC-bus capacitance of a single SST module, and the parameters of the PI controllers have been set as $K_P = C/\tau$ and $K_I = K_P/20\tau$.

V. Validation on a Single ISOP SST Module

The proposed control algorithm has been first validated on a single SST module, to test its performances to locally neutralize the second-order harmonic ripple. This section summarizes the results obtained in this preliminary configuration.

A. Harmonic Controller Activation

The first test has been conducted by activating the harmonic controller of the SST cell 1 while the ISOP SST is working in steady-state conditions at a 220 V DC-bus voltage and 6 kW power. The results are reported in Fig.7. They show the DC-bus voltage v_{DC}, the current i_{APF} absorbed by the DC-bus, and the buck-capacitor voltage v_C of the ISOP SST module 1. For comparison, Fig.7 also shows the same variables for another SST module (i.e., module 2), and the voltage $v_{DC,out}$ of the secondary-side of the overall converter.

To better appreciate the behaviour of the controller, the right side graphs in Fig.7 show the magnitude of the second-order harmonic of the same variables, computed as per (5)-(7).

As can be noted, after the activation of the harmonic controller (at around 50 ms), the current $i_{APF,1}$ is controlled to be sinusoidal at $2\omega_{AC}$, and a second-order harmonic is

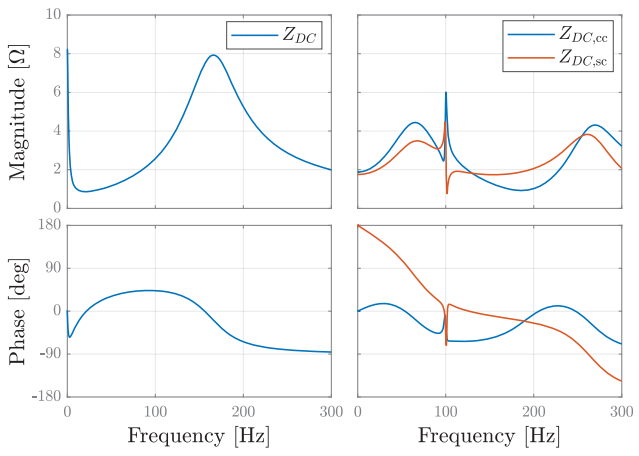

Fig. 5. Equivalent impedance seen from one module of the PETT.

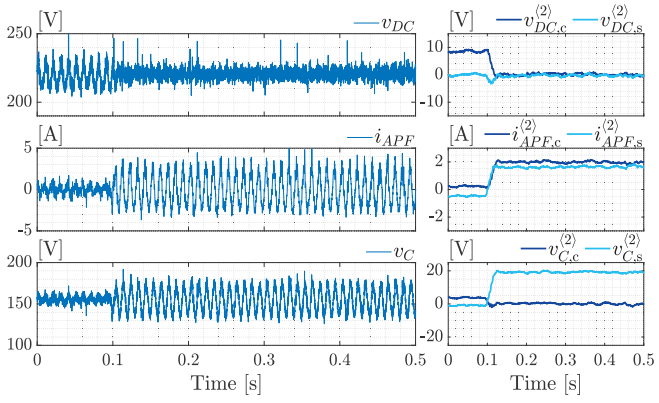

Fig. 6. Results following the activation of one active filter of the SST, used to derive the equivalent harmonic impedances of the system. Left) Time domain waveforms; Right) Time-moving coefficients of the second-order harmonic.

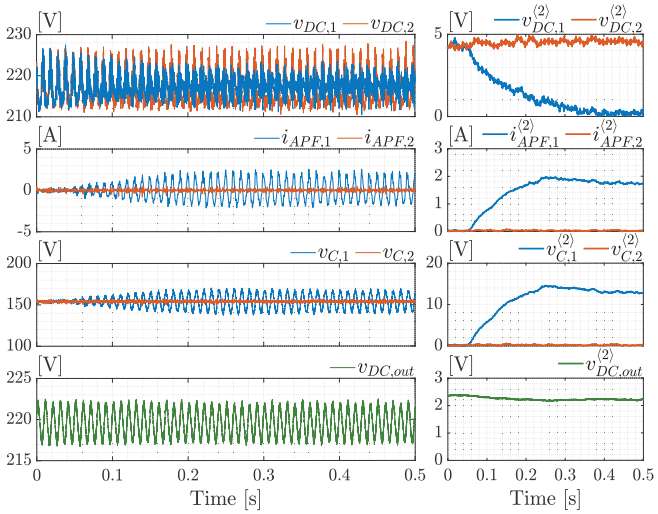

Fig. 7. Results following the activation of the harmonic controller on the active filter of the SST module 1. Left) Time-domain waveforms; Right) Time-moving magnitude of the second-order harmonic.

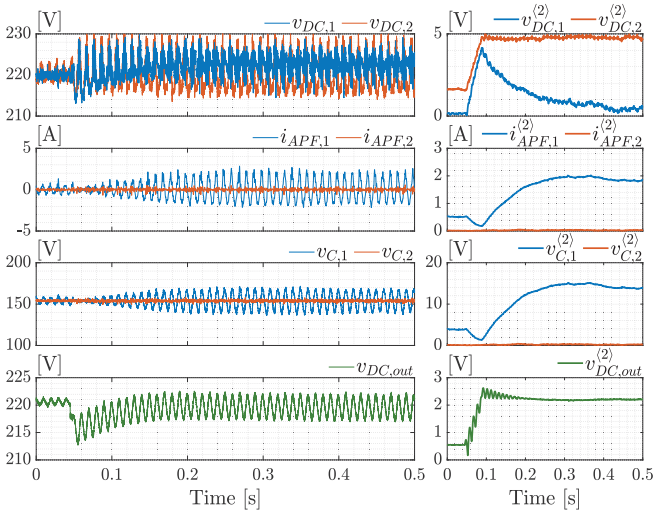

Fig. 8. Results following a power transient in the ISOP SST, while the harmonic controller of the module 1 is enabled. Left) Time-domain waveforms; Right) Time-moving magnitude of the second-order harmonic.

imposed on the buck capacitor voltage $v_{C,1}$. This affects the DC-bus voltage $v_{DC,1}$, whose second-order harmonic $v^{\langle 2\rangle}_{DC,1}$ quickly decreases to zero. As desired, the dynamic evolution of $v^{\langle 2\rangle}_{DC,1}$ is approximately equal to the evolution of a first-order system with a time constant of 100 ms.

The harmonic controller can also influence the DC-bus voltage of the other SST modules (e.g., $v_{DC,2}$) and of the output of the overall converter (i.e., $v_{DC,out}$). However, in the analyzed scenario, the activation of a single active filter has negligible effects.

The additional harmonics present on $v_{DC,1}$ and $v_{DC,2}$ are related to the low switching frequency of the AC/DC conversion stages. However, as also previously mentioned, thanks to the phase shift modulation of the AC/DC stages, these harmonics do not propagate to $v_{DC,out}$.

B. Performances during a power transient

To validate the performances of the proposed controller during different SST operating condition, a test has been performed considering a power transient in the system.

The system, starting from a steady-state condition at 220 V and around 1.5 kW, is subject to a power step change to a final value of around 6 kW. During the whole test, the harmonic controller on the SST module 1 has been kept enabled. The results are shown in Fig.8.

The effect of the power step change can be immediately noted on both the DC-bus voltages $v_{DC,1}$,$v_{DC,2}$, and on the overall secondary voltage $v_{DC,out}$, that show both an average voltage drop and an increase of the second-order harmonic oscillation. The drop in the average voltage, of around 5 V, is quickly compensated by the closed-loop control of the AC/DC stages, while the increase of the magnitude of the second-order harmonic is only compensated on $v_{DC,1}$, thanks to the effect of the active filter.

Once again, the dynamic performances of the harmonic controller are coherent with the desired specifications, and the second order harmonic ripple $v^{\langle 2\rangle}_{DC,1}$ is almost completely suppressed in around 400 ms.

VI. Validation on all the ISOP SST modules

The proposed control, successfully validated on a single module of the ISOP SST, has been finally applied to all the active filters of the converter. This section summarizes the results of the test on the complete system.

A. Harmonic Controller Activation

Similarly to SectionV-A, the first test has been conducted by activating the harmonic controllers while the ISOP SST is working in steady-state conditions at a 220 V DC-bus voltage and 6 kW power. The results are reported in Fig.9.

As can be noted, in this case the performances of different SST modules (e.g., module 1 and 2) are perfectly matching. The simultaneous activation of all the harmonic controllers not only leads to the neutralization of the harmonic ripple on the local DC-bus voltages (as can be noted from $v^{\langle 2\rangle}_{DC,1}$ and $v^{\langle 2\rangle}_{DC,2}$), but also leads to the neutralization of the second-order harmonic ripple on the output of the overall ISOP converter (as can be seen from $v^{\langle 2\rangle}_{DC,out}$). This proves that the proposed controller can effectively operate in the complete setup.

B. Performances during a power transient

Once again, to validate the performances of the proposed controller in different SST operating conditions, it has been tested considering a power transient from 1.5 kW to 6 kW. The results are shown in Fig.10.

Similarly to Section V-B, the power step change affects both the average DC-bus voltages (that show a temporary drop) and their second-order harmonic ripple.

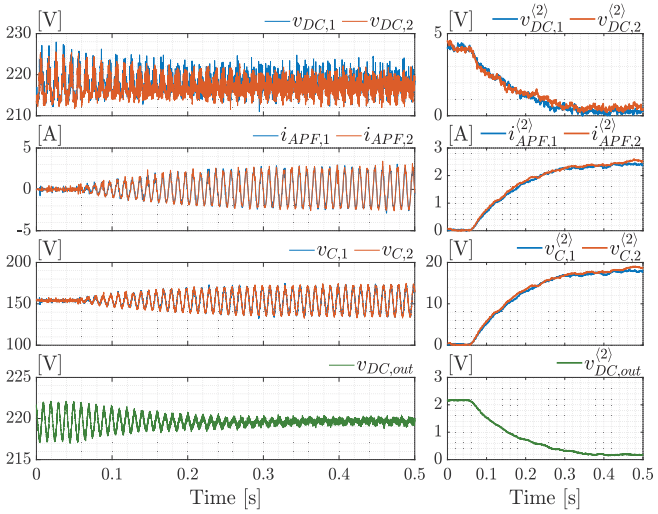

Fig. 9. Results following the simultaneous activation of the harmonic controllers on all the active filters of the ISOP SST. Left) Time-domain waveforms; Right) Time-moving magnitude of the second-order harmonic.

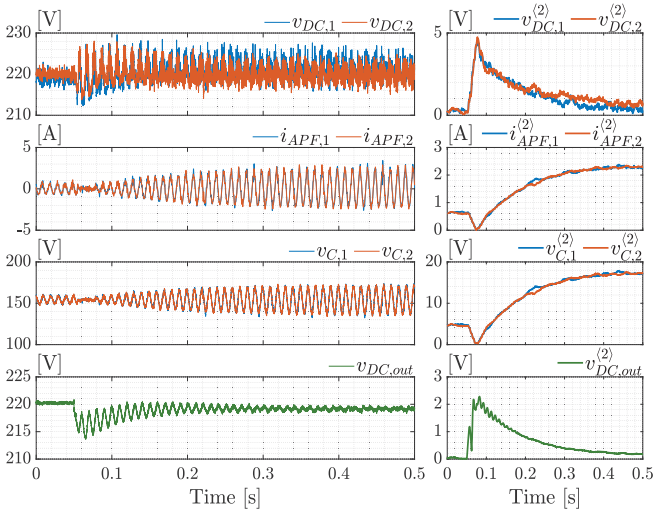

Fig. 10. Results following a power transient in the ISOP SST, while the harmonic controllers of all the active filters are enabled. Left) Time-domain waveforms; Right) Time-moving magnitude of the second-order harmonic.

Thanks to the active filters, the increase of the second-order harmonic ripple is quickly compensated by the increase of $i_{APF,k}$ and $v_{C,k}$ (with $k = 1, ..., 9$), and is almost completely neutralized in around $400\,\text{ms}$.

VII. Conclusions

ISOP SST converters suffer a second-order harmonic ripple caused by a local single-phase AC/DC conversion on each module. This ripple can be neutralized through active filters.

This paper presented a control algorithm for second-order harmonic active filters employed in ISOP SST configurations. The proposed approach does not require any external measurement other than voltages and currents internal to each active filter, and is therefore suitable for plug-and-play solutions and for installation on a pre-existing system.

The control algorithm is based on a time-moving Fourier decomposition of the system variables, and allows a precise control of the dynamic evolution of the second-order harmonics of interests. Thanks to the adopted formalism, the harmonic evolution can be analyzed through time-moving sine and cosine components, that can be dynamically decoupled and can be separately regulated using standard PI controllers.

The algorithm has been experimentally validated on a LV PETT, used as a case example of a single-phase ISOP SST configuration, showing satisfactory performances.

References

[1] J. E. Huber and J. W. Kolar, "Solid-State Transformers: On the Origins and Evolution of Key Concepts," in IEEE Industrial Electronics Magazine, vol. 10, no. 3, pp. 19-28, Sept. 2016, doi: 10.1109/MIE.2016.2588878.

[2] E. R. Ronan et al., "A power electronic-based distribution transformer," in IEEE Transactions on Power Delivery, vol. 17, no. 2, pp. 537-543, April 2002, doi: 10.1109/61.997934.

[3] N. Hugo, P. Stefanutti, M. Pellerin and A. Akdag, "Power electronics traction transformer," 2007 European Conference on Power Electronics and Applications, Aalborg, Denmark, 2007, pp. 1-10, doi: 10.1109/EPE.2007.4417649.

[4] D. Dujic et al., "Power Electronic Traction Transformer-Low Voltage Prototype," in IEEE Transactions on Power Electronics, vol. 28, no. 12, pp. 5522-5534, Dec. 2013, doi: 10.1109/TPEL.2013.2248756.

[5] C. Zhao et al., "Power Electronic Traction Transformer—Medium Voltage Prototype," in IEEE Transactions on Industrial Electronics, vol. 61, no. 7, pp. 3257-3268, July 2014, doi: 10.1109/TIE.2013.2278960.

[6] Y. Sun et al., "Review of Active Power Decoupling Topologies in Single-Phase Systems," in IEEE Transactions on Power Electronics, vol. 31, no. 7, pp. 4778-4794, July 2016, doi: 10.1109/TPEL.2015.2477882.

[7] T. Wei, A. Cervone and D. Dujic, "Second Harmonic Ripple Voltage Suppression for Single-Phase ISOP Solid-State Transformer by Active Power Decoupling," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 1496-1502, doi: 10.1109/APEC43580.2023.10131324.

[8] D. Neumayr et al., "Comparative Evaluation of a Full- and Partial-Power Processing Active Power Buffer for Ultracompact Single-Phase DC/AC Converter Systems," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 2, pp. 1994-2013, April 2021, doi: 10.1109/JESTPE.2020.2987937.

[9] Z. Qin et al., "Benchmark of AC and DC Active Power Decoupling Circuits for Second-Order Harmonic Mitigation in Kilowatt-Scale Single-Phase Inverters," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, no. 1, pp. 15-25, March 2016, doi: 10.1109/JESTPE.2015.2490199.

[10] R. Wang et al., "A High Power Density Single-Phase PWM Rectifier With Active Ripple Energy Storage," in IEEE Transactions on Power Electronics, vol. 26, no. 5, pp. 1430-1443, May 2011, doi: 10.1109/TPEL.2010.2090670.

[11] Z. Kong, X. Huang, Z. Wang, J. Xiong and K. Zhang, "Active Power Decoupling for Submodules of a Modular Multilevel Converter," in IEEE Transactions on Power Electronics, vol. 33, no. 1, pp. 125-136, Jan. 2018, doi: 10.1109/TPEL.2017.2661539.

[12] Nguyen, V.T., Kim, J.W., Park, J.W., Lee, J.M., Park, B.G.: "A modified submodule of modular multilevel converter using active power decoupling method for reducing capacitor voltage ripple under low-frequency operation," in IET Power Electron. 16, pp. 868–882, 2023. https://doi.org/10.1049/pel2.12432

[13] A. Cervone, T. Wei and D. Dujic, "Coupling Dynamics of Second-Order Harmonic Active Filters in Single-Phase Input-Series/Output-Parallel AC-DC Converters," PCIM Europe 2023, Nuremberg, Germany, 2023, pp. 1-10, doi: 10.30420/566091033.