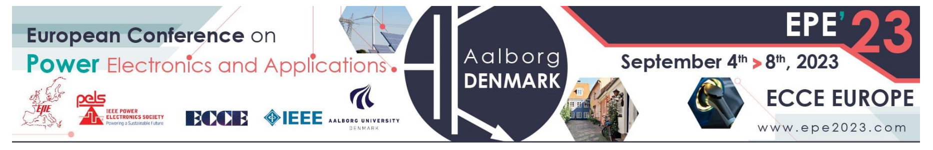


SIC MOSFET GATE DRIVERS FOR HIGH-POWER APPLICATIONS

Prof. Dražen Dujić, Dr. Chengmin Li

École Polytechnique Fédérale de Lausanne (EPFL)
Power Electronics Laboratory (PEL)
Lausanne, Switzerland

EPFL

pel

INTRODUCTION

Power Electronics Laboratory at EPFL

INSTRUCTORS

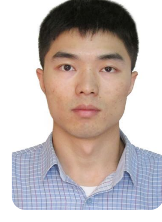
Prof. Drazen Dujic

Experience:

2014 – today	École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland
2013 – 2014	ABB Medium Voltage Drives, Turgi, Switzerland
2009 – 2013	ABB Corporate Research, Baden-Dättwil, Switzerland
2006 – 2009	Liverpoool John Moores University, Liverpool, United Kingdom
2003 – 2006	University of Novi Sad, Novi Sad, Serbia

Education:

2008	PhD, Liverpoool John Moores University, Liverpool, United Kingdom
2005	M.Sc., University of Novi Sad, Novi Sad, Serbia
2002	Dipl. Ing., University of Novi Sad, Novi Sad, Serbia



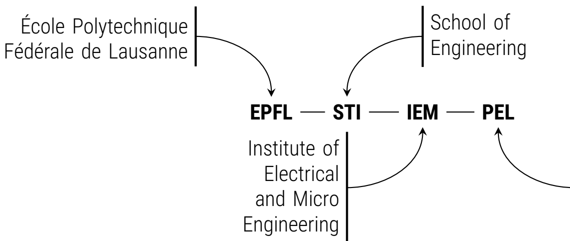
Dr. Chengmin Li

Experience:

soon –	TU/e, Eindhoven, Netherlands
2020 – 2023	École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland

Education:

2019	PhD, Zhejiang University, Zhejiang, China
2013	B.Sc., Huazhong University of Science and Technology, Wuhan, China



- Online since February 2014
- Currently: 10 PhD students, 4 Post Docs, 1 Administrative Assistant
- Funding CH: SNSF, SFOE, Innosuisse
- Funding EU: H2020, S2R JU, ERC CoG
- Funding Industry: OEMs
- `https://www.epfl.ch/labs/pel/`

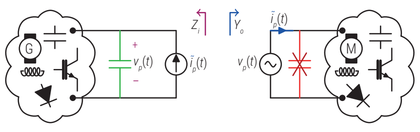
Competence Centre

▲ PEL Medium Voltage Laboratory

RESEARCH FOCUS

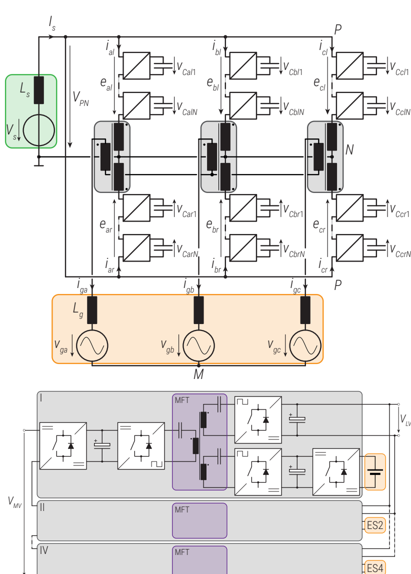
MVDC Technologies and Systems

- System Stability
- Protection Coordination
- Power Electronic Converters



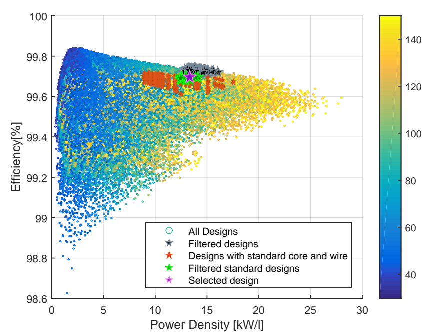
High Power Electronics

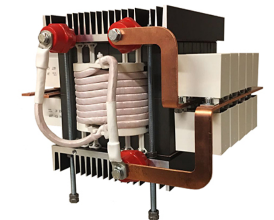
- Multilevel Converters
- Solid State Transformers
- Medium Frequency Conversion



Components

- Semiconductor devices
- Magnetics
- Modeling, Characterization





SCHEDULE

Before the coffee break

1) Semiconductor Devices

- An overview
- Si vs. WBG devices
- IGBT vs SiC gate driving

2) Gate Driving of SiC Devices

- Switching characteristics
- Gate driver structure and principles
- Auxiliary power supply considerations

3) Protection of SiC devices

- Crosstalk voltage elimination
- Short circuit protection
- Measurements and sensing

After the coffee break

4) High power converters with SiC

- State of the art solutions
- Features, Advantages, Benefits
- SiC integration challenges

5) SiC MOSFET integration

- Parallel connection
- Series connection
- Si/SiC hybrid solutions

6) Discussion

- Trends
- Challenges
- Opportunities

⇒ Tutorial pdf can be downloaded from: *(Source:* `https://www.epfl.ch/labs/pel/publications-2/publications-talks/`*)*

SEMICONDUCTOR DEVICES

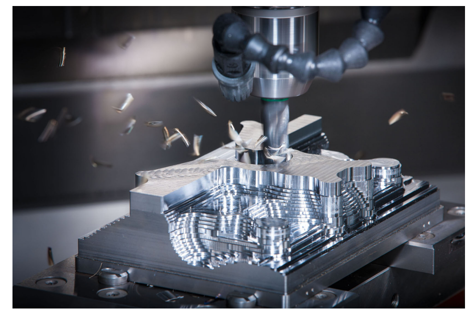
An overview

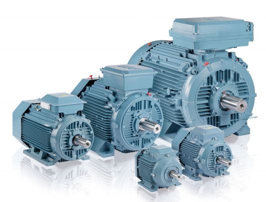
POWER ELECTRONIC APPLICATIONS - SMPS

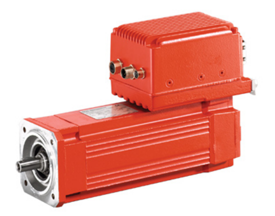
- By far the largest market in power electronics

POWER ELECTRONIC APPLICATIONS - VARIABLE SPEED DRIVES

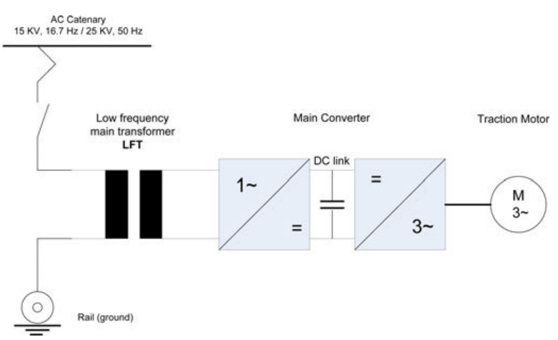
- Continuously improving the efficiency in industrial processes

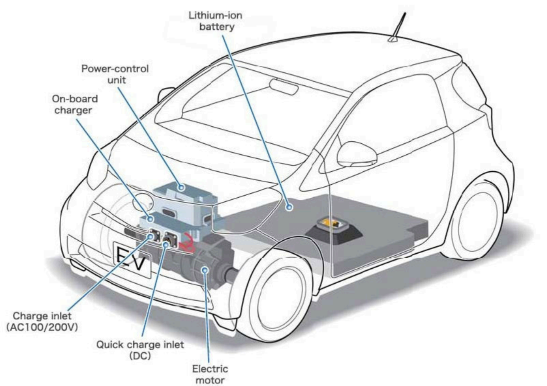


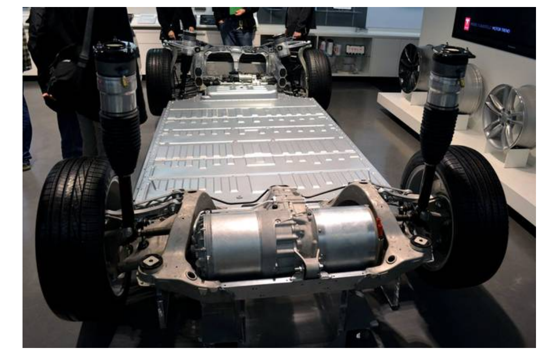




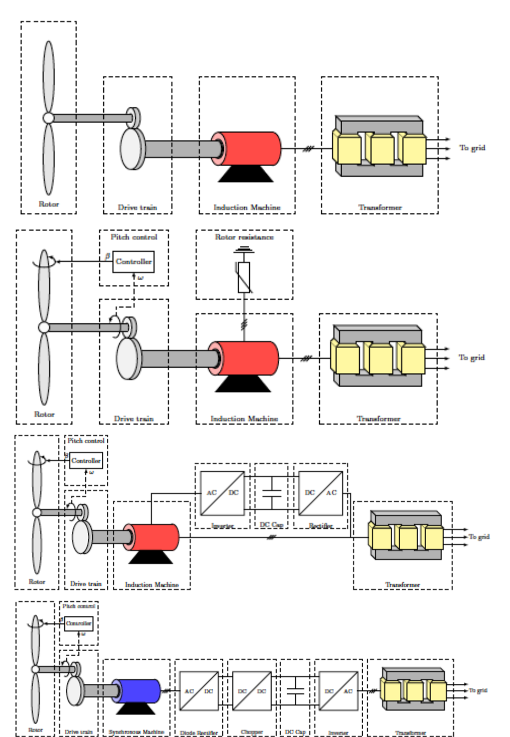
- Moving people and goods with electrical energy





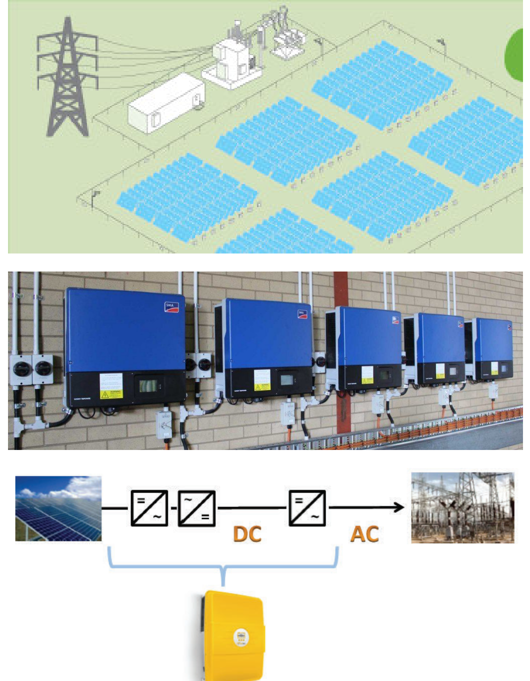


- Enabling renewable energy generation



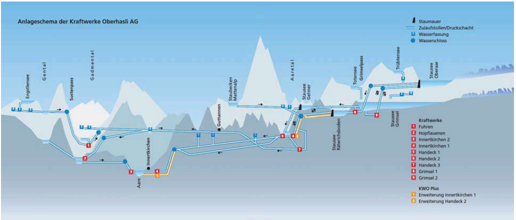
POWER ELECTRONIC APPLICATIONS – PHOTOVOLTAIC POWER GENERATION

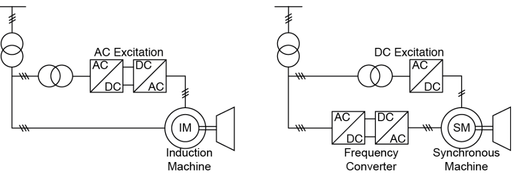
- Enabling renewable energy generation

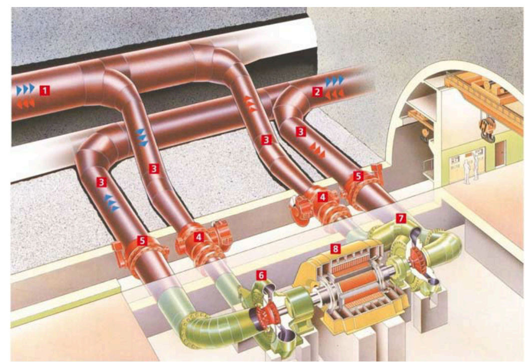


POWER ELECTRONIC APPLICATIONS - PUMPED HYDRO STORAGE PLANTS

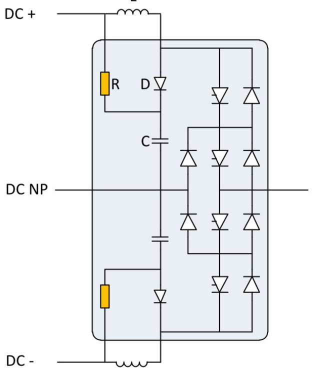
- Improving flexibility and efficiency in hydropower applications

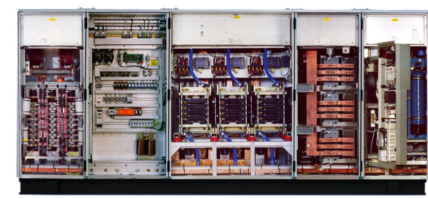






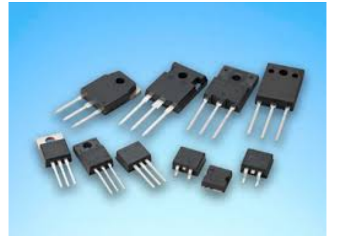
- Medium voltage drives for high power applications

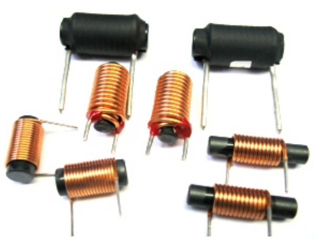




POWER ELECTRONIC DEVICES

- Power semiconductors are key enabling technology for modern power electronics





POWER SEMICONDUCTORS - REQUIREMENTS

Power Density Handling Capability

- Low on-state and switching losses (traditional trend: improved technology curves)
- Low thermal resistance (device active area selection and chip joining technology)
- High operating temperatures (low leakage current and robustness)

Controllable and Soft Switching Characteristics

- Soft and controllable turn-off (low overshoot voltages and EMI levels)
- Turn-on controllability (gate control/response for optimum transients and losses)

Ruggedness and Fault Handling

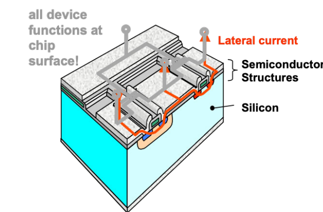
- SOA: Turn-off current capability (wide Safe-Operating-Area)
- Fault-Handling: Short circuit capability for IGBT (protection for system)
- Fault-Handling: Surge current capability for diode/IGCT (protection for system)

Device Reliability

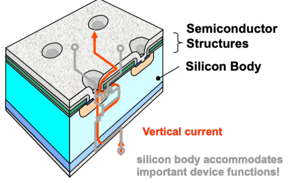
- Current/voltage sharing paralleled/series devices (positive temp co. in on-state)
- Stable conduction/switching (stable device parameters)
- Stable voltage blocking (stable device parameters, low cosmic ray FIT)

Powerfull and Reliable Package

- Compact (chip packing density, low parasitic elements, optimum electrical layout)
- Powerful (high current, high voltage, high temperature)
- Reliable (temperature and power cycling, chip protection)
- Fault Conditions (explosion resistance, fail short)



▲ Signal processing - Lateral devices



▲ Power processing - Vertical devices

▲ Typical high power packages (Hitachi Energy)

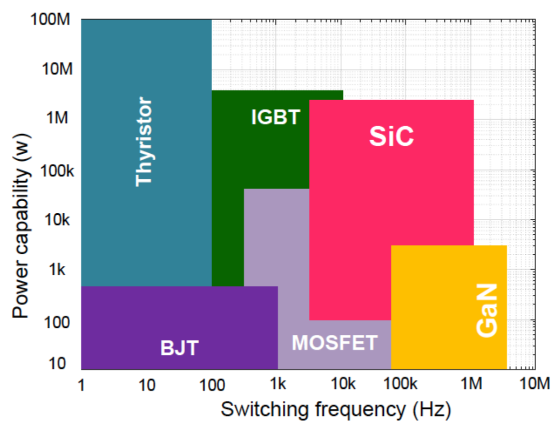
[0] Source: Dr. Munaf Rahimo, MTAL

Wide Band-Gap materials are available, offering:

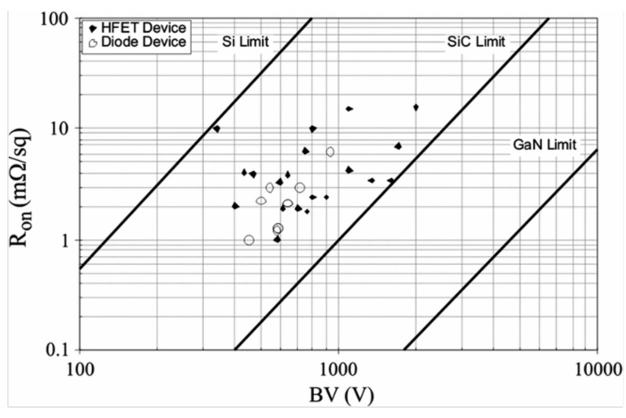
- higher operating frequencies
- higher operating temperatures
- lower leakage currents
- smaller devices

Parameter		Silicon	SiC	GaN
Band Gap – E_g	eV	1.12	3.26	3.39
Critical Field – E_{crit}	MV/cm	0.23	2.2	3.3
Electron Mobility – μ_n	cm^2/Vs	1400	950	1500
Permitivity – ε_r		11.8	9.7	9
Thermal Conductivity – λ	W/cmK	1.5	3.8	1.3

$$R_{on} = \frac{4BV^2}{\varepsilon_0 \varepsilon_r E_{crit}^2}$$



▲ Coverage area of different devices



▲ Device limits (theoretical)

SOME DIFFERENCES BETWEEN SIC AND SI DEVICES

Device

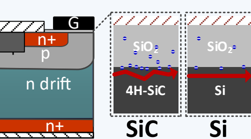
Wide Bandgap

Si 1.12eV

4H-SiC 3.23eV

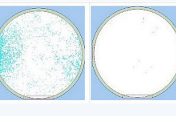
- High electric field stress

Defects in gate oxide



- V_{th} Shift

Defects in SiC crystal

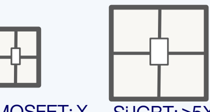


4H-SiC Si

- Bipolar degradation

Package

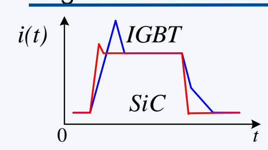
Smaller chip



SiC MOSFET: X Si IGBT: >5X

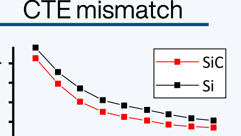
- Larger thermal resistance and thermal coupling

High dv/dt and di/dt



- Significant electromagnetic coupling

CTE mismatch



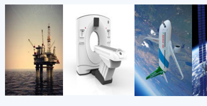
- Higher thermal fatigue

Application

Fast switching

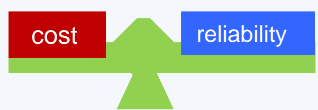
- Gate driving
- Increased EMI noise

Survivability in field



- Different SOA
- Harsh environment

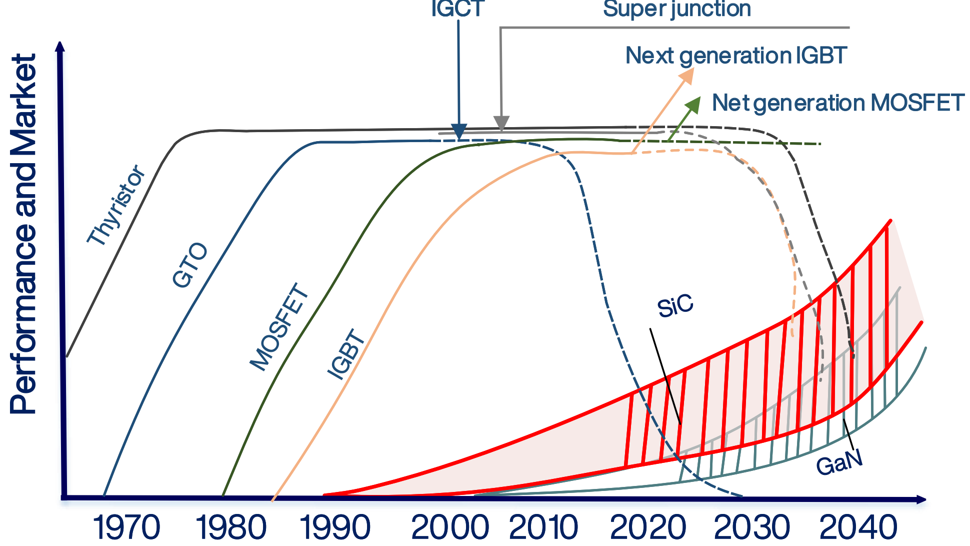
Design for reliability



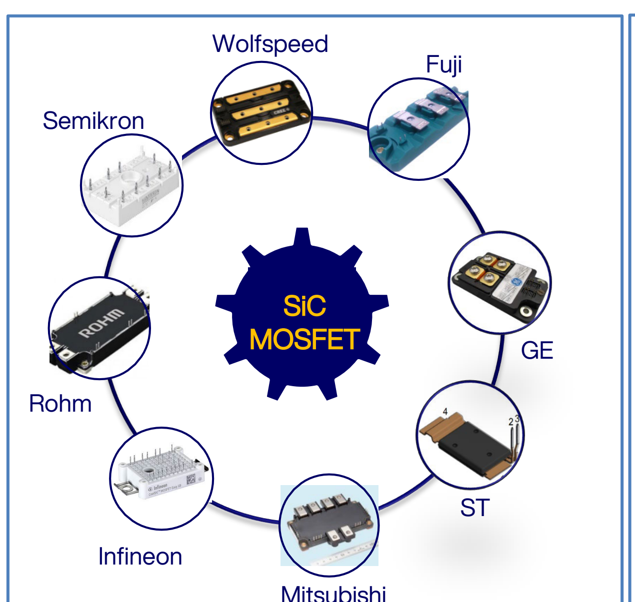
- Cost, performance & reliability trade-off

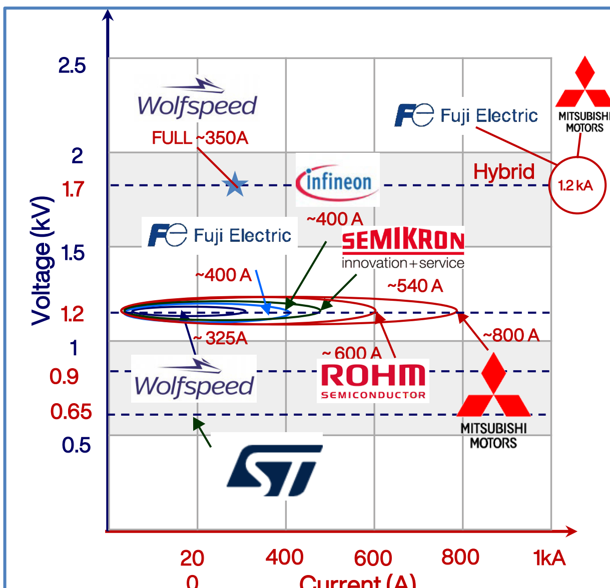
PREDICTION OF MARKET GROWTH

- Si devices are approaching its material limit, but still mature and reliable
- SiC power MOSFETs are suitable for high voltage, high efficiency and high power density applications



- Industrial products released are mainly below 1.7kV
- Medium voltage device (3.3kV, 6.5kV) are under development
- Higher voltage device (10kV, 15kV) are already demonstrated
- Main high power contenders are IGBT and IGCT (SCR and GTO as well)





IGCT: CHARACTERISTICS

IGCTs' main characteristics:

- Thyristor based device
- Lowest conduction loss of fully controllable devices
- Integrated in GDU
- Only available as press-pack
- Snubberless turn-off

Traditional IGCT application:

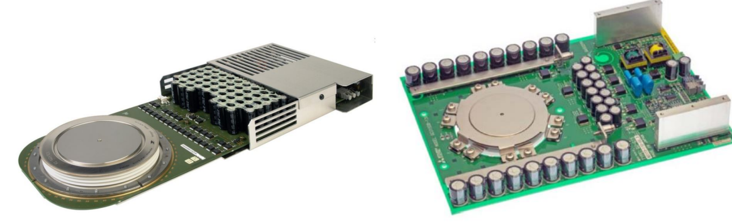
- Low frequency (<1 kHz)
- Hard switched

The main types of IGCTs:

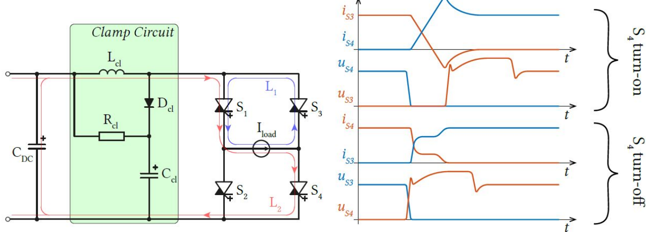
- Asymmetric
- Reverse conducting - RC-IGCT
- Reverse blocking - RB-IGCT

Compared to the IGBT the IGCT:

- Cannot control turn-on di/dt through GDU
- Requires clamp circuitry
- Cannot turn *OFF* short circuit current
- Has significant GDU power consumption
- Requires bulky GDU capacitors to maintain constant gate-cathode voltage at turn-off



▲ The press-packed GCT is always integrated into the gate driver board to minimise inductance between gate and cathode



▲ The clamp circuit and current and voltage waveforms for the S_3 and S_4 during turn-on and turn-off transients

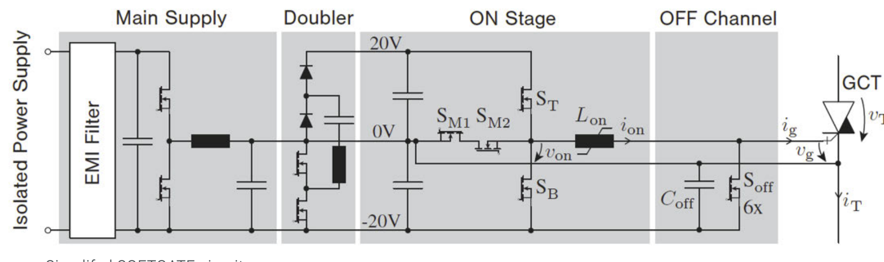
IGCT - GATE UNIT DESIGN

SOFTGATE IGCT Gate Unit

- Gate unit tailored for soft switching
- Historically, gate unit is designed for hard turn-OFF

Integration of multiple functions into a single ON channel:

- Turn-ON function
- Retrigger function
- Backporch function
- Negative-Voltage Backporch functions



▲ Simplifed SOFTGATE circuitry

▲ Realized SOFTGATE gate unit [1]

IGCT - GATE UNIT DESIGN.

SOFTGATE IGCT Gate Unit

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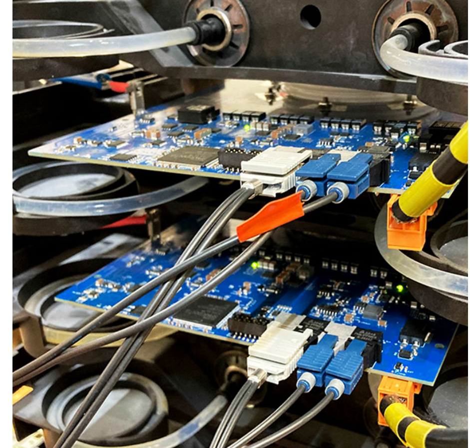


▲ SOFTGATE units during testing

▲ IGCT stacks

IGBT: CHARACTERISTICS

IGBTs' main characteristics:

- Insulated gate
- Fully controllable
- Voltage controlled
- High power/voltage ratings
- High switching speed
- Simple integration
- Available as module and press-pack

Additional benefits:

- Limitation and turn-off of short circuit current
- Low voltage drop in *ON* state

Commonly available in:

- Modules
- Press-Pack
- StakPak

Switching performance:

- Can be externally affected by Gate Drive Unit
- Offers controllable di/dt with adequate gate resistance values
- Does not require external circuitry for safe operation

Device	Voltage Class [kV]	Current Rating [A]	V_{ON} @1kA[V]	V_{ON} @2kA[V]
IGBT/diode	4.5	1600	2.30	3.40
IGBT/diode	4.5	2000	2.55	3.65
IGBT	4.5	2100	1.90	2.70
GTO	4.5	2000	2.20	2.70
Thyristor	4.5	1150	1.35	1.65
IGCT/diode	4.5	2200	2.00	2.50
IGCT	4.5	4000	1.50	1.80

▲ Typical conduction performance of common semiconductor devices

Typical ratings for MV IGBTs:

- 4.5 kV-6.5 kV
- 900 A-1200 A

▲ IGBT packaging includes modules, press-pack, and StakPak units

IGBT - GATE DRIVER DESIGN

Multiple functions

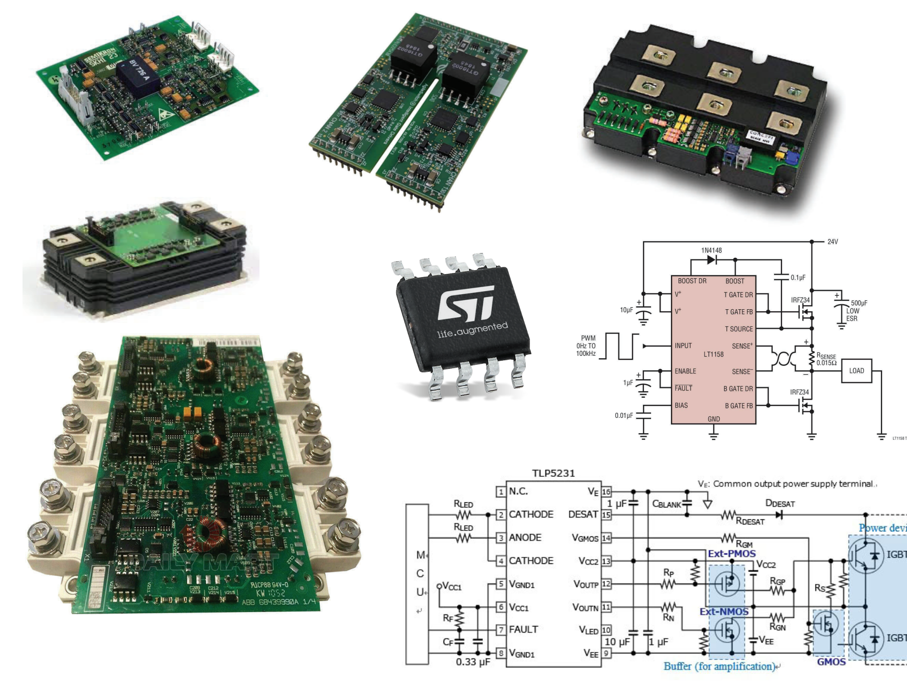
- Turn on
- Turn off
- Protection
- Monitoring
- Communication

Features

- Power supply (isolated, Bootstrap,...)
- De-saturation (short circut protection)
- Undervoltage monitoring
- Interlocking time management (in dual GD)
- Active Miller Clamp
- TSEP supervision
- Error handling
- ...

Realizations

- Many dedicated ICs (driver core)
- Integration of desired features
- Analogue vs. digital
- Integration with/into device
- ...



▲ Various IGBT Gate Driver realizations

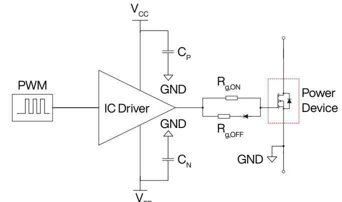
GATE DRIVING OF SIC DEVICES

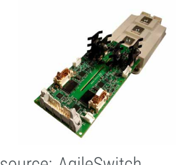
Reliability-oriented gate driving of SiC devices

IMPORTANCE AND CHALLENGES

Gate driver: the link between the control and the power

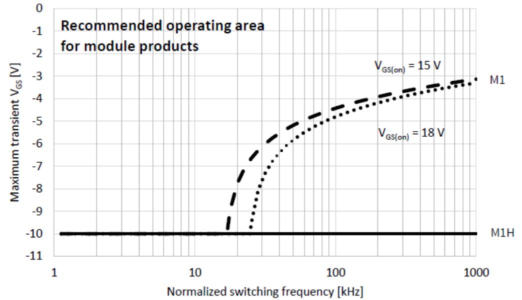
- Suitable gate driving voltage window
- Protection
- High speed switching capability



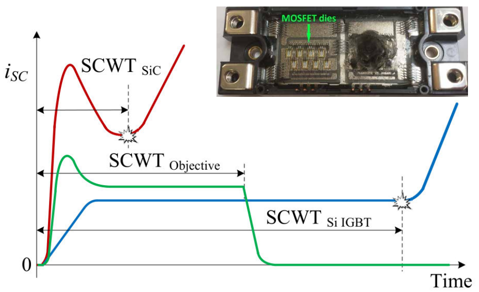


▲ source: AgileSwitch

▲ source: EPFL Racing Team



▲ source: Infineon

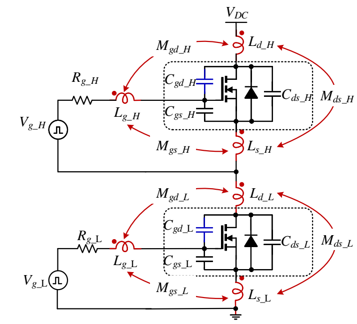


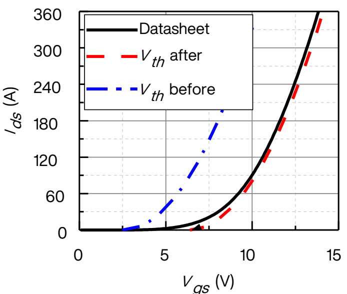
▲ Short circuit withstanding time.

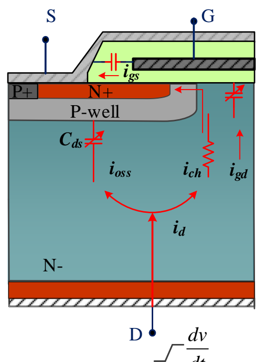
⇒ Realizing reliable and noise-free gate driving of SiC MOSFET is challenging

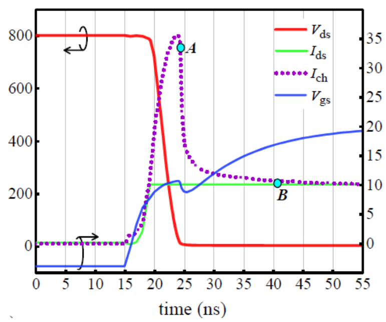
Analyze the influence of parasitics on the switching of SiC MOSFETs

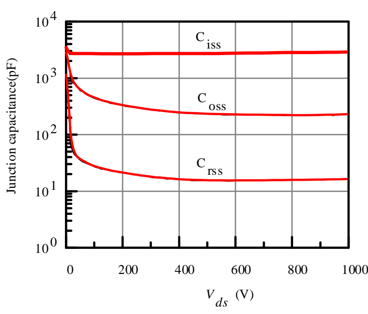
- Coupling of common source inductance
$$L_s = \begin{bmatrix} L_{dd} & M_{ds} & M_{dg} \\ M_{sd} & L_{ss} & M_{sg} \\ M_{gd} & M_{gs} & L_{gg} \end{bmatrix}$$
- Nonlinear junction capacitance
$C_{oss} = f(v_{ds})$
- Channel current introduces heat generation [2]
$i_{ch} = i_d - i_{ch}$, where $i_{ch} = k_m(v_{gs} - V_{th})^2$







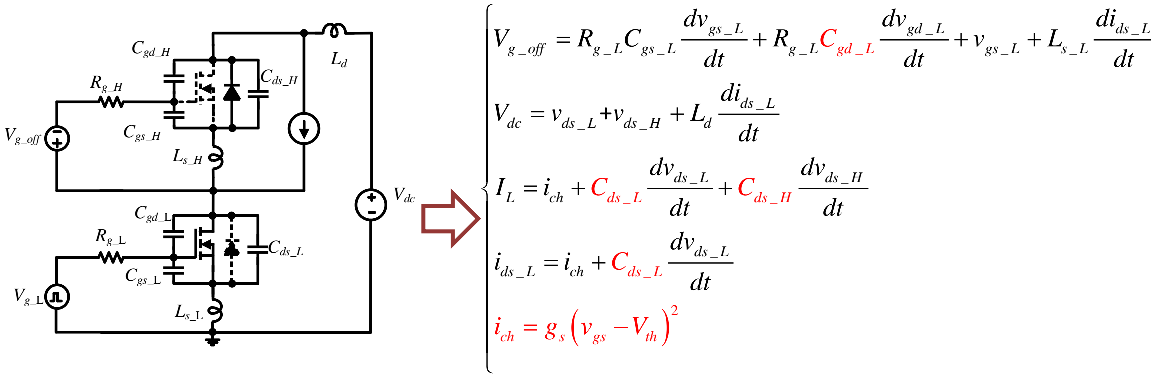




HIGH-SPEED SWITCHING OF SIC MOSFETS - CIRCUIT MODEL

Modeling of switching characteristics of SiC MOSFETs

- Nonlinear junction capacitance
- Influence of the common source inductance
- Influence of the C_{oss} charging and discharging current



Nonlinear differential equations

Case by case simplifications are required based on different configurations and switching stage [3] [4].

HIGH-SPEED SWITCHING OF SIC MOSFETS - SWITCHING PROCESS

Modeling of switching characteristics of SiC MOSFETs

$t_1 - t_2$: Drain-source current rising stage.
$\frac{dv_{ds}}{dt} \approx 0, \frac{di_{ds}}{dt} > 0$

$t_2 - t_3$: Drain-source voltage falling stage.
$\frac{di_{ds}}{dt} \approx 0, \frac{dv_{ds}}{dt} < 0, \frac{dv_{gs}}{dt} \approx 0$

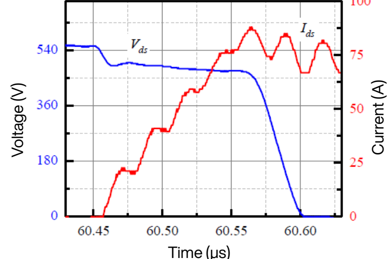
$t_5 - t_6$: Drain-source voltage rising stage.
$\frac{di_{ds}}{dt} \approx 0, \frac{dv_{ds}}{dt} > 0, \frac{dv_{gs}}{dt} \approx 0$

$t_6 - t_7$: Drain-source current falling stage.
$\frac{dv_{ds}}{dt} \approx 0, \frac{di_{ds}}{dt} < 0$

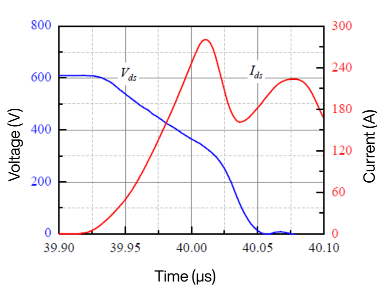
Common source inductance $Ls \approx 0$

Common source inductor has significant influence on high speed switching

- $\frac{di}{dt}$ is limited by common source inductor
- Switching loss is higher due to reduced speed



▲ Turnon waveform for $L_s = 4.8nH$, 560V and 70A.



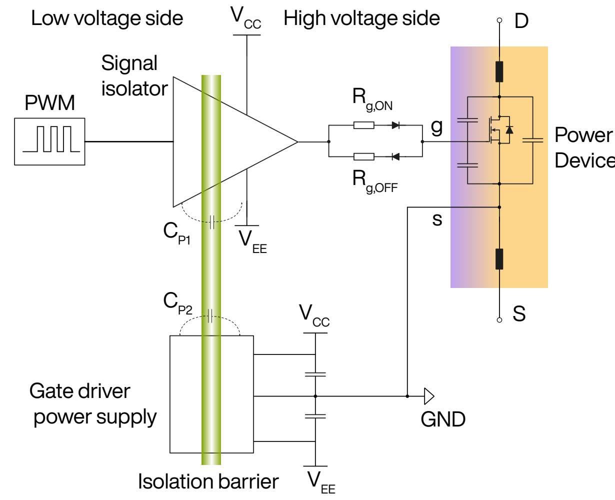
▲ Turnon waveform for $Ls = 0$, 600V and 200A.

High common source inductance

CRITICAL ISSUES REGARDING GATE DRIVING OF SIC MOSFETS

Basic elements of a gate driver:

- Positive gate driving voltage
- Negative gate voltage
- Gate driver resistor
- Signal isolator
- Auxiliary power supply
- Common Mode Transient Immunity (CMTI)
- Crosstalk voltage suppression
- Short circuit protection
- Overvoltage protection
- Digital gate driver

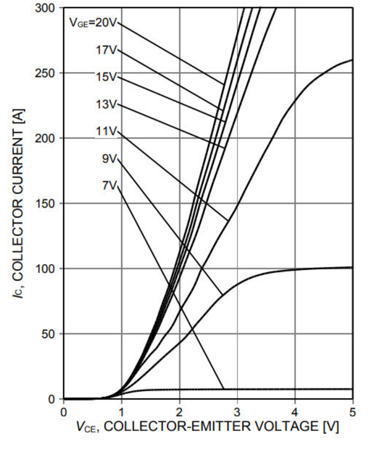


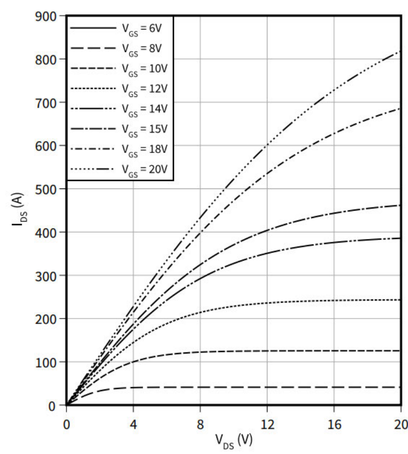
▲ Source: Infineon [5] [6].

POSITIVE GATE VOLTAGE

Tradeoff between short circuit withstanding capability and on state voltage drop:

- Higher positive gate source voltage brings less conduction loss
- Higher positive gate source voltage brings higher short circuit current





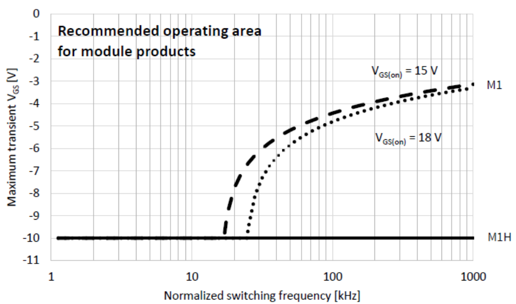
▲ Source: Infineon. Left: 1.2kV/150A Si IGBT, IKY75N120CS6. Right: 1.2kV/127A SiC MOSFET, IMW120R014M1H

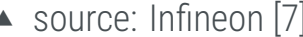
⇒ Auxiliary power supply voltage should be carefully monitored

OFF-STATE GATE VOLTAGE

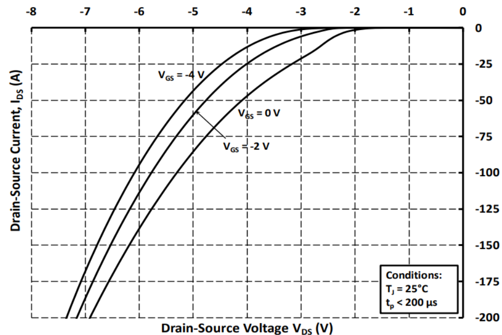
Tradeoff between reliability and false turnon of the device:

- Lower gate-source voltage put more stress to the weak gate oxide of the device
- Lower threshold voltage of SiC MOSFET. Higher gate-source voltage increases risk of false turnon
- Lower gate-source voltage brings more third-quadrant conduction loss





▲ source: Infineon [7]

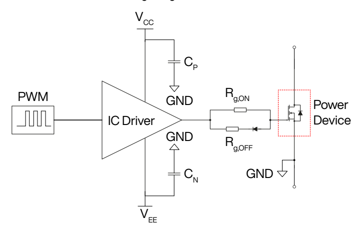


▲ source: Wolfspeed, CPM3-1200-0021A.

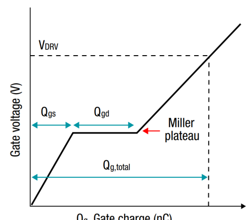
⇒ Tolerable negative gate source voltage of SiC MOSFET is much smaller than Si IGBT

Fully control of power switch is realized by changing gate source voltage (R_g, v_g)[5]

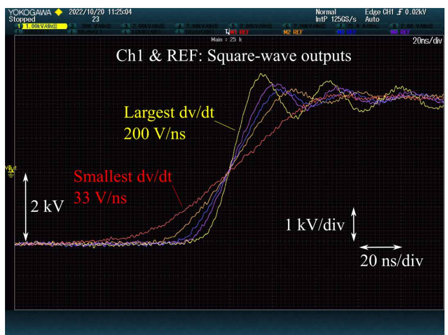
- voltage slew rate - from load requirement
  $$\frac{dv_{ds}}{dt} = \frac{1}{C_{gd}} \frac{V_G - V_{miller}}{R_g}$$
- Current slew rate - from voltage overshoot
  $$\frac{di_{ds}}{dt} = 2k_m(v_{gs} - V_{th})\frac{v_{gs}}{dt}$$

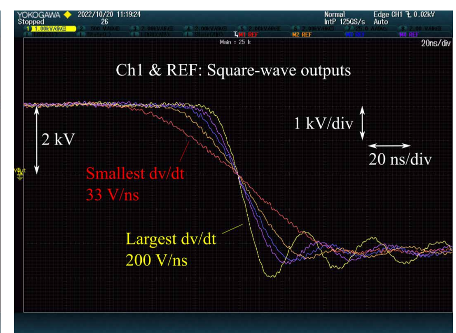


▲ Gate driver structure.



▲ Gate charge curve from the device datasheet.





▲ Dependence of turn off dv/dt on gate driving resistance.

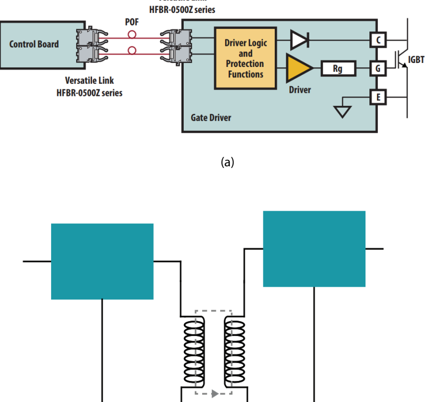
SIGNAL ISOLATOR

Types [8][9][10]

- Fiber Optics (a)
- Optocoupler (b)
- Coreless transformer (c)
- Transformer with magnetics (c)
- capacitive coupling (d)

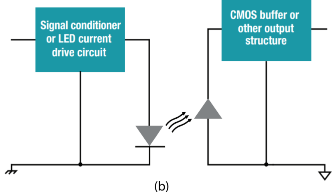
Selection Considerations

- Isolation voltage
- Common mode transient immunity
- Temperature
- Time delay

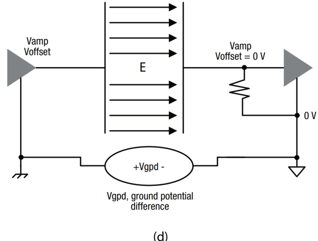


(a)

(c)



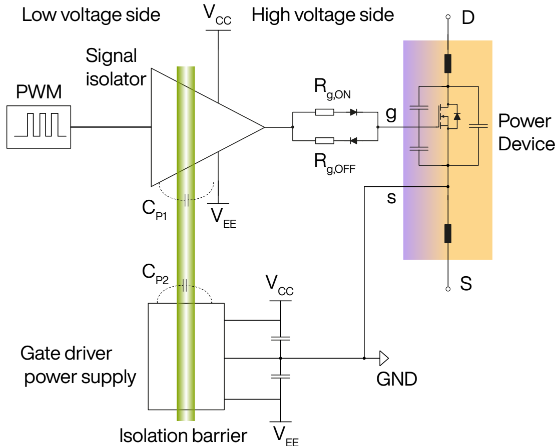
(b)



(d)

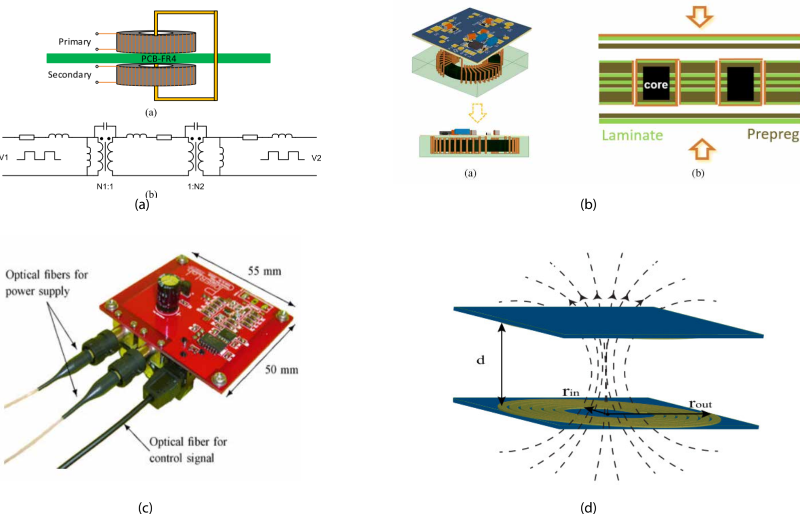
Selection consideration [11] [12]

- Higher accuracy of the power supply
- Enough gate driving power
- Importance of isolation voltage
- Lower coupling capacitance between primary side and secondary side



Novel gate driver isolator concept

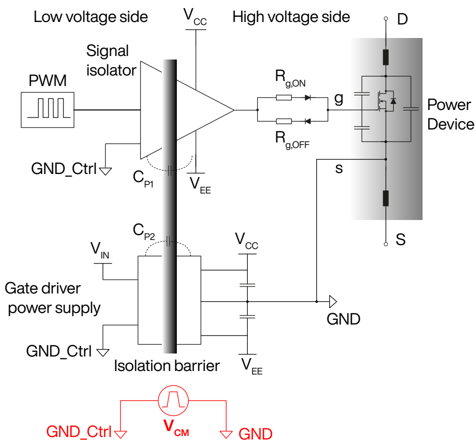
- Coupled inductor [13]
- PCB embedded transformer [14]
- Optic isolated power supply [15]
- Wireless power transfer [16] [17]

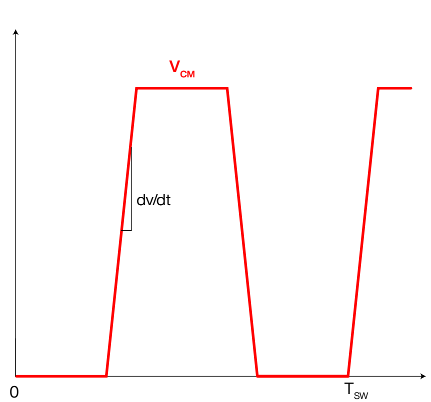


COMMON MODE TRANSIENT IMMUNITY

Common mode transient immunity [18]

- Avoid false triggering of PWM > 100V/ns
- Reduce EMI on low voltage circuits





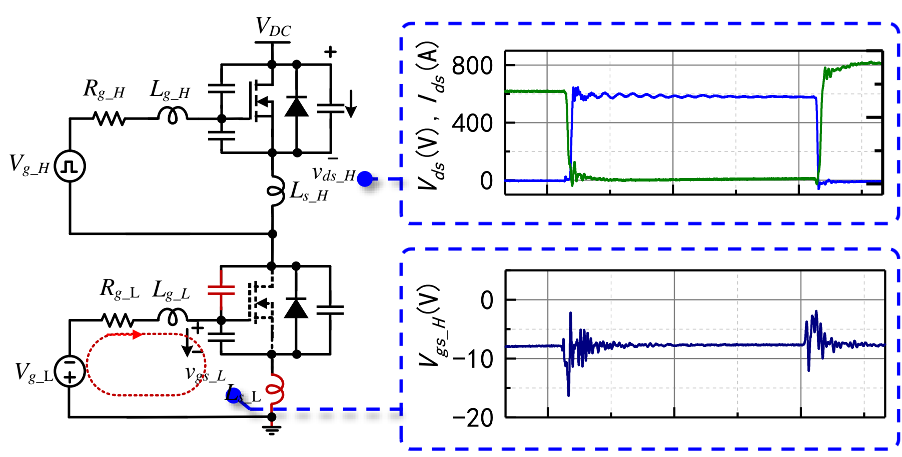
PROTECTION OF SIC DEVICES

Crosstalk Phenomenon Elimination

WHAT IS CROSSTALK PHENOMENON?

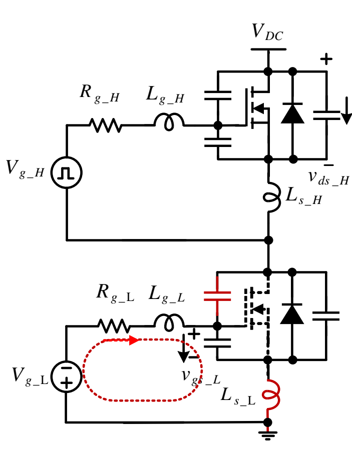
The coupling between gate loop and power loop

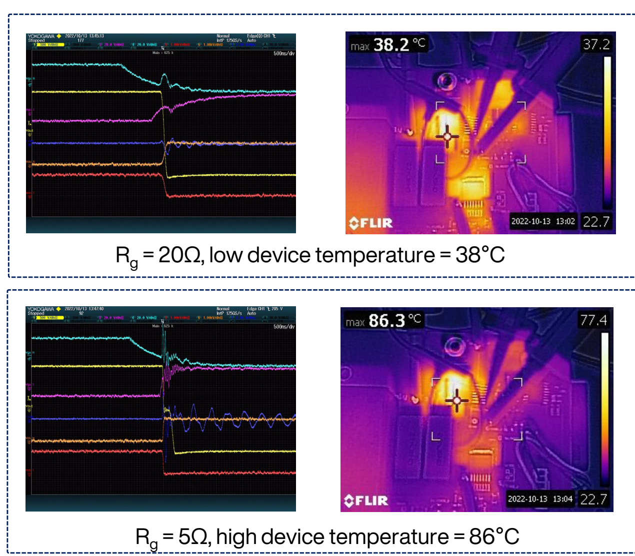
- Gate-drain capacitance
- Common source inductance



Side effect cause by crosstalk phenomenon

- Unwanted turn-on introduce extra power loss
- Overstress of the weak gate oxide of SiC MOSFETs



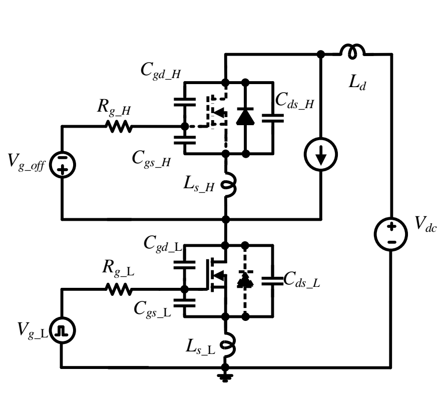


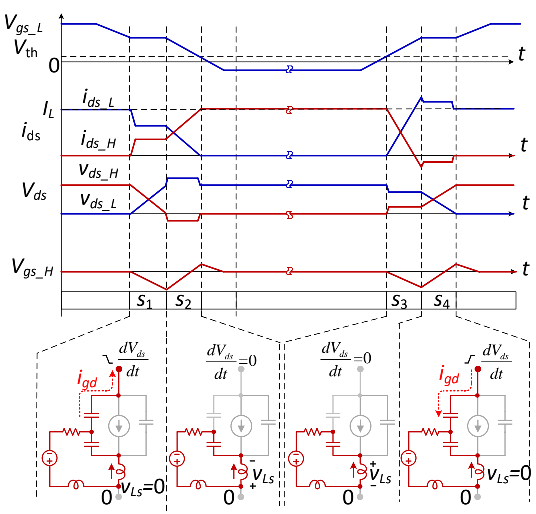
R_g = 20Ω, low device temperature = 38°C

R_g = 5Ω, high device temperature = 86°C

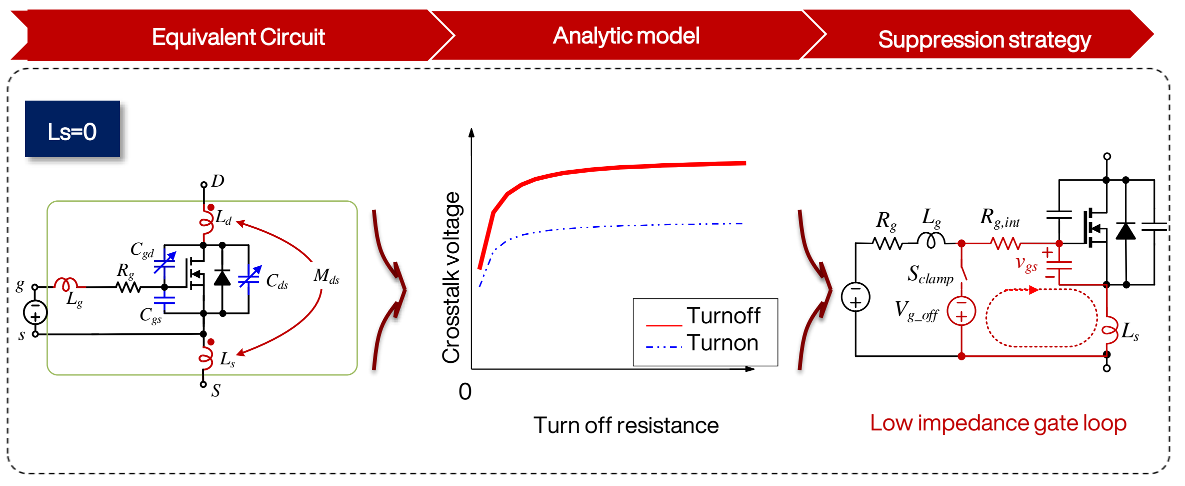
Based on device switching model

- Symmetrical complementary devices during switching
- Analytic model based on the active device model





For devices without common source inductor

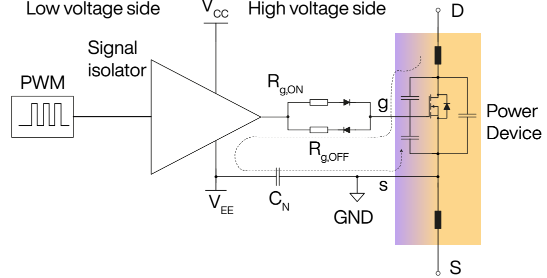


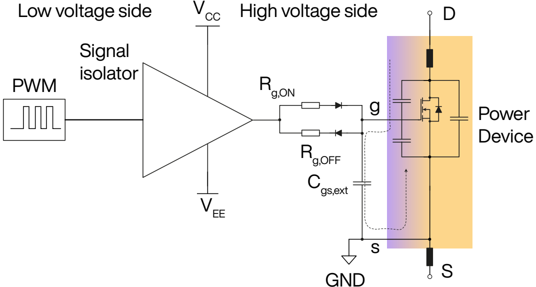
⇒ Creating low impedance gate loop during off-state is of vital importance

CROSSTALK VOLTAGE ELIMINATION - ADDING PARALLEL CAPACITOR

For devices without common source inductor

- Negative gate source voltage [19]
- Added gate-source capacitor [20]

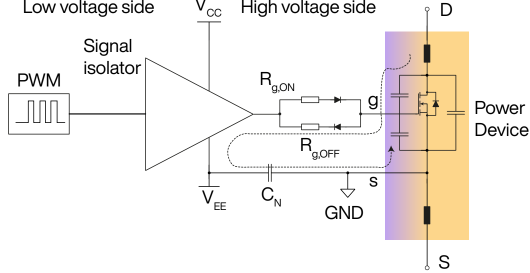


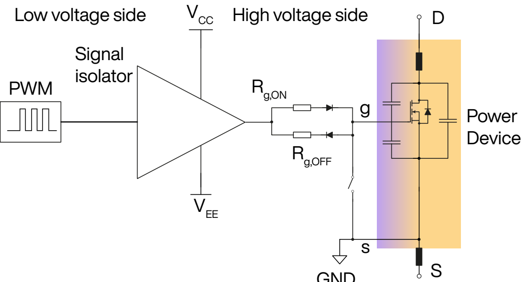


CROSSTALK VOLTAGE ELIMINATION - ACTIVE MILLER CLAMP

Method reported in 2006 [21]

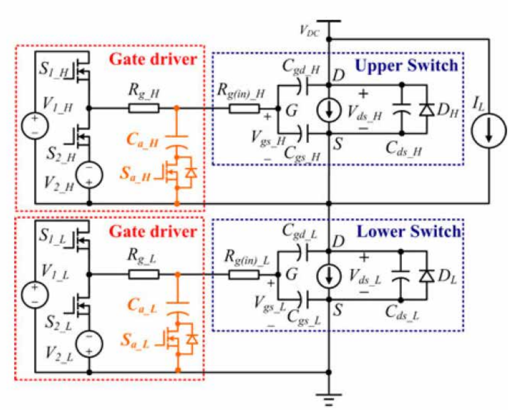
- Gate source voltage is sensed and compared with a lower value
- Clamping branch to bypass the turnoff resistor

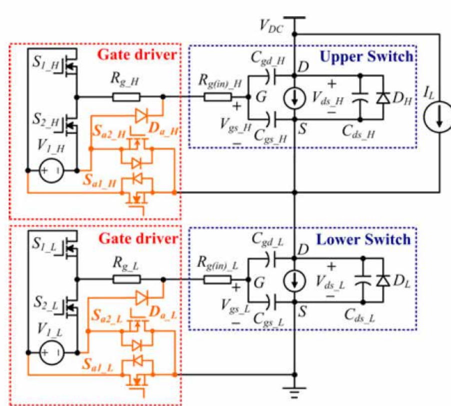




Active gate driver [22]

- Large internal gate resistance cancels with the effectiveness of Miller clamp circuit
- Precharge/discharge gate source capacitor during different phases of switching device

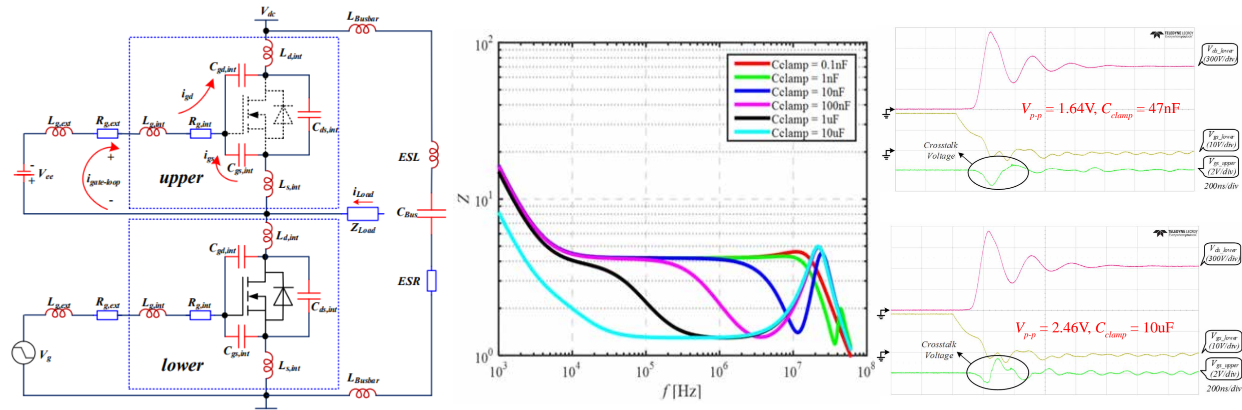




DESIGN CONSIDERATIONS FOR ACTIVE MILLER CLAMP

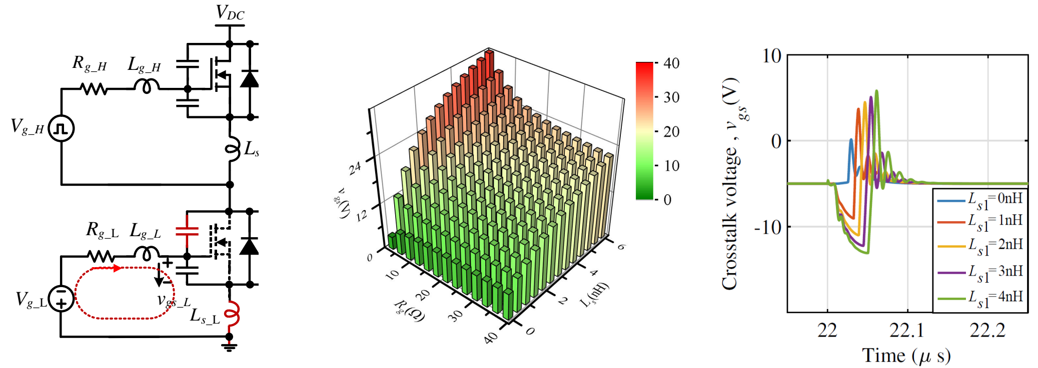
Influence of loop parasitic parameters [23]

- Clamping circuit should be palced as close to gate as possible
- Clamping loop impedance coordination between gate loop and the power loop oscillation frequency



Influence of common source inductor [4]

- Influence of the common source inductor cannot be bypassed by low impedance off-state gate loop
- Measurement of gate source voltage is incorrect

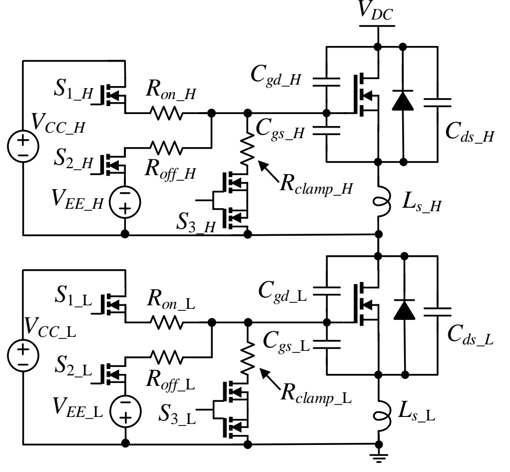


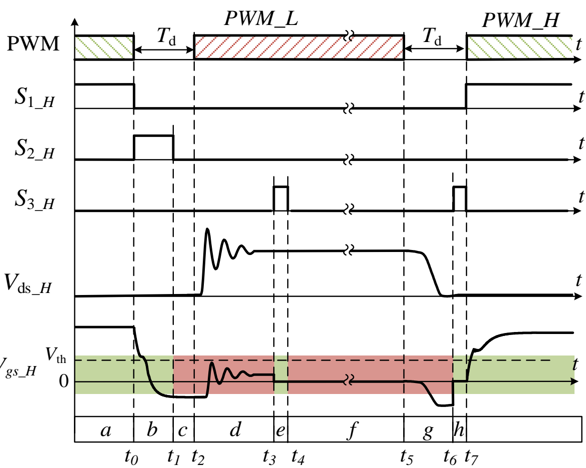
Simply reducing off-state impedance may even increase the crosstalk voltage

HIGH OFF-STATE IMPEDANCE GATE LOOP CROSSTALK VOLTAGE ELIMINATION

A bidirectional clamping branch is added in parallel with the gate-source capacitor [4]

- High off-state impedance gate loop to bypass influence of common source inductor
- Pre-charged negative gate-source voltage to eliminate influence of gate-drain capacitor





HIGH OFF-STATE IMPEDANCE GATE LOOP CROSSTALK VOLTAGE ELIMINATION

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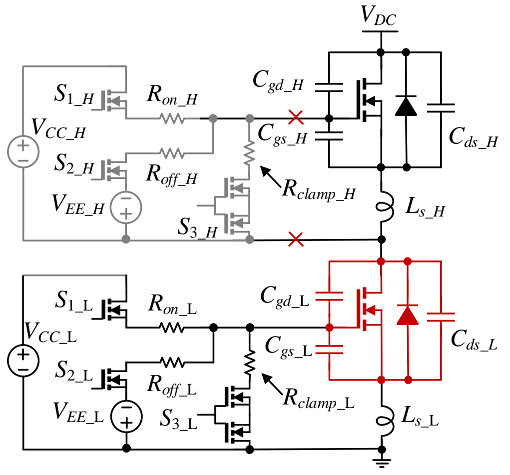
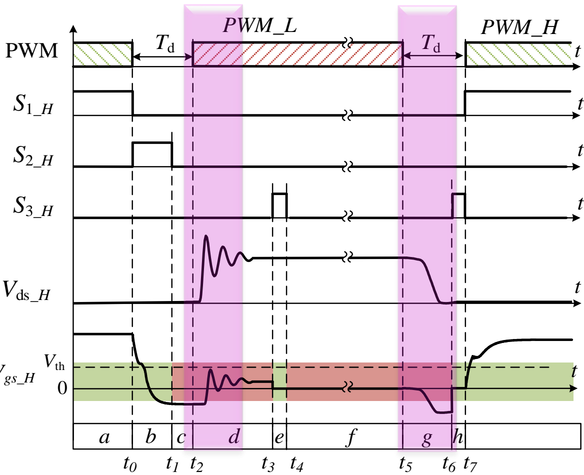
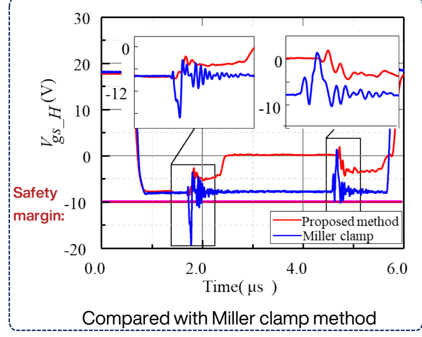


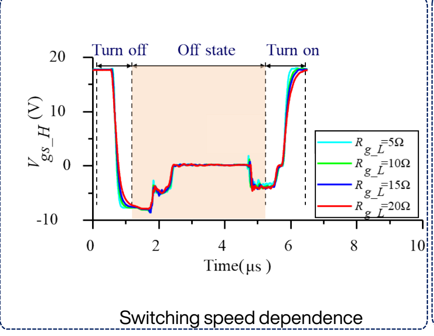


EXPERIMENTAL VERIFICATION

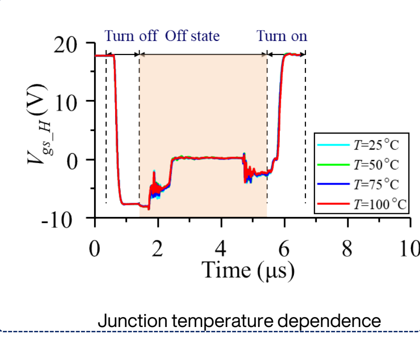
- Peak negative gate source voltage is greatly reduced
- Crosstalk voltage is independent of switching speed
- Crosstalk voltage is independent of junction temperature



Compared with Miller clamp method



Switching speed dependence

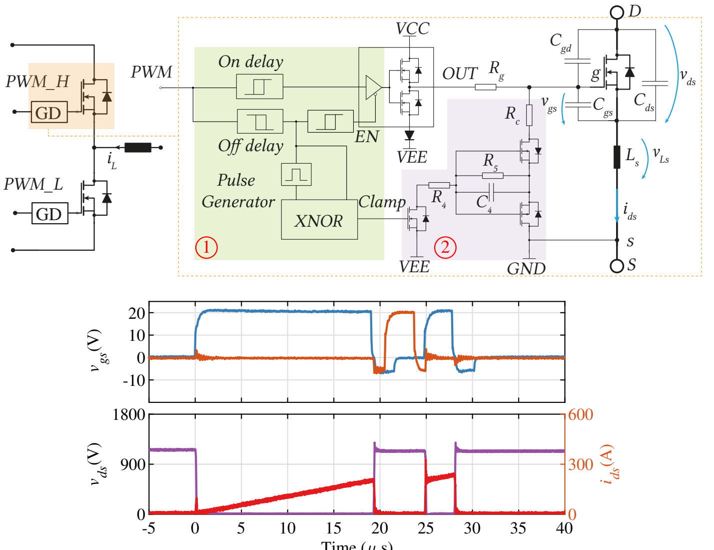


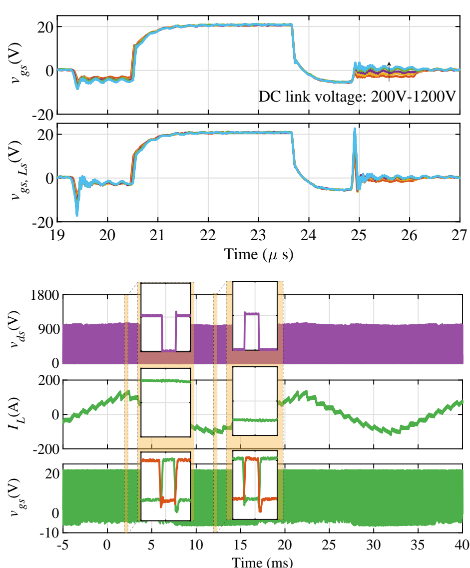
Junction temperature dependence

⇒ Suitable for high speed switching

An improved version [4]

- Bidirectional switch based on p-MOSFETs
- No extra control signals are required
- Zero negative gate -source voltage for most of time



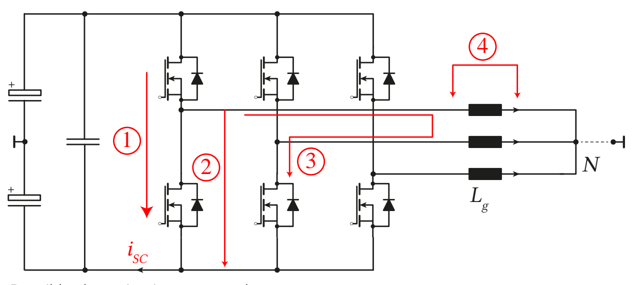


PROTECTION OF SIC DEVICES

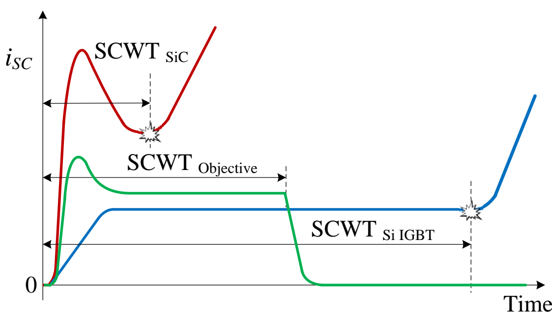
Short-circuit protection of SiC MOSFETs

Short-circuit (SC) withstanding time (SCWT) of SiC MOSFET is much shorter than Si IGBT

- Much smaller chip size for the same current ratings - 5 times smaller roughly
- Large short circuit current - much higher than 10 times rated current
- Gate oxide is sensitive to over temperature - reliability issue
- Extremely high dv/dt - as high as 100V/ns



▲ Possible short-circuit current paths.

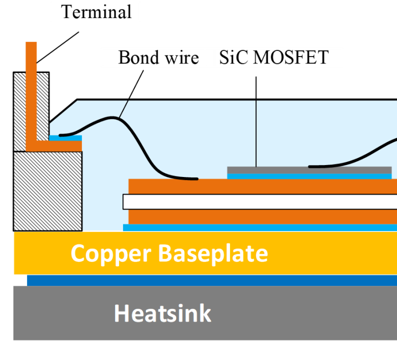


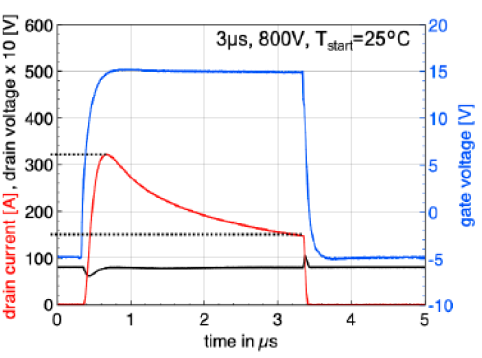
▲ Short-circuit Withstanding Time comparison: Si IGBT vs. SiC MOSFET

⇒ Objective: realizing ultra-fast detection, noise immune short-circuit protection for SiC MOSFETs

MODELING OF SHORT CIRCUIT CAPABILITY

- Short circuit current
  $i_{SC} = k(v_{gs} - v_{th})^2$
- Short circuit energy density [24]
  $E_{SC} = \int_0^t v_{ds} i_{SC}\, dt = A\rho C_p d(T_C - T_A)$
- Failure mode after short circuit [7]
  Thermal runaway of the devices; Melting of metal connections





DESAT PROTECTION

Method

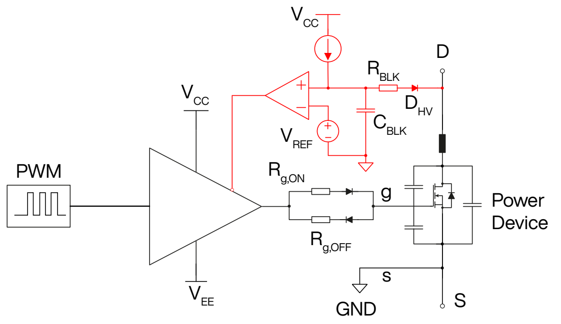
- On-state voltage drop across device is measured compared with reference value
- Blanking time is inserted to bypass the influence of switching transition

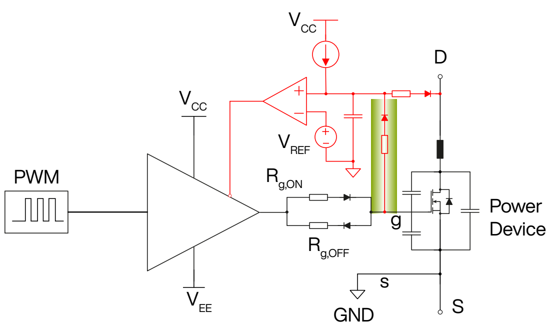
Design

- Voltage at DESAT:
  $V_{DESAT} = I_{DESAT}R_{BLK} + V_{D,HV} + V_{ds}$
- The blanking time is set by C_{BLK}: $C_{BLK} = \frac{C_{BLK}V_{DESAT}}{I_{DESAT}}$

Challenges

- Blanking time limits the response speed
- There is no knee voltage on V_{ds} of SiC MOSFETs



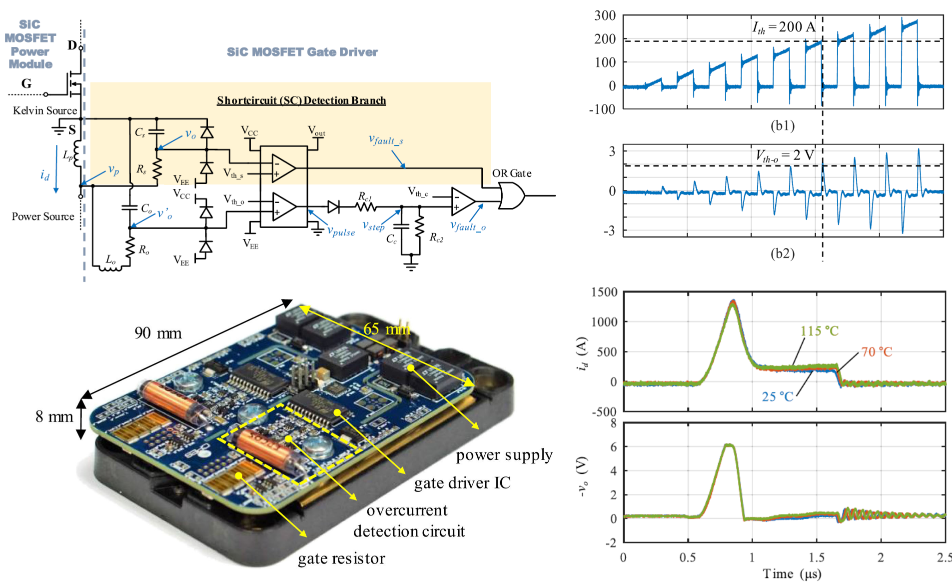


▲ [25].

⇒ DESAT protection of SiC MOSFETs requires accurate detection and fast response speed

SC current sensing with loop leakage inductor

- Voltage across leakage inductor is adopted
- An integrator is adopted to re-construct the SC current
- Two types of filter is adopted to identify the SC and over current event



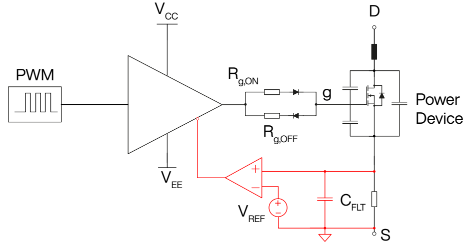
▲ [26].

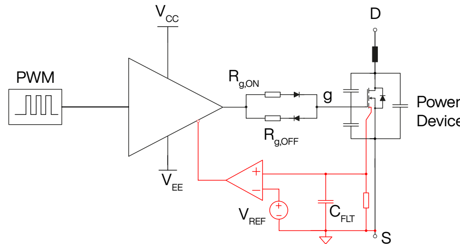
Solution

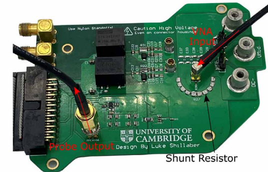
- Current sensing with series connected shunt resistor [27] [28]
- Current sensing with parallel connected SenseFET [29]

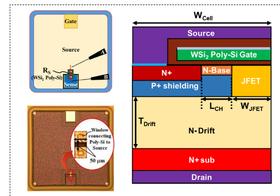
Characteristics

- Non-isolated current detection
- High response speed







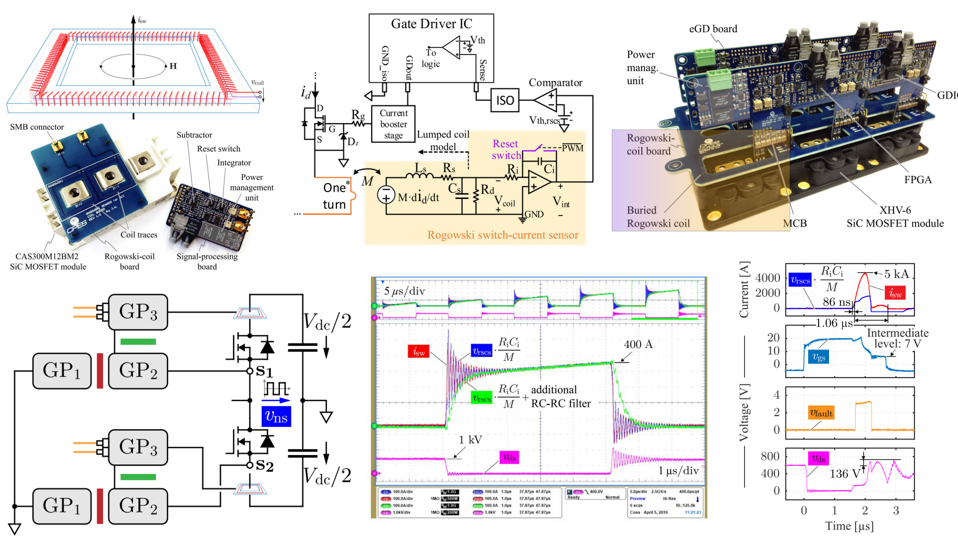


SC current sensing with Rogowski Coil [30]

- Voltage across leakage inductor is detected
- An integrator is adopted to re-construct the SC current

Characteristic

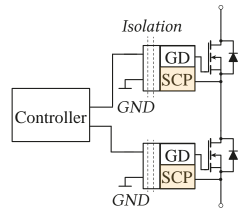
- For AC current only
- Isolated current detection



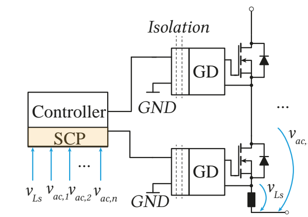
▲ [30].

TWO-STEP SHORT CIRCUIT PROTECTION

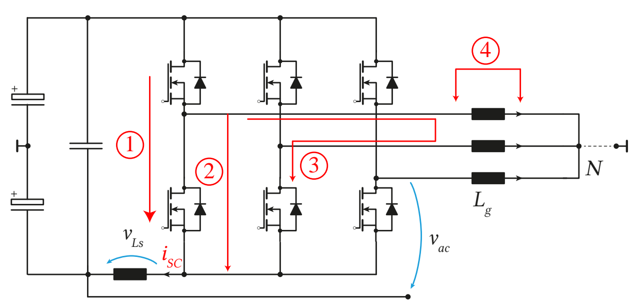
- Centralized protection - compact design, suitable for devices in series/parallel
- Two-level turnoff - extended SCWT of devices
- Detection of SC current to DC capacitor - fast response
- Detection of SC AC voltage at phase leg output - high accuracy



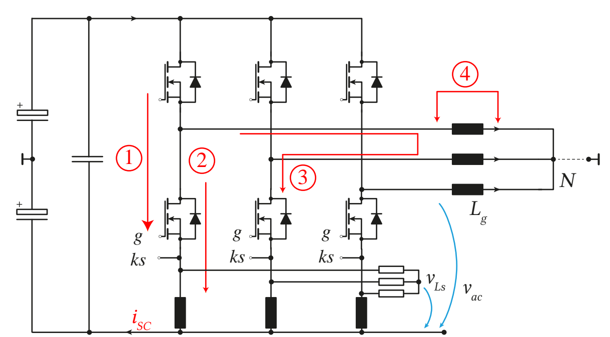
▲ Architecture of conventional GD.



▲ Architecture of proposed GD.



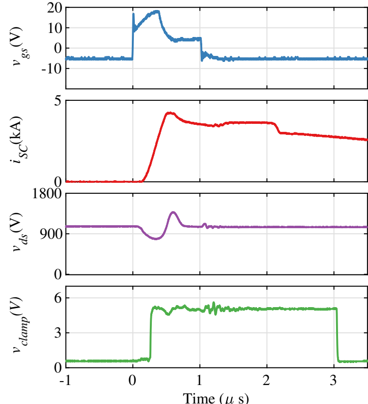
▲ Configuration of converter with a common stray inductor.



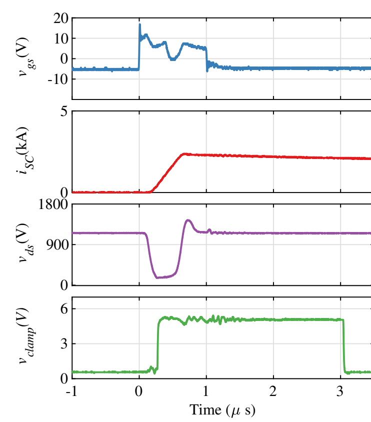
▲ Configuration of converter with multiple Kelvin source terminals.

EXPERIMENTAL VERIFICATION

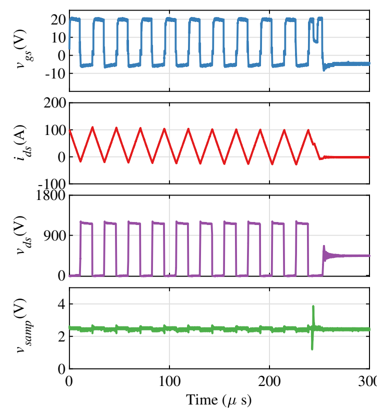
- SC current detected within 300ns
- Two-step short circuit protection with extended SC withstanding time
- False protection will be released after clamping time



▲ SC protection under $L_{SC} = 4nH$.



▲ SC protection under $L_{SC} = 580nH$.

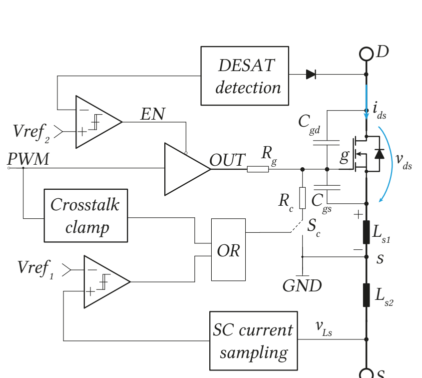


▲ Continuous switching / false triggering.

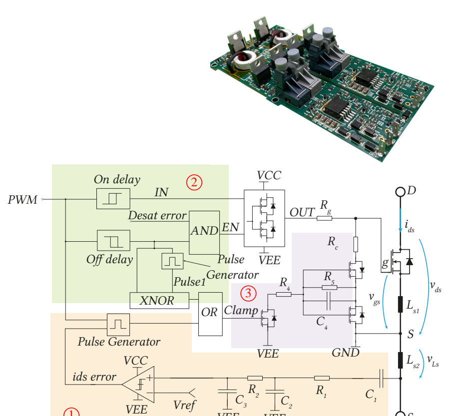
GATE DRIVER WITH SC PROTECTION AND CROSSTALK VOLTAGE ELIMINATION

Combined short circuit protection and crosstalk voltage suppression

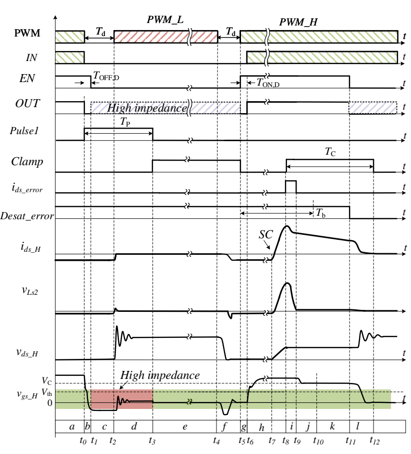
- High off-state Impedance gate driver
- Two level SC protection – increased SC withstanding time



▲ Structure of the gate driver.

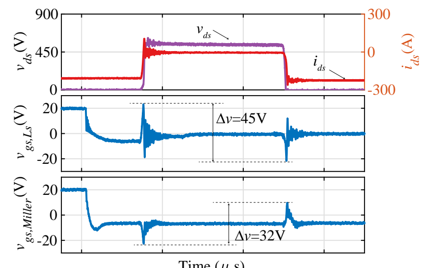


▲ Detailed implementation.

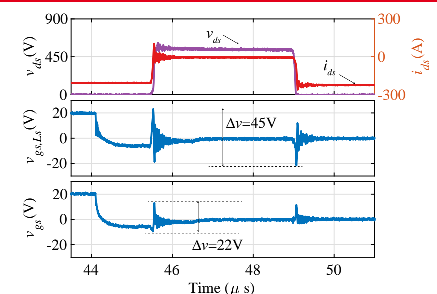


▲ Time sequence.

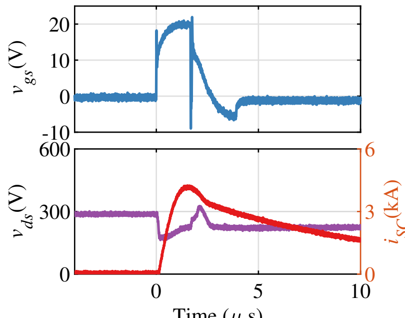
EXPERIMENTAL VERIFICATION



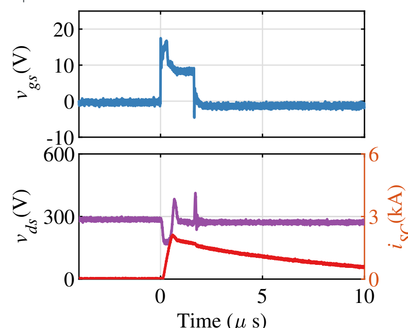
▲ Miller Clamp method.



▲ High off-state impedance method.



▲ DESAT protection method.



▲ Two-stwp protection method.

? A solution for trade-off among reliability and high speed switching?

PROTECTION OF SIC DEVICES

Measurement and sensing

Double pulse test procedure

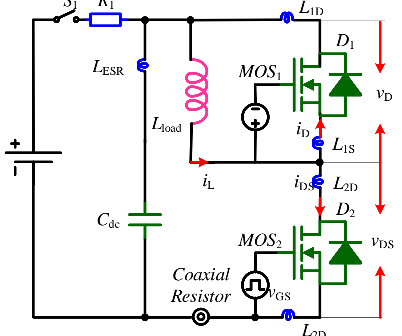
- First pulse to build up current
- t_1: Turn-off of the device under test
- Second pulse for freewheel of load current
- t_2: Turn-on of the device under test

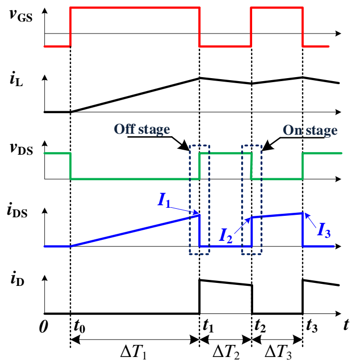
Information acquisition

- Switching speed
- Switching loss
- Reverse recovery waveform
- Switching at different currents/voltages
- Switching under different temperatures
- Loop parasitic parameters
- ...

Benefits

- Safer and faster test
- Early phase design verification





ELECTRICAL SIGNAL MEASUREMENT

Probe selection

- Enough accuracy
- Safety
- Less complexity

Voltage measurement

- Normal non-isolated probe
- High voltage passive probe
- Differential probe
- Optical isolated voltage probe - IsoVu Isolated Probes

Current measurement

- Shunt resistor
- Rogowski coil
- Hall Effect sensor
- Current transformer

BASIC PRINCIPLE IN SELECTION OF PROBE

Bandwidth and 10%-90% rise time

$$BW = \frac{0.35}{t_r}$$

Total rise time of cascaded system

$$t_{rise,t} = \sqrt{t_{rise,1}^2 + t_{rise,2}^2 + \ldots + t_{rise,n}^2}$$

CMRR of the probe

$$V_{measure} = A_c(V_{DIFF} + \frac{V_{CM}}{CMRR})$$

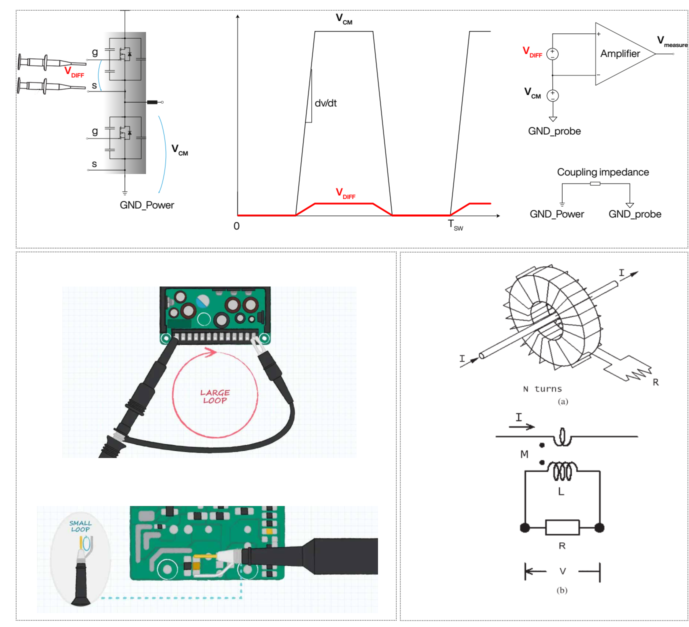
CMRR should be as large as possible

Measurement consideration

- Measurement should be as less as possible
- Different delay among current measurement and voltage measurement

Influence of probe on measurement [31]

- Shunt has its own impedance
- Current transformer introduce extra impedance
- Probe has input impedance, e.g. 50Mohm



COFFEE BREAK

Well deserved...

HIGH POWER CONVERTERS

What are the application areas for SiC devices

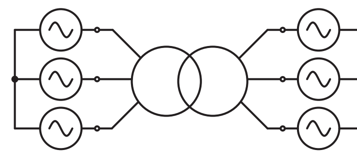
SOLID-STATE TRANSFORMER (SST)

Can SiC make a difference?

- SST = Switching stages + Isolation
- Firstly envisioned within AC grids
- Variety of Power Electronic Building Blocks (PEBBs)
- Conventional transformer vs SST?
- Operating frequency increase **(MFT)**

	Grid Tx	SST
Controlability	No	Yes
Efficiency	$\eta \geq 99\%$	$P_?$
Q compensation	No	Yes
Fault tolerance	No	Yes
Size	Bulky	Compact
Cost	Low	High

Advantages at the expense of cost and reduced efficiency!



▲ Conventional AC grid transformer

▲ Solid-State Transformer employed with the aim of interfacing two AC systems **2007_Akagi_TPEL**, **2014_Kolar_IPEC**

SOLID STATE TRANSFORMER FOR TRACTION (ABB - 1.2MW PETT)

Characteristics

- 1-Phase MVAC to MVDC
- Power: 1.2MVA
- Input AC voltage: 15kV, 16.7Hz
- Output DC voltage: 1500 V
- 9 cascaded stages (n + 1)
- input-series output-parallel
- double stage conversion

99 Semiconductor Devices

- HV PEBB: 9 x (6 x 6.5kV IGBT)
- LV PEBB: 9 x (2 x 3.3kV IGBT)
- Bypass: 9 x (2 x 6.5kV IGBT)
- Decoupling: 9 x (1 x 3.3kV Diode)

9 MFTs

- Power: 150kW
- Frequency: 1.75kHz
- Core: Nanocrystalline
- Winding: Litz
- Insulation / Cooling: Oil

▲ ABB PETT scheme [32], [33]

Retrofitted to shunting locomotive

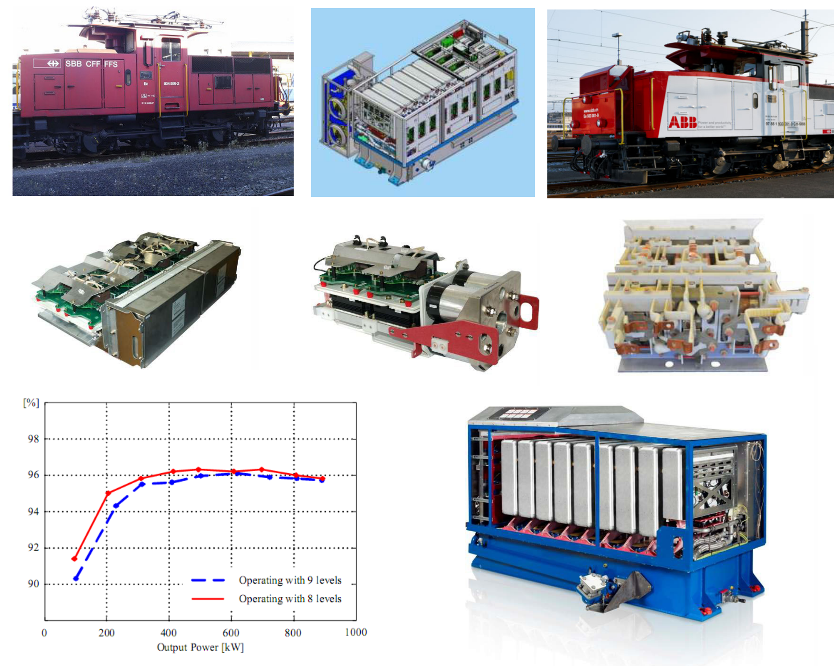
- Replaced LFT + SCR rectifier
- Propulsion motor - 450kW
- 12 months of field service
- No power electronic failures
- Efficiency around 96%
- Weight: ≈ 4.5 t

Technologies

- Standard 3.3kV and 6.5kV IGBTs
- De-ionized water cooling
- Oil cooling/insulation for MFTs
- n + 1 redundancy
- IGBT used for bypass switch

Displayed at:

- Swiss Museum of Transport
- https://www.verkehrshaus.ch

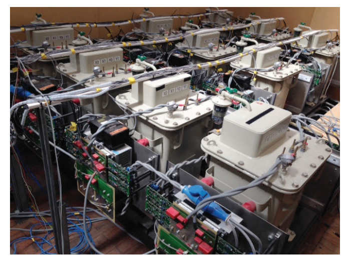


▲ ABB PETT prototype [32], [33]

SOLID-STATE TRANSFORMER - UTILITIES

UNIFLEX-PM

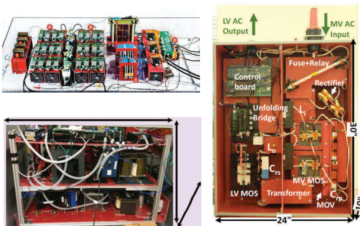
- Reduced scale prototypes



▲ UNIFLEX-PM prototype

FREEDM

- Reduced scale prototypes



▲ FREEDM SSTs [35]

HEART

- Reduced scale prototypes

▲ HEART project

GE

- Full scale prototype

▲ GE prototype [34]

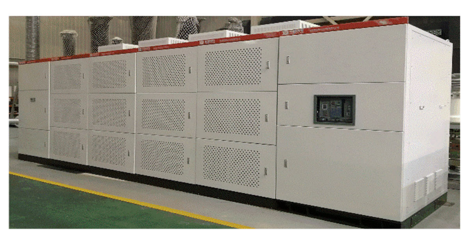
HUST

- Full scale prototype

▲ HUST SST [36]

XD Electric Company

- Full scale prototype



▲ XD Electric Company SST [37]

HUST, WUHAN - 500KVA ELECTRONIC POWER TRANSFORMER - EPT

Ratings

- Power: 500kVA
- Input AC voltage: 10kV, 50Hz
- Output AC voltage: 400V, 50Hz
- Efficiency: 93.72% (at 105 kW)
- Cost: 10x conv. transformer

Topology

- AC-DC + DC-DC + DC-AC
- 6 cascaded stages per phase
- Unidirectional

Semiconductor Devices

- HV side: 3.3kV IGBTs
- LV side: 1.2kV IGBTs?

MFT

- Power: 30kW per MFT
- Frequency: 1kHz
- Core: Iron-based amorphous alloy
- Insulation / Cooling: solid /air

▲ HUST reported EPT [36]

GE - 1MVA - SOLID STATE POWER SUBSTATION

Ratings

- Power: 1MVA
- Input AC voltage: 13.8kV, 60Hz
- Output AC voltage: 270V, 60Hz
- Efficiency: 97% (at 855 kW)
- Remark 1: 3 times the LFT losses
- Remark 2: 1/3 of the LFT weight
- Remark 3: 1/2 of the LFT volume

Topology

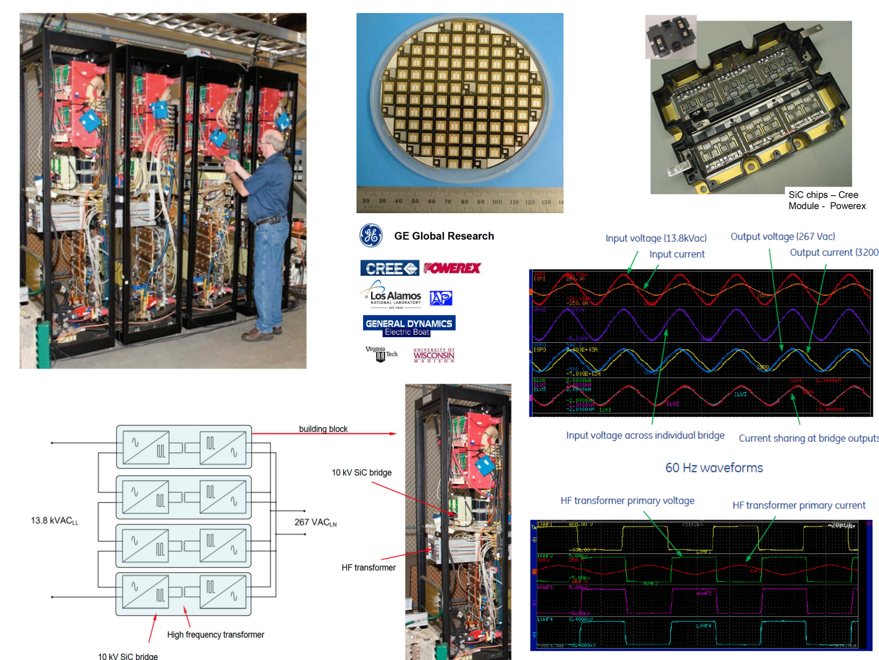
- AC-DC + DC-DC + DC-AC
- 4 cascaded stages per phase
- Input Series Output Parallel

Semiconductor Devices

- HV side: 10kV SiC MOSFET

MFT

- Power: 250kW per MFT
- Frequency: 20kHz
- Core: nanocrystalline
- Insulation / Cooling: oil /water



▲ Solid State Power Substation [34]

PET - 300KVA - LAPLACE, TOULOUSE

Ratings

- Power: 300kVA
- Input DC voltage: 3kV
- Output DC voltage: 1.5kV
- Efficiency: 99%

Topology

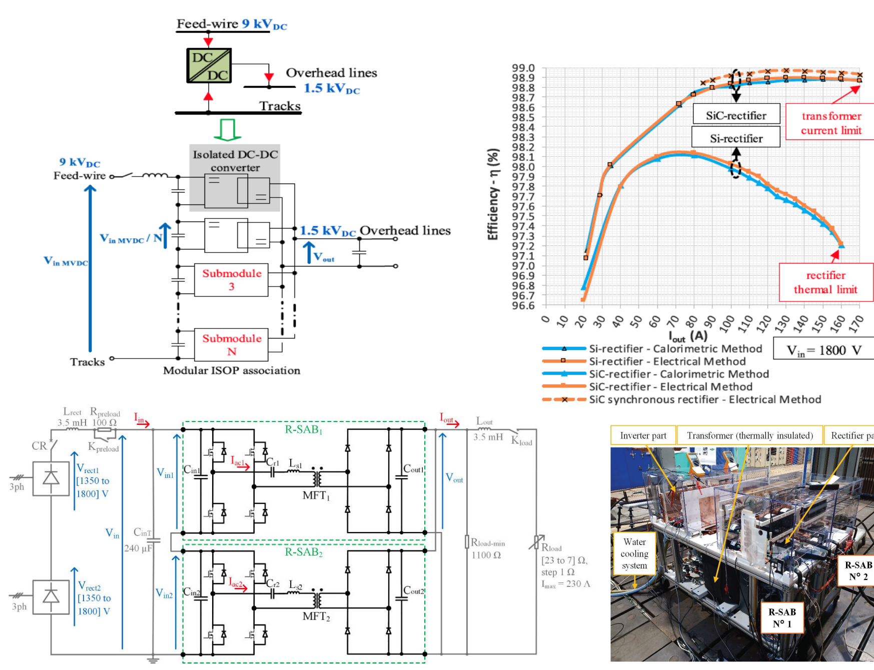
- Back to Back test setup
- DC-DC (SiC SAB cells)
- Input Series Output Parallel

Semiconductor Devices

- HV side: 3.3kV SiC MOSFET
- LV side: 3.3kV SiC MOSFET / 3.3kV Si Diodes

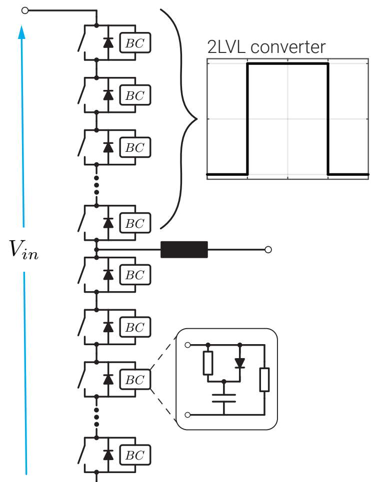
MFT

- Power: 300kW per MFT
- Frequency: 15kHz



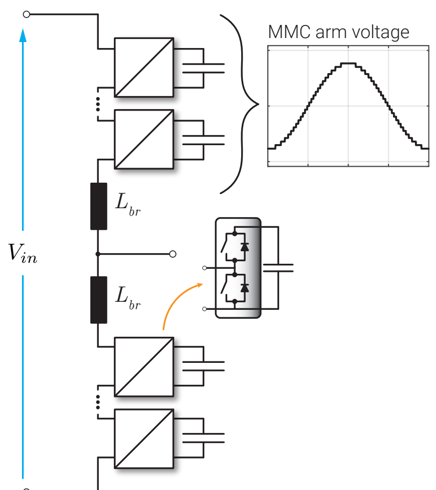
▲ ISOP SAB test setup [38]

HOW TO HANDLE HIGH/MEDIUM VOLTAGES?



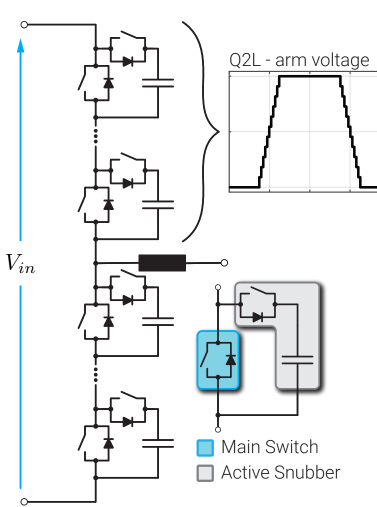
▲ Series connection of switches

- Series connection of switches with snubbers
- Two voltage levels ($n_{LVL} = 2$)
- Two-Level voltage waveforms



▲ Modular Multilevel Converter (MMC)

- Series connection of Submodules (SM)
- n_{LVL} depending upon number of SMs
- Arbitrary voltage waveform generation



▲ Quasi Two-Level (Q2L) Converter [39][40]

- Series connection of MMC-alike SMs
- n_{LVL} depending upon number of SMs
- Quasi Two-Level (trapezoidal) voltage waveform

SIC SERIES CONNECTION - FREEDM

Ratings

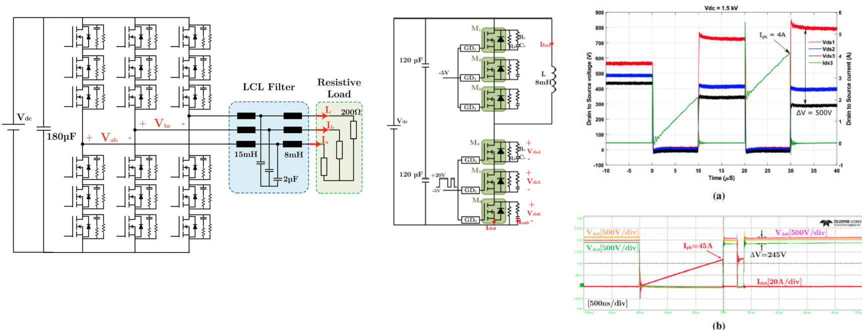
- Power: 100kVA
- Input DC voltage: 7.2kV
- Output AC voltage: 4kV
- Efficiency: 97%

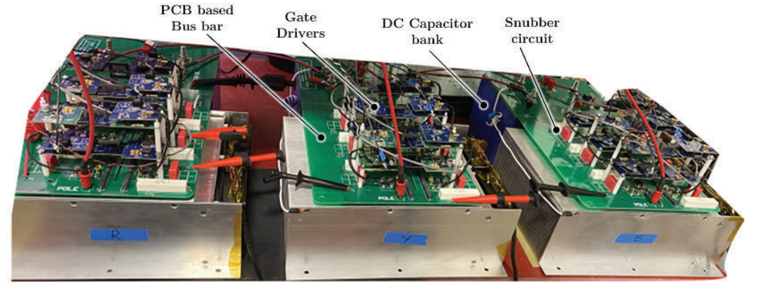
Topology

- Three-phase VSI
- LCL output filter
- 3 series connected 3.3kV MOSFETs

Semiconductor Devices

- 3.3kV SiC MOSFET





▲ Three-phase inverter with series connected SiC devices [41]

HV SIC SST - FREEDM

Ratings

- Power: 100kVA
- Input AC voltage: 4.16kV
- Output AC voltage: 480kV
- Efficiency: 95.5% - one power block 35kW
- 2-phase cooling

Topology

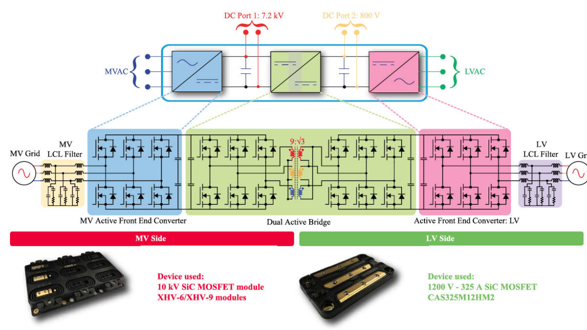
- Three-phase VSI
- Three-phase DAB
- Three-phase VSI

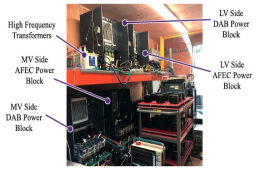
Semiconductor Devices

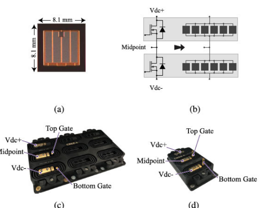
- HV side: 10kV SiC MOSFET
- LV side: 1.2kV SiC MOSFET

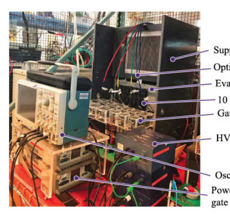
MFT

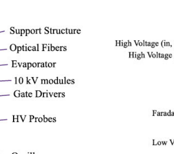
- Power: 100kW per MFT
- Frequency: 10kHz
- Core: nanocrystalline
- Insulation / Cooling: oil /oil

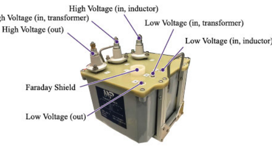












▲ Three-phase AC-AC SST (MUSE-SST) [42], [43]

Ratings

- Power: 100kVA
- Input AC voltage: 13.8kV
- Output AC voltage: 480V
- Efficiency: 97%

Topology

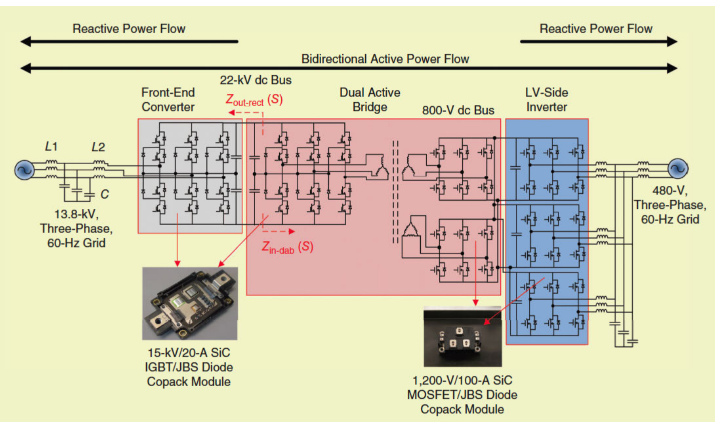
- Three-phase B2B NPC
- Three-phase DAB
- Three-phase VSI

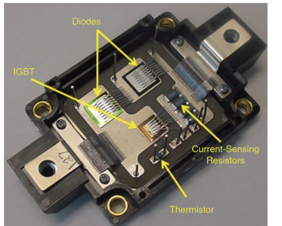
Semiconductor Devices

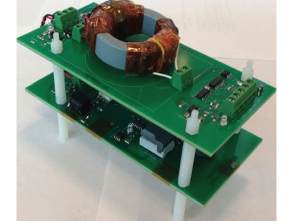
- HV side: 15kV SiC IGBT
- LV side: 1.2kV SiC MOSFET

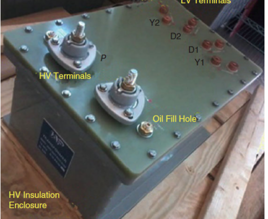
MFT

- Power: 100kW per MFT
- Frequency: 10kHz
- Core: nanocrystalline
- Insulation / Cooling: oil /oil





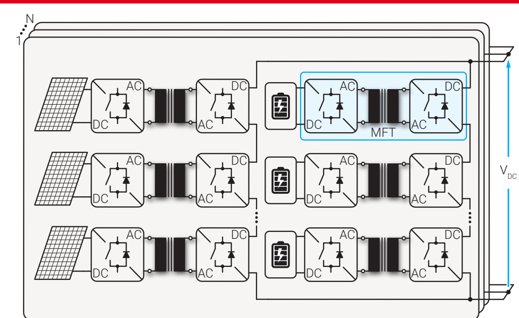




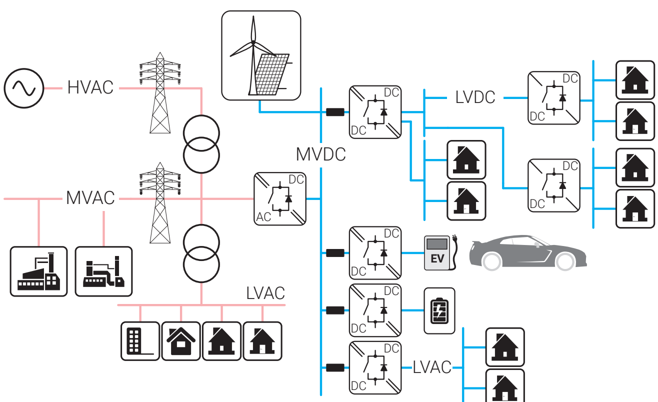
▲ Three-phase SST [44], [45]

DC-DC CONVERTERS

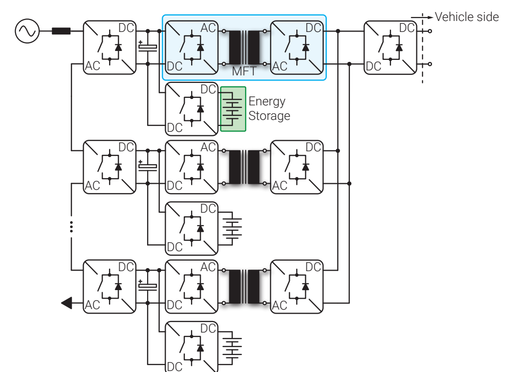
- Inherent part of the almost all SST topologies
- Expansion of the existing power system
- Enabling technology for MVDC
- Penetration of renewable energy sources
- Fast / Ultra Fast EV charging
- **Medium Frequency conversion**



▲ Employment of a DC-DC SST within RES-based systems



▲ Concept of a modern power system

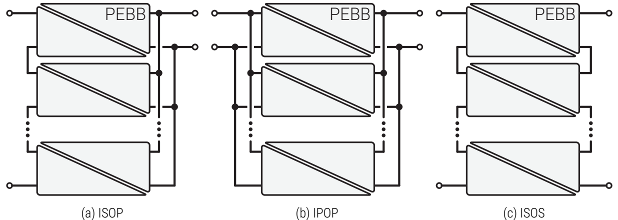


▲ Fast EV charging concept

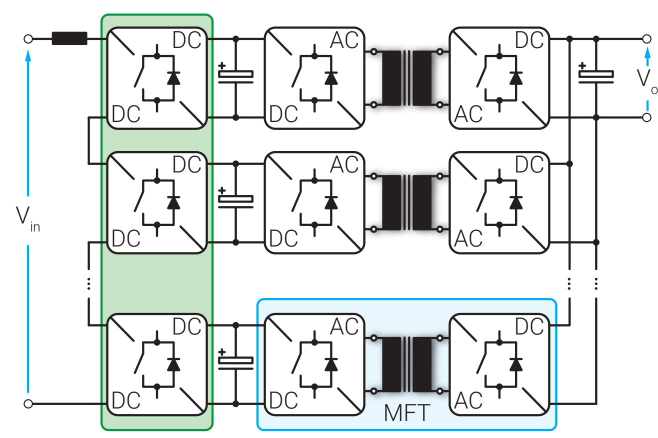
DC-DC SST - BASIC CONCEPTS

Fractional power processing

- Multiple MFTs
- Equal power distribution among PEBBs
- MFT isolation?
- Various PEBB configurations



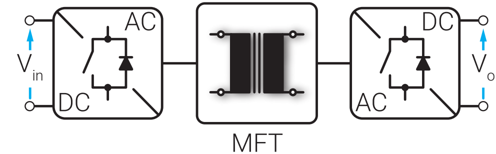
▲ Different structures employed depending upon the voltage level



▲ ISOP Structure

Bulk power processing

- Single MFT
- Isolation solved only once
- Various configurations/operating principles



▲ Bulk power processing concept

HITACHI ENERGY - 0.5MVA - DAB

Ratings

- Power: 0.55MVA
- Input DC voltage: 2.5kV
- Output DC voltage: 1.2kV
- Efficiency: 98.4% (at 360 kW, 2.5kHz) for Si IGBT
- Efficiency: 99.2% (at 360 kW, 4kHz) for SiC MOSFET
- Remark: calorimetric measurements

Topology

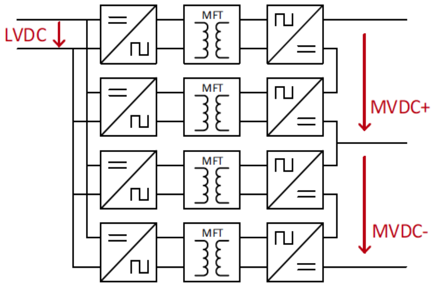
- Back to Back test setup
- DC-DC (Si DAB and SiC DAB cells)
- Input Series Output Parallel

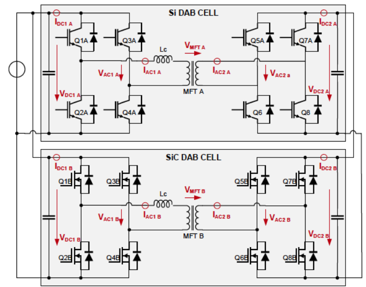
Semiconductor Devices

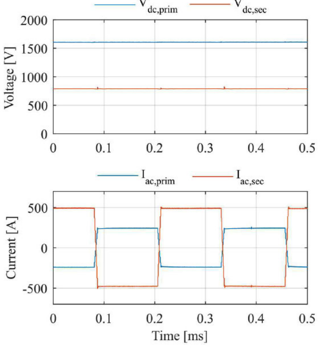
- HV side: 3.3kV Si IGBT / SiC MOSFET
- LV side: 1.7kV Si IGBTs / SiC MOSFET

MFT

- Power: 550kW per MFT
- Frequency: 2.5 - 8 kHz







▲ DAB Back-to-Back test setup [46]

MFT VARIETY OF DESIGNS...

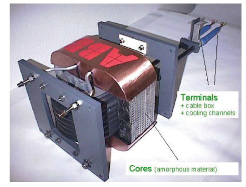


ABB: 350kW, 10kHz

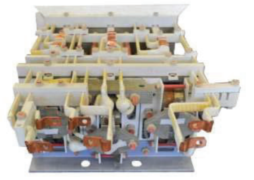
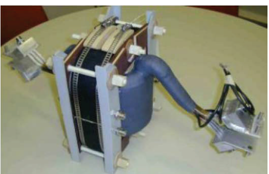
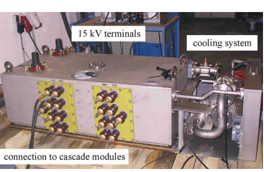


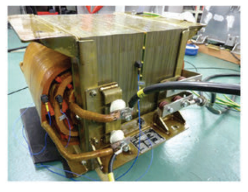
ABB: 3x150kW, 1.8kHz

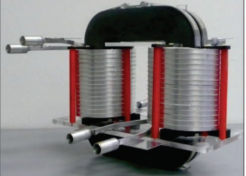

BOMBARDIER: 350kW, 8kHz



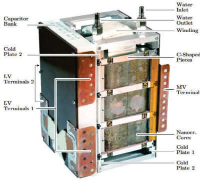
ALSTOM: 1500kW, 5kHz

IKERLAN: 400kW, 5kHz

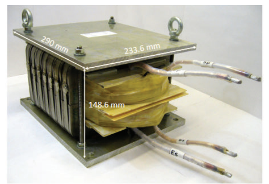

IKERLAN: 400kW, 1kHz


FAU-EN: 450kW, 5.6kHz

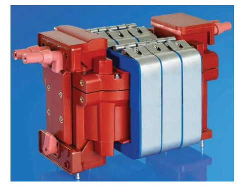
CHALMERS: 50kW, 5kHz

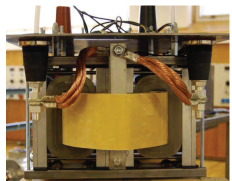


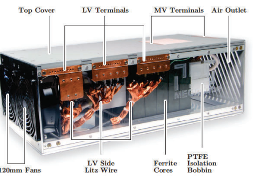
ETHZ: 166kW, 20kHz



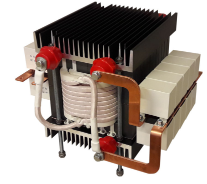
EPFL: 300kW, 2kHz

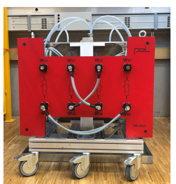

STS: 450kW, 8kHz


KTH: 170kW, 4kHz



ETHZ: 166kW, 20kHz


EPFL: 100kW, 10kHz


EPFL: 1000kW, 5kHz

HV INDUCTOR - TENNESSEE

Ratings

- Power: 100kVA
- Input DC voltage: 850V
- Output AC voltage: 13.8kV
- Efficiency: 97%

Topology

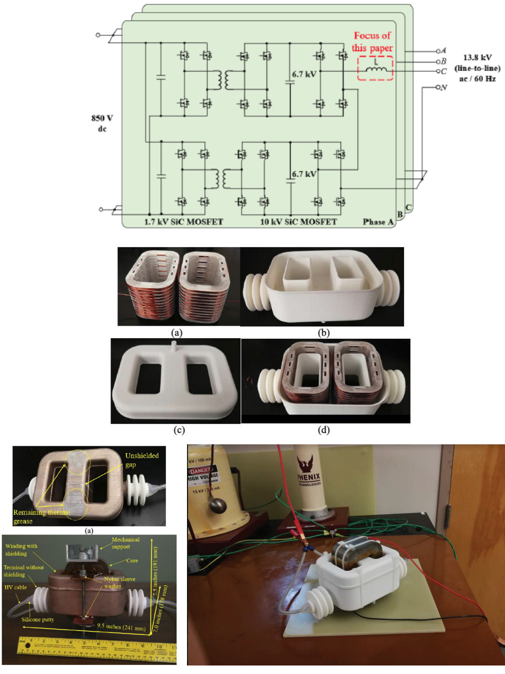
- DC-DC
- 5L CHB
- Three-phase VSI

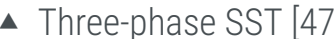
Semiconductor Devices

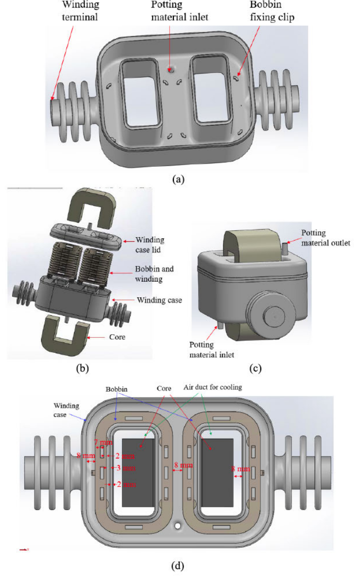
- HV side: 10kV SiC MOSFET
- LV side: 1.7kV SiC MOSFET

Inductor

- L = 44mH
- Ratings: 4.2Arms
- Effective switching frequency 40kHz
- Core: amorphous
- Insulation / Cooling: solid / air
- AC Withstand: 31kV (60 second)
- BIL: 95kV



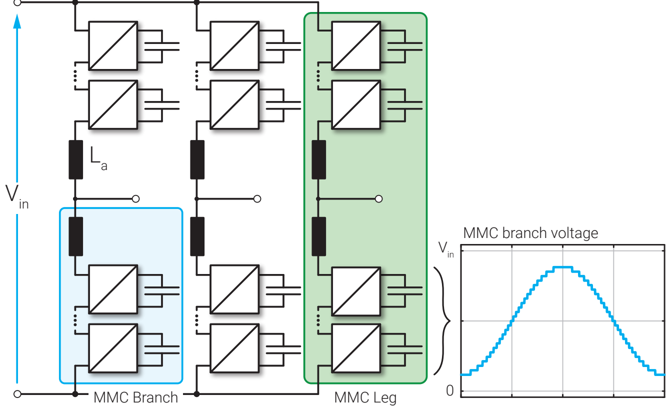




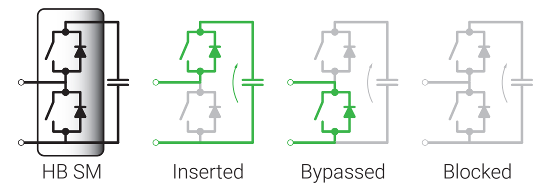
▲ Three-phase SST [47]

MODULAR MULTILEVEL CONVERTER (MMC)

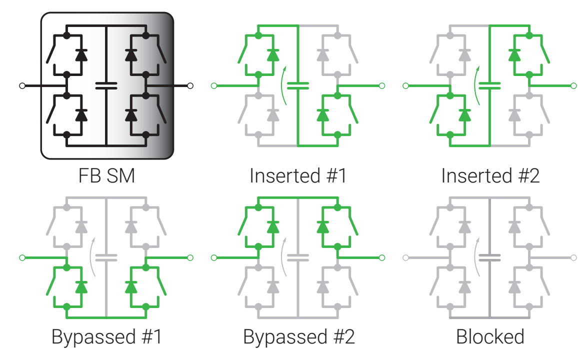
- Variety of conversion possibilities
- Variety of modulations
- Different types of submodules (SMs)
  - Half-Bridge (HB)
  - Full-Bridge (FB)
  - Others...
- Arbitrary voltage waveform generation



▲ Modular Multilevel Converter (MMC)



▲ Half-Bridge submodule and its allowed states



▲ Full-Bridge submodule and its allowed states

SIC IN AUTOMOTIVE - TESLA MODEL 3

Ratings

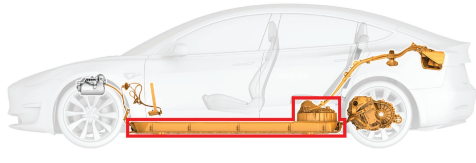
- Battery voltage: 300 - 400V
- Inverter ratings: 165kW (peak)

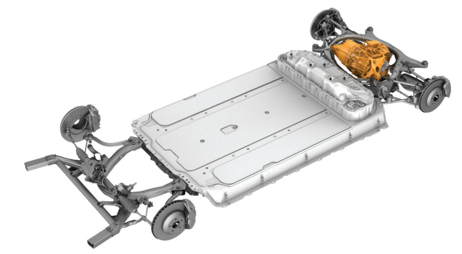
Topology

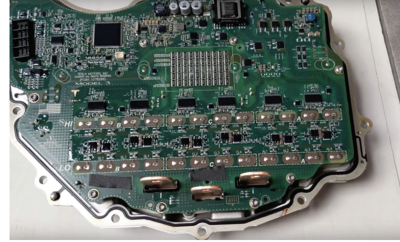
- Three-phase VSI

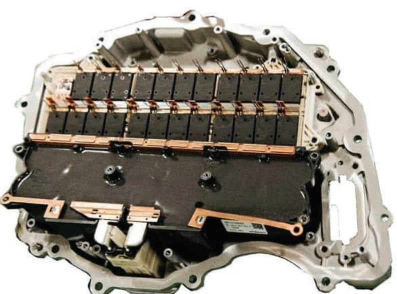
Semiconductor Devices

- 24 x 650V, 100A SiC MOSFET
- ST Microelectronics
- 4 parallel devices per switch









▲ TESLA model 3 uses SiC MOSFETSs

SIC MOSFET INTEGRATION

Parallel Connection of SiC MOSFETs

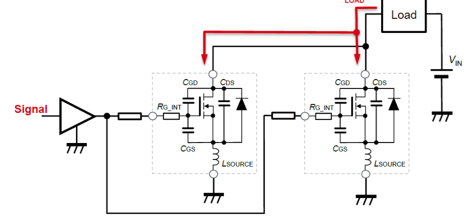
MOTIVATION OF PARALLEL CONNECTION

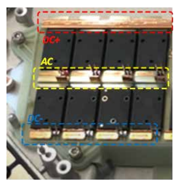
Current rating expansion

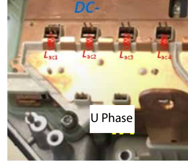
- Parallel connection of chips
- Parallel connection of modules

Challenges

- Current imbalance among paralleled devices/chips
- Possible osculations caused by parallel connection



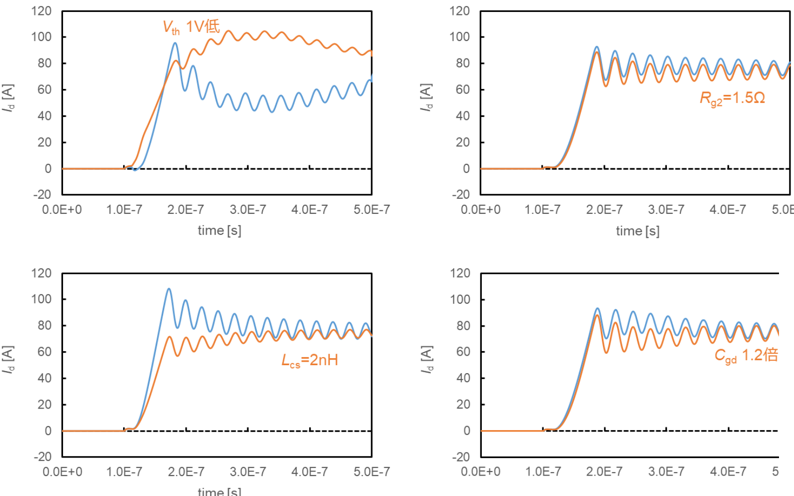




▲ *Source: Infineon, Rohm, Tesla.*

CURRENT IMBALANCE OF PARALLEL CONNECTION

- **Device parameters**
  Threshold voltage, bodydiode, trans-conductance, junction capacitance (C_{gd}), etc.
- **Uneven parasitics parameters**
  Common source inductor, different loop leakage inductors
- **Gate driving signal difference**
  Gate driver resistor, gate driver time delay
- **Different device temperatures**

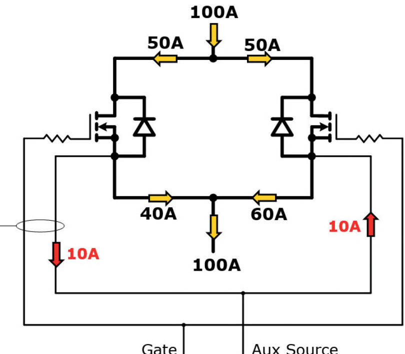


▲ *source: Rohm [48]*

CURRENT IMBALANCE OF PARALLEL CONNECTION

Static current sharing

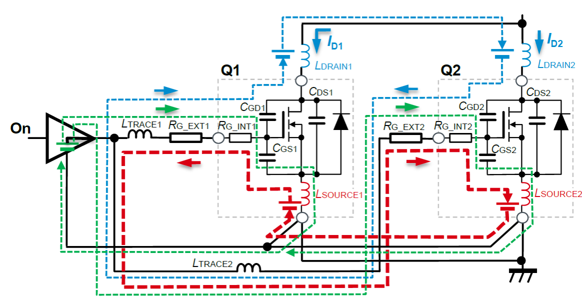
- Uneven device parameters in volume production
- Positive temperature coefficient of on-state resistance



▲ *source: Infineon [49]*

Dynamic current sharing

- v_{gs} **oscillation due to parallel connection of MOSFET**
- Uneven parasitic parameters



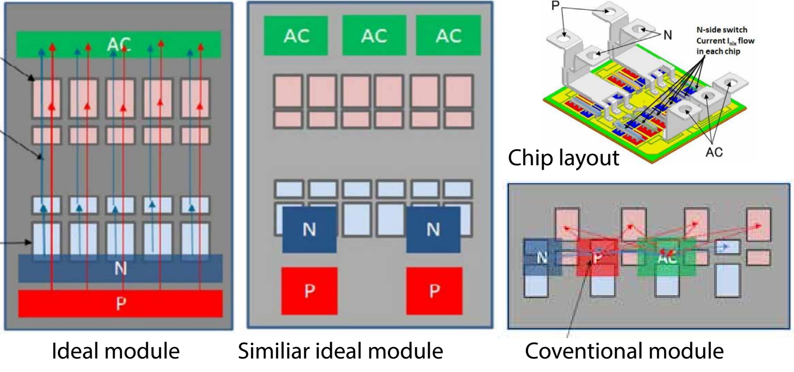
▲ *source: Rohm [48]*

Enough damping should be provided in the oscillation loop

CURRENT BALANCE OF PARALLEL CONNECTION

Balance from package perspective

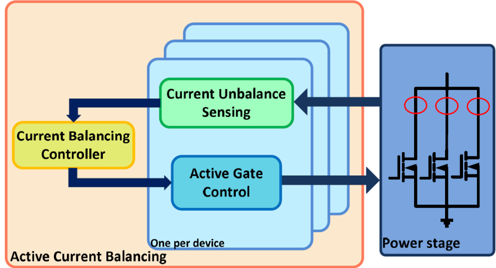
- Symmetrical in packaging, new package consideration (Open standard package etc.)
- Device selection criteria, parameters variation exists in massive production



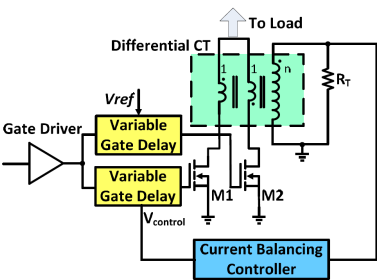
▲ *source: Mitsubishi [50]*

▲ *source: Hitachi Energy [51]*

Active current balance methods [52]



Control scheme



Implementation

PARALLEL CONNECTION - A PRACTICAL EXAMPLE

Oscillation caused by variation of bodydiode of SiC MOSFET

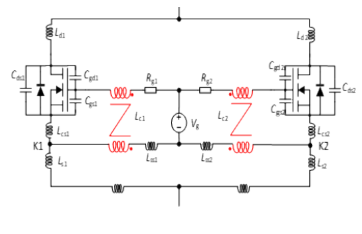
- There exists large variation on bodydiode of SiC MOSFETs
- Application with large individual AC inductance for the chip
- Oscillation happens when device is turned on
- No oscillation when device is turned off

source: Zinsight, https://mp.weixin.qq.com/s/dw_GXgqNq6fPyE7R_cb9ww

PARALLEL CONNECTION - A PRACTICAL EXAMPLE

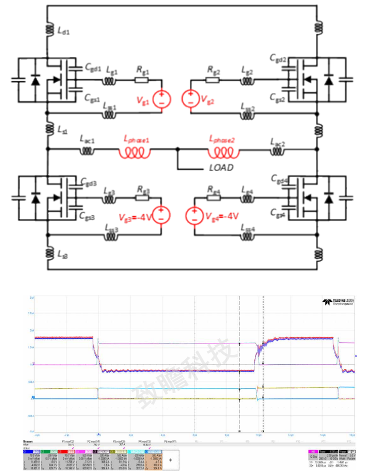
Coupled inductor

- Large oscillation on coupled inductor
- Largely eliminated but not completely removed



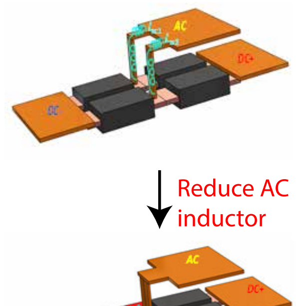
Separate gate driver

- Oscillation disappeared
- Separate gate driver required for parallel devices



Reducing AC inductance

- Improving layout of AC terminal
- Low cost design



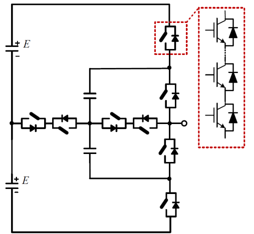
⇒ Hard paralleling of SiC MOSFETs is feasible. Careful device selection and design consideration are required

SIC MOSFET INTEGRATION

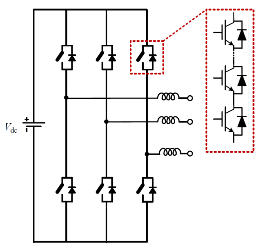
Series connection of SiC MOSFETs

Series connection of Si devices is a widely used technology

- MV drive
- HV power transmission



GE MV6000 MV drive



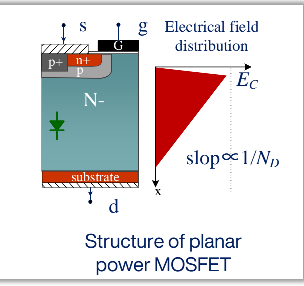
Hitachi HVDC Light

Chips

- High N- zone thickness
- low N- doping concentration
- high electric field

Application challenge

- High cost
- Low reliability
- Low efficiency



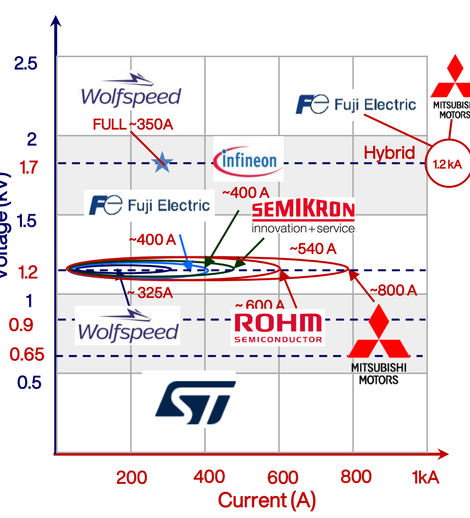
Structure of planar power MOSFET

Rated Voltage (kV)	Doping Concentration(cm^{-3})	Specific on resistance ($m\Omega \cdot cm^2$)	Breakdown voltage(kV)
1.2	8×10^{15}	2.7	1.6
1.7	6×10^{15}	3.4	1.9
6.5	1.3×10^{15}	40	7.2
10	6×10^{14}	125	11
15	3.6×10^{14}	250	16

▲ *source: Wolfspeed [53]*

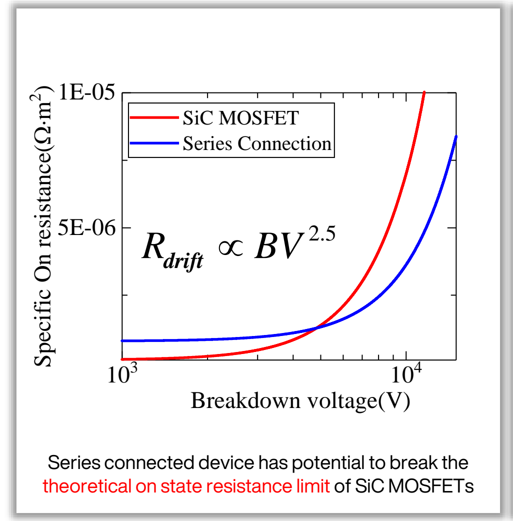
SERIES CONNECTION OF SIC MOSFETS

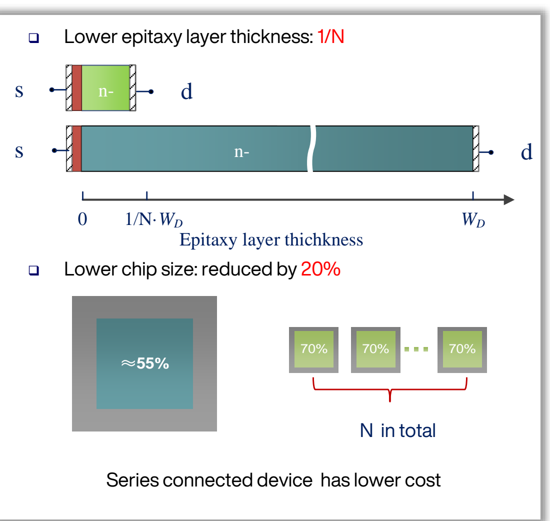
- Industrial products released at 1.2-1.7kV
- HV devices and modules are not commercially available



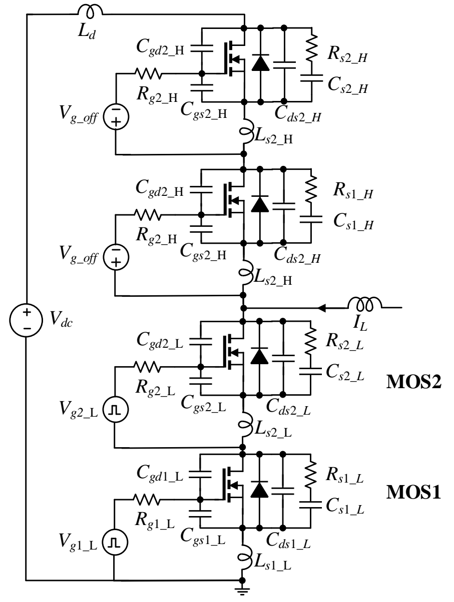
SERIES CONNECTION OF SIC MOSFETS

Comparison between single device and series-connected devices

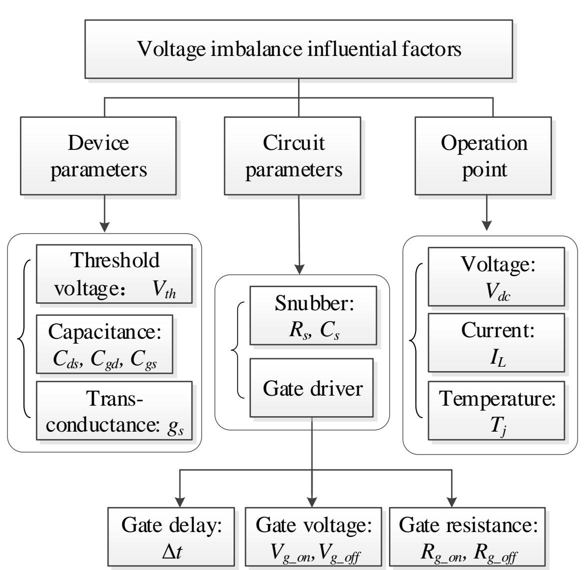




⇒ Series-connected SiC MOSFET has advantages in low on-resistance and cost



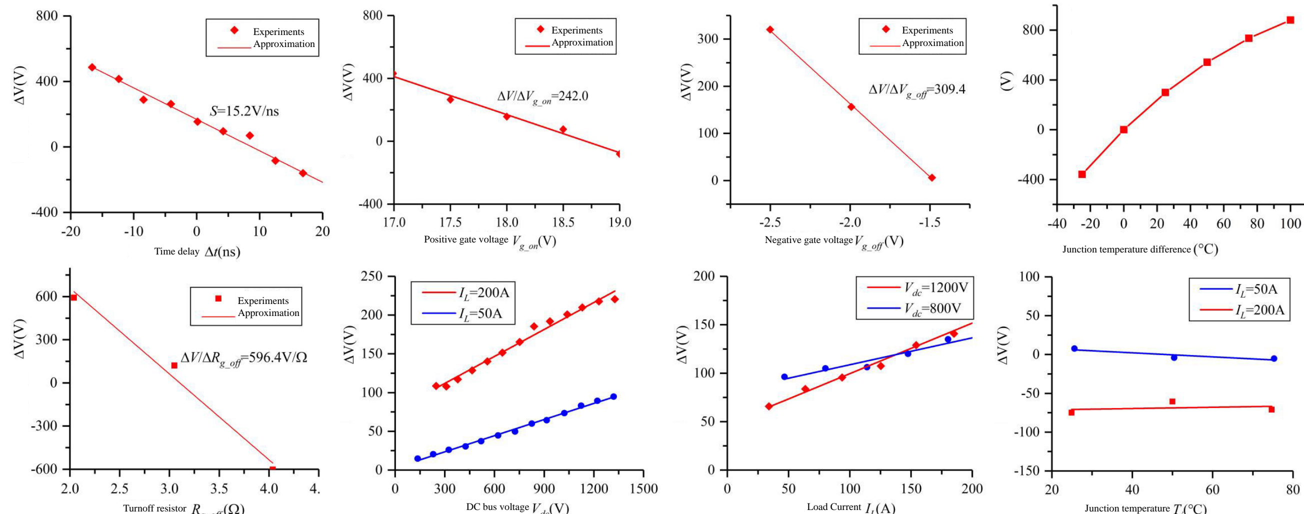
L_d
C_{gd2_H}
R_{s2_H}
C_{s2_H}
R_{g2_H}
V_{g_off}
C_{gs2_H}
C_{ds2_H}
L_{s2_H}
C_{gd2_H}
R_{s1_H}
C_{s1_H}
R_{g2_H}
V_{g_off}
C_{gs2_H}
C_{ds2_H}
L_{s2_H}
V_{dc}
I_L
C_{gd2_L}
R_{s2_L}
C_{s2_L}
MOS2
R_{g2_L}
V_{g2_L}
C_{gs2_L}
C_{ds2_L}
L_{s2_L}
C_{gd1_L}
R_{s1_L}
MOS1
C_{s1_L}
R_{g1_L}
V_{g1_L}
C_{gs1_L}
C_{ds1_L}
L_{s1_L}



Voltage imbalance influential factors
Device parameters
Circuit parameters
Operation point
Threshold voltage: V_{th}
Capacitance: C_{ds}, C_{gd}, C_{gs}
Trans-conductance: g_s
Snubber: R_s, C_s
Gate driver
Voltage: V_{dc}
Current: I_L
Temperature: T_j
Gate delay: Δt
Gate voltage: V_{g_on}, V_{g_off}
Gate resistance: R_{g_on}, R_{g_off}

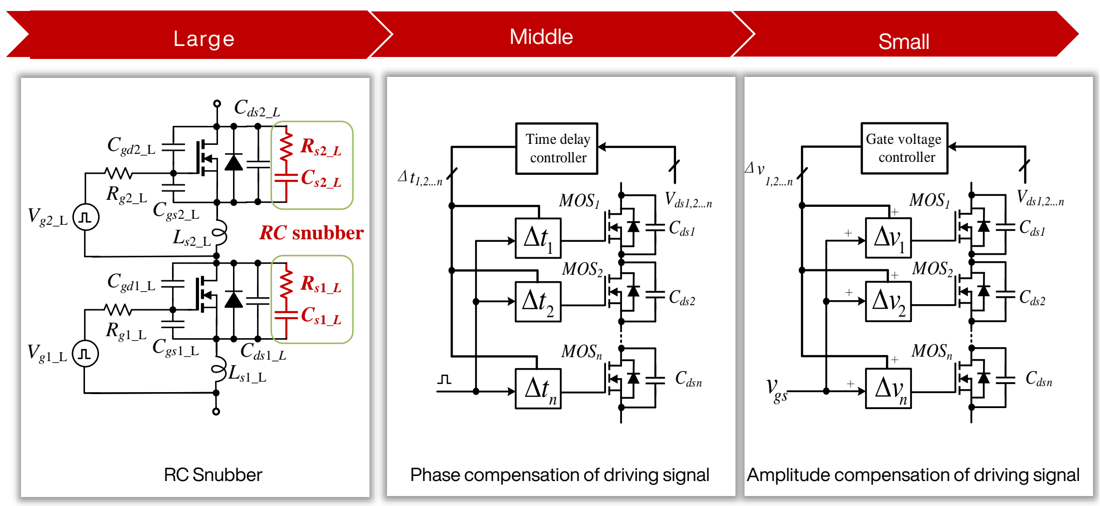
VOLTAGE IMBALANCE INFLUENTIAL FACTORS

- Gate driving time delay
- Gate source voltage mismatch
- Junction temperatures
- Gate driving resistance
- Voltages and currents

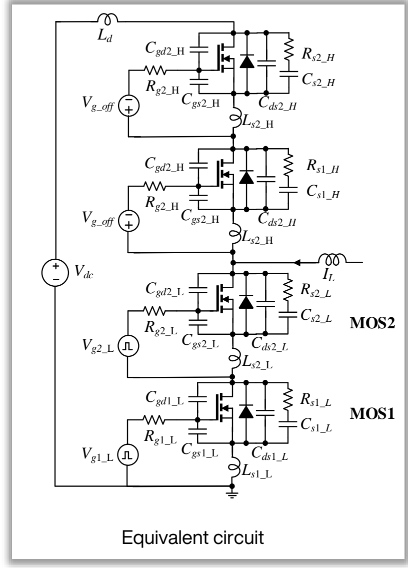


VOLTAGE BALANCE METHODS OVERVIEW

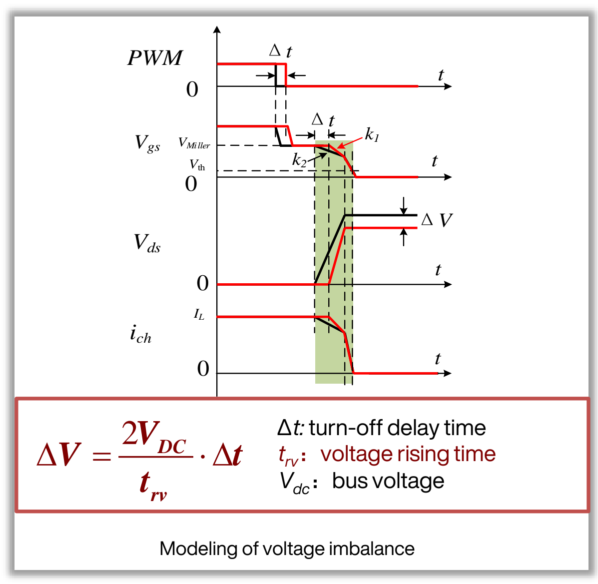
- Coarse tuning: passive snubbers
- Fine tuning: active gate driver time delay
- Accurate tuning: active gate driving voltage compensation



Analytic modeling of voltage imbalance [54]



Equivalent circuit



Modeling of voltage imbalance

⇒ The accurate model of the turn-off voltage rising time t_{rv} is of vital importance

PASSIVE SNUBBER DESIGN

Design steps [54]

- Voltage imbalance sensitivity (VIS) versus $C_{snubber}$ curve acquire by test or modeling
- Non-significant Miller plateau consideration
- Snubber capacitor is selected with lookup table from VIS-Csnubber curve

Voltage imbalance sensitivity: voltage imbalance caused by unit time delay

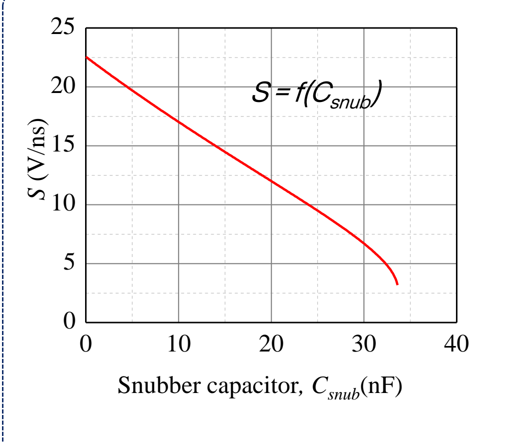
$$S = \frac{2V_{dc}}{t_{rv}}$$

✓ No significant Miller plateau

$$v_{gs}(t) = V_{miller} - kt$$

$$\begin{cases} t_{rv} = f\left(Q_{gd}, Q_{ds}, I_L, R_g, C_{gs}, k\right) \\ k = g\left(Q_{gd}, Q_{ds}, I_L, R_g, C_{gs}\right) \end{cases}$$

Analytical model of t_{rv}



Give targeted S, select snubber capacitor based on the S-$C_{snubber}$ curve

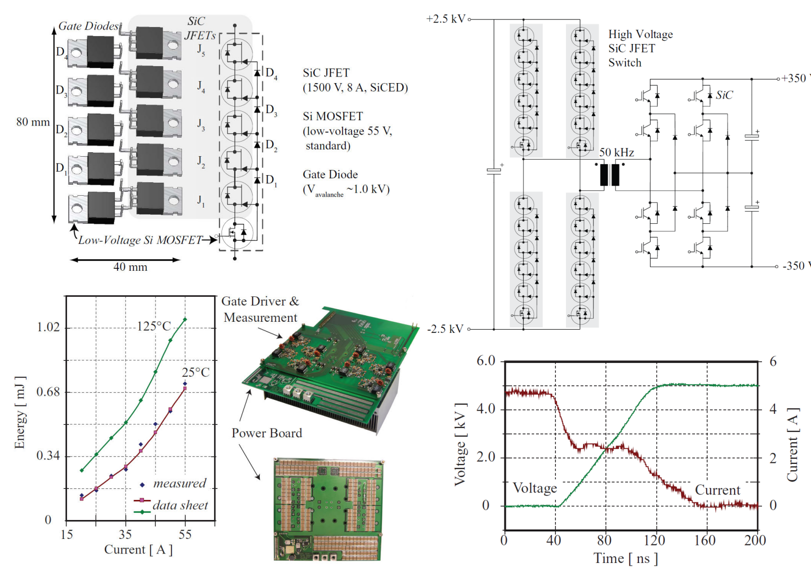
VOLTAGE BALANCE BASED ON PASSIVE SNUBBER

SiC JFETs Supercascode [55]

- SiC MOSFET + SiC JFETs
- One gate signal
- Passive snubber

Benefits

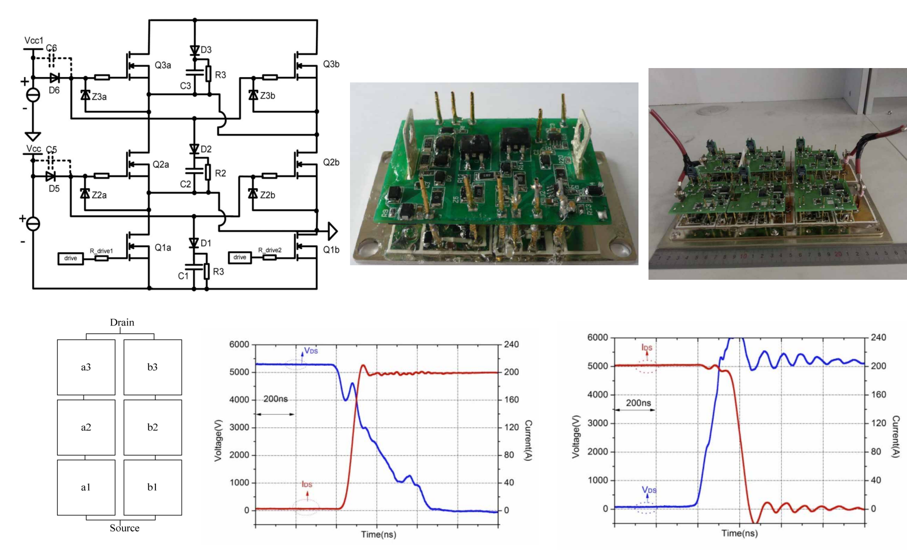
- Low cost
- Similar on-state resistance with HV device
- Low thermal conductivity



VOLTAGE BALANCE BASED ON PASSIVE SNUBBER

Characteristics [56] [57]

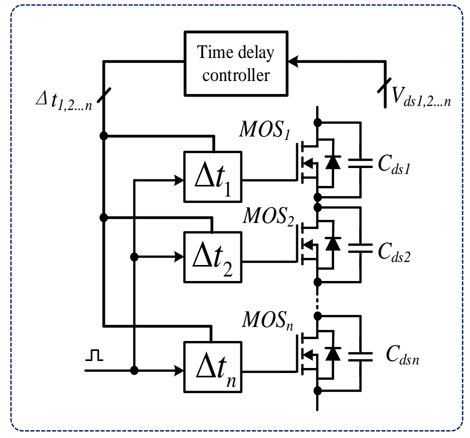
- SiC MOSFET + RCD snubber
- One gate signal
- 3.3kV/200A, three in series to 10kV/200A
- Integration to get three-terminal device

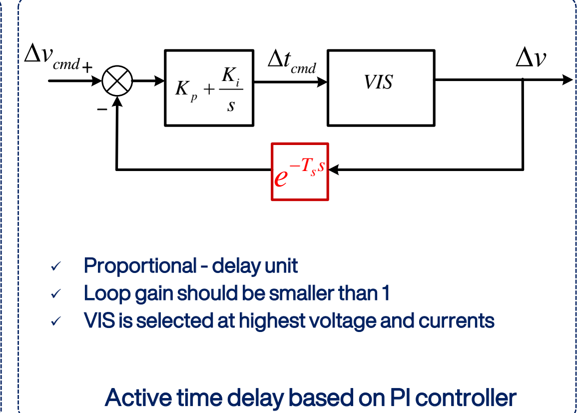


ACTIVE GATE DRIVING TIME DELAY (1)

Design steps [54]

- Offset calibration to get the relationship between delay time and voltage imbalance
- Close loop adjustment based on analytic VIS model



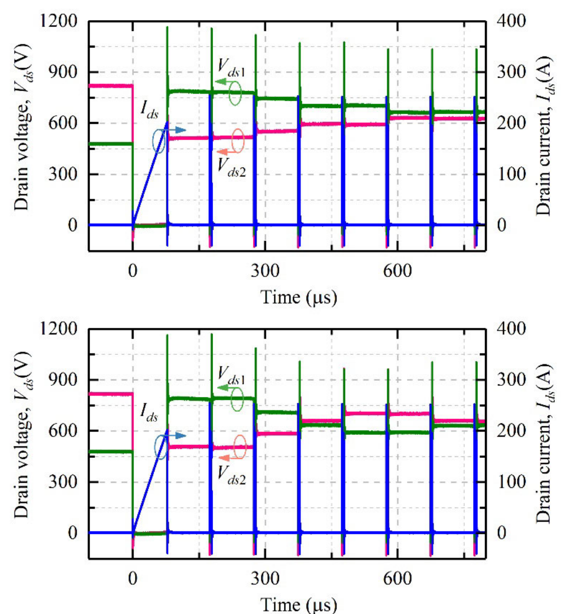


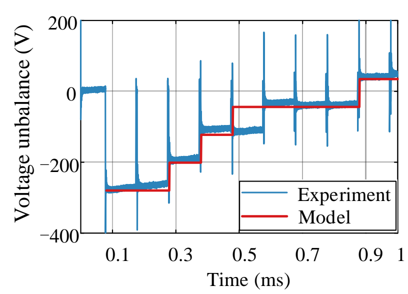
Active time delay based on PI controller

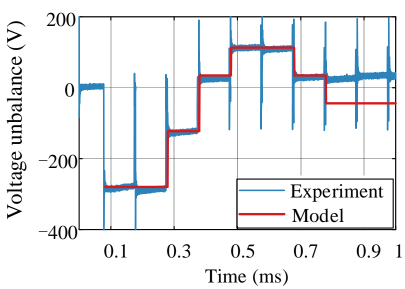
ACTIVE GATE DRIVING TIME DELAY (1)

Experimental verification [54]

- Device voltage is balanced after several switching cycles
- The measurement matches well with the model

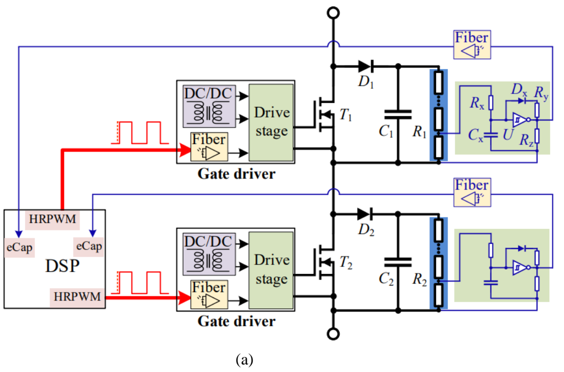




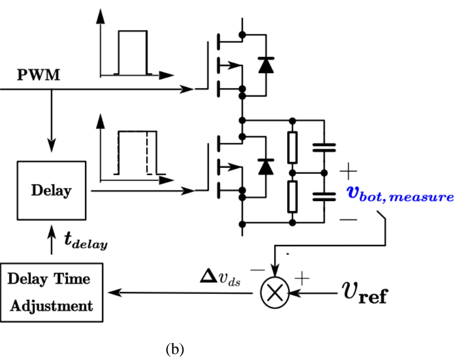


Other methods of active gate driving signal delay

- (a) RCD clamping resistor as feedback [58]
- (b) One device voltage is sampled for two in series [59]



(a)

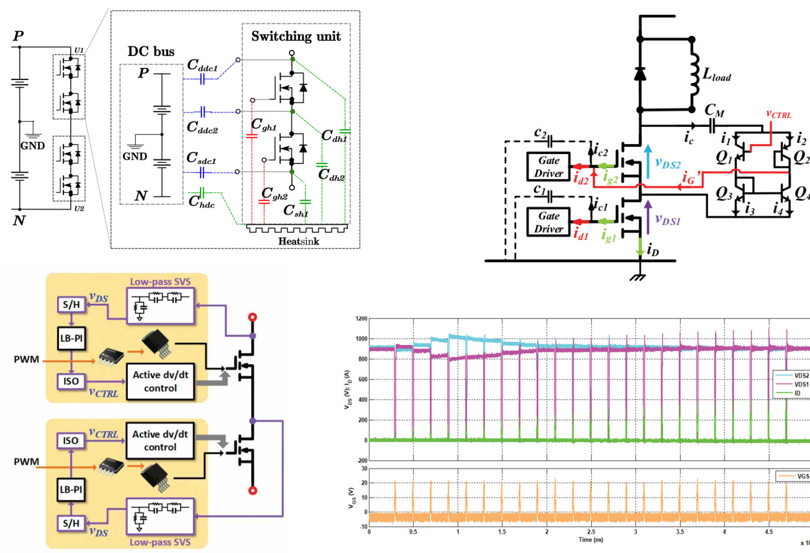


(b)

ACTIVE GATE SOURCE VOLTAGE COMPENSATION (1)

$\frac{dv}{dt}$ **slew rate control of SiC MOSFETs** [60]

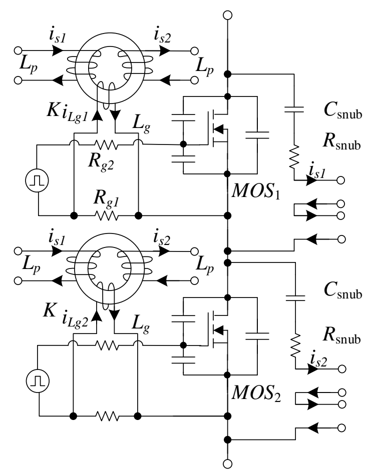
- Voltage imbalance is introduced by parasitic capacitance from the gate driver to the ground
- The imbalance is compensated by dv/dt controller

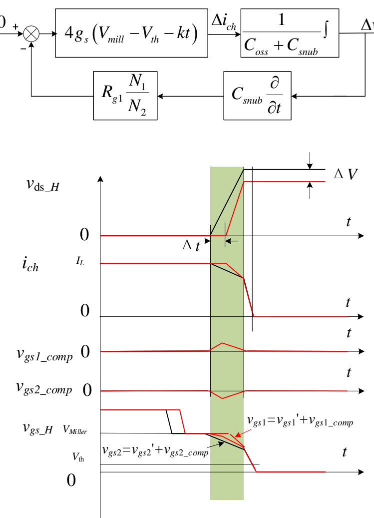


ACTIVE GATE SOURCE VOLTAGE COMPENSATION (2)

$\frac{dv}{dt}$ **slew rate control of SiC MOSFETs** [61]

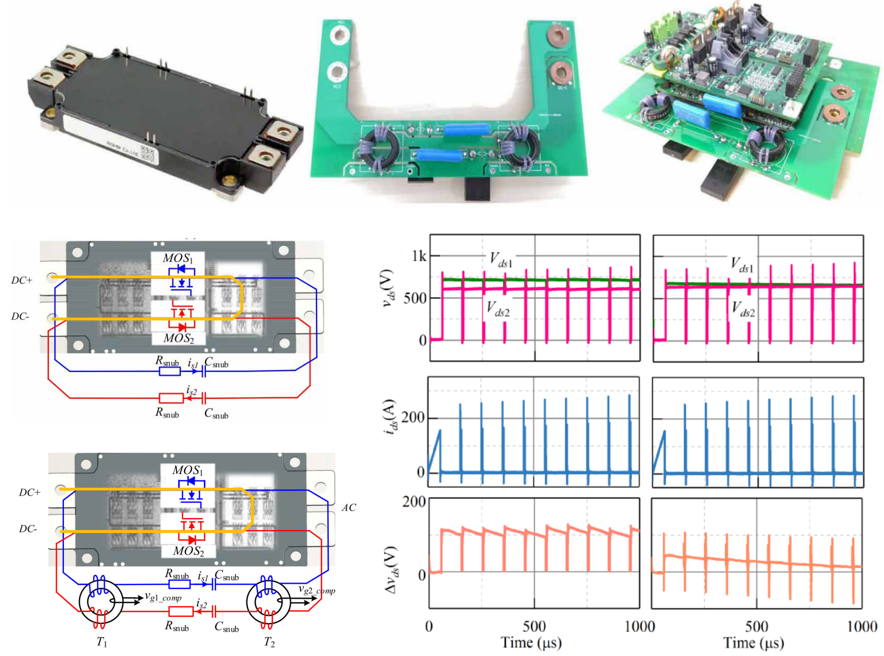
- Voltage imbalance is converted to snubber capacitor current deviation
- Isolation is realized by coupled inductor
- Gate source voltage is compensated





ACTIVE GATE SOURCE VOLTAGE COMPENSATION (2)

Experimental verification [61]



APPLICATION EXAMPLE OF SERIES CONNECTION (1)

Characteristics [62]

- 10kV/200A Power module
- Half bridge interface
- RC snubber
- 5kV/200A/20kHz switching
- 25kW/L power density

Series connection of eight 1.2kV@200A power modules

Picture of 10kV@200A power block, 25kW/L power density

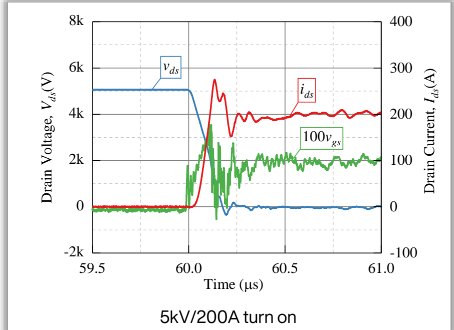
5kV/330kW/5kHz

Parameters	Value
Blocking voltage V_{ds}	10kV
Drain current I_{ds}	200A
On state resistance $R_{ds,on}$	97.7mΩ
Gate voltage $V_{g_on}/_{off}$	18V/-2V
Leakage inductance L_d	219nH
Snubber C_s/C_{snub}	5 Ω/4.7nF

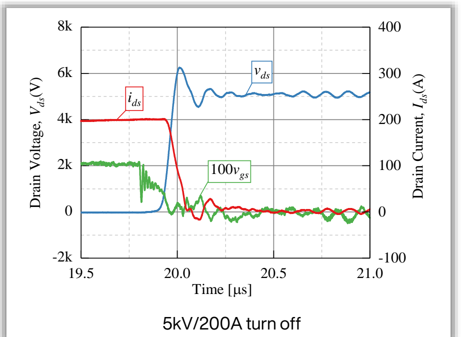
APPLICATION EXAMPLE OF SERIES CONNECTION (1)

Switching characteristics [62]

- Similar to single HV device
- 100V/ns voltage slew rate
- 2A/ns
- 100mJ total switching energy at 5kV/200A
- Stable switching loss with temperature



5kV/200A turn on



5kV/200A turn off

Device	Operation point	Turn on loss (mJ)	Turn off loss (mJ)	Freewheel diode (mJ)	Total loss (mJ)
Proposed block	**5kV/200A**	**31**	**56**	**13**	**100**
CREE 10kV/100A SiC	5kV/200A	161	50	-	210
Si IGBT, ABB 6.5kV/200A	5kV/200A	1328	1595	-	2923

⇒ The power block demonstrates the extremely low switching loss among counterparts

APPLICATION EXAMPLE OF SERIES CONNECTION (1)

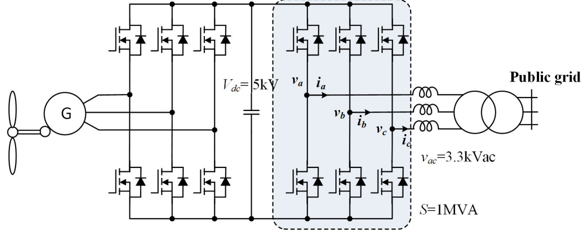
System efficiency analysis and comparison

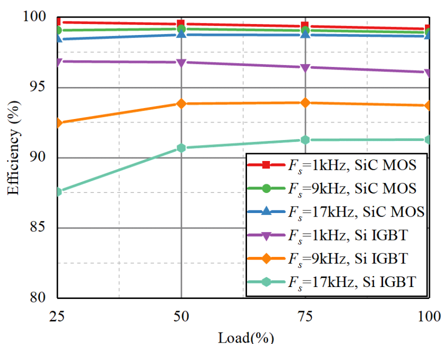
Parameters

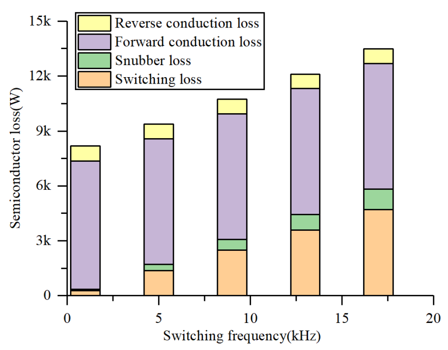
- Bus voltage: 5kV
- Power: 1MVA
- AC voltage: 3.3kV

Results

- Conversion efficiency at full load at 1kHz is 99.2%
- Conversion efficiency at 25% load at 1kHz is 99.6%
- Conduction loss dominates in the total loss - space to improve



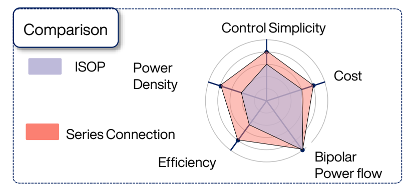




APPLICATION EXAMPLE OF SERIES CONNECTION (2)

Soft switching [63]

- Series connection
- Soft switching
- Centralized DC/DC conversion

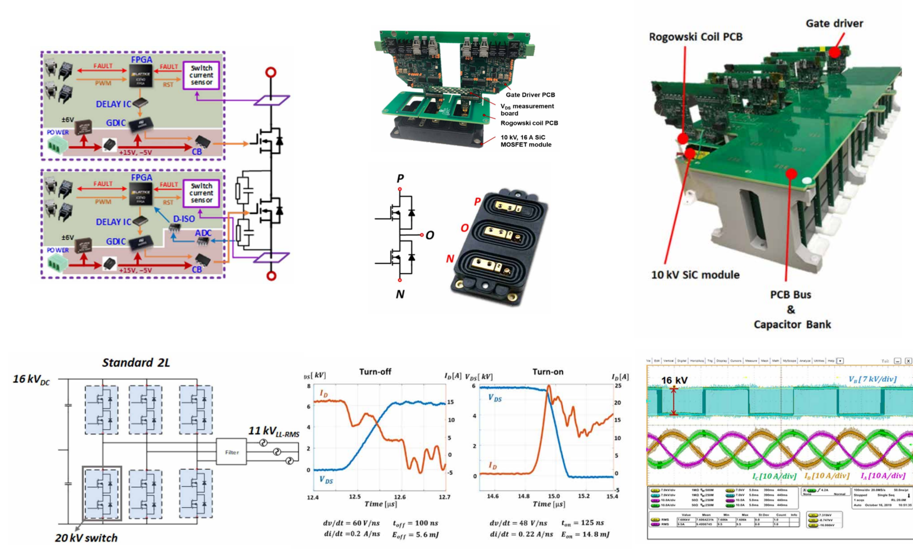


⇒ Soft-switching + series connection achieves voltage balancing and low loss switching

APPLICATION EXAMPLE OF SERIES CONNECTION (3)

System parameters [64]

- Two 10kV SiC MOSFETs in series
- 11kV AC grid voltage
- 16kV DC
- 200kW power
- 10kHz switching frequency

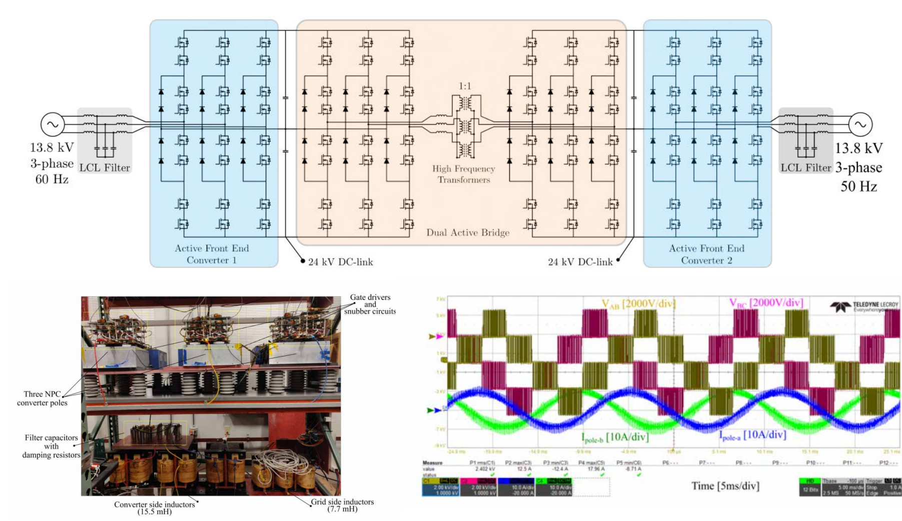


▲ *source: CPES*

APPLICATION EXAMPLE OF SERIES CONNECTION (4)

System parameters [65]

- Two 10kV SiC MOSFETs in series
- 13.8kV AC grid voltage
- 24kV DC
- 100kW power
- 10kHz switching frequency



▲ *source: FREEDM*

SIC MOSFET INTEGRATION

SiC-Si Hybrid solutions

SIC DEVICES + SI DEVICES HYBRID SOLUTIONS

Hybrid Multi-level converters with SiC & Si Devices

- SiC devices: High frequency switching and high cost
- Si Devices: Low frequency and low cost

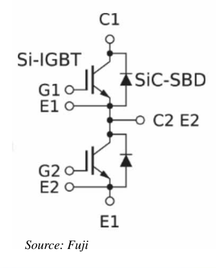
Power Device	Si IGBT Half-bridge		SiC MOSFET Half-bridge	
Type	FF300R12KT4		BSM300D12P2E001	
Voltage rating (V)	1200			
Current rating (A)	300			
Temperature	25℃	150℃	25℃	150℃
$E_{on}+E_{off}+E_{rr}$ (mJ) @I_C=300A, V_{ce}=600V	49	88.5	21.6	20.8
Retail Price ($)	111.64		643.43	

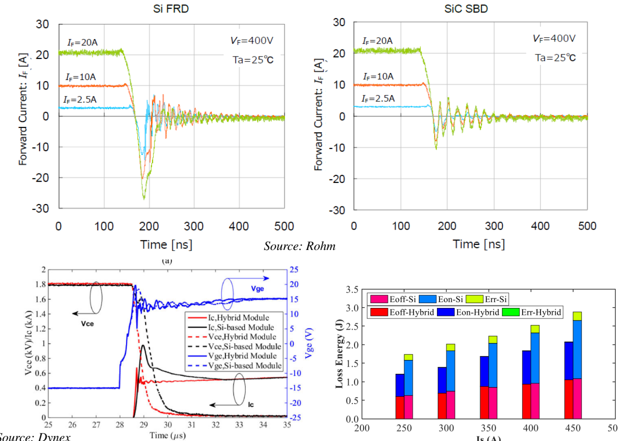
? Cost and performance trade-off: hybrid switch, hybrid converter, novel converters

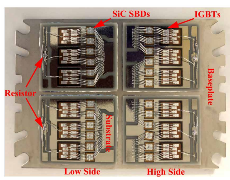
SI IGBT + SIC SBD

Improved switching performance of IGBTs [66] [19]

- Low reverse recovery loss
- Low turn-on loss
- Mature and commercially available



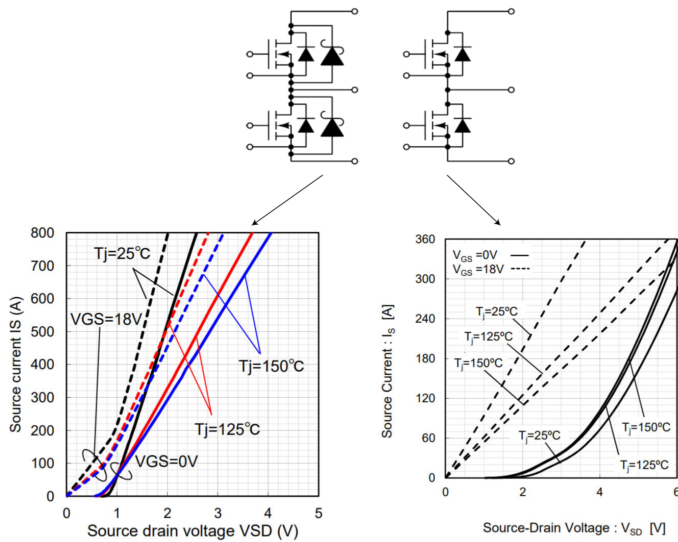




SIC MOSFET + SIC SBD

Performance [66]

- Avoid bipolar degradation of SiC MOSFETs
- Reduced cost for certain application

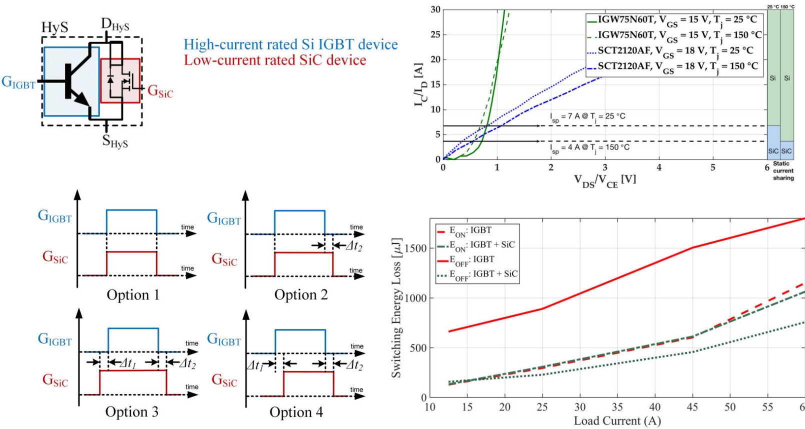


▲ *source: Rohm Datasheet*

SIC MOSFET + SI IGBT HYBRID SWITCH

Performance [67]

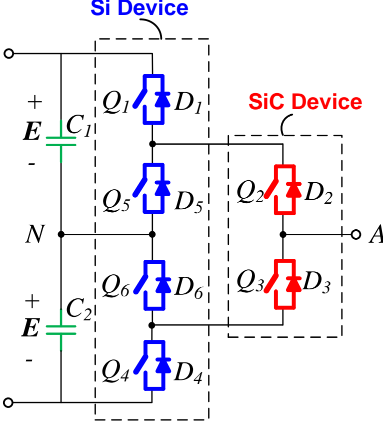
- No reverse recovery loss
- No tail current loss of Si IGBT
- Low cost
- High light load efficiency
- Increased driving complexity

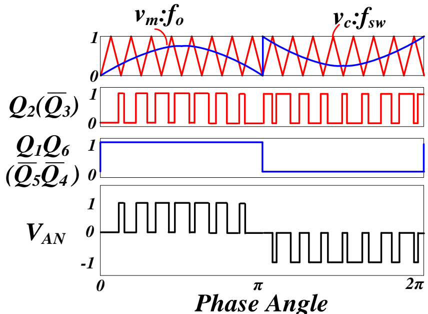


Hybrid Multi-level converters with SiC & Si Devices [68]

- Hybrid ANPC Converter and Modulation
- Only requires 1/3 of SiC devices
- Si devices are low-frequency switching

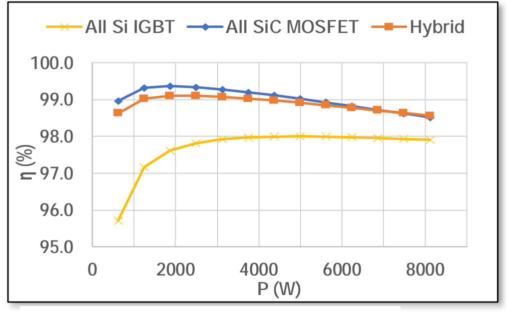
Output Voltage v_{AN}	Switching State					
	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6
E	0	0	1	1	1	0
0	0	1	0	1	1	0
	1	0	1	0	0	1
$-E$	1	1	0	0	0	1

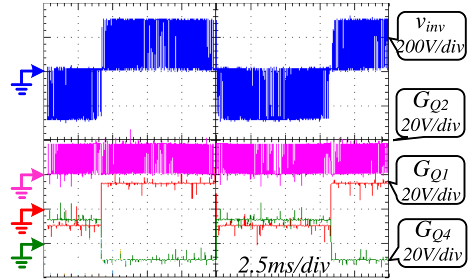


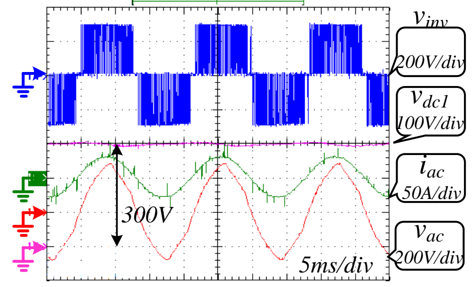


Experimental Results [68]

- Si IGBT Q1, Q4 are low-frequency switching
- SiC MOSFET Q2 is high-frequency switching
- Typical ANPC waveforms
- High efficiency is achieved



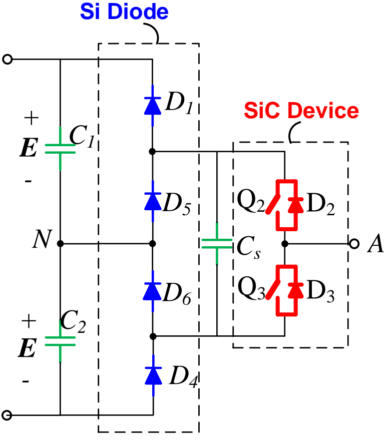


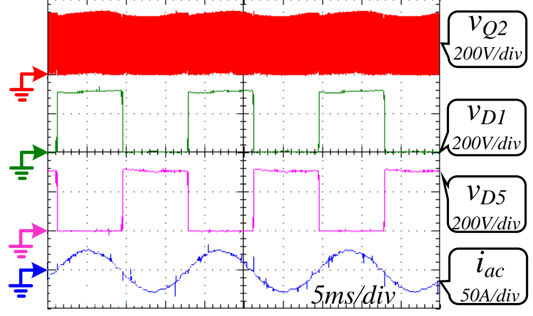


Simplified Hybrid NPC Converter: Unidirectional energy flow [69]

- Only requires Si diodes and SiC MOSFETs
- Si diodes are low-frequency switching
- Fewer high-frequency devices

Input Voltage or Input Current	Output Voltage v_{AN}	Q_2	Q_3
-	*-E*	0	1
	0	1	0
+	*0*	0	1
	+E	1	0

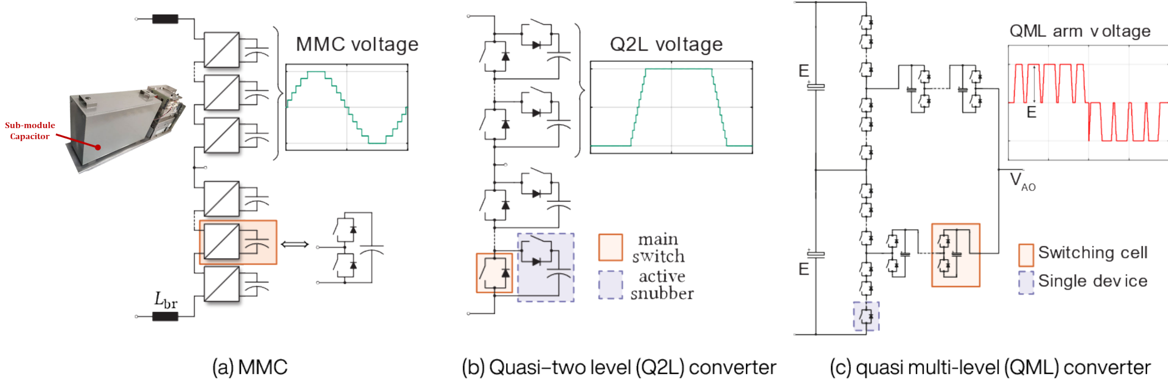




COMPACT CASCADING TECHNIQUE (1)

Concepts of quasi multilevel converter

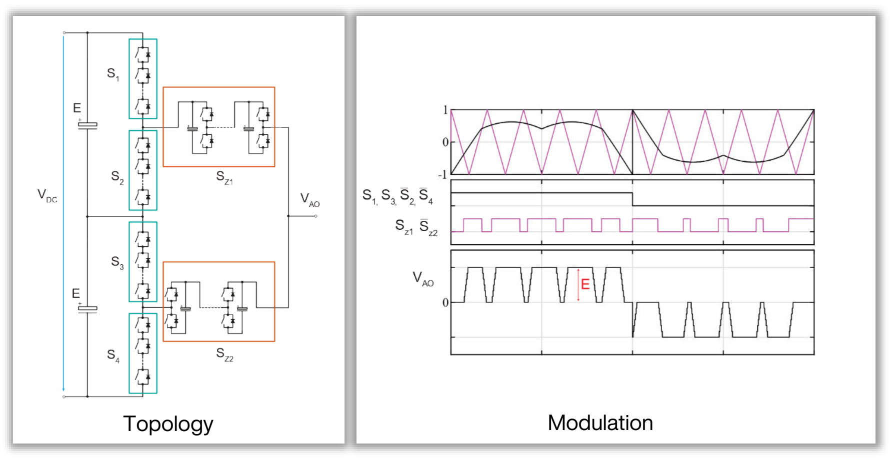
- Replacing the specific branch of conventional multilevel converter with a string of switching cells
- Multilevel output voltage waveform
- Transition between adjacent voltage levels is with trapezoidal shape



(a) MMC (b) Quasi–two level (Q2L) converter (c) quasi multi-level (QML) converter

Modulation and control

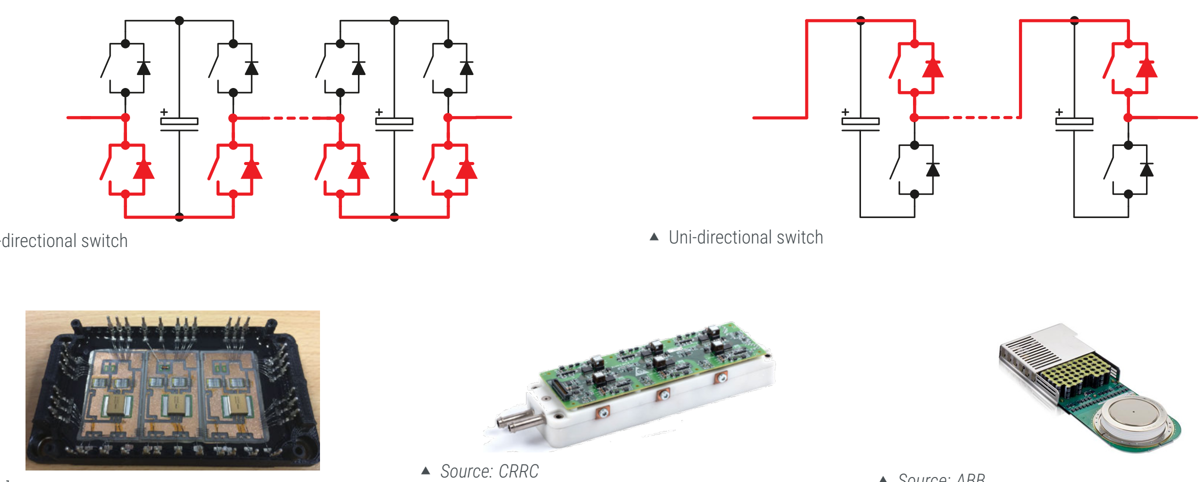
- Vertical arm: direct series connection of the power devices, line switching frequency
- Horizontal arm: cascaded half bridge submodules, high switching frequency



⇒ Size of submodule can be greatly reduced

Integrated SiC devices based switching cell

- Current commutation within sub cell – low switching loss
- Temporarily support output voltage – low cell capacitor



▲ Bi-directional switch

▲ Uni-directional switch

▲ *[70]*

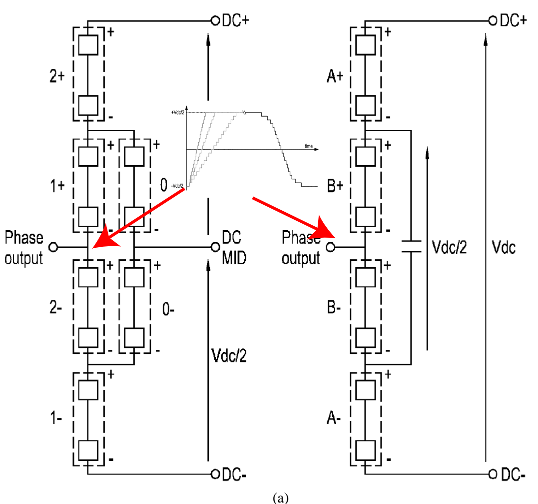
▲ *Source: CRRC*

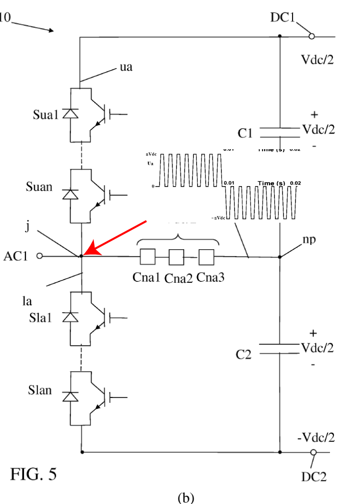
▲ *Source: ABB*

COMPACT CASCADING TECHNIQUE (2)

Novel topologies [66]

- Replace switch in multi-level converter with a string of SiC cells
- Reduced dc link capacitance
- Partial device adopts Si devices





▲ *source: (a) ABB-WO2019238443; (b) US2017257022A1.*

COMPACT CASCADING TECHNIQUE (3)

Topology [71]

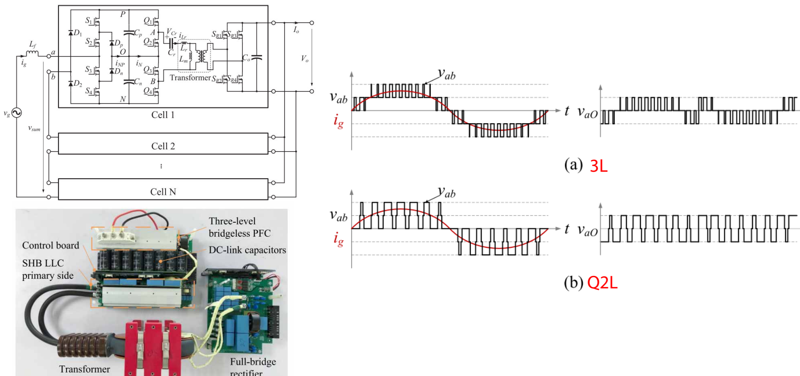
- Cascaded 3L bridgeless PFC stage
- Series-half-bridge (SHB) LLC dc–dc stage

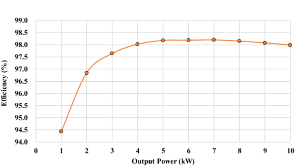
Control

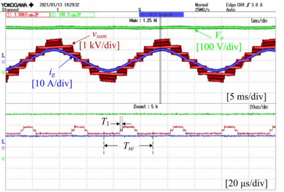
- Quasi-two-level modulation for PFC
- Phase-shift-based 3L operation of SHB LLC

Experimental validation

- DC bus voltage ripple is reduced
- Over 98% efficiency



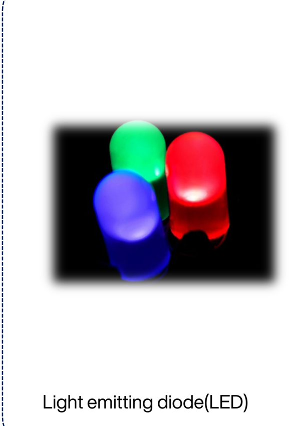




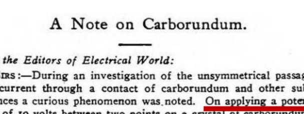
SUMMARY AND DISCUSSION

IS SIC DEVICES COMPLETELY NEW?

The first LED, probably first wide bandgap device, is a orange-green LED based on SiC diode, reported by H.J. Round in 1907



Light emitting diode(LED)



A Note on Carborundum.

To the Editors of Electrical World:

SIRS:—During an investigation of the unsymmetrical passage of current through a contact of carborundum and other substances a curious phenomenon was noted. On applying a potential of 10 volts between two points on a crystal of carborundum, the crystal gave out a yellowish light. Only one or two specimens could be found which gave a bright glow on such a low

...

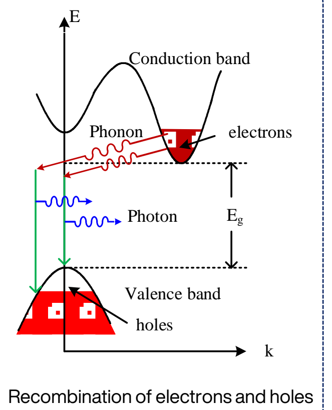
place, only one section of the crystal will glow and that the same section wherever the positive pole is placed.

There seems to be some connection between the above effect and the e.m.f. produced by a junction of carborundum and another conductor when heated by a direct or alternating current; but the connection may be only secondary as an obvious explanation of the e.m.f. effect is the thermoelectric one. The writer would be glad of references to any published account of an investigation of this or any allied phenomena.

NEW YORK, N. Y. H. J. ROUND.

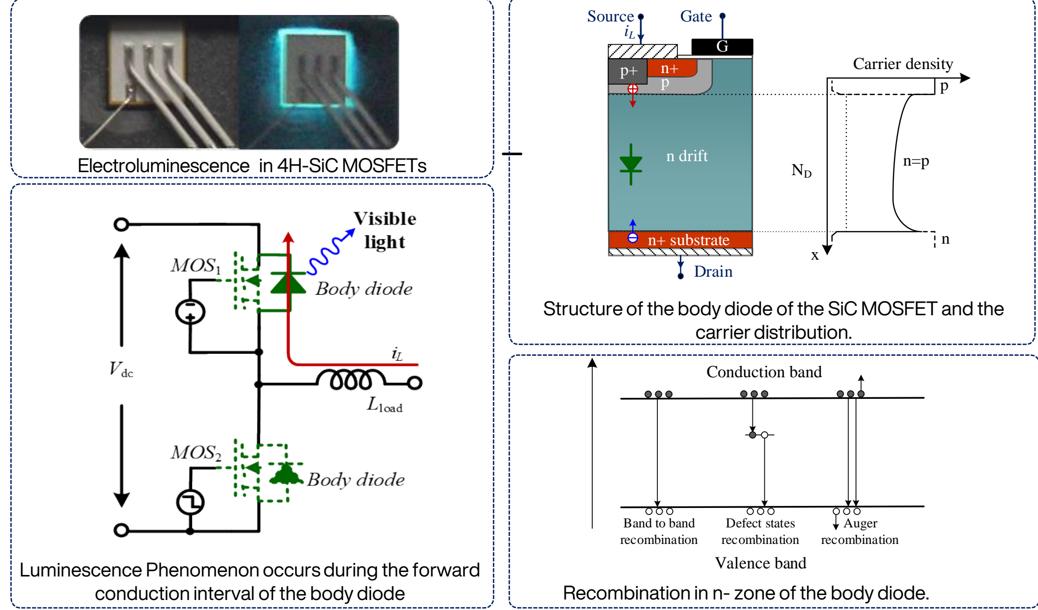
On applying a potential of 10 volts between two points on a crystal of carborundum, the crystal gave out a yellowish light.

H.J. Round, *Electrical World* 49, 309, 1907.



Recombination of electrons and holes

Electroluminescence of SiC Power MOSFETs [72]



Electroluminescence in 4H-SiC MOSFETs

Luminescence Phenomenon occurs during the forward conduction interval of the body diode

Structure of the body diode of the SiC MOSFET and the carrier distribution.

Recombination in n- zone of the body diode.

HOW TO BETTER UTILIZE THIS DEVICE?

Replace Si Devices

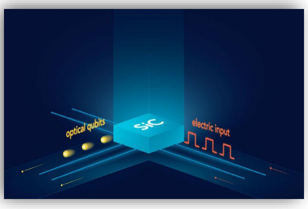
Renewable energy

Automotive

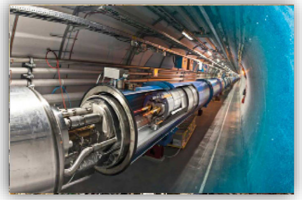
Data centers

New applications

Space



SiC Quantum Tech



Special power supply

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Thank you for your attention

…questions, discussion time…

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