MICRO-498: Microengineering project I

Piezoelectric thin films on Quartz substrate

Advanced NEMS Laboratory
Semester project report

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Contents

1 Introduction

The aim of this project is to deposit a thin film of aluminum nitride (AlN) or aluminum scandium nitride (AlScN) on a quartz substrate showing good piezoelectric properties for use in tuning fork oscillators. Quartz oscillators are commonly used in various applications such as clocks, watches, and electronic devices due to their high stability and reliability. By depositing AlN or AlScN films on a quartz substrate, we hope to enhance the performance and reliability of quartz oscillators and take advantage of the high coupling of AlN and the low temperature coefficient of frequency (TCF) of quartz. The Pfeiffer Spider 600 sputtering machine at the Center for Micronanotechnology (CMi) at EPFL will be used to optimize the deposition parameters for AlN or AlScN films on quartz substrate. After the depositions, the thin films will be characterized using techniques such as scanning electron microscopy (SEM) and X-ray diffraction (XRD).

This project is being conducted in collaboration with the company Microcrysal AG. The first part of the semester involved mainly reading literature, CMi training on the various machines, and constructing a holder for the chip to be carried in the clean room equipments. The second part involved conducting deposition tests on the Pfeiffer Spider 600, characterizing the deposited films, and designing a second holder.

2 Piezoelectric materials

2.1 Quartz

Quartz is a mineral composed of silicon and oxygen atoms in a continuous framework of SiO4 silicon-oxygen tetrahedra, with each oxygen being shared between two tetrahedra, giving an overall chemical formula of SiO2. It is the second most abundant mineral in Earth's continental crust, behind feldspar.

Piezoelectricity is the electric charge that accumulates in certain solid materials in response to applied mechanical stress. Quartz is piezoelectric, which means that when it is subjected to mechanical stress, it produces an electric charge and when an electric field is applied to it, it undergoes mechanical deformation. The piezoelectric effect in quartz is a result of the asymmetry of the silicon-oxygen tetrahedra in its crystal structure. When mechanical stress is applied to a quartz crystal, it causes the crystal structure to deform, which results in a change in the position of the electric dipoles formed by the asymmetry of the silicon-oxygen tetrahedra. This change in the position of the electric dipoles results in the generation of an electric charge on the surface of the crystal. Conversely, when an electric field is applied to a quartz crystal, it causes the electric dipoles to align with the field which results in a mechanical deformation of the crystal structure, causing the crystal to expand or contract. The piezoelectric effect in quartz is reversible, which means that it can be used to both generate and detect electric charges. This property of quartz has made it useful in a variety of applications, including oscillators for watches, microphones, and pressure sensors.

2.2 AlN and AlScN

Aluminum nitride (AlN) and aluminum scandium nitride (AlScN) are both inorganic compounds consisting of aluminum and nitrogen. AlN is a type of semiconductor material with a direct bandgap of 6.2 eV, making it suitable for use in high-temperature, high-power, and high-frequency applications. In particular, AlN has the highest thermal stability and piezoelectricity among the IIIA nitrides [1]. AlScN, on the other hand, is a ternary compound that includes scandium in addition to aluminum and nitrogen. It has a high Curie temperature, making it suitable for use in high-temperature environments, and a high piezoelectric coefficient.

By depositing AlN or AlScN films on quartz substrates, we hope to improve the performance and reliability of quartz oscillators and benefit from the high coupling of AlN and the low temperature coefficient of frequency (TCF) of quartz. The TCF descirbes the sensitivity of resonator's frequency to temperature changes. When the temperature changes, this can impact the physical characteristics of materials, such as their elasticity and their tendency to expand or contract due to heat. This, as a result, may change the resonance frequency of the oscillator. The electromechanical coupling coefficient, K_T^2 is related to the conversion rate between mechanical energy and electrical energy, which is defined as the ratio of the output mechanical energy and the input electrical energy [2].

The piezoelectric response of AlScN strongly depends on the growth temperature and scandium concentration. The grain size of AlScN increases with increasing growth temperature and scandium concentration, improving the crystallinity and crystal orientation. The crystal structure and orientation of AlScN can be investigated using X-ray diffraction (XRD). The XRD peak intensity of AlScN alloys increases with increasing scandium concentration, with a maximum value at a scandium concentration of 27%. These alloys have a wurtzite crystal structure and c-axis crystal orientation. The peak intensity decreases between scandium concentrations of 30% and 40%, but increases again between 40% and 45%. When the scandium concentration is 43%, the alloys exhibit a peak d_{33} of 24.6 pC/N, the highest reported to date for nitride semiconductors [3]. As mentioned in [4], Sc doped AlN film demonstrated a 400 % increase in piezoelectric modulus d_{33} for scandium aluminum nitride ($Sc_xAl_{1x}N$) alloys with x = 0.43. Also, the electro-mechanical coupling coefficient K_T^2 is improved from 7 to 10% by alloying AlN with up to 20 mol% ScN [3] [1].

2.3 c-axis, deposition optimisation

According to [5], orientation of c-axis (002) AlN thin film is desired for obtaining a high piezoelectric coefficient. The c-axis is the axis perpendicular to the plane of the crystal lattice. The c-axis is also the direction in which the crystal exhibits the highest symmetry. For these reasons, it is the direction in which the crystal exhibits piezoelectric properties.

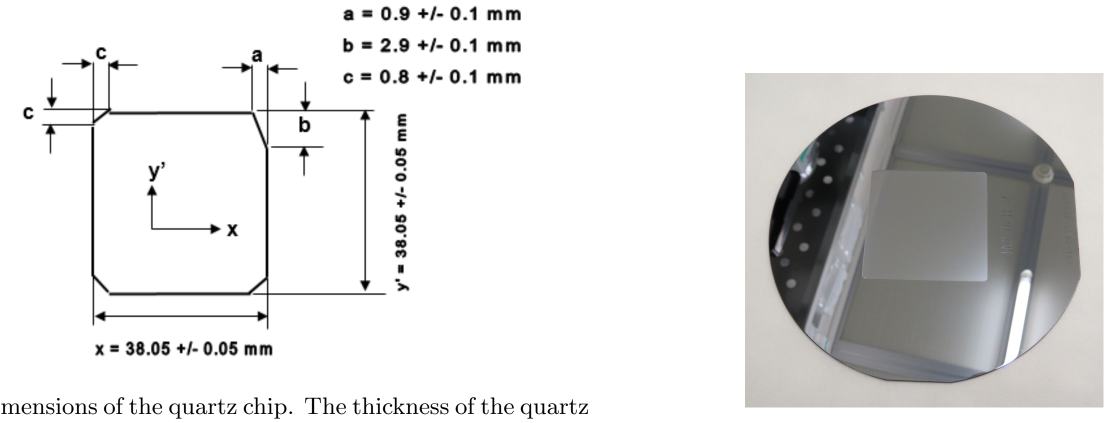
Among the different deposition method, reactive sputtering is a favourable deposition method for obtaining a specific orientation because of its simple process parameters control. In the article from Iriarte et Al. [6], several tests of AlN thin film deposition were made by varying the sputtering parameters, including the substrate, AlN layer thickness, substrate temperature, substrate bias voltage, gas flow ratio of Argon to Nitrogen, and process pressure. The authors concluded that among all the tested parameters, the process pressure and the discharge power are the most influential on the degree of c-axis orientation of the AlN thin films. By decreasing the sputtering pressure, the kinetic energy transfer from the plasma to the growing film surface is increased as the mean free path of a gas molecule at constant temperature is inversely proportional to the pressure, which can enhance the degree of c-axis orientation. On the other hand, they observed that AlN thin films deposited at low discharge power (below 300 W in their study) did not exhibit crystalline orientation, possibly because the atoms did not have enough energy to form the desired structure. According to [4] the ratio of Ar/N_2 is of great importance to obtain quality AlScN thin films. Moreover, according to [7], Pt, Ti or Au are reported to be more suitable bottom layers for textured c-axis AlN growth because of their smooth surface and low lattice mismatch.

As the Pfeiffer Spider 600 was used in this work for the depositions, direct control of pressure in the chamber was not possible. For this reason, most of the tests were done by varying the Ar/N_2 ratio.

3 Holder fabrication and depositions

3.1 Holder fabrication

The first part of the process flow (see section 6.1) consisted in the fabrication of a cavity in a wafer. This wafer will then be used to carry the quartz chip in the Pfeiffer Spider 600, as no chip can directly be inserted inside the chamber. To do so, a dummy wafer was covered with AZ ECI 3027 photoresist (PR) to be used as a mask during the dry etching step with the SPTS Rapier DSE. As in this machine the PR etch rate is 6nm/loop, the one of Si 800nm/loop, and the quartz thickness is 127 μm, we need approximately 159 loops ($127\mu m/800nm$) to create the cavity, which corresponds to 953nm of etched PR (159 loops $\cdot$ $6n$m). A thickness of 2μm of PR was chosen, taking into account that O_2 descum steps also remove some PR. The Heidelberg Instruments MLA150-2 was used to pattern the PR. Figure 1a shows the dimensions of the quartz chip and figure 1b shows a Si wafer with its cavity and the quartz chip inside. The masks used to pattern the PR are of the same dimensions as the quartz chip but with 0.1mm of tolerance. In practice, 200 loops with the SPTS Rapier DSE correspond to approximatively 127μm. This was measured optically with a microscope. At the end, two holder were fabricated, one normal (holder 1) and one with little bumps (holder 2) on each border to reduce the space between the chip and holder if any. However, in practice, only the holder 1 was used so not to constraint the chip too much during the depositions.



(a) Dimensions of the quartz chip. The thickness of the quartz is 127μm.

(b) Holder with a quart chip inside.

Figure 1

Once the cavity was created, the deposition tests could start and followed the layered structure shown on figure 2.

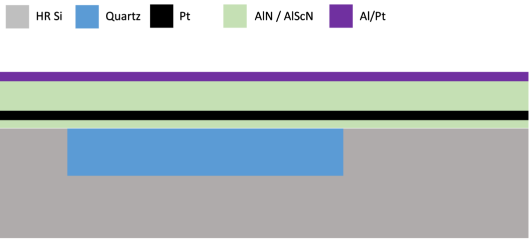
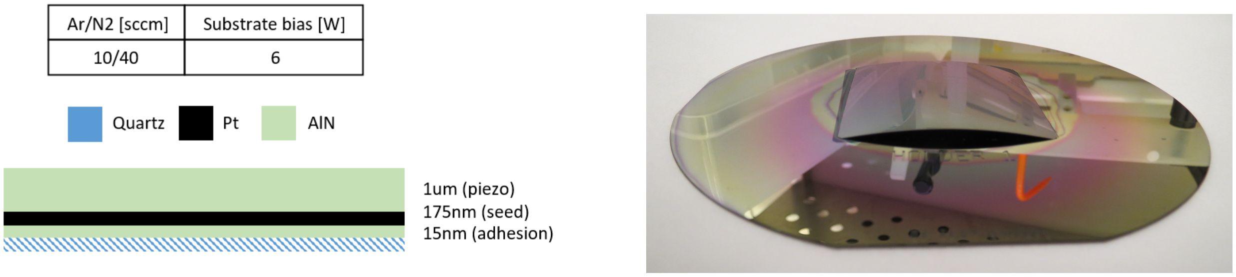


Figure 2: Layered structure of the wafer with the quartz chip in it (blue) after the deposition

AlN/AlScN is first used as an adhesion layer for the platinum. In our case, titanium cannot be used for the adhesion because it would be removed later on in the process by the use of HF. This step is not included in the process flow because it is not part of the project. On top of the adhesion layer, a Pt metal layer is used as seed layer for the AlN/AlScN piezoelectric layer so to influence the c-axis orientation of this layer [7]. Finally, another Al or Pt layer is used on top of the piezoelectric layer as an electrode. The high conductivity of this layer is also advantageous for SEM imaging after the deposition.

3.2 First deposition on quartz

The first deposition performed on a quartz substrate was done by depositing the same materials, thicknesses and parameters as shown on figure 3a. These values were chosen as other research conducted by the laboratory previously demonstrated favourable results when used on other types of substrates. The Si wafer is not represented on this schematic as it is only used to carry the wafer in the Spider for the deposition.



Ar/N2 [sccm]	Substrate bias [W]
10/40	6

(a) First deposition on the quartz substrate. AlN is deposited as adhesion and piezoelectric layer and Pt as seed layer.

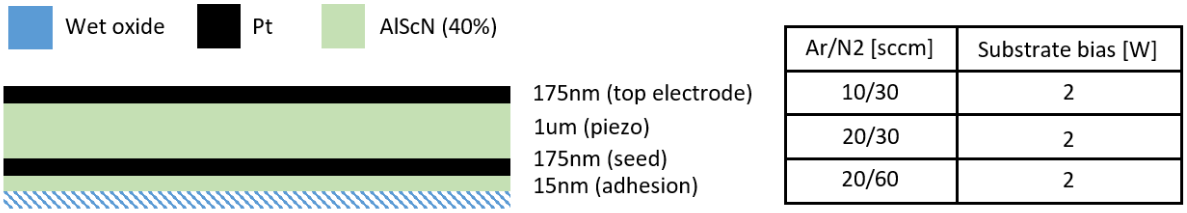
(b) Quartz substrate stressed after the deposition of AlN and Pt.

Figure 3

As it can be observed on figure 3b, the quartz was curved due to stress after the deposition of the piezoelectric layer made of AlN. No top Pt electrode was deposited as we could already see some cracks in the chip due to stress after the deposition of the second AlN layer. Due to this issue of having cracks in the chip, it was decided to do some deposition tests on dummy wafers with a 200nm wet oxide layer in an effort to reduce the stress. The oxide layer was chosen because it has the same chemical formula as quartz and as the number of quartz substrates available for the tests is limited.

3.3 Depositions on wet oxide for stress characterisation

According to [8], the pressure, the Ar/N_2 flow rates and the rf-induced substrate potential have a great influence on the stress and d_{33} coefficient of AlN layers. As the Pfeiffer Spider 600 does not allow a precise control of the pressure and as some previous work in the laboratory showed good results with a 2W substrate bias, only tests by varying the Ar/N_2 ratio were carried. Moreover, changing the gas ratio seems to be the more effective way to affect the stress in the deposited layers as the substrate bias was already very low (2W). Figure 4 shows the parameters of the three depositions done.



Ar/N2 [sccm]	Substrate bias [W]
10/30	2
20/30	2
20/60	2

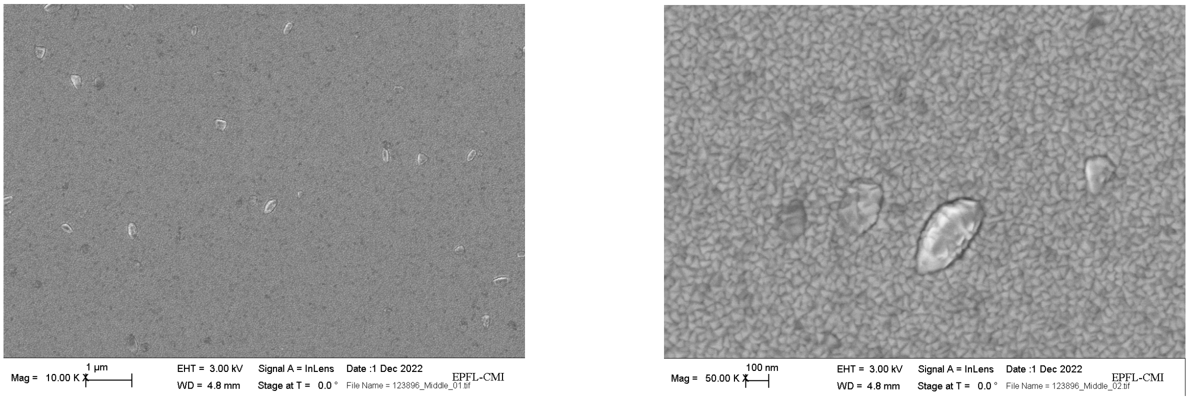
Figure 4: Materials deposited and parameters of deposition to characterize the effects of these parameters on the stress.

Results of the measured stress are shown in table 1. This was measured by using the Toho Technology FLX 2320-S tool and by entering a total thickness of 13'650Å. It can be observed that the stress decreases with the quantity of Ar in the gas mixture and with the overall pressure in the chamber with the same gas ratio (Ar/N_2=10/30 sccm versus Ar/N_2=20/60 sccm) passing from compressive stress to tensile stress. As the same thickness was entered for the calculation of the stress by the machine, the true values of stress might differ a little bit as the deposition rate for the different piezo layers is probably a bit different. The FilMetrics F54 tool was used to measure the thickness of the piezo layer that was deposited. However, the machine did not produce accurate results (poor fit). It is likely that the differences between the measurements and the true value are not significant, and we can still observe the effect of the gas ratio on the stress, which follows a similar trend as described in the reference [8]. Once the stress was measured, some SEM pictures of the surface were taken to observe the effect of the deposition parameters on the piezoelectric layer (see figures 5). The results are much better with a lower pressure (Ar/N_2=10/30 sccm) as

Wafer ID	Ar/N$_2$[$sccm$]	Stress 0° [MPa]	Stress 90° [MPa]
123896	10/30	-374.6	-379.1
110162	20/30	-262.9	-263.1
110164	20/60	132.8	135.0

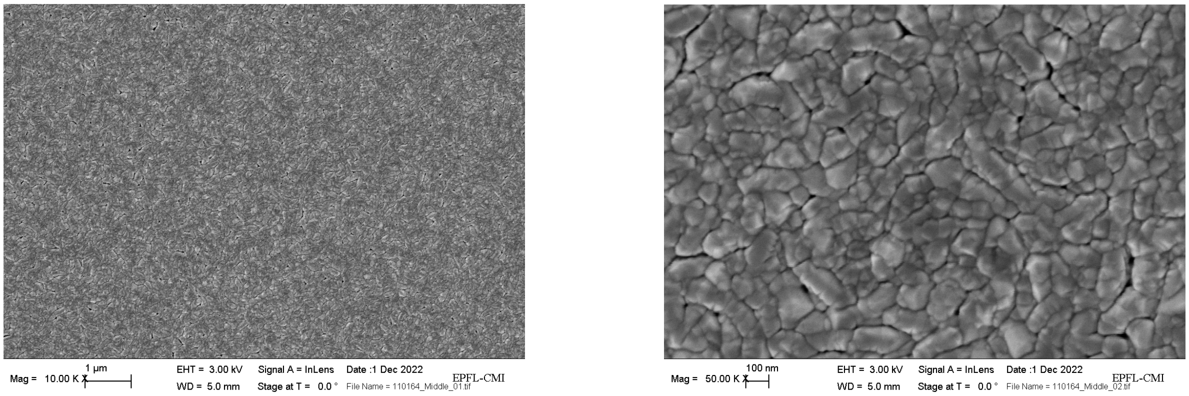
Table 1: Deposition parameters of the AlScN (40%) piezo layer on Pt done with the Pfeiffer SPIDER 600 at 300°C

there are much less abnormal grains on the surface (grains with a different orientation of growth). The abnormal grains are quite big and this can be explain by the presence of the thick layer of Pt on the surface. As wafer 123896 with an Ar/N_2 ratio seems to be the best candidate, some XRD measurements were performed on this wafer. Indeed, both SEM and XRD are required to characterise the piezoelectric layer. SEM gives information about the number of abnormal grains whereas XRD provides informations about the orientation of the crystal. A low number of abnormal grains in a necessary condition but not sufficient to guarantee good piezoelectric properties. The XRD measurements showed a peak at 36° for the AlScN [4] with a HWHM value of 1.3 shwowing a good cristallinity of the deposited layer (see figure 6).



(a) Middle of wafer 123896 with a magnitude of 10k. Only few abnormal grains are visible.

(b) Middle of wafer 123896 with a magnitude of 50k. Only few abnormal grains are visible.



(c) Middle of wafer 110164 with a magnitude of 10k. A lot of abnormal grains are visible.

(d) Middle of wafer 110164 with a magnitude of 50k. A lot of abnormal grains are visible.

Figure 5: SEM results of wafers with an oxyde bottom layer.

No XRD measurements were done on the two other wafers (110162 and 110164) due to the short amount of time at disposal before the next deposition with the Spider Pfeiffer 600 and the limited availability of the tool with the right targets.

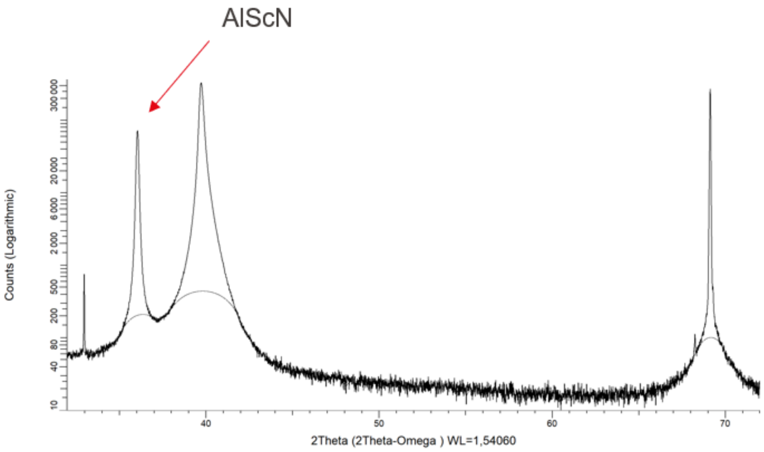


Figure 6: XRD measurements on wafer 123896.

3.4 Second deposition on quartz

As we obtained good results in term of number of abnormal grains, crystalline orientation and stress with the gas mixture of $Ar/N_2 = 10/30$ sccm, a new test was performed on quartz with the same parameters. Figures 7a and 7b show the difference between the quartz chips after the first and second deposition. After the second deposition and with the new deposition parameters (on the right), the chip is slightly less curved but also has a Pt layer on top that is not present on the other chip. However, in this case, no cracks are visible on the surface of the chip.

(a) Quartz chip after the first deposition (left) and after the second deposition (right.)

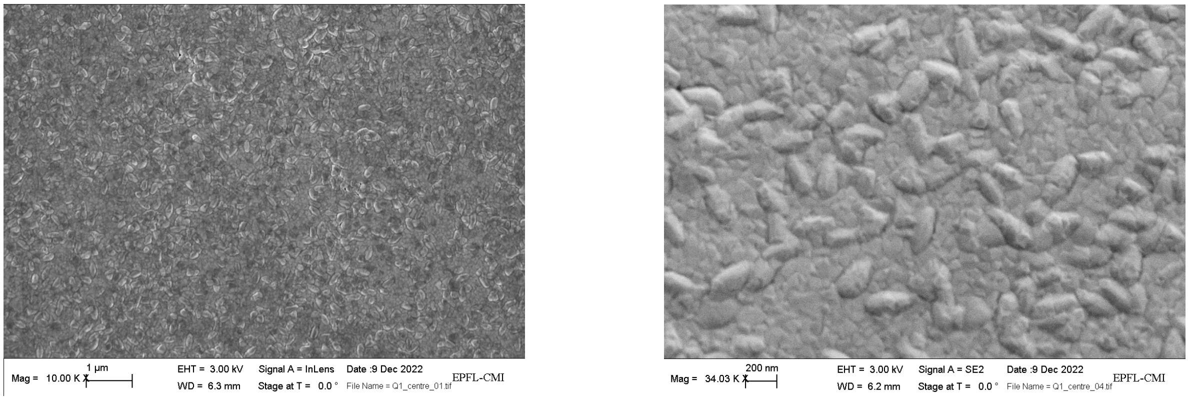
(b) Quartz chip after the first deposition (left) and after the second deposition (right).

Figure 7

Figure 8 shows a SEM image of the surface. Contrary to what was obtained with the tests on oxide (figures 5a and 5b), the obtained results are not good as a lot more abnormal grains are visible on the surface. The first hypothesis proposed to explain these results is that the stress causing the quartz to bend during the deposition process may lead to fewer contact points with the carrier wafer, reducing the opportunities for the charge of the plasma to evacuate. This could result in an accumulation of charges that may impact the orientation of the deposited layer. The CMi staff proposed a second hypothesis which suggests that the issue may be related to thermal problems. As previously mentioned, the stress on the quartz leads to fewer points of contact with the carrier wafer, which may cause the chip's temperature to drop below 300°C. This decrease in temperature may result in a decline in the quality of the deposited film. In both case, it seems beneficial to try to maintain the quartz substrate flat during the depositions. A second holder was hence designed for that purpose.

3.5 Holder modification

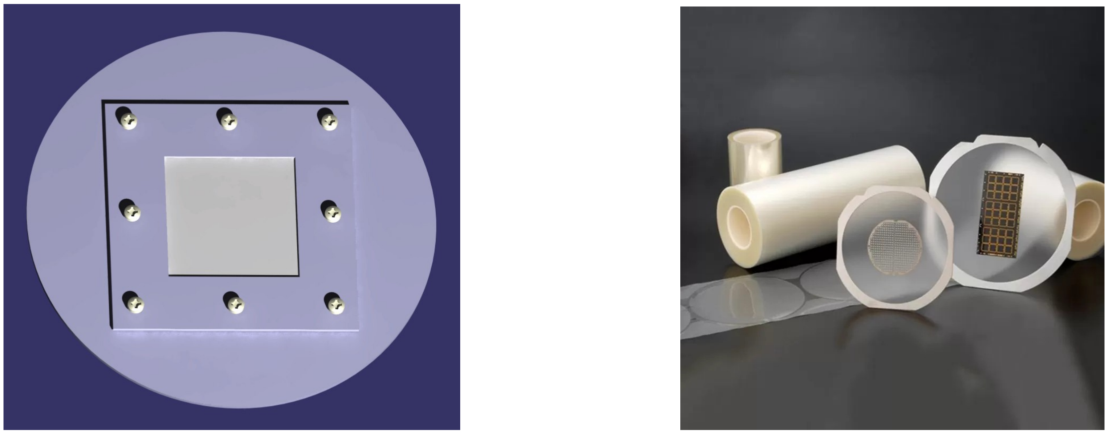
The first idea that was discussed was to use screws to attach an aluminum frame to an aluminum wafer, holding the border of the quartz chip in between (see figure 9a). Aluminum was chosen because it is easy to work with and



(a) (b)

Figure 8: Middle of quartz chip with a magnitude of 10k (a) and 34k (b) after the deposition of AlScN (40%) with a gas ratio of $Ar/N_2 = 10/30$.

has high thermal conductivity. However, this method has the drawback of the screws extending beyond the wafer, which could potentially interfere with the movement of the Spider's arm. A second idea was to use an aluminum ring with UV-tape to hold the chip in place, similar to the method used in the CMi for wafer dicing (figure 9b). This method would be easy to implement and could hold the entire chip flat and not only in the borders. However, that kind of tape is not allowed in the Spider chamber. Additionally, the high temperature of the deposition process, 300°C, would likely render any tape ineffective. This method may also not be very efficient in term of thermal dissipation as the chip would be directly in contact with the tape which would probably isolate it a bit from the heater. However, this technique could potentially be useful for other applications at lower temperatures.

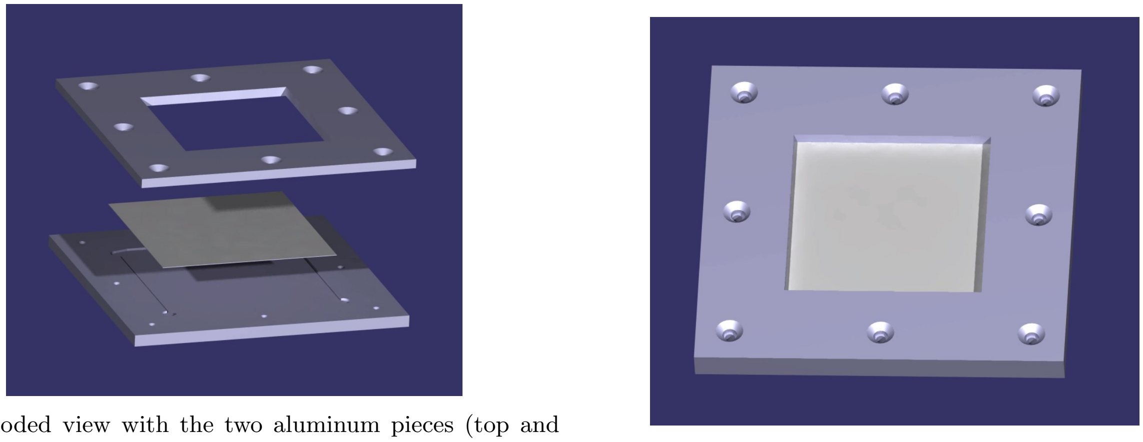


(a) (b) [9]

Figure 9: First design ideas for the holder

The CMi staff suggested a third approach that appears to be the most promising. This method is similar to the first one, but instead of using an aluminum wafer, a squared bottom piece would be fabricated (figure 10). The whole system would then be deposited on a carrier wafer. This approach allows for the use of a standard carrier wafer and eliminates the risk of screws extending beyond the wafer and potentially interfering with the Spider's arm, which simplifies the design.

The constraint given by the CMi staff is that the whole system should not have a thickness of more than 5mm. For that reason, the top and bottom aluminum pieces were chosen with a thickness of 2mm and 2.5mm respectively. The chosen screws are M2 conical head screws with a length of L=4mm based on some found in the Misumi



(a) Exploded view with the two aluminum pieces (top and bottom) with a quartz chip in between.

(b) Image of the mounted system.

Figure 10: Images of the third solution for the holder. The screws are not shown on these images.

catalog[1]. By using these, a total thickness of around 4.6mm is reached (4.5mm for both aluminum pieces + 127 for the quartz). The screws are directly screwed in the bottom piece instead of using nuts on the other side of that piece. By doing that, we are sure that there is no gap between the holder and the carrier wafer, which would result in a bad thermal conduction.

A cavity with similar dimension to those of the quartz chip with a tolerance might be created in the bottom piece so to be able to align the quartz chip on the bottom piece before screwing the system. The drawing with dimensions of the pieces can be found in 6.2. The system was discussed with the ATPR mechanical lab and CMi at EPFL.

4 Other depositions

4.1 Layer by layer stress measurements

Several other depositions were performed on wafers with a 200nm wet oxide layer to measure the stress induced by the deposition of each layer. One wafer was deposited with AlScN (40%) and Pt and a second one with three layers: AlScN (40%) - Pt - AlScN (40%). The thickness of the deposited layers are the ones shown on figure 2.

Wafer ID	Layers on top of oxide	$Ar/N_2[sccm]$	Substrate bias [W]
110167	AlScN (40%) - Pt	-	-
110166	AlScN (40%) - Pt - AlScN (40%)	10/30	2
123896	AlScN (40%) - Pt - AlScN (40%) - Pt	10/30	2

Table 2: Deposition parameters for the stress characterisation of each deposited layer. Ar/N_2 ratio and substrate bias are the values used for the piezoelectric layer.

The results for wafer 123896 seem unexpected compared to the stress measured on wafer 110166 (table 3), because the addition of a Pt layer typically reduces compressive stress. One possible explanation for this difference is that the wet oxide layer on one of the wafers may not have been 200nm thick due to a potential error, which could lead to an error in the calculation as the wrong layer thickness is then used. An other explanation could be that, as each deposition was done on different wafers, it would results in slight changes in the thickness of the layers and on the bending of the wafers due to stress and hence gives results that are not perfectly correct.

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[1] `https://fr.misumi-ec.com/vona2/detail/110302280970/?CategorySpec=00000230620%3a%3ah%0900000230744%3a%3anvd00000000000001`

Wafer ID	Thickness [Å]	Stress 0° [MPa]	Stress 90° [MPa]
110167	1’900	85.7	96.3
110166	11’900	-335.1	-339.6
123896	13’650	-374.6	-379.1

Table 3: Layer by layer stress measurements using the Toho Technology FLX 2320-S tool with the thickness given in column two.

4.2 Tests with Molybdenum

Due to the accessibility of target materials with the Spider, some tests were also done with Molybdenum layers instead of Pt. Indeed, it was shown by [10] that Mo is also a good seed layer for the preferred orientation of AlN films. We can see in table 4 that very low value of stress were obtained in this case. The thickness of the AlScN piezoelectric layer was measured using the Filmetrics F54 instrument. The quality of the fit was not ideal, with a goodness of fit value around 0.6-0.7. However, it is unlikely that this would significantly affect the results obtained with the Toho Technology FLX 2320-S tool as the differences between the measured thickness and real values should be small.

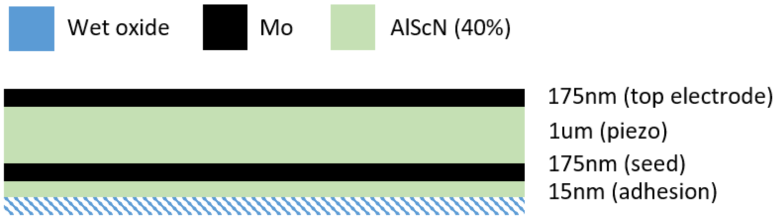

Figure 11: Thicknesses and materials deposited.

Wafer ID	Ar/N$_2$[$sccm$]	Substrate bias [W]	Thickness [Å]	Stress 0° [MPa]	Stress 90° [MPa]
110123	10/30	2	13’130	95.4	94.9
110130	20/30	2	13’260	97.6	97
110135	10/30	3	12’880	59.5	62.3

Table 4: Deposition parameters of the AlScN (40%) piezoelectric layer on molybdenum done with the Pfeiffer SPIDER 600 at 200°C. Thickness of the forth column is the one used for the calculation of stress

5 Conclusion

The purpose of this project was to find the best parameters for depositing AlN and AlScN layers onto a quartz substrate in order to take advantage of the strong coupling of AlN and the low temperature coefficient of frequency of quartz. To do so, a first test was conducted on a quartz substrate, but the quartz experienced stress and developed some cracks. To address this issue, additional tests were performed on wafers with a wet oxide layer in order to determine the optimal deposition parameters that would minimize the stress in the layers. After identifying suitable parameters, a second test was conducted on quartz using the determined parameters. Unfortunately, the result was not the one expected. However, it is hoped that using a new holder that would maintain the substrate flat during the deposition may help to obtain better piezoelectric properties of the AlN or AlScN films. Moreover, using shadow masks as the ones provided by the company towards the end of the project could also result in lowering the amount of stress on the quartz after the depositions.

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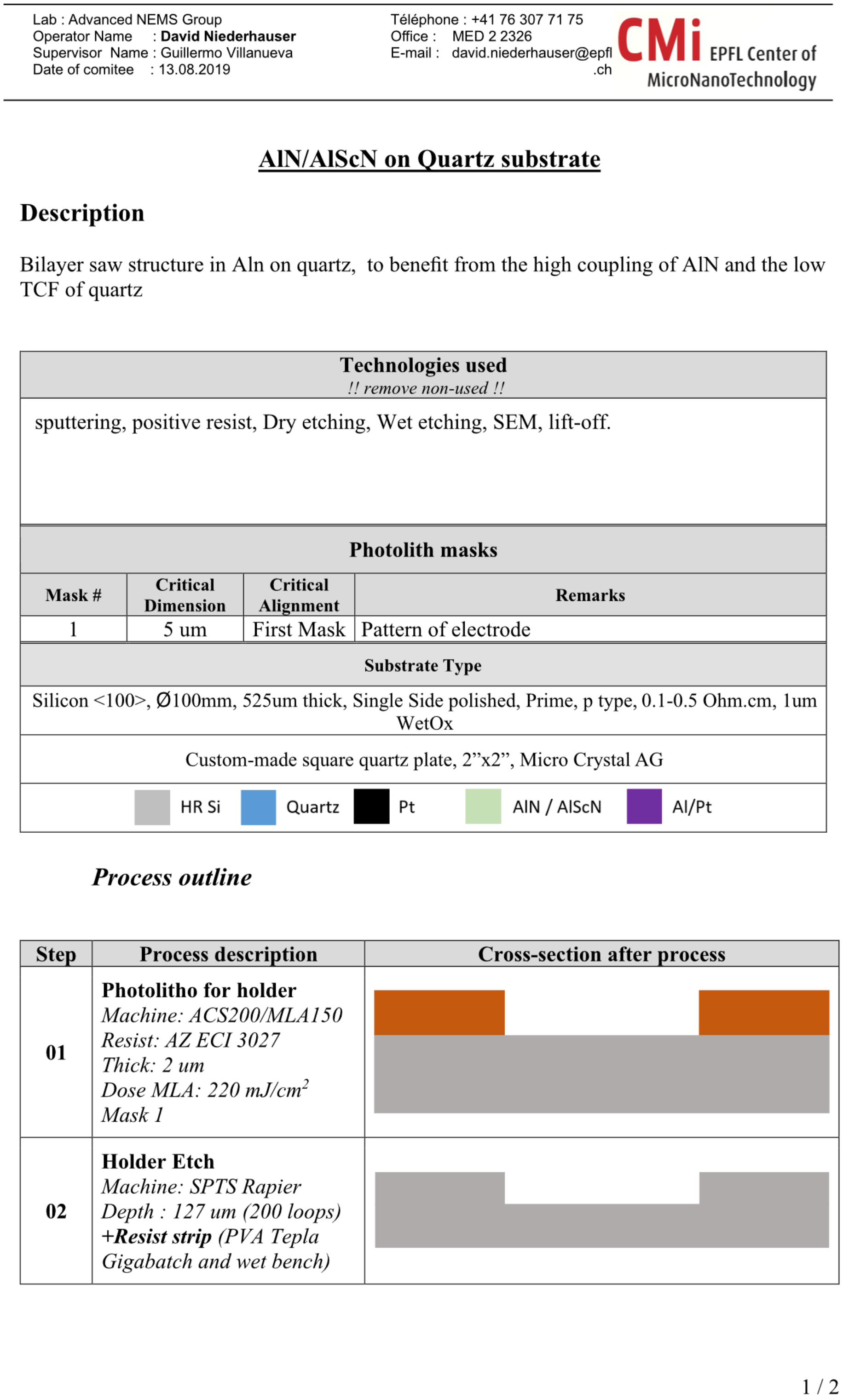
6 Supplementary material

6.1 Process flow



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AlN/AlScN on Quartz substrate

Description

Bilayer saw structure in Aln on quartz, to benefit from the high coupling of AlN and the low TCF of quartz

Technologies used *!! remove non-used !!*
sputtering, positive resist, Dry etching, Wet etching, SEM, lift-off.

Photolith masks			
Mask #	**Critical Dimension**	**Critical Alignment**	**Remarks**
1	5 um	First Mask	Pattern of electrode

Substrate Type
Silicon <100>, Ø100mm, 525um thick, Single Side polished, Prime, p type, 0.1-0.5 Ohm.cm, 1um WetOx
Custom-made square quartz plate, 2”x2”, Micro Crystal AG
▩ HR Si 🟦 Quartz ⬛ Pt 🟩 AlN / AlScN 🟪 Al/Pt

Process outline

Step	Process description	Cross-section after process
01	**Photolitho for holder** *Machine: ACS200/MLA150* *Resist: AZ ECI 3027* *Thick: 2 um* *Dose MLA: 220 mJ/cm^2* *Mask 1*	
02	**Holder Etch** *Machine: SPTS Rapier* *Depth : 127 um (200 loops)* ***+Resist strip** (PVA Tepla Gigabatch and wet bench)*	

Lab : Advanced NEMS Group
Operator Name : **David Niederhauser**
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Date of comitee : 13.08.2019

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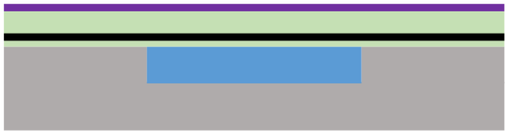
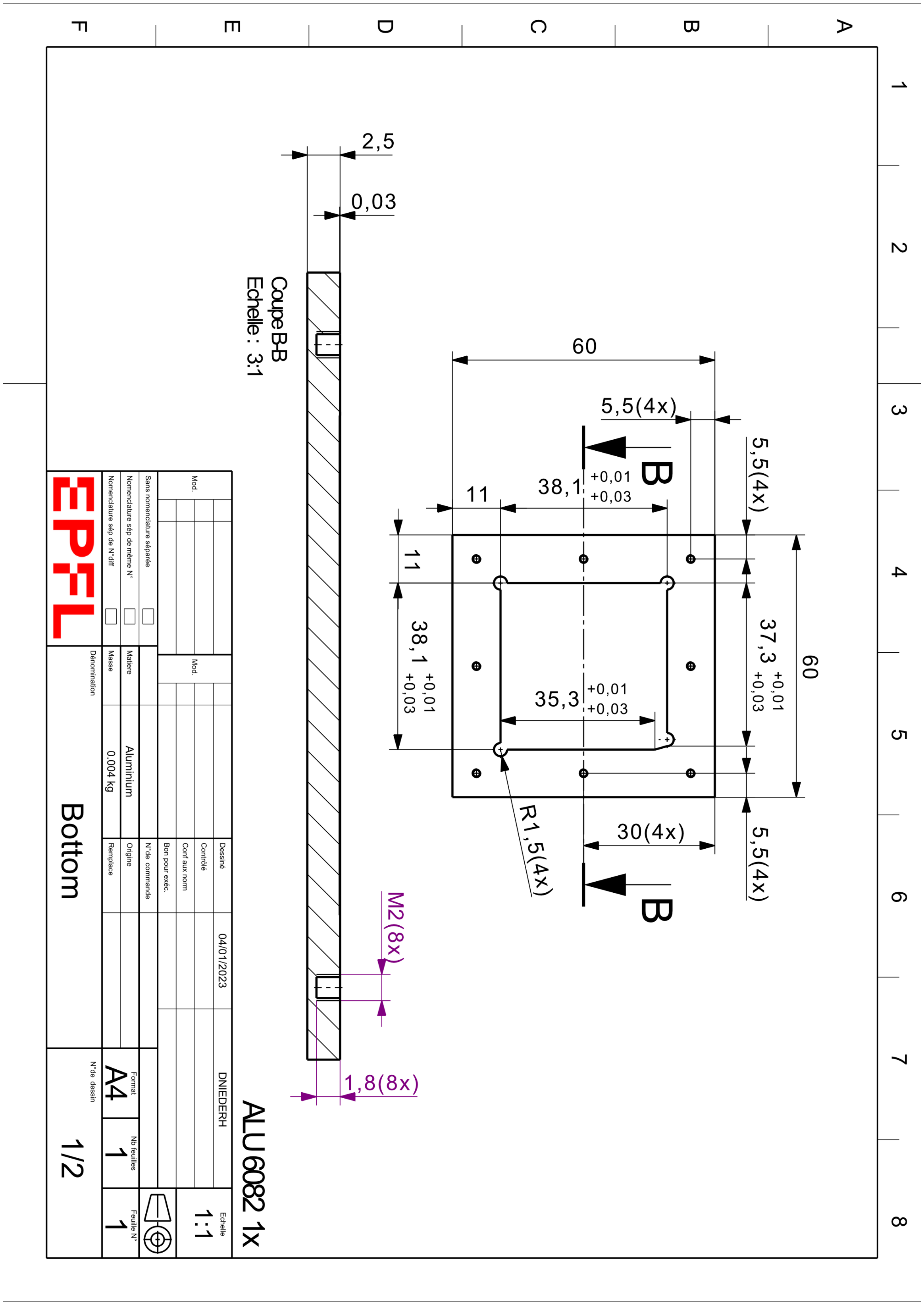
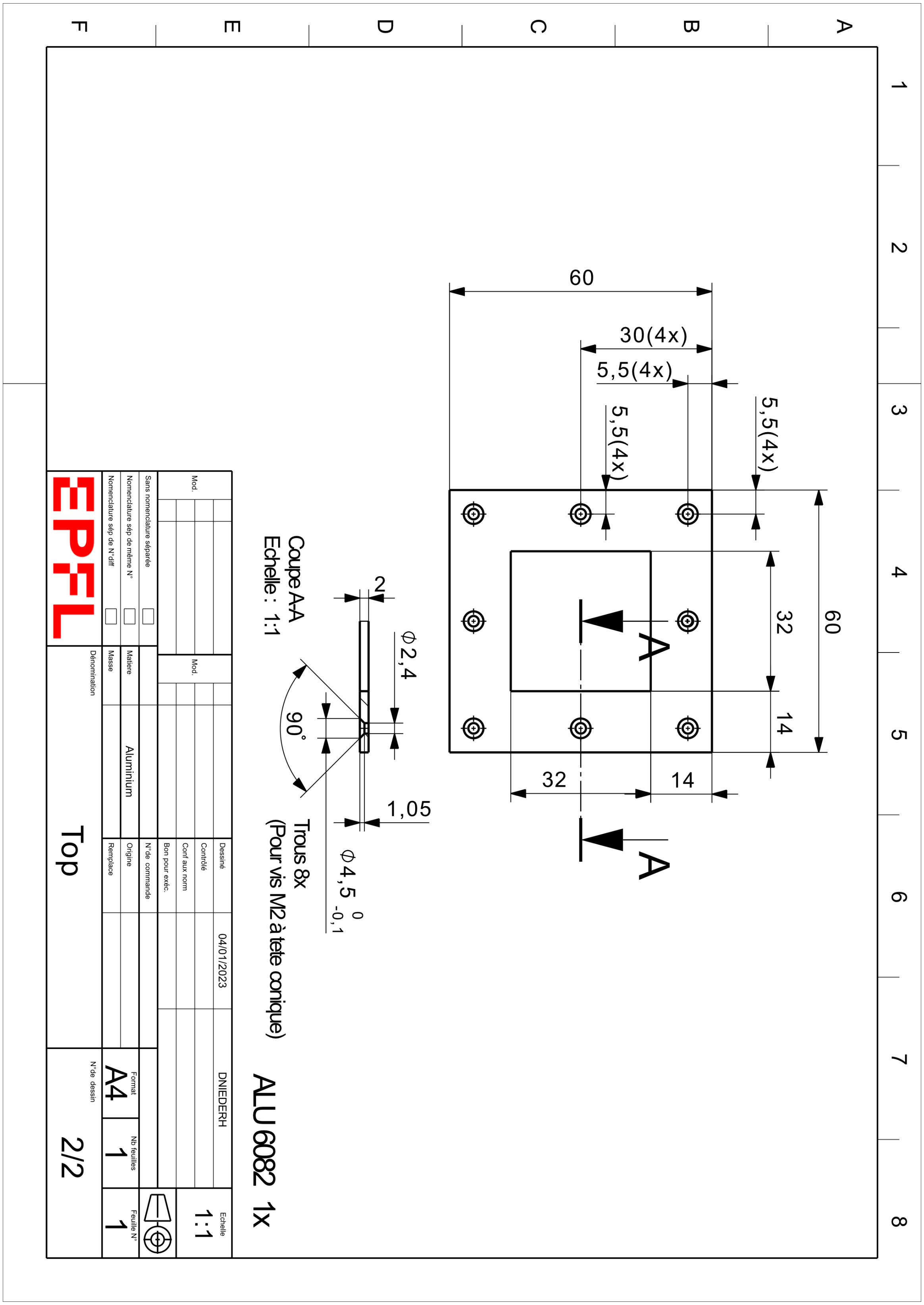
03	**Piezo layer sputtering** *Machine: Pfeiffer Spider 600* *Materials :* *Al(Sc)N-Pt-Al(Sc)N-[Al/Pt]* *Thickness :* *15nm (18s) /175nm (33s) /1000nm (18min) /175 nm (33s)* *Temperature :* *AlN/AlScN: 300°C* *Pt: 200°C*	

6.2 Catia drawings



Sans nomenclature séparée ☐
Nomenclature sép de même N° ☐
Nomenclature sép de N°diff ☐
Matiere: Aluminium
Masse: 0.004 kg
Dénomination: Bottom
Dessiné: 04/01/2023 DNIEDERH
Contrôlé
Conf aux norm
Bon pour exéc.
N°de commande
Origine
Remplace
Format: A4
Nb feuilles: 1
Feuille N°: 1
Echelle: 1:1
N°de dessin: 1/2


A
B
C
D
E
F
1
2
3
4
5
6
7
8
60
30(4x)
5,5(4x)
5,5(4x)
5,5(4x)
60
32
14
32
14
A
A
2
ϕ2,4
90°
1,05
ϕ4,5 0 -0,1
Coupe A-A
Echelle : 1:1
Trous 8x
(Pour vis M2 à tete conique)
ALU 6082 1x
EPFL
Sans nomenclature séparée
Nomenclature sép de même N°
Nomenclature sép de N°diff
Mod.
Mod.
Dessiné
04/01/2023
DNIEDERH
Contrôlé
Conf aux norm
Bon pour exéc.
N° de commande
Origine
Remplace
Matière
Aluminium
Masse
Dénomination
Top
Format
A4
Nb feuilles
1
Feuille N°
1
Echelle
1:1
N° de dessin
2/2