CPSS Transactions on Power Electronics and Applications, pp. 1–13, 2023

Scalability assessment of the parallel operation of direct current transformers

R. P. Barcelos and D. Dujic

POWER ELECTRONICS LABORATORY
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication.

Scalability Assessment of the Parallel Operation of Direct Current Transformers

Renan Pillon Barcelos, *Graduate Student Member, IEEE,* and Drazen Dujic, *Senior Member, IEEE,*

***Abstract*—Paralleling duty-cycle controlled high-power converters is well understood while achieving the same with uncontrolled resonant converters poses certain challenges. In order to predict the current sharing unbalance after paralleling several direct current transformers, this paper proposes a methodology to define the quality of the parallel connection considering system-level parameters. Based on the input impedance of the small signal model, critical parameters are identified, and the impact of the different levels of parameter variation on the current sharing of direct current transformers is evaluated. Then, design constraints based on the model are set to achieve satisfying current sharing considering the resultant input impedance. Further, the impact of the switching frequency, considered the only design degree of freedom, on the input impedance is used to modify the current sharing between the modules. Modeling and predictions are verified by means of simulation and experimental investigations.**

***Index Terms*—Current sharing, DCT, Impedance, LLC converter, parallel operation, resonant converter.**

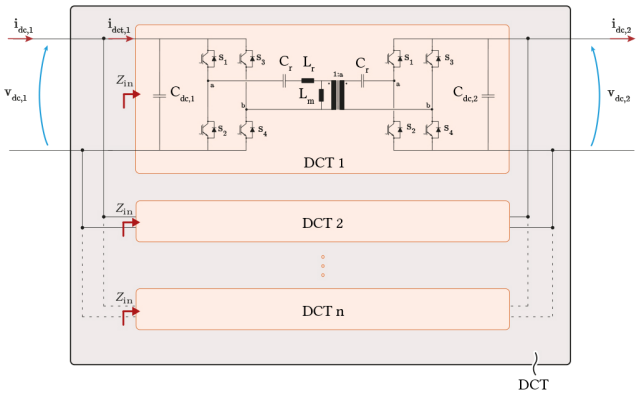


Fig. 1. A high-power DCT composed of several DCTs operating in parallel. Every DCT operates in an open loop.

I. Introduction

High-power DC-DC converters are key technology, still largely underdeveloped, to interface two DC buses, particularly for DC grids at medium and high voltage ranges. Among several applications, DC collection and DC microgrids are the most popular use cases for these power converters [1], [2]. Their goal is to integrate renewable generation and create more advanced DC grids. However, considering MW level power requirements and the corresponding impact on the voltage and current rating, scalable arrangement of lower rating power converters becomes an alternative to reach high power [3].

The Direct Current Transformer (DCT) relying on LLC resonant converter, has operation principles similar to an ac transformer. This converter connects and isolates two DC buses and transmits power according to the natural power flow of the system [4]. Nevertheless, only a few prototypes have been demonstrated in the range of a few MW [5], [6], and the parallel connection of several DCTs can become an option to meet the demands of higher power applications, especially once DC voltages are standardized.

The obvious advantage of the parallel operation is the possibility to increase the power rating beyond the single unit. With this configuration, the building block can be connected in parallel keeping the same operational principle [7] (as illustrated in Fig. 1). However, in practice, every parallel module is likely slightly different due to variations and tolerances of parameters, which creates a natural power/current unbalance between the modules. In this way, the parallel operation brings challenges around the parameter variation and the converter interaction that need to be addressed to ensure a satisfying current sharing.

The parallel operation of converters has been extensively analyzed and demonstrated for different power converters. In the literature, the active methods are based on the use of control loops, adjusting the switching frequency or resonant parameters by detecting the current of each module and realizing a satisfactory current sharing. For instance, in [8] and [9] the current feedback is used to adjust the power of each converter ensuring the correct current sharing. In [10] current sharing problem is solved by using a switch-controlled capacitor to modulate the voltage gain of individual power converters.

Different approaches rely on the passive solutions by means of hardware integration or as a complete integrated design with multi-winding transformer [11], [12], [13]. The main advantage is the absence of current measurements to ensure the current sharing, but they require extra elements and internal connection between modules.

All of the previously mentioned solutions perform the analysis aiming to draw design rules and promote correction on the current sharing unbalance using the available degrees of freedom (e.g. control, hardware changes, etc. [14], [15],

The results presented in this paper are a part of the EMPOWER project that has received funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation program (Grant agreement No. 818706).

R. Barcelos and D. Dujic are with Power Electronics Laboratory, Ecole Polytechnique Federale de Lausanne (EPFL), 1015 Lausanne, Switzerland. (Corresponding author: renan.pillonbarcelos@epfl.ch)

Digital Object Identifie 10.24295/CPSSTPEA.2023.00030

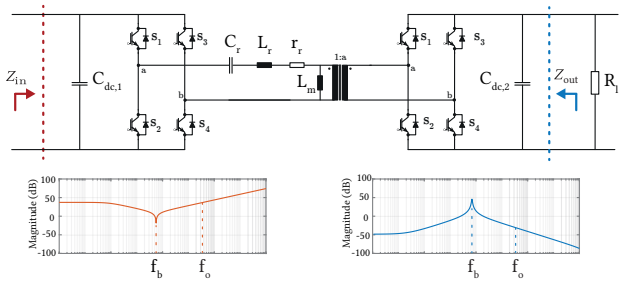


Fig. 2. DCT circuit and illustration of the input impedance vs output impedance for the sub-resonant operation, adapted from [20]. f_0 is the resonant frequency, and f_b is the beat frequency pole given by $L_r\left(1+(\omega_0/\omega_s)^2\right)$ and output capacitor C_{dc}.

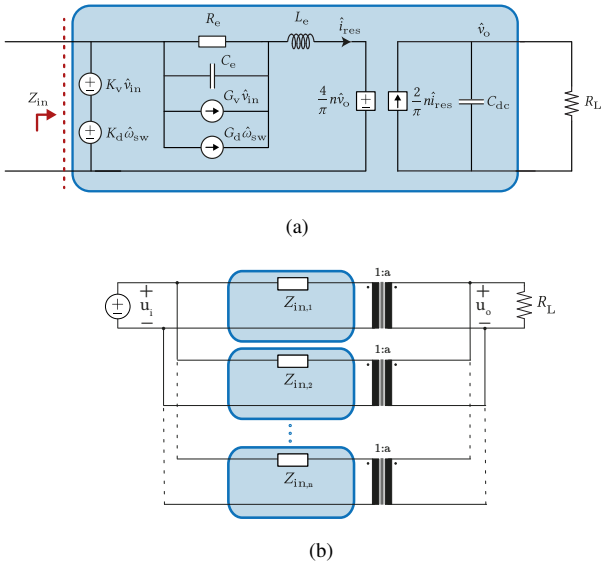


Fig. 3. (a) Small signal model of LLC converter [20]. (b) Resultant input impedance circuit of the converter with ideal transformer representation when paralleling several modules.

[16], [17], [18], [19].) However, in this work, we consider that each module operates in an open loop at the fixed switching frequency, without any connection in the resonant tank between the paralleled modules. Thus, the converter characteristics dictate the current sharing unbalance and the feasibility of parallel connection, which must be understood, modeled, and eventually controlled.

Firstly, the parallel connection of the DCTs is analyzed by considering all combinations of parameter variations, in certain ranges. Secondly, the current sharing unbalance is mapped and predicted in order to ensure the operation of DCT within the requirements. And finally, if the predicted current sharing unbalance satisfies the requirements (e.g. being less than tolerated or within ratings of each DCT module), the high-power DCT can be operated with the selected design constraints.

To quantify this analysis, this paper proposes an input impedance-based methodology to evaluate the viability of parallel operation of DCTs. Further, sensitivity analysis of the input impedance is performed using the small signal model to highlight the impact of each contributor on the input impedance and the current sharing performance. Consequently, design constraints are set, and crucial information about the parallel operation is assessed. Lastly, this paper proposes a solution to enhance the current sharing with the switching frequency and demonstrate with experiments the impact of switching frequency in the current sharing.

This paper is organized as follows: Section 2 describes the LLC converter modeling and the sensitivity analysis of the parameters variation on the input impedance; Section 3 investigates the current sharing unbalance and the scalability aspect for multiple DCTs in parallel connection; In Section 4, simulation results for some design examples and the use of frequency modulation to perform corrections are evaluated; In Section 5, the experimental results of two similar, but not identical, DCTs operating in parallel are presented followed by Section 6, where discussion is provided. The conclusions are presented in Section 7.

II. DCT Modeling and Sensitivity Analysis

The most popular modeling approach for the resonant converter is based on the First Harmonic Approximation. This model allows very simple and direct converter design rules, providing the resonant tank and voltage gain characteristic, and a good representation of the load impact in the converter characteristics. With this model, the rectifier and output filter can be easily represented by an equivalent AC resistance on the primary side. However, as only the first harmonic is considered and the current is not purely sinusoidal, this model leads to big mismatches when the operation is away from close proximity of resonant frequency.

Alternatively, models with more details are derived based on the terminal behavior dynamics [21], time domain equations [22], model in rotational frame [23], [24], [25], and small signal model [26], [20], [27], [28], [29]. In particular, the small signal modeling of the LLC converter is very demanding due to splitting the harmonic signals into sine and cosine components. It results in a large state-space matrix recently explored in [30]. Nevertheless, the approximated equivalent circuit described in [20] is used in this work, which has enough details to perform the necessary analysis based on the input or output impedance.

Works analyzing parallel operation usually rely on the voltage gain [16], [31], [14], resonant tank parameters [32], [15], or on the analysis of the resulting output impedance [33]. The input impedance has been the focus of works related to stability analysis as in [34], however, it can also be used for current sharing prediction. From one side, the output impedance defines the contribution of each DCT block to provide current to the output load. And from the other side, the input impedance indicates how much current is taken from the primary source. Either of them could be used to evaluate power-sharing of parallel connected DCTs, as open loop operation is considered. Figure 2 shows the DCT topology and an illustration of input and output impedance.

For the parallel operation, it is important to map the impact of variation on the resonant tank parameters, involved in power

TABLE I
BASE DCT PARAMETERS

Description	Symbol (Unit)	DCT
DC Voltage 1	$V_{dc,1}$ (V)	750
Turns ratio	a	1
Load	P_{dc} (kW)	50
Switching frequency	f_{sw} (kHz)	10
Magnetizing inductance	L_m (μH)	750
Leakage inductance	L_r (μH)	11.6
Resonant Capacitor	C_r (μF)	37.5

TABLE II
RANGE OF PARAMETER VARIATION AROUND THE RATED VALUE FOR SENSITIVITY ANALYSIS

Tol	L_r (μH)	C_r (μF)	L_m (μH)	f_s (kHz)
Rated	11.6	37.5	750	10
20%	9.28↔13.92	30↔45	-	-
15%	9.86↔13.34	31.875↔43.125	-	-
10%	10.44↔12.76	33.75↔41.25	675, 750, 825	9, 10, 11
5%	11.02↔12.18	35.62↔39.37	-	-
1%	11.48↔11.71	37.12↔37.87	-	-

transfer. Variations of the leakage inductance, magnetizing inductance, and resonant capacitance are the individual parameters of each DCT. The load and the DC link capacitors are hard-wired and can be considered perfectly connected, meaning that the load is seen equally by each module and dc capacitors are connected in parallel increasing the total capacitance at terminals, with an increase of total power ratings. Yet, the MFT turns ratio is considered constant and the winding resistance variation of each MFT is not considered.

A. Small signal modeling of LLC converter

The advantage of the small signal model for sensitivity analysis is the easy inclusion of relevant design parameters. Yet, while evaluating the resonant tank variation, the model can easily shift between under and over-resonance operation. The equivalent circuit is shown in Fig. 3(a). Based on the model described in [20], the input impedance of the LLC converter is described by (1), where $\omega_n = \omega_{sw}/\omega_r$, and details are available in Appendix A.

The small signal model is derived separately for operation with over and under-resonance operation. For the situation where the switching frequency is lower than the resonant frequency, the magnetizing inductance also participates in the resonant circuit. For switching frequencies higher and equal to the resonant frequency, the magnetizing inductance is clamped by the output voltage and is modeled in parallel with the equivalent output load.

With this description, the DCT can be represented with an equivalent input impedance as showed in Fig. 3(b). Thus, when paralleling several DCTs, the complete equivalent model will consist of several impedances in parallel, and the current flowing throughout the branches depends on the equivalent impedance of the DCT.

B. Sensitivity analysis of the input impedance

There are two types of variations that occur on a DCT that impacts the impedance: i) resonant tank parameters variations, and ii) switching frequency. In this sense, the impedance of the DCT can be described as a function of all of these parameters,

$$Z_{in}(\omega) = f(L_r, C_r, L_m, f_s, R_l). \tag{2}$$

The quality factor (Q) could also be included in this equation, but this parameter represents a correlation between factors already listed: $Q = \sqrt{L_r/C_r}/R_{ac}$.

In order to represent results more clearly, the leakage inductance (L_r) and resonant capacitance (C_r) are the base of the input impedance surface. The analysis is performed with normalized values in order to make it as general as possible, and the impedance is computed at the switching frequency, where the power is transferred. The base parameters used are presented in Table I, and the range of values for each of the allowed tolerance under analysis is detailed in Table II.

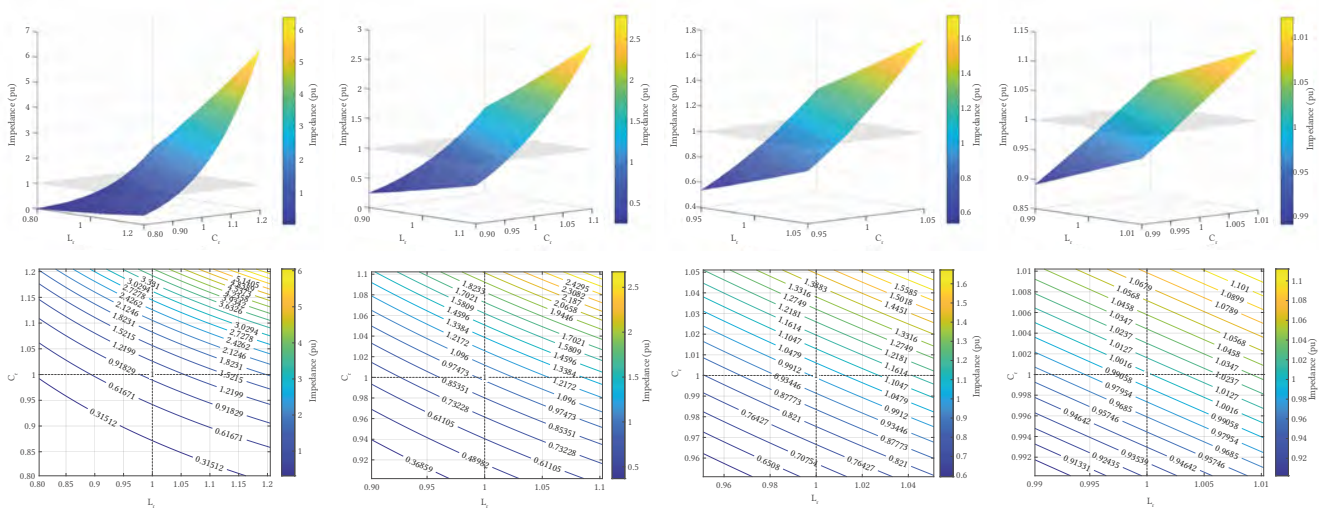
Figure 4 shows the resulting input impedance at switching frequency for an allowed parameters variation of ±20%, ±10%, ±5%, ±1% on L_r and C_r.

With a tolerance of ±20% on L_r and C_r as shown in Fig. 4(a), the value of the input impedance can reach almost 7 times the rated value. It shows that the parameter variation has a big impact on the input impedance value. The contour plot on the bottom details the impedance variation. It highlights the impact of the higher resonant frequency - resulting in a bigger difference between resonant and switching frequency - which leads to a higher input impedance.

However, if the allowed variation is reduced to ±10% as shown in Fig. 4(b), the maximum value is around 2.5 times the rated value. Even further, if the allowed variation is reduced to ±5% and ±1% the maximum deviation of the rated value is reduced to almost 1.8 and 1.15 times the rated value, respectively. Nevertheless, from these plots, it is visible the impact of small variations on the resonant tank parameters and their big influence on the input impedance.

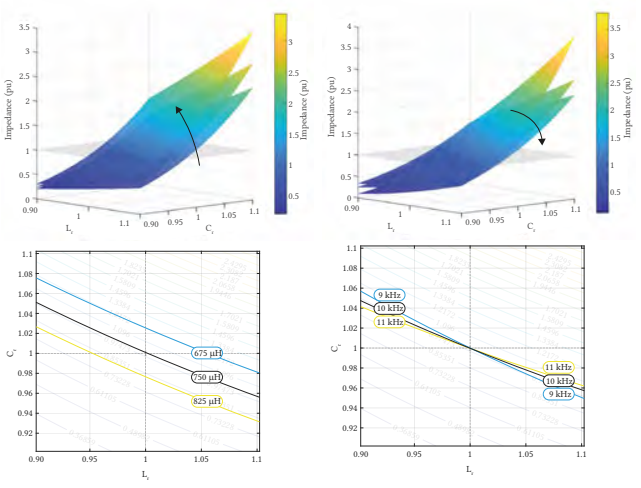
In the previous plots, the switching frequency and magnetizing inductance were fixed at the rated value. However, they also have an influence on the input impedance. The variation of the magnetizing inductance and switching frequency are

$$Z_{in}(s) = \begin{cases} \dfrac{\pi^2}{2}\left(sL_e + \dfrac{\frac{8n^2}{\pi^2}R_L}{R_L C_f s + 1}\right), & \text{for } \omega_n < 1 \\ \dfrac{\pi^2}{2}\dfrac{\left(s^2\ L_e^2 + sL_e R_{eq} + X_{eq}^2\right)(1 + R_L C_f s) + R_{eq}\left(sL_e + R_{eq}\right)}{s^2\ L_e C_f R_L + sL_e + sC_f R_L \frac{R_{eq}^3}{R_{eq}^2 + X_{eq}^2} + R_{eq}}, & \text{for } \omega_n \geq 1 \end{cases} \tag{1}$$



(a) ±20% (b) ±10% (c) ±5% (d) ±1%

Fig. 4. Input impedance variation for different L_r and C_r tolerance. In (a) allowed variation of ±20% can lead to a maximum variation of 7 times the rated value; in (b) ±10% with a maximum variation of almost 3 times; in (c) ±5% with a maximum variation of almost 1.8 times; and in (d) ±1% with a maximum variation of almost 1.15 times. The unity plane represents the impedance having the same value as the base values. The contour plot details the variation of the input impedance.



(a) L_m (b) f_s

Fig. 5. Input impedance for ±10% tolerance on L_r and C_r. In (a) the impact of magnetizing inductance, considering 3 discrete values of -10%, 0%, and +10% of tolerance. Arrow represents the increase in the value under analysis. In (b) the impact of switching frequency on the input impedance, considering 3 discrete values of -10%, 0%, and +10% of tolerance. The contour plot details the surface interception with a unity plane, showing the displacement and rotation/tilt of the curves.

shown in Fig. 5, and the simulated values are also described in Table II. It is considered ±10% tolerance on these two values, which is a realistic and affordable tolerance.

In Fig. 5(a), the impact of the magnetizing inductance is shown. The magnetizing inductance impacts the main input impedance level, and not directly the curve. Its impact is directly related to the resonant tank impedance as the magnetizing inductance is in parallel with the load and in series with resonant inductance and capacitance.

The change in the switching frequency also impacts the input impedance characteristics. By changing the switching frequency, the inclination of the surface changes as shown in Fig. 5(b). In this case, the switching frequency alters the curve more expressively. By acknowledging this, it is possible to observe that the impedance can be modified to some extent, for the same set of parameters only by changing the switching frequency. As will be demonstrated later, by increasing or decreasing the switching frequency one can increase or decrease the input impedance, respectively.

III. Current Sharing of DCTs

Having determined input impedance dependence on the variations of various parameters, the current sharing unbalance is calculated according to the currents flowing on each branch. In this way, relating to the schematic in Fig. 3(b) considering only two DCTs, the currents on each branch is:

$$i_{dct,1} = \frac{u_o - u_i}{Z_{dct,1}}, \tag{3}$$

and

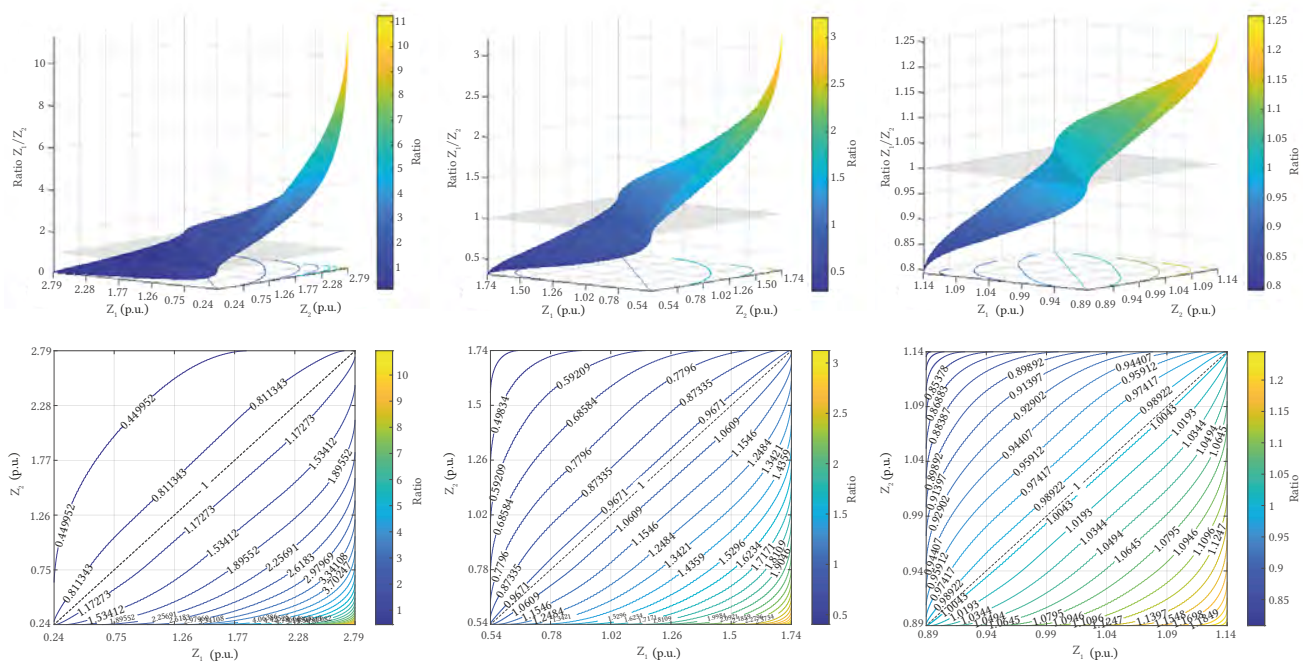
$$i_{dct,2} = \frac{u_o - u_i}{Z_{dct,2}}. \tag{4}$$

As the voltage drop across the DCTs is the same, i.e. $\Delta V_{dct,1} = u_o - u_i = \Delta V_{dct,2}$, the impedance ratio for the case of two DCTs can be defined as (5).

$$\frac{i_{dct,1}}{i_{dct,2}} = \frac{Z_{dct,2}}{Z_{dct,1}} = \delta_I \tag{5}$$

Thus, the impedance ratio brings information regarding the current sharing between the two involved impedances. This definition leads to the following conclusion:

- If $\delta_I = 1$, representing an ideal case, unreachable in practice where two impedance are absolutely identical.



(a) ±10% (b) ±5% (c) ±1%

Fig. 6. Input impedance ratio for two DCTs considering a variation of ±10%, ±5%, and ±5% on L_r and C_r. The unity plane represents the ideal case when the impedance is the same. In (a) parameters variation of ±10%; (b) ±5%, and (c) ±1%. The contour plot details the variation of the impedance ratio value.

- If $\delta_I < 1$ impedance of DCT 1 is bigger than the value of DCT2 which will conduct more current. Until the extreme case where $\delta I = 0$, implying that all power (2 p.u.) is taken by DCT 1 rated for 1 p.u., which is not feasible nor desired in practice.
- If $\delta_I > 1$, similar to the previous case for but DCT 2.

Therefore, Fig. 6 shows the impedance ratio of two DCTs considering a parameters tolerance of ±10%, ±5%, and ±1%. As can be seen, the combination of two DCT designs can result in any of these combinations, with the specified parameters tolerance. For the case of ±10% shown in Fig. 6(a), the impedance ratio can reach a very high value of almost 11 times the ideal case; consisting in the extreme case of one impedance being the highest and other the lowest, among the values provided in Fig. 4(b). However, when reducing the tolerance to ±5%, the maximum reach is 3 times, and when considering ±1%, 1.25 times.

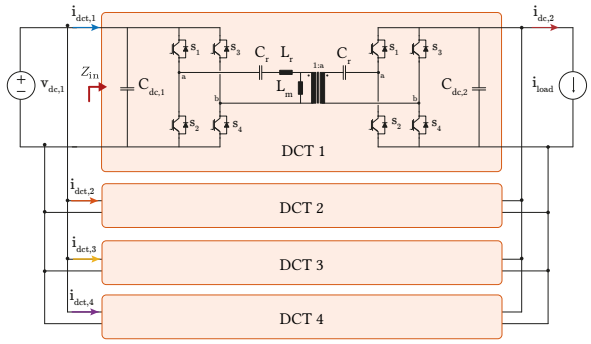
From Fig. 6 one can conclude some important information:

- Even with a highly restrictive parameter tolerance of ±1%, there is a possibility that a combination of DCTs could result in an impedance ratio of 0.79 and 1.25, as shown in Fig. 6(c). These cases are a result of a combination of parameters where each DCT has its variation at the extreme opposite situation, i.e. DCT 1: +1% on L_r and C_r; and DCT2: −1% on L_r and C_r. Thus, with ±1% tolerance on L_r and C_r, the combination of two DCTs can result in a worst case of 25% current sharing unbalance, meaning that for a total load current of 2 p.u., DCT 1 will conduct 1.12 p.u. and DCT 2 will conduct 0.87 p.u. This requirement is hard and expensive to impose on the designs. Still, DCT 1 will have to be oversized for 1.12 p.u. or more, knowing the expected unbalance.
- For designs with a maximum allowed parameter tolerance of ±5%, the worst combination leads to an impedance ratio of 0.31 and 3.2, as shown in Fig. 6(b). This combination results in an overload in DCT 1 of 1.52 p.u. and DCT 2 0.47 p.u. for a 2 p.u load current. Similarly to the previous case, the DCT 1 will have to be oversized to 1.52 p.u. or more.
- If one considers ±10% or higher, there will be more combinations with higher deviation, which can lead to a poor current sharing. For the designs with ±10% as shown in Fig. 6(a), the worst case is $\delta_I = 0.08$, meaning that practically all the current will flow in only one branch. For the case of 2 p.u. load current, DCT 1 will conduct 0.15 p.u. and DCT 2 1.85 p.u. As the parameters can vary in a wider range, the possible combinations between two DCTs increase, and therefore, there will be more chance that the ratio of two DCTs is far away from the unity value, resulting in an unfeasible current sharing situation.

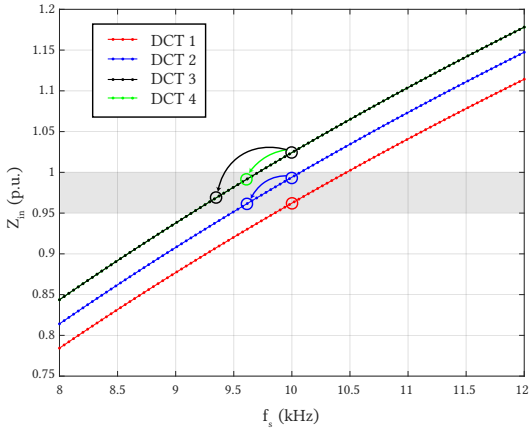
A. Scalability for n DCTs

Similarly, the same approach can be used to assess the current sharing conditions for more than two DCTs. Extending the criteria for the current sharing error, the maximum deviation can be found by:

$$\delta_{I(1,2,..,n)} = max(\delta_{I(1,2)}, \delta_{I(1,3)}, \delta_{I(2,3)}, \ldots, \delta_{I(m,n)}) \quad (6)$$



(a)



(b)

Fig. 7. (a) Four DCTs in parallel to create a higher power DCT. DC currents signalize the corresponding color in the results plots. (b) Input impedance of DCTs for different switching frequencies. The first circle shows the operation at 10 kHz, and the second circuit the final switching frequency used for simulation results. Shaded area with acceptable current sharing range.

Now, in this case, this function takes the maximum unbalance of all the possible dual combinations, and therefore, the final result will give the maximum current sharing error for the set of DCTs. As consequence, the result highlights the two most extreme impedances, that could be adjusted to enhance the current sharing unbalance.

IV. Simulation Results

The simulation of four parallel connected DCTs is performed in this paper to demonstrate and verify the proposed methodology. The system is shown in Fig. 7(a) and Table III summarize the DCTs parameters. DCT 2 is chosen to be the reference base. DCT 1 is chosen to have −10%, and DCT 3 and DCT 4 are chosen to be the same extreme top for the case of +10%, to show that both DCTs create the same current sharing unbalance, for different power levels.

Each DCT operates by itself, in an open loop, and PWM pulses are not synchronized with an initial phase shift of +15° with 10 kHz. In every load step, another DCT is added to ensure that there will be always enough leverage to verify the current sharing unbalance and modify it by changing the switching frequency.

TABLE III
DCTs Parameters of Simulation

Description	DCT 1	DCT 2	DCT 3	DCT 4	Unit
DC Voltage 1		750			V
Rated power		50			kW
Load		50, 100, 150, 200			kW
Switching Freq.		10			kHz
Magnetizing Ind.		750			μH
Leakage Ind.	10.35	11.5	12.65	12.65	μH
Resonant Capacitor	34.537	38.375	42.212	42.212	μF
Leakage Ind.	-10	0	+10	+10	%
Resonant Capacitor	-10	0	+10	+10	%

TABLE IV
Most significant input impedance in p.u., and expected and simulated current sharing unbalance (100% perfect sharing, 0% no sharing).

Case	Lower Z_{dct}	Higher Z_{dct}	Analytical	Simulated
①	0.24	1	24.9%	25.7%
②	0.31	0.33	96.7%	97.2%
③	0.31	1.79	17.3%	18.2%
④	0.29	0.31	93.93%	94.41%
⑤	0.29	1.79	16.2%	17.5%
⑥	0.29	0.34	85.3%	86.6%
⑦	0.29	0.34	85.3%	86.2%

The switching frequency alters the input impedance as seen in Section II, and it can be used to alter the current sharing. Figure 7(b) shows the input impedance of the four simulated DCTs for different switching frequencies. From this plot, one can reduce or increase the switching frequency to change the input impedance and improve the current sharing.

Figure 8 shows the complete simulation of four DCTs. Firstly, only DCT 1 is operating with the nominal load. At t = 0.025 s, the DCT 2 is added to share the total current. At this moment the expected current sharing unbalance is δ_I = 0.24, which leads DCT 1 to conduct 0.76 p.u., and DCT 2, 0.24 p.u. of total power. A summary of the cases with prediction and simulation results is detailed in Table IV.

One alternative to correct the current sharing is changing the switching frequency. In this case, the switching frequency of DCT 2 is reduced to f_s = 9.9 kHz, and the new expected current sharing unbalance is δ_I = 0.33. Reducing even further, a good current sharing is achieved when DCT 2 operates at f_s = 9.6 kHz with a current sharing unbalance of δ_I = 0.82. To further adjustment, the switching frequency of DCT 1 increases to f_s = 10.1 kHz, resulting in a current sharing unbalance of δ_I = 0.96. Still, further adjustment and fine-tuning of the switching frequency for an even better current sharing is also possible.

At the time t = 0.1 s, the load increases to 2 p.u. (100 kW), at this moment both DCTs already sharing the current increases the power equally. Then, the DCT 3 is activated. At this moment, the current sharing unbalance of DCT 3 with DCT 1 is δ_I = 0.17, and with DCT 2 is δ_I = 0.22, resulting in $\delta_{I\,(1,2,3)}$ = [(0.96), (**0.17**), (0.22)]. Therefore, the worst current sharing unbalance is given by DCT 1/DCT 3, and DCT 3 will barely conduct any current, as shown in case ③.

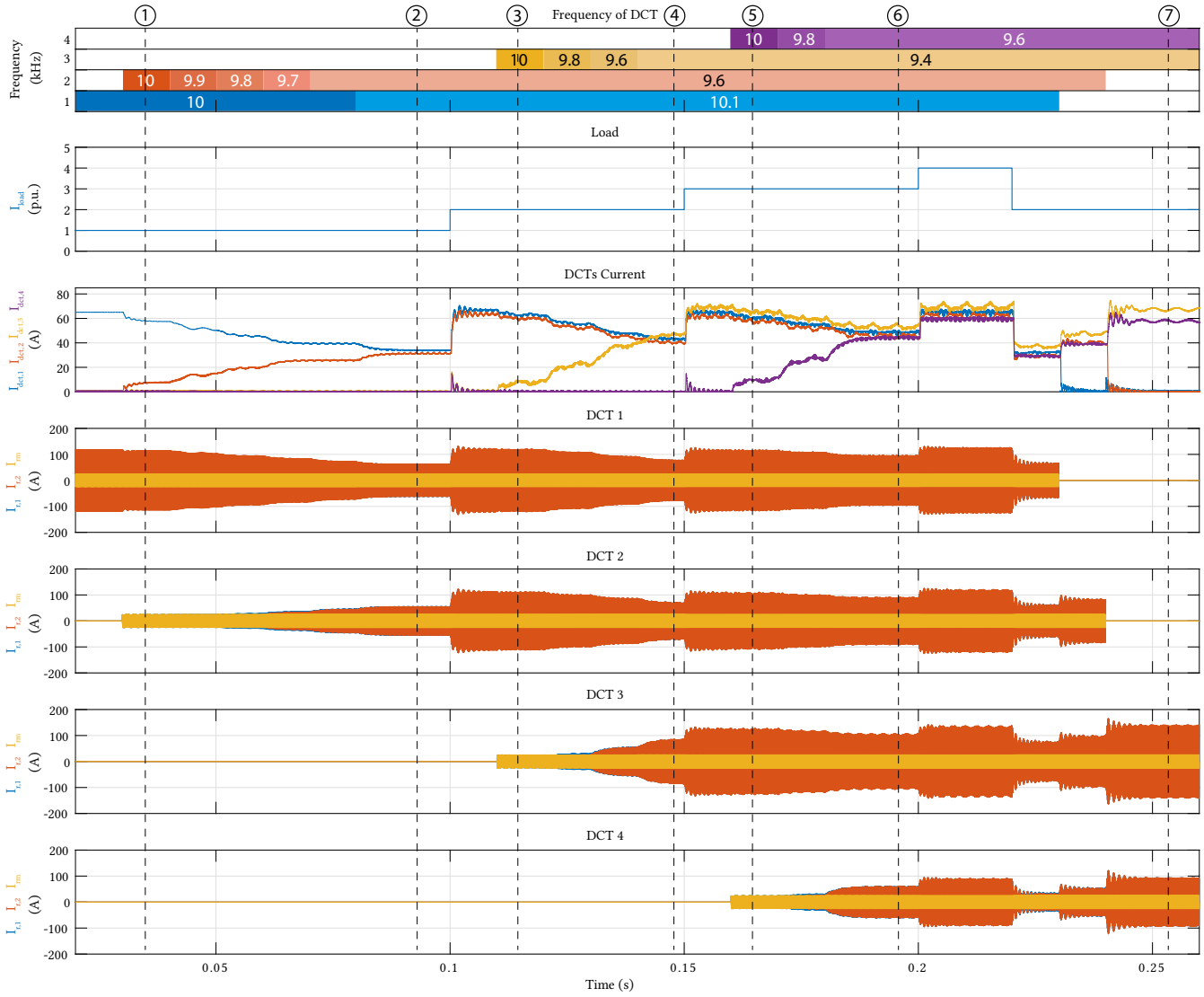


Fig. 8. Simulation results for the parallel operation of four DCTs. From top to bottom: DCTs switching frequency; Load profile; Output DC current of DCTs; Resonant current of primary and secondary side, and magnetizing current of each DCT. Circled numbers correspond to described cases.

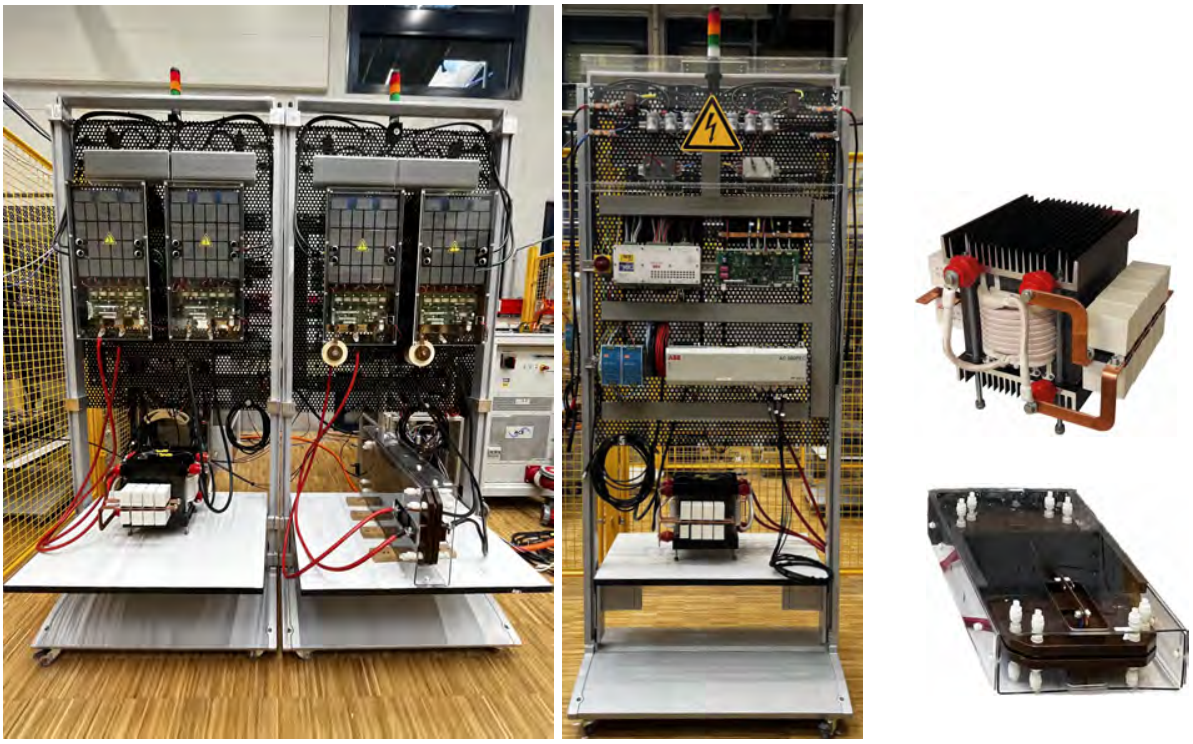
In this situation, the arrangement will not support the 3 p.u. load and an increase in the load would cause overload for DCT 1 and DCT 2. Thus, the same process of adjusting the switching frequency of DCT 3 is performed to reduce the input impedance and enhance the current sharing. The DCT 3 reduces the switching frequency to $f_s = 9.4$ kHz, resulting in a maximum current sharing unbalance of $\delta_I = 0.94$. Which results in case ④.

At the time $t = 0.15$ s, the load increases to 3 p.u. (150 kW), and similarly to the previous case, all DCTs increase the processed power equally.

Later, DCT 4 is activated and starts conducting current according to the current sharing unbalance with the other DCTs of $\delta_{I\,(1,2,3,4)} = [(0.96), (0.85), (0.21), (0.93), (0.23), (\mathbf{0.18})]$, shown in case ⑤.

Then, the switching frequency of DCT 4 is adjusted to $f_s = 9.6$ kHz, resulting in a maximum current sharing unbalance of $\delta_I = 0.85$, given by the combination of DCT 3/DCT 4. Thus, at time $t = 0.2$ s, the load increases to 4 p.u. (200 kW), all DCTs increase the processed power equally. As the current sharing unbalance with DCT 4 is $\delta_I = 0.85$, this leads to an overload of almost 1.2 p.u. of DCT 3, as can be seen in the dc currents of Fig. 8.

Later the load decreases to 2 p.u., and DCT 1 is deactivated. At the time $t = 0.225$ s, it is possible to note that the current sharing unbalance is still given by the maximum current sharing unbalance between DCT 3 and DCT 4. Thus, DCT 2 is deactivated and the current sharing unbalance keeps the same, now operating only with DCT 3 and DCT 4, showing that the maximum current sharing unbalance predicted by the most significant impedance remains true in any case, and it is not affected by the load.



(a) DCTs (b) Rear view of DCT 1 (c) MFTs

Fig. 9. (a) Two DCTs prototypes side by side. (b) Back side of DCT, with AC 800PEC, relays, voltage and current sensors, PECMI, and COMBI-IO. and (c) 100 kW MFTs used to build the two DCTs.

V. Experimental Validation

The experimental verification is performed using the two DCTs prototypes available in the lab. The DCT uses a three-phase VSI developed in the lab, with only two legs operated as FB. Figure 9(a) shows the two DCTs side by side. The power stages are controlled by the ABB's AC 800PEC. Each DCT has its own PWM carrier and there is no synchronization between them. Both DCTs have the same features for the open-loop operation, as described in [35].

The MFTs were built upon the same design specifications: 100 kW, 750:750 V, 10 kHz, $I_{off} \approx 20$ A. However they are realized using different technologies, which resulted in variations on the resonant parameters. Firstly, Fig. 9(c) on top, shows a core type MFT made with square litz wire, air-insulated, core of SiFerrite (UU9316 - CF139) with air-cooled heatsink, and resonant capacitors mounted closely to the MFT [36]. The second MFT, shown in Fig. 9(c) on the bottom, is a planar type with windings made of copper and litz wire, nanocrystalline core (VITROPERM 500F), solid insulation (cast resin), and forced air for cooling, with external resonant capacitors [37]. The parameters of the DCTs are described in Table V.

The input impedance characteristics of the two DCTs prototypes for different switching frequencies are shown in Fig. 10. As one can see, the input impedance of both DCTs is almost the same due to the extra impedance added by the cable connection between the power stage and MFT. Thus, in this case, it is expected the DCTs to have good current sharing during parallel operation.

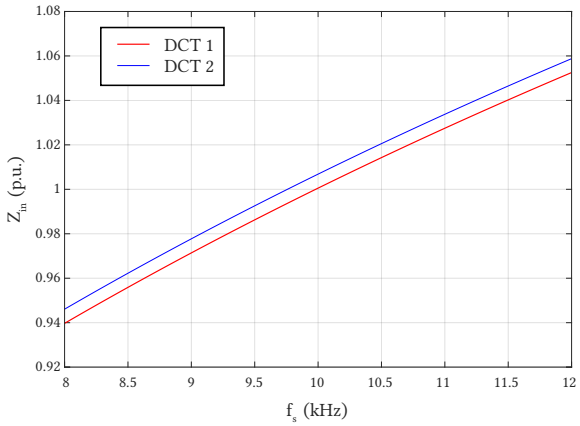


Fig. 10. Variation of the input impedance of the experimental DCT for different switching frequencies, using the analytical model.

For the experimental test, the two DCTs were hard-parallel, and the DC buses are created with two switched power amplifiers - TC.ACS from Regatron, where two legs of a 3-phase 50 kW rated system were used.

The schematic of the parallel operation of the DCT is shown in Fig. 11. The experiment proceeds as follows: i) First the two dc buses are energized, and DCTs DC links are charged; ii) DCT 1 starts its operation and transmits the power according to the voltage difference of the two DC ports; iii) Later, the

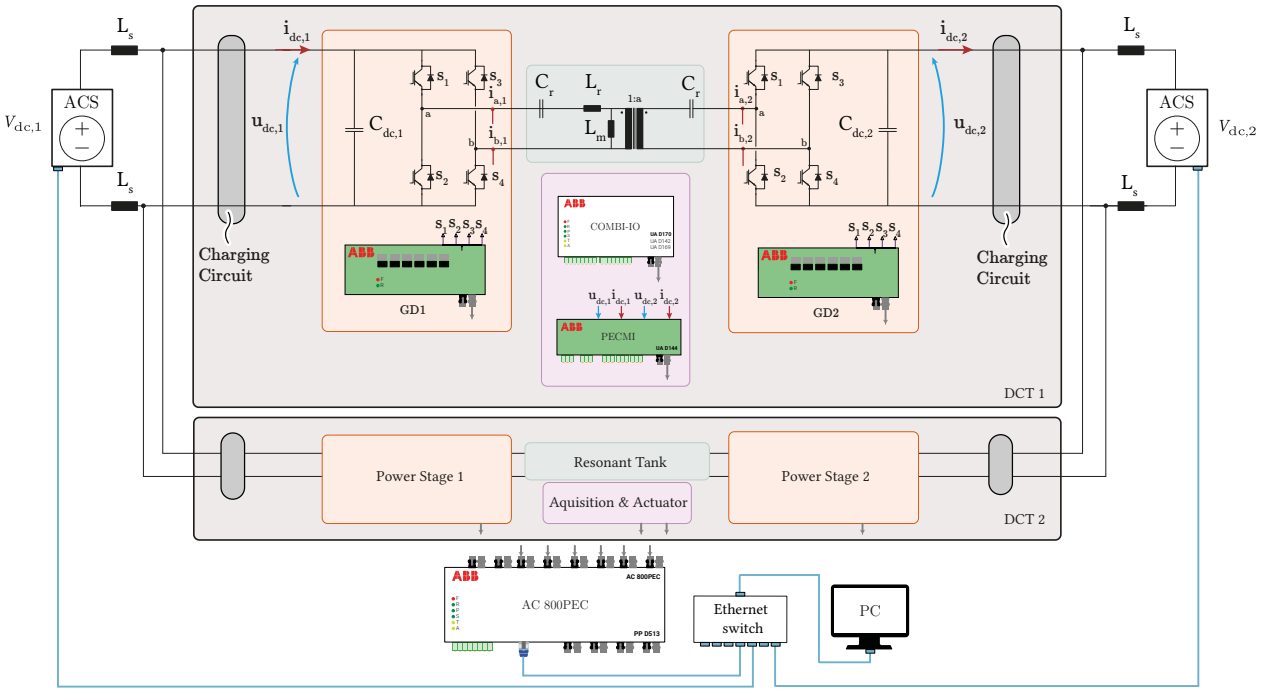


Fig. 11. Schematic of the complete system. The two DC buses are created with voltage sources. For the test setup system, the controller, relays, and power sources are accessed through PC.

TABLE V
EXPERIMENTAL SETUP PARAMETERS

Description	Symbol (Unit)	DCT 1	DCT 2
DC Voltage	$V_{dc,1}$ (V)	750	
Grid inductance	L_s (μH)	30	
Grid resistance	R_s (Ω)	0.1	
Transformer Ratio	$1:a$	1:1	
Leakage inductance	L_r (μH)	11.6^a	9.5
Magnetizing inductance	L_m (μH)	750^a	1100
Resonant capacitor	C_r (μH)	$37.5^{a,b}$	37^c
Cable resistance	R_c (Ω)	0.1^a	0.1
Cable inductance	L_c (μH)	10^a	10
Input Impedance	Z_{in} ($p.u.$)	1	1.02 (1.16)
Switching frequency	f_{sw} (kHz)	10	10 (11)

[a] Base values, [b] ± 5 tolerance, [c] ± 10 tolerance

DCT 2 starts its operation and DCTs start sharing the current naturally.

Figure 12 shows the experimental waveform for the parallel operation of both DCTs operating at 10kHz. In Fig. 12(a) the overview of the transition is shown with dc currents of each DCT, the total DC current, and the secondary resonant currents. In Fig. 12(b) only the dc currents are shown. In this figure, at time $t = 0.5$ s, the DCT 2 is enabled. After the inclusion of DCT 2, the soft-start logic dictates the transient dynamics until the steady-state operation is met. The soft-start duration was pre-defined to 0.1 s, for both DCTs. Lastly, Fig. 12(c) shows the details of the resonant currents, the voltage applied to the resonant tank, and the dc current of each DCT, when operating in parallel.

A second test was performed to evaluate the switching frequency impact. Figure 13 shows the results. Similarly to

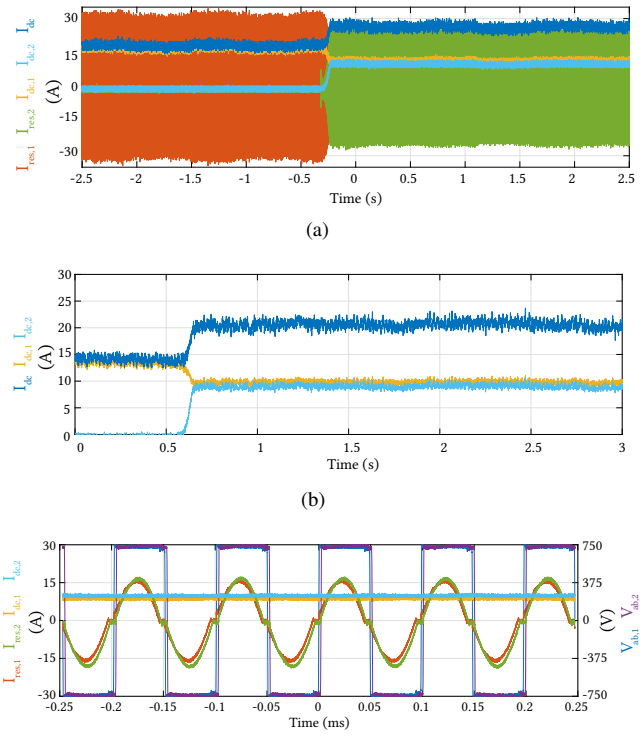


Fig. 12. Experimental waveform of the parallel operation of 2 DCTs (a) Overview of the test with resonant currents and dc currents of both DCTs; (b) DC current of each DCT and total DC current; (c) Details on the resonant currents on the secondary, voltage applied to the resonant tank and the dc current of each DCT. Numbers 1 and 2 represent DCT 1 and DCT 2 respectively.

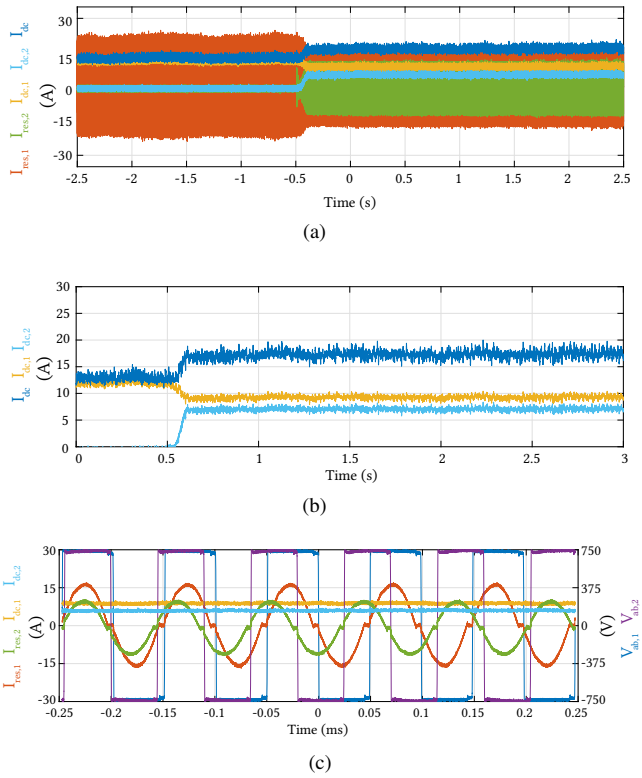


Fig. 13. Experimental waveform of the parallel operation of 2 DCTs with DCT 2 operating with 11 kHz. (a) Overview of the test with resonant currents and dc currents of both DCTs; (b) DC current of each DCT and total DC current; (c) Details on the resonant currents on the secondary, voltage applied to the resonant tank and the dc current of each DCT. Numbers 1 and 2 represent DCT 1 and DCT 2 respectively.

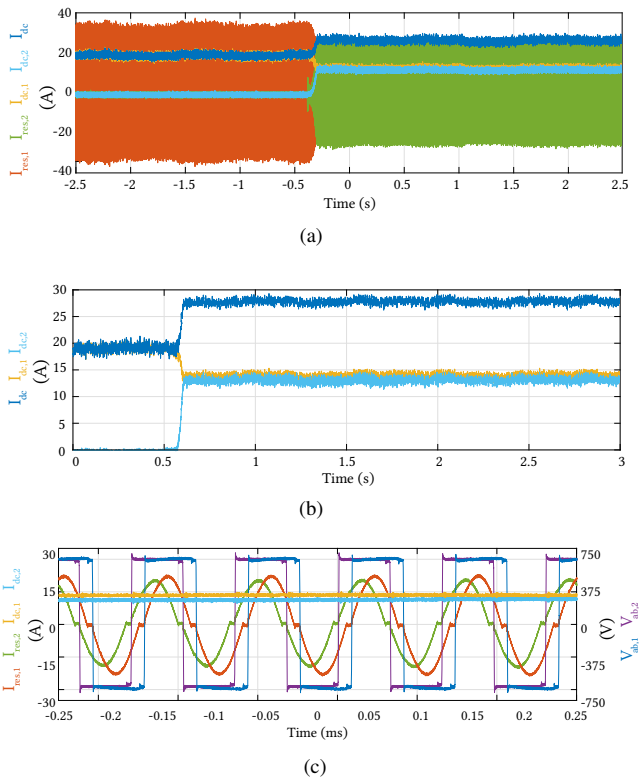


Fig. 14. Experimental waveform of the parallel operation of 2 DCTs, processing $P_{load} \approx 20$ kW. (a) Overview of the test with resonant currents and dc currents of both DCTs; (b) DC current of each DCT and total DC current; (c) Details on the resonant currents on the secondary, voltage applied to the resonant tank and the dc current of each DCT. Numbers 1 and 2 represent DCT 1 and DCT 2 respectively.

the previous test, Fig. 13(a) shows the overview of the test, and Fig. 13(b) the dc current of each DCT and the total dc current feeding the load. Here it can be seen the impact of the switching frequency, where by increasing the frequency of DCT 2 also increased the input impedance and therefore created an unbalance in the current sharing. In Fig. 13(c) the resonant current and the voltage applied to the resonant tank of each DCT are shown.

A third experiment with a different load condition was performed in order to verify its impact on the current sharing. Figure 14 shows the main waveform for this test. Both DCTs are operating with 10 kHz, and at $t = 0.5$ s the DCT 2 is enabled, and two DCTs split the load. The current sharing behavior is the same as for the first test shown in Fig. 12.

VI. Discussion

Clearly, achieving perfect current sharing through a design is hard, next to impossible. The presented analysis on the parallel operation of DCTs helps to solve several questions regarding the requirements and restrictions on the parameter tolerance. The variation in the resonance parameters has a big impact on the current sharing when paralleling DCTs, and differently to the passive solutions to fix the current sharing, there is no connection in the resonant tank between the paralleled modules. In this case, the impedance of the DCT dictates current sharing, and the degrees of freedom to correct the current sharing unbalance is reduced to one variable - switching frequency.

The main question addressed in this paper is to upscale DCTs, acknowledge the current unbalance, and provide guidance about the required trade-off for parallel operation of DCTs. The necessity of operating DCTs in parallel comes with a cost in terms of tighter design tolerance, and the need to still oversize the converter. For example, in case it is desired to have a 4 MW DCT, knowing that the maximum current sharing unbalance could be 20%, one should oversize the DCT by adding an extra module or increasing the module's power ratings. The two options are:

1) Use 4 DCTs rated to 1.2 MW; or
2) Use 5 DCTs rated to 1 MW.

However, when considering both options, one should care about redundancy in case of one module fails. The DCT with 5 modules would still be able to operate at relatively high power while the converter with 4 will be drastically reduced, however, this solution is potentially more costly.

Besides restriction on the parameters tolerance, the switching frequency strongly affects the input impedance and consequently the current sharing. In this sense, performing small adjustments with the operation frequency can enhance the parallel operation. However, this solution would require some attention to its effect on the power stages (an increase of losses), circulating current at the DC link (inclusion of beat

frequency), and different operation points at the resonant tank (higher period of time during discontinuity).

A strategy to enhance the current sharing during operation consists of an upper-level supervisory logic. This should be implemented with the knowledge of the total load and individual processed power. Ideally, this is integrated with the logic to activate and deactivate DCTs when the load changes, focusing on the best efficiency of the overall system.

A simple logic to adjust the switching frequency to enhance the current sharing could be used for this purpose. As an example to adjust the switching frequency of the DCTs, a finite state machine could be created as shown in Fig. 15(a). With this extra layer of operation logic, the arrangement will identify the DCT overloaded and adjust the switching frequency of the DCTs to improve the current sharing. Another option is to use a more aggressive logic where the strategy always tries to correct the modules to share the current all the time.

Figure 15(b) shows a logic that acts on the switching frequency, focusing in increase the power consumption of the DCT consuming less power/current, and decreasing the power of the DCT consuming more power/current. As an example, the DCT 1 and DCT 2 used in the simulation section were simulated with this strategy, as shown in Figure 15(c). The DCTs have all the basic operational open loop control techniques as power reversal detection, idle mode operation during the transitions and soft start, as described in [35].

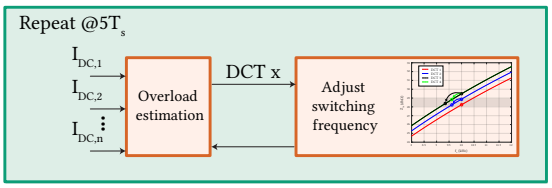
It can be seen that during the start-up of converters due to the high non-linear model, the current sharing is not yet established. Then as the DCTs enter in steady state and the current sharing is given naturally. At the time $t = 0.02$ s, the logic to correct the current sharing unbalance is activated. Immediately, the frequency of DCT 2 decreased to 9.5 kHz, reaching the acceptable current sharing unbalance pre-defined of 5 A, and the steps of frequency were set to 0.1 Hz/ms. Later, a load profile is performed to reverse the power with ramp and step dynamics, showing that only small corrections are performed to fine-tune the current sharing.

In the end, this logic could be used to control the current sharing unbalance all the time, or used only to correct the fabrication differences and let modules operate in parallel at different frequencies during normal operation. Thus, with the second option, the DCT would operate with satisfying current sharing without a closed-loop control.

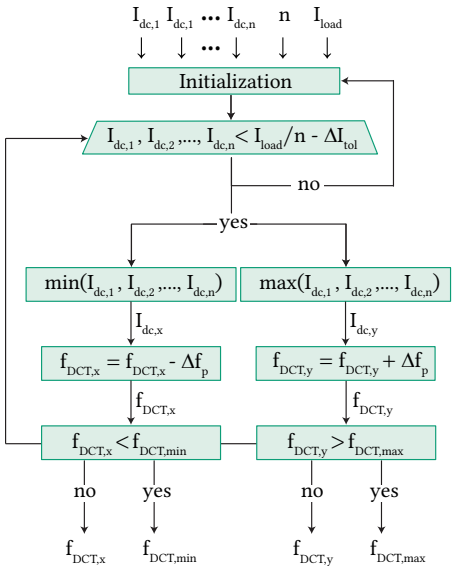
VII. Conclusion

This paper presented a methodology to assess the quality of the parallel operation considering the DCTs, and how to quantify the current sharing unbalance based on the input impedance. With the presented methodology, the design constraints considering the required current sharing percentage can be defined. Besides that, the impact of the switching frequency on the input impedance was investigated in order to enhance the current sharing.

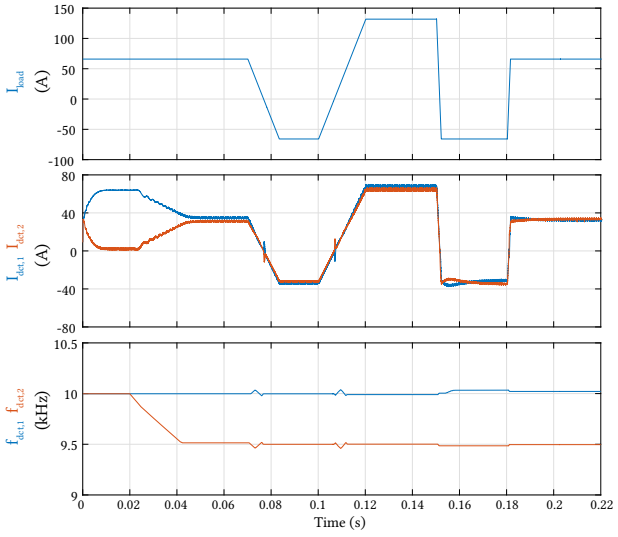
This paper showed that the parallel operation of DCTs is challenging and requires few trade-offs. The input impedance of the LLC converter is very sensitive to the resonant tank



(a)



(b)



(c)

Fig. 15. (a) Finite state machine for parallel operation. Online adjustment of switching frequency to alter the input impedance and improve current sharing unbalance. (b) More aggressive logic to correct the current sharing with switching frequency. ΔI_{tol} the allowed unbalanced, and Δf_p is the step in frequency. (c) Simulation of the parallel operation of DCT 1 and DCT 2 with the logic to enhance the current sharing with switching frequency described in Fig. 15(b). Test with rated power and two times the rated power, with power reversal.

parameters and small deviations in any parameter lead to a high difference in the input impedance. Consequently, the current sharing is directly affected. From the analytical analysis, parameters tolerance from ±1% to a maximum of ±5%, are preferable to be the target tolerance to ensure a minimum current sharing for any possible design. After that, the input impedance needs to be verified in order to verify if DCTs will achieve satisfying current sharing.

The use of different switching frequencies for the DCTs to enhance the current sharing is a possibility to correct the parameter variation of each module. However, an extended evaluation of its impact is required to operate these modules in parallel with different switching frequencies.

APPENDIX
INPUT IMPEDANCE OF SMALL SIGNAL MODEL

This appendix describes the required variables used to compute the input impedance of the small signal model based on the LLC parameters.

- Case $\omega_n \geq 1$

$$R_{eq} = \frac{8}{\pi^2} n^2 R_L \tag{7}$$

$$X_{eq} = \omega_s L_r - \frac{1}{\omega_s C_r} \tag{8}$$

$$L_e = \left(1 + \frac{\omega_o^2}{\omega_s^2}\right) L_r \tag{9}$$

- Case $\omega_n < 1$

$$L_e = L_r \left(1 + \frac{1}{\omega_n^2}\right) + L_m \left(1 - \omega_n\right) \tag{10}$$

ACKNOWLEDGMENT

The results presented in this paper are a part of the EM-POWER project that has received funding from the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme (Grant agreement No. 818706).

REFERENCES

[1] J. Saha, G. N. Brahmendra Yadav, and S. Kumar Panda, "A bidirectional matrix-based ac-dc dual-active bridge for modular solid-state-transformers," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, 2020, pp. 1136–1141.

[2] J. Huber, P. Wallmeier, R. Pieper, F. Schafmeister, and J. W. Kolar, "Comparative evaluation of mvac-lvdc sst and hybrid transformer concepts for future datacenters," in *2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)*, 2022, pp. 2027–2034.

[3] GRIDCON® DC Transformer, Maschinenfabrik Reinhausen GmbH webpage, accessed 26 December 2022, https://www.reinhausen.com/productdetail/power-conversion/gridconr-dc-transformer.

[4] R. Barcelos and D. Dujić, "Direct current transformer impact on the dc power distribution networks," *IEEE Transactions on Smart Grid*, vol. 13, no. 4, pp. 2547–2556, 2022.

[5] S. Joseph, A. K. Abraham, P. Harikrishna Raj, J. Joseph, and K. Nair, "An iterative algorithm for optimum design of high frequency transformer in sst application," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, 2020, pp. 1538–1543.

[6] N. Djekanovic and D. Dujic, "Design optimization of a mw-level medium frequency transformer," in *PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2022, pp. 1–10.

[7] J. Kucka and D. Dujic, "Smooth power direction transition of a bidirectional llc resonant converter for dc transformer applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6265–6275, 2021.

[8] E. Orietti, P. Mattavelli, G. Spiazzi, C. Adragna, and G. Gattavari, "Two-phase interleaved llc resonant converter with current-controlled inductor," *2009 Brazilian Power Electronics Conference*, pp. 298–304, 9 2009.

[9] Z. Hu, Y. Qiu, Y.-F. Liu, and P. C. Sen, "A control strategy and design method for interleaved llc converters operating at variable switching frequency," *IEEE Transactions on Power Electronics*, vol. 29, pp. 4426–4437, 8 2014.

[10] Z. Hu, Y. Qiu, L. Wang, and Y.-F. Liu, "An interleaved llc resonant converter operating at constant switching frequency," *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 3541–3548, 9 2012.

[11] B.-C. Kim, K.-B. Park, C.-E. Kim, and G.-W. Moon, "Load sharing characteristic of two-phase interleaved llc resonant converter with parallel and series input structure," *2009 IEEE Energy Conversion Congress and Exposition*, pp. 750–753, 9 2009.

[12] X. Wang, B. Liu, L. Jiang, and Z. Zhan, "Current sharing analysis for novel paralleled clllc converters," *IEEE Access*, vol. 9, pp. 141 307–141 320, 2021.

[13] H. Wang, Y. Chen, Y.-F. Liu, J. Afsharian, and Z. Yang, "A passive current sharing method with common inductor multiphase llc resonant converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6994–7010, 2017.

[14] B.-C. Kim, K.-B. Park, and G.-W. Moon, "Analysis and design of two-phase interleaved llc resonant converter considering load sharing," in *2009 IEEE Energy Conversion Congress and Exposition*, 2009, pp. 1141–1144.

[15] W. Tang, H. Wang, X. Zhu, W. Mo, W. Gao, and X. Yue, "The analysis of current sharing effect for two-unit paralleled common capacitor llc resonant converter," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2022.

[16] H. Figge, T. Grote, N. Froehleke, J. Boecker, and P. Ide, "Paralleling of llc resonant converters using frequency controlled current balancing," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 1080–1085.

[17] J. Rajagopalan, K. Xing, Y. Guo, F. Lee, and B. Manners, "Modeling and dynamic analysis of paralleled dc/dc converters with master-slave current sharing control," *Proceedings of Applied Power Electronics Conference. APEC '96*, pp. 678–684, 1996.

[18] J. Shi, L. Zhou, and X. He, "Common-duty-ratio control of input-parallel output-parallel (ipop) connected dc–dc converter modules with automatic sharing of currents," *IEEE Transactions on Power Electronics*, vol. 27, pp. 3277–3291, 7 2012.

[19] S. S. Shah, S. K. Rastogi, and S. Bhattacharya, "Paralleling of llc resonant converters," *IEEE Transactions on Power Electronics*, vol. 36, pp. 6276–6287, 6 2021.

[20] S. Tian, F. C. Lee, and Q. Li, "Equivalent circuit modeling of llc resonant converter," *IEEE Transactions on Power Electronics*, vol. 35, no. 8, pp. 8833–8845, 2020.

[21] J. E. Huber, J. Minibock, and J. W. Kolar, "Generic derivation of dynamic model for half-cycle dcm series resonant converters," *IEEE Transactions on Power Electronics*, vol. 33, pp. 4–7, 1 2018.

[22] J. Niu, Y. Tong, Q. Ding, X. Wu, X. Xin, and X. Wang, "Time domain simplified equations and its iterative calculation model for llc resonant converter," *IEEE Access*, vol. 8, pp. 151 195–151 207, 2020.

[23] Y.-H. Hsieh and F. C. Lee, "Modeling resonant converters in a rotating, polar coordinate," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 938–943.

[24] D. J. Kapupara, "Modeling of llc converter using synchronous reference frame transformation approach," in *2020 IEEE International Power and Renewable Energy Conference*, 2020, pp. 1–6.

[25] V. T. Chacko and N. Lakshminarasamma, "Modeling of series resonant converter in synchronous rotating frame," in *2022 IEEE International Conference on Power Electronics, Smart Grid, and Renewable Energy (PESGRE)*, 2022, pp. 1–6.

[26] Y.-H. Hsieh and F. C. Lee, "Accurate small-signal model for llc resonant converters," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 660–665.

[27] ——, "Accurate small-signal modeling of resonant converter based on perturbation on the state plane," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 6809–6816.

[28] M. Mohammadi, F. Degioanni, M. Mahdavi, and M. Ordonez, "Small-signal modeling of llc converters using homopolarity cycle," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 4076–4093, 2020.
[29] Y.-H. Hsieh and F. C. Lee, "Small-signal dynamic and high-bandwidth design of llc resonant converters," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 6136–6143.
[30] J.-D. Hsu, M. Ordonez, W. Eberle, M. Craciun, and C. Botting, "Enhanced small-signal modeling for charge-controlled resonant converters," *IEEE Transactions on Power Electronics*, vol. 37, no. 2, pp. 1736–1747, 2022.
[31] H. Wang, Y. Chen, and Y.-F. Liu, "A passive-impedance-matching concept for multiphase resonant converter," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 2304–2311.
[32] X. Wang, B. Liu, L. Jiang, and Z. Zhan, "Current sharing analysis for novel paralleled clllc converters," *IEEE Access*, vol. 9, pp. 141 307–141 320, 2021.
[33] S. S. Shah, S. Kumar Rastogi, and S. Bhattacharya, "Output plane analyses of llc resonant converter," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 927–934.
[34] S. S. Shah, U. Raheja, and S. Bhattacharya, "Input impedance analyses of charge controlled and frequency controlled llc resonant converter," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 1–5.
[35] R. P. Barcelos, J. Kucka, and D. Dujic, "Power reversal algorithm for resonant direct current transformers for dc networks," *IEEE Access*, vol. 10, pp. 127 117–127 127, 2022.
[36] M. Mogorovic and D. Dujic, "100 kW, 10 kHz medium-frequency transformer design optimization and experimental verification," *IEEE Transactions on Power Electronics*, vol. 34, pp. 1696–1708, 2 2019.
[37] D. Dujic, J. Kucka, G. Ulissi, N. Djekanovic, and R. Barcelos, "Bulk dc-dc conversion for mvdc applications," *TUTORIAL at: EPE'22 ECCE Europe, European Conference on Power Electronics and Applications, Hannover, Germany, September, 5-9, 2022*, 2022. [Online]. Available: http://infoscience.epfl.ch/record/296466

Renan Pillon Barcelos (S'13) received the B.S. degree in electrical engineering from the Federal University of Santa Maria (UFSM), Brazil, in 2018 and M.Sc degrees from the Federal University of Santa Catarina (UFSC), Brazil, in 2020. Since 2021, he is a Doctoral Assistant with the Power Electronics Laboratory at Swiss Federal Institute of Technology Lausanne (EPFL), Switzerland. His research interests include modeling, design, system identification, and stability in the domain of DC power distribution networks with DC transformers.

Drazen Dujic (S'03-M'09-SM'12) received the Dipl.-Ing. and M.Sc. degrees from the University of Novi Sad, Novi Sad, Serbia, in 2002 and 2005, respectively, and the Ph.D. degree from Liverpool John Moores University, Liverpool, U.K., in 2008, all in electrical engineering. From 2002 to 2006, he was with the Department of Electrical Engineering, University of Novi Sad, as a Research Assistant. From 2006 to 2009, he was with Liverpool John Moores University, as a Research Associate. From 2009 to 2013, he was with the ABB Corporate Research Centre, Switzerland, as the Principal Scientist, working on the power electronics projects spanning the range from low-voltage/power SMPS in below kilowatt range to medium voltage high-power converters in a megawatt range. From 2010 to 2011, he was a member of a project team responsible for the development of the world's first power electronic traction transformer successfully commissioned on the locomotive. From 2013 to 2014, he was with ABB Medium Voltage Drives, Turgi, Switzerland, as a Research and Development Platform Manager, responsible for ABB's largest IGCT-based medium voltage drive ACS6000.

He is currently with the École Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, as an Associate Professor and the Director of the Power Electronics Laboratory. He has authored or coauthored more than 200 scientific publications and has filed 20 patents. His current research interests include the areas of design and control of advanced high-power electronics systems for medium voltage applications.

He has received the First Prize Paper Award from the Electric Machines Committee of the IEEE Industrial Electronics Society, in 2007. In 2014, he has received the Isao Takahashi Power Electronics Award for outstanding achievement in power electronics, and in 2018, the EPE Outstanding Service Award from the European Power Electronics and Drives Association. He is an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS.