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Crosstalk Voltage Suppression of SiC MOSFET With An Auxiliary Bidirectional Switch

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***Abstract*—The crosstalk voltage generated by high-speed switching of SiC devices may introduce false turn-on or over-negative gate-source voltage of the power devices. The conventional Miller clamp method is only adopted to minimize the crosstalk voltage introduced by capacitive coupling among the gate-loop and power loop. In light of the capacitive and inductive coupling introduced crosstalk voltage, this paper proposes a highly effective crosstalk voltage suppression circuit considering their effects together. To eliminate the influence of the voltage drop on the coupling inductor between the power loop and gate driving loop, a bidirectional high impedance auxiliary switch is adopted instead of the conventionally adopted Miller clamp circuit when there exists voltage/current step change in the power circuit. Meanwhile, the potential false turn-on of the device is eliminated by a pre-charged negative gate-source voltage. The proposed method is simple and can ensure the safe gate driving voltage window of any fast switching device, independent of the package, temperature and switching speed of the device.**

***Index Terms*—SiC MOSFETs, crosstalk voltage, gate driver**

I. Introduction

As one of the next-generation power devices, SiC MOSFETs are extremely attractive for high voltage, high frequency and high-temperature applications. As with the wide application of SiC MOSFETs, reliability-related issues are drawing more and more attention. Owing to the weakness of the gate-oxide of the device, the gate driving voltage of SiC MOSFETs should be strictly limited within a certain window [1]. In a typical phase leg circuit made of SiC MOSFETs, parasitic elements are unavoidable. These unwanted parameters bring challenges to the application of SiC MOSFETs. Among them, the crosstalk phenomenon, meaning that the gate-source voltage of the off-state device is influenced by the switching of another device, is one of the critical issues in gate driving of SiC MOSFETs. The crosstalk voltage is generated by the capacitive and inductive coupling between the power loop and gate driving loop. The typical parasitic parameters include the device gate-drain capacitor and the common source inductor. It should be pointed out that in some device packages, the auxiliary gate-source terminal is adopted to effectively reduce the coupling inductor. However, the inductive coupling may still be present due to the stray magnetic flux. In some cases, such inductor is even intentionally designed to achieve longer short-circuit withstanding time or the current balance of parallel connected chips [2].

As a consequence, the crosstalk voltage may bring the false turn-on of the device, which causes extra power loss or even thermal runaway of the device. Such phenomenon is well recognized in Silicon devices and the Miller clamp method is widely adopted to avoid the false turn-on of the device [3] [4]. However, the Miller clamp circuit is merely effective in reducing the crosstalk voltage from the gate-drain (gate-collector) capacitors by bypassing the gate resistor with a low-impedance branch [5]. In reality, the crosstalk voltage is introduced by the capacitive coupling and inductive coupling among the gate driving loop and power loop [6]. Miller clamping can't reduce the crosstalk voltage or even increase the gate-source voltage due to the existence of the inductive coupling. In some research, the negative gate-source voltage is generated to suppress the positive crosstalk voltage generated by switching [7] [8]. However, the inductive coupling still can't be fully eliminated. The negative gate-source voltage, together with the potential negative voltage introduced by the inductive coupling, may be lower than the bottom limit of the gate-driving voltage window of SiC devices. To solve the challenge, a high-impedance off-state gate driver solution is proposed in [9]. However, the solution is complex, with multiple isolated independent gate driving signals and extra isolated auxiliary power supplies.

This paper proposes a novel gate driver solution to suppress the crosstalk voltage introduced by the capacitive coupling and the inductive coupling simultaneously. A bidirectional switch with p-MOSFETs is adopted to actively regulate the off-state impedance of the gate-driving loop. Compared with state-of-the-art solutions, the proposed method results in simple circuitry and ease of implementation, independent of the presence of the inductive coupling between the gate loop and power loop.

II. Operation Principles of Proposed Method

In a typical half-bridge circuit, the switching of one device may introduce undesirable voltage in the gate-source voltage of the off-state device, owing to the existence of the coupling between the power loop and gate-loop (gate-drain capacitance C_{gd}, common source inductor L_s). The simplified circuit for the gate-driving loop considering the common source inductance and gate-drain capacitance is shown in Fig. 1. In the off-state of the SiC MOSFET, when $i_{ds} < 0$ and the other

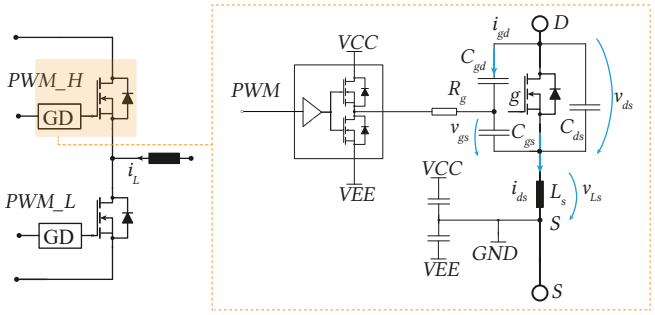


Fig. 1: Simplified equivalent circuit of the gate driver of the power device.

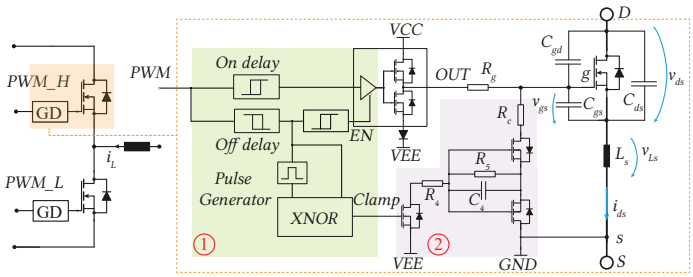


Fig. 2: Structure of the proposed gate driver with crosstalk voltage suppression for one device in a phase leg configuration.

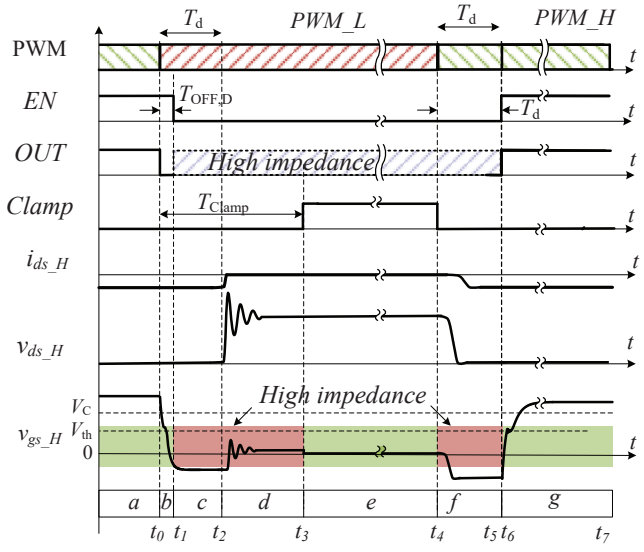


Fig. 3: Time sequence of the operation of the proposed gate driver.

device in the phase leg is turned on or turned off, there will be v_{ds} step-down or step-up across the off-state of the device. The variation of v_{ds} induces a gate-drain displacement current i_{gd}, which is capacitive coupling introduced crosstalk voltage. The smaller the off-state gate driving resistance R_g, the lower the crosstalk voltage will be generated across C_{gs}. In addition, there is another component, namely the voltage drop across L_s owing to the device current i_{ds} step-up or step-down, which is inductive coupling introduced crosstalk voltage. For this coupling, the smaller the off-state resistance R_g, the higher the induced crosstalk voltage. In conclusion, there exist different requirements for R_g for the two types of crosstalk inducted voltage. Conventional methods such as Miller clamping, which reduce the off-state impedance in the gate driving loop, may be incomplete in reducing the crosstalk voltage.

The proposed gate driver structure is given in Fig. 2. To deal with this, apart from the conventional gate-driving current amplifying stage, a logic unit (part 1) is adopted to generate the time sequence of the clamping circuit and a bidirectional switch (part 2) is adopted to adjust the gate-driving loop impedance. In such a configuration, when $Clamp$ signal is high, Capacitor C_4 will be charged by $GND - V_{EE}$ path, result in turn-on of both anti-parallel connected p-MOSFETs. On the contrary, when $Clamp$ signal is low, the charges stored in C_4 will be discharged through R_5, then two p-MOSFETs are turned off.

With the proposed solution, whenever there is a voltage and current change in the power loop, the gate driving loop is in the high impedance, which blocks the gate-source voltage from being influenced by voltage drop on the common source inductor. Since there may be positive or negative voltage drops across the common source inductor, a bidirectional blocking capability switch configuration is adopted. As a result, the induced crosstalk voltage is only influenced by the gate-drain displacement current, or gate-drain voltage change during switching, independent of the switching speed, junction temperature and current [9]. By properly adjusting the gate loop impedance and the gate-source capacitor voltage, the device will be kept in the reliable gate driving window and false turn-on or negative voltage overshoot will be avoided.

Besides, another diode may be required in the negative gate driving stage to avoid the possible reverse current from the negative power supply rail VEE to the output of the gate driving stage OUT, which may happen when the voltage drop across the stray inductor L_s is negative and the absolute value is even higher than $|VEE|$. In the implementation, the diode can also be taken away for packages with small common-source inductance between the gate driving loop and the power loop, such as the package with Kelvin source terminal.

The time sequence of the proposed driving scheme is given in Fig. 3 and in each stage, the equivalent circuit is demonstrated in Fig. 4. In the following section, the operating principle of the gate driver, specifically for the upper device in Fig. 2, is elaborated in detail.

Before t_0: the upper device in a phase leg is in the on-state. $PWM\_H = 1, PWM\_L = 0$ is the driving signal from the controller. The equivalent circuit of the upper gate driver is demonstrated in Fig. 4(a). In this example, the drain-source current of the upper device is negative so that when the lower device is turned on, there will be gate-drain voltage toggle in the upper device.

$t_0 - t_1$: PWM_H switches to zero. The equivalent circuit

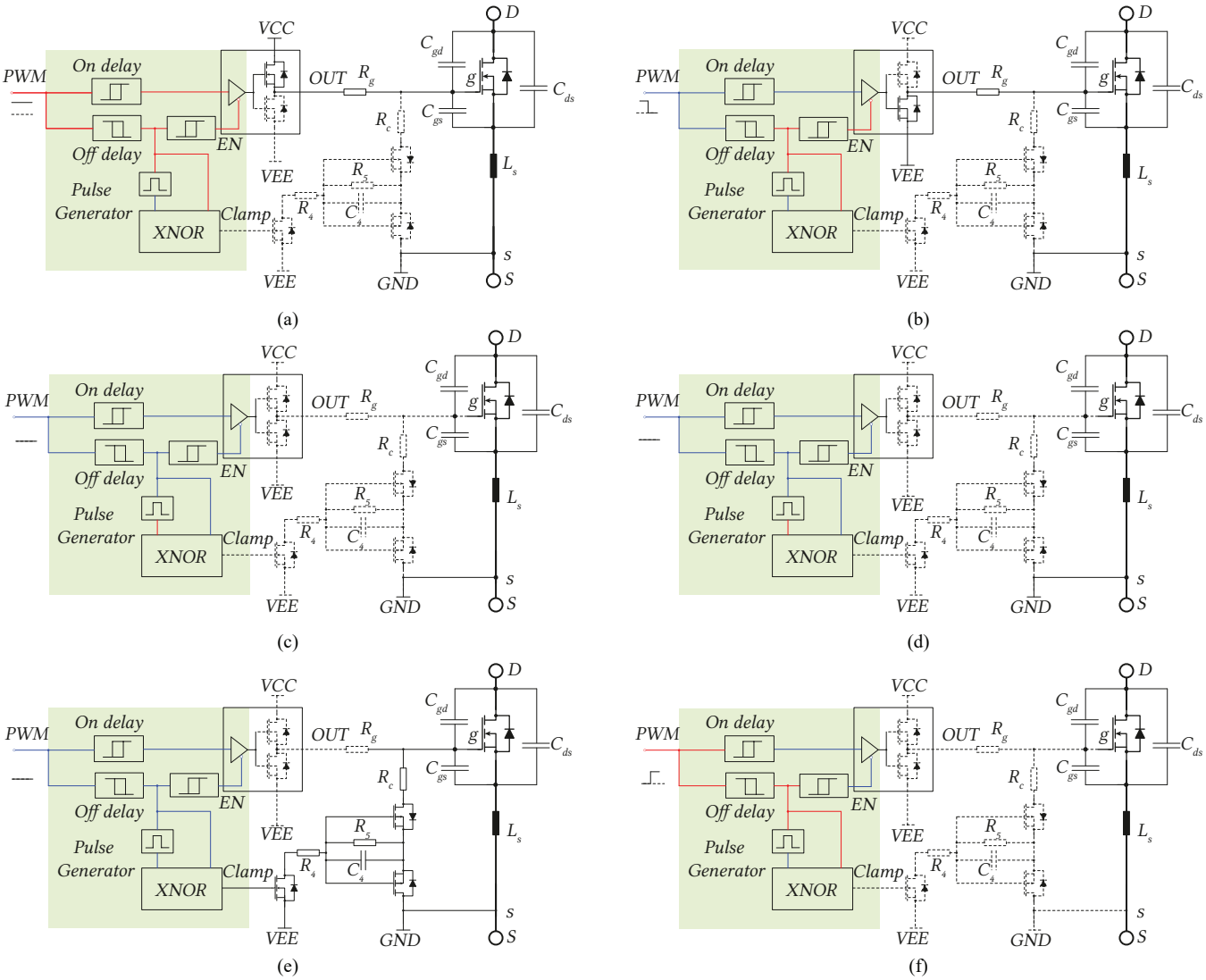


Fig. 4: Equivalent circuit at different stages of the time sequence. Blue line means the signal is in low state, red line means the signal is in high state.

in this stage is demonstrated in Fig. 4(b). The OUT of the gate driving stage will be connected to VEE immediately. The gate-source voltage starts to decrease. After a short delay time, $T_{OFF,D}$, the enable signal of the gate driver circuit EN is disabled. The duration of the $T_{OFF,D}$ is slightly longer than the turn-off time of the device. At t_1, the gate-source voltage is VEE. The negative voltage is kept on the device gate-source capacitor to prevent the false turn-on of the device when the lower device is turned on.

$t_1 - t_2$: When EN is in the low state, OUT is in the high impedance state. And the clamp switch remains in off-state. As a result, as demonstrated in Fig. 4(c), the gate driving loop of the device is in the high impedance state. At t_2, the lower device is turned on after the deadtime T_d ends.

$t_2 - t_3$: At t_2, the lower device is turned on. The equivalent circuit is demonstrated in Fig. 4(d). Since the output current of the phase leg is negative, the voltage of the upper device increases rapidly. There will be a displacement current from the gate-drain capacitor of the upper device. Meanwhile, since the gate loop is in the high impedance state, the influence of current variation in the power loop is isolated. The only concern is the crosstalk voltage introduced from the gate-drain capacitor. By selecting the proper value of the negative gate-source voltage, the device will remain in the off-state although there is a voltage step up on the gate-source capacitor. The value of VEE depends on the ratio between the gate-drain capacitor and the gate-source capacitor C_{gd}/C_{gs}. Fortunately, nowadays, there is a general trend to design the device with lower ratio of C_{gd}/C_{gs}. The required VEE can be in the reliable gate driving voltage window for most of the devices [9]. The duration of $t_0 - t_3$ T_{Clamp} is generated by the pulse generator in Fig. 2. It can be the commercially available monostable pulse generator triggered by the step down of

PWM_H. T_{Clamp} should meet the requirement as follows

$$T_{Clamp} > T_d + T_{on} \tag{1}$$

where T_d is the dead-time; T_{on} is the turn-on time of the lower device. In extreme cases, the duty cycle is too low so that *PWM_L* is switched to zero even before the stage $t_1 - t_3$ is finished. In this case, the $Clamp$ signal will be automatically ignored for the off-state device.

$t_3 - t_4$: When the lower device is completely turned on, the clamping switch of the upper gate driver will be turned on to clamp the gate-source voltage to zero, as demonstrated in Fig. 4(e), to avoid floating gate-source capacitor during the off-state of the device.

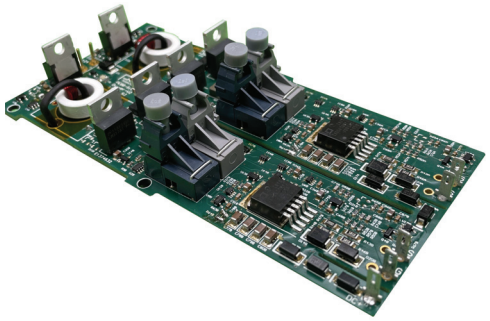
$t_4 - t_5$: At t_4, the lower device is turned off and the upper device PWM_H will be in the high state. Different from the conventional solution, the input signal of the upper device PWM_H is switched to the high state immediately, without any blanking time from the controller side. Instead, to avoid the shoot-through of the dc-link, the dead-time, which is the turn-on delay of the power device, is inserted locally in EN to disable the gate driving output. The equivalent circuit is the same as Fig. 4(e). When the lower device is completely off, the gate loop of the lower device remains in the high impedance state. After the inserted dead-time, the upper device will be turned on. Thus, the drain-source voltage of the upper device is decreased from the dc-link voltage to zero. As a result, the gate-source voltage of the lower device is reduced to the negative value. The current change in the power loop has little influence on the induced crosstalk voltage.

After t_5: The upper device will be turned on and the equivalent circuit is the same as Fig. 4(a).

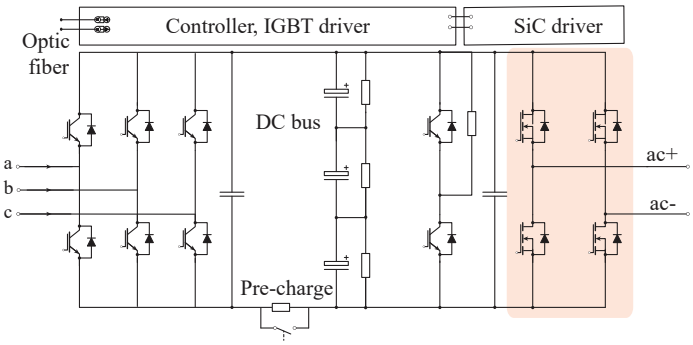
In the proposed method, all the control signals, including EN, $Clamp$, OUT, are generated with the fixed shift to the PWM input of the gate driver. Therefore, no extra control signal from the central controller is required, which reduces the complexity of the solution.

III. Experimental Verification

To verify the proposed solution, a gate driver with adjustable gate-driving loop impedance is realized. The gate driver is targeted for $1.7\,\mathrm{kV}$ and $225\,\mathrm{A}$ power module. The photo of the gate driver is shown in Fig. 5a and a three-phase converter rated $67\,\mathrm{kW}$ with $1.2\,\mathrm{kV}$ is designed,utilizing two of these dual gate drivers, as shown in Fig. 5b and Fig. 5c. In the experiments, the dead-time T_d is selected as $1\,\mu\mathrm{s}$. The EN signal delay time is $T_{OFF,D} = 40\,\mathrm{ns}$. The double pulse test waveform is given in Fig. 6. In general, the gate-source voltage is three-level shape. When the device is turned off, the gate-source voltage is clamped to the negative voltage, $-6.0\,\mathrm{V}$ in the experiments. The proposed gate driver works fine under double pulse test conditions and the introduced crosstalk voltage is within $[-6.0\,\mathrm{V}, 4\,\mathrm{V}]$ at $1.2\,\mathrm{kV}$ / $250\,\mathrm{A}$ switching. It should be pointed out that the actual gate-source voltage of the device is difficult to measure from the terminal since there exists parasitic inductance and internal device



(a)



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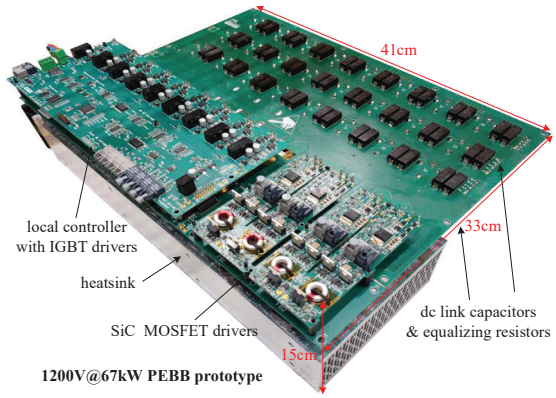

(c)

Fig. 5: (a) Photo of the gate driver; (b) Topology of the test platform; (b) Photo of the 1.2kV/67kW experimental setup.

resistance. However, it can be judged from the device drain-source current that there is no false turn-on of the device, even the measured peak voltage waveform is higher than the threshold voltage of the device.

To explore the performance of the proposed gate driver under different voltage and current conditions, a series of experiments are conducted at different lengths of pulses from $5\,\mu\mathrm{s}$ to $20\,\mu\mathrm{s}$ and different dc link voltages from $200\,\mathrm{V}$ to $1200\,\mathrm{V}$. The results are demonstrated in Fig. 7. It can be seen that, at different dc-link voltages, the induced crosstalk voltage increase with dc bus voltage, which is the result of the

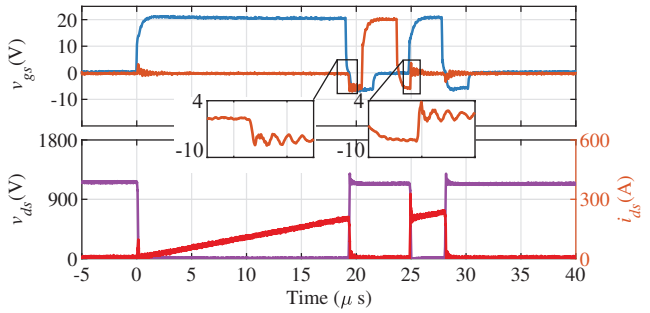

Fig. 6: The waveforms at 1.2 kV/250 A double pulse test.The upper device is active switching. Lower device gate-source voltage is interfered by the switching.

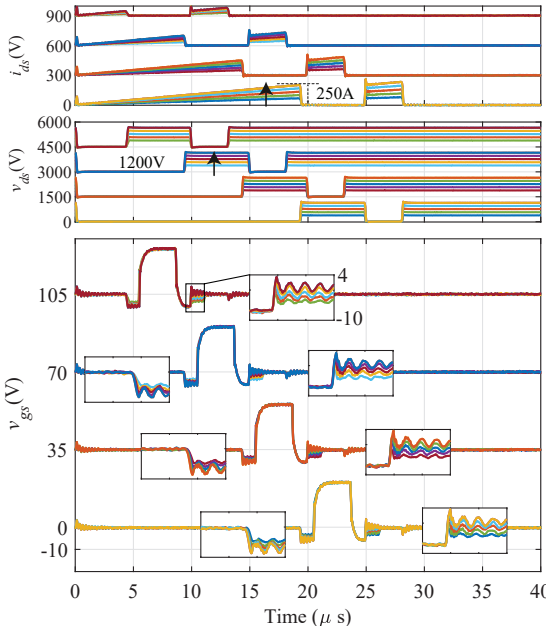

Fig. 7: Crosstalk voltage at different voltage and current levels.

increased gate-drain charge stored in the gate-drain capacitor. However, at the same dc-link voltage, the crosstalk voltage is almost the same at different switching currents. Under any voltage and current points, the off-state gate-source voltage is within the proper range.

As mentioned before, the proposed method is not influenced by the common source inductance. In the experimental power module, the auxiliary source terminal exists and common source inductance is relatively small. In the test, the power source terminal of the module is connected to the negative output of the gate driver, instead of the auxiliary source terminal, resulting in extra 2 nH leakage inductance inserted, as demonstrated in Fig. 8. The results are demonstrated in Fig. 9. It can be seen that even there exists a piece of common source inductance in the gate driving loop, the actual gate-source voltage is still not influenced. To go further, in the proposed method, since a piece of the common source inductor exists in the gate loop, it is beneficial for prolonging the device

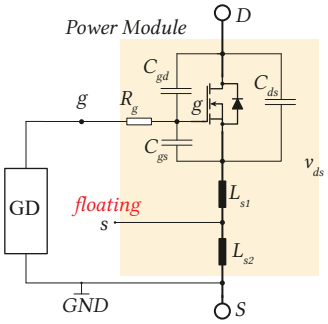

Fig. 8: A piece of common source inductor is inserted into the gate-driving loop.

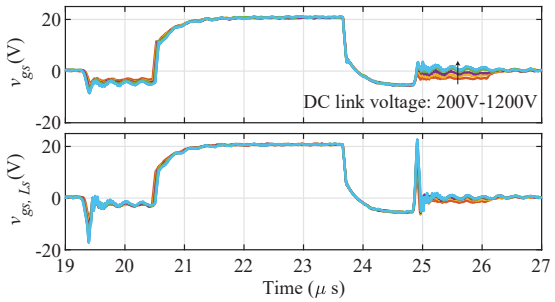

Fig. 9: The waveform of the gate-source voltage under different common source inductance at dc link voltage from 200 V to 1200 V. The upper figure is the measured gate-source voltage. Lower figure is the measured gate-source voltage plus the voltage drop on the L_s. With the proposed method, the influence of L_s can't be observed from the measured gate-source voltage.

short-circuit withstanding time.

To further verify the reliability of the proposed gate driving method, the gate driver under continuous switching is tested, as demonstrated in Fig. 10. The results at 1.0 kV, 100 Arms and 20 kHz are demonstrated. The results verify that the

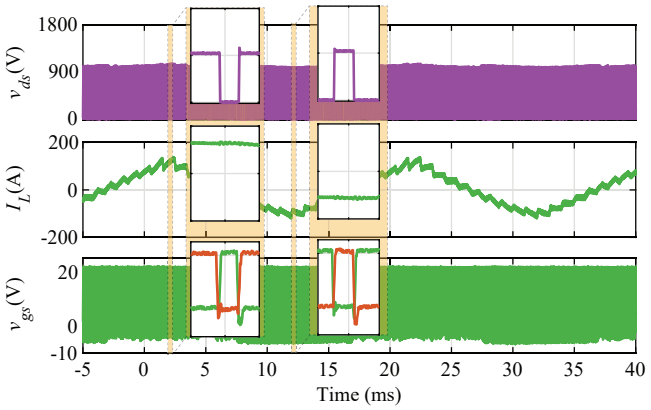

Fig. 10: The waveform of the gate-source voltage at steady state continuous operation. The gate driver is tested at 1.0 kV, 100 ARMS and 20 kHz

proposed gate driver can effectively operate in continuous switching conditions without false activation of protection circuitry. The gate-source voltage is always within the proper range at different currents.

IV. Conclusion

In this paper, a simple circuit for crosstalk voltage suppression of SiC MOSFET is proposed to eliminate the influence of drain-source capacitor and common source inductor introduced crosstalk voltage simultaneously. With the proposed method, the induced crosstalk voltage is merely introduced by the gate-drain capacitor, which is well predictable from the device parameter and independent of the switching speed, the junction temperature, and the device current. The proposed method successfully reduces the crosstalk voltage regardless of the package of the device, which is a general solution without adding too much complexity compared with the existing gate drivers. With the proposed solution, the source inductance can even be introduced to increase the short-circuit withstanding time of the SiC MOSFETs.

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