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Second Harmonic Ripple Voltage Suppression for Single-Phase ISOP Solid-State Transformer by Active Power Decoupling

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***Abstract*—The solid-state transformers with input-series output-parallel structure are considered for various applications where MVAC to LVDC conversion is needed. However, due to the inherent second harmonic pulsating power in the single-phase AC system, large DC link capacitors are required to smooth the voltage ripple of all floating cells, which reduces achievable power density. The active power decoupling method can shift away the pulsating power from the DC link capacitors, leading to a significant reduction to the DC link capacitance and resulting voltage ripple. So far, the application of active power decoupling is limited to single-level converters, and little research on the impact in modular converters has been done. This paper investigates the feasibility of applying active power decoupling to solid-state transformers. The active power filter with dc-split-capacitor circuit is selected to minimize the DC link capacitance. Simulation results show that the active power filter can significantly reduce the second harmonic voltage ripple and the total DC link capacitance of the SST. A prototype of the active power filter has been built and tested to verify the design.**

***Index Terms*—active power decupling, active power filter, solid-state transformer, input-series output-parallel, second harmonic ripple voltage suppression**

I. Introduction

Solid-state transformer (SST) is an emerging technology that could make an extraordinary impact in many areas such as traction systems, smart-grids, data center and renewable energy sources [1]–[9]. The MVAC to LVDC conversion is one of the typical applications of SST. Due to the high input voltage, many SST prototypes adopted the input-series output-parallel (ISOP) structure.

As shown in Figure 1, the ISOP SST contains several cells, which are made up of an AC/DC converter, a DC/DC converter with MV galvanic isolation and DC link capacitors on both MV and LV sides. The cells are connected in series at their MV terminals and in parallel at their LV terminals, which realized the high step-down AC to DC conversion. In the ISOP structure, the input voltage rating can be easily expanded and each cell's power rating is greatly reduced.

In single-phase AC/DC converters, the instantaneous power from the AC side contains not only a DC component but also a pulsating component at twice the AC line frequency. This

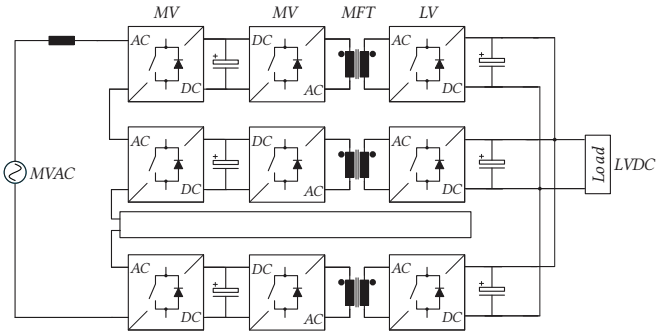

Fig. 1: Solid-state transformer with input-series output-parallel structure.

pulsating power will cause the second harmonic ripple voltage on the DC link, which affects the operation of the converter. The ISOP SST also suffers from the same problem, which leads to the second harmonic ripple voltage on the MV side DC links. The pulsating power could be propagated through the DC/DC converters to the LV side and influence the output voltage quality as well [10]. The ripple voltage also exists in three-phase ISOP SST, as it usually adopts phase separation configuration where three identical single-phase ISOP SSTs process the three-phase power independently. Although the ripple voltage on the LV side DC link is neutralized, a considerable ripple voltage still exists in the MV side DC links.

As passive harmonic suppression methods, a bulk DC link capacitor is usually installed to buffer the pulsating power. Most of the ISOP SST adopted this solution, which leads to low power density of employed power stages. The LC trap filter is another passive solution, which provides a selective low impedance path for the second harmonic current [11]. However, the volume and weight of the passive components are considerable, as the resonant frequency of the LC branch is very low.

Several control methods have been proposed for harmonic suppression in three-phase ISOP SST. Considering the ripple voltage on the LV side DC link will be canceled, one solution

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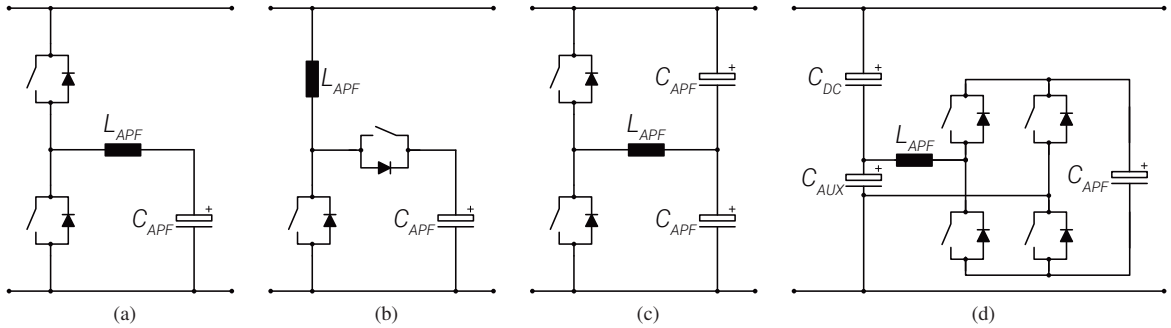

Fig. 2: Typical topologies of active power filters: a) buck-type b) boost-type c) dc-split-capacitor d) stacked capacitor

is to transfer the pulsating power from the MV side to the LV side by controlling the power flow of the DC/DC converter, and the MV side DC link capacitance can be significantly reduced [12]–[14]. The third-harmonic voltage injection method has been widely employed in cascaded H-bridge (CHB) converter to reduce the second harmonic ripple voltage [15], [16], and this method can also be applied to ISOP SST [17].

Unfortunately, the above mentioned methods are no longer valid for single-phase ISOP SST. The capacitors installed in the SST need to be large enough to cope with the full pulsating power from the AC source. In this case, the active power decoupling (APD) method becomes an attractive solution for the second harmonic ripple suppression [18]. When APD is applied, the pulsating power is shifted away from the DC link capacitor and stored by separate components. As a result, the pulsating power is buffered in a more efficient and reliable way.

So far, the application of APD is limited to single-level converters and little research of APD for multi-level converters has been done. Several active power filters (APF) are shown in Figure 2 [19]. A buck-type APF, as shown in Figure 2a, is analyzed in [20]. The minimum required energy storage capacitance of this topology is $C_{min\_Buck} = 2P_r/(\omega U_{DC}^2)$, and P_r is the amplitude of the pulsating power. It is worth noting that a much smaller DC link capacitor is still required to filter out the ripple voltage at the switching frequency of the converter.

A similar APF topology based on boost converter as shown in Figure 2b is analyzed in [21]. However it is excluded from further analysis in this paper as the voltage rating of switching devices and capacitors in this topology need to be higher than the DC link voltage [22].

An APF with dc-split-capacitor circuit as shown in Figure 2c is analyzed in [23]. Two identical capacitors are connected in series to form the DC link capacitor. The midpoint of these two capacitors is connected to a half-bridge circuit through an inductor. The advantage of this topology is that the APF capacitors also contribute to the overall DC link capacitor while buffering the pulsating power. The smallest total capacitance of this topology is $C_{min\_Split} = 8P_r/(\omega U_{DC}^2)$ [24].

An APF with stacked capacitor as shown in Figure 2d, where the APF is connected in series to the DC link capacitor, is proposed in [25]. Although the voltage rating of the APF is greatly reduced, four switching devices are required which leads to higher complexity.

All of the above-mentioned APF topologies can be applied to ISOP SST. When the buck-type APF operates with the minimum required capacitance C_{min_Buck}, the APF capacitor is fully discharged and its voltage reference signal contains sharp turns which are difficult for the controller to track [19], [26]. Increasing energy storage flattens the reference signal but reduces power density. In contrast, the APF with dc-split-capacitor circuit requires a much simpler controller as the voltage of APF capacitor is sinusoidal. The minimum capacitance C_{min_Split} is higher than the buck-type APF, but can be adopted directly without any margin. Therefore the APF with dc-split-capacitor circuit is selected for further analysis.

II. Second Harmonic Pulsating Power in SST

The second harmonic pulsating power in the ISOP SST can be derived from the grid voltage, current and parameters of the grid filter [20]. Figure 3 shows the topology and power flow of a ISOP SST without APD. Assuming the AC voltage u_{ac} and current i_{ac} are sinusoidal, the instantaneous power from

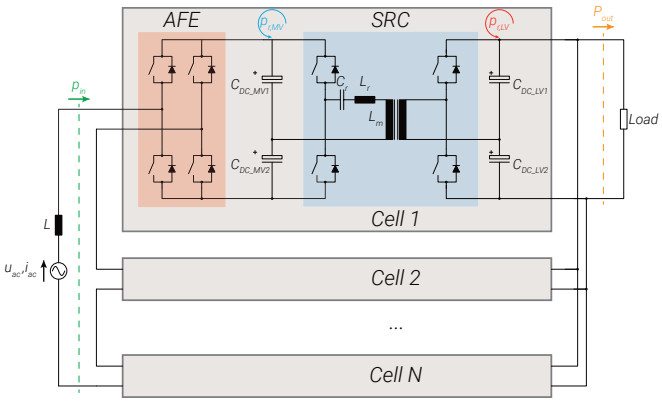

Fig. 3: The topology and power flow of a ISOP SST using SRC as the DC/DC converter.

the AC grid can be expressed as follows:

$$\begin{aligned} p_{ac} &= u_{ac} i_{ac} = U_{ac} \sin(\omega t) I_{ac} \sin(\omega t - \phi) \\ &= \frac{U_{ac} I_{ac}}{2} \cos\phi - \frac{U_{ac} I_{ac}}{2} \cos(2\omega t - \phi) \end{aligned} \tag{1}$$

where U_{ac} and I_{ac} are the amplitude of the grid voltage and current, respectively; ϕ is the angle between the voltage and current; while ω is the frequency of the grid.

Assuming an L filter is adopted, the reactive power of inductor L is:

$$\begin{aligned} p_L &= L \frac{di_{ac}}{dt} i_{ac} = \omega L I_{ac}^2 \sin(\omega t - \phi) \cos(\omega t - \phi) \\ &= \frac{\omega L I_{ac}^2}{2} \sin(2\omega t - 2\phi) \end{aligned} \tag{2}$$

By ignoring the losses of the converter, the input power of the SST can be expressed as:

$$\begin{aligned} p_{in} = p_{ac} - p_L = P_{out} + p_r = \frac{U_{ac} I_{ac}}{2} \cos\phi \\ - \left(\frac{U_{ac} I_{ac}}{2} \cos(2\omega t - \phi) + \frac{\omega L I_{ac}^2}{2} \sin(2\omega t - 2\phi) \right) \end{aligned} \tag{3}$$

(3) shows that the input instantaneous power of the SST consists of a constant power P_{out} and a pulsating power p_r.

$$\begin{aligned} P_{out} &= \frac{U_{ac} I_{ac}}{2} \cos\phi \\ p_r &= -\frac{U_{ac} I_{ac}}{2} \cos(2\omega t - \phi) - \frac{\omega L I_{ac}^2}{2} \sin(2\omega t - 2\phi) \end{aligned} \tag{4}$$

The amplitude of the pulsating power is:

$$P_{r,max} = \sqrt{P_{out}^2 + \left(\frac{2\omega L P_{out}^2}{U_{ac}^2 \cos^2\phi} - \frac{P_{out} \sin\phi}{\cos\phi} \right)^2} \tag{5}$$

P_{out} is the power which will be feed to the DC side. p_r is second harmonic pulsating power, which is the cause of the second harmonic voltage ripple on the DC link. During normal operations, the power flow of the entire SST is evenly distributed into every cell. Each portion of the power is fed into the cell by the active front-end (AFE) converter, and the pulsating component of the power will introduce second harmonic voltage ripple on the MV side DC link. If the isolated DC/DC conversion is realized by a dual active bridge (DAB) converter, the power flow and the second harmonic voltage ripple on the LV side DC link can be controlled as demonstrated in [13]. The series resonant converter (SRC) operating at a fixed frequency is another promising choice for SST as it provides isolation and reduced switching losses. Unlike DAB, SRC provides a fixed voltage transfer ratio when operating at the resonant frequency. Although this reduces the complexity of control, it also causes the second harmonic ripple voltage on the MV side to be inevitably propagated to the LV side.

As the DC link capacitance is usually much larger than the resonant capacitance in the SRC, it can be approximated that

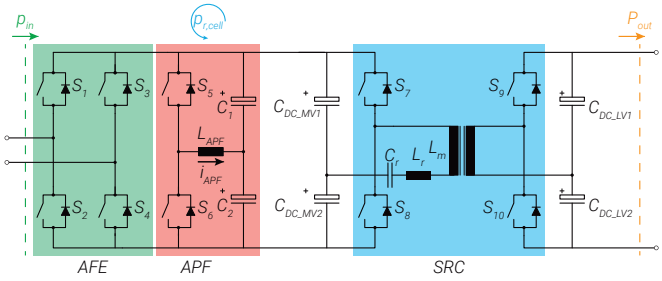

Fig. 4: Modified SST cell with APF installed.

the all pulsating power is stored in the DC link capacitor, which can be expressed as:

$$p_r = p_{r,cell} N_{cells} = (p_{r,MV} + p_{r,LV}) N_{cells} \tag{6}$$

where $p_{r,cell}$ is the pulsating power of each cell, $p_{r,MV}$ and $p_{r,LV}$ are the pulsating power stored in the MV and LV side DC link capacitors, respectively; N_{cells} is the number of cells in the SST. To cope with this pulsating power by bulky capacitor, the required DC link capacitance can be calculated as:

$$C_{DC} = \frac{P_{r,max}}{\omega U_{DC} \Delta U_{DC}} \tag{7}$$

where ΔU_{DC} is amplitude of the voltage ripple. Since $\Delta U_{DC} \ll U_{DC}$, only a small fraction of the capacitor energy storage is utilized to suppress the voltage ripple.

Figure 4 shows the modified SST cell with APF installed. The APF is installed on the MV side DC link of the SST cell. All of the pulsating power is stored in the APF and the power decoupling is achieved. A much smaller DC link capacitor is still required to filter out the voltage ripple at the switching frequency of AFE and SRC.

Figure 5 shows the hardware platform used in this paper, which is the LV prototype of the power electronic traction

Fig. 5: The LV PETT prototype, which serves as SST research platform for the works presented in this paper.

transformer (PETT) [6]. The LV PETT adopts the ISOP structure with nine cells composed of an H-bridge AFE converter and an SRC converter. Due to the constraint of laboratory infrastructure, the power rating of the test platform is limited to 8kW. Accordingly, the rating of each APF is set to 1kVA. This paper presents the design and test results of a single APF. To evaluate the performance of APD method, nine APFs will be installed into the nine cells respectively, and the final results will be reported separately.

III. Design of the APF for ISOP SST

A. Operating Principles of the APF

Figure 4 shows the diagram of an ISOP SST cell using APF with dc-split-capacitor circuit [23]. Two identical capacitors C_1 and C_2 are connected in series to absorb ripple energy and support DC link, where $C_1 = C_2 = C_{APF}$. The DC voltage controller of the AC/DC converter will maintain the sum of the two capacitor voltages as U_{DC}. To compensate second harmonic pulsating power, the voltage of C_1 and C_2 are controlled to be sinusoidal with an offset:

$$\begin{aligned} u_{C1} &= \frac{U_{DC}}{2} + U_{APF}\sin(\omega t + \theta) \\ u_{C2} &= \frac{U_{DC}}{2} - U_{APF}\sin(\omega t + \theta) \end{aligned} \tag{8}$$

The capacitor voltage should be always above zero, which means $U_{APF} < U_{DC}/2$. The capacitor current can be calculated as:

$$\begin{aligned} i_{C1} &= \omega C_{APF} U_{APF}\cos(\omega t + \theta) \\ i_{C2} &= -\omega C_{APF} U_{APF}\cos(\omega t + \theta) \end{aligned} \tag{9}$$

The instantaneous power generated by C_1 and C_2 is:

$$p_C = u_{C1} i_{C1} + u_{C2} i_{C2} \tag{10}$$

$$= \omega C_{APF} U_{APF}^2 \sin(2\omega t + 2\theta) \tag{11}$$

The instantaneous power of the inductor L_{APF} is:

$$\begin{aligned} p_L &= L_{APF}\frac{di_{APF}}{dt} i_{APF} \\ &= -2\omega L_{APF}(\omega C_{APF} U_{APF})^2 \sin(2\omega t + 2\theta) \end{aligned} \tag{12}$$

The total instantaneous power generated by the APF is:

$$\begin{aligned} p_{APF} &= p_C + p_L \\ &= [\omega C_{APF} U_{APF}^2 - 2\omega L_{APF}(\omega C_{APF} U_{APF})^2] \\ &\quad \sin(2\omega t + 2\theta) \end{aligned} \tag{13}$$

To achieve a proper harmonic suppression, the instantaneous power provided by the APF should be the same as the ripple energy $p_{r,cell}$ in (6). By equating the time-varying terms of (4) and (13), U_{APF} and θ can be calculated as:

$$\begin{aligned} U_{APF} &= \sqrt{\frac{P_{r,max}}{(\omega C_{APF} - 2\omega L_{APF}(\omega C_{APF})^2) N_{cells}}} \\ \theta &= -\phi + \frac{\psi}{2} \\ \psi &= \arctan\frac{P_{out}}{\frac{2\omega L P_{out}^2}{U_{ac}^2\cos^2\phi} - \frac{P_{out}\sin\phi}{\cos\phi}} \end{aligned} \tag{14}$$

$P_{r,max}$ is the amplitude of the pulsating power; ψ reflects the influence of the grid filter on the phase of the second harmonic pulsating power.

B. Parameter Design of the APF

When calculating the required C_{APF}, the inductor L_{APF} in (14) is negligible and U_{APF} can be approximated as:

$$U_{APF} \approx \sqrt{\frac{P_{r,max}}{\omega C_{APF}}} \tag{15}$$

Considering $U_{APF} < \frac{U_{DC}}{2}$, following can be obtained:

$$C_{APF} > \frac{4P_{r,max}}{\omega U_{DC}^2} \tag{16}$$

The rating of the APF P_{APF} is determined as 1kVA. According to (16), the minimum value of C_{APF} is calculated as:

$$C_{APF\_min} = \frac{4P_{APF}}{\omega U_{DC}^2} = 203\mu\text{F} \tag{17}$$

The switching frequency ripple on the MV side DC link capacitor is also considerable as the AFE is operating at a low frequency. To limit the switching frequency ripple within 15V, the required DC link capacitance is approximated as [27]:

$$C_{DC\_min} = \frac{P_{APF}}{4 f_{AFE} U_{DC} \Delta U_{DC}} = 190\mu\text{F} \tag{18}$$

Result shows that a supplementary DC link capacitor is still required, even though half of C_{APF} will contribute to the total DC link capacitance.

Inductor L_{APF} should be large enough to limit the ripple of i_{APF} within desired level. However, (13) shows that the inductor L_{APF} should be minimized as it reduces the ripple energy compensation capability of the APF. The value of L_{APF} is determined to be 200μH, and the maximum current ripple is limited within 50% at 20kHz switching frequency.

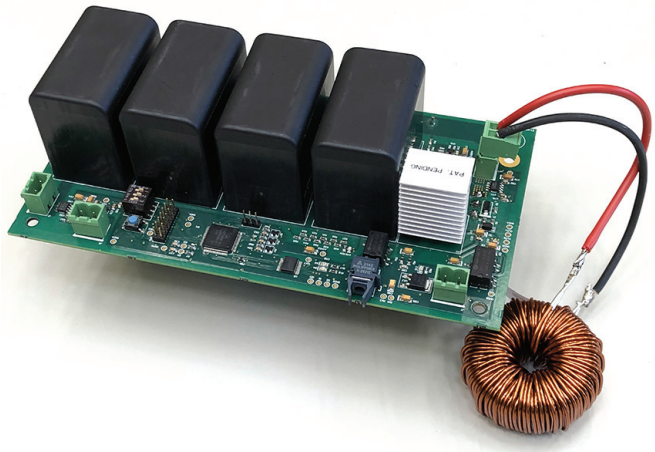

Fig. 6: The 1kVA APF prototype. The dimension of the shown APF prototype is 200mm × 107mm × 102mm.

TABLE I: Key components of the APF prototype

Components	Description
Switch S_5 and S_6	Infineon IMW65R039M1H, 35A/650V
Capacitor C_1 and C_2	3 × Vishay MKT1820712255, 120µF/250V
Inductor L_{APF}	60 Turns, Magnetics 58716, 2 × AWG15

Based on above analysis, a 1kVA APF prototype is build, which is shown in Figure 6. The key components selection of the APF is given in Table I.

C. Control Method of the APF

Figure 7 shows the control structure of the APF. The MV side DC link voltage contains considerable ripple voltage at the switching frequency of AFE and SRC, which introduces common mode interference to u_{C1} and u_{C2}. To eliminate the disturbance from the DC link voltage, an intermediate variable u_Δ is introduced:

$$u_\Delta = u_{C1} - u_{C2} = u_{DC} - 2u_{C2} \tag{19}$$

Since u_Δ is the difference between the top and bottom capacitor voltage, the common mode voltage is canceled. u_Δ is sinusoidal wave without DC bias, and reflects only the second harmonic pulsating power generated by the APF. A closed-loop control is implemented on u_Δ, and a proportional resonant (PR) controller is adopted. The resonant term at the grid frequency guarantees a zero steady-state error when tracking the sinusoidal reference u_Δ^*. A constant 0.5 is added to the duty cycle to maintain the $U_{DC}/2$ offset of the capacitor voltages. The voltage reference of the APF in the above-mentioned control method can be calculated based on (14).

IV. Simulation and Experiments

A. Simulation Results

To evaluate the performance of the APF, the simulation model of the LV PETT with APF is built in PLECS, and the parameters are given in Table II. As shown in Figure 4, additional DC link capacitor C_{DC_MV1} and C_{DC_MV2} are installed to filter the switching frequency ripple and provide a stable neutral point voltage for the SRC. Instead of individual LV side DC link capacitors in each cell, two 2mF capacitor C_{DC_LV} are installed in the common LV side DC link. The total installed capacitor is 8mF.

Figure 8 shows the simulation result of the LV PETT with APF. Before the APF is enabled, the LV side DC link voltage has a 35V voltage ripple. At t=0.1s, the APF is enabled. After 0.4s, the system reaches a steady state and the LV

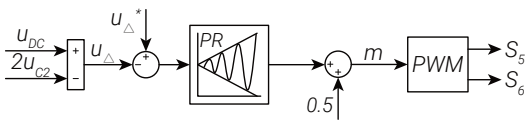

Fig. 7: Control principle of the APF with dc-split-capacitor circuit

TABLE II: Parameters of the ISOP SST and APF

Parameters	Value
Rated Power P_{out}	8kW
Line Voltage U_{AC}	800V
Line Frequency f_{AC}	50Hz
Line Inductor L	25mH
DC Link Voltage U_{DC}	250V
Number of Cells N_{cells}	9
MV side DC link capacitor C_{DC_MV}	120µF
LV side DC link capacitor C_{DC_LV}	2mF
Switching Frequency of AFE f_{AFE}	350Hz
Switching Frequency of SRC f_{SRC}	1500Hz
APF Capacitor C_{APF}	360µF
APF Inductor L_{APF}	200µH
Switching Frequency of APF f_{APF}	20kHz

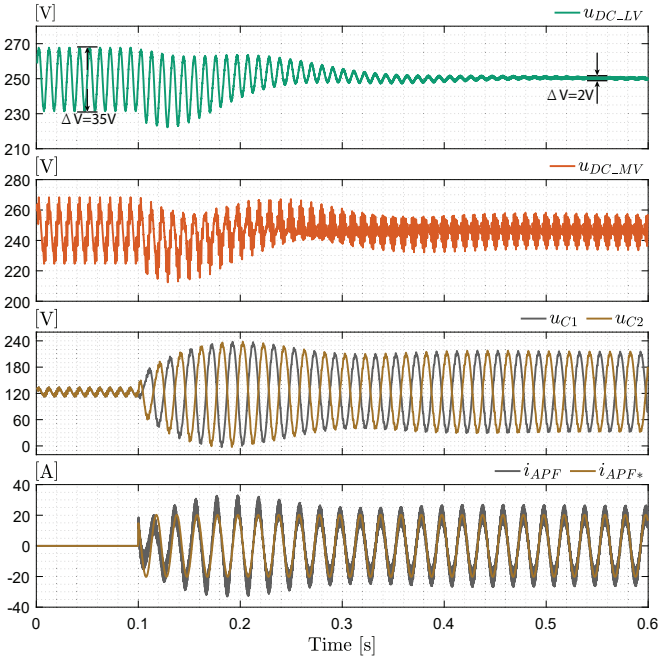

Fig. 8: Simulation waveform of LV PETT with APF.

side DC voltage ripple is reduced to less than 2V. The MV side DC link voltage still contains a considerable 25V ripple voltage at f_{AFE}, but it will not be propagated to the LV side due to the phase shift operation of AFE. The voltage of the capacitor C_1 and C_2 oscillates between 35V and 215V, while the current ripple of L_{APF} is limited to 50%. As a comparison, to achieve such a low voltage ripple without APF, the required capacitance can be calculated as:

$$C_{Bulk} = \frac{P_{r,max}}{\omega U_{DC} \Delta U_{DC}} = 51\text{mF} \tag{20}$$

B. Experimental Results

A 1kVA prototype is built to verify the ripple voltage suppression capability of the APF. Figure 6 shows the photo of the prototype and its parameters are given in Table I. Two 360µF capacitors, which are composed of three 120µF capacitors, are connected in series. Two 120µF capacitors are added

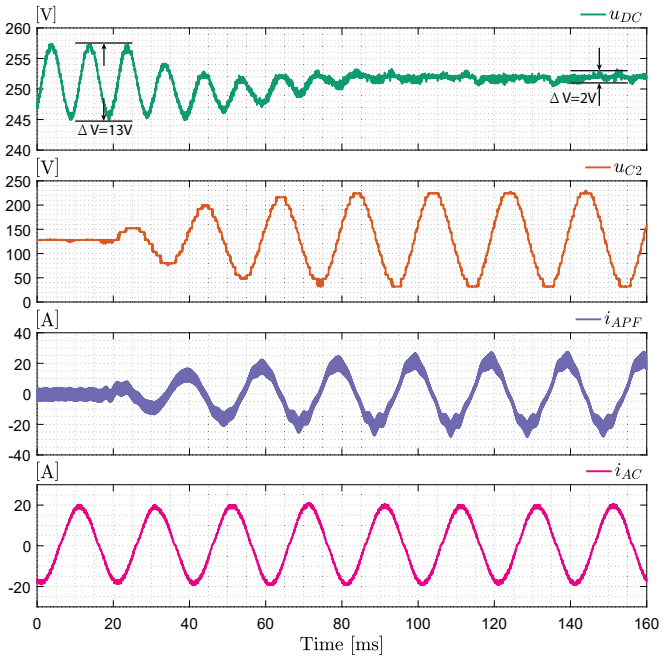

Fig. 9: Transient of the system when APF is enabled at t=20ms

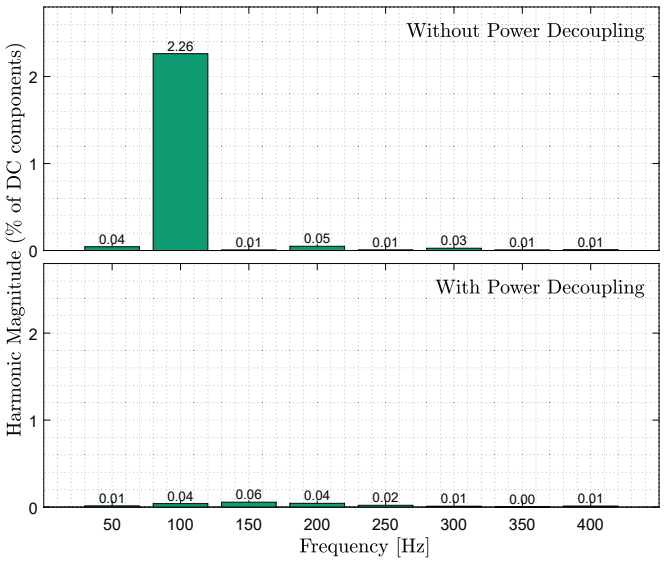

Fig. 10: FFT analysis of the output DC voltage

as additional DC link capacitor to cope with the switching frequency ripple. To verify the design of the APF before the final implementation on the overall SST, the prototype has been experimentally tested with an external AC/DC rectifier and an ohmic-inductive load. The AC/DC rectifier has $1.1\mathrm{mF}$ DC link capacitance, and its DC outpit is connected to the APF. The rectifier operates at 5kHz and provides a 250V DC link voltage with second harmonic ripple voltage, which is expected to be suppressed by the APF.

Figure 9 shows the transient of the system when APF is

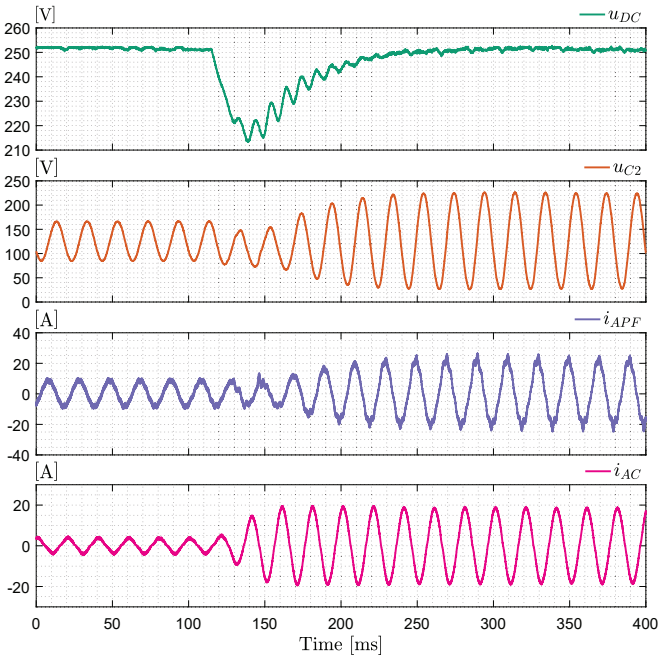

Fig. 11: Transient response of the APF during a load step from 200W to 1kW

enabled. In the first 20ms, the APF controller is disabled and the AC/DC rectifier is operating at 1kW. Due to the low DC link capacitance in the system, the amplitude of second harmonic voltage ripple reaches 13V. At t=20ms, the APF is enabled and the second harmonic voltage ripple is significantly reduced. A 2V residual voltage ripple is observed due to the control error and mismatch of parameters. Figure 10 gives the FFT analysis of the output DC voltage. Same calculation as (20), the DC link capacitance of the AC/DC rectifier needs to be increased from $1.1\mathrm{mF}$ to $6\mathrm{mF}$, in order to achieve such a low ripple voltage without APF.

Figure 11 and 12 shows the transient response of the APF during a load step from 200W to 1kW and a voltage step from 220V to 250V, respectively. The DC link voltage is regulated by the external AC/DC rectifier, while the APF can always suppress the second harmonic voltage ripple under different conditions. The test results show that the developed APF prototype can give satisfactory results on the suppression of the second-harmonic ripple.

V. Conclusion

This paper investigates the feasibility of applying APD technology in ISOP SST to suppress the second harmonic voltage ripple on the DC link capacitor. The APF with dc-split-capacitor circuit is selected. The second harmonic pulsating power flow in the SST is analyzed, and a modified ISOP SST cell with APF installed is given. The operating principle, parameter design and control method of the APF are demonstrated. Simulation result shows that the APF can greatly reduce the second harmonic ripple voltage and the total

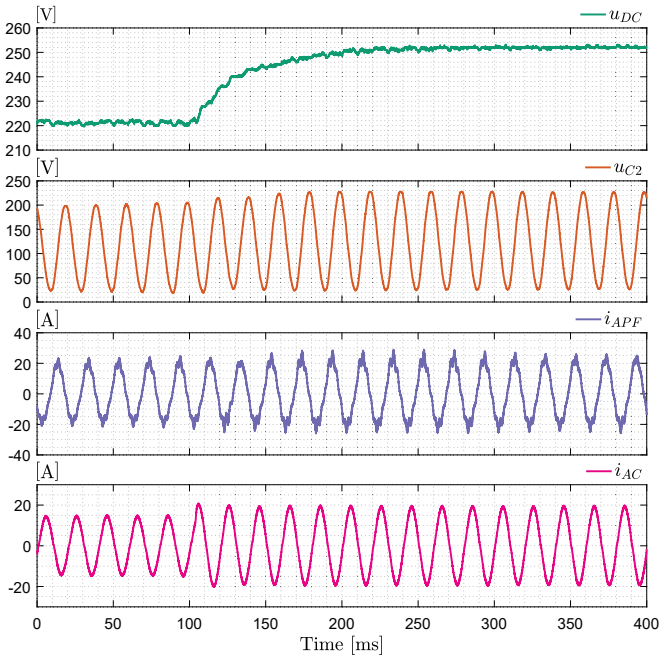

Fig. 12: Transient response of the APF during a voltage step from 220V to 250V

DC link capacitance of the SST. A 1kVA prototype of the APF has been built and tested to verify the design. Nine APF units are currently being manufactured for testing on the overall ISOP SST, and the result will be given in future works.

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