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Topical Review

# Review: III–V infrared emitters on Si: fabrication concepts, device architectures and down-scaling with a focus on template-assisted selective epitaxy

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**Abstract**

The local integration of III–Vs on Si is relevant for a wide range of applications in electronics and photonics, since it combines a mature and established materials platform with desired physical properties such as a direct and tuneable bandgap and high mobility. The large thermal expansion coefficient and lattice mismatch, however, pose a challenge for the direct growth of III–Vs on Si. In this paper we will review fabrication concepts to overcome this mismatch for the local integration of III–Vs on Si. In particular, we will briefly discuss processing methods based on aspect ratio trapping, nanowire growth, and template-assisted selective epitaxy (TASE). The focus of this review will be on the latter, where we will provide an overview of the different possibilities and embodiments of TASE and their promise for locally integrated active photonic devices.

Keywords: nanolasers, nanophotonics, III-V epitaxy, monolithic integration

(Some figures may appear in colour only in the online journal)

## 1. Introduction

Comparable to the downscaling of integrated circuits and transistors, there has been a tremendous journey from the first generation of lasers in the 1960s, to the development and commercialization advanced semiconductor lasers and light emitting diodes (LEDs). Owing to their capability to convert electrical signal into optical ones and localize the electromagnetic field to small volumes, while potentially maintaining a small energy budget and fast dynamics, nanoscale light sources are at the heart of many applications and strive to enter in new realms of technologies such as quantum information processing applications and optical communication [1–4], sensing and tracking [5, 6], or display technologies.

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Specially in light of the increasing global internet traffic and higher demand for data storage [7] and processing there is a need for alternative communication solutions to leverage the interconnect bottleneck [8–10]. Since modulation speed scales inversely and energy consumption proportionally with laser volumes [11] it is hereby essential to downscale todays emitters in order to be a true complementary asset to traditional electronic chip-components.

Group-IV semiconductors, especially Si provide an ideal platform since they already possess a well-established and cost-effective fabrication infrastructure. Also, state-of-the-art integrated high-speed photodetectors are made of Ge [12–14]. However, their indirect bandgap pose a constraint for efficient light sources, although there have been some promising developments on GeSn-based materials [15–18].

III–V semiconductors on the other hand have proven to be ideal compound materials for light sources in the visible and infrared region due to their direct and tunable bandgap. They also enable the implementation of hetero-junctions, quantum wells (QWs) and quantum dots on the same material platform. Moreover, due to their high absorption coefficients and mobilities they are also promising material alternatives to Ge-based photodetectors.

The ultimate goal would be a side-by-side integration of electronic and photonic function on chip, to achieve a fully integrated optoelectronic communication platform with added functionalities as well as high clock and modulation speeds when necessary. For this it is crucial to not only scale active and passive photonic components down, but also to establish a processing routine which makes a seamless integration with Si-based components feasible. Bearing this long-term vision in mind we will discuss the different integration techniques for III–V on Si and their potential for scaled light sources for on-chip communication.

For emitters in the visible wavelengths, excellent devices in particular based on III-nitrides (III-N) have been demonstrated. Indeed, III-N based devices have driven the revolution that the solid-state lighting market has experienced in the past years. The pioneering work of I. Akasaki, H. Amano and S. Nakamura was recognized with the 2014 Nobel Prize in Physics 'for the invention of efficient blue-LEDs which has enabled bright and energy saving white light sources'. Since we focus on emitters in the near infrared, we will not include demonstrations based on III-Ns. Instead we refer the reader to further readings like [19, 20].

In this paper we shall first review different approaches at monolithic integration of III–V on silicon, focusing on nanolaser technologies. In particular related to template-assisted selective epitaxy (TASE), which is an epitaxy technique pioneered in/by our group. Then we will discuss different types of cavity architectures, as well as possibilities for electrical actuation which is one of the great challenges of micro- and nanolasers. While in the following we cannot cover all the developments in the field of scaled lasers, our aim was to cover representative work rather than an exhaustive literature collection.

## 2. Integration of III–Vs on silicon

Si is an excellent material for fabricating cost-effective and efficient electrical chips. It also has a natural well-passivating oxide, and it is extremely abundant in nature. In terms of photonics, it provides a suitable basis to serve as an optical waveguide for transmission above 1.1 $\mu$m, such as low loss single mode waveguides and passive structures that can be built on a silicon-on-insulator (SOI) platform. The seamless integration of efficient light emitting materials on a Si platform is the main challenge. This is due to a significant mismatch in crystal lattice, polarity, and thermal coefficient between both semiconductor families.

Heterointegration of III–Vs on Si can be divided into two main approaches: Wafer-level or local integration. The first approach is aimed to integrate a layer of III–Vs covering large fractions of or the entire Si wafer surface. With respect to maturity for large scale manufacturing, established techniques like buffered layer growth or wafer bonding, have been used to demonstrate the most advanced devices, such as vertical-cavity surface-emitting lasers (VCSELs) or heterogeneously integrated distributed Bragg reflectors (DBR) lasers, which in terms of performance currently supersede that of the local integration techniques. In contrast, the local integration of small volumes of III–V material is of interest for the implementation of hybrid III–V/Si devices as well as for an integration with Si-based passives or electronics. We believe that as the local integration techniques mature, the ability to place the III–V devices in-plane with silicon electronics or passive features will provide for new opportunities. Hence, in the following we will introduce both techniques, but mainly focus on the latter as monolithically integrated devices are the central point of the present review.

### 2.1. Wafer scale approaches

*2.1.1. Wafer bonding.* Wafer bonding is one of the most mature techniques for the integration of III–Vs on Si. Lattice matched active material is grown on a donor wafer and then bonded onto an acceptor wafer. Moreover, an intermediate oxide layer, whose thickness can be tailored, is included when needed. The devices can either be fabricated before or after being bonded and in principle the donor wafer is reusable. The ability to bond the III–V layer on top of a pre-processed silicon photonic integrated circuit (PIC) or just a regular integrated circuit (IC) makes this solution particularly attractive for high-performance devices and novel chip schemes such as a 3D integration with different functionality layers while maintaining an appropriate thermal budget. Both, lasers [21–23] as well as photodetectors [24–26] have been demonstrated using bonding.

One drawback of wafer-bonding is the mismatch between the typical size of the III–V substrates (usually 100 mm or 4") and silicon substrates used in commercial processes (up to 300 mm or 12"). In this case the bonding of a III–V active layer on top of the silicon wafer for post-processing would result

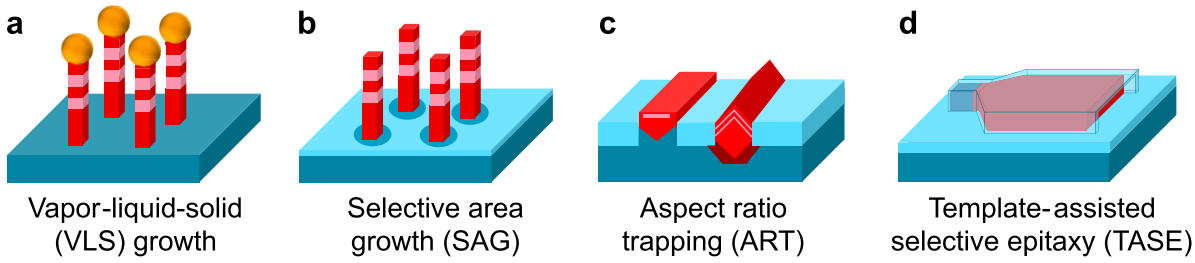


**Figure 1.** Illustrations of monolithic integration methods for III–Vs on Si. From left to right: (a) vapor-liquid-solid (VLS) growth, (b) selective area growth (SAG), (c) aspect ratio trapping (ART), and (d) template-assisted selective epitaxy (TASE).

in a substantial waste of Si die area. A solution to this is die-bonding where instead of a full wafer individual III–V dies are bonded onto the Si acceptor wafer [27, 28]. Another is micro transfer printing, where micron-sized III–V based devices are transferred to a Si photonics wafer in a highly parallel manner using an elastomer stamp [29–31].

Bonding and transfer printing are undoubtedly presently the most cost-efficient and mature technologies for bringing large areas of III–V material onto a silicon platform. A couple of recent reviews cover applications of III–V wafer bonding for electronics and photonics integration and we would refer the reader to these [31–34].

*2.1.2. Buffered layer growth.* The direct growth of III–V films on top of a pristine silicon wafer is bound to lead to dislocations and defects. First, because the lattice constants of III–Vs and silicon crystal differ and secondly because of mismatch of thermal expansion coefficients. The latter means that even if we were to grow III–V on top of silicon without excessive defects at the elevated temperatures, which are typically used in different epitaxial techniques (500 °C–700 °C), cooling down the wafer again to room temperature could induce strain and defects.

Techniques to mediate the defects from the lattice mismatch between III–Vs and Si is to use buffer layers with graded lattices, introducing defect trapping layers, as well as thermal annealing steps [35, 36]. In this way defects densities are reduced and the upmost material layer is of higher quality. This approach has been successfully employed to realize electro-optical devices using quantum dots and QWs among others [37–41]. The main benefit in this method is in bringing III–Vs onto the wafer sizes of silicon to benefit from subsequent fabrication platforms. In addition, it is a relatively low-cost approach. However, the need for long epitaxial growth runs with a large thermal budget and overall stack thickness including the buffer layer makes the co-integration with electronics and photonics challenging, despite clever engineering methods like growth on grooves with the preferred Si(111) facet [39, 42].

A very recent demonstration shows the integration of mushroom-shaped microdisks on on-axis Si(001) via an InP buffer [43]. Optically pumped continuous-wave (cw) lasing around 1550 nm is achieved from InAs/InGaAs based quantum dashes with average thresholds of around 500 $\mu$W. Special care is taken for smooth sidewalls and air cladding is chosen for optical confinement. While the threshold is still larger than the 200 $\mu$W which is achieved on similar devices directly on an InP substrate, it is notably, to the best of our knowledge, the first room-temperature cw lasers with C-band emission to be grown on Si, based on that material stack, and fabricated using buffered layer growth.

### 2.2. Local integration techniques

For many applications, local integration of III–V micro- or nanostructures at predefined positions on a Si wafer, as well as the side-by-side co-integration of different compounds, lateral integration to Si, and co-integration to electronics is desired. In the following we introduce some of the local integration techniques such as nanowire (NW) growth, aspect-ratio trapping (ART), and TASE which are illustrated in figure 1. We will also discuss their benefits and challenges to achieve the above-mentioned goals. At the end of section 3, in table 1, a non-exhaustive list of some representative results in this field is included, focusing only on room-temperature devices which are monolithically and locally grown on Si without using a buffer layer. A recent review focusing on selective hetero epitaxy of III–Vs on Si(001) platforms is given in [44].

*2.2.1. NW growth.* NW growth on Si is a promising approach for scaled photonic devices, since it allows for the integration of high-quality material with small footprints directly grown on Si [45]. In NWs the surface of nucleation on Si, i.e. the cross-section of the NW at the stem, is small, usually on the order of 100 nm$^2$ or less: This means that those defects that arise due to the lattice mismatch will terminate within a few nanometers of the interface and not lead to propagating dislocations along the NW length.

Another feature of NWs is that by tuning the precursor composition and growth conditions it is possible to incorporate homo- or heterojunctions either cross-sectional (along the axis/length of the NW) or radially creating core shell structures [46–49]. In the axial direction the same advantage is true as for the nucleation step: Due to the small cross-sectional area of the NW, heterostructures of highly lattice mismatched

Table 1.Examples of monolithically grown III-V emitters from litterature.

| Growth Method | Material | Geometry | Dimensions diameter ($D$), length ($L$), width ($W$), height ($H$) | Wavelength | Threshold | Reference |
|---|---|---|---|---|---|---|
| Catalyst-free core–shell NW on Si(111) | InGaAs | Nanowire | $D = 700$ nm, $H = 3$ $\mu$m | ∼950 nm | ∼93 $\mu$J cm$^{-2}$ | [166] |
| Catalyst-free core–shell NW on Si(111) | InGaAs | Nanowire | $D = 650 \pm 50$ nm, $H = 3.5 \pm 0.7$ $\mu$m | ∼980 nm | 38.2 $\mu$J cm$^{-2}$ | [64] |
| SAG on SOI(111) | InGaAs | 1D nanowire PhC | $D = 180$ nm, $H = 700$ nm, $L =$ | 1100–1440 nm | 80–110 $\mu$J cm$^{-2}$ | [45] |
| SAG on SOI(111) | InGaAs | SOI WG in 1D nanowire PhC | $D = 140$ nm, $H = 800$ nm, $L = 6.7$ $\mu$m | 1100 nm | 100 $\mu$J cm$^{-2}$ | [63] |
| SAG on SOI(111) | InGaAs | Nanowire | $D = 140$ nm, $H = 800$ nm | 1100 nm | 16 $\mu$J cm$^{-2}$ | [63] |
| ART on Si(001) | InGaAs QW | DFB | $L = 100$ $\mu$m, $W = 500$ nm | 1354 nm | 7.8 mW | [91] |
| ART on SOI | InGaAs QWs | FP | $W = 450$ nm, $H = 800$ nm, $L = 38$ $\mu$m | 1511 nm | 16 $\mu$J cm$^{-2}$ | [89] |
| ART on Si(001) | InP | Suspended DFB | $W = 500$ nm, $H = 250$ nm (triangle), $L = 45$ $\mu$m | 930 nm | 22 mW | [81] |
| SAG on Si(111) | InP | Pillar FP | $D = 1.7$ $\mu$m, $L = 5$–$20$ $\mu$m | 874 nm | 300 kW cm$^{-2}$ | [66] |
| ART on Si(001) | InGaAs QWs | Nano ridge, DFB | $W = 458$ nm, $H = 602$ nm, $L = 102$ $\mu$m | 1028 nm | ∼37 mW | [90] |
| NW-overgrowth on Si(001) | InP | FP | $D = 400$ nm, $L = 1.4$ $\mu$m | 840–920 nm | 1.69 pJ | [167] |
| TASE on Si(111) | GaAs | Microdisks | $D = 1$–$3$ $\mu$m, $H = 335$ nm | 880 nm | 2–18 pJ pulse$^{-1}$ | [116] |
| NRE on Si(001) | InGaAs MQWs | Loss coupled DFB with Au gratings | $L = 300$ $\mu$m, $W = 460$ nm, $H = 600$ nm | 1024 nm | 10 kW cm$^{-2}$ | [93] |
| TASE on SOI | GaAs | Microdisk and micro ring | $D = 1.2$ $\mu$m | 860 nm | 10 pJ pulse$^{-1}$ | [117] |
| ART on SOI(001) | InGaAs QW | FP | $L = 50$ $\mu$m, $W = 500$ nm | 1500 nm | 40 $\mu$J cm$^{-2}$ | [84] |
| ART on SOI(001) | InGaAs QW | FP with DBR | $L = 20$ $\mu$m, $W = 500$ nm | 1478 nm | 38 $\mu$J cm$^{-2}$ | [92] |
| TASE on Si(111) | InP | Microdisk | $D = 1.28$ $\mu$m | 840 nm | 200 $\mu$J cm$^{-2}$ | [115] |
| TASE on Si(111) | InGaAs | Microdisk | $D = 1.5$ $\mu$m | 1530 nm | 2.72 pJ pulse$^{-1}$ (270 $\mu$J cm$^{-2}$) | [118] |

systems can be grown. This is not generally the case for planar approaches.

Typical NW growth techniques include vapor-liquid-solid (VLS) growth which employs a metal catalyst to initiate growth. The size of the catalyst particle (usually gold) determines the diameter of the NW [49–51]. An example is shown in figure 2(a), where a NW array with axial heterojunctions on Si is grown from Au particles by VLS growth [52]. Complementary MOSFET (CMOS) technology-compatible VLS growth using Sn- [53] or Ga-catalyst particles have been employed successfully for III–V NW growth. In [54] for example self-catalyzed VLS is used to grow radial InGaAs multi quantum well (MQW) NWs on Si(111) (see figure 2(b) for SEM images). The growth conditions, in particular regarding the QW design, kinetics and control over composition are studied for tuneability in emission wavelengths and the NWs

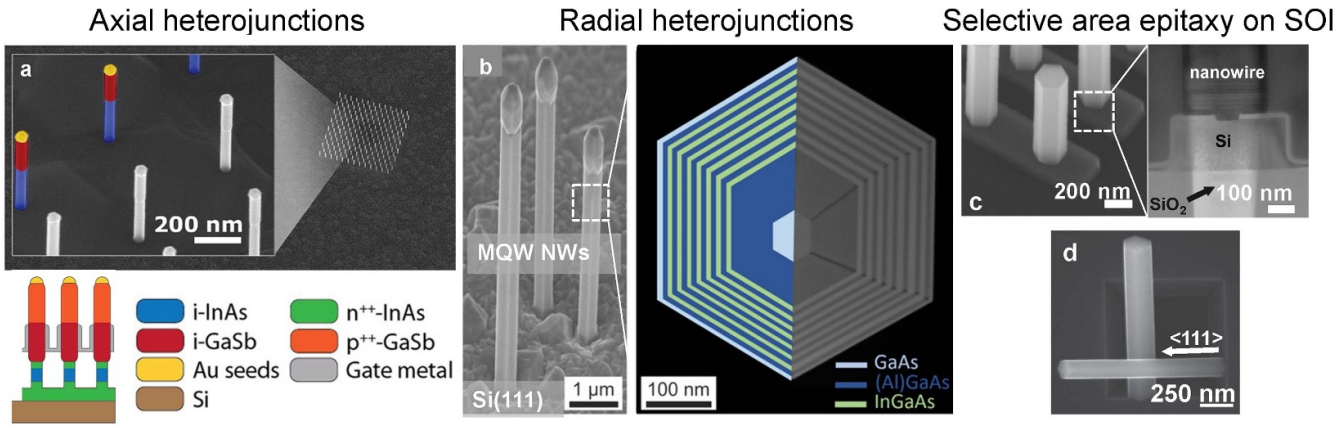


**Figure 2.** Representative examples of nanowire growth methods of III–Vs on Si. (a) Axial heterojunctions on Si grown from Au particles by VLS growth. Reprinted with permission from [52]. Copyright (2015) American Chemical Society. (b) Radial InGaAs/AlGaAs multi quantum well nanowires grown via self-catalyzed VLS on Si(111). Reprinted with permission from [54]. Copyright (2018) American Chemical Society. Selective area epitaxy on SOI: (c) top: nanowires grown on SOI with (111) orientation. Reprinted with permission from [57]. Copyright (2016) American Chemical Society. (d) Bottom: nanowires grown on SOI with (001) orientation. [58] John Wiley & Sons. Copyright (2020) WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

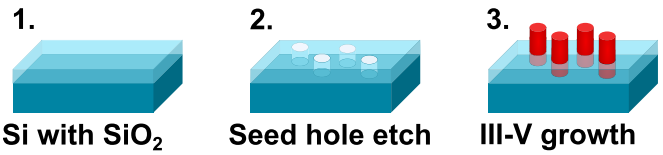


**Figure 3.** Illustration of a representative process flow for SAG used to grow vertical nanowires. Holes are etched into the oxide, which serve as seeds for the subsequent growth of the III–V nanowires.

are transferred to a sapphire substrate to study the PL and lasing behavior. Compared to a Si substrate, sapphire has a better refractive index contrast to the III–V NWs and hence enables lasing.

Another advantage of VLS grown NWs is, that they allow for crystal phase tuning [55, 56] with the principal growth direction along [111]zincblende (ZB) or [0001] wurtzite (WZ), which is not generally the case in TASE and ART.

Alternative to VLS, NWs can be grown via selective area growth (SAG), in which the growth substrates is covered by a dielectric mask, with openings in the mask defining areas of possible nucleation (seeds) (see figure 3 for a representative process flow for the growth of vertical NWs using SAG). In SAG NW growth the diameter of the NW is defined by both the mask opening and the growth conditions.

In [57] a first demonstration of InGaAs NWs grown on 3D structures and planar SOI layers with a Si(111) orientation was demonstrated using a catalyst-free SAG. This enables waveguide coupling to nanorods as well as rod-type photonic crystal (PhC) designs. Figure 2(c) shows a tilted scanning electron microscopy (SEM) image of such a NW array as well as a cross-sectional TEM image of the bottom part of one wire. Recently an approach for the integration of NWs on SOI with the more established Si(001) orientation has been presented by exposing specific (111) facets by wet etching and subsequent selective area epitaxy [58] (see figure 2(d)).

NW growth can be extremely versatile in terms of the choice of materials and provide for many unique concepts, such as core–shell NWs with radial QWs [54], NWs with embedded quantum dots [59], or scaled active photodetectors [60, 61]. Several different architectures for NW lasers have been demonstrated on both III–Vs [49, 62], and Si substrate [45, 63–67] (see figure 2 and table 1). However, there are also some drawbacks from a device perspective: Firstly, vertical geometry does present a challenge for advanced device designs and contacting, hence many electrically active demonstrations are based on pick- and place of the NW onto another platform [68, 69], hindering facile scalability. Secondly, it is difficult to prevent radial growth, so that when incorporating junctions along the length of the NW, overgrowth of the previous segments can be an issue [70, 71]. Besides demonstration of lasing, low device-to-device variations and reproducibility are important in order to gain more technological maturity. In bottom-up integration methods, inhomogeneous growth across the wafer may lead to differences in material quality and cavity geometry. Some work on correlation and statistics give insight into important material, growth and size parameters for optimizing room temperature lasers [72, 73]. In [72] GaAs/AlGaAs radial MQW NW lasers on GaAs (as fabricated in [49]) are studied by combining statistical analysis and an all-optical characterization technique. It is found that thicker wells with reduced disorder and longer wires for reducing cavity mode separation lead to more uniform low-threshold operation. In [73] the effect of doping on lasing and growth is studied for Zn-doped GaAs NW.

Vertical NWs can sustain helical modes, given that the contrast in refractive index between the NW and the substrate allows for a sufficient optical feedback. Specially for InP-based NWs on Si this can be challenging, since InP has a lower refractive index than Si. One solution is by growing the NWs on a SOI substrate, where the bottom reflection is

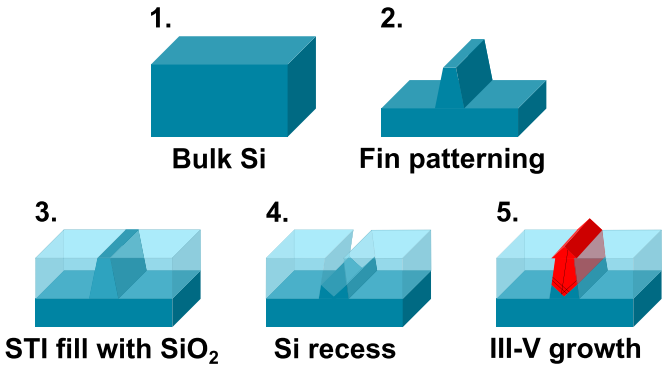


**Figure 4.** Illustration of a representative process flow for ART. Si fins are patterned into bulk Si. The Si recess with a trench is formed after filling the structures with $SiO_2$ using a STI method. The III–V material is grown onto the trench.

improved due to the low-index oxide. Alternatively, for optically pumped devices on Si an undercut can improve quality factors of the devices [65]. Through selective etching of the Si under the NW, the bottom reflection is improved due to the air gap between the Si and the NW. Also, a shell might provide additional passivation [64, 74], improved radiative recombination, and improved internal quantum efficiencies [64, 75, 76], enabling lasing at room temperature. For electrical devices this might however complicate the contacting scheme. In fact, to the best of our knowledge, locally integrated III–V NW lasers on Si with electrical or cw-operation at room temperature remain to be demonstrated. Finally, in [77] co-axial GaAs-InGaAs MQW nanolasers were grown on Si(111) with an intermediated strain-compensating buffer layer between the core and the MQWs region. Those NWs showed room temperate lasing (after transferred to sapphire substrates) at 1.3 $\mu$m with lower thresholds than comparable InGaAs/AlGaAs based NW-lasers with highly strained MQWs [54] (see figure 2(b)). This is a very remarkable achievement, since only few locally integrated nanolasers emitting above 1.1 $\mu$m have been demonstrated so far.

An extensive and detailed review on fabrication and applications of III–V NWs is given in [78] and a review on challenges and pathways to industrial scalability of NW arrays was recently published in [79].

*2.2.2. ART.* ART and nano-ridge engineering (NRE) are alternative local epitaxial methods used for electronic [80] and optical [81–85] applications. Here, oxide trenches are used to direct the growth of III–V ridges starting in most cases from an (111) interface on Si via SAG [86, 87]. NRE is a variation of ART: While it still uses confined and narrow trenches, the III–V volume can be increased by growing out of the trench. Figure 4 sketches a representative process flow for ART, starting from a bulk Si substrate.

In the following we will not distinguish the terms ART and NRE, but we refer to [88] where a more detailed introduction on ART and NRE is given.

The relatively high-aspect ratio oxide trenches assure that threading dislocations are terminated on the sidewalls of the

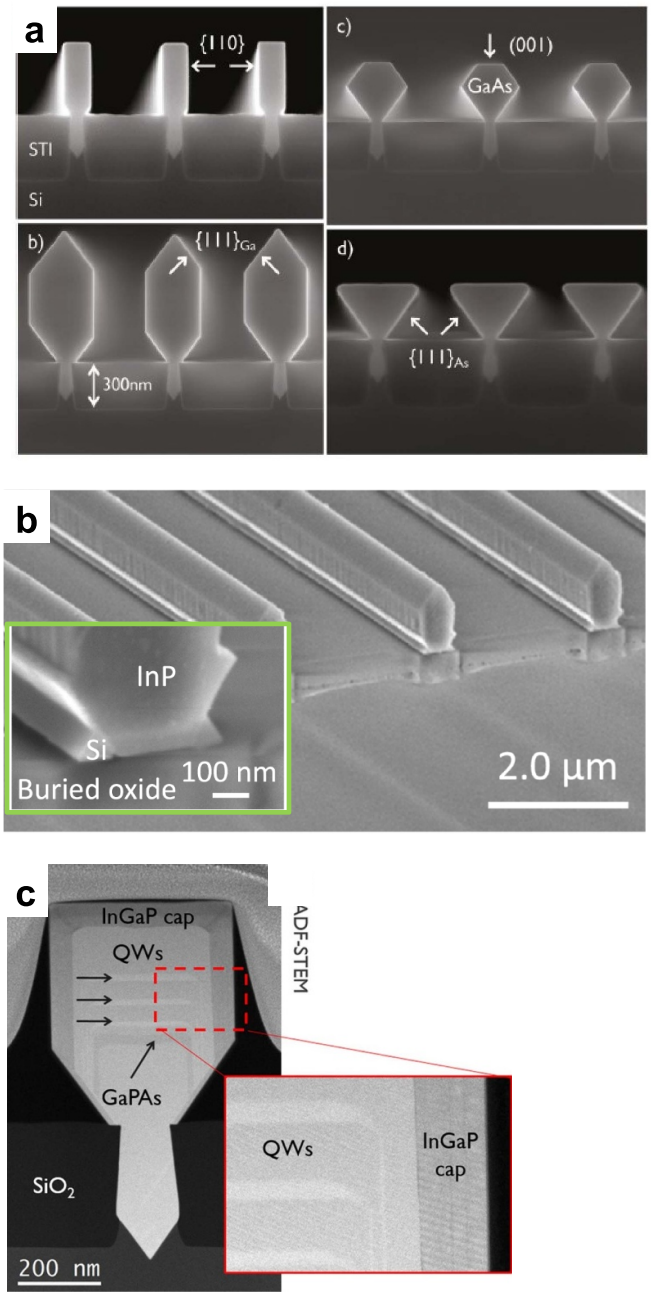


**Figure 5.** Examples of ART grown materials on Si. (a) Shape and materials tuning by careful device and growth engineering. Reprinted from [88], Copyright (2019), with permission from Elsevier. (b) InGaAs/InP ridge lasers grown on Si by using trapezoidal troughs instead of V-shaped grooves. Adapted with permission from [89] © The optical Society. (c) InGaAs/GaAs MQW single-mode DFB laser grown on standard Si. Adapted with permission from [91] © The optical Society.

oxide trenches and therefore do not propagate into the III–V gain material. The material itself is typically grown via metal-organic chemical vapour deposition (MOCVD) and the geometry, surface reconstruction, and shape can, to some extent, be controlled through the growth conditions, as it is shown in figure 5(a).

One of the advantages of this technique is that it is highly parallel and unlike NW growth one ends up with

nanostructures integrated in-plane on silicon which are much more compatible with conventional IC processing techniques.

The defect termination is very effective in two directions, but there is no defect trapping by oxide trenches along the length of the III–V ridge. Therefore, to minimize threading dislocations, ART often makes use of a sacrificial intermediate material like GaAs, similar to a buffer layer growth but much thinner, which reduces the lattice mismatch toward the substrate. This buffer layer is subsequently selectively removed [81]. Typical buffer thicknesses in ART are around 200–300 nm (and dependent on trench widths). In planar buffer layer growths, the dislocation filtering layers can be around 1–2 $\mu$m thick.

In [89] a modified version of ART is used to grow III–V ridge lasers emitting at 1.5 mm on top of an SOI Si photonics platform (see figure 5(b) for a SEM of the device). By using trapezoidal troughs instead of V-shaped grooves more flexibility on the underlying Si device thicknesses can be obtained.

In [90] a sophisticated distributed feedback (DFB) nano ridge laser is fabricated based on a GaAs nano ridge extending out from the substrate and incorporating InGaAs (20% In) QWs (following the growth method introduced in [82]), see figure 5(c) for cross-sectional SEM of the device. The device emits at 1028 nm under optical excitation. Unlike previous demonstrations on InP and InGaAs [81, 91], an under etching of the Si substrate to prevent leakage loss due to the high refractive index of Si is not needed, since the III–V material can be extended above the wafer surface. This improves the confinement of the mode and reduces losses.

The devices integrated by ART are usually confined in two dimensions but have a length of tens of micrometers. DBR enable a reduction of the device length to some extent: For example in [84] a Fabry–Pérot (FP) type laser with a length of around 50 $\mu$m integrated on SOI with (001) was presented. By using DBRs at the ends of the cavity in [92], the length of the devices using similar materials could be reduced down to 20 $\mu$m, because the mirror reflectance was improved.

Electrically pumped DFB lasers on Si realized via ART have, to our knowledge, not been demonstrated yet. However, in [93] a viable option for contacting these kind of devices is given, by using metallic DFB gratings, instead of III–V ones, which would be etched into the ridge.

*2.2.3. TASE.* The key concept of TASE is the growth of III–V material within a hollow pre-defined $SiO_2$ template exposing at one extremity a confined Si seed on which the III–V may nucleate [94]. Originally, it was inspired by NW growth, but targeted to alleviate the issues related to overgrowth of junctions in vertical NW structures [95, 96]. Later on, variations of TASE were developed for growth along the surface of the silicon wafer—we refer to this as in-plane as this facilitates the fabrication of contacts and more advanced architectures than the vertical NW geometry. To this end, TASE based on an SOI process was developed [94], as well as for planar growth proceeding from a seed on a conventional Si wafer [97]. The nucleation seed is kept small to avoid propagating dislocations similar to NW growth. But unlike NW growth, where the shape and orientation of the NWs is mainly determined by the growth conditions, the shape of the TASE-grown features is given by the shape of the hollow template into which it is grown. This allows for a lot of variation in the possible designs. Similarly, in TASE the growth is from a Si(111) facet, but the direction of the growth can be chosen freely, since the growth facet can be tuned by the growth conditions [98]. Figure 6 shows a simplified process flow for the integration of III–Vs on both, Si(111) and SOI substrates. For the TASE on Si(111) process a Si pillar with a diameter of 50–100 nm is etched into the wafer and the substrate is subsequently covered with oxide and planarized to the Si pillar height using chemical-mechanical polishing and reactive ion etching. Alternatively, the oxide can be deposited first and a narrow trench can be etched into the material, if the aspect ratio is sufficiently small. To protect the Si seed from the following processes, around 5 nm $Al_2O_3$ is deposited before a sacrificial amorphous Si (aSi) layer is sputtered and etched. This will define the shape and location of the template. An oxide layer, which will serve as the template is deposited on the sample and locally opened. After opening the templates, the sacrificial aSi layer and the protection oxide on the Si pillar are selectively etched. Now, the III–V material can be grown inside the template using MOCVD. The template shape and position have potentially a nanometer precision, since they are defined in a one-step electron-beam lithography process. Hence, any imprecision stems from process variations, such as roughness when patterning the initial Si features or shrinking/expansion of the template during the subsequent processing. However, there is an upper limit to the template size, given by the diffusion length of the precursors from the template opening to the nucleation seed. Larger area coverage could be realized by merging multiple III–V regions. Also, in general, higher aspect ratios can be more challenging to realize due to the facet-dependent growth rates. For the TASE on SOI process, there is no need of a sacrificial aSi layer since the template positions and shape can directly be defined on the topmost Si layer. In the bottom schematics of figure 6 the case for a waveguide coupled p–i–n photodetector with self-aligned waveguides is shown. For details on the process we refer the readers to [61].

Figure 7 shows some of the key characteristics of TASE, divided into different segments such as feasible integration schemes (blue, first row), different material platforms (green, second row), devices with applications in electronics (pink, third row) and photonics (orange, bottom row).

As illustrated in figures 7(a)–(d), TASE offers flexibility on integration schemes, where lateral (figure 7(a) [100]), vertical (figure 7(b) [101]), Hall-bar structures (figures 7(c) and (d) [94]), and stacked configurations (figure 7(e) [94]) can be realized.

Another important feature of TASE is that by repeating the process, multiple III–V materials can be integrated independently and closely spaced by using consecutive growth runs. This was demonstrated specifically for InAs and GaSb [102] (see figure 7(f) for top view and cross sectional view SEM images).

Heterojunctions, specially with well-defined doping regions are crucial for electrically operated devices. Using

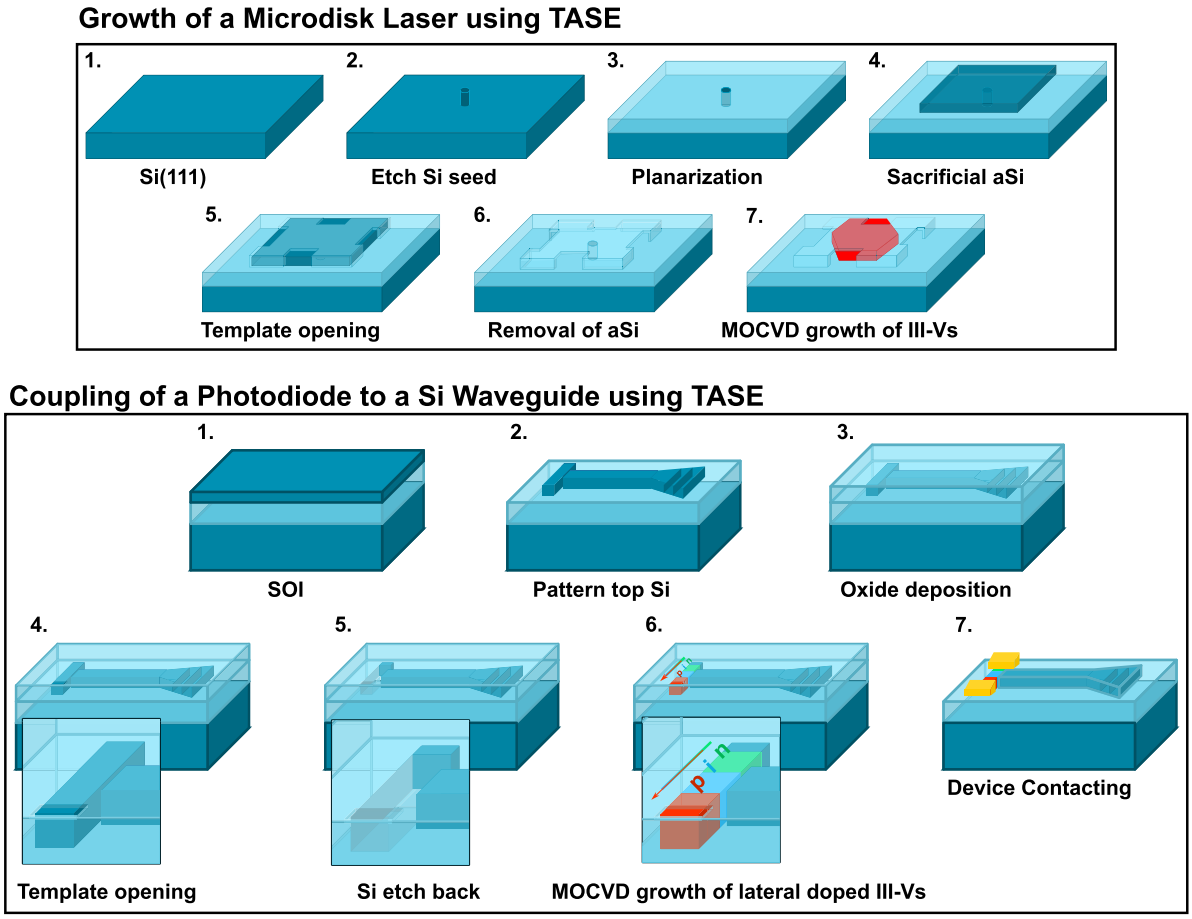


**Figure 6.** Illustration of the process flow for TASE. Top row: Example for a microdisk on a Si(111) platform. A Si seed is etched into the substrate first and then oxide is deposited and planarized to the seed level. The template shape is defined by the patterned sacrificial amorphous Si (aSi) which is covered with oxide. The template oxide is opened at selected positions and the sacrificial aSi is removed before the III–V material is grown via MOCVD. Bottom row: Schematics to fabricate a waveguide-coupled lateral doped p–i–n-structure on a SOI platform. In comparison to the TASE on Si(111) process no sacrificial aSi is needed, since the top-most Si layer is patterned to define the template shapes which are self-aligned to the waveguides and any other Si structures.

TASE, such profiles can be grown without the need of complex doping diffusion and regrowth processes [60, 103]. Figure 7(g) shows the cross-section of such a heterojunctions, consisting of an i–InGaAs and n-InP interface [61] and figure 7(h) depicts a vertical NW with a sharp InAs/InSb heterojunction [95]. In comparison to other NW growth processes the wires shown in [95], do not suffer from interface mixing.

Furthermore, TASE offers the possibility for integration of QWs radially along the disk periphery, similar to what may be achieved in vertical NW architectures, but with a very different aspect ratio. However, careful growth optimization is needed for compositional control of ternary materials [104] or to obtain a given crystal facet [98], both of which is essential for high-quality wells. Insightful work on defect control in confined structures and horizontal heterojunctions on InP-platforms [105, 106] has been conducted, enabling the successful integration of InGaAs-InP wells (see figure 7(i)) [105]. Similar studies would be helpful for the TASE on SOI platforms, specially to control the nucleation facet of Si. Due to the selective Tetramethylammonium hydroxide back etch the Si facet is tilted, leading to angled heterojunctions [61]. By using a (110) SOI platform, vertical, straight interfaces can be obtained, by orienting the templates along the (111) direction. This was demonstrated in [107] for the growth of InAs in-plane NWs.

Some derivations of the classical TASE approach have been developed more recently: In [108] pulse electrodeposition and recrystallization instead of MOCVD growth is used to integrate InSb on Si into predefined oxide templates. This method would allow to overcome some limitations associated with the MOCVD growth such as low growth rates or difficulty in realizing structures with a high aspect ratio. In [107] the hybrid-TASE approach is presented: The integration of InAs NWs integrated on Si with cavities/templates containing TiN allowing for sharp semiconductor–superconductor interfaces open up for future applications in quantum computing, for example for cryogenic qubit control electronics (see figure 7(j)).

Originally electronic applications were targeted, where TASE provided a unique opportunity for the integration of in-plane heterojunctions [109] and also more versatile device architectures, such as Hall-bar structures [94] MOSFETs

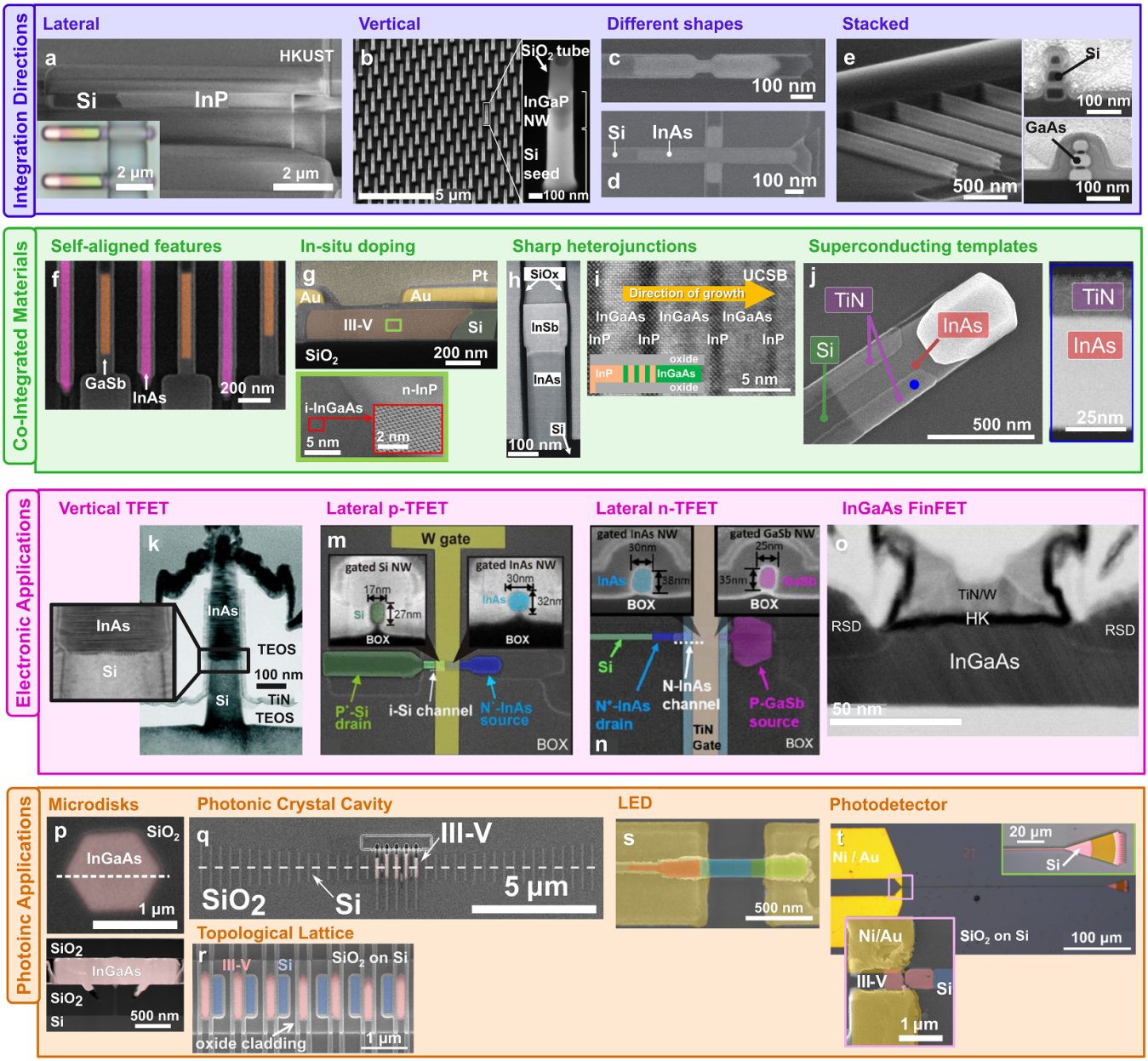


**Figure 7.** Summary of key demonstrations based on TASE exhibiting the integration capabilities featured by this approach. Integration directions: The III–V material can be integrated in (a) lateral and (b) vertical orientation with respect to the substrate. Reproduced from [100]. CC BY 4.0. Reprinted with permission from [101]. Copyright (2018) American Chemical Society. The III–V material can be grown into (c), (d) different shaped and (e) stacked templates. Reprinted from [95], with the permission of AIP Publishing. Integrated materials: (f) Self-aligned co-integration of different materials is possible. Reprinted with permission from [102]. Copyright (2017) American Chemical Society. (g) Heterojunctions and doping profiles with (h) sharp interfaces can be defined directly during the growth. Reproduced from [61]. CC BY 4.0. Reproduced from [96]. © IOP Publishing Ltd All rights reserved. Besides Si/SiO2, different platforms can be used, such as (i) InP or (j) TiN based cavities for quantum applications. Reprinted with permission from [105]. Copyright (2019) American Chemical Society. Adapted with permission from [107]. Applications: Using TASE, several different devices for electronics applications such as (k) vertical and (m), (n) lateral tunnel field-effect transistors (TFET) and (o) FinFETs have been realized. © 2015 IEEE. Reprinted, with permission, from [112]. © 2016 IEEE. Reprinted, with permission, from [109]. Reproduced from [114]. CC BY 4.0. For photonics applications, (p) whispering gallery mode emitters, © 2021 IEEE. Reprinted, with permission, from [118], (q) hybrid photonic crystal cavities, Reprinted with permission from [103]. Copyright (2020) American Chemical Society, (r) topological lattices, © 2022 IEEE. Reprinted, with permission, from [120], (s) LEDs, Reproduced from [60]. CC BY 4.0, and (t) waveguide coupled photodetectors [61] have been demonstrated amongst others. Adapted with permission from [121] © The optical Society.

[94, 110], nanosheet-FET [111], vertical [112] (figure 7(k)) and lateral TFETs [109, 113] (figures 7(m) and (n)), and InGaAs FinFETs [114] (figure 7(o)).

Recently we have shifted our focus toward photonic applications [60, 103, 115–117], which include microdisk cavities [115–118] (figure 7(p)), PhC cavities [103, 119]

(figure 7(q)), topological lattices [120] (figure 7(r)), LEDs [60, 61] (figure 7(s)), and photodetectors [60, 61, 121] (figure 7(t)). More details, in particular on the PhC cavities and microdisks will be give in the next subsection.

From a device fabrication perspective each of the different integration techniques introduced in this section, have their own merits and challenges. While NW growth allows for the dense integration of structures with a small footprint and well controlled material compositions, for practical applications pick and place methods have to be employed. The complexity of this along with the alignment precision is a serious limitation from a system integration perspective. ART is a highly parallel integration technique where the III–V material is already integrated in plane/parallel to the substrate. This is beneficial for further device processing. In ART the III–V structures are grown within a trench. High-quality material and QWs have been demonstrated, however, the geometries of the resulting structures are inherently limited in this approach. This also results in a difficulty for direct coupling to in-plane features.

Compared to other local and wafer-scale integration methods, TASE is a relatively novel process, where growth parameters to control composition and facets are still being optimized and calibrated. However, it allows for in-plane doping profiles, heterojunctions, different growth shapes, self-alignment to existing Si features and full wafer-scale processing, making it a promising integration method in the long-term.

## 3. Micro- and nanolaser architectures

The main types of optical cavities employed in laser architectures can be roughly divided into three categories: FP, which rely on reflection, whispering gallery mode (WGM) cavities, in which modes are formed by total internal reflection, and PhC cavities, which use the modulation of the refractive index to confine light with certain wavelengths in the cavity. In the following we will briefly cover these cavity designs and highlight some specific work on WGM and PhC cavities.

### 3.1. FP type cavities

FP type cavities rely on reflection at the end of the facets, this is the standard architecture for most conventional lasers including (VCSELs), where the reflectors are based on highly reflective dielectric stack mirrors. The end facets of NWs naturally form mirrors because of the index contrast to the surrounding media, and FP cavities are also realized in slab waveguides. In [66] vertical InP rods of around 1–2 $\mu$m in diameters and around 10–20 $\mu$m in length grown on Si are shown to sustain FP modes due to reflections at the top facets with a reflectivity of $R \sim 0.3$, and the bottom of $R \sim 0.16$ as a result of the radial overgrowth of the InP pillar over the $SiO_2$ mask. While the InP rods shows evidence of room temperature lasing at 870 nm, the incorporation of radial InGaAs MQWs allows to shift the emission to 1.2 $\mu$m with lasing evidence at 5 K [66], being the first demonstration of site-controlled III–V rod lasers which are monolithically integrated on Si with Si-transparent emission.

In [67, 76] a similar approach is used, but based on pure GaAs also emitting around 870 nm: In [76] an AlGaAs shell is used to improve passivation of the rods, with room-temperature lasing of NWs transferred to a glass slide and in [67] beta factors of around 0.2 for NW on Si lasers are demonstrated at temperatures on the order of 10 K.

In [122] $In_{0.22}$ $Ga_{0.78}As$ quantum dots (QDs) are grown along the axial direction of a GaAs NW growth, this is done on a GaAs substrate but the method should be portable to Si. The NW forms a FP type cavity and pulsed optically pumped lasing at ∼920 nm is observed at 7 K.

The examples above are based on vertical geometries, which makes contacting and electrical pumping challenging. One notable demonstration is presented in [123] where they observe room temperature optically pumped lasing as well as electrically actuated bulk emission from individual InGaAs/InP MQW rods. Several sophisticated demonstrations are also reported, for example, based on pick-and-place methods: In this case the NWs are placed in a Si PhC to form hybrid cavities [124–126]. More details will be given in section 3.3.

### 3.2. Microdisks/WGMs

WGMs rely on total internal reflection at the surface of disk-like cavities (spheres in 3D) and rings, leading to potentially low mode volumes and light concentrated at the circumference of the device. After the VCSELS in the 80 s, the first demonstration of a room temperature microdisk laser in the 90 s [127] started a new chapter of downscaling cavities and obtaining low thresholds. WGM cavities have a robust design and, compared to more sophisticated cavity types, like PhC cavities, or DFB architectures, where the cavity has to be precisely designed and is highly sensitive to changes in the refractive index of the surrounding medium, a reduced fabrication complexity.

Another experimental advantage is that by simply varying the diameter of the device one can tune the resonant wavelength which will overlap with the gain profile.

Typical quality (Q)-factors are in the range of a couple of hundreds to a few thousands, generally increasing with the size of the disk (wavelength). While there is a limit for downscaling the mode volume due to increasing radiation losses, WGMs have the advantage of having a relatively small device footprint.

TASE allows for a bottom-up and local integration. The growth proceeds radially from a central seed taken from a conventional Si(111) wafer. This is similar to radial growth in NWs, but here the axial growth is prevented by the template. Also, the as-grown material inherently leads to a hexagonal WGM with smooth sidewalls without any further processing due to the preferred growth of III–Vs on the 111-facet. Figure 8(a) illustrates the 3D and cross-section of such a WGM

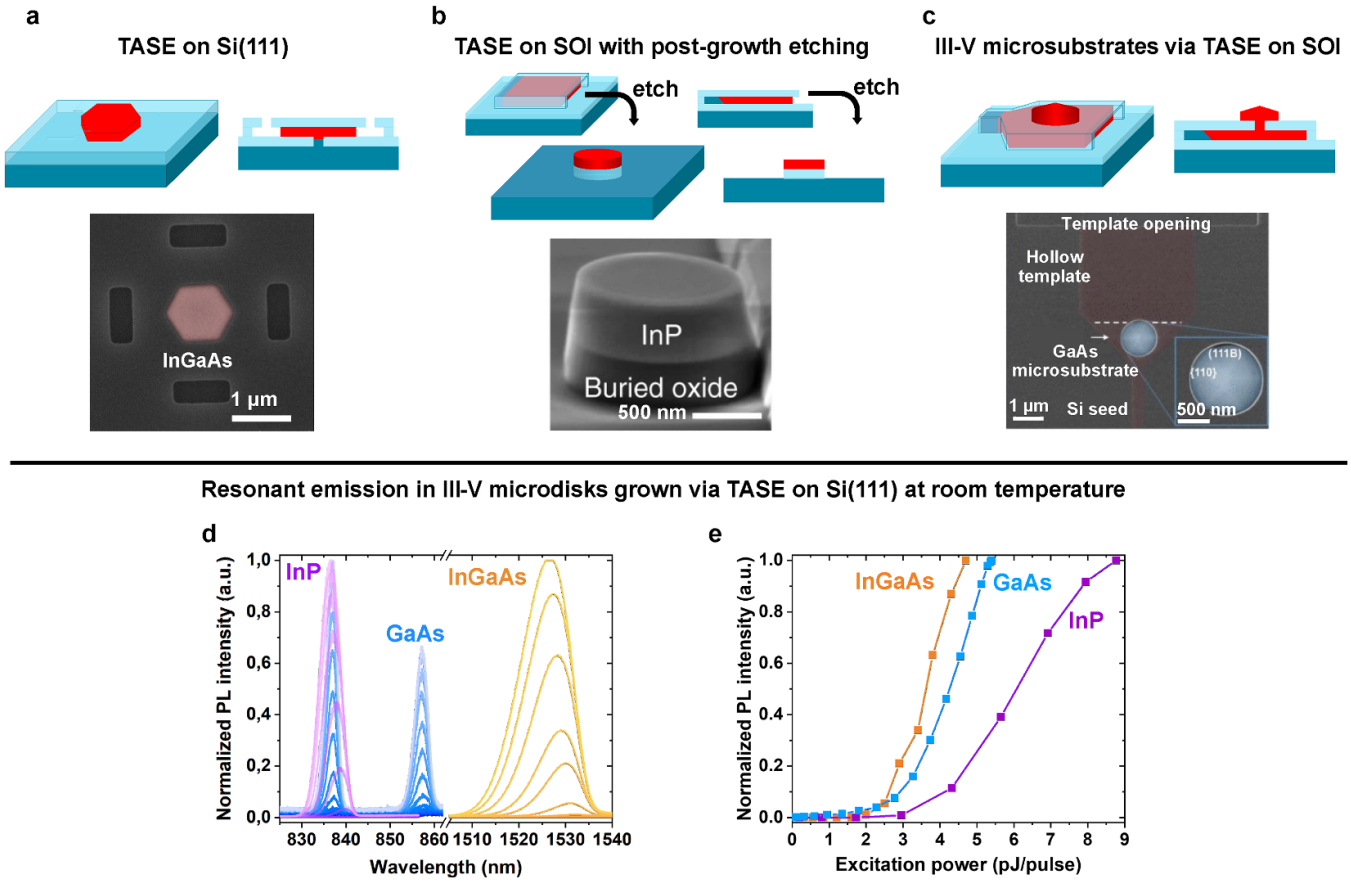


**Figure 8.** Examples of III–V microdisks on Si using (a) TASE on Si(111), © 2021 IEEE. Reprinted, with permission, from [118], (b) TASE on SOI with subsequent etching. Reproduced from [100]. CC BY 4.0 and (c) Two-step growth via TASE on SOI. © 2019 IEEE. Reprinted, with permission, from [117]. (d) Room temperature emission spectra under pulsed optical excitation with increasing input power, and (e) linear light-in-light-out curve for a GaAs [116], InP [115], and InGaAs [118] microdisk grown by TASE on Si(111) corresponding to lasing/resonant modes emitting at 837 nm and 857 nm (GaAs), 840 nm (InP), and 1530 nm (InGaAs).

as well as a SEM image of a recent demonstration [118]. A modification of the TASE technique was shown in [100], where instead of a scaled seed a trench is used, like in ART or epitaxial lateral overgrowth (ELO) which allows to create wider sheets, in which cavities can be defined by etching (see figure 8(b) for concept and SEM image). In addition, a two-step variation was explored, first employing TASE to grow a virtual substrate along the silicon substrate and subsequently in a second growth step integrate a microdisk laser [117] (see figure 8(c)) or a QW stack [128]. Using TASE on Si(111), the first demonstration of a microdisk laser was based on GaAs [116], which has the smallest mismatch to silicon of around 4%. Then evidence of room temperature lasing was demonstrated on InP WGM cavities [115], which has a mismatch of around 8% and lately to the ternary compound InGaAs [118], which showed evidence of room-temperature lasing in the telecommunication band. Figure 8(d) shows the emission spectra for these three cavities taken at room temperature and under pulsed optical excitation with increasing input power and figure 8(e) shows the linear light-in-light-out curve which is extracted from the measurements shown in figure 8(d). It should be noted, that the threshold for the different devices is similar, even though the InGaAs microdisk emits at much higher wavelengths but has similar dimensions as the GaAs and InP microdisks (around 300 nm thick and 1.3–1.5 $\mu$m wide).

The most advanced devices have been demonstrated on bonded substrates [129, 130], by micro-transfer printing [131] or fabricated by the selective under etching of a disk etched in a III–V based stack grown by molecular beam epitaxy [37, 43, 132]. A study comparing optically pumped TASE grown devices with bonded ones shows similar device thresholds and improved characteristic temperature of 190 K for the monolithically integrated cavity compared to the bonded one, which is 90 K [115]. These results imply that one can expect similar device metrics for TASE grown cavities while having the additional possibility for co-integration of different materials and devices on the same chip level.

So far, the TASE grown devices are operated under pulsed condition. Similar as for the case of NWs and pillars [64, 75, 76, 133], surface passivation may reduce surface recombination and improve the device performance. Improved heat sinking by using a metal-cladding as shown in [134] might further improve performance.

An electrically pumped and waveguide coupled WGM is demonstrated in [135] and electrically pumped micro ring

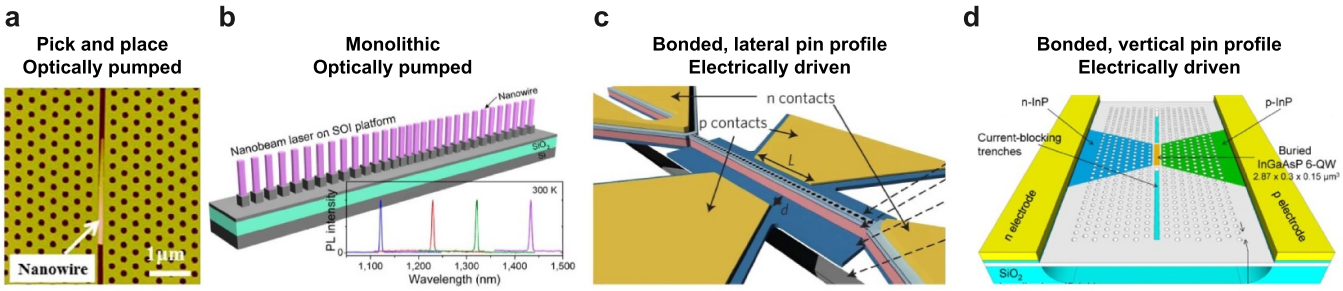


**Figure 9.** Examples of photonic crystal cavity architectures. (a) III–V nanowire integrated in a Si PhC via pick-and-place method. Reproduced from [126]. CC BY 4.0. (b) 1D PhC cavity consisting of nanowires array on (111) SOI grown via selective area growth. Reprinted with permission from [45]. Copyright (2017) American Chemical Society. (c) Nanobeam with stacked pin structures. Reprinted with permission from [21]. Copyright © 2017, Nature Publishing Group. (d) Horizontal doping profile on bonded platform, realized by ion implantation and diffusion. Adapted with permission from [161] © The optical Society.

lasers based on buffered layer growth on GaP/Si substrates [42, 136] or use of Si grooves have been demonstrated at room temperature [42]. Compared to similarly fabricated FP-type lasers [137, 138], their footprint and number of discrete modes are smaller, however, electrically pumped microdisk lasers with dimensions comparable to the emission wavelength have not been realized since losses related to heat dissipation and emission via the side facets increase substantially when the device diameter is reduced. A review in [139] focused on microdisk lasers with quantum dots summarizes recent work and compares the characteristics of electrically pumped microdisk lasers obtained via different integration methods and substrates.

While electrically pumped WGM cavities integrated via TASE remain to be demonstrated, optoelectronic simulations based on GaAs microdisks on Si suggest that a top-contacting scheme might have a lower threshold than laterally contacted devices due to potentially lower Auger losses and higher confinement and reflectivity [140]. It is notable, that for scaled lasers not only electrical pumping, but also cw operation becomes increasingly difficult for III–V lasers on Si, due to poor thermal conductivity and increased surface recombination. In that respect, using quantum dots as active material, cladding with materials with high thermal conductance or configurations with larger interfaces between cavity and substrate might improve the performance as it is for example studied in [141], where the heating in InP/InAs NW lasers with and without a $Al_2O_3$ shell layer are integrated on different platforms, such as SiN PhC, Si waveguides or a gold substrate is examined.

Some of the main challenges of WGM cavities for PICs are phase matching for waveguide coupling as well as emission and directivity control. By introducing asymmetry to the otherwise symmetric cavities emission engineering and directivity can be obtained [142–144]. Light coupling is usually done by means of evanescent coupling to an adjacent waveguide or optical fiber [145].

### 3.3. PhC cavities

By a periodic modulation of the dielectric constant photonic band gaps and resonant cavities are created. PhC cavities are popular since they combine small mode volumes and ultrahigh Q-factors on the order of $10^6$ [21, 147, 148].

The most common PhC architectures are free-standing membrane slabs usually fabricated by under etching of III–V structures grown lattice matched on an e.g. InP platform [149–151]. A general challenge in such membrane structures is heat dissipation. An important development to mitigate this and to provide additional carrier confinement was the use of a smaller volume of active gain material using an InP/InGaAsP buried heterostructure architecture, as demonstrated in [152]. It confines the active gain region with five integrated QWs to the central part of the cavity. This led to a significant reduction of the active region temperature and improved carrier confinement inside the cavity, resulting in a strong reduction of the threshold power down to 1.5 $\mu$W at room temperature. A similar approach is exploited by other groups [153].

Another approach to locally place a small active gain materials within a PhC structure is using pick-and place techniques, e.g. a III–V NW inside a Si 2D PhC structures as shown in figure 7(a) [124–126]. Such method, in the most recent work in [125] enabled Q-factors up to 25 000 along with ps-fast switching of the optically pumped NW.

While 2D PhCs have a relatively large foot print compared to mode volumes, 1D PhCs, also called nanobeams, are extended in one direction only and thus ease the integration possibilities and reduce the effective area needed on a chip significantly [154]. Nanobeam PhCs featuring electrical actuation [21, 155], tunable emission [45, 103], high modulation rates [21, 156] and waveguide coupling [157], all essential for an on-chip communication platform, have been demonstrated.

A very interesting approach is shown in [63] where InGaAs NWs are grown on top of a SOI waveguide to form a 1D periodic PhC. By varying the NW interspacing the emission wavelength can be tuned from ∼1100 to 1500 nm (see figure 9(b)) [45]. While this demonstration is on a (111) oriented facets, a PhC crystal design on a SOI with a (001) orientation is proposed in [158] which potentially could be realized using the approach presented in [58]: Specific (111) facets on a SOI wafer with Si(001) orientations are exposed by wet-etching, and the NWs are grown using selective area epitaxy (see figure 2(d) for example of a grown NW).

Electrical actuation can be challenging, because it is difficult to approach the contacts without deteriorating the cavity itself. Creating p–i–n doping profiles can also be a challenge. There are two main approaches to achieve electrical actuation in PhC structures: as-grown p–i–n vertical profiles [21] or horizontal lateral doping based on diffusion and/or ion implantation [159, 160].

Some notable demonstrations include the 1D nanobeam in [21], where a vertically stacked p–i–n layer is bonded on Si (see figure 9(c)) and the 1D QW nanobeam on InP in [155], where a semiconductor post serves as bottom electrode, and a metal as top one.

Furthermore, horizontal doping schemas as presented in the so-called lambda-scale embedded active region photonic crystal (LEAP) laser [161] led to key achievements such as data transmission as low as 4.4 fJ bit$^{-1}$. The active region consisted of InAlGaAs MQWs on a InP substrate and regrowth methods were used to create the active region. The doping regions were formed by using ion implantation and diffusion techniques. In figure 9(d) we can see a similar LEAP laser which was realized on a Si platform [146] with cw operation at room-temperature. More recently this concept was extended in [162], where through the use of the LEAP laser, a Si waveguide and a photodetector, data transmission at a bit rate of 10 Gbit s$^{-1}$ was demonstrated. PhC cavities are very sensitive to any variations in index contrast, therefore precise alignment is crucial. In our own work [103, 163], we are exploiting TASE to simultaneously limit the use of active gain material to the central cavity and ensure self-alignment between the cavity and the active medium [103]. Here the overall Si PhC is defined first on SOI with a (001) orientation. The cavity design is taken from an all Si design as proposed in [148]. Selected rods in the Si PhC lattice are then replaced by III–V material as the gain material is grown into selected areas of interest by creating an oxide cavity around the Si feature and selectively removing the Si to be replaced. This ensures an optimal overlap between the mode region and the active material, with intrinsic perfect alignment of the gain material within the Si PhC lattice. By varying the period of the PhC lattice constant (separation between two adjacent rods) optically pumped pulsed resonant emission was demonstrated over the entire telecom band at 300 K top-view and cross-section SEM images and emission spectra for different cavities with varying periodicities are shown in figure 10.

One beauty of this approach is the potential to reuse cavity designs proposed by other researchers, another is the straightforward way to introduce a lateral doping profile to the cavity; a milestone needed toward electrical actuation. In recent work [61, 121] we demonstrated the electrical actuation of detectors fabricated on the same substrate as the PhC resonant emitters, consisting of the same doped n-InP/i–InGaAs/p-InP/p-InGaAs heterojunction materials discussed above and also evaluate the device performance in LED mode. While the PhC resonators do not yet show electrically actuated lasing, we were able to measure electroluminescence in contacted NWs and waveguide coupled high-speed photodetection with bandwidths up to 70 GHz and data reception up to 100 Gbps. Compared to the previous demonstration of free-space coupled photodetection

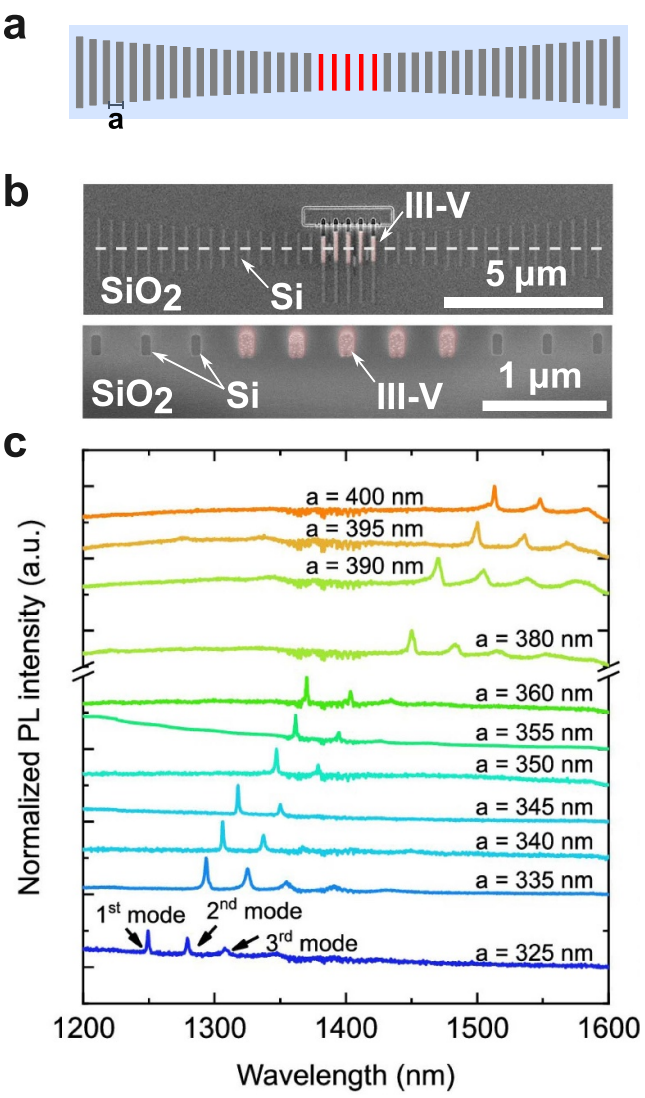


**Figure 10.** (a) Illustration of a hybrid III–V/Si 1D PhC cavity and (b) top view and cross-section SEM images of the device fabricated using TASE. By tuning the lattice periodicity a, the resonances can be tuned over the entire telecommunication range, as show in the spectra in (c) taken at room temperature under pulsed optical excitation. Reprinted with permission from [103]. Copyright (2020) American Chemical Society.

in thin NW detectors [60] (see figure 7), the device thickness in [61, 121] allows for a more efficient light emission if the diode is operated in forward bias and for propagating modes in the Si waveguide.

In [164] p–i–n heterostructures are grown on a InP/SOI platform. The devices exceed a free-space bandwidth of 40 GHz and it is shown that by using QWs instead of a bulk intrinsic region, the dark currents can be lowered.

The ability to selectively replace Si parts within the PhC structure with III–Vs with nm precision also has applications in topological photonics, which is gaining interest due to more robust device designs [165]. Initial demonstrations on a single mode topological interface PhC have been presented on wafer-bonded devices [119]. Similar structures in a hybrid III–V/Si cavity on a SOI platform are feasible as well: In [120] 1D

topological photonic lattices are fabricated via TASE. They exhibit single-mode cw emission at room temperature, which is tuneable over the entire telecommunication range. In contrast, conventional PhC cavities fabricated on the same chip have multimodal emission.

## 4. Sub-diffraction scaling

While conventional photonic lasers can achieve impressive modulation rates at very low thresholds and are also being used commercially [168], they are inherently limited in their size compared to their electronic counterparts due to the diffraction limit of light: A typical electronic switch is measured in the tens of nms whereas a typical on-chip integrated laser has lengths on the order of hundreds of microns [169, 170].

The field of plasmonics experienced an increased interest in the past decades for both metamaterials and sensing applications. Effort has also been devoted to developing and fabricating nanolaser architectures employing metal-claddings to downscale cavities, either by leveraging plasmonic resonances or by benefits of the metal in terms of increased reflectance or heat sinking. In this section we will briefly cover both approaches. A recent more comprehensive review on this topic can be found in [171].

### *4.1. Plasmonic or metal-clad emitters*

The direct advantage from using metal in the cavity design is not straightforward and the advantages are offset by increased absorption losses leading to debates about the ultimate benefits of metals in proximity of the active material [172–174]. However, particularly in a nanolaser architecture, achieving electrically modulated lasing will always be critical as this inevitably means approaching contacts to the laser cavity. As there is only a limited number of metal-clad III–V nanolasers we will not restrict ourselves here to locally grown devices on Si as for the rest of the paper. For further information specifically on plasmonic nanolasers in different material systems, there are a couple of excellent reviews [171, 175, 176].

In a surface plasmon polariton laser the mode is highly bound to the interface of the metal and the dielectric gain medium, this can provide for tight confinement and very scaled structures, whereas the proximity of the metal will invariably also lead to high loss. In other structures, generally larger, and using a thicker interface dielectric, the mode is photonic, and the metal may enhance the reflectivity.

Whereas, there are many different metal-semiconductor architectures only a subset of these are truly plasmonic, and it can be difficult to distinguish the nature of the mode unless the cavities are specifically designed to differ between transverse-electric (TE) and transverse-magnetic (TM) polarization [177].

In our own work [134] we investigated microdisk cavities of different dimensions and geometries and explored their properties with and without an Au cladding. Based on simulation, experimental micro-photoluminescence experiments [134], and more recently quantitative Raman thermometry measurements [178] we could establish that the metal cladding serves as a heat sink and has a dramatic effect on device temperature. Therefore, metal-clad devices, as expected, presented higher thresholds but may be scaled to smaller dimensions than their purely dielectric counterparts. Figure 11 depicts the main experimental findings related to this work: figure 11(a) shows the emission spectra of a 400 nm wide cavity with and without a metal-cladding at low and high excitation energies: Only the metal-clad cavity exhibits resonant emission [134]. Cavity temperatures extracted by Raman thermometry match well with simulated device temperature, revealing that the metal-cladding reduces the temperature inside the cavity by up to 450–500 K (see figure 11(b)) [178]. In the simulated temperature distribution shown in figure 11(c), one can see that the heat generated inside the bare InP cavity cannot escape efficiently due to the underlying $SiO_2$ layer, which serves as an optical insulator. For the metal-clad cavity, however, the generated heat can be transferred from the InP due to the Au side-walls [134].

In terms of electrical actuation, a breakthrough in 2007 was demonstrated on Au-covered III–V NWs supporting a dielectric mode [179]. Due to high metallic losses, only lasing at very low temperatures of about 10 K was demonstrated. Nevertheless, this was for a scaled device with a diameter of only 260 nm. By the use of Ag instead of Au encapsulation and a nano ridge structure, the authors also demonstrated pulsed electrically actuated lasing, for the first time with plasmonic modes in [180]. The design was further improved by the etching of DBR in the nano ridge structure in [181]. A couple of years later in 2012 [182] and 2013 [183] Ding *et al* demonstrated for the first time room temperature electrically actuated cw lasing at 1591 nm from an Ag-clad InP/InGaAs rectangular cavity, showing the continued potential of this architecture.

The proximity of the metal to the cavity makes efficient out-coupling of the light in an integrated scheme even more challenging. To overcome this in [184] a metal-clad vertical NW coupled to an underlying InP waveguide is demonstrated. Although only operated as a LED and not as an electrically actuated laser, it is still an important step towards sub-micron scaled on-chip emitters. Furthermore, one may argue that possibly for plasmonic nanolasers LED emission might be preferred if the communication distances are sufficiently short [173].

Lastly, it should be noted that nanocavity lasers can exhibit spontaneous emission factors ($\beta$) close to unity, as for example in the coaxial nanocavity shown in figure 11(e) [185]. This results in light-in-light-out curve exhibiting a *threshold less* like behavior, i.e. the transition between LED operation and lasing is a soft one. This further complicates the experimental verification of lasing since further studies on carrier lifetime and photon statistics are needed.

Based on various experimental results, a fully metal-clad structure undoubtedly improves scalability, but also leads to an increase in threshold as a result from the metal losses, which for presently known materials are still high in the near-IR region of interest. Therefore, it is pertinent to explore alternative routes.

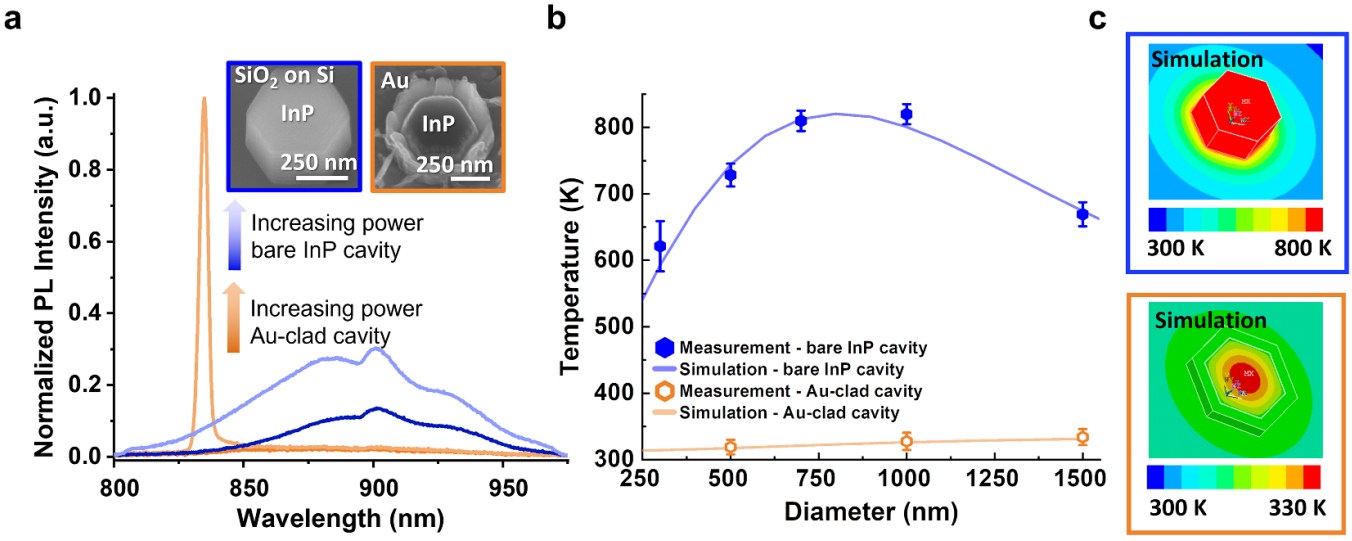


**Figure 11.** (a) Spectra for a 400 nm wide InP cavity without (blue) and with Au-cladding (orange) at low and high excitation powers. (b) Simulated temperature (solid lines) and temperature derived from the Raman peak broadening (points) of micro- and nanocavities without (blue line, solid shapes) and with Au-cladding (orange line, hollow shapes). (c) Thermal simulations of the temperature distribution of a InP cavity assuming constant pumping of the same average power as used in the experiment for a cavity without (top, blue) and without (bottom, orange) Au-cladding. Adapted with permission from [135] © The optical Society.

## 5. Conclusion

In this paper we provide a general overview of the opportunities and challenges for scaled emitters integrated on silicon. Monolithic integration on silicon is primarily of interest for photonic devices for on-chip applications and to this end we focused on devices emitting within or close to the important telecom bands in the near-infrared (NIR) which would be suitable for the implementation of transparent Si passives. Rather than an exhaustive review of all the works in this area, we put the focus on the aspects which we believe to be of importance and provide a general overview of the different techniques. We have discussed different approaches for monolithic III–V integration on Si with a special emphasis on TASE as this is the method pursued by our group. TASE is unique in that it replaces existing Si features and hence allows for self-aligned structures with in-plane doping profiles and heterostructures.

Then we discussed different types of cavity architectures. An interesting aspect of nanolasers is that often the device geometry and type of lasing cavity is intrinsically related to the material integration approach. Such that harvested NWs directly provide for a FP-type cavity when placed on another substrate or that by a proper choice of growth parameters and wafer orientation we may directly grow a hexagonal microdisk using TASE, which will support a WGM. Hybrid PhC cavities are promising, due to their potential for low mode volumes and straightforward waveguiding schemes. The recent demonstrations on tuneable resonances in PhC cavities and waveguide coupled photodetection using TASE lay a fundament to more advanced demonstrations toward a full optical link.

Lastly, we can conclude that in the field of nanolasers many challenges remain to be addressed. A plethora of novel device designs are being proposed and it is an extremely dynamic and fast-moving field, but this is what makes it such an exciting topic to work on.

## Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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