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# Reliable Gate Driving of SiC MOSFETs With Crosstalk Voltage Elimination and Two-Step Short-Circuit Protection

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# Reliable Gate Driving of SiC MOSFETs with Crosstalk Voltage Elimination and Two-step Shortcircuit Protection

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***Abstract*—The over-stress of the negative gate-source voltage of SiC MOSFET, even in a short period of time, could cause the threshold voltage drift of the device, resulting in increased on-state resistance. In this paper, we propose an integrated gate driver to specially limit the peak negative gate voltage of SiC MOSFETs introduced by the crosstalk phenomenon and the reliable short-circuit protection. A simple auxiliary branch with bidirectional blocking capability is adopted in crosstalk voltage suppression and the negative peak voltage of the gate, introduced by common source inductor, is eliminated by the high impedance gate driving loop. Furthermore, the auxiliary circuit is reused to assist a two-step short-circuit protection of the device by identifying dc-link shoot-through current on the stray inductor. By rapidly reducing the gate-source voltage to a lower value when short-circuit happens, the short circuit withstanding time of the device is prolonged, enabling a longer allowable detection time to confirm the fault event accurately. The proposed method comprehensively integrates the crosstalk voltage suppression and short circuit protection together and is verified by the experiments.**

***Index Terms*—SiC MOSFETs, short-circuit protection, crosstalk voltage, reliability, threshold voltage drift**

## I. Introduction

SIC MOSFETs are rapidly growing in power processing due to their superior performances in high frequency, high voltage and high-temperature converters. With the growing applications, the reliability issues related to gate driving are becoming more and more critical. The threshold voltage ($V_{th}$) drift phenomenon of SiC MOSFET is one of the challenges that need to be adequately considered for these devices to be widely deployed in power converters. Threshold voltage drift refers to the variation of the threshold voltage of the power device after accumulation of voltage stress of the gate-source oxide [1] [2]. It is a common phenomenon that is widely recognized in power devices, including SiC MOSFETs and Si devices. However, compared with Si devices, the threshold voltage drift of SiC MOSFET is much more obvious due to the defects in the gate-oxide of SiC MOSFETs [3]. Such defects are intrinsic and can be found in all types of SiC MOSFETs, regardless of the planar or trench MOSFET technology [4]. The mechanism behind this phenomenon and the methods to improve it are ongoing hot topics that still need further exploration.

It has been confirmed that $V_{th}$ is obviously shifted to a higher value after a certain amount of switching cycle for SiC MOSFETs [5]. Several factors contribute to such phenomenon, including turn-off gate-source voltages, temperature and switching frequency [4], [6]–[8]. To make things worse, only a short period of overstressing of the gate driving voltage still introduces the significant threshold voltage drift [9]. Therefore, it is of vital importance to control the negative peak of the gate-source voltage to achieve the targeted lifetime of the power devices. However, the negative gate-source voltage is necessary to prevent the potential false turn-on of the device in a phase leg circuit. As a consequence, there exists a contradiction between reliability enhancement and avoiding the potential false turn-on of the device, especially in medium voltage and high voltage converters.

Conventionally, the crosstalk voltage suppression mainly focuses on avoiding the false turn-on of the device. The miller clamp method is widely adopted [10]. Although there exist different realizations, the main idea is to add an extra low impedance branch to suppress the displacement current from the gate-drain capacitor. In [11], it has been pointed out that the crosstalk voltage is influenced by the common source inductor and the low impedance of clamping circuit even increases the negative gate-source voltage. The negative voltage introduced by the common source inductor, together with the steady-state negative gate-source voltage, may cause overstress of the gate-source oxide of the device, bringing reliability issues [12].

Another important consideration for the gate driver is the short-circuit (SC) protection. Due to a smaller size of the chip and relatively large short circuit current, the survivable time of SiC MOSFETs is much shorter than Si IGBT. In general, the short-circuit time of mainstream commercially available devices is not guaranteed (even not provided in datasheet), especially at high gate-source voltage conditions. The de-saturation (DESAT) protection methods are the most widely adopted method in short-circuit protection [13] [14]. To avoid the influence of the switching transition on the DESAT protection, a period of time, called blanking time, is normally inserted to bypass the short-circuit detection circuit for a piece of time. However, whether DESAT circuit can be directly adopted in short circuit protection of SiC MOSFETs is questionable. Firstly, there is no apparent saturation current

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('knee current') for SiC MOSFETs, which means SC current can rise extremely high. Secondly, a fast detection circuit is required to reduce the short-circuit detection time. However, such a circuit is sensitive to the noise generated by the switching. There exists a trade-off between the short-circuit reaction time and the noise immunity. In [15] [16], a short-circuit protection is proposed to detect the short-circuit and has higher short-circuit capability by reducing the gate-source voltage. In this solution, the voltage dip on the dc link is adopted to indicate the short circuit event and quickly clamp the gate-source voltage to a lower value. The solution needs special consideration for converter with multiple phase legs and layout design for high voltage sensing.

In this paper, we propose a simple gate driving solution to realize effective crosstalk voltage suppression and short-circuit protection. The negative voltage generated by the gate loop and power loop coupling inductance is eliminated and only the gate-source voltage from the gate-drain capacitor is considered. In the proposed design, the extra parallel branch in crosstalk voltage suppression and short-circuit protection can be multiplexed with proper parameter design. The paper is organized as follows, in section II, the operation principles of crosstalk voltage suppression are given. In section III, the short-circuit protection circuit is analyzed and in section IV, the parameter selection of the clamping resistor is discussed in detail to achieve the balance between crosstalk voltage suppression together with the short circuit protection. Then the proposed method is verified by experiment.

## II. Crosstalk Voltage Elimination Principles

The proposed brief diagram of the circuit is given in Fig. 1a. There are several considerations in the gate driving of SiC MOSFETs. Normally, the crosstalk voltage suppression is functioning during the off-state of the device and short-circuit protection happens during the on-state of the device. With proper design, the auxiliary branch in crosstalk voltage suppression can be adopted in short circuit protection as well. Therefore, multiple usages of the clamping circuit are possible to simplify the gate driver structure. Besides, circuit for DESAT protection is still presented with the highest priority in protection.

### A. Operation Principle of Crosstalk Voltage Elimination

Fig. 2 gives a more detailed realization of the aforementioned scheme in Fig. 1a. The proposed scheme consists of three main parts. The first part is the crosstalk voltage suppression logic circuit, including on-delay, off-delay and pulse generator. The second one is the short-circuit detection circuit, including stray inductor $L_{s2}$, a bandpass filter for $V_{Ls2}$ and a comparator. The third one is the bidirectional blocking clamping switch, which contains anti-series connected p-MOSFETs and the control circuit. The DESAT circuit in Fig. 1a can be from the widely adopted solutions, and it is neglected here. In the diagram, PWM signal is from the upper-level controller. The driving power supply includes high voltage $VCC$ and low voltage $VEE$ (negative value). The source terminal of the power device is connected to $GND$.

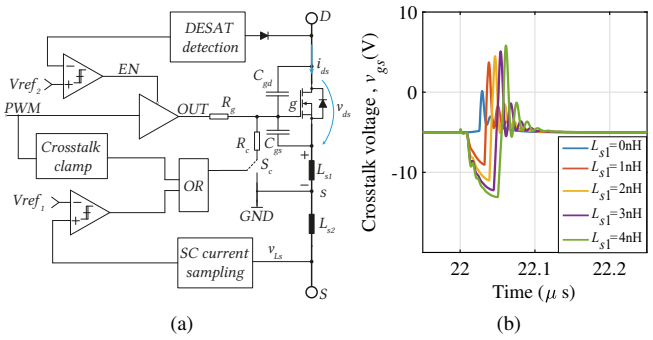


Fig. 1: (a) Structure of the proposed gate driver with crosstalk voltage suppression and short-circuit protection. (b) Simulation of the crosstalk voltage when the other device in the same phase leg is turned on (cases for $i_{ds} < 0$), with simulation models from device manufacturer.

All the voltage potential references of the signal circuit are referred to $VEE$.

There are two types of crosstalk voltages, introduced by the gate-drain capacitor $C_{gd}$ and the common source inductor $L_{s1}$ among the gate loop and power loop, as shown in Fig. 1a. To be suppressed, they demonstrate completely different requirements on the off-state loop impedance of the gate driver. $C_{gd}$ introduced crosstalk voltage requires lower gate loop impedance to reduce the influence on the gate-source voltage, which can be realized by a lower impedance path (e.g., Miller clamp circuit) to bypass the gate resistor $R_g$. Meanwhile, the common source inductor introduced crosstalk voltage requires a higher gate loop impedance to isolate the voltage from the gate-source capacitor, which can be worsened by Miller clamp circuit. For a typical case, when another switch in the phase leg is turned on, the absolute value of drain-source current $i_{ds}$ will decrease first, which causes a negative voltage overshoot on $L_{s1}$ [12]. Together with $VEE$, the gate-source voltage is reduced to a lower value than the steady-state off-state voltage, which may be harmful to the gate-oxide reliability even in a short period of time [4], [6]–[8]. Then when the device voltage $v_{ds}$ increases, there will be a voltage step-up on the gate-source voltage. As an example, simulation of crosstalk voltage, using

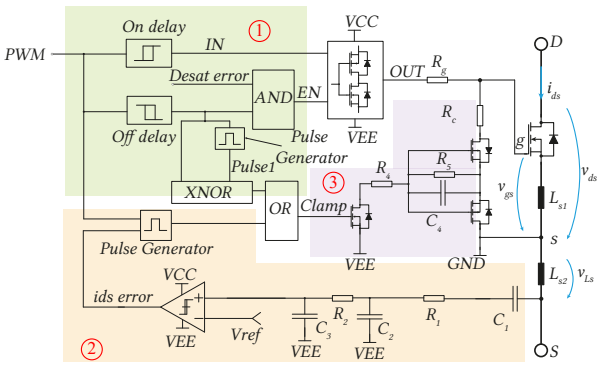


Fig. 2: A detailed implementation of the proposed gate driver.

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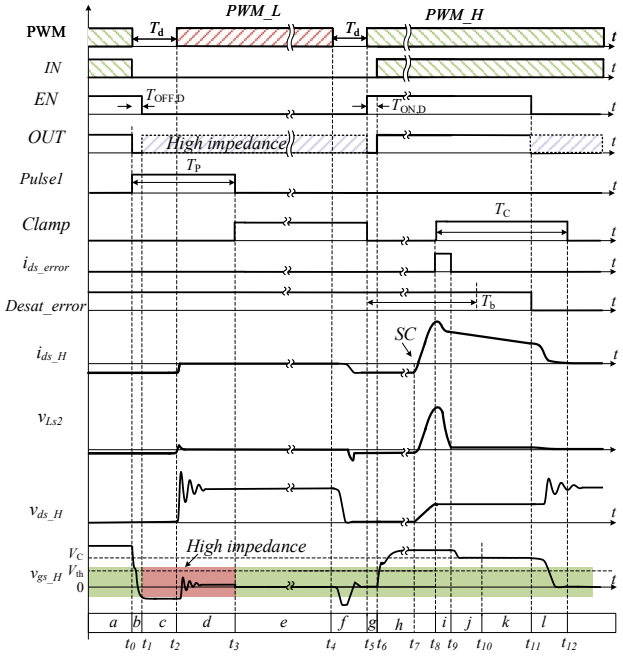


Fig. 3: Time sequence of the proposed gate driver.

spice models from the device manufacture, is shown in Fig. 1b [11]. The higher the common source inductor, the lower the off-state negative gate-source voltage.

In some device packages, the common source inductor is relatively small with a separate gate driving loop (e.g., auxiliary source terminal). However, even if the auxiliary source terminal is adopted, the coupling between the gate loop and power loop still exists [12] [17]. For example, if $L_{s1} = 1\,\mathrm{nH}$, when the current slew rate during turn-off is $5\,\mathrm{A/ns}$ , there will be at most $5\,\mathrm{V}$ decreasing of the gate-source voltage (the gate loop impedance is not considered), which adds extra negative stress to the gate capacitor.

### B. Time Sequence of Crosstalk Elimination

The time sequence of operation is given in Fig. 3. In the following section, the crosstalk voltage suppression during off-state will be discussed first. The high side device in a phase leg configuration is used as an example. At the beginning, the device current $i_{ds}$ is negative.

$0-t_0$: In Fig. 3, before $t_0$, PWM signal of high side device is in the high level and the gate-source voltage $v_{gs\_H}$ is equal to the high side supply voltage $VCC$. $EN$ is the enable signal of the output stage of the gate driver $OUT$. When $EN$=1, the output stage follows the input PWM signal and if PWM =1, the output voltage is $VCC$. If PWM = 0, output stage is connected to $VEE$. When $EN$ is low, the output signal $OUT$ is in high impedance state. The enable/disable functions of the output stage can be widely found in commercially available gate driver chips.

$t_0 - t_1$: At $t_0$, PWM signal switches to zero. At the same time, $OUT$ switches to a lower value, the device starts to turn off and the gate-source voltage begins to decrease. After turn-off time, the gate-source voltage is decreased to the negative value $VEE$. In this stage, the gate loop impedance is in the low state due to the output stage being connected to $VEE$ with low resistance. After a piece of delay time $T_{OFF,D}$, $EN$ falls to zero. $T_{OFF,D}$ needs to be slightly larger than the turnoff time of the power device in the worst case. At $t_1$, the gate capacitor voltage is decreased to $VEE$.

$t_1 - t_2$: At $t_1$, $EN = 0$, the $OUT$ is in high impedance off-state. In this stage, the gate-source voltage keeps in the low state until the dead-time period $T_d$ ends. Then the other device in the phase leg ($PWM\_L$) will be turned on at $t_2$. In this stage, to be able to block the voltage of the $L_{s1}$ to the gate-source capacitor, only the high impedance of the output voltage is not enough ($EN = 0$). The impedance of the clamping switch should also be high as well. In Fig. 1a, the bidirectional switch is composed of two back-to-back connected p-MOSFETs, and the switching is controlled by a n-MOSFET. When the clamping signal $Clamp$ is high, since GND is higher than VEE, the gate-source voltage of p-MOSFET will be negative and the two p-MOSFETs will be turned on. Compared with the solution in [11], one clamp signal is enough to control the device and no isolated power supply and control signals are required for the two p-MOSFETs. As a result, the circuit is greatly simplified. In this stage, since the bidirectional switch in Fig. 1a is in the bidirectional blocking state, the gate loop impedance is in the high-impedance state. Therefore, any current changes on the common source inductor will not be transferred to the gate-source capacitor. The crosstalk voltage introduced by common source inductor is fully eliminated.

$t_2 - t_3$: When the dead-time ends, the other device in the phase leg will be turned on. The drain-source voltage of the device $v_{ds\_H}$ will increase to the dc link voltage. As a result, the gate-source capacitor will be charged by the displacement current from the gate-drain capacitor. Since negative gate-source voltage has been pre-charged to $VEE$, with proper selection of the parameter, the induced gate-source voltage can be controlled below the threshold value [11]. Besides, the selection of $VEE$ should also consider the lifetime of the device under certain switching frequencies, which can be acquired from the device manufacturers [4]. Then after a certain period of time, at $t_3$, the clamping switch will be turned on again to form a low impedance gate loop during the off-state, avoiding the floating gate-source capacitor. $Clamp$ signal is from a pulse generator, which is triggered after a pre-defined period of time when $PWM$ steps to low value.

Since the p-MOSFETs are turned on by the voltage drop across the $R_5$, sufficient voltage sharing among $GND$ and $VEE$ should be provided to fully turn on the device. Assume the threshold voltage of p-MOSFET is $V_{th,p-mos}$, following condition should be satisfied

$$\frac{R_5}{R_4 + R_5}(-VEE) > V_{th,p-mos} \tag{1}$$

On one hand, to increase the response speed of the clamping circuit, $R_4$ and $R_5$ should be selected as small as possible. On the other hand, lower resistance brings higher power dissipation. The parameter selection can be achieved with the above mentioned trade-off. For $C_4$, the idea is to reduce the

influence of the switching noise in the circuit, which is not mandatory in the design.

The duration of $t_0 - t_3$ is $T_P$, which can be achieved by configuring the pulse generator. The duration of the $T_P$ should be as less as possible to avoid the floating gate-source capacitor of the power device but should be long enough so that another switch is completely turned off. Therefore

$$T_P > T_d + T_1 + T_0 \tag{2}$$

where $T_1$ is the total turn-on transient time of another device, which include turn-on delay time, current rising time and voltage falling time; $T_0$ is the margin adopted in the design.It should be pointed out that the off-state pulse duration of the device should be higher than $T_P$ to ensure the turn-off of the clamping switch before the device is turned on. Therefore, the duty cycle of the device should be selected within a certain range to avoid very small duty cycle and very large duty cycle, with $T_P$ counted into the dead-time period.

$t_3 - t_4$: The device is in the off-state until the other device in the phase leg is turned off at $t_4$.

$t_4 - t_5$: From $t_4$, the drain-source voltage starts to drop and the absolute value of the drain-source current starts to increase. Ideally, the gate loop impedance should also be in the high state to prevent the potential influence from the common source inductor, which means $Clamp$ signal should be off when $PWM\_L$ is off. However, due to the clamping switch is still on, the gate loop impedance is still in low impedance state. It is hard for the high-side gate driver to predict when to turn off the clamping switch since the gate driving signal of $PWM\_H$ has no information from the complementary switch $PWM\_L$, supposing that deadtime is generated by the central controller. To simplify the gate driver structure, the low impedance gate loop is still kept in the proposed solution. With proper selection of the clamping resistor, it is possible to control the crosstalk voltage to be within a reasonable range.

$t_5 - t_6$: When the deadtime ends, the upper device is supposed to be turned on. When the gate driver receives $PWM$ from the upper controller, $T_{ON,D}$ is generated by the rising edge delay of the input PWM signal $PWM$. As a result, the input signal of the gate driving amplifying stage $IN$ is slightly delayed. $T_{ON,D}$ is to ensure that the clamping switch is turned off before the turn-on of the device. $T_{ON,D}$ is typically in the range of tens of nanoseconds and has less influence on the duty cycle loss of the switching. Then the device will be turned on and any logic related to crosstalk voltage elimination will be disabled.

## III. Short-circuit Protection

In the proposed design, the conventional DESAT detection method is still required. Such method is used to detect the voltage drop across the device and if it is higher than a certain value, the device is turned off. Since there exists a blanking time in the detection, the SC current can still go very high.

To solve the challenge, another piece of information is added and a two-step protection method is adopted. Firstly, the current passing through the loop stray inductor $L_{s2}$ is sensed. Such inductor can be from the stray inductor from the auxiliary source terminal and the power terminal of the device. The stray inductance must be acquired in advance from calibration test or from FEM simulation. When the short circuit current is higher than a certain value, the gate-source voltage is clamped to a lower value rapidly. Therefore, the SC current is reduced by the reduced gate-source voltage [18]. Then after a certain period of time, the fault will be detected by DESAT circuit and the device will eventually be turned off. Since short-circuit only happens during the on-state of the power device, in Fig. 2, the output of the pulse generator is also controlled by the PWM signal to completely block short-circuit protection during the off-state of the device.

In some cases, the $V_{Ls2}$ detection circuit may be triggered by the noises inside the circuit. Such false detection can be cleared by the DESAT circuit with the relatively low response speed. If the DESAT circuit is activated, the device will be turned off. If there is no short-circuit protection event, the gate-source voltage will be released and the converter's normal operation will not be interrupted. Such protection scheme is beneficial to achieving ultra-fast detection as well as reliable short-circuit protection. In the following analysis, the high-side device is turned on into short circuit, as an example.

$t_7 - t_8$: In Fig. 3, before $t_7$, the phase leg is under normal operation. At $t_7$, SC happens and the drain-source current rises dramatically in a short period of time. A high voltage drop occurs at $V_{Ls2}$ owing to the high $di/dt$ of the current. With proper configuration of the sensing circuit, the output voltage of the filter $v_{Ls2}$ is proportional to the current passing through the stray inductor $L_{s2}$.

In designing the filters of the $v_{Ls2}$ , it is important to filter out the noise generated during switching as well as bypass the disturbance from the normal operation (fundamental frequency and switching frequency related harmonics) [19]. As given in Fig. 2, a passive bandpass filter is adopted in the proposed circuit. Capacitor $C_1$ is used to block the DC components and switching frequency related components. $R_2, C_3$ are used to filter out the oscillations after hard switching of the device. The transfer function of the output of the filter $v_{Ls2}$ and the drain-source current $i_{ds}$ is

$$\frac{v_{Ls2}}{i_{ds}} = \frac{sL_\sigma}{s^2 R_1 R_2 C_2 C_3 + s(C_3 + C_2)(R_2 + R_1) + \frac{C_1+C_2+C_3}{C_1}} \tag{3}$$

In the parameter design phase, it can be determined that $C_1 \gg C_2 \gg C_3$ and $R_1 \gg R_2$. Thus, the corner frequency $f_L$, $f_H$ between the low-frequency range, the medium frequency range and the high-frequency range are approximately calculated as

$$f_L = \frac{1}{2\pi R_1}(\frac{1}{C_1} + \frac{1}{C_2}), f_H = \frac{1}{2\pi R_2 C_3} \tag{4}$$

It is of vital importance to choose the corner frequency of the transfer function to get useful information on short-circuit current as well as to eliminate the unwanted high-frequency harmonics. Considering that there will be DC components and low-frequency harmonics related to the switching frequency, the corner frequency should be selected to be higher than the switching event-generated harmonics. For example, if the switching frequency is 20 kHz, the corner frequency can be

selected as $f_L = 200\,\text{kHz}$ to eliminate the influence of the switching ripple as high as ten times the switching frequency. After switching, the stray inductor and output capacitor of the device starts to oscillate, the frequency range is higher than several Mhz. For example, $f_H = 20\,\text{MHz}$ for a typical case. With the proposed parameters selection, in the medium frequency range, the transfer function can be simplified as

$$\frac{v_{Ls2}}{i_{ds}} \approx \frac{L_\sigma}{(C_2+C_3)(R_1+R_2)} \tag{5}$$

As a result, the output voltage directly reflects the value of the short-circuit current. The output of the filter will be compared with a pre-set value $V_{ref2}$. The threshold value of the comparator is determined by the switching frequency, the device characteristics and the loop parasitic parameters.

$t_8 - t_9$: When the inductor current is higher than a certain value, at $t_8$, the error indicator $i_{ds\_error}$, which is the output of the comparator, will be generated.

$t_9 - t_{12}$: After receiving the short pulse $i_{ds\_error}$ (voltage step-up) from the output of the error comparator, the $i_{ds\_error}$ signal of the device will generate a clamping pulse $Clamp$ to turn on the bidirectional switch with $T_c$ time length. The pulse generator can be a commercially available monostable multi-vibrator that can generate a fixed time pulse based on the input signal. When the $Clamp$ signal is on, the gate-source voltage will be clamped to a lower value since $R_c$ and $R_g$ share the high-level voltage of $OUT$. During this period, depending on whether there will be short circuit error generated from DESAT circuit, two cases may happen:

- case 1: DESAT error detected
  In this case, at $t_{10}$, after the blanking time of DESAT $T_b$ and detection time, DESAT detection is enabled. At $t_{11}$, when the $Desat\_error$ signal is generated, the EN is pulled down to disable the OUT signal. And the device is turned off by the DESAT block from separate circuits (soft-turn off may still present but not mandatory). $PWM\_H$ will remain high for a period of time until the upper-level controller receives the fault signal from the feedback of the gate driver. At $t_{12}$, the clamping switch will be released when the clamping time ends.
- case 2: DESAT error not detected
  Owing to the fast detection circuits, it is highly possible to be falsely triggered by the noises inside the gate driver. The DESAT detection circuit has lower response speed and is not easily disturbed by the noise if a larger filter is added. If there is no error signal generated from the DESAT circuit, at $t_{12}$, after $T_c$ , the gate-source voltage will be increased to the rated value again and operation of the device will not be interrupted.

The duration of the clamping time is a trade-off between the short-circuit withstanding time (SCWT) and the clamped gate-source voltage. Since the saturation current of the power device is directly controlled by the gate-source voltage, the lower the clamped gate-source voltage, the longer the SCWT time. However, a relatively large on-state resistance of the SiC MOSFETs appears in case 2. Fortunately, the clamping signal lasts for a short period of time and the influence on increased loss is relatively small. There are other types of short-circuits as well. The general protection scheme is the same as the analysis before and is ignored here.

## IV. Selection of Clamping Resistor

With high off-state impedance during the turn-on of the another device, the crosstalk voltage is properly limited to a safe window. However, as analyzed before, the crosstalk voltage generated by turn-off of another device should be carefully handled since there is no high-impedance in this state for the sake of simplicity in gate driver. Based on the analysis, the selection of the clamping resistor needs to consider both the short circuit protection requirement (during $t_8 - t_{12}$) and the crosstalk voltage limitation (during $t_4 - t_5$) when other device is turned off. Both conditions must be satisfied under different cases. This section gives a detailed discussion on the selection of the clamping resistor.

Firstly, SC current limit is considered. In $t_8 - t_{12}$, the channel current of the device $i_{ds}$ is

$$i_{ds} = g_m(v_{gs} - V_{th})^2 \tag{6}$$

where $g_m$ and $V_{th}$ can be extracted from the transfer curve of the device datasheet. During SC, the heat generated by SC current and voltage is accumulated and the total value should be lower than the critical energy of the device $E_{SC}$ [20] [21], which can be found from device manufactures or by calibration test. $E_{SC}$ is temperature dependent and the value at the highest ambient temperature should be adopted [22]. Assuming that the gate-source voltage is clamped to the lower value very fast when the device is directly short circuit to dc-link and neglecting the temperature dependence of the $g_m$, the total heat generated is approximately

$$\int_0^{T_c} V_{dc} i_{ds} dt < E_{SC} \tag{7}$$

where $T_c$ is the clamping time, $V_{dc}$ is the dc link voltage. Therefore, the gate-source voltage is

$$V_C < V_{th} + \sqrt{\frac{E_{SC}}{g_m T_C V_{dc}}} \tag{8}$$

It should be pointed out that in reality, $g_m$ decreases with the junction temperature of the device. As a result, the heat accumulation speed decreases as junction temperature increases. (8) is a conservative design in the worst case condition.

The gate-source voltage is the voltage divider between the gate driver resistor $R_g$ and the clamping resistor. $R_c$ satisfies

$$R_c < R_g V_C / (V_{CC} - V_C) \tag{9}$$

where $V_{CC}$ is the turn-on gate-source voltage.

Another important consideration is crosstalk voltage suppression. Taking the voltage drop on the common source inductor into consideration, the crosstalk voltage is generated when the other device is turned off (lower device), as illustrated in Fig. 4. The linear waveform is depicted and the equivalent circuits of the off-state devices are given at different switching stages of the active device. Firstly, in stage $s_1$ in Fig. 4, the lower device in the same phase leg is turned off, the drain-source voltage of the higher device is decreased to zero.

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$$V_{gs-off,peak} = \left(\frac{L_{s1}(I_L - 2I_{OSS})}{t_{s2}}\right)\left(1 - e^{-\frac{t_{s2}}{R_C C_{gs}}}\right) + \left(\frac{2L_{s1}I_{OSS}^2}{Q_{OSS}} - \frac{R_C C_{gd} I_{OSS}}{C_{gd} + C_{ds}}\right)\left(1 - e^{-\frac{Q_{OSS}}{R_C C_{gs} I_{OSS}}}\right) e^{\frac{-t_{s2}}{R_C C_{gs}}} \quad (10)$$

$$\frac{2L_{s1}}{Q_{OSS}R_g} I_{OSS}^2 + \left(\frac{C_{gd}}{C_{gd} + C_{ds}}\right) I_{OSS} - \frac{1}{R_g}\sqrt{\frac{I_L - 2I_{OSS}}{g_m}} + \frac{V_{EE} - V_{th}}{R_g} = 0 \quad (11)$$

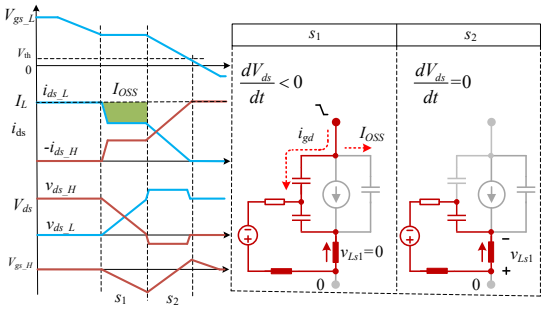



Fig. 4: Modeling of the crosstalk voltage when the lower device is turned off.

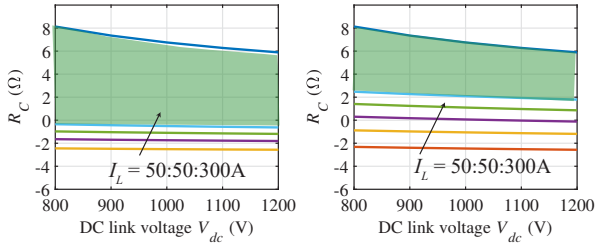



Fig. 5: Range of clamping resistor under difference $V_{dc}$ and load currents. Device data is cas300m17bm2 (1700V/250A) from CREE. (a) $L_{s1} = 1\text{nH}$ and (b) $L_{s1} = 2\text{nH}$.

The displacement current from the gate-drain will discharge the gate-source capacitor, as indicated in stage $s_1$. Secondly, following the voltage decreasing transition stage, $|i_{ds}|$ will rise to the load current $I_L$. The negative voltage drop across the common source inductor $L_{s1}$ introduces a positive voltage into the gate-source loop, as indicated in stage $s_2$. The peak crosstalk voltage happens at the end of this stage and should be lower than the threshold voltage of the SiC MOSFETs. It should be noted that there may be negative spikes at the end of the stage $s_1$. Since the peak negative voltage at this stage is within the safe operation value for most cases [11], it is ignored in the following discussion.

In the following analysis, the analytic model from [11] is adopted to calculate the peak crosstalk voltage generated by the turn-off of the another device, which considers the influence of the charging current of the output capacitors $I_{OSS}$ as well. The maximum crosstalk voltage is (10). Where $I_L$ is the maximum load current; $Q_{OSS}$ is the charge stored in the output capacitor of the device, which can be found from the capacitor-voltage curve in the datasheet; $C_{gd}$, $C_ds$ is the drain-source capacitor at the blocking voltage of the device. These parameters can be found in the datasheet of the device. $I_{OSS}$ is the capacitor averaging discharging current, which can be found by solving (11). In (11), $t_{s2}$ is the duration time of the second stage in Fig. 4, in which the voltage decrease from the miller plateau voltage to the threshold voltage. In this stage, since there is no displacement current from the gate-drain capacitor, the duration of $s_2$ is purely the discharging time of gate capacitor. $t_{s2}$ is

$$t_{s2} = \left(R_g C_{gs} + \sqrt{g_m(I_L - 2I_{OSS})}L_{s1}\right)\ln\left(\frac{V_{th} - V_{EE}}{V_{miller} - V_{EE}}\right),$$
$$V_{miller} = V_{th} + \sqrt{\frac{I_L - 2I_{OSS}}{g_m}} \quad (12)$$

where$V_{EE}$ are positive and negative gate driving voltage.

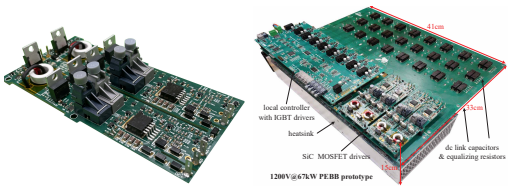
In the selection of the clamping resistor, the target is to limit the crosstalk voltage to be lower than the threshold value of the device at the end of $s_2$ in Fig. 4.

$$V_{gs-off,peak} < V_{th} - V_m \quad (13)$$

where $V_m$ is the margin selected in the design. For example, $V_m = 1.0\,\text{V}$ can be selected. At a given voltage and current, a minimum clamping resistor can be found from (13). Together with (9), which is the maximum value of the clamping resistor, the range of the clamping resistor can be decided. An example of the range of the resistor is given in Fig. 5a. The device data is from CREE 1700V/250A datasheet and the switching current is at 300A. The selection of clamping resistor must be within the shadow area. In the calculated module, the common source inductance is relatively small, around $L_{s1} = 1\text{nH}$. The negative value means no additional external clamping resistor is required in terms of the crosstalk voltage elimination. In another case, when $L_{s1} = 2\text{nH}$ is adopted for the same device, the influence of common source inductance is more obvious and a narrow range is demonstrated.

## V. Experimental Verification

A gate driver based on the presented principles is built and verified in this section. The designed gate driver is targeted for




(a) (b)

Fig. 6: (a) Photo of the gate driver; (b) Photo of the 1.2kV/67kW experimental setup.

TABLE I: Parameter design results.

| Description and Symbol | Value/Range |
|---|---|
| $L_{s2}$, $L_{s1}$ | 1.6 nH, 1.0 nH |
| $C_1, C_2, C_3$ | 100 nF , 1 nF , 0.047 nF |
| $R_1, R_2$ | 0.1 kΩ , 6.81 kΩ |
| $T_d, T_{OFF,D}, T_{ON,D}$ | 1000 ns, 350 ns, 15 ns |
| $V_{clamp}$ | 8.0 V |
| $V_{CC}/V_{EE}$ | 20.0 V/−6.0 V |
| Gate driver IC | IXDD630MYI |
| $R_{g,on}/R_{g,off}$ | 2.6 Ω/3.6 Ω |
| $R_4/R_5$ | 4.5 kΩ/ 0.5 kΩ |
| $p\_MOS/n\_MOS$ | IRLML5103/IRLML0040 |
| $T_w$,$T_b$, $T_P$ | 3.0 µs, 1.2 µs,2.0 µs |

the industrial 1.7 kV 62 mm packages, which is a standard package that can be widely found nowadays. The prototype is demonstrated in Fig. 6. The list of the key parameters is given in Table I. The symbols in the table are the same as in Fig. 2. The stray inductor between the auxiliary source terminal and power source terminal is utilized as the current sensing inductor in the proposed gate driver. Except for the parts for the proposed short circuit and crosstalk elimination, other parts, such as the auxiliary power supply and optic fiber, are using the traditional solutions and neglected here for the sake of simplicity.

### A. Gate driver waveform of double pulse test

Fig. 7 demonstrates the waveform of the proposed gate driver at 1.2 kV/250 A switching condition. The lower device in the phase leg acts as the active device and an inductor is connected in parallel with the upper device. The two gate signals for the upper and lower devices are complementary, with 1 µs deadtime inserted. When the lower device is turned on at 5 µs, the inductor current starts to increase. At 24 µs, the lower device is turned off. The dynamics is accordingly demonstrated in the period in $t_4 - t_5$ in Fig. 3. The gate-source voltage of the upper device is in the proper range thanks to the proper selection of the clamping resistor. It should be pointed out that the actual gate-source capacitor voltage cannot be directly measured owing to the parasitic parameters and the internal gate-source resistance. There exist error in the measurement. Judging from the current waveform, there is no false turn-on of the device.

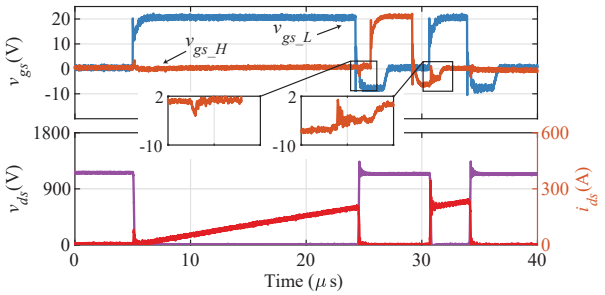
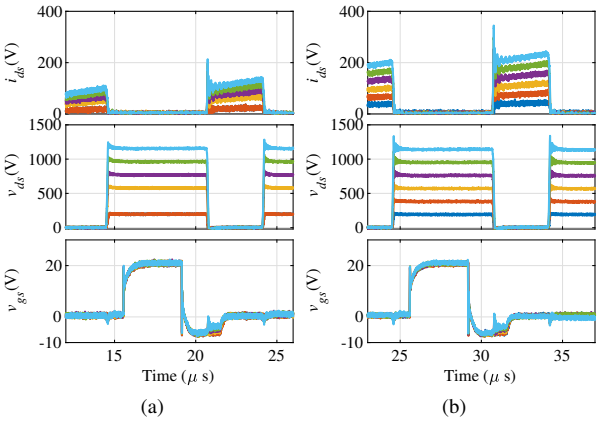



Fig. 7: The waveforms at 1.2 kV/250 A double pulse test.

At 29.0 µs, the upper device is turned off and the anti-parallel diode clamps the drain-source voltage. There will be no voltage step over the device. At 30.2 µs, the lower device is turned on. There is a drain-source voltage step-up in the upper device, as indicated in $t_2 - t_3$ in Fig. 3. Therefore, a voltage step-up across the gate is observed on the measured gate-source voltage, from −6.0 V to 0.5 V. After 0.5 µs, the gate-source voltage is clamped to zero again. The double pulse test result verifies that the proposed gate driver works fine under the inductive switching condition.

### B. Crosstalk voltage at different voltages and currents

Using the same parameters in Table 1, the crosstalk voltage under different currents and different voltages are given in Fig. 8. During the test, the dc link voltage is increased from 200 V to 1200 V. The pulse duration is at 5 µs and 20 µs. Different combinations of voltage and current are demonstrated in the figure. It can be seen that, when the load current changes while the dc link current keeps at the same, the crosstalk voltage keeps almost the same. Whereas the crosstalk voltage changes with the dc link voltage. Under any conditions, the induced crosstalk voltage is well managed to below the threshold voltage. And the negative voltage is higher than −6 V under any conditions.




(a) (b)

Fig. 8: Crosstalk voltage at different lengths of pulses. (a) Crosstalk voltage at 5 µs; (b) Crosstalk voltage at 20 µs.

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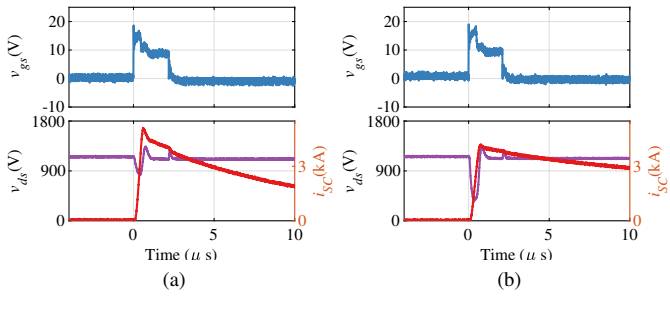


Fig. 9: Short circuit protection of the SiC MOSFETs under low and high SC inductance conditions. (a) 2 nH and (b) 400 nH.

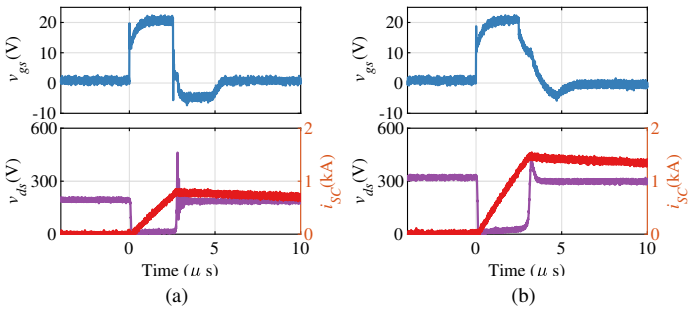


Fig. 10: Over circuit protection of the SiC MOSFETs when SC inductor is 1 µH. (a) Protection does not trigger at 900A and (b) DESAT protection is triggered at 1.4 kA.

### C. Operation under fault condition

When SC happens, the gate driver should be able to limit the fault current and safely turn off the power device. To verify the effectiveness of the proposed method, the short circuit under different inductance are tested. SC is conducted by directly connecting the device to the dc link capacitor through busbar or cables. The result is demonstrated in Fig. 9a and Fig. 9b. When short circuit inductance is around 2 nH, the SC current increases to 5.3 kA in a short period of time. The SC current across the stray inductor is detected and compared with the preset value. The total detection and reaction time is 350 ns, which is similar to the response speed of using Rogowski Switch-Current Sensor in [18] and much faster than DESAT protection. Then the gate-source voltage is clamped to 8.0 V. The high voltage across the device is detected by the DESAT protection circuit, and the device is turned off. When there is a high SC inductance, the current rising slew rate is much smaller. The proposed method can still detect the SC event. But the SC event is detected slower than the direct SC condition, around 400ns at 400 nH.

Another important consideration is the over-current protection (OCP) of the device. To test the behavior of the gate driver under high inductance conditions, a 0.75 µH inductor is inserted into the circuit. The test results at 250 V and 300 V are demonstrated in Fig. 10a and Fig. 10b. It can be seen at 900 A, the SC is not triggered by either the clamping circuit or the DESAT detection. At 1.5 kA, the protection is activated and successfully turn off the power device. It should be pointed out that in this case, the device is turned off with a large turnoff resistor by the DESAT protection. The value of the OCP can be designed by setting the proper value of the DESAT threshold. In the proposed scheme, DESAT is more effective in identifying the over current.

### D. Crosstalk Voltage mitigation comparison

It is difficult to measure the gate-source voltage directly owing to the parasitic parameters inside the power module. Therefore, to compare the crosstalk voltage suppression among different solutions, extra common source stray inductance is intentionally inserted into the gate loop. As demonstrated in Fig. 11b, extra inductance is from stray inductor between auxiliary source terminal and power source terminal. Afterwards the gate-source voltage is measured between the gate terminal and the auxiliary source terminal of the package, as demonstrated in Fig. 11. It should be pointed out that in this case, the actual gate-source voltage is still not accessible. Nevertheless, the limitation of the miller clamping method can still be observed. For the configuration of the Miller clamp circuit, as demonstrated in Fig. 11a, when the device is off-state, the gate terminal is connected to the negative gate-source terminal with the clamping switch. The gate loop is in the low impedance to bypass the gate turn-off resistor $R_{g,off}$ of the device. $v_{gs,Miller}$ is the measured gate-source voltage. In the proposed method, as demonstrated in Fig. 11b, GND is connected to the power source terminal of the package. $v_{gs}$ is the measured gate-source voltage, $v_{gs,Ls}$ is the measured gate-source voltage including the voltage drop across the inserted $L_{s2}$.

The test results are shown in Fig. 12. To avoid the risk of damaging the gate-source of the device, the waveform is measured at 600 V / 200 A. At high gate loop impedance condition, the peak to peak voltage of $v_{gs,Ls}$, which includes the gate-source voltage and voltage drop across the stray inductor $L_{s1}+L_{s2}$, is around 45 V. When the Miller clamp is adopted, the peak-to-peak voltage is decreased to 32 V. And the extra stray inductor $L_{s2}$ has an obvious influence on the measured waveform. In the proposed method, the gate-source voltage, which contains gate-source capacitor voltage and the voltage drop across the $L_{s1}$, is 22 V. Comparing $v_{gs,Ls}$ and $v_{gs}$, the peak-to-peak voltage is significantly reduced. The difference is the voltage drop across $L_{s2}$. Besides, although the auxiliary source terminal is adopted in high power modules, the influence of $L_{s1}$ is still not eligible if a low impedance gate loop is adopted. Since the gate-loop is in the high-impedance state, the influence of $L_{s1}$ can be bypassed in reality as well.

### E. Short circuit Protection comparison

The comparison between the DESAT protection and the proposed two-step SC protection are given in Fig. 13. To ensure the safety of the SiC device, the test is conducted at 300 V dc-link voltage with low SC inductance condition. When SC happens at DESAT protection, the SC current rises

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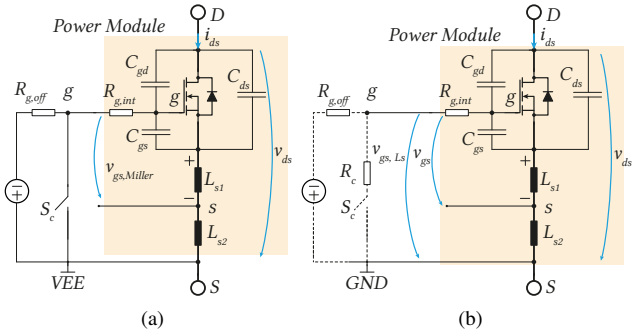


Fig. 11: Circuit diagram and measurement setup of the (a) gate driver adopting Miller clamp and (b) proposed gate driver.

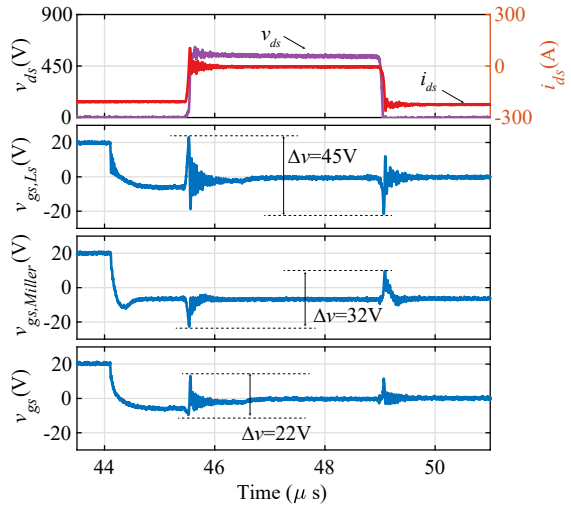


Fig. 12: Comparison of the probe measured gate source voltage at different conditions.

to 4.1 kA, which is more than 16 times the rated current. And after around 2 µs, the device is softly turned off. When two-step protection is adopted, the SC current is around 2.0 kA, which is much smaller than DESAT protection method. The peak device voltage is higher than DESAT condition due to the lack of the soft turn-off function. Nevertheless, it is still within the safe operation area of the SiC device (even at the rated voltage condition). Since the SC current is greatly reduced, the longer SC withstanding time of the power device can be guaranteed.

### F. Continuous switching test result

In this part, the converter operates in a continuous switching state is given to verify the proposed solution, as demonstrated in Fig. 14. The zoomed waveform at 0A and 140A are also given. In the test, the dc-link voltage is 1.2 kV, the switching frequency is 20 kHz, and the load AC current $i_L$ is 100 A RMS. The estimated steady-state junction temperature is 90 °C. It can be seen that the proposed gate driver can successfully operate at a continuous switching state even at

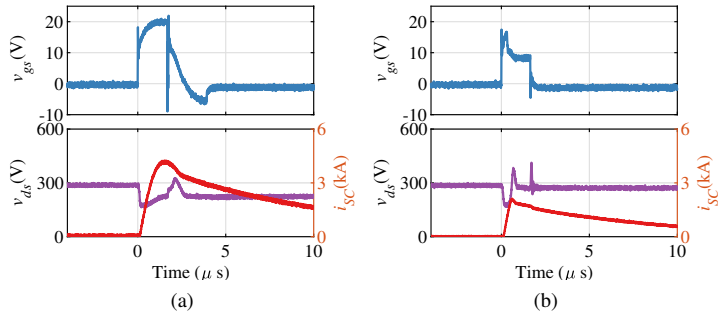


Fig. 13: Comparison of the short-circuit currents. (a) DESAT protection at 300 V; (b) two-step protection at 300 V.

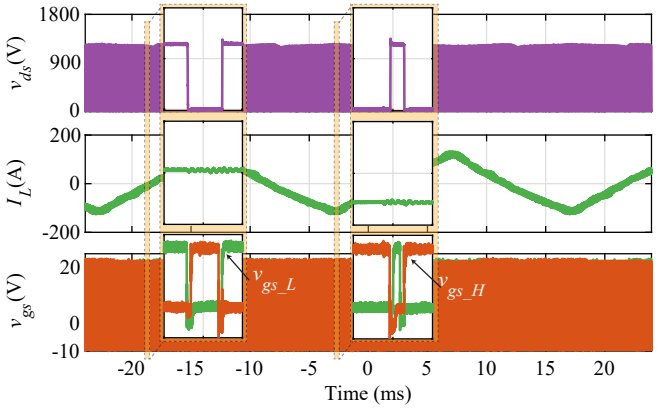


Fig. 14: The waveform of the drain-source voltage, the load current and gate-source voltages at steady state continuous operation. The orange waveform is the high side switch.

a higher junction temperature. There is no false triggering of protection during the switching of the converter.

## VI. Conclusion

The proposed method offers a novel solution for designing the SiC gate driver considering the reliability of the gate-oxide of the device. The limited negative peak turnoff voltage, together with the reliable short circuit protection, is guaranteed by the proposed driving method. With the proposed circuit, control and parameter design method, the crosstalk voltage is limited within the safe operation range under various conditions. The proposed gate driver solution is universal and can be used for different types of packages, independent of the value of the common source inductor and switching speed. Together with the DESAT circuit, the SC current on the stray inductor in the package is adopted to realize a two-step short circuit protection with ultra-fast response speed and high noise immunity. In the experiments, when SC happens, the gate-source voltage can be clamped to the lower level as fast as 350 ns. Integration of the proposed solution can be expected at the chip level to further simplify the gate driver structure.

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