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***Abstract*—DC systems connected to single-phase AC/DC converters are subject to a second-order harmonic ripple affecting the DC-bus voltage. Such ripple can be neutralized through an active filter circuit. This paper presents an improved control algorithm for a symmetrical half-bridge based active filter architecture. Contrarily to standard control approaches, the proposed solution does not require any external measurement other than the voltages and current internal to the active filter itself. This makes the analyzed active filter architecture suitable for a plug-and-play solution, meaning that it can be connected to the DC-bus terminals of a pre-existing system without any additional modification. The proposed control algorithm is based on multiple cascaded feedback loops, and the frequency and phase synchronization with the second-order harmonic component to be eliminated is based on an internally developed Phase-Locked-Loop (PLL). The developed approach has been numerically tested and validated in different operating conditions, showing satisfactory performances.**

***Index Terms*—Active filters, Second-Order Harmonic Elimination, Power Electronics Converters Control.**

I. Introduction

Modern power systems are characterized by an increasingly higher attention on the interoperability of different equipment, apparatus and subsystems, that must coexist and operate coordinately and harmoniously with one another. In this framework, AC/DC conversion plays a central role, especially considering new concepts of hybrid and smart grids, where different networks can be interconnected together in a flexible and controllable way through power electronic converters.

However, single-phase AC/DC conversion is subject to a major drawback, being that the instantaneous power transferred between the AC and the DC side contains not only a DC component, but also an oscillating harmonic at twice the AC line frequency. This pulsating power may introduce a significant harmonic ripple on the DC-bus voltage, which could hamper the correct functionality of the system as a whole [1]. This problem is nowadays also significant in some multilevel converter architectures, especially in the medium and high voltage range, and even in three-phase converters. This is because some multilevel architectures are typically realized by cascading multiple independent single-phase AC/DC conversion cells, each of which suffers from a second-order harmonic ripple affecting its DC-bus voltage [2], [3].

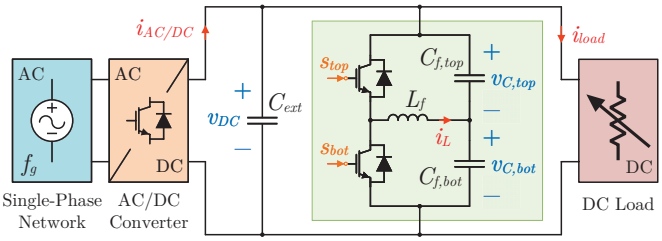

Fig. 1. Circuit architecture of the symmetrical half-bridge based active filter.

The DC-bus voltage ripple can be reduced by installing large DC-bus capacitor banks, designed to absorb the ripple power generated by the AC/DC converter. However, this approach increases the overall size, weight and cost of the overall converter. Another solution to suppress the second-order harmonic ripple is to use LC trap filters, in a way to introduce (through a series LC resonance) a low-impedance path for the second-order harmonic current generated (on the DC side) by the AC/DC converter. However, since the required resonance frequency is low (i.e., 100 Hz or 120 Hz for grid connected applications), the volume and weight of the passive components would be considerable, thus presenting the same bulkiness issues of an increased DC-bus capacitor bank [4].

A different approach is to use an active filter. By introducing additional controllable circuitry, the second-order power harmonic can be shifted away from the DC-bus and stored in other components in a more efficient and effective way [5], [6]. At the expense of a slightly more complex system and of additional switching components, this solution allows to mitigate the second-order harmonic ripple without compromising size, weight and cost.

Many different active filter topologies have been proposed in the technical literature [2], [3], [5]–[11]. They differ in terms of the energy storage device (i.e., inductive or capacitive), in terms of the connection to the system (i.e., on the AC or DC side, in series or in parallel, etc...) and in terms of the circuit topology (i.e., buck, boost, buck-boost, full-bridge, etc...).

An active filter based on a Symmetrical Half-Bridge topology has been proposed in [3]. With this architecture, schematically represented in Fig. 1, two series-connected DC-bus capacitors can be used to sustain the DC voltage and to absorb

the ripple power at the same time. These capacitors (that typically need to be rated for the entire DC-bus voltage) can transfer power between one another, thanks to the proper control of the current flowing in a small filtering inductor, which is itself driven through a standard half-bridge conversion circuit. Such controlled exchange of energy can be synchronized with the AC/DC converter in order to filter out the second-order power harmonic, leading to a constant overall DC-bus voltage.

Typically, the control of this active filter is synchronized and developed together with the single-phase AC/DC converter, in a way to take advantage of the AC side measurements to compute the reference current to be forced in the filtering inductor. A current-mode controller is then used to generate the switching signals for the semiconductor devices [3], [12], [13]. This solution is convenient if the whole system is designed at once, but makes the active filter less attractive to be installed on a pre-existing system, since it would either require communication with the controller of the AC/DC converter or to have direct access to the measurements on the AC side circuit.

To overcome such drawback, this paper presents an improved control algorithm for the symmetrical half-bridge based active filter topology. The proposed solution does not require any external measurement other than the voltages and current internal to the active filter itself, and the frequency and phase synchronization is achieved thanks to an internally developed Phase-Locked-Loop (PLL), specifically designed with respect to the second-order harmonic to be neutralized. A control algorithm based on multiple cascaded feedback loops is then used to neutralize the second-order harmonic ripple affecting the overall DC-bus voltage.

The paper is structured as follows: first, Section II derives the mathematical model of the system, that is used in Section III to develop the proposed control algorithm; then Section IV shows the numerical validation of the approach in multiple operating conditions, and finally Section V summarizes the conclusions of the work.

II. Circuit Topology and Mathematical Model

The circuital architecture of the active filter under analysis is represented in Fig. 1. The output of a regular half-bridge leg is connected, through an inductor of inductance L_f, to the midpoint of two series-connected capacitors with equal capacitance $C_{f,top} = C_{f,bot} = C_f$. The half-bridge leg and the capacitors are then connected to the overall DC-bus of the system, which may also include an additional external capacitor C_{ext} (note that, since $C_{f,top}$ and $C_{f,bot}$ contribute to the overall DC-bus capacitance, the external capacitor C_{ext} may also be absent).

In the analyzed setup, the DC-bus is connected to a single-phase AC/DC converter, that introduces to the DC-bus voltage an undesired frequency oscillation at $2\,f_g$ (f_g being the fundamental frequency of the AC grid), and feeds a generic DC load which, without loss of generality, is here supposed not to introduce any harmonic at $2\,f_g$.

The working principle of the active filter is based on the injection of a controlled current i_L in the inductance L_f, which creates an unbalance between the voltages $v_{C,top}$ and $v_{C,bot}$ of the DC-bus capacitors. This voltage unbalance, here defined as $v_{C,\Delta} = v_{C,top} - v_{C,bot}$ can generate a periodic oscillation at frequency $2\,f_g$ into the overall DC-bus voltage $v_{DC} = v_{C,top} + v_{C,bot}$, which can be used to neutralize the harmonic oscillation introduced by the AC/DC converter [3].

The two switches of the half-bridge leg are always controlled in a complementary way, and their state can be identified by the switching signal $s_{top} \in \{0, 1\}$ of the top device (the bottom device being controlled by $s_{bot} = 1 - s_{top}$).

Considering a Pulse Width Modulation (PWM) algorithm with a modulation frequency f_{sw}, and denoting as $d \in [0; 1]$ the duty-cycle of the half-bridge leg (i.e., the average of s_{top} in a modulation period), the average voltages across the bottom and top devices are equal to $d \cdot v_{DC}$ and $(1 - d) \cdot v_{DC}$, respectively. Similarly, the average currents flowing through the top and bottom devices are $d \cdot i_L$ and $(1 - d) \cdot i_L$, respectively. A mathematical model for the system, suited for control purposes, can be formulated by applying a standard state-space averaging procedure considering the modulation period $T_{sw} = 1/f_{sw}$.

The average dynamics of the current i_L of the inductor can be found by applying Kirchhoff's voltage law to the loop involving L_f, $C_{f,bot}$ and the bottom switching device:

$$L_f \cdot \frac{\mathrm{d}i_L}{\mathrm{d}t} = d \cdot v_{DC} - v_{C,bot} \tag{1}$$

The average dynamics of the voltages $v_{C,top}$ and $v_{C,bot}$ can be found by applying Kirchhoff's current law to the positive and negative nodes of the DC-bus:

$$C_f \cdot \frac{\mathrm{d}v_{C,top}}{\mathrm{d}t} + C_{ext} \cdot \frac{\mathrm{d}v_{DC}}{\mathrm{d}t} = -d \cdot i_L + (i_{AC/DC} - i_{load}) \tag{2}$$

$$C_f \cdot \frac{\mathrm{d}v_{C,bot}}{\mathrm{d}t} + C_{ext} \cdot \frac{\mathrm{d}v_{DC}}{\mathrm{d}t} = (1-d) \cdot i_L + (i_{AC/DC} - i_{load}) \tag{3}$$

and the difference $(i_{AC/DC} - i_{load}) = i_{DC}$ represents the equivalent current injected into the DC-bus by the combined contributions of the AC/DC converter and of the DC load. In steady-state conditions, the average value of $i_{AC/DC}$ is equal to the average value of i_{load}, and thus i_{DC} is only the harmonic current at frequency $2\,f_g$ to be neutralized through the active filter. Note that, despite the presence of three capacitors (i.e., $C_{f,top}$, $C_{f,bot}$ and C_{ext}), the voltage on C_{ext} is always equal to $v_{DC} = v_{C,top} + v_{C,bot}$, and does not represent an additional state variable for the system.

The dynamics of the overall DC-bus voltage v_{DC} can be found by summing term-to-term the equations (2) and (3), and dividing the result by 2, which leads to:

$$\begin{aligned} C_{eq} \cdot \frac{\mathrm{d}v_{DC}}{\mathrm{d}t} &= \left(C_{ext} + \frac{C_f}{2}\right) \cdot \frac{\mathrm{d}v_{DC}}{\mathrm{d}t} = \\ &= \left[\frac{-d \cdot i_L + (1-d) \cdot i_L}{2}\right] + (i_{AC/DC} - i_{load}) = \\ &= i_{AF} + i_{DC} \end{aligned} \tag{4}$$

where $C_{eq} = (C_{ext} + C_f/2)$ is the overall equivalent DC-bus capacitance, while $i_{AF} = [-d \cdot i_L + (1-d) \cdot i_L]/2$ can be interpreted as an equivalent current generated by the active filter. This current can be controlled through d and i_L to compensate the effect of i_{DC}.

The dynamics of the voltage unbalance $v_{C,\Delta}$ can be found by subtracting term-to-term (2) and (3), resulting into:

$$C_f \cdot \frac{\mathrm{d}v_{C,\Delta}}{\mathrm{d}t} = -i_L \tag{5}$$

III. Proposed Control Algorithm

Considering equation (4), the neutralization of the harmonic ripple at $2\,f_g$ on v_{DC} can be achieved if the equivalent current i_{AF} introduced by the active filter can balance the harmonic current i_{DC}. However, two main challenges hamper this goal.

Firstly, the expression of i_{AF} is non-linear, and depends on the product of the duty-cycle d and of the inductor current i_L, the last of which is itself dynamically depending on d through the effects of v_{DC} and $v_{C,bot}$, as can be seen by (1) and (3).

Secondly, the direct knowledge of the harmonic current i_{DC} is typically not available, since its measurement would require introducing additional sensors externally of the active filter (e.g., additional current sensors on the DC-bus or measurements on the AC side of the AC/DC converter).

As a result, a proper control algorithm must be developed to overcome these drawbacks and allow to achieve the desired control target by only using measurements available within the active filter itself (i.e., i_L, $v_{C,top}$ and $v_{C,bot}$). This section describes the proposed solution.

A. Control of the Equivalent Current of the Active Filter

The expression of i_{AF} can be simplified by assuming that the voltage across the filtering inductor is small enough when compared to the voltages of the top and bottom capacitors. With this approximation (which is typically verified in most designs and that would not anyhow alter the applicability of the proposed approach) from (1) it can be derived that:

$$d \approx \frac{v_{C,bot}}{v_{DC}}, \qquad \text{and} \qquad (1-d) \approx \frac{v_{C,top}}{v_{DC}} \tag{6}$$

Then, the expression of i_{AF} becomes:

$$\begin{aligned} i_{AF} &= \frac{-d \cdot i_L + (1-d) \cdot i_L}{2} \approx \\ &\approx \frac{(v_{C,top} - v_{C,bot}) \cdot i_L}{2 \cdot v_{DC}} = \frac{v_{C,\Delta} \cdot i_L}{2 \cdot v_{DC}} \end{aligned} \tag{7}$$

The task of the active filter is to generate a sinusoidal current i_{AF} with frequency $2\,f_g$. By denoting as $\omega_g = 2\pi f_g$ the angular frequency of the AC grid, the second-order harmonic current to be developed can be expressed as:

$$i_{AF}(t) = I_{AF,2} \cdot \cos\left(\theta(t)\right) = I_{AF,2} \cdot \cos\left(2\,\omega_g\,t + \theta_0\right) \tag{8}$$

with $I_{AF,2}$ and $\theta(t) = (2\,\omega_g\,t + \theta_0)$ denoting the magnitude and instantaneous phase angle of the second-order harmonic current (with respect to an arbitrary initial instant of time, which defines the value of the initial phase angle θ_0).

When the active filter is operating in steady-state conditions, the voltage v_{DC} is constant and equal to its average value $V_{DC,0}$. Then, to generate a sinusoidal current i_{AF} at frequency $2\,f_g$, it is sufficient that both $v_{C,\Delta}$ and i_L are sinusoidal waveforms at frequency f_g.

The voltage $v_{C,\Delta}$ can be expressed as:

$$v_{C,\Delta}(t) = V_{C,\Delta,1} \cdot \cos\left(\gamma(t)\right) = V_{C,\Delta,1} \cdot \cos\left(\omega_g\,t + \gamma_0\right) \tag{9}$$

with $V_{C,\Delta,1}$ and $\gamma(t) = (\omega_g\,t + \gamma_0)$ denoting the magnitude and phase of the voltage harmonic at frequency f_g.

The corresponding expression of i_L can be found from (5):

$$\begin{aligned} i_L(t) &= \omega_g\,C_f\,V_{C,\Delta,1} \cdot \sin\left(\omega_g\,t + \gamma_0\right) = \\ &= I_{L,1} \cdot \sin\left(\omega_g\,t + \gamma_0\right) = I_{L,1} \cdot \sin\left(\gamma(t)\right) \end{aligned} \tag{10}$$

with $I_{L,1} = \omega_g\,C_f\,V_{C,\Delta,1}$ denoting the magnitude of the current harmonic at frequency f_g.

By replacing (9) and (10) in the approximate expression of i_{AF} given in (7), it results that:

$$\begin{aligned} i_{AF}(t) &\approx \frac{V_{C,\Delta,1} \cdot I_{L,1}}{4\,V_{DC,0}} \cdot \sin\left(2\,\omega_g\,t + 2\,\gamma_0\right) = \\ &= \frac{(\omega_g\,C_f) \cdot V_{C,\Delta,1}^2}{4\,V_{DC,0}} \cdot \sin\left(2\,\gamma(t)\right) = \\ &= \frac{I_{L,1}^2/(\omega_g\,C_f)}{4\,V_{DC,0}} \cdot \sin\left(2\,\gamma(t)\right) \end{aligned} \tag{11}$$

The expression (11) can be compared to the expression (8) to find the equivalence between the magnitude and phases:

$$V_{C,\Delta,1} = \sqrt{(4\,V_{DC,0})/(\omega_g\,C_f) \cdot I_{AF,2}} \tag{12}$$

$$I_{L,1} = \sqrt{(4\,V_{DC,0}) \cdot (\omega_g\,C_f) \cdot I_{AF,2}} \tag{13}$$

$$\sin\left(2\,\gamma(t)\right) = \cos\left(\theta(t)\right) \;\Leftrightarrow\; \gamma(t) = \frac{\theta(t)}{2} + \frac{\pi}{4}\;(+k\pi) \tag{14}$$

Several properties can be deduced from (12)-(14).

- Firstly, the control of i_{AF} does not depend on the value of C_{ext}, but it is instead only related to the internal capacitance C_f of the active filter.
- Secondly, in steady-state, both the top and bottom capacitors of the active filters are simultaneously subject to a DC voltage (being equal to $V_{DC,0}/2$) and to an harmonic oscillation at frequency f_g, with magnitude $V_{C,\Delta,1}/2$. Since the required $V_{C,\Delta,1}$ is proportional to the square root of $I_{AF,2}$, the higher is the ripple suppression requirement, the higher is the voltage rating of the active filter capacitors. In the extreme case, both $C_{f,top}$ and $C_{f,bot}$ need to be rated for the full DC-bus voltage $V_{DC,0}$.
- Additionally, the required current magnitude $I_{L,1}$ is also changing proportionally to the square root of $I_{AF,2}$. This not only represents a design requirement for the choice of the inductor and of the switching devices, but may also be relevant for the energetic efficiency of the active filter itself, since both the conduction and switching losses depend on the required current i_L.

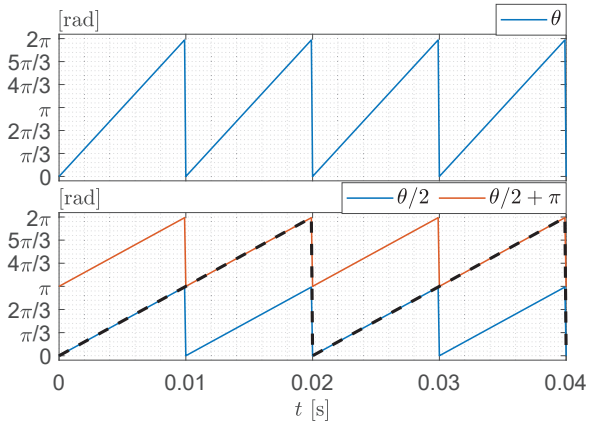

Fig. 2. Generation of an angle at frequency f_g from an angle at frequency $2\,f_g$ while avoiding discontinuities.

- Finally, the phase angle $\gamma(t)$ of the voltage $v_{C,\Delta}$ and of the current i_L is related to half of the phase angle $\theta(t)$ and, since $\theta = \theta + 2k\pi$ (with $k \in \mathbb{Z}$), there is more than one possible available angle γ. Any choice of $k \in \mathbb{Z}$ would provide a feasible angle γ in (14). However, to guarantee the continuity of the trigonometric functions (e.g., to avoid discontinuities in γ when θ jumps from 2π to 0), the angle γ can be computed as $\gamma = \theta/2 + \pi/4$ on odd-order cycles of θ, and as $\gamma = \theta/2 + \pi + \pi/4$ on even-order cycles of θ (starting from any arbitrary initial condition). This easily allows generating an angle varying at frequency f_g starting from an angle varying at frequency $2\,f_g$, as graphically exemplified in Fig. 2.

B. Neutralization of the External Harmonic Current

As previously mentioned, the equivalent current i_{AF} of the active filter is required to track the overall harmonic current i_{DC}. However, this current is typically not available, because it would either require a direct measurement (e.g., by placing additional current sensors on the DC-bus of the system), or it would need to be reconstructed or estimated (e.g., by measuring the AC voltage and current of the AC/DC converter and reconstructing the corresponding DC-side current, which is the source of the second-order harmonic disturbance).

Moreover, the equivalent current i_{AF} developed by the active filter can show a mismatch with respect to its desired reference i^*_{AF}, resulting from non-idealities in the modeling and control approach. For example, the tracking of i^*_{AF} may be affected by the simplifying assumption (6), by some parameter uncertainties (e.g., tolerances on the capacitances $C_{f,top}$ and $C_{f,bot}$), by imperfect control performances or by the presence of additional higher-order harmonics in the system.

Therefore, the control of the active filter requires overcoming these drawbacks. A simple, but effective solution, is to use a closed-loop control algorithm acting on the overall DC-bus voltage v_{DC}, with a resonant action at the frequency $2\,f_g$. Since no second-order harmonic is desired on the DC-bus voltage, the reference signal of such controller is zero, while the output represents the reference current i^*_{AF} to be applied by the active filter. As known, the resonant action achieves an infinite gain at the resonance frequency, and helps neutralizing the effect of both the current i_{DC} (which acts as an external disturbance at frequency $2\,f_g$ on the model (4)) and of the imperfect tracking of i^*_{AF} (which can be treated as the result of unmodeled dynamics in the model (4)).

Finally, to properly identify the magnitude $I^*_{AF,2}$ and the instantaneous phase angle θ^* to be applied, a Phase-Locked-Loop (PLL) algorithm can be employed on i^*_{AF}. The same PLL can be also used to estimate in real-time the frequency $2\,f_g$ of the second-order harmonic oscillation, which helps guaranteeing a selective behaviour of the active filter and compliance against fluctuations of the AC grid frequency.

C. Overall control algorithm

The block diagram of the overall control algorithm described in the previous subsections is represented in Fig. 3.

The closed-loop control of the second-order harmonic of v_{DC} (yellow subsystem in Fig. 3) is realized through a pure resonant controller, which is designed to have a narrow bandwidth around $2\,f_g$, in order for it to be very selective around the second-order harmonic to be compensated and not to interfere with the other harmonic components of the DC-bus voltage. The output of this control loop is the reference current i^*_{AF} to be generated through the active filter. In case there is any available information regarding the DC-side currents (e.g., through the direct or indirect knowledge of $i_{AC/DC}$), it can be used as a feed-forward term $i^*_{AF,FF}$ to improve the dynamic performances of the controller.

A single-phase PLL is then executed (grey subsystem in Fig. 3) on i^*_{AF}. It estimates the magnitude $I^*_{AF,2}$ of the second-order harmonic to be generated, the instantaneous phase angle $\theta^*(t)$ and the frequency $2\,f_g$ of the second-order harmonic.

The magnitude $I^*_{AF,2}$ is used to compute $V^*_{C,\Delta,1}$ and $I^*_{L,1}$ via (12) and (13) (blue subsystem in Fig. 3). The value of $V_{DC,0}$ is estimated as the average of v_{DC} in a long time interval (i.e., several fundamental periods).

The phase θ^* is used to compute γ^* through (14) (orange subsystem in Fig. 3). As also previously mentioned, the angle is computed as $\gamma = \theta/2 + \pi/4$ on odd-order cycles of θ, and as $\gamma = \theta/2 + \pi/4 + \pi$ on even-order cycles of θ.

The instantaneous reference voltage unbalance $v^*_{C,\Delta}$ is reconstructed as per (9), and a closed-loop control is implemented on it (red subsystem in Fig. 3). A Proportional-Integral-Resonant (PIR) controller architecture can be used for this purpose. The resonant action, synchronized with f_g, guarantees a zero steady-state error when tracking the sinusoidal reference $v^*_{C,\Delta}$. The integral action instead guarantees that the steady-state average values of $v_{C,top}$ and $v_{C,bot}$ are equal with one another (and equal to $v_{DC}/2$). The output of this controller is the reference current i^*_L to be tracked with the active filter. To improve the dynamic performances of the controller, it is possible to introduce a feedforward term $i^*_{L,FF}$ computed through $I^*_{L,1}$ and γ^* as per (13).

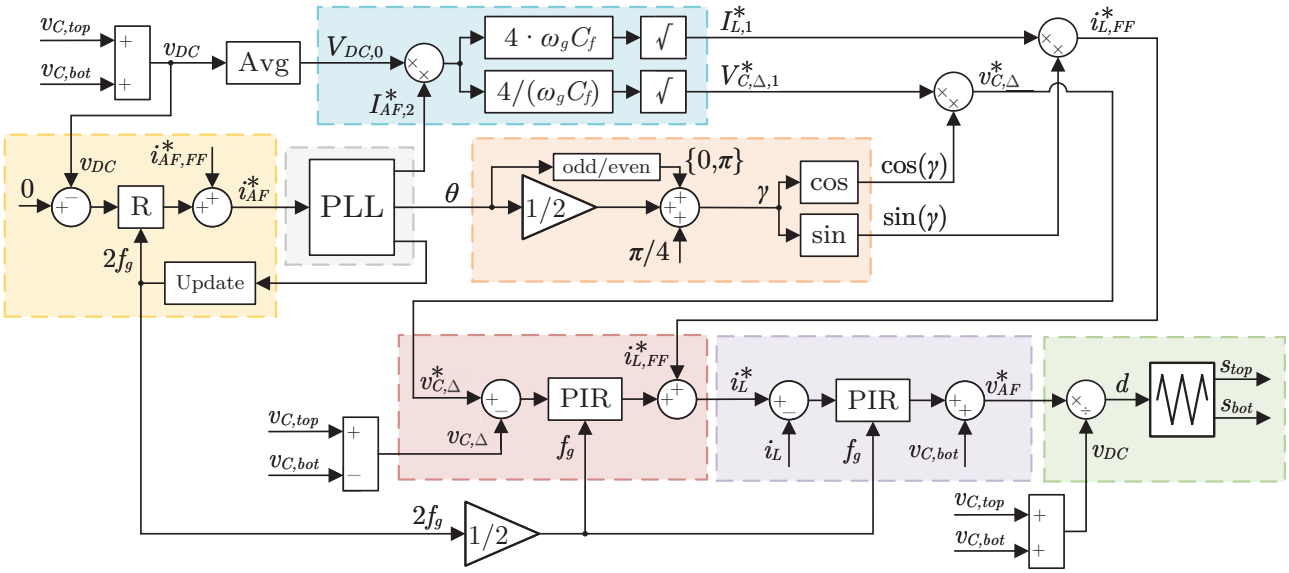

Fig. 3. Block diagram of the proposed control algorithm.

The closed-loop control of i_L (purple subsystem in Fig. 3) is also based on a PIR structure, with the resonance frequency synchronized with f_g, and the measured voltage $v_{C,bot}$ is here added as a feed-forward term.

The output of this controller is a reference voltage v^*_{AF} to be applied with a standard PWM algorithm (green subsystem in Fig. 3). The duty-cycle d is immediately computed by dividing v^*_{AF} by v_{DC}, and is finally compared with a triangular carrier to compute the switching signals s_{top} and s_{bot} to control the gate drivers of the semiconductor devices.

To improve the controller reliability and prevent dynamic instabilities, the resonance frequencies of the resonant controllers are updated at a much slower rate than the overall system dynamics, and based on a periodic average of the PLL estimated frequency.

IV. Algorithm Validation

The proposed control algorithm has been numerically validated in the PLECS simulation environment.

The parameters of the system are summarized in Tab. I.

In all the following simulations, the single-phase AC/DC converter controls the average value of the DC-bus voltage, while the DC load has been simulated with a controlled current source. The AC/DC and the active filter controllers are completely independent from one another, and no information is exchanged between them. To better evaluate the active filter performances independently from the surrounding system, the AC/DC converter has been simulated with an averaged model (meaning that the switching-related injected harmonics have been neglected), while the active filter has instead been simulated with a switching model.

The PLL for the synchronization with the instantaneous angle θ of the reference current i_{AF} has been realized based on a standard Second-Order Generalized Integrator (SOGI) [14]. The resonance frequencies of the feedback controllers have been updated at constant time intervals of $T_{update,f_g} = 2\,\mathrm{s}$ based on the average value of the PLL estimated frequency over the previous $T_{avg,f_g} = 1\,\mathrm{s}$ time interval. No additional external measurements have been included in the control of the second-order harmonic of $v_{DC,\Delta}$, meaning that the feedforward term $i^*_{AF,FF}$ of Fig. 3 is absent.

TABLE I
System Parameters

Symbol	Description	Value
$f_{g,rated}$	Rated Frequency of the AC Grid	50 Hz
$S_{g,rated}$	Rated Apparent Power of the AC Grid	1 kVA
$V_{g,rated}$	Rated Voltage of the AC Grid (RMS)	90 V
$I_{g,rated}$	Rated Current of the AC Grid (RMS)	11.1 A
$V_{DC,rated}$	Rated DC-bus Voltage	250 V
$P_{load,rated}$	Rated Power of the DC Load	1 kW
L_f	Inductance of the Active Filter	200 µH
C_f	Internal Capacitance of the Active Filter	240 µF
f_{sw}	Switching frequency of the Active Filter	20 kHz
C_{ext}	External DC-bus Capacitance	60 µF

A. Nominal Operation

The first test is aimed at showing the effect of the active filter in nominal operating conditions.

Initially, the system is charged at the nominal voltage of $v_{DC} = 250\,\mathrm{V}$, the top and bottom capacitors of the active filter are equally charged (i.e., $v_{C,top} = v_{C,bot} = 125\,\mathrm{V}$), and both the AC/DC converter and the DC load are inactive. At the instant $t_0 = 0\,\mathrm{s}$, the load is activated and, in a time window of $0.25\,\mathrm{s}$, its power is linearly increased from zero to $1\,\mathrm{kW}$. The AC/DC converter reacts to the load power change and it

also starts absorbing power from the AC grid. In this process, it injects into the DC-bus a current $i_{AC/DC}$ with a frequency of $2\,f_g = 100\,\text{Hz}$ and, as a consequence, generates into the DC-bus voltage a ripple at the same frequency. At the instant $t_1 = 0.5\,\text{s}$ the control of the active filter is enabled, and it operates to actively neutralize such DC-bus voltage ripple.

The results are depicted in Fig. 4. The top graph shows the instantaneous DC-bus voltage v_{DC} and its average value $V_{DC,0}$ (computed with a moving average algorithm with a time window of $T_{avg} = 1/(2\,f_g) = 10\,\text{ms}$). The second subplots shows the magnitude of the second-order harmonic component $V_{DC,2}$ of the DC-bus voltage (computed through a Fourier decomposition in a $T_{avg} = 1/(2\,f_g) = 10\,\text{ms}$ moving time window). The third subplot shows the instantaneous waveforms of the voltages of the top and bottom capacitors $v_{C,top}$ and $v_{C,bot}$ of the active filter. The fourth subplot shows the equivalent current i_{AF} injected by the active filter (computed as per (7)), the current $i_{DC} = i_{AC/DC} - i_{load}$, that identifies the equivalent contribution of the AC/DC converter and of the load on the DC-bus voltage (to be more specific, the graph shows the current $-i_{DC}$, to allow for an easier comparison with i_{AF}), and the reference magnitude current $I^*_{AF,2}$ computed by the feedback control algorithm. The fifth subplot shows the voltage unbalance $v_{C,\Delta}$, together with its instantaneous reference $v^*_{C,\Delta}$ and with the reference magnitude $V_{C,\Delta,1}$ computed by the control algorithm. Finally, the last subplot shows the inductor current i_L, together with its instantaneous reference i^*_L and with the magnitude $I^*_{L,1}$ computed by the control algorithm (and used as feedforward term in the controller).

As can be noted, after the load is activated, the current i_{DC} increases, and the DC-bus voltage v_{DC} shows a visible ripple at $2\,f_g$, whose magnitude reaches around $V_{DC,2} \approx 35\,\text{V}$. The voltages $v_{C,top}$ and $v_{C,bot}$ are also affected by this ripple, but are still equal to one another (as can also be seen from $v_{C,\Delta} = 0$). Once the active filter is enabled, the current i_{AF} is increased by properly acting on $v_{C,\Delta}$ and i_L, in a way to compensate for the harmonic current i_{DC}. The second-order harmonic component $V_{DC,2}$ is then reduced and is effectively neutralized in around $0.5\,\text{s}$.

The steady-state results of this test are shown in Fig. 5. It can be seen that the DC-bus voltage is only affected by the switching ripple, while the second-order harmonic has been effectively canceled. It can also be noted that, apart from the switching ripple, the fundamental component of the current i_{AF} is equal to the equivalent current $-i_{DC}$ injected by the AC/DC converter and by the DC-bus load.

However, for the correct functioning of the active filter, the voltages $v_{C,top}$ and $v_{C,bot}$ of the top and bottom capacitors need to oscillate at the frequency $f_g = 50\,\text{Hz}$ with an overall peak-to-peak excursion almost equal to $V_{DC,0} = 230\,\text{V}$. This is also evident from the analysis of the voltage unbalance $v_{C,\Delta} = v_{C,top} - v_{C,bot}$.

Finally, it can be noted that, thanks to the resonant actions, both the voltage $v_{C,\Delta}$ and the current i_L can track the corresponding references $v^*_{C,\Delta}$ and i^*_L, and the magnitudes

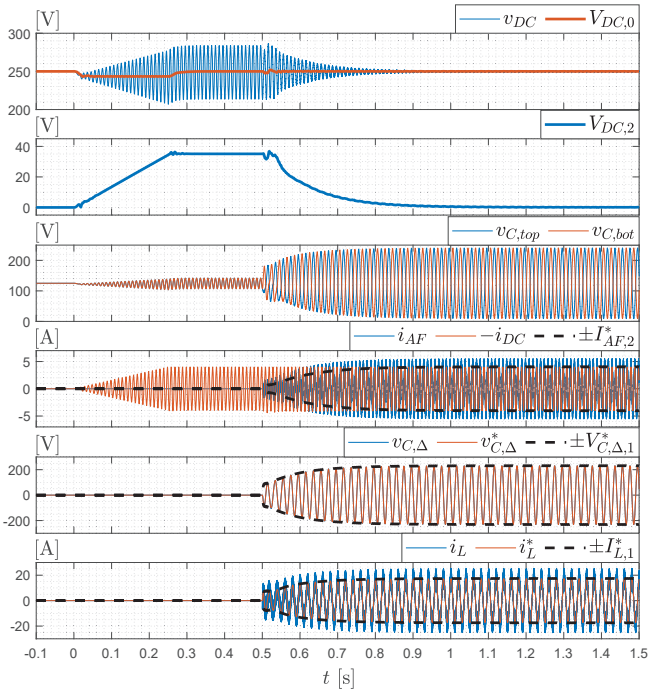

Fig. 4. Results of the Active Filter enabling at nominal operating conditions.

$V^*_{C,\Delta,1}$ and $I^*_{L,1}$ are effectively representing the envelopes of these sinusoidal waveforms. The switching-related behaviour is evident for the current i_L, while it is instead almost completely filtered for the voltages of the capacitors.

B. Response to Reactive Power Injection

This test shows the performances of the active filter following a change in the reactive power of the AC grid. The results are shown in Fig. 6. Initially, the system is working in steady state operation with a power absorption equal to $P_{load} = 500\,\text{W}$ from the DC load. To stabilize the average DC-bus voltage, the AC/DC converter is absorbing the same power $P_g = 500\,\text{W}$ from the AC grid, and is controlled to work with unitary power factor, meaning that its apparent power is $S_g = P_g = 500\,\text{VA}$. The active filter is already enabled and the second-order harmonic ripple generated by the AC/DC converter is compensated.

At the instant $t_0 = 0\,\text{s}$, the AC/DC converter references are modified, and it starts absorbing a reactive power of $Q_g = 866\,\text{VAr}$ from the AC grid, in a way that the apparent power becomes $S_g = \sqrt{P_g^2 + Q_g^2} = 1\,\text{kVA}$. As a consequence of the AC-grid apparent power doubling, the AC-grid current I_g is also doubled, and the second-order harmonic of $i_{AC/DC}$ increases accordingly. This phenomenon produces itself a second-order ripple in v_{DC}, which is sensed and neutralized by the active filter control.

As can be seen, after the reactive power change, the magnitude of the second-order harmonic of the DC-bus voltage reaches around $V_{DC,2} \approx 40\,\text{V}$, but it is quickly neutralized by the active filter control in around $0.5\,\text{s}$.

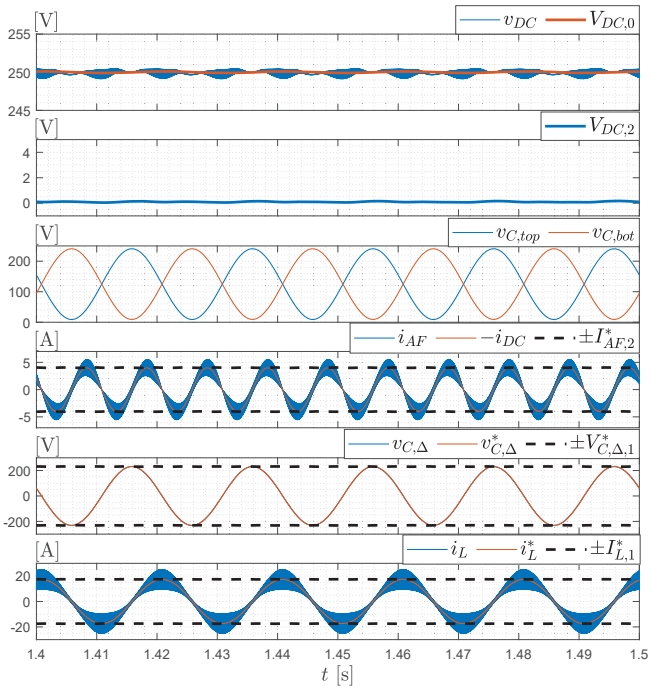

Fig. 5. Steady-State waveforms at nominal operating conditions.

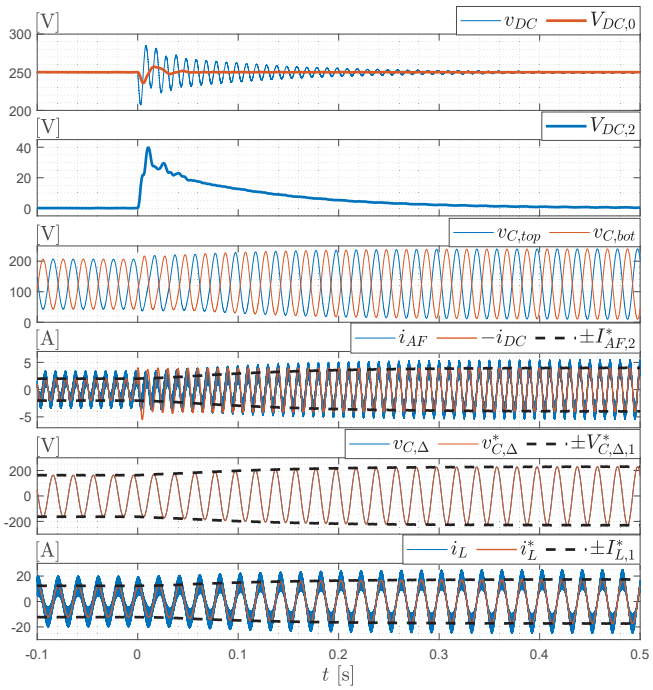

Fig. 6. Results following a reactive power step change in the AC grid.

At the end of the test, the magnitude of the fundamental current of i_{AF} has also been doubled with respect to the initial conditions (i.e., from around 2 A to around 4 A) and, coherently with (12) and (13), the magnitude of the fundamental components of $v_{C,\Delta}$ and i_L have been increased by around $\sqrt{2}$ times (i.e., from 163.6 V to 230.4 V, and from 12.3 A to 17.3 A, respectively).

C. Response to Load Power Change

This test shows the performances of the active filter with respect to changes in the DC-bus load power. The results are shown in Fig. 7. Initially, the system is working in nominal operating conditions. At the instant $t_0 = 0\,\text{s}$ the load is changed, and its power is linearly changed from $P_{load} = 1\,\text{kW}$ to $P_{load} = -1\,\text{kW}$ in a time window of $0.5\,\text{s}$ (i.e., the load becomes active).

The AC/DC converter always works with unitary power factor, and the change in the active power results in a change in both the AC grid current and in the current i_{DC}.

As can be noted, the second-order harmonic ripple $V_{DC,2}$ increases up to around 17 V during the power load change, but is again quickly brought back to zero after the transient. Since the apparent power of the AC grid at the end of the sequence is the same as in the beginning, the final magnitudes of i_{AF}, $v_{C,\Delta}$ and i_L are also equal to their initial values.

D. Response to AC Grid Frequency Changes

This final test is aimed at showing the controller performances with respect to changes in the AC grid frequency. The results are shown in Fig. 8. Initially, the system is working in nominal operating conditions, with a load power absorption of $P_{load} = 1\,\text{kW}$. At the time instant $t_0 = 0\,\text{s}$, the AC grid frequency is immediately changed from $f_{g,0} = 50\,\text{Hz}$ to $f_{g,1} = 51\,\text{Hz}$, while all the other operating conditions are kept unchanged. The frequency change has been simulated to act simultaneously on both the AC grid voltage and the AC grid current (i.e., the grid synchronization dynamics of the AC/DC converter has been neglected). Simultaneously with the frequency step change, the averaging time for the computation of $V_{DC,0}$ and $V_{DC,2}$ have also been changed from $T_{avg,0} = 1/(2\,f_{g,0}) = 10\,\text{ms}$ to $T_{avg,1} = 1/(2\,f_{g,1}) = 9.8\,\text{ms}$.

Following the change in the AC grid frequency, the active filter is not able to neutralize the second-order harmonic ripple of $V_{DC,2}$ which, after a short transient, stabilizes around 27 V. This is due to the finite gain provided by the resonant controller of v_{DC} at the frequency $2\,f_{g,1} = 102\,\text{Hz}$, while its resonance frequency is still at $2\,f_{g,0} = 100\,\text{Hz}$.

At the instant $t_1 = 2\,\text{s}$, the resonance frequencies of the active filter controller are updated based on the frequency estimated by the PLL in the last $1\,\text{s}$ time window. Thanks to this change, the voltage ripple $V_{DC,2}$ is again actively controlled and it is effectively neutralized in around $0.5\,\text{s}$.

V. Conclusions

This paper has proposed an improved control algorithm for the elimination of the second-order harmonic ripple in a DC-bus supplied by a single-phase AC/DC converter, based on a symmetrical half-bridge active filter topology.

Contrarily to standard control algorithms adopted for such a circuital architecture, the proposed approach does not require

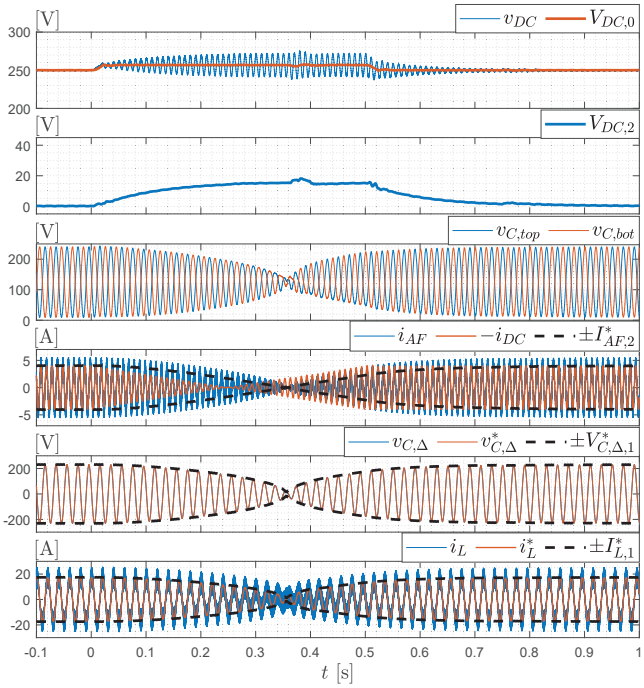

Fig. 7. Results following a load power inversion.

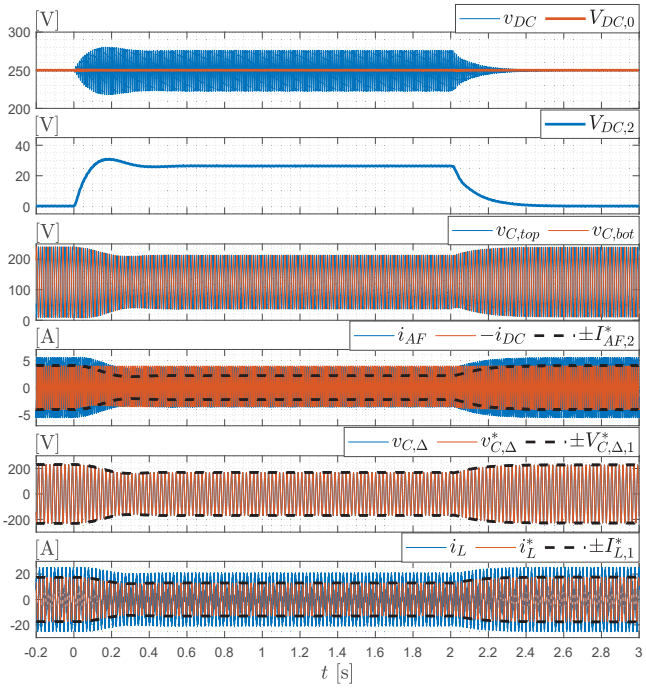

Fig. 8. Results following a change in the AC grid frequency.

any external measurements other than voltages and current internal to the active filter itself. Indeed, the controller achieves the frequency and phase synchronization (required for the second-order harmonic cancellation) thanks to a feedback control action and to an internally developed PLL algorithm.

The control algorithm is based on multiple cascaded feedback loops, and the elimination of the second-order harmonic component is guaranteed by a self-tuning resonant action. The approach has been successfully validated in different operating conditions, showing satisfactory results.

The proposed solution makes the considered active filter architecture suitable for a plug-and-play circuit, meaning that it can just be directly connected to the DC-bus terminals without any need for additional modifications in a pre-existing system.

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