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Exploring negative capacitance and neuromorphic devices based on CMOS-compatible ferroelectric HfO_2

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par

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I can live with doubt and uncertainty and not knowing. I think it's much more interesting to live not knowing than to have answers which might be wrong.

—Richard Feynman

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Lausanne, 11 November 2022 Carlotta Gastaldi

Abstract

Ferroelectric materials are explored for numerous applications thanks to their properties associated with electrically switchable spontaneous polarization. Perovskites are an established class of ferroelectrics used for sensors and actuators. However, they present limitations if integrated into microelectronics since they are neither CMOS compatible nor easily scalable. The game-changing solution came from the new family of ferroelectric materials based on HfO_2 that emerged within the last decade, which shows integrability in scaled CMOS devices.

HfO_2-based ferroelectrics are considered a rising candidate for different applications, among which neuromorphic devices and negative capacitance (NC) logic switches. Neuromorphic devices rely on the gradual polarization switching capability, which can reproduce synaptic plasticity. By mimicking the analog operation of the human brain, neuromorphic computing is expected to be more energy-efficient than the digital Von Neumann architecture. On the other hand, in logic switches, hysteresis is usually avoided, and a steep subthreshold swing is desired. For this purpose, negative capacitance field-effect transistors (NC-FETs) show a strong promise of overcoming the thermionic Boltzmann constraint of 60 mV/dec and continuing CMOS scaling. NC-FETs rely on exploiting the NC region of the polarization-electric field curve predicted by the Landau-Ginzburg-Devonshire (LGD) model.

This thesis aims to study the NC effect and its interplay with the polarization switching mechanisms of one of the best-known members of HfO_2-based ferroelectrics, the Si-doped HfO_2 (Si:HfO_2), and then to integrate it onto electronic devices. Temperature-dependent switching in Si:HfO_2 capacitors were studied, and the results were used to calibrate the LGD model, confirming the intrinsic switching mechanism experimentally. Then Si:HfO_2 was integrated into gate stack transistors to verify its functionality. In this framework, two structures were studied, one with an inner metal gate (IG) between the insulator and ferroelectric and one without it. Thanks to nanosecond-range pulse measurement, the S-shaped curve, predicted by the LGD model, was extracted, and the NC region was observed.

Following the previous study, the two gate stacks were implemented in a junctionless transistor (JLFET) platform with a Si channel of 12 nm, resulting in a device with Ion/Ioff of 6 orders of magnitude. The ferroelectric-JLFET (Fe-JLFET) without IG presented a hysteresis-free transfer characteristic and an improved subthreshold swing of 35% over 1.3 decades of drain current with pulse gate voltages compared to DC. On the contrary, the Fe-JLFET with IG showed a ferroelectric hysteretic behavior, and the Si:HfO_2 gradual switching is exploited to mimic the

synaptic plasticity. Additionally, the back-gate voltage biasing is used to tune the synaptic weight by more than 400x. Overall, this Ph.D. work confirms the potential of Fe-JLFET for both neuromorphic synapses and NC logic devices and highlights the requirements and limits of operation by studying how HfO_2-based ferroelectric properties evolve from the capacitor to integration into the gate stack.

Keywords: ferroelectricity, HfO_2, intrinsic switching, Landau-Ginzburg-Devonshire (LGD) theory, negative capacitance (NC), neuromorphic synapses, junctionless transistor (JLFET), ferroelectric transistor (Fe-FET), Silicon-On-Insulator (SOI) wafer.

Sommario

I materiali ferroelettrici sono studiati per numerose applicazioni grazie alle loro proprietà, associate alla polarizzazione spontanea commutabile elettricamente. Le perovskiti sono una classe consolidata di materiali ferroelettrici utilizzati per sensori e attuatori. Tuttavia, presentano limitazioni se integrati nella microelettronica poiché non sono né compatibili con circuiti CMOS né facilmente scalabili. La soluzione rivoluzionaria è arrivata dalla nuova famiglia di materiale ferroelettrico a base di HfO_2 emersa nell'ultimo decennio, che mostra l'integrabilità nei dispositivi CMOS in scala.

I ferroelettrici a base di HfO_2 sono considerati un candidato in ascesa per diverse applicazioni, tra cui dispositivi neuromorfici e interruttori logici a capacità negativa (NC). I dispositivi neuromorfici si basano sulla capacità di commutazione graduale della polarizzazione, che può riprodurre la plasticità sinaptica. Imitando il funzionamento analogico del calcolo neuromorfico del cervello umano, ci si aspetta che questi dispositivi siano più efficienti dal punto di vista energetico rispetto all'architettura digitale di Von Neumann. Negli interruttori logici, l'isteresi viene solitamente evitata e si desidera meccaanismo di sepgnimento e accensione a basso consumo energetico. A tal fine, i transistor a effetto di campo a capacità negativa (NC-FET) mostrano una forte promessa di superare il vincolo termoionico di Boltzmann di 60 mV/dec e di continuare lo scaling della tecnologia CMOS. Gli NC-FETs si basano sullo sfruttamento della regione NC della curva di polarizzazione-campo elettrico prevista dal modello Landau-Ginzburg-Devonshire (LGD).

Questa tesi si propone di studiare l'effetto NC e la sua interazione con i meccanismi di commutazione della polarizzazione di uno dei più importanti componenti dei ferroelettrici a base di HfO_2, l'HfO_2 drogato con Si (Si:HfO_2), per poi integrarlo in dispositivi elettronici. In primo luogo i condensatori con Si:HfO_2 sono stati misurati in un ampio intervallo di temperature e i risultati sono stati utilizzati per calibrare il modello LGD, confermando sperimentalmente il meccanismo di commutazione intrinseco. Quindi Si:HfO_2 è stato integrato nei gate del transistore per verificarne la funzionalità. In questo lavoro sono state studiate due strutture, una con un gate metallico interno (IG) situato tra l'isolante e il ferroelettrico e una struttura senza IG. Grazie alle misure con impulsi di nanosecondi, è stata estratta la curva a forma di S, prevista dal modello LGD, ed è stata osservata la regione NC.

In seguito allo studio precedente, i due stack gate sono stati integrati in una piattaforma

di transistor senza giunzioni (JLFET) con un canale Si di 10 nm e con Ion/Ioff di 6 ordini di grandezza. Il JLFET ferroelettrico (Fe-JLFET) senza IG ha una transcaratteristica priva di isteresi e una pendenza di sottosoglia migliorata del 35% con tensioni di gate a impulsi rispetto che a corrente continua. Al contrario, il Fe-JLFET con IG ha mostrato un comportamento isteretico ferroelettrico e la commutazione graduale Si:HfO_2 viene sfruttata per imitare la plasticità sinaptica. Inoltre, la tensione di back-gate viene utilizzato per regolare il peso sinaptico di oltre 400 volte.
Nel complesso, questo lavoro di dottorato conferma il potenziale del Fe-JLFET sia per le sinapsi neuromorfiche che per i dispositivi logici NC e mette in evidenza i requisiti e i limiti di funzionamento studiando come le proprietà ferroelettriche a base di HfO_2 si evolvono dal condensatore all'integrazione nel gate stack.

Parole chiave: ferroelettricità, HfO_2, commutazione intrinseca, Landau-Ginzburg-Devonshire (LGD), capacità negativa (NC), sinapsi neuromorfiche, transistor senza giunzioni (JL) (JLFET), transistor ferroelettrico (Fe-FET), Silicon-On-Insulator (SOI) wafer. italian

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1 Introduction

1.1 From More-Moore to Beyond CMOS approach

The events of these last two years were dramatic, with the entire world fighting against the first pandemic in a century. However, the need for remote communication, purchasing goods online, and handling business transactions pushed various parts of the electronics and informatics sector. Under normal circumstances, it would have taken far longer for so many technologies to grow naturally. Consequently, the market exploded in 2020, and in particular, consumer electronics revenues increased by 17% in the United States [1]. However, these last two years are just a continuation of the digital revolution that started in the 50s, which profoundly altered how we experience and interact with the world around us [2].

1.1.1 Evolution of semiconductor industry

Austrian physicist Julius Edgar Lilienfeld first introduced the basic principle of the field-effect transistor (FET) in 1926. As the cover of the electronic magazine "Crystal Triode" reported in Figure 1.1, the first working transistor was built by Shockley, Bardeen, and Brattain in 1947 at Bells Lab [3], for which they won a Nobel prize. Nevertheless, the discovery of Complementary Metal-Oxide-Semiconductor (CMOS) at Bell Lab in 1959 revolutionized the electronics industry. Thanks to the CMOS introduction, the digital electronic era enabled an increase in the transistor area density and, consequently, higher performance while keeping low power consumption.

Since the discovery of CMOS's capability, the semiconductor industry has spent its resources to shrink the physical size of transistors and increase their density. In 1965, Gordon Moore, thanks to his experience as co-founder of Intel and Fairchild Semiconductor, observed and predicted that the number of transistors in an integrated circuit doubles every two years. As shown in Figure 1.2, this empirical trend, called Moore's law, has been rigorously followed for several years till nowadays [5].

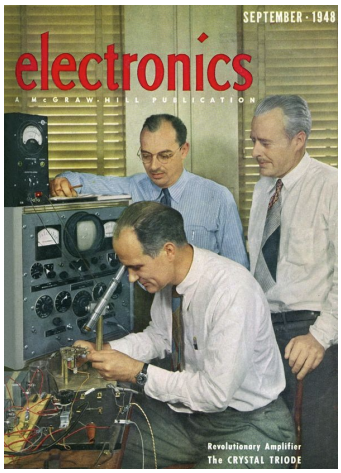


Figure 1.1: Cover of "Crystal Triode", an electronic magazine, showing Bardeen, Brattain, and Shockley in the Bells Lab where they built the first transistor. (Adapted from [4])

Reducing transistor size increased device density, i.e., less necessary space for a fixed transistor count. Furthermore, it improved performances by lowering the capacitances in the device and increasing the maximum operating frequency, as shown in Figure 1.3. Additionally, when transistors are scaled down, their power density remains constant, maintaining the power proportional to the area. This scaling principle is called Dennard's rules [7, 8] and allowed to follow Moore's trend strictly.

However, continuing this aggressive scaling was not a straightforward achievement [9, 10]. From the 1990s, power density became a critical concern due to the physical limitations of the transistor: scaling down transistor dimensions caused an increase in static consumption. In the 2000s, power density increased, reaching its maximum thermal limit above which the device's functionality and safety would have been affected. Since then, it became clear that Dennard's scaling was close to an end. Transistor density continues to increase at the expense of processor clock speed, which has remained invariant. However, to keep increasing the performance, multiple cores were added to split the tasks and reduce the power density per core, as highlighted in Figure 1.3. Although parallel calculations were proven effective, the system's complexity unavoidably grows as the number of cores increases. The processing design's complexity might also reach a limit beyond which increasing the parallelism is neither feasible nor efficient.

In the meantime, to continue the scaling several technological changes were made to sustain this rate of progress: lithography techniques were improved, new transistor designs from planar to 3D structure, the use of silicon-on-insulator wafer to reduce the off-current, and the use of strained silicon technique and novel dielectric materials to increase the on-current. Despite the substantial evolution of the CMOS technology, no significant changes were made in computer architecture. Indeed it had not been altered significantly since Von Neumann's introduction in 1945.

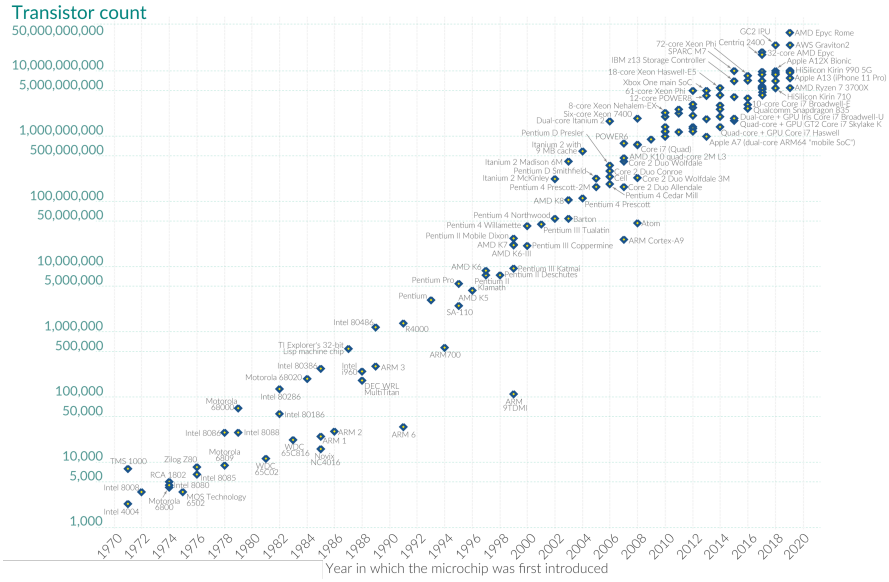


Figure 1.2: Exponential growth projection of transistor count in integrated circuits plotted vs the year of introduction (taken from [6]).

Nowadays, the technology node reaches 5 nm [12, 13], but the semiconductor manufacturers, TSMC and Samsung, announced the production of the 3 nm node by the second half of 2022 [14, 15]. However, continuing the scaling down may prove not economically viable, especially in developing infrastructures and lithographic tools, like extreme ultraviolet lithography [16]. This may be why GlobalFoundries, one of the biggest semiconductor industries, said it was stopping at the 10 nm technology. As a result, only Intel, Samsung, and TSMC remained in the semiconductor market to produce smaller transistors. Even these colossus may eventually be unable to balance the cost, revenues, and danger of continuing the node scaling down.

In contrast to the "More Moore" approach, which imposes speed and density limitations on devices due to heating issues, International Roadmap for Devices and Systems (IRDS) identified the "Beyond CMOS" approach as a possible future digital technology. This paradigm is focused on finding great performance systems working at low-lower consumption, as shown in Figure 1.4. The research focuses on alternatives to traditional random-access memory (RAM), such as Phase-Change RAM (PCRAM), Resistive RAM (ReRAM), Magnetic RAM (MRAM), and Ferroelectric RAM (Fe-RAM) [17]. Also, novel emerging devices with low power switching are investigated, like Negative Capacitance FET (NCFET) and Tunnel FET (TFET). Another approach is to change the computing architecture. Recently a heavy focus has been placed on novel computing paradigms like neuromorphic or quantum computing.

In the following sections, two energy-efficient solutions that operate with ferroelectric material are discussed in detail: NCFETs, as an emerging low-power device (Section 1.1.2), and neuromorphic computing, as a novel energy-efficient architecture (Section 1.1.3).

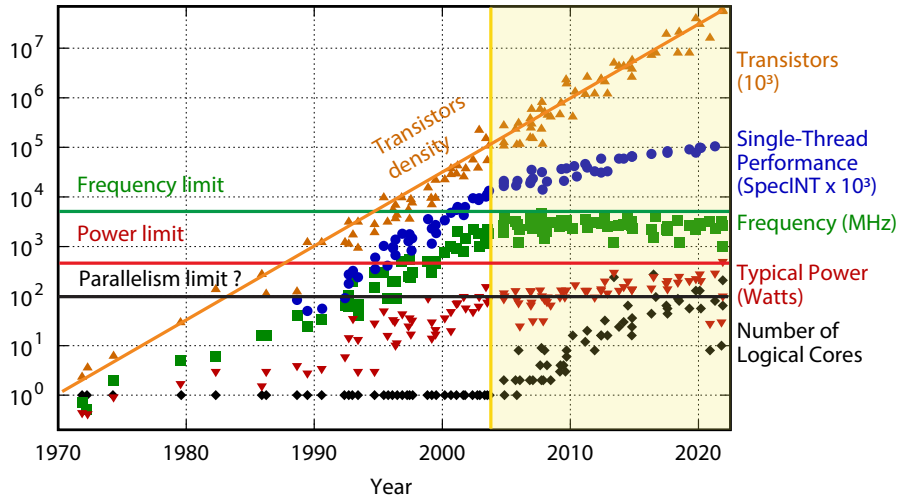


Figure 1.3: Microprocessor scaling trends throughout 52, highlighting the end of Dennard scaling after the 2000s (adapted from [11]).

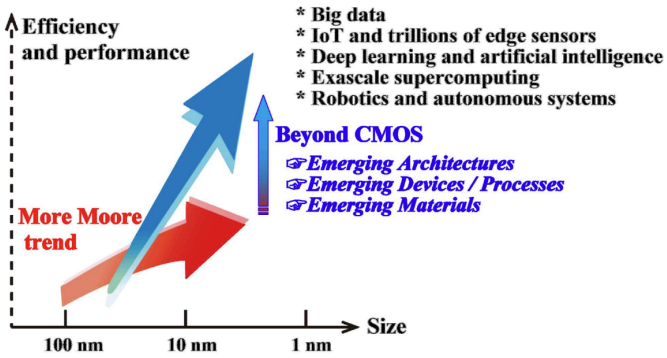


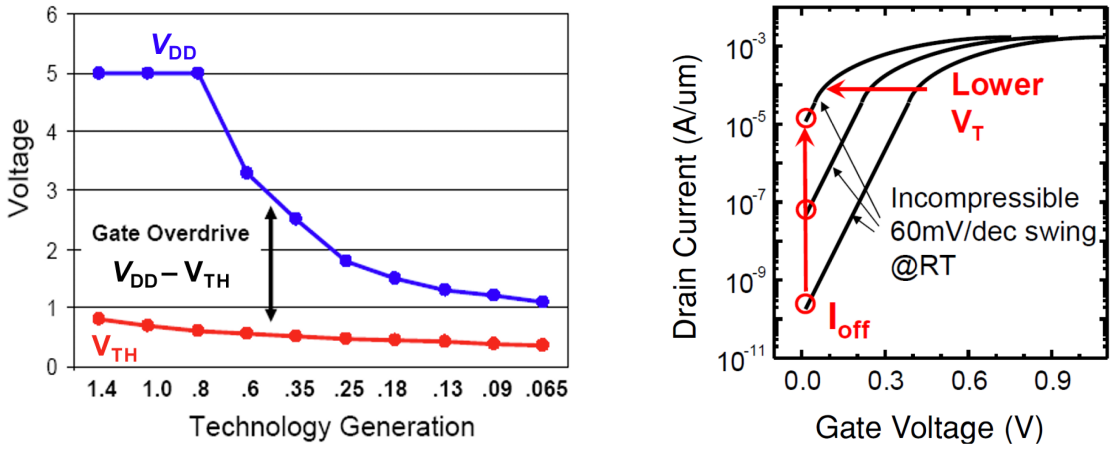
Figure 1.4: Schematic showing the objective of Beyond CMOS vs More Moore approach (taken from [18]).

1.1.2 Negative capacitance FET as energy efficient logic device

As mentioned in Section 1.1.1, starting from the 1990s, Dennard scaling arrived at the end. The supply (V_{DD}) and the threshold voltages (V_{TH}) could not be scaled anymore of the same factor, as shown in Figure 1.5(a). This choice was made to limit the exponential increase of off-current (I_{off}) with the V_{TH} (Figure 1.5(b)) since I_{off} is proportional to static power ($Power_{static}$):

$$Power_{static} = I_{off} V_{DD}. \tag{1.1}$$

A way of reducing the power dissipation is to increase the turn-on steepness, which means decreasing the average subthreshold swing (SS), which is defined as:



(a) (b)

Figure 1.5: (a) Scaling trend of V_{TH} and V_{DD} with respect to CMOS technology (adapted from [19]). (b) Schematic showing that a linear increase of V_{TH} causes an exponential rise of I_{off} value because of the incomprehensibility of the swing (from[20]).

$$SS = \frac{\partial V_G}{\partial log I_D} = \frac{\partial V_G}{\partial \psi_S} \times \frac{\partial \psi_S}{\partial log I_D}, \tag{1.2}$$

where V_G, I_D, and ψ_S denote the gate voltage, the drain current, and the surface potential of the semiconducting channel, respectively. The first term of Equation 1.2 is the body factor, also called m-factor which is usually greater than 1. It can be rewritten as:

$$m = \frac{\partial V_G}{\partial \psi_S} = (1 + \frac{C_S}{C_{OX}}) \tag{1.3}$$

where C_{OX} and C_S are respectively the capacitance gate oxide and semiconductor capacitance. The second term on the right is known as the n-factor, and in the case of MOSFETs with thermionic injection mechanism is equal to:

$$n = \frac{\partial \psi_S}{\partial log I_D} = \frac{KT}{q} ln10 \tag{1.4}$$

where k is the Boltzmann constant and T is the temperature. In this case, the minimal n-factor value is equal to 60 mV/dec at 300 K. This limits the transistor turn-on steepness by imposing a minimum SS.

One of the techniques proposed to get energy-efficient devices is to reduce the SS. As shown in Figure 1.6 several steep switching devices are proposed, either by reducing the n-factor or the body factor.

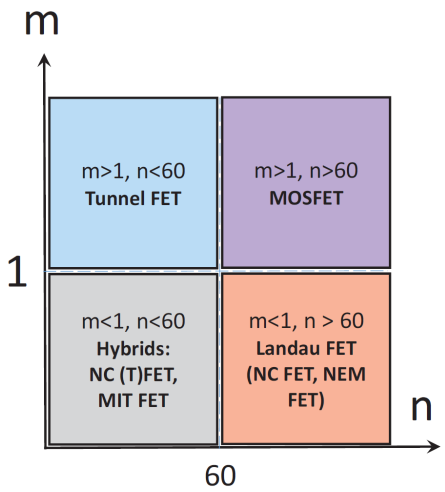


Figure 1.6: Map of FET design space (adapted from [21]).

Among those TFET [20] is one of the most common devices proposed in the literature. Its SS is no more limited by the thermionic injection since it works based on a tunneling mechanism and, therefore, can be smaller than 60 mV/dec. Another method to reduce the SS is to have m-factors smaller than 1. It can be obtained by introducing a negative capacitance inside the field-effect transistors using a so-called Negative Capacitance FET, (NC-FET) [22]. Figure 1.7(b) shows the comparison between transfer characteristics obtained with a MOSFET (blue curve) and a NC-FET (red curve).

The turn-on steepness is obtained by adding a ferroelectric material to the gate stack on top of the linear insulator, as shown in the schematic of Figure 1.7(b). The subthreshold swing (SS_{FE}), can be rewritten as follows:

$$SS_{FE} = SS_{min}\,(1+\frac{C_{OX-S}}{C_{FE}}) = 60\,\frac{mV}{dec}\,(1+\frac{C_{OX-S}}{C_{FE}}) \tag{1.5}$$

where C_{OX-S} is the series capacitance of the gate oxide and the silicon, while C_{FE} is the equivalent ferroelectric capacitance. Consequently, if $C_{FE} < 0$, the SS_{FE} becomes steeper than $60 mV/dec$ an internal amplification of the voltage occurs. This happens when the transistor works in a negative capacitance regime offered by the intrinsic ferroelectric switching described in Section 1.2.3. This idea, which aroused great interest in the device community, was first proposed by Salahuddin in 2008 [22] and then validated by several experimental results[24, 23, 25, 26, 27].

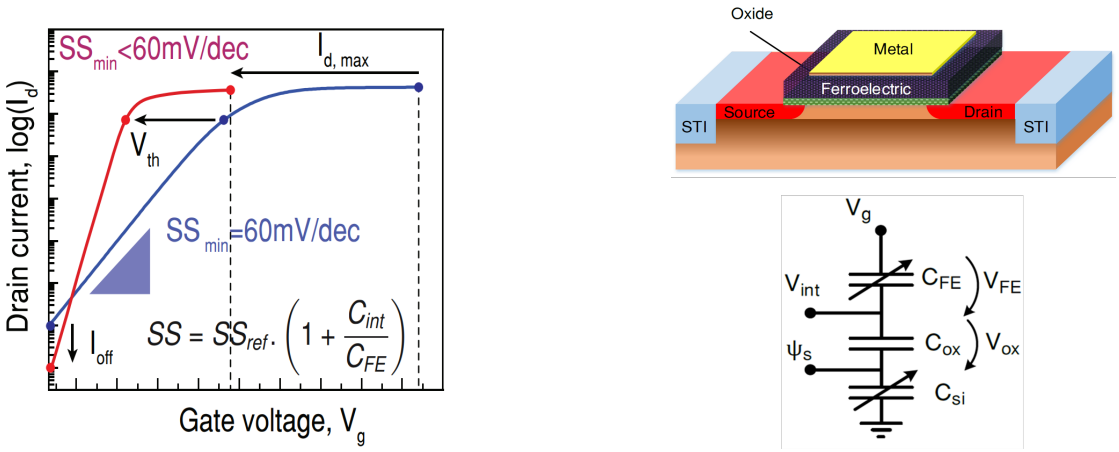


Figure 1.7: (a) Comparison of transfer characteristics obtained with a MOSFET (blue line) and a NC-FET (red line); SS improvement and threshold voltage reduction highlighted.(Adapted from [23]) (b) Structure of a generic ferroelectric transistor (from[24]) and its equivalent capacitance model.

1.1.3 Neuromorphic computing

In von Neumann's architecture, the exchange of data between the central processing units and the main memory is performed by share buses, which limit the throughput and increase the processing time and power consumption [28] [29]. Nowadays, to overcome Von Neumann's bottleneck, other emerging computing systems are proposed. Among the different strategies, one of the most studied is quantum computing, which makes use of physical phenomena like superposition and entanglement to solve some categories of classically intractable problems [30]. Another potential new solution, which attracted much attention in the last few years, is neuromorphic computing. This paradigm is intuitively inspired by a computing technology existing already in the realm of biology: the brain. Contrary to Von Neumann, the human brain can achieve efficient data processing thanks to combining memory and computation in the same unit by mean neurons and synapses.

The neuron is a nerve cell generally composed of a nucleus called soma, several dendrites, which receive the information to the pre-synaptic neurons, and an axon that transmits the information to a post-synaptic neuron. The soma processes the signal coming from dendrites. If it is strong enough, an electric signal, called an action potential, is fired to the axon terminal. The communication between neurons occurs through a specialized structure called synapses, shown in Figure 1.8. The pre-synaptic neuron contains neurotransmitters packed into vesicles. When a pre-synaptic neuron is excited by an action potential, the neurotransmitters are released into the synaptic cleft and interact with post-synaptic receptors, causing the generation of an action potential in the dendrites terminal. The connection strength between two neurons depends on the transmission history, and it is called synaptic weight. Synaptic

plasticity refers to the increase (potentiation) or decrease (depression) of the synaptic weight change. In conclusion, thanks to the massive interconnection between 10^{11} neurons and 10^{15} synapse, the brain performs energy-efficient and parallel data processing.

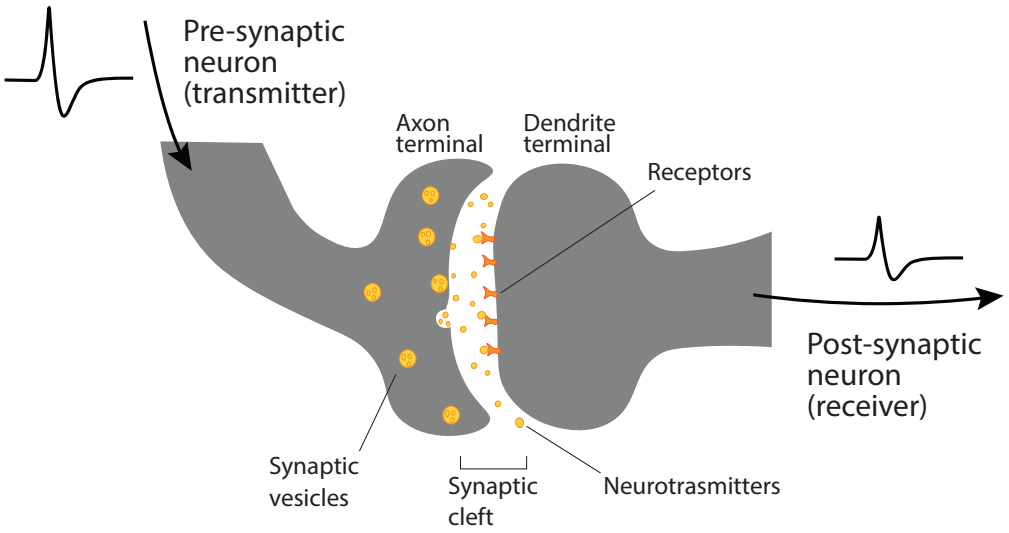


Figure 1.8: Schematic of a synaptic transmission mechanism showing a firing pre-synaptic neuron releasing neurotransmitters binding to receptors of the post-synaptic neuron.

Up to now, the potential of neuromorphic computing has been mainly tested using machine algorithms and classical CMOS-based hardware. However, these solutions require high power consumption and have a low learning speed [31, 32], and bio-inspired hardware has to be introduced to mimic the low power computing of neurons and synapses.

Several emerging memories [33] have been considered to mimic the synaptic functionality. Among those, ferroelectric transistors (Fe-FET) have attracted considerable attention as promising candidates thanks to multistate capabilities, which emulate synaptic plasticity, and low-power switching [34, 35, 35].

1.2 Ferroelectricity

As discussed above, one possibility to improve power efficiency in systems and devices is the introduction of ferroelectric materials. They are a dielectric material class that possesses a spontaneous electric polarization reversible by an external electric field. Thanks to their broad spectrum of properties, they are suitable for numerous applications, such as:

- memory and neuromorphic application [36, 37](due to their highly reversible polarization)
- negative capacitance [22] (thanks to the intrinsic polarization switching)
- sensors and actuators [38, 39](given their piezoelectric and pyroelectric properties)

- electrostatic supercapacitors and energy harvesting [40, 41] (due to energy conversion based on piezoelectric and pyroelectric effect)

This dissertation will focus on two energy-efficient applications, negative capacitance and neuromorphic applications. In the first class of application, the digital information is stored through spontaneous polarization, and having a large hysteretic window is fundamental for a correct reading of the stored data.

In the second class, hysteresis is avoided, and the ferroelectric is used to have a steeper subthreshold swing in the transistor by an internal amplification of the voltage. Ferroelectric NC devices rely on the exploitation of the NC region of the polarization-electric field (P-E) curve predicted by the Landau-Ginzburg-Devonshire (LGD) model, as discussed in Section 1.2.3).

1.2.1 History

Ferroelectricity was discovered 100 years ago, in 1921 [42] by a Ph.D. student called Joseph Valasek, working under the supervision of William Swann at the University of Minnesota in Minneapolis. He was investigating the dielectric properties of Rochelle salt while noticing that the polarization switched in a hysteretic way by applying an electric field. However, from an application point of view, one of the major turning points was the discovery in 1946 of BaTiO3 [43], an inorganic compound with a perovskite structure. Unlike Rochelle salt, it is insoluble in water, chemically stable at room temperature, and with better electromechanical properties. Since then, ferroelectric material has been widely used in diverse fields, including sensors, actuators, and memories. After these discoveries, many structural families of ferroelectric were identified; among them, it is worth remembering the first ferroelectric polymer (PVDF) in 1971 [44].

In the meantime, the discussion about the theoretical backgrounds of these materials progressed considerably with the work of Devonshire. He developed the phenomenological theory of ferroelectrics built upon the earlier ideas of Landau and Ginzburg. It resulted in the LGD theory published in 1949 [45], which takes as a reference BaTiO3. One of the last breakthroughs is the discovery of a new major class of ferroelectric materials based on HfO_2. This occurred in 2011 with the identification of Si-doped HfO_2 (Si:HfO_2) ferroelectricity by Böscke et al [46]. Ferroelectric HfO_2 became the focus of significant attention because, contrary to conventional ferroelectric, it offers CMOS compatibility in thin layers, making it the perfect candidate for Fe-RAM [36, 47].

In this section, the basic concepts of ferroelectricity, relevant to the present thesis work, are briefly introduced, together with the thermodynamic switching model. To conclude the section, HfO_2-based ferroelectric are presented.

1.2.2 Fundamentals of ferroelectricity

Ferroelectric materials are part of the dielectric material category. Among 32 symmetry point groups of crystalline materials, 20 non-centrosymmetric groups are compatible with piezoelectricity. Thanks to their lack of symmetry, it is possible, by applying mechanical stress, to polarize the material by displacing the atoms inside the unit cell. This effect is called the direct piezoelectric effect and is used for sensors application. Moreover, also the opposite effect is valid; by applying an external voltage drop, one can observe the deformation of the piezoelectric. The inverse piezoelectric effect is the working principle of actuators.

Out of the 20 point groups of crystalline materials, 10 groups are polar i.e. possess at least one unique direction that cannot be altered by symmetry operations. This direction is called polar because electric polarization in this direction is permitted by symmetry. A variation in temperature affects material polarization. In view of their properties, they were called pyroelectric. Ferroelectric materials are a subgroup of pyroelectric. Even though they share the same crystallographic structure, ferroelectric polarization can be switched in the opposite direction by the application of an electric field. Figure 1.9 depicts the classification of dielectric materials by means of the Van diagram, which enforces the concept that not all piezoelectric crystals are ferroelectric, but all ferroelectric crystals are piezoelectric.

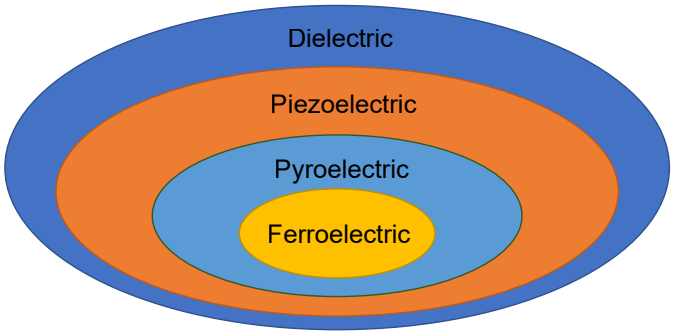


Figure 1.9: Venn diagram showing the relationship between dielectric, piezoelectric, pyroelectric, and ferroelectric materials.

Even in the absence of an electric field, a ferroelectric material has a spontaneous electric polarization (P_S), which can be switched by applying an external electric field larger than the coercive field (E_C). This behavior gives rise to a hysteretic behavior observable in the polarization vs. electric-field plot ($P-E$).

In capacitor structure, the ferroelectric response is typically studied by monitoring the transient current while applying an electric field, as shown in Figure 1.10(a). The polarization is obtained by integrating the current in time, obtaining the hysteretic $P-E$ plot depicted in 1.10(b). The intercept of the y-ax is called remnant polarization (P_R), and the intercept of the x-axis is the coercive electric field.

However, if the temperature increases over a certain threshold called Curie temperature (T_C),

the material loses ferroelectricity because it transitions to a centrosymmetric crystal, and as a consequence, it behaves as paraelectric. In the next section, the thermodynamic theory is briefly outlined.

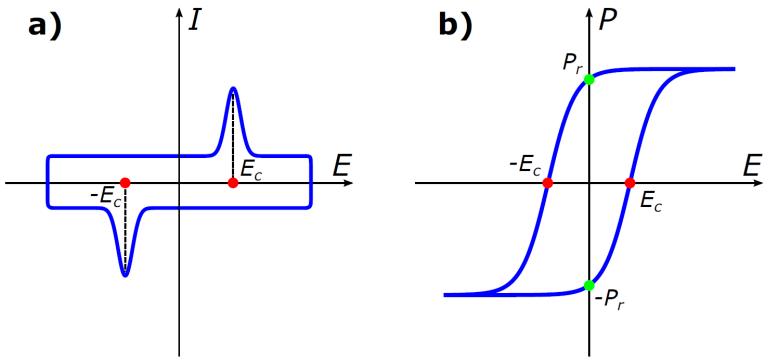


Figure 1.10: (a) Displacement current vs. electric field and (b) hysteresis loop (P-E) derived from it (adapted from [48]).

1.2.3 Phenomenologoical theory of ferroelectric phase transitions

The phenomenological thermodynamic theory, also called LGD theory, arose from the necessity to explain the ferroelectric to paraelectric phase transformation when the temperature is higher than Curie temperature. Here, for the sake of simplicity, the thermodynamic theory is described in a one-dimensional case, and polarization and applied electric field vector are considered parallel. The Gibbs free energy density (G) described within LGD theory [49, 50, 51, 45], can be expressed as a polynomial expansion up to the sixth order:

$$G = \frac{\alpha}{2} P^2 + \frac{\beta}{4} P^4 + \frac{\gamma}{6} P^6 - P\,E \tag{1.6}$$

where α, β and γ are Landau coefficients dependent on the material. The order parameter of Equation 1.6 is the polarization (P) since the dielectric displacement is equal to P when no electric field (E) is applied. Notably, the coefficient α represents the reciprocal of the dielectric susceptibility, and it deserves particular attention because it is the only temperature-dependent Landau coefficient. The following conditions must be satisfied to derive its temperature dependence: the minimization of G, to change of sign T_C and guarantee continuity below and above T_C. Following the requirement, α can be expressed with a linear temperature dependence:

$$\alpha = \frac{(T - T_C)}{C} \tag{1.7}$$

Equation 1.7 is called Curie-Weiss law, and C is the Curie constant. If the temperature is lower than T_C, α is negative, and the energy state has two minimum in correspondence to the stable ferroelectric states. On the contrary, if it is higher than T_C, α is positive, and it shows just one minimum at $P = 0$, which means that the material encountered a phase transition from ferroelectric to paraelectric. Figure 1.11(a) illustrates the effect of the phase change on the energy landscape and on the polarization.

The sign of the β coefficient defines the phase transition type. If positive, the phase transition is called the second-order transition. On the contrary, if it is negative, the phase transition is called first-order. Conversely to the other coefficients, γ is always positive, and its value is smaller than the others.

By minimizing G with respect to the polarization in Equation 1.6, the equation of state of ferroelectric is derived, which yields the relation between the electric field across the ferroelectric and the polarization:

$$\frac{\mathrm{d}G}{\mathrm{d}P} = 0 \quad \Rightarrow \quad E = \alpha P + \beta P^3 + \gamma P^5 \tag{1.8}$$

As shown in the red curve of Figure 1.11(b), Equation 1.8 displays an S-shaped polarization curve, which has a negative slope region with negative equivalent permittivity ($\epsilon_R \propto dP/dE$). This region corresponds to the area where there is the local maximum of the energy, as illustrated by red curve in Figure 1.11(a). The negative capacitance region is unstable and can not be experimentally observed in standard ferroelectric capacitor measurements. However, it can be exploited to get a differential voltage amplification in FET if integrated into the gate stack of a FET.

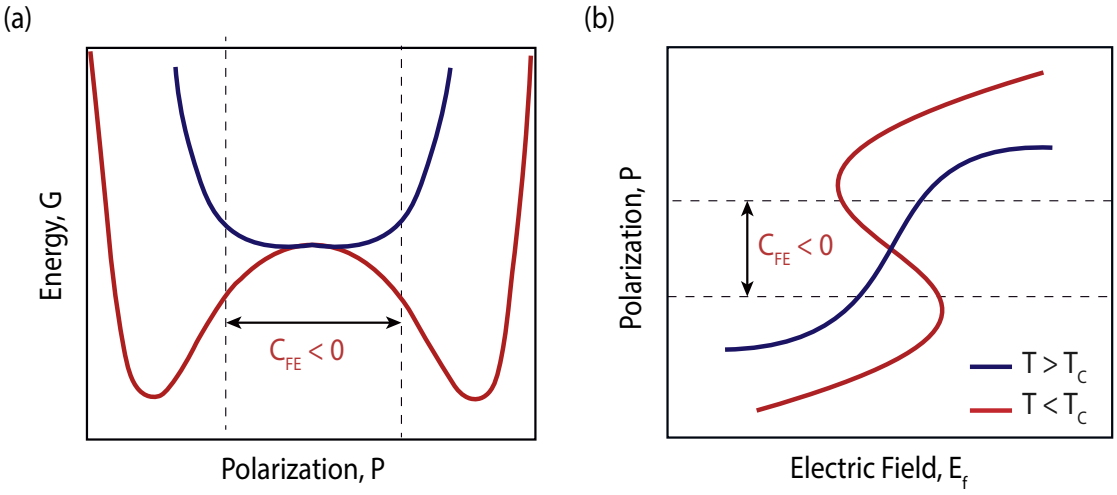


Figure 1.11: Schematic of the energy landscape and polarization behaviour in the ferroelectric phase ($T < T_C$) and in the paraelectric($T > T_C$).

Furthermore, from Equation 1.8 one can retrieve essential parameters related to polarization hysteresis in terms of the Landau coefficients. The free energy presents one maximum around $P = 0$, which is the unstable NC state, and two minima, which are the two stable states, such as the positive and negative spontaneous polarization P_S, which can be calculated as follow:

$$P_S = \pm\sqrt{\frac{-\beta + \sqrt{\beta^2 - 4\alpha\gamma}}{2\gamma}} \tag{1.9}$$

It can be shown that if $\beta > 0$ and $T < T_C$ $\gamma \approx 0$, and LGD theory offers a simpler description of P_S:

$$P_S = \pm\sqrt{-\frac{\alpha}{\beta}} \tag{1.10}$$

In this last case, with negative β, the spontaneous polarization value reduces gradually with temperature until it reaches $P_S = 0$ at the Curie temperature (Figure 1.12(b)). On the contrary, if $\beta > 0$ and $\gamma > 0$, the spontaneous polarization value decreases little with temperature and at $T = T_C$ jumps to zero. As it is illustrated in Figure 1.12(a), it generates a discontinuity of a first-order, from which it takes its name.

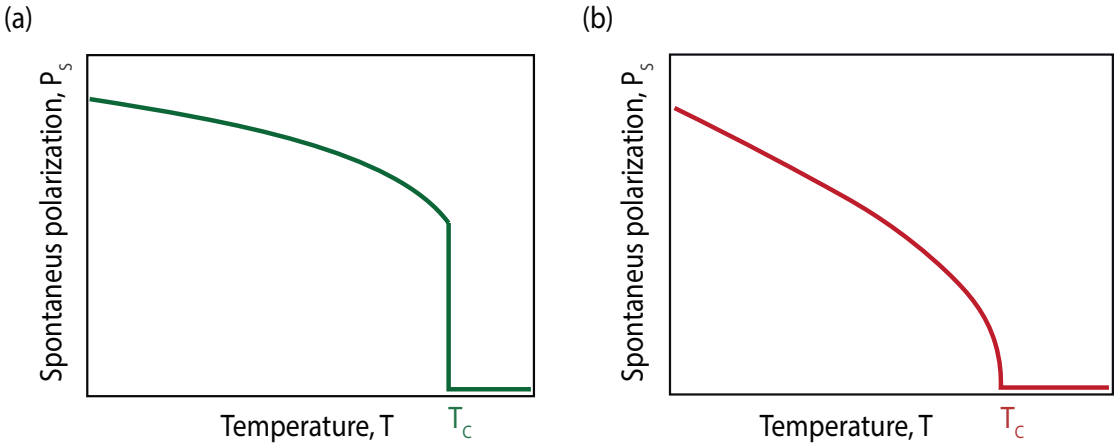


Figure 1.12: Schematic of spontaneous polarization temperature dependence in case of first order (a) and second order (b) phase transition.

1.2.4 HfO_2-based ferroelectric

Perovskites, which are arguably the most studied and used ferroelectrics, have excellent ferroelectric properties and a very high dielectric constant. For this reason, they are used for different ranges of applications. However, if integrated into microelectronic technology, they have two main disadvantages: Pb diffusion that leads to CMOS incompatibility and instability of the material at smaller thickness [47].

The extensive investigation of HfO_2 as a high-κ gate dielectric [52, 53, 54] brought to light that

if this material is subjected to certain stress, it reveals ferroelectricity. One of the first studies appeared in 2011 when Böscke et al. [46, 55] revealed ferroelectricity in Si:HfO_2 thin films deposited with ALD technique.

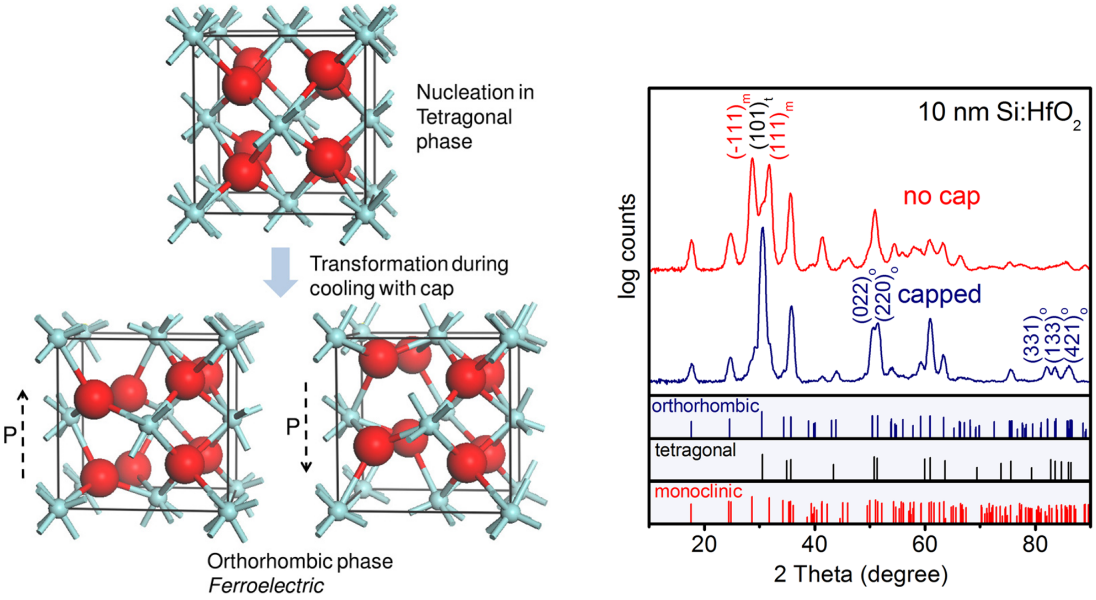


Figure 1.13: (a) Schematic of the Si:HfO_2 unit cell before the annealing with TiN as capping electrode and after, showing the transformation from tetragonal phase (paraelectric) to orthorhombic (ferroelectric). (b) Grazing incidence x-ray diffraction measurements with the TiN capping (typical for orthorhombic phase) and without (typical for tetragonal/monoclinic phase). Reproduced from [46])

At room temperature, the most stable crystal structure of HfO_2 is the monoclinic one, but if subjected to higher temperature (T), it shows a phase transformation into tetragonal (T > 1700 °C) and then cubic phase (T > 2600 °C) [56]. However, new studies [46, 55] showed that, if enough pressure is applied, it can transform into a non-centrosymmetric orthorhombic phase, which is believed to be the origin of ferroelectricity. In this crystallization phase, the unit cell is composed of Hf^{4+} cations (at corners) and O^{2-} the anions (at the eight tetrahedral interstitial sites). As depicted in Figure 1.13a the polarization switching originates from a movement of O^{2-} anions inside the interstitial sites of the orthorhombic unit cell.

In the first studies, [46], the stabilization of the orthorhombic phase, together with some monoclinic one, was reached by capping Si:HfO_2 with TiN before the annealing step, to build an in-plane strain in the thin film (Figure 1.13b). Furthermore, Figure 1.14 shows that an optimal concentration window between 2.6 mol% and 4.3 mol% is needed to observe ferroelectricity. When the concentration is larger than 4.3 mol%, it leads to an anti-ferroelectric HfO_2, and above 6 mol%, to a linear dielectric behavior.

Later it was shown that, by creating a lattice distortion into HfO_2, other dopants could help

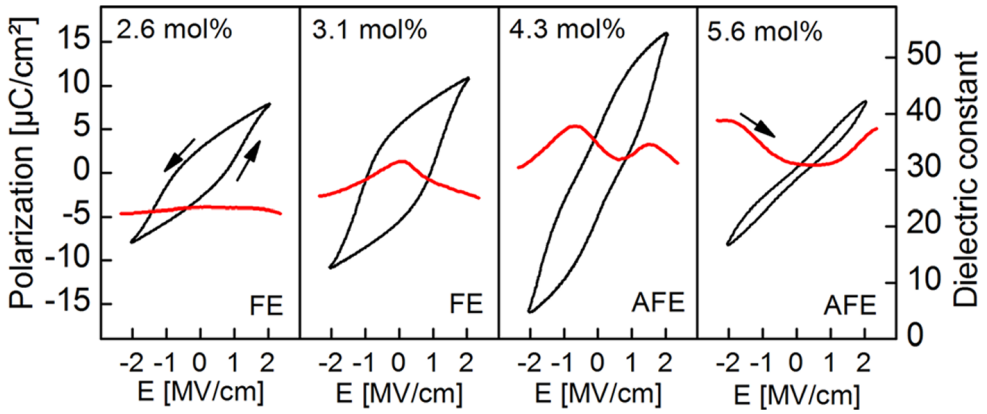


Figure 1.14: Polarization-Voltage (black) and Dielectric constant-Voltage (red) characteristics of a series of capped HfO_2 capacitors showing a gradual transition from ferroelectric to anti-ferroelectric behavior with the increase of the Si doping (reproduced from [46]).

stabilize the orthorhombic phase. It was demonstrated with Al [57], Gd [58], La [59], Sr [60], Zr [61] and Y [62], but remarkably also undoped HfO_2 was proven to show ferroelectricity below 7 nm [63].

Another important property that influences ferroelectricity is thickness. It was discovered that thin HfO_2 layers (< 30 nm) show a higher remnant polarization [64]. Later it was proven that this trend originated from the fact that the small grains in thin films tend to favor the crystallization of the orthorhombic phase [65]. However, this trend does not continue for very thin layers [66], below 10 nm, the polarization degrades. A root cause can be found in the formation of a dead layer that forms between the ferroelectric and the electrode. As it is known from previous studies on perovskite material, when the dead layer becomes comparable to the ferroelectric one, the depolarization gets stronger and reduces the spontaneous polarization [67]. It's worth mentioning that in the presence of TiN electrodes, one can observe the generation of a non-ferroelectric layer rich in oxygen vacancy, which tens to stabilize in the tetragonal phase [68, 69]. This behavior is attributable to the scavenging propriety of TiN, which binds to oxygen atoms and forms a rutile TiO_2 and TiO_xN_y layer [70, 69]. Nevertheless, TiN remains a good candidate in CMOS application [71], thanks to its thermal stability, good electrical conductivity, and chemical stability (it is used as a diffusion barrier).

As already mentioned at the beginning, one of the most essential factors in stabilizing the orthorhombic phase is the annealing conditions, in terms of thermal budget (time and temperature) [72] and atmosphere condition [73]. Also, the deposition temperature influences HfO_2 ferroelectricity, it was proven that the best condition to deposit it by ALD is a temperature between 300 °C and 800 °C, based on the doping type [72, 74].

Furthermore, another factor that is affecting ferroelectricity is electric field cycling [75, 76, 68]. HfO_2 based ferroelectric generally requires some electrical cycling to improve the polarization

value and reduce leakage current; this procedure is called wake-up [77]. However, if cycled more than a certain threshold, ferroelectric degradation, also called fatigue [78, 79], starts to occur. At first, the origin of the wake-up behavior was believed to be induced by electric-field phase transiti. However, then the hypothesis of oxygen vacancies redistribution by cycling seemed to be the primary mechanism [80].

In conclusion, as shown in Figure 1.15, several factors can stabilize the orthorhombic phase and the ferroelectric properties:

- annealing conditions (time, temperature, and atmosphere)
- dopants type and content
- film thickness and grain size

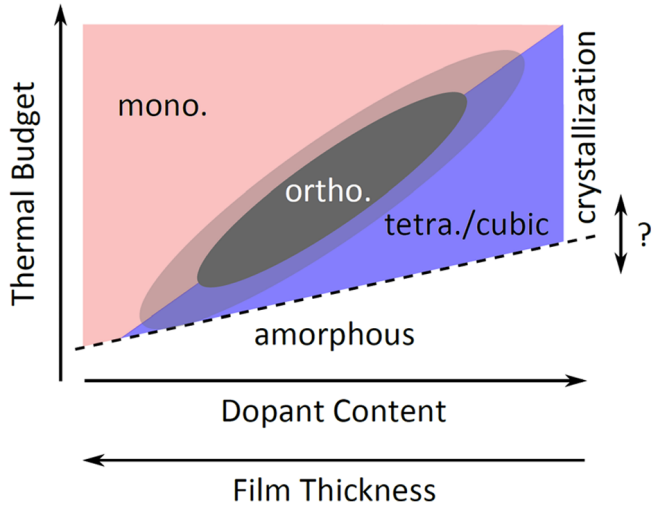


Figure 1.15: Qualitative schematic of the phase transitions of HfO_2 and its trend with annealing, doping, crystallization and film thickness (reproduced from [80]).

1.3 Junctionless FET as the platform for a ferroelectric transistor

Since the first publication in 2009 [81], junctionless (JL) transistors have become a popular device among research groups [82], and they are used for applications like gas detectors and chemical sensors [83, 84].

As illustrated in Figure 1.16, the device channel is made of a highly and uniformly doped silicon, which behaves as a resistor modulated by the gate voltage. Although the JLFET structure is similar to a metal oxide field-effect transistor (MOSFET), the key difference is the absence of source (S) and drain (D) junctions.

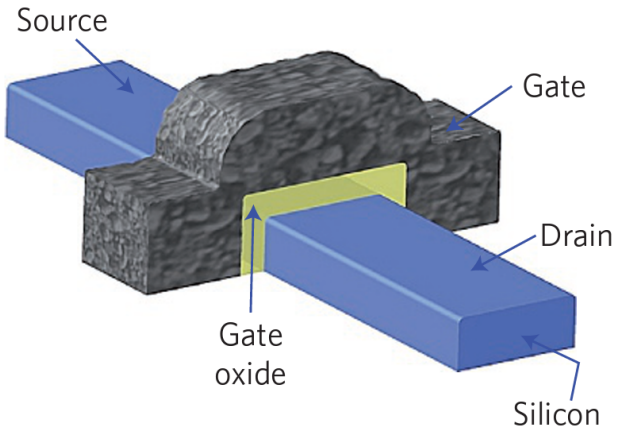


Figure 1.16: Schematic of a JLFET with a highly uniform doped silicon channel and no drain and source implantation. Reproduced from [85]

Considering a p-type JLFET having a metal gate work-function, which is not depleting the Si. If a positive gate voltage is applied, the channel gets fully depleted, and the transistor is turned off. On the contrary, if the gate voltage is negative, the transistor is on. The reversed behavior occurs if the Si is n-type doped. Figure 1.17 shows the transfer characteristic of a JLFET n-type and p-type compared to a classical trigate n-type MOSFFET. The devices look remarkably similar even though the physics behind them is different: no inversion mode occurs in JLFET.

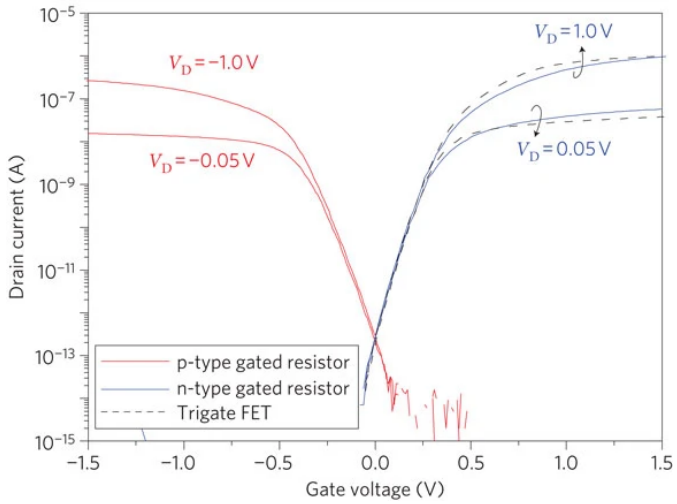


Figure 1.17: Transfer characteristic taken of a JLFET of n-type, p-type compared to a classical trigate MOSFFET n-type. Reproduced from [85].

It is worth mentioning that in the design, one should remember that the Si thickness must be small enough so that the gate can completely deplete the heavily doped channel. Generally, the transistor is fabricated on an oxide layer or using an SOI wafer to define the Si channel and electrically insulate to the bulk.

The absence of junctions is beneficial for many factors. It simplifies the process fabrication for the scaled device since there is no need for ultra-sharp doping concentration gradients. Consequently, there are fewer limitations on the thermal processing budget. Hence, a simpler process results in cost reduction. Furthermore, in scaled devices and in the absence of source and drain junction, some short-channel effects, such as drain-induced barrier lowering, are less critical in scaled devices. Additionally, JLFETs have the potential to operate faster than the conventional transistor, thanks to the absence of parasitic capacitance at S and D.

Contrary to inversion-mode FET, where the conduction is located at the top Si surface, most carriers flow in the whole Si channel. Consequently, they show a lower mobility degradation with gate voltage and temperature compared to standard inversion-based MOSFET, in which the mobility is affected by surface scattering. However, the mobility degradation due to impurity is higher because of the high doping concentration.

This work uses JLFET as the platform to fabricate ferroelectric JLFET (Fe-JLFET) by integrating Si:HfO_2 in the gate stack. The final goal is to manufacture steep slope switches and devices for neuromorphic applications.

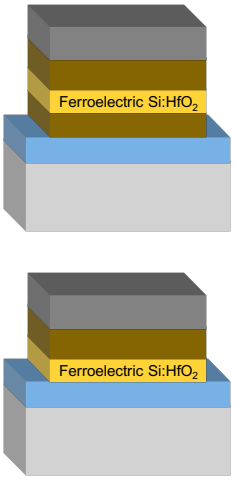
1.4 Thesis outline

The thesis is structured in building blocks; it starts from the capacitor, then gate stacks, and finally, FET.

Chapter 2: Si:HfO_2: ferroelectric fabrication and switching mechanisms study

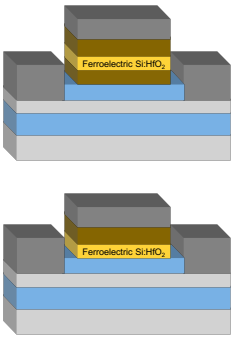
This second Chapter studies Si:HfO_2 capacitor, also called Metal-Ferroelectric-Metal (MFM) device, and it provides parameters for ferroelectric devices design and manufacturing, described in the next Chapters. It starts with the fabrication and characterization of the fabricated device. Then, it shows fabrication optimization of the Si:HfO_2 in terms of annealing temperature and thickness to tackle application relevant requirements. The analysis of variance is performed to research the parameters mainly affecting the polarization. To conclude, the Chapter reports the study of Curie-Weiss law and intrinsic switching implications for NC-FET.

Chapter 3: HfO_2–based bilayer gate stack structure



This Chapter is focused on the investigation of heterostructures where a dielectric layer is placed in contact with the ferroelectric. This configuration is of great interest since it allows accessing NC regime in the ferroelectric material and can be helpful for the engineering NC-FET. In the first part, a comparison between Si:HfO_2 gate stack devices with and without metal interlayer is performed to investigate the structure to use in the FET architecture. For this purpose, we used electrical measurement in the quasi-static regime and ultra-fast (200 MHz). To get more insights into the integrated ferroelectric property, we carried out a microscopic electromechanical characterization. To corroborate the previous on gate stacks devices results and increase the knowledge on HfO_2-based ferroelectric, a similar study is performed on the HZObilayer device. Finally, comparing different measurement approaches, we draw a conclusion on which the possible polarization reversal mechanism occurs in the ferroelectric-dielectric bilayer.

Chapter 4: Ferroelectric Junctionless FET



The fourth Chapter reports Fe-FETs, which uses JLFET technology and Si:HfO_2 (optimized in Chapter 2) as ferroelectric. Based on the in-depth study of the gate stack in Chapter 3, the Fe-JLFETs presented here have two ferroelectric gate stacks targeting opposite applications. The gate stack with an internal metal interlayer is employed for neuromorphic devices and the one without for NC steep slope switches. The NC-JLFET fabrication is described step by step, followed by a ferroelectric analyst by PFM to verify the integration. Then an in-depth characterization is performed both in DC and pulse mode.The fabricated neuromorphic device consists of double-gate Fe-JLFET acting as a three-terminal synapse, capable of emulating the functionality of biological tripartite synapses by ferroelectric gradual switching. The back-gate voltage is used to tune further the synaptic weight. The proposed Fe-JLFET synapse device is tested with different pulse schemes, at various temperatures, and for several cycles.

Chapter 5: Conclusion and future work

The last Chapter outlines the main achievements of this dissertation and proposes the research directions left open by this thesis and in the broader context of HfO_2-based ferroelectric devices.

2 Study of growth and ferroelectric switching of Si:HfO_2 thin films

This second Chapter report the study on Si:HfO_2 capacitor, which will be integrated into logic and memory device in Chapter 4. Section 2.1 describes the fabrication techniques adopted to manufacture it. The consequent microstructural, electrical, and electromechanical analysis are illustrated in Section 2.2, 2.3 and 2.4, respectively. To get an optimal fabrication recipe for the targeted application, we examined the impact of the ferroelectric thermal budget and thickness on the polarization and the leakage current (Section 2.5). Finally, Section 2.6 reports the study of temperature-dependent switching in Si:HfO_2 capacitor, which can give insight into the highly debated switching mechanism. This work is based on the work presented in [86].

2.1 Fabrication

This section describes the fabrication technique used to deposit Si:HfO_2 and the process flow to realize the capacitor structures, which is the building block of all the devices manufactured in this dissertation.

2.1.1 Atomic layer deposition

Atomic layer deposition (ALD)[46] is the deposition generally use for Si:HfO_2. ALD is a mature thin-film deposition technique already used in the microelectronic industry to deposit HfO_2 for high-κ gate stacks. ALD belongs to the family of chemical vapor deposition (CVD) processes. It consists of growing the material by a controlled chemical reaction of precursors on the substrate surface inside a reactor chamber. It is worth mentioning that the substrate surface should be either functionalized or naturally possess functional groups that can react with the precursor.

The sample is first placed inside the reactor, in which pressure and temperature are controlled. Then, the first precursor is added and reacts with the surface of the sample by chemisorption to form a monolayer. After this step, the reactor is purged with an inert gas (e.g. N_2) to eliminate by-products and remains of the precursor. Afterward, the second precursor is injected, and

then the chamber is purged. As shown in Figure 2.1 the four previous steps are repeated until the desired thickness is reached. This means that the growth is self-limited and that every cycle of deposition corresponds to one atomic layer growth, hence the origins of the name ALD.

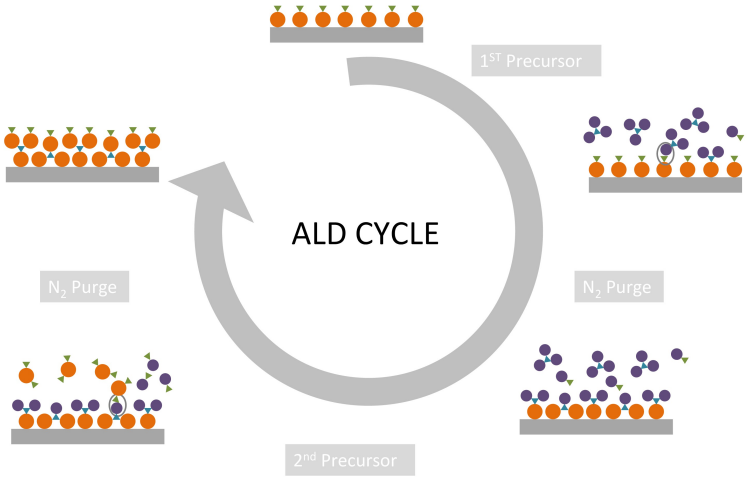


Figure 2.1: Schematic of an ALD cycle (reproduced from [87])

ALD allows depositions with lower temperatures compared to other CVD techniques. It also permits excellent 3D conformality, precise film thickness control, and stoichiometry. Consequently, it represents a good candidate tool for scaling down microelectronics. However, the excellent control in growth makes the deposition rate slow (0.1 nm/cycle), and it can potentially generate toxic by-products [88].

In this study, the ALD Si:HfO_2 is fabricated in the EPFL CMi cleanroom facility using the tool Beneq TFS200, which is dedicated to CMOS compatible processes and the deposition of thin dielectrics. Following the previous works [89, 46], the precursors used for the deposition are tetrakis(ethylmethylamino)hafnium (TEMAHf) for Hf and $SiH_2(N(C_2H_5)_2)_2$ (also called SAM24) for Si.

2.1.2 Process flow

The fabrication process of the Si:HfO_2 capacitor started with the deposition of the bottom electrode through sputtering a 15 nm of TiN on a silicon wafer. Subsequently, ferroelectric Si:HfO_2 was deposited by ALD. To reach the desired silicon doping concentration, around 3.4%, the cycle ratio of the Si and Hf precursor was varied. Knowing that the growth rate of ALD films is about 0.1 nm/cycle, the cycles used in our recipe were a total of 165 pulses to reach an estimated thickness of 16 nm.

The ALD deposition temperature was 300 °C. As a result, HfO_2 was amorphous and needed a subsequent annealing step to crystallize and reach the non-centrosymmetric orthorhombic phase. To do so, the Si:HfO_2 film was capped with 10 nm of TiN via sputtering, and rapid thermal annealing (RTA) was performed at 800 °C for 20 s at nitrogen ambient. At this fabrication step, it can be useful to perform an GI-XRD to get some information on the crystallization phase of Si:HfO_2. The results and the method are illustrated in Section 2.2.1.

After the RTA, a Pt layer 25 nm thick was deposited to serve as top metal contact. Finally, ion beam etching (IBE) was used to pattern the top electrode with different dimensions: 100×100μm^2 devices were used for the electrical characterization, while 5×5 μm^2 devices were used for piezoelectric force microscopy (PFM). As depicted in Figure 2.2, the capacitor consists of a TiN/Pt top electrode and a shared TiN bottom electrode.

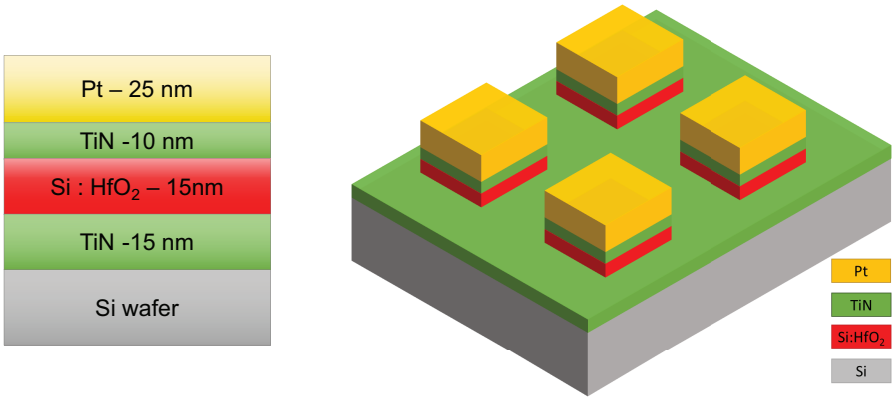


Figure 2.2: Schematic of the chip's capacitor cross-section and 3D view.

2.2 Microstructural analysis

Microstructural analyses were performed before the electrical characterization to get the thicknesses and crystallization phase. We carried out the crystallographic analysis using Grazing Incidence X-Ray Diffraction (GI-XRD) and the high-resolution images with scanning electron microscopy (SEM) and transmission electron microscopy (TEM). Here the technique are first illustrated (Section 2.2.1) and then the relative results on the Si:HfO_2 capacitor are shown (Section 2.2.2).

2.2.1 Method for microstructural analysis

Grazing Incidence X-Ray Diffraction

X-ray Diffraction (XRD) is a technique used to analyze the crystal structure of a material. Due to the atomic structure within the crystal the incident X-ray beam is scattered, yielding a characteristic diffraction pattern. The diffracted radiation intensity is collected through a

movable detector and typically plotted as a function of the angle between the incident beam and the scattered one (2θ).

Grazing Incidence X-Ray Diffraction (GI-XIRD) is a type of XRD used to analyze thin layers. In this case, the incident beam has a small and fixed incident angle (ω), and the detection angle (θ) is always greater than ω. In this condition, it is possible to ensure that the diffraction comes from the topmost layer.

All the GI-XRD patterns reported in this work have been taken in EPFL with a configuration called ω-2θ scan, with an Empyrean diffractometer by Panalytical, equipped with a pixel-1D detector and using a Cu (λ = 1.54 Å) X-ray beam [48, 90]. The incident angle ω was at 1°, while the 2θ angle was scanned between 27° and 33°, a range in which it is possible to detect the orthorhombic peak, the monoclinic peaks, and the tetragonal peaks for HfO_2-doped ferroelectrics.

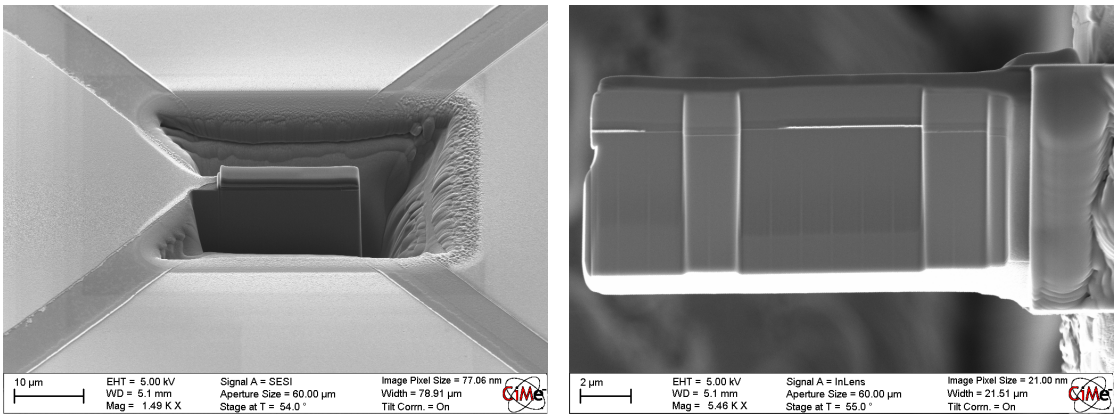
Electron microscopy

One of the electron microscopy techniques used was scanning electron microscopy (SEM), which consists of an electron beam focused into a small probe scanning the sample surface in a raster scan pattern. Detectors collect primary electrons, elastically backscattered from the beam, and secondary electrons, emitted by atoms excited by the electron beam. Images of the sample surface are generated by detecting these signals and associating signal intensity with probe position. The type of signal provides different information on the sample analyzed. In this work, we used SEM to visualize the surface of a sample when the feature was too small for an optical microscope.

The most frequently used electron microscopy technique in this work is transmission electron microscopy (TEM), which consists of an electron parallel beam passing through a very thin portion of the sample called lamella. In Figure 2.3, a TEM lamella preparation is shown by SEM images. Once the region of interest is first covered by carbon as a protecting material, and the holes are milled by a focus ion beam (FIB), the lamella can be lifted out and attached to support where the final thinning is performed.

When the TEM reaches atomic resolution, it is called high-resolution TEM (HR-TEM). It is very powerful since it can be used to study the atomic structure and analyze the interfaces. TEM can also be used in scanning mode (STEM). In this case, the beam is not parallel like in standard TEM, but it converges and scans the sample in a raster mode like in SEM. Two possible detectors can be used: the dark field (DF) and the bright field detector (BF), which are used respectively for DF-TEM and BF-TEM.

Another analysis used in this work is Energy Dispersive X-Ray Spectroscopy (EDX), a powerful composition analysis technique that can be used in combination with TEM or SEM. The accelerated electron beam induces the emission of electrons from the material inner atomic orbitals. The resulting vacancies are filled by electrons from the higher energy shell, emitting



(a) (b)

Figure 2.3: SEM image of the lamella preparation of the JLFET sample (discussed in Chapter 4).

energy that provides a univocal footprint characteristic of an element.

In this study, we used for TEM analysis a FEI Tecnai Osiris in the EPFL Interdisciplinary Center for Electron Microscopy (CIME), with an acceleration voltage of 200 kV and a current of 1 nA.

2.2.2 Results on the Si:HfO_2 capacitor

To obtain information about the crystallization phase of the Si:HfO_2, the sample was analyzed by GI-XRD. It is worth noting that the sample was analyzed with GI-XRD before the deposition and patterning of the Pt top electrode since the area necessary for the analysis is larger (around 10 mm^2) than the capacitor structure themselves (100×100 μm^2 for the largest) and it could not be recognized.

The analysis is carried out by scanning 2θ between 27° and 33°. Range in which the main monoclinic, tetragonal, and orthorhombic phase peaks are located. The GI-XRD results in Figure 2.4 show just a predominant peak around 30.4°. It is attributable to the overlapping of the orthorhombic and tetragonal phase [91, 90]. The absence of secondary peaks at 28.3° and 31.7°, excludes the possibility of a predominant monoclinic phase in Si:HfO_2.

Figure 2.5 shows a BF-STEM image of the cross-section capacitor, which enabled us to measure the thickness of the layers and verify their uniformity. The thickness for Si:HfO_2 resulted in 14.5 nm, 2 nm less than the value predicted by the ALD growth rate.

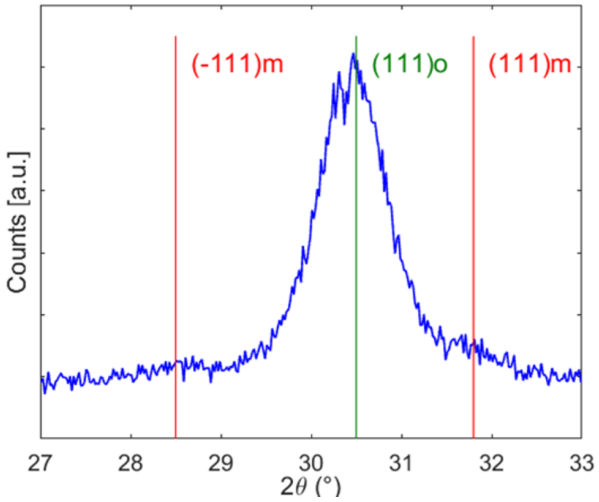


Figure 2.4: GI-XRD pattern of ferroelectric capacitor showing the ferroelectric orthorhombic peaks at 30.4°.

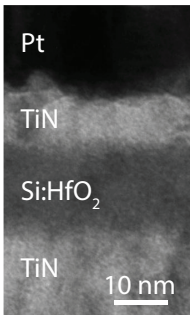


Figure 2.5: Cross-section STEM of the capacitor structure.

2.3 Electrical characterization

This Section describes electrical measurements applied to ferroelectric capacitors. Thanks to these methods, one can induce the spontaneous polarization switch by an external electric field. The first part of the Section will introduce the method, and the second will provide the result taken on the Si:HfO_2 capacitor.

2.3.1 Electrical characterization methods

Electrical measurements are the most used characterization techniques in this work since they are used with numerous devices and for different scopes, from ferroelectric capacitor testing to transistor characterization. The tool used is Keithley 4200A-SCS Parameter Analyzer with 4225-PMU Ultra-Fast I-V Module. Unless it is not stated otherwise, the hardware was connected

to the Cascade Microtech probe station with triaxial cables. To contact the device under test, probes with a radius of 5 μm are maneuvered via micro-manipulators. Thanks to 4225-RPM Remote Amplifier/Switch with integrated swinging mechanism, it was possible to make a capacitance-voltage (CV), current-voltage (IV), pulsed IV, and transient pulse responses without changing the configuration of the cables.

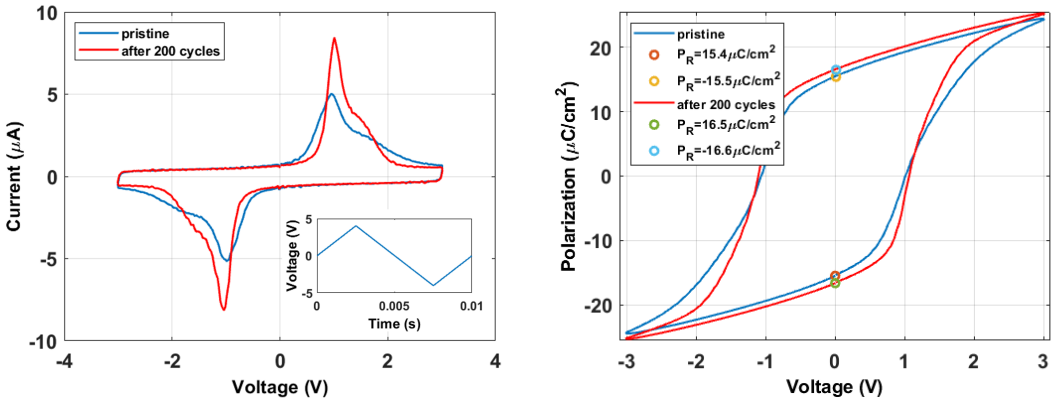
Polarization voltage (P-V) dependence is the most common measurement to characterize ferroelectric. It is typically performed using a Sawyer-Tower circuit, which consists in applying a triangular waveform on the capacitor and measuring using an oscilloscope the polarization charge on a load capacitor as it is charging. Nevertheless, in this approach, there are some downsides. The load capacitor, which is in series with the ferroelectric, should be larger than the latter to ensure that most of the voltage drop falls on the ferroelectric. This implies that the voltage read by the oscilloscope will be reasonably small, affecting the measurement accuracy.

In this work, to extract P-V loop, we used just Keithley 4200A-SCS with 4225-PMU and 4225-RPM, which applies the voltage and contemporary samples the current in time.

2.3.2 Electrical characterization result

Pulsed characterization

From the P-V hysteresis loop, it is possible to extract ferroelectric properties, like coercive voltage V_C and remanent polarization P_R. In Figure 2.6 the characteristics in blue show the behavior at the first cycle, also called pristine state, and the one in red are after the wake-up procedure, such as after 200 cycles.



(a) (b)

Figure 2.6: IV curve (a) and PV loop (b) of MFM cap before and after wake-up procedure measured at a frequency of 500 Hz (see inset).

P-V testing consists in applying a triangular pulse across the capacitor by using two probes, one on the top electrode (TE) and the other on the shared bottom electrode (BE). Simultaneously

the current (I) is sampled in time (t). Figure 2.6(a) shows the behavior of the current with respect to the applied voltage value, where one can notice the presence of two clear peaks in correspondence of the switching of the Si:HfO_2 around 1V. Then, the polarization is calculated as charge (Q) per unit area (A):

$$P = \frac{Q}{A} = \frac{\int I\,dt}{A} \tag{2.1}$$

The resulting behavior is depicted in Figure 2.6(b), from which it is possible to extract the coercive voltage V_C and the remanent polarization P_R. V_C is the voltage at which the polarization switches orientation and is the intercept of the curve with the x-axis. P_R is the polarization value when zero bias is applied, and it corresponds to the intercept of the curve with the y-axis.

After the ferroelectric wake-up, the remanent polarization slightly increases from 15.5 $\mu m/cm^2$ to 16.5 $\mu m/cm^2$, while the coercive voltage reduces from 1.1V to almost 1V. One can also observe that after wake-up, the switching gets more abrupt, corresponding to sharper and higher current peaks.

Comparing the polarization curve before and after cycling (Figure 2.6(b)), we can notice a slight improvement in the characteristic. It can also occur to see a ferroelectric in which the hysteresis is pinched in the pristine state. An example is shown in Figure 2.7. However, by cycling, it is possible to observe an "opening" of the loop.

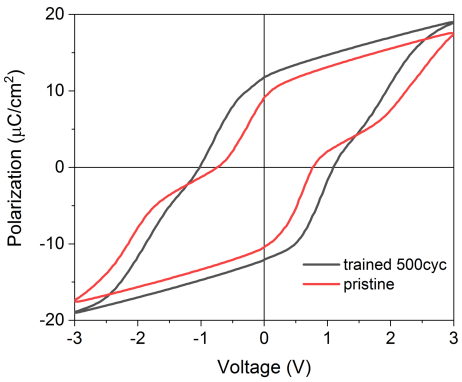


Figure 2.7: PV hysteresis before and after wake-up (500 cycles).

Once the characteristic has been shown at pristine, and after wake-up, it is worth checking the endurance of the capacitor, i.e., how long it can operate. This was performed for 10^8 cycles with a rectangular waveform at 1KHz. As shown in Figure 2.8, the capacitor does not show any degradation of the remanent polarization. The polarization opening during the wake-up procedure (200 cycles) is not shown here.

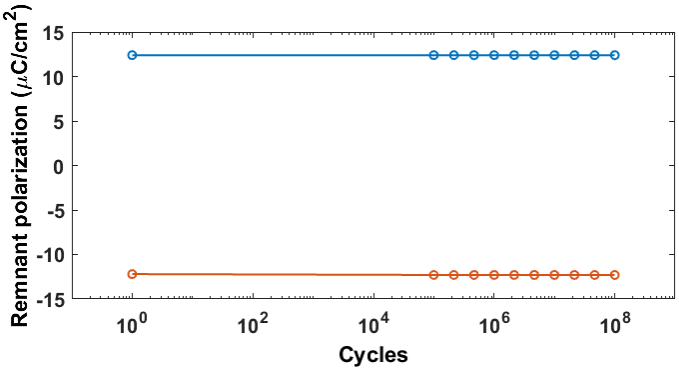


Figure 2.8: Endurance test performed wake-up procedure (200 cycles)

Quasi-static current characteristic

Another useful measurement for the ferroelectric capacitors is the evaluation of the quasi-static leakage current. These results were obtained by applying a ramping voltage from -3 V to 3 V and back in quasi-static mode while monitoring the current. In Figure 2.9, it is possible to observe that the leakage current is below 600 pA at 3 V. Considering that the measurement has been taken on a 50 μm x 50 μm capacitor, the leakage current density at 3 V is equal to 24 $\mu A/cm^2$.In the insert of Figure 2.9, one can observe the switching current peak is below 1 V.

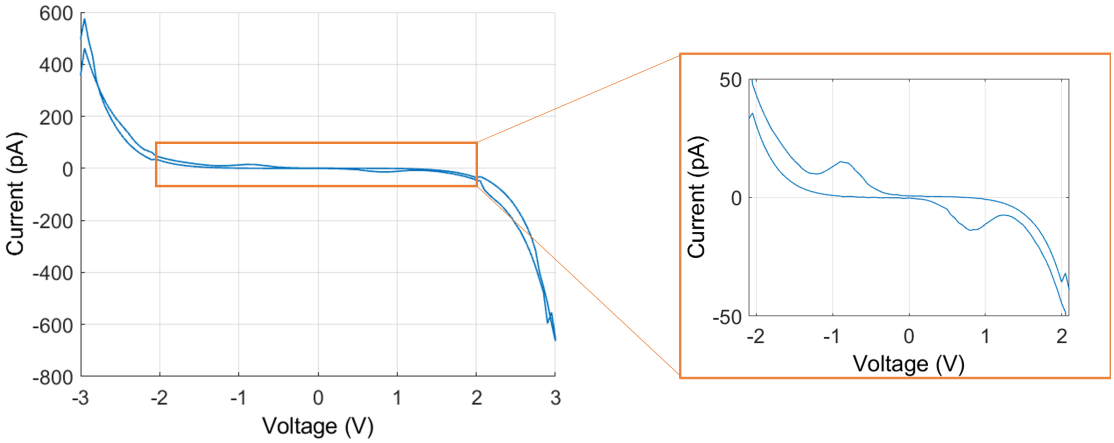


Figure 2.9: IV plot with an insert highlighting the switching current peaks.

Capacitance characteristic

The capacitance measurement is another technique used to prove genuine ferroelectricity. The ferroelectric capacitance-voltage (C-V) curve is also called the butterfly characteristic because of two peaks in correspondence of the polarization switching.

Figure 2.10 shows a CV measurement of an MFM capacitor after wake-up, extracted at 50 kHz

with an AC signal of 100 mV. The symmetry observed indicates that the ferroelectric properties like remanent polarization and coercive voltage are symmetric. On the contrary, in the case of imprint, the P-V plot would be shifted in the x-axes. This would give rise to a difference in the positive and negative coercive voltage and, in turn, to a difference in the positive and negative remanent polarization. Consequently, the asymmetry would be reflected in the C-V as well.

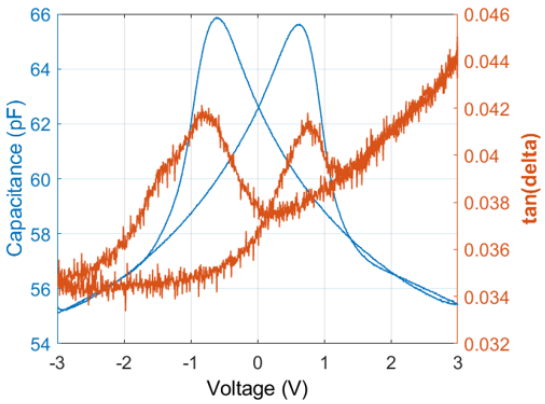


Figure 2.10: (a) Capacitance–voltage trend. (b) Corresponding loss tangent measurement.

By approximating the MFM structure to an ideal parallel plate capacitor, it is possible to extract the relative dielectric constant of the material (ε_R):

$$\varepsilon_R = \frac{C\,d}{\varepsilon_0 A} \tag{2.2}$$

where ε_0 is the vacuum permittivity ($8.85 \times 10^{-12} Fm^{-1}$), d is the thickness of the Si:HfO_2 ($15nm$) and A is the area ($2500\mu m^2$). The resulting Si:HfO_2 ε_R is between 37 and 45 depending on the switching condition, which is in line with literature estimation [46].

Always in Figure 2.10 is indicated the dissipation factor, also called $tan\delta$, which is the ratio of the loss current I_R to the charging current I_C:

$$tan\delta = \frac{I_R}{I_C} \tag{2.3}$$

The dissipation factor represents the tangent of the phase difference between the input AC voltage waveform and the measured one. As the name suggests, it is used to determine the practical power dissipation in a dielectric material. In Figure 2.10, one can observe that its value is consistently below 0.05, such as $I_R < 5\% I_C$, suggesting that the dielectric leakage current can be considered low.

2.4 Electromechanical characterization

So far, we have measured the ferroelectric properties macroscopically. In this Section, we use piezoelectric force microscopy (PFM) as an electromechanical characterization technique to get insights into microscopic switching. At the beginning of the Section, the PFM working principle is introduced, followed by PFM results on the ferroelectric capacitor.

2.4.1 Introduction on piezoelectric force microscopy

Scanning probe microscopy (SPM) is a family of metrology techniques that create surface images using a physical probe scanning on the sample. The probe is moved in a raster scan mode, line by line, through a piezoelectric actuator. The probe-surface interaction is recorded as a function of position in a two-dimensional data point array, displayed with a colored data scale in a standard digital image. SPM techniques are classified according to the interaction principle of the probe with the surface. The one used in this work is the Atomic Force Microscopy (AFM) which probes the surface of a sample with a very sharp tip, placed at the free side of a cantilever, as shown in Figure 2.11. The cantilever bends due to the atomic forces between tip and material. This deflection is measured optically by means of a laser beam pointed on the cantilever, and a four-quadrant photodiode measures its reflection. The cantilever deflection is used as the input of a feedback system, which is designed to maintain the deflection constant. This is achieved by a piezoelectric actuator, which can change the sample's vertical position based on the feedback loop's output.

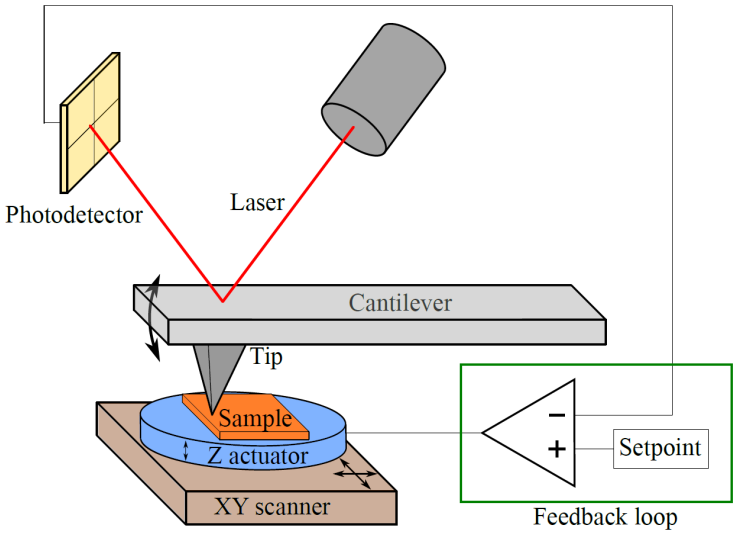


Figure 2.11: Schematic showing the basic principles of AFM measurement system (reproduced from [90])

AFM is classified according to two scanning modes, based on the atomic force interaction, which depends on the tip-surface gap. When the tip-surface distance is about a few

angstroms, the force is repulsive, and the mode is called contact, the resolution is higher, and tip-contamination due to pollutant effect is less, but a tip or sample damage may occur. When the tip is farther from the surface, in the so-called non-contact mode, the interaction is repulsive, the resolution is lower, and less damages occur. Furthermore, by using a biased conductive tip, AFM allows the probing of electrical properties, enabling the invention of several characterization measuring modes.

The technique used in this work is the Piezoelectric Force Microscopy (PFM), a variant of AFM performed in contact mode with a biased conductive tip that, thanks to an extra lock-in amplifier, allows the readout of amplitude (d_{33}) and phase of the material piezoresponse. The physical principle is based on the converse piezoelectric effect that results in electrically induced displacement, which is measured by the cantilever deflection. The d_{33} effectively measured by PFM (d_{33eff}) is smaller than the actual d_{33}. It may occur either when the material is polycrystalline with a randomly oriented domain or by the encapsulation caused by electrodes [88, 92].

To amplify the d_{33} value and simplify the measurement, a common technique called resonance PFM is generally used. As the name suggests, it consists in applying the AC signal with a frequency equal to the system's resonance frequency. However, the resonant frequency may shift due to changes in tip-surface interaction caused by different factors like surface feature, tip wear, and electrostatic charges.

In this work, to reduce the possible source of artifacts and simplify the data interpretation, we work using off-resonance PFM, such as PFM working at a frequency far from the resonance. The drawback of this technique is that since the response to the probe is lower, the measurement takes longer (45 min for a map) due to the higher integration time required. However, it shows several improvements compare to resonance PFM like the opportunity to get frequency-independent data. It enables the possibility to quantify the d_{33} of the material, and the capability of probing extremely weak piezoelectric responses with sub-picometer sensitivity [93, 90].

All the PFM measurements performed in this work are taken on Asylum Research Cypher AFM with an extra Zurich Instruments HF2LI lock-in amplifier used to read out the PFM signals and controlled by a LabView script [90]. The measurements are always performed with the HfO_2-doped capped with a top electrode to avoid any possible electrostatic artifact. Since the electric field is applied uniformly under the electrodes, the response is higher. This is convenient for HfO_2-doped, which are known to have smaller d33 compared to perovskites [94, 95]. Moreover, this technique can study the property of the ferroelectric integrated into the device and not just the material itself. The drawback is that the resolution is lower, and the response gets weaker with a thick electrode. As a result, the capping metals (TiN and Pt by-layer) on top of HfO_2-doped are consistently thinner than 40 nm.

PFM loops are also measured using spectroscopy mode, a configuration in which the tip is kept steady in a location and a voltage ramp composed of discrete steps is applied (see

Figure 2.12). Simultaneously, a superimposed AC signal is applied to the sample to extract the piezoresponse amplitude and phase. In the plots, DC ON represents the case with non-zero DC voltage applied, while DC OFF is the case when it is removed. The double measurement with and without a constant field is useful to check if the electromechanical response is coming from the ferroelectric material response and not other electrostatic forces affecting the measurement. Furthermore, a similarity between DC OFF and DC On gives information about polarization retention.

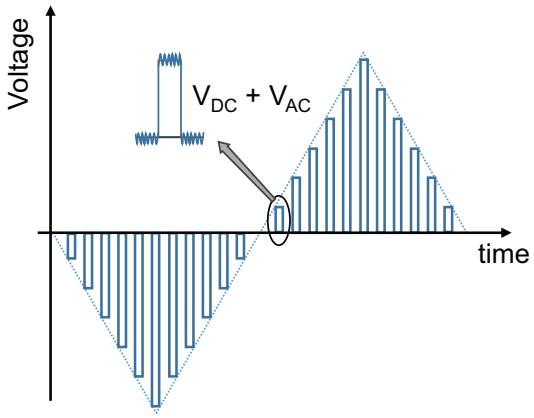


Figure 2.12: Schematic of the voltage applied in time during a PFM loop in point spectroscopy

2.4.2 Electromechanical characterization results

Through PFM, we studied the Si:HfO_2 switching dynamics at the nanoscale by scanning the surface of the capacitor with a sharp tip coated with Pt conductive tips. The bias was applied at the tip, and the bottom electrode was grounded. The device tested was the smallest fabricated (100 μm^2) to prevent frequency limitation from the equivalent RC circuit. The AC voltage amplitude used was 500 mV. This value allows a good signal but does not interfere with the polarization switching since it is lower than the coercive voltage.

PFM maps displaying the phase, the amplitude, and the topography were taken on the same area with dimensions of 0.5 um^2 in different switching stages. At first, as shown in Figure 2.13 (a), the mixed state was induced with the tip voltage of -1 V (close to the negative coercive voltage at room temperature). Subsequently, the capacitor was pre-poled at +4 V, which led to a uniform phase representing the positive out-of-plane component of the polarization (as shown in Figure 2.13 (b)). Finally, the negative state was induced with -4 V in order to saturate the polarization in the negative direction (Figure 2.13 (c)). All the maps were taken with an AC voltage of 0.5 V, which was low enough to prevent the Si:HfO_2 switching and high enough to get a clean signal.

The positive and negative states (Figure 2.13 (b) and (c)) correspond to the saturated polarization response measured in P-V loops, indicating that a homogeneous polarization is obtained

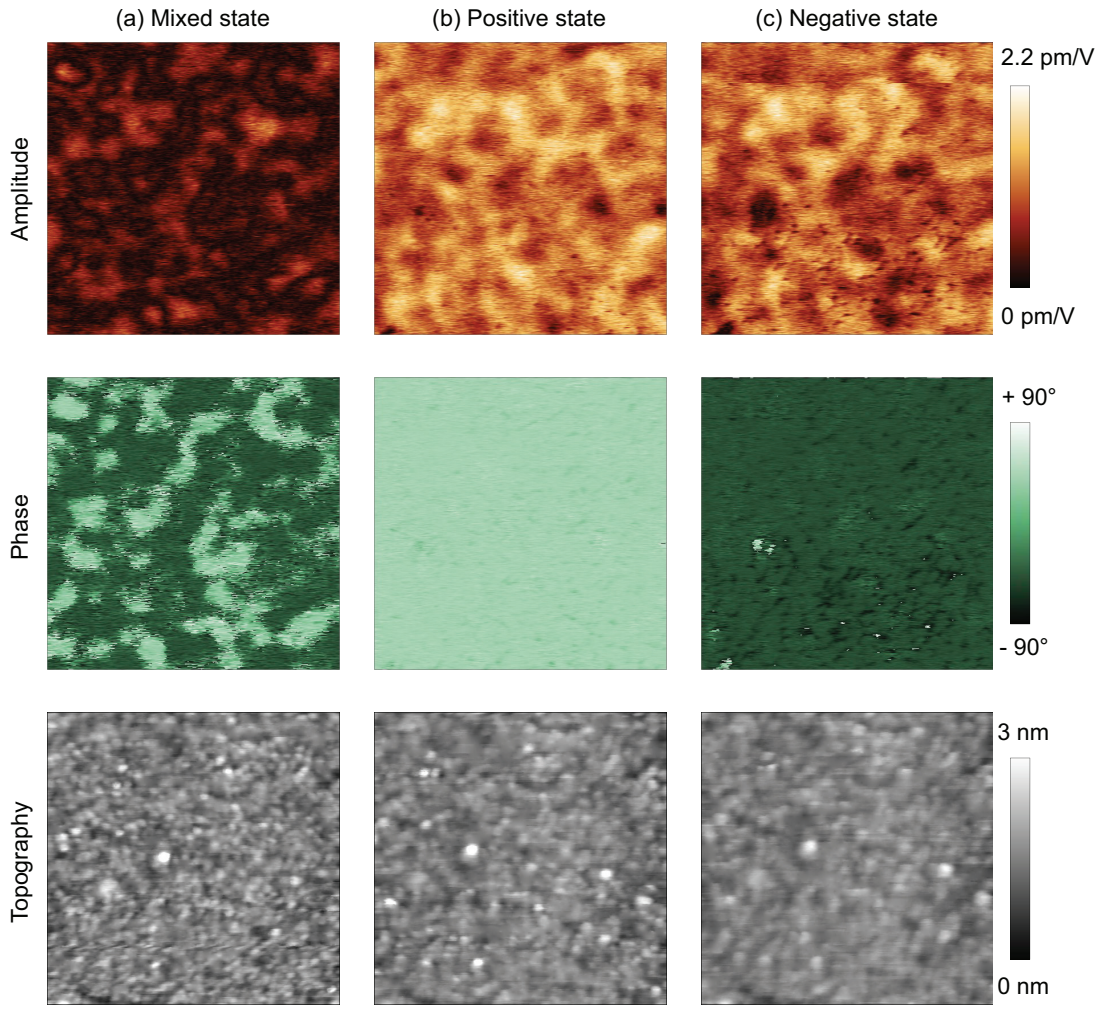


Figure 2.13: PFM maps of phase and amplitude of the same device area (1 um^2) in different polarization conditions: (a) mixed-state phase and amplitude (after the application of -1 V), (b) positive state phase and amplitude (after the application of +4 V), and (c) negative state phase and amplitude (after the application of -4 V).

in both directions. Looking at Figure 2.13 (a), one can see independent switching regions, with dimensions ranging from 50 to 200 nm, switched from a positive to a negative state, while others remained fixed; similar observations were reported in other works and have been associated to extrinsic switching [96, 93].

It's worth mentioning that thanks to off-resonance PFM, the measurement is subjected to less artifact than resonance PFM. The resolution is reduced due top electrode's presence, making it difficult to observe single ferroelectric domains, which are about 10 nm.

The surface features in the topography maps confirm that the thermal drift during scanning is minimal, even though the three maps scanning took almost eight hours, a time long enough to change the temperature of the sample during the measurement. Furthermore, it can be observed that there is no correlation between the feature in topography and the once in amplitude and phase maps. In addition, from the topography analysis, it is evident that the maps got less defined and more blurred. The tip wears most probably caused it since the tips used are very sharp, with a hard cantilever, and after hours of scanning, the conductive coating tends to get damaged.

PFM loops are measured in a ferroelectric active area using spectroscopy mode, and the voltage is swept between -3 V to 3 V with an AC voltage of 500 mV. Before the measurement, a wake-up of 100 cycles at 3 V is performed. The PFM loops were measured on the same spot at frequencies of 12, 92, and 230 kHz. We chose these values to be far from the resonant frequency and the system's noise. As shown by Figure 2.14, the amplitudes values are practically independent of frequency, as by a genuine ferroelectric sample measured by off-resonance PFM.

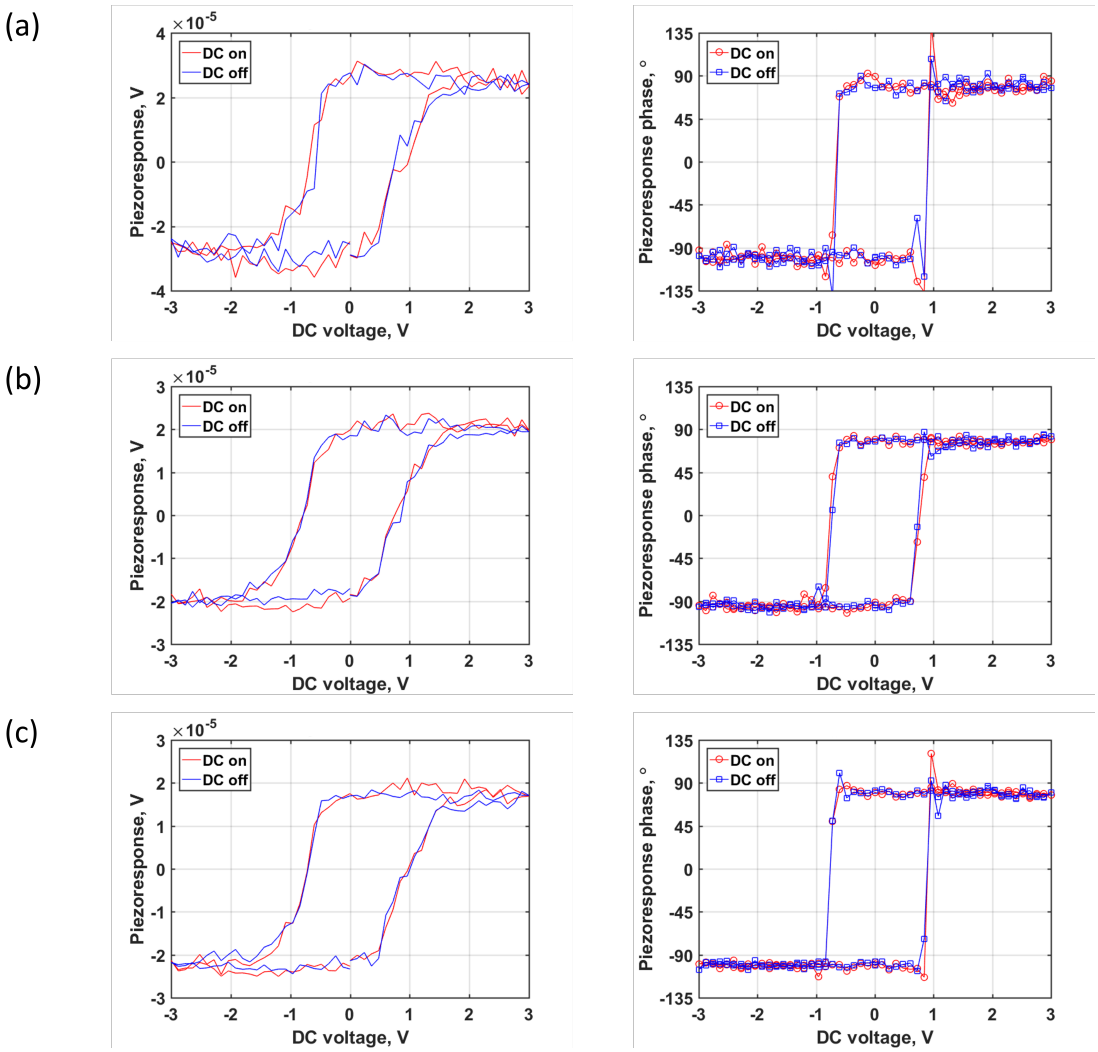


Figure 2.14: Off-resonance PFM amplitude (left column) and phase (right column) loops on 15nm Si:HfO_2 capacitors measured at 12 (a), 92 (b) and 230 (c) kHz with AC voltage of 500 mV.

2.5 Fabrication optimization

In this section, we describe some fabrication improvements of Si:HfO_2 ferroelectric, that is the building block of the gate stack devices of Chapter 3 and for Fe-FET of Chapter 4. The optimization targets two fundamental requirements for memory and NC applications: leakage current and polarization. Remanent polarization is generally the main figure of merit of ferroelectrics. Leakage current can reduce memory endurance and is detrimental to NC stabilization. To minimize the leakage current and keep a sufficient high remanent polarization, we investigated the effect of thermal budget and thickness variation on the ferroelectric property in Section 2.5.1 and 2.5.2, respectively.

2.5.1 Thermal budget

In this Section, we study the influence of the annealing conditions and wake-up cycling on a 16 nm thick Si:HfO_2 thin film. The fabrication technique follows the one presented in Section 2.1.2. The only difference is that the wafer was diced after Si:HfO_2 capping. Hence, all the subsequent steps were performed at the chip level. This choice permits the study of thermal budget and field cycling effects without being affected by ALD deposition variability. Furthermore, chip-level manufacturing becomes interesting for research purposes when testing different fabrication approaches without sacrificing costly wafers, such as SOI in Chapter 4.

It is worth mentioning that the thermal budget must be adapted when moving from wafer level to chip level process. In JetFirst 200 system, the temperature is measured by a thermocouple on the wafer backside, whereas the lamp heats the wafer from the top. In the case of chip processing, a wafer holder contains the sample, and because of JetFirst 200 system, it is subjected to a higher temperature than the one set due to differences in heat mass. The effect is visible by comparing P-V loop of samples annealed at the wafer level (Figure 2.6(b)) and at the chip level (Figure 2.15): if the RTP is performed at the chip level, the tip of the P-V curve is more open, which is a sign of higher leakage current.

Figures 2.16 (a) and (b) show the scattered plot of the remanent polarization and leakage current density versus a variable annealing time (20s, 60s, and 120s) and at two different temperatures (700 °C, and 600 °C). The extracted value is taken by averaging from five capacitors. The data at 800 °C is not considered here since its leakage current is more than one order of magnitude larger than 700 °C. It is worth noting that the values extracted are measured after a ferroelectric wake-up of 1000 cycles. Cycling caused an increase of 20% of the remanent polarization and a leakage current reduction of approximately of 30%. Anyhow, most variation (around 15% on the P_R) occurs by training MFM capacitors with 100 cycles.

Figure 2.16 shows that the polarization increases with both time and temperature. However, the leakage current seems to grow faster than the remanent polarization with respect to time at 700 °C. From a first look, it appears that the effect of the annealing time depends on the

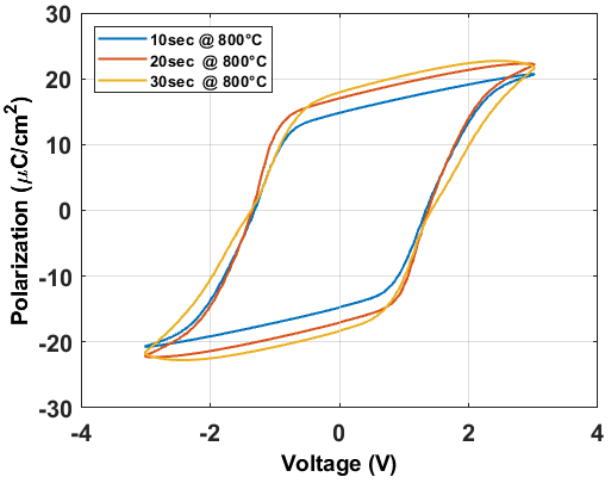
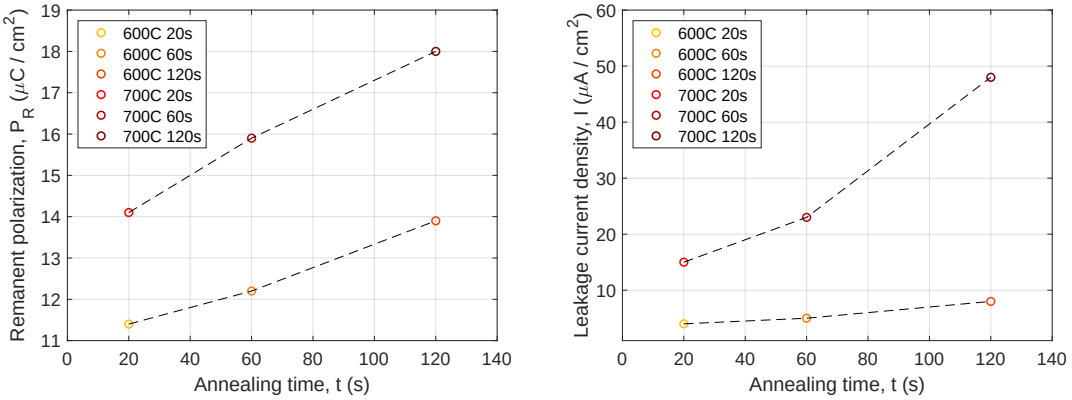


Figure 2.15: PV loop taken at 1kHz of MFM capacitor under three different annealing annealing time.

temperature at which the sample is annealed. On the contrary, there seems to be no correlation with the wake-up procedure.



(a) (b)

Figure 2.16: Plot of remanent polarization and leakage current density versus annealing time at two temperatures 700 °C and 600 °C.

The results are evaluated to assess the influence of the factors, such as annealing time (t), annealing temperature (T), and wake-up cycles (w), on the remanent polarization (P_R) of 16 nm thick Si:HfO_2. The Analysis of Variance (ANOVA) was performed on these data using the linear model with interaction between the factors. The study has been implemented in MATLAB, using the N-way ANOVA function, and the obtained results are shown in Figure 2.1 and Table 2.1, in which the statistical quantities are defined as:

- **Source** is the source of the variability

- **ss** is the sum of squares due to the source
- **df** is the degrees of freedom of the source
- **ms** is the mean squares (SS/df)
- **F** is the ratio of the mean squares
- **p** is the probability that F-value takes a value larger than the computed test-statistic value

Source	**ss**	**df**	**ms**	**F**	**p**
wake-up cycles(w)	17.599	2	8.799	189.51	0.0001
time (t)	3.897	2	1.948	41.96	0.0021
temperature (T)	21.451	1	21.451	461.98	0.0000
w*t	0.110	4	0.028	0.59	0.6874
w*T	0.002	2	0.001	0.02	0.9785
t*T	16.181	2	8.091	174.24	0.0001
ϵ	0.186	4	0.046		
Total	59.426	17			

Table 2.1: ANOVA results of the linear model with interaction obtained with MATLAB

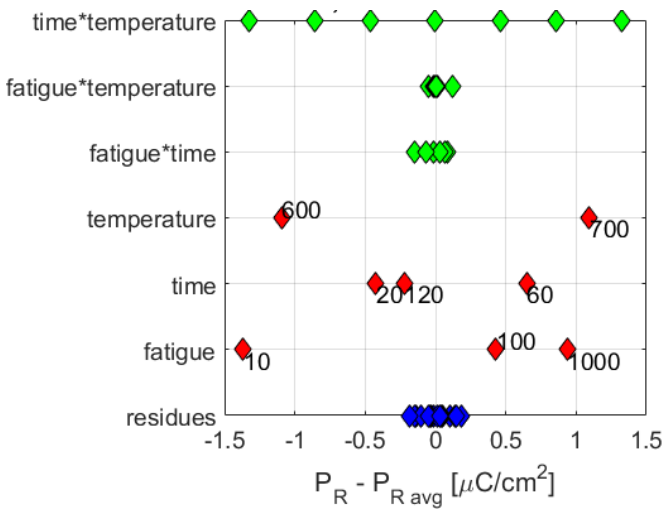


Figure 2.17: Dot plot of the effects of the factor (w, t, T), the interaction (t*T w*T w*t) and residues (ϵ)

Looking at the mean sum of squares and the value p, the parameters primarily affecting the polarization are temperature and wake-up cycles. From the dot plot (Figure 2.17), it is clear that the residuals are almost negligible compared to the other sources. This means that the linear model with the first degree of interaction represents a good approximation. Interestingly, the interaction term between time and temperature has a strong impact, and its p-value is

very low (0.0001). On the contrary, other interactions are negligible, as evident from their low statistical quantity.

In conclusion, compared to what was observed [72, 97], the analysis confirms a dependence between annealing time and temperature. Nevertheless, we did not notice a correlation with the wake-up procedure, even if in literature it is said that a higher thermal budget can significantly reduce the wake-up effect [98, 72].

2.5.2 Thickness

Following the previous optimization of the thermal budget, the thickness optimization is the next step to improve further the ferroelectric robustness. Since it is known that Si:HfO_2 shows an optimal thickness fabrication window (around 10-12 nm [88, 64]), depositions of sub-16nm thick Si:HfO_2 was performed.

The fabrication process is similar to the one shown in Section 2.1.2, but it was performed at the chip level. The Si:HfO_2 thicknesses considered in this study are 9 nm and 12 nm, obtained by performing 99 and 132 pulses ALD cycles, respectively. Tuning of the thermal budget is needed for each thickness since thinner ferroelectrics are known to require a lower thermal budget [64, 80]. Therefore, seven samples were fabricated for each of the two thicknesses with the following annealing condition:

- 800 °C for 20 s,
- 700 °C for 20 s, 60 s and 120 s,
- 600 °C for 20 s, 60 s and 120 s.

The chips were subsequently tested electrically to extract the polarization, the leakage current, and the dielectric constant. The devices with 12 nm and 9 nm did not survive the highest annealing conditions of 800 °C for 20 s and 700 °C for 120 s. They became very leaky, making it impossible to measure any P-V and C-V curves on them.

In Figure 2.18 (a), the PV loops at 1.0 kHz, measured on the 12 nm Si:HfO_2 capacitors and trained with 1000 cycles, are illustrated for different thermal budgets. This study confirms what was shown in Figure 2.16: the remanent polarization increases with annealing temperature and time. However, looking at Table 2.2 one can observe that the leakage current density (J) is increasing with the thermal budges, and it gets particularly high at 700 °C.

Figure 2.18 (b) shows the capacitance butterfly curves measured at 100 kHz, together with the dielectric constant values. One can notice that the dielectric constant is inversely proportional to the thermal budget. It has been demonstrated computationally and experimentally that, in HfO_2, the tetragonal phase has a higher dielectric constant than the orthorhombic and monoclinic one [99, 100]. Si in HfO_2 is a strong stabilizer for the tetragonal phase, more than

other HfO_2 [101, 102]. Consequently, the decrease of the dielectric constant with the thermal budget can be caused by a reduction in the non-ferroelectric tetragonal phase percentage. On the contrary, a higher thermal budget can cause the tetragonal phase transforms into the ferroelectric orthorhombic phase [80].

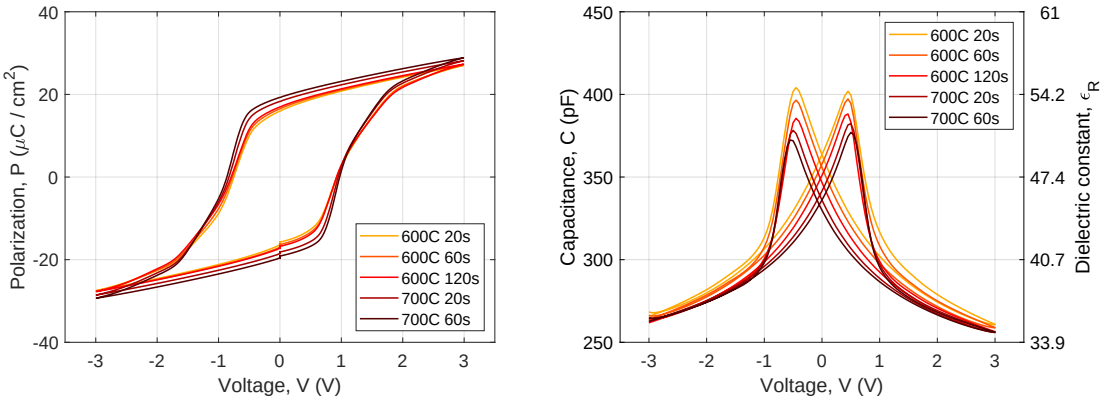


Figure 2.18: Effect of different thermal budget on ferroelectric properties of 12 nm Si:HfO_2: P-V (a), C-V and ϵ_R-V (b) curves.

Annealing conditions	20s	60s	120s
800 °C	leaky	-	-
700 °C	$P_R = 18.3\ \mu C/cm^2$ $J = 330\ \mu A/cm^2$	$P_R = 19.2\ \mu C/cm^2$ $J = 2105\ \mu A/cm^2$	leaky
600 °C	$P_R = 15.9\ \mu C/cm^2$ $J = 29\ \mu A/cm^2$	$P_R = 16.5\ \mu C/cm^2$ $J = 30\ \mu A/cm^2$	$P_R = 17.1\ \mu C/cm^2$ $J = 45\ \mu A/cm^2$

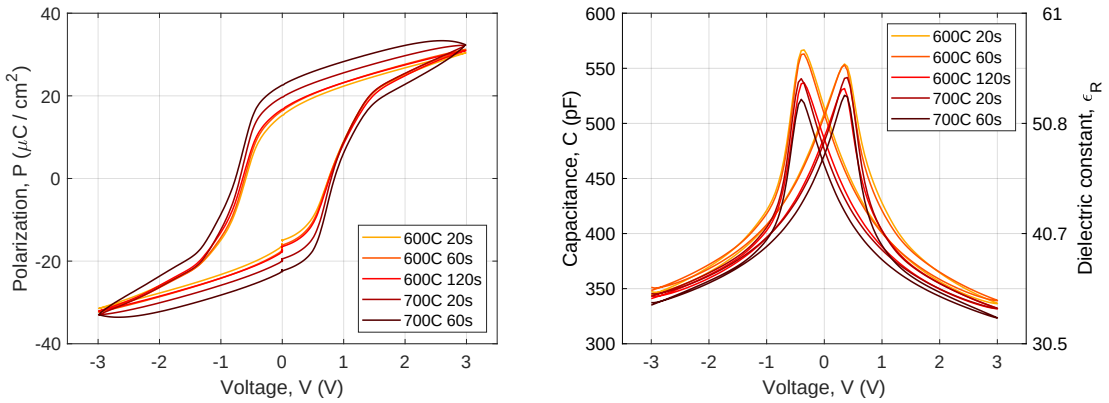
Table 2.2: Effect of different annealing conditions on remanent polarization and leakage current density (at 3V) taken on 12 nm Si:HfO_2 capacitor.

A similar polarization and dielectric constant trend is observed for 9 nm Si:HfO_2 (Figure 2.19). However, in this case, the leakage current value is much higher than the 12 nm layer (around 10x for the same thermal budget), as shown in Table 2.3. It increases particularly high for 700 °C annealings, and the hysteresis becomes distorted. Indeed, leakage is one of the limiting factors in doped-HfO_2 scaling down. Comparing the P_R and the ϵ_R of the two thicknesses for the same thermal budgets, one can observe a moderately lower P_R and higher ϵ_R in the 9 nm MFM.

It is known that TiN electrodes tend naturally to oxidize, capturing oxygen from HfO_2 and causing vacancies. When the thickness of the ferroelectric is thinner, oxygen vacancy concentration can increase. This variation causes an increase in leakage current, and dielectric constant, which is linked to tetragonal phase percentage [69, 80]. That would explain the

dependence of current and dielectric constant behavior with thickness.

Furthermore, it can be observed that the coercive voltage seems to decrease with the thermal budget (Figure 2.18 and 2.19). This behavior can be as well justified with the same logic as before: the TiN oxidation and oxygen vacancy generation can degrade the ferroelectric properties, increasing the leakage current and creating more trap sited for electric carriers [103, 104].



(a) (b)

Figure 2.19: Effect of different thermal budget on ferroelectric properties of 9 nm Si:HfO_2: P-V (a), C-V and ϵ_R-V (b) curves.

Annealing conditions	20s	60s	120s
800 °C	leaky	-	-
700 °C	$P_R = 16.6\ \mu C/cm^2$ $J = 2\ mA/cm^2$	$P_R = 22.5\ \mu C/cm^2$ $J = 11\ mA/cm^2$	leaky
600 °C	$P_R = 15.2\ \mu C/cm^2$ $J = 0.1\ mA/cm^2$	$P_R = 16.3\ \mu C/cm^2$ $J = 0.3\ mA/cm^2$	$P_R = 16.6\ \mu C/cm^2$ $J = 0.9\ mA/cm^2$

Table 2.3: Effect of different annealing conditions on remanent polarization and leakage current density (at 3V) taken on 9 nm Si:HfO_2 capacitor.

Moreover, in Table 2.4) the coercive field data are collected for different Si:HfO_2 thicknesses at the same annealing condition (600 °C for 120 s). Here one can notice that the electric field needed to switch the polarization increases by decreasing the film thicknesses. This trend is coherent with what was observed above: the higher the oxygen vacancy concentration, the higher the probability of trapping and the higher the coercive field.

To conclude, a GI-XRD was taken on 9nm and 12nm samples annealed at 600 °C. In 2θ region chosen, 27-33°, in which the main monoclinic, tetragonal, and orthorhombic peaks are located. As shown in Figure 2.20 there is no sign of m-phase, whose peaks should be visible at 28.3° and

Film thickness	Coercive field
15 nm	E_F = 0.66 MV/cm^2
12 nm	E_F = 0.71 MV/cm^2
9 nm	E_F = 0.79 MV/cm^2

Table 2.4: Effect of film thickness variation on the coercive field at the same annealing condition (600 °C for 120 s).

31.7°. The only peak appearing in Figure 2.20 results from the overlapping of tetragonal and orthorhombic phases, which is generally the case in small crystallites with broad diffraction peaks. Consequently, it is difficult to estimate the fraction of the two phases, and quantitative estimation in XRD might be misleading.

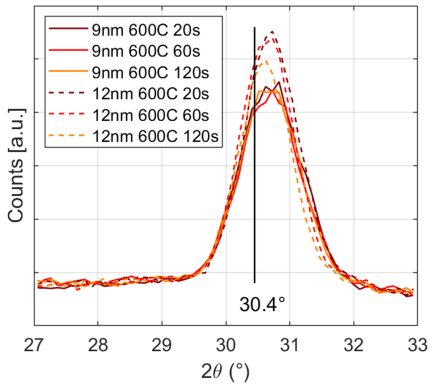


Figure 2.20: GI-XRD taken on 9 nm and 12 nm Si:HfO_2 capacitors annealed at 600 °C for different annealing times.

To summarize, the effect of film thickness and annealing conditions was evaluated and analyzed to find the most robust ferroelectric layer for negative capacitance and neuromorphic application. For the ferroelectric to be used for the transistor (Chapter 4) it was chosen the 12 nm SiO_2 with RTP at 600 °C for 120 s. These conditions provide a sufficient remanent polarization (17.4 $\mu C/cm^2$) while retaining low leakage current density (45 $\mu A/cm^2$).

2.6 Intrinsic switching mechanism in Si:HfO_2 capacitor

In this Section, we study Si:HfO_2 switching mechanism to support the ferroelectric device development for NC logic switches, discussed in the following Chapters. A significant number of publications studied NC-FET devices while implicitly assuming the intrinsic (thermodynamic) polarization response, because the alternative mechanisms based on extrinsic (nucleation-driven) switching do not result in a hysteretic-free NC effect. There is little experimental evidence that intrinsic switching occurs in these materials, and most of the reports on thin-film ferroelectric materials evoke extrinsic switching [34, 96]. In this work, we experimentally calibrate the LGD model through polarization hysteresis measured over a wide range of tem-

peratures to extract the Curie temperature and assess the intrinsic switching mechanism in Si:HfO_2 capacitor.

2.6.1 Temperature-dependent polarization switching in Si:HfO_2

The fabrication process of the ferroelectric capacitor analyzed in this study follows the fabrication steps described in Section 2.1. The 15 nm Si:HfO_2 was annealed at chip level with the optimize condition, 600 °C for 120 s, which is described in Section 2.5.1.

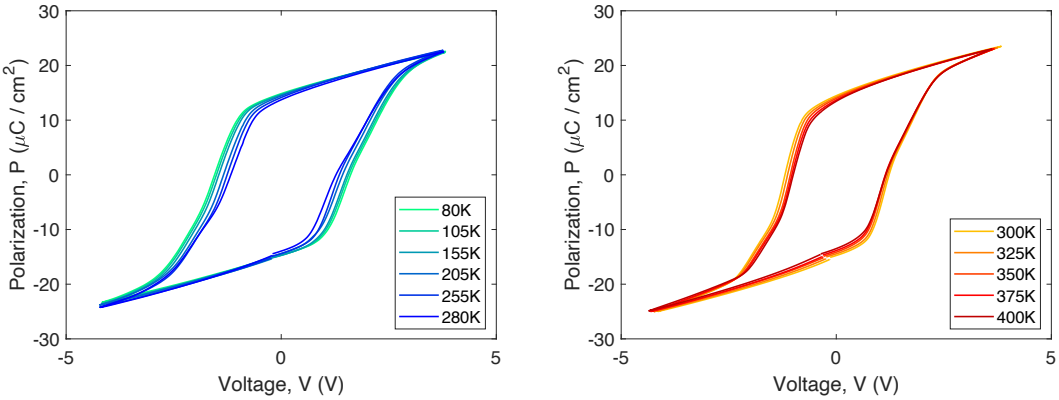
The polarization of the ferroelectric capacitor was measured in a wide temperature range, by applying a triangular waveform at a frequency of 1.0 kHz using a Keithley 4200A-SCS parameter analyzer. The low-temperature measurements (80 K to 280 K) were obtained using a cryogenic microprobe system PMC-150 in a high-vacuum condition (10^{-6} mbar), while high-temperature characteristics (325 K to 475 K) were measured at atmospheric pressure using a different probe station from Cascade Microtech. Before performing the measurements presented in this work, the capacitor under study had been subjected to a "wake-up" procedure, 100 cycles at 4 V.

Figure 2.21 shows the P-V loops measured within two segments of the temperature range examined in this work, from 80 to 280 K and from 300 to 400 K, respectively, where two different probe stations were used. Figure 2.21 (a) shows the P-V hysteretic curves below room temperature. As temperature decreases, a shift of coercive voltage to higher values is observed. Reducing the temperature also has an impact on the remanent polarization (P_R), and a total increase of $1\mu C/cm^2$ was detected. A similar trend was observed in the higher temperature range (Figure 2.21 (b)): as temperature increases, the coercive voltage, and the remanent polarization decrease. In Figure 2.21 (b), the loops show an offset, and their shift towards positive voltage increases with the temperature. In addition to this imprint-like behavior, the symmetry of the polarization hysteresis deteriorates; distortions in the curve are evident above 425 K and dielectric breakdown occurs at 475 K (not shown here).

The positive and negative coercive voltage values, respectively V_{C+} and V_{C-}, extracted from Figures 2.21 (a) and 2.21 (b), are presented as a function of temperature in Figure 2.22. The discontinuity between the two segments of curves occurs due to the different testing environments used for P-V-loop measurements above and below room temperature. The effect of imprint results in a significant shift of V_{C+} and V_{C-} above room temperature, but the average coercive field follows a smooth and close-to-linear trend vs temperature (inset Figure 2.22).

Looking at off-resonance PFM maps at RT in Figure 2.13 (a), one can see independent switching regions, which are switched from a positive to a negative state, while others remained fixed; similar observations were reported in other works and have been associated to extrinsic switching [96, 93]. However, it was argued in our previous work [105] that true intrinsic switching may occur in such systems despite the apparent similarity of the data in Figure 2.13 (a) to the patterns typical for a nucleation-limited switching mechanism.

Furthermore, by observing the trend of the coercive field at different temperatures, it can be



(a) (b)

Figure 2.21: Evolution of P–V hysteresis loops at different temperature conditions: from 80 K to 280 K (a) and from RT to 400 K (b).(Reproduced from [86])

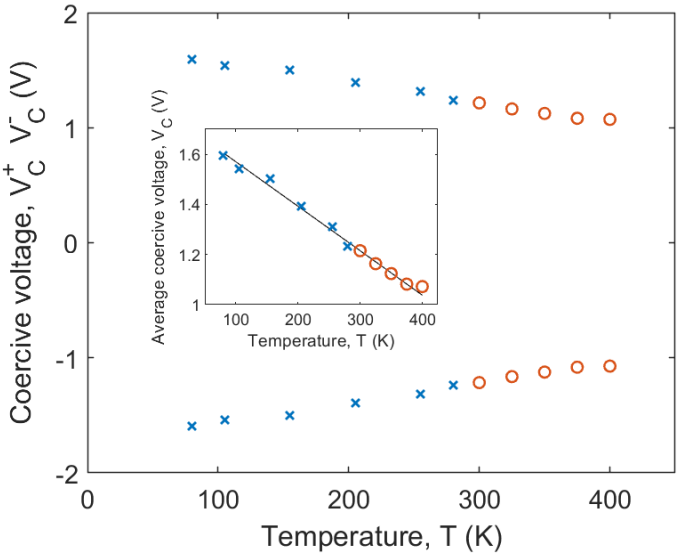


Figure 2.22: Positive, negative and averaged coercive voltage versus temperature.(Reproduced from [86])

seen that it does not follow the trend of E_C proportional to $1/T$ known for NLS switching. On the contrary, our coercive field trend in temperature (inset of Figure 2.22) has a close-to-linear behavior with temperature, which is coherent with the thermodynamic model. However, in the case of NLS, E_C may vary depending on the distribution of activation energies of nuclei, so this discussion cannot be regarded as strict proof.

2.6.2 Curie-Weiss law

The thermodynamic free energy density (U) described within LGD theory [49, 106], can be expressed as a polynomial expansion up to the sixth order, as shown in Equation 1.6. Within this approximation, α is considered linearly dependent on temperature while β and γ are temperature independent.

Although the possibility of first-order phase transition can not be excluded since the Curie temperature is not reached, features like the absence of a broken ferroelectric hysteresis up to 475K (not shown here) and the gradual reduction of polarization are coherent with second-order phase transition. Based on this assumption, the energy polynomial expansion can be simplified and rewritten up to the fourth-order, β is positive and the sign of α changes from negative to positive when the Curie temperature is reached. From Equation 1.6 the electric field across the ferroelectric can be obtained as follow:

$$E(T) = \alpha(T)P + \beta P^3 \tag{2.4}$$

The LGD theory for the second-order phase transition offers a simple description of the two essential parameters related to polarization hysteresis, spontaneous polarization (P_S) and coercive field (E_C) in terms of the coefficients α and β. It is demonstrated later that using this assumption results in a model that is well supported by the experimental data of this work. The free energy presents one maximum around $P = 0$, which is the unstable state; and two minima, which are the two stable states, the positive and negative spontaneous polarization can be calculated as:

$$P_S = \pm\sqrt{-\frac{\alpha}{\beta}} \tag{2.5}$$

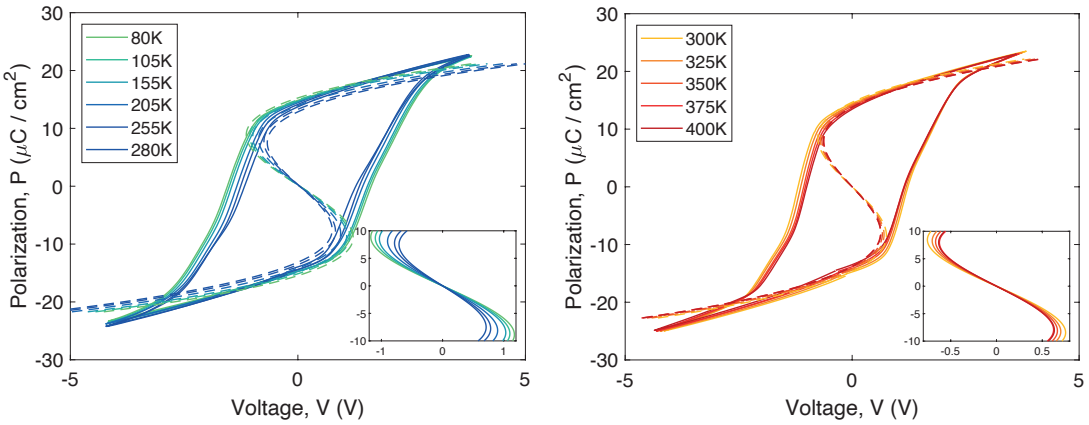
The coercive field can be derived finding the local extremes of the electric field:

$$E_C = \pm\frac{2\alpha}{3}\sqrt{-\frac{\alpha}{3\beta}} \tag{2.6}$$

Using the Equation 2.5 and 2.6, α and β can be extracted from the experimentally measured hysteresis loops. In order to calculate the effective P_R and E_C, the built-in field has been

introduced in order to take into account the imprint effect, and the curves were plotted with respect to the effective voltage drop on the ferroelectric.

Figure 2.23 (a) and (b) show S-shaped polarization curves calibrated on the experimental measurements. Corresponding to the two stable polarization states, the calibrated model follows the experimental data. However, as expected, the negative-susceptibility region of the P-V curve cannot be observed experimentally in a stand-alone capacitor because of its natural instability, as it corresponds to an energy maximum. As the temperature increases, the negative slope of the S-shaped curve increases, resulting in a smaller energy barrier to overcome and a higher equivalent negative capacitance.



(a) (b)

Figure 2.23: P–V hysteresis loops and equivalent S-shaped LGD curve at different temperature condition: from 80 K to 280 K (a) and from RT to 400 K (b).(Reproduced from [86])

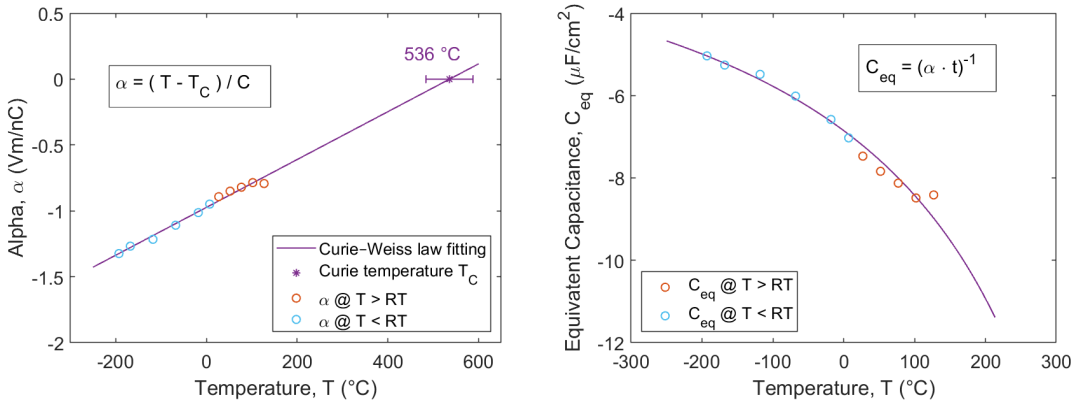
The values of $\alpha(T)$ extracted from the fit follow the linear temperature dependence, in agreement with the intrinsic switching description by LGD theory (Figure 2.24 (a)). The extrapolation of this temperature dependence enables an estimation of the Curie temperature (T_C), according to the Curie-Weiss law (Figure 2.24 (a)):

$$\alpha(T) = \frac{(T - T_C)}{C} \tag{2.7}$$

where C is the Curie constant. Through a fitting of the Curie-Weiss law, the Curie temperature is found to be around 536 °C, which is in line with what was reported for other HfO_2-based ferroelectrics [107, 108, 109]. Based on the experimental extraction of $\alpha(T)$ one can directly plot the dependence of the negative capacitance on the temperature (Figure 2.24 (b)).

As expected from the observations in Figure 2.23, the equivalent negative capacitance increases with temperature following a hyperbolic behavior. Yet, the range of voltage for which the NC region exists shrinks, making the matching more difficult and the instability higher. Insights on the NC values and range of bias are critical in designing a stable NC-FET. Therefore, the

proposed extraction method described here is a useful analytical tool for the assessment of ferroelectric materials and the engineering of NC-FETs.



(a) (b)

Figure 2.24: Alpha coefficient at different temperature and its fitting based on Curie-Weiss law to extract the Curie temperature (536 °C) and the Curie constant (551 K nC / V m) (a). Equivalent negative capacitance extracted from alpha at different temperature and the trend evaluated from the Curie-Weiss law fitting (b). In the equations, A is the area and t is the thickness of Si:HfO_2. (Reproduced from [86])

In conclusion, temperature-dependent polarization and electric field behavior have been studied in polycrystalline Si:HfO_2 thin films. A series of hysteretic P-V curves collected within the temperature range from 80 to 400 K have been analyzed in terms of LGD formalism. The Curie-Weiss law provides a good fit to the extracted coefficients, and the extrapolated Curie temperature (536 °C) is close to the values obtained using alternative techniques. This analysis, together with the previously reported work [105] shows consistency with the intrinsic switching mechanism in HfO_2-based ferroelectrics and supports the use of the LGD model for the description of temperature dependence in these materials. Further, this investigation also illustrates a method to estimate the ferroelectric equivalent negative capacitance, hence helping to engineer a stabilized NC-FET. Finally, these results advance the current understanding of the switching kinetics in ferroelectric hafnia thin films, which is highly relevant for non-volatile memory and NC-FET performance.

2.7 Summary

The work reported in this chapter was focused on the experimental study of Si:HfO_2 capacitors. The first part was dedicated to fabrication and characterization techniques used in this work. In particular, it was focused on ALD technique for Si:HfO_2. Then, the microstructural analysis (GI-XRD, TEM and SEM), electrical (I-V, C-V, P-V), and electromechanical (PFM) characterization were presented as complementary techniques useful to get insights into the fabricated ferroelectric capacitors.

The second part of the chapter reported the optimization of the Si:HfO_2 deposition in terms of annealing conditions and thickness. These parameters were optimized to improve the remanent polarization, such as the main figure of merit in ferroelectric, and to reduce the leakage current, which can impact severly the functionality logic and memory applications. It destabilizes negative capacitance and reduces memory endurance. The Si:HfO_2 optimizations follow some application-relevant requirements for logic and memory applications because the optimized ferroelectric was planned to be integrated into gate stacks and junctionless devices, which are respectively discussed in Chapter 3 and 4. The best-achieved values for application-relevant purposes are: 17 μC/cm^2 of remanent polarization, 45 μA/cm^2 (at 3 V) of of leakage current density and 0.7 mV/cm^2 coercive electric field.

At the end of the Chapter we reported an original study on the switching mechanism in ferroelectric Si:HfO_2, which is highly relevant for the applications targeted in this work: non-volatile memory and NC-FET performance. The data analyzed is essentially based on P-V hysteresis loops measured over wide temperature ranges on various ferroelectric capacitor devices. Based on classic LGD theory, the analysis yielded the temperature-dependent dielectric susceptibility values, which fitted the Curie-Weiss law. The extrapolated Curie temperature value (536 °C) was in line with the data obtained for other HfO_2-based ferroelectrics using different techniques. The work also illustrated a method to evaluate the ferroelectric equivalent negative capacitance value and range of voltages, aiming to study and optimize a stabilized negative capacitance FET.

3 HfO_2–based bilayer gate stack structure

This Chapter is focused on heterostructures in which a linear dielectric is placed on top of the HfO_2-based ferroelectric. This stack is crucial since it gives access to the ferroelectric material's NC region. In the first part of the Chapter, a comparison between Si:HfO_2 FET gate stacks with and without a metal interlayer is performed to evaluate the best configuration for NC stabilization and to extract information on the switching mechanism of the integrated ferroelectric, useful for the Fe-FET design in Chapter 4. The fabricated gate stacks are first characterized by the conventional electrical characterization method (Sections 3.2.2) and then by nanosecond pulse measurements (Sections 3.2.3) to observe NC. To get some insight into the local switching of the integrated ferroelectric, the PFM investigation is performed in Sections 3.2.4. Then to corroborate the previous results on gate stacks devices and increase the knowledge on HfO_2-based ferroelectric switching, a similar study is performed on the HZO bilayer device (Section 3.3). By comparing different measurement approaches (Section 3.3.4), such as nanosecond pulse measurements and quasi-static PFM data, we draw conclusions on the possible polarization reversal mechanism in the ferroelectric-dielectric bilayer. The content of this Chapter is based on the study reported in [110, 111, 105].

3.1 From ferroelectric capacitor to ferroelectric multi-layers devices

The ferroelectric NC effect was proposed to differentially amplify the voltage, allowing the reduction of the SS. This application was proposed by Salahuddin [22], but the concept was first theorized in 1976 by Landauer [112]. The free energy density of a monodomain ferroelectric is modeled as a double-well landscape with respect to the polarization (Figure 3.1(a)), with two energy minima corresponding to the two stable states of the ferroelectric. When the ferroelectric is switching from one stable polarization state to the other, it introduces an effective capacitance that is negative. This corresponds to a negative curvature in the energy profile and a negative slope in the polarization curve.

The S-shaped curve cannot be measured experimentally in a ferroelectric capacitor in isolation. Instead, one observes a hysteretic loop (Figure 3.1(b)), as described in Chapter 2. The voltage

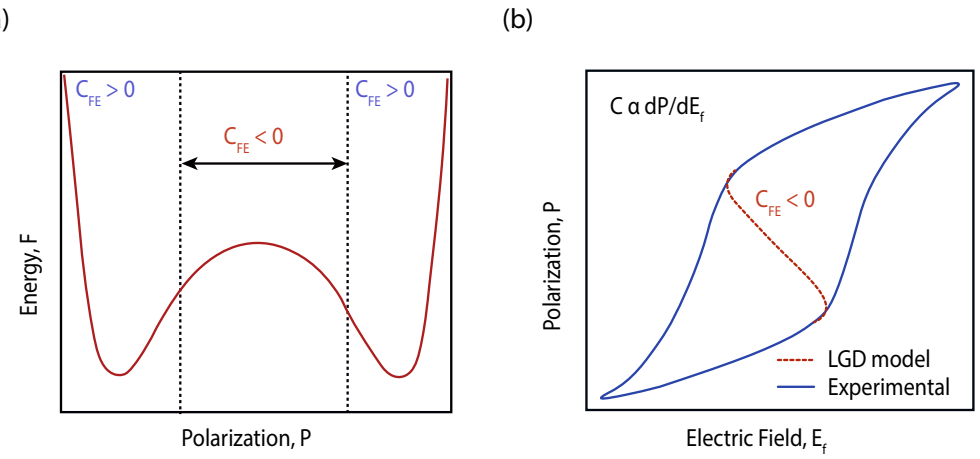


Figure 3.1: (a) Free energy profile predicted by LGD theory. (b) LGD S-shaped polarization curve (red) and experimental hysteretic polarization curve in capacitors (blue). (Reproduced from [111])

is forced across the ferroelectric, and the polarization jumps from one state to the other due to the immediate compensation of the polarization by electrode-free carriers [113]. However, by employing a short pulse measurement method [26], the S-shaped $P-E_f$ curve can be extracted by applying short pulses to a bilayer stack. In this Chapter, this method is used to study the negative capacitance and hysteresis-free $P-E_f$ curve in three structures, two gate stacks and one bilayer device. In addition, we make use of the PFM technique to investigate microscopic local switching in quasi-static mode.

3.2 Si-doped HfO$_2$ gate structures with and without metal interlayer

In NC-FETs, the ferroelectric material is placed in series with the linear gate dielectric to reduce polarization compensation [26] and improve the NC stabilization ([114]). Two gate structures are possible, the metal-ferroelectric-metal-insulator-semiconductor (MFMIS) and the metal-ferroelectric-insulator-semiconductor (MFIS). A significant fraction of NC publications employs the inner metal plane between the ferroelectric and the insulator (MFMIS) [115, 116, 117], while the rest place the ferroelectric in direct contact with the insulator (MFIS) [118, 119]. Despite the apparent similarity between the two structures, one can underline some crucial differences: the presence of an equipotential metal, the interfaces seen by the ferroelectric, and the leakage current. For these reasons, several simulation studies have been done to investigate the impact of the inner metal plane [120, 121]. Experimental studies, however, are less frequent in the literature.

In this section, MFMIS and MFIS gate structures are compared side-by-side by means of electrical measurements. Then we experimentally investigate the negative capacitance by probing the hysteresis-free polarization response, which we analyze in terms of the Landau-

LGD theory. To conclude, we show through PFM how the absence of the inner metal influences the switching dynamics and can affect the NC effects.

3.2.1 Fabrication

The two gate stack structures MFIS and the MFMIS have Si:HfO_2 as ferroelectric and thermally grown SiO_2 as a linear dielectric, which we chose for its thermal stability and ability to provide a low defect interface with the silicon substrate. Figure 3.2 and 3.3 show schematics of the complete devices, together with a summary of the process flow and a TEM image.

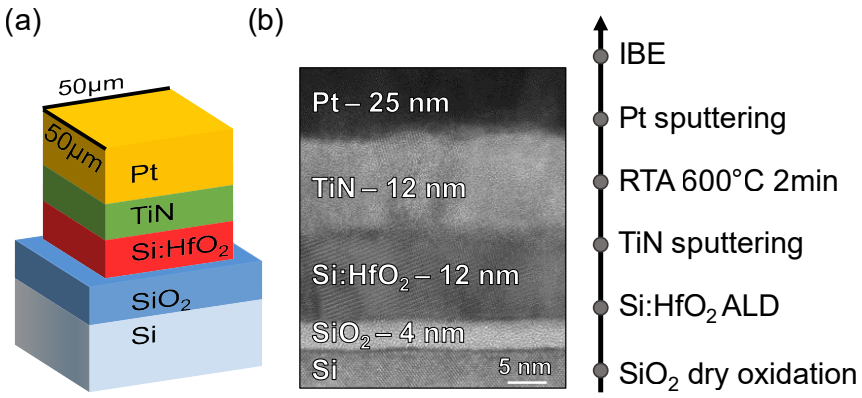


Figure 3.2: MFIS gate stack. (a) Cross section schematic. (b) Cross-section HR-TEM of the fabricated device structure and process steps.

The fabrication process of the MFIS structure (Figure 3.2) began with a p-doped Si wafer (0.2 Ωcm resistivity), which enables it to be employed as a shared bottom electrode for the devices. Afterward, 4 nm of SiO_2 was grown through a dry oxidation process. Subsequently, 15 nm of Si:HfO_2 was deposited by ALD, following the steps in Section 2.1.1. Then, the Si:HfO_2 film was capped with 12 nm of TiN via sputtering. Rapid thermal annealing was performed at 600 °C for 2 min in order to crystallize the Si:HfO_2. On top of TiN, 25 nm of Pt were deposited to serve as top metal contact. Finally, ion beam etching was used to etch the top electrode with different dimensions, 50x50 μm^2 devices being used for the electrical characterization, while 5x5 μm^2 devices are employed for PFM analysis.

The fabrication of the MFMIS, outlined in Figure 3.3 (b), follows the same process steps, the only difference, in this case, was the sputtering of a 24 nm TiN layer between the SiO_2 and Si:HfO_2. This metal contact is employed in order to separate the ferroelectric layer from the SiO_2 with an equipotential layer.

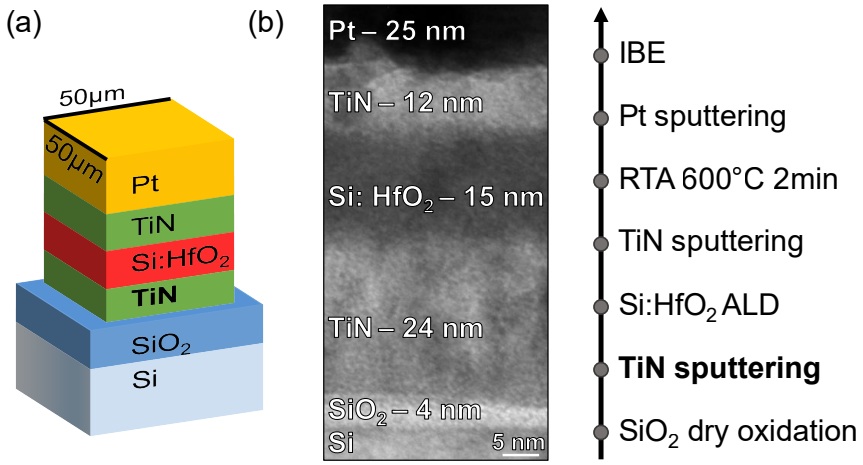


Figure 3.3: MFMIS gate stack. (a) Cross section schematic. (b) Cross-section TEM of the fabricated device structure and process steps.

3.2.2 Integrated silicon-doped hafnia XRD and electrical characterization of the gate

Grazing incidence X-ray diffraction (GIXRD) patterns were measured on the two fabricated gate structures in order to initially investigate the ferroelectric quality of the Si:HfO_2 layer. The

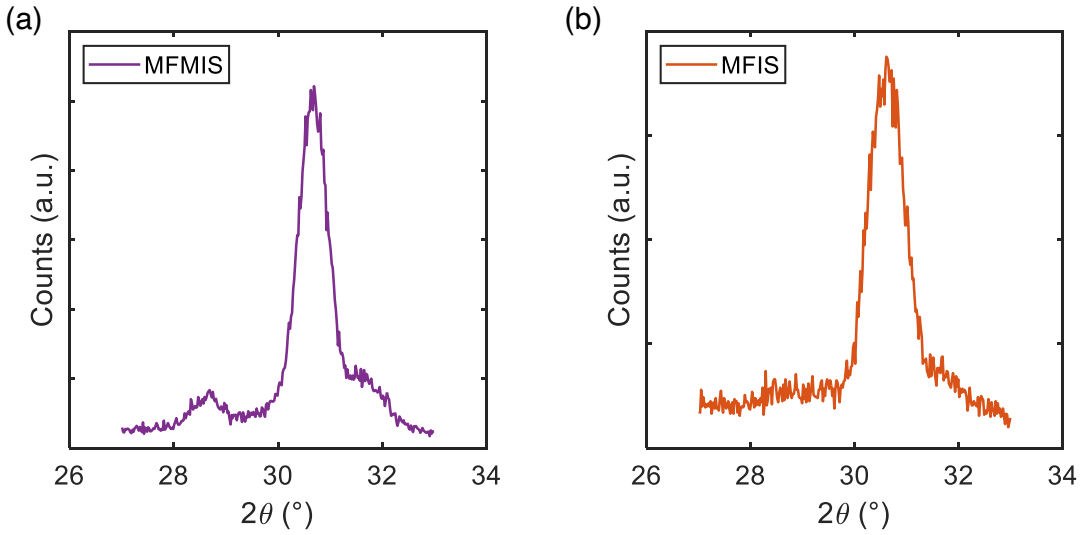


Figure 3.4: GI-XRD pattern of the MFMIS (a) and MFIS (b) showing the ferroelectric orthorhombic peaks at 30.4°.(Reproduced from [111])

scan range of the diffraction angle (2θ) is limited to the 27°-33° range. As it is possible to see from Figure 3.4, in both the gate stacks, there is a predominant diffraction peak around 30.4° attributable to the orthorhombic/tetragonal phase, while the monoclinic phase at 28.3° and 31.7° is a small fraction in MFMIS and a negligible one in MFIS.

In order to study the electrical properties of the two Si:HfO_2 devices, IV measurements were conducted. Figure 3.5 shows the two current peaks originating from reverse domain-induced ferroelectric switching. It is possible to observe that the MFMIS device exhibits a higher leakage current for the same voltage applied (in particular for negative biases). In MFMIS, device breakdown occurs more easily than in MFIS since a single leakage path can kill the device. To reduce the contribution of leakage-related charge transport, which causes polarization screening and destabilization of the NC effect [122], we subsequently used a pulse measurement technique to study the polarization response in these gate stacks.

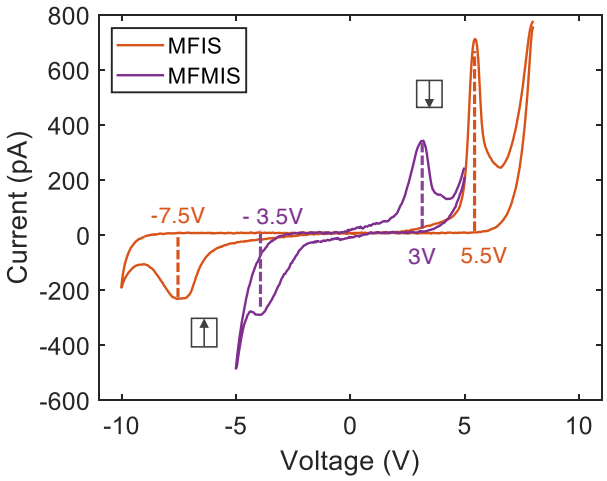


Figure 3.5: Quasi-DC current-voltage measurements on 50x50 μm^2 MFMIS and MFIS gate stacks with the extracted polarization switching voltage for the two polarization states (black arrows). (Reproduced from [111])

3.2.3 Pulse measurements

Uniform non-hysteric polarization and small leakage current are the main requirements for studying NC. To approach this ideal situation, we adopted the concept originally proposed by Hoffmann et al. [26], where their imprinted bilayer was tested in the non-hysteretic regime using short pulses. Thanks to the imprinted state, we can approach the uniform polarization state, and by applying pulses against it, we can extract hysteresis-free $P-E_f$ without really reversing the polarization. In this Section, we study the hysteresis-free $P-E_f$ curve and its negative capacitance region in the fabricated gate stacks devices by the short pulse measurement method.

Method

Figure 3.6(a) depicts the experimental set-up of the device under test (DUT), which is connected in series with a resistor (R) of 1.2kΩ by conductive silver paste. Short negative pulses

are applied to the platinum top electrode using a Keithley 4200A-SCS PMU with RPM units, and, at the same time, the voltage drop on the resistor (V_r) is measured using an Agilent DSOX2024A oscilloscope. In Figure 3.6(b), the short negative pulses (V_a) and the current (I), calculated from V_r, are plotted with respect to time. The pulse width used is 500 ns, which was optimized in order to reduce the hysteresis as discussed below, in Section 3.2.3.

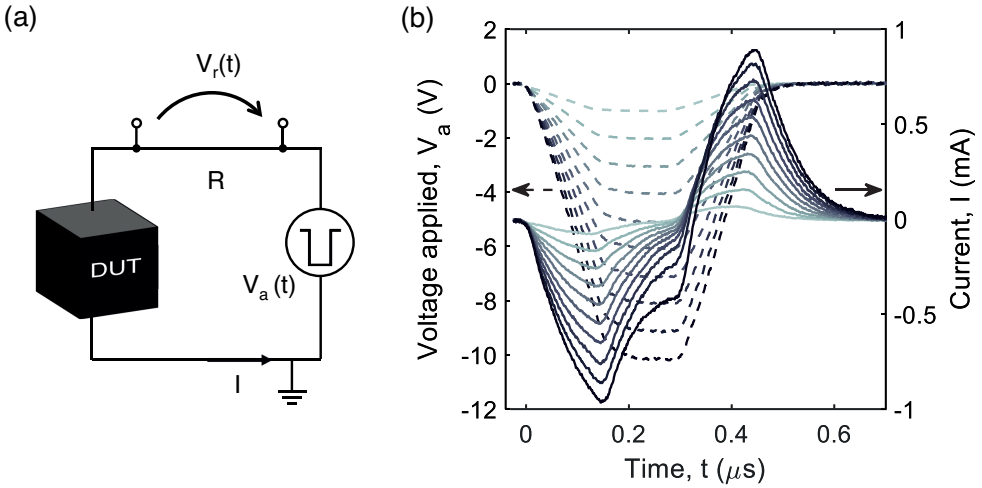


Figure 3.6: (a) Measurement set-up to extract the S-shaped P-Ef curve. (b) Applied voltage pulses and current flow with respect to time for the MFMIS. (Reproduced from [111])

After the integration of the charging and discharging current in time, the charge is evaluated (Figure 3.7(a)). For each pulse, the maximum charge, Q_{max}, and the residual charge, Q_{res}, are extracted. Whereas the effective reversible charge Q_{rev} is defined by:

$$Q_{rev} = Q_{max} - Q_{res} \tag{3.1}$$

In Figure 3.7(b) Qmax, Qres and Qrev are plotted with respect to the maximum voltage applied during each pulse (Vmax). Figure 3.6(b) and Figure 3.7 are obtained on the MFMIS stack. The same procedure was been followed for the MFIS device. The polarization curves presented in the next sections (Figures 3.10(a) and 3.11(a)) are extracted from the reversible charge considering in the calculation also the remanent polarization. This value was quantified as half of the total switchable polarization, an artificial centering technique commonly adopted for PV loop measurement in characterization tools, in which the polarization is the switchable one, not absolute. The electric field across the ferroelectric is calculated as:

$$E_f = \frac{V_a - (Q_{res}/C_d) - V_r}{t_f} \tag{3.2}$$

where t_f is the measured thickness of the ferroelectric. The value of the dielectric series capacitance (C_d) was evaluated by modeling the gate stack and by fabricating and measuring an MIS capacitor with the same oxide thickness and silicon doping. On this sample, capacitive

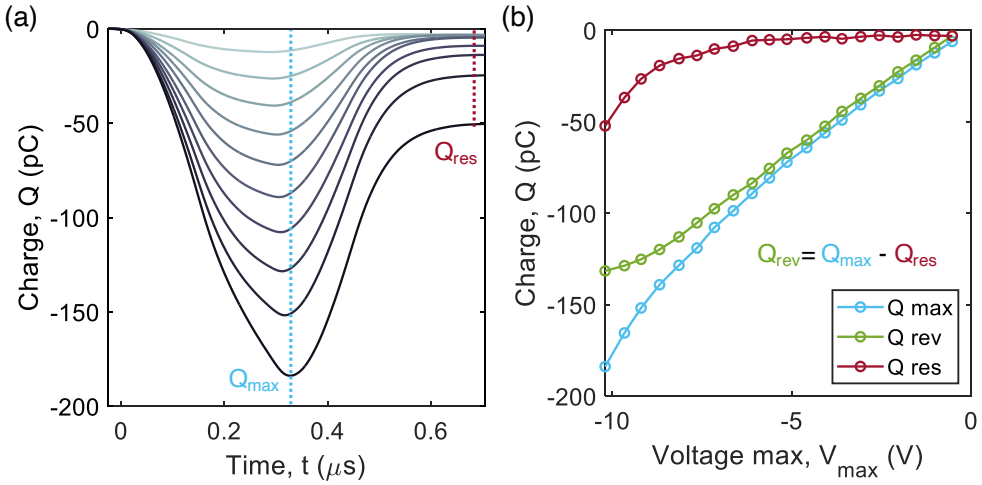


Figure 3.7: (a) Charge as a function of time in MFMIS with dotted lines indicating the maximum charge and the residual charge (b) Maximum residual charge and reversible charge with respect to the maximum voltage applied at each pulse. (Reproduced from [111])

measurements were performed at 100kHz, as shown in the blue curve ($C_{MIS\ meas\ @HF}$) of Figure 3.8. As expected from a p-type substrate, for negative gate voltage, the semiconductor goes into accumulation, and the value of the MIS capacitance normalized by the area is equal to the oxide one (C_{OX}), such as:

$$C_{OX} = \frac{\varepsilon_0 \varepsilon_{SiO2}}{t_{SiO2}} = 860 \frac{nF}{cm^2}, \tag{3.3}$$

where ε_{SiO2} and t_{SiO2} are the permittivity dielectric thickness of and SiO_2, respectively. Figure 3.8 shows also the modeled modelled MIS capacitance at low frequency ($C_{MIS\ mod\ @LF}$).

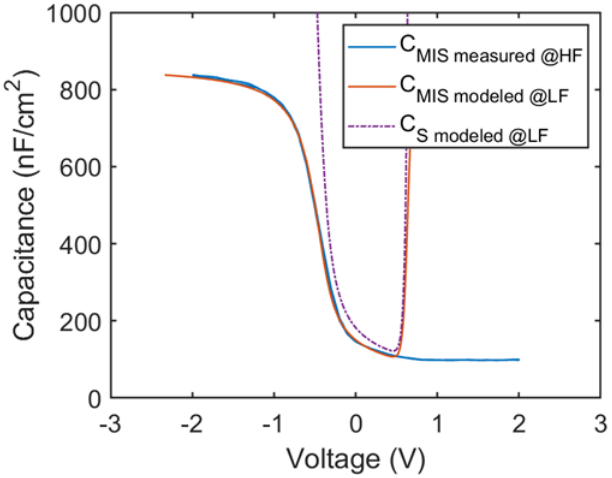


Figure 3.8: MIS CV plot: measured at high frequency (HF) and curve modeled at low frequency (LF)

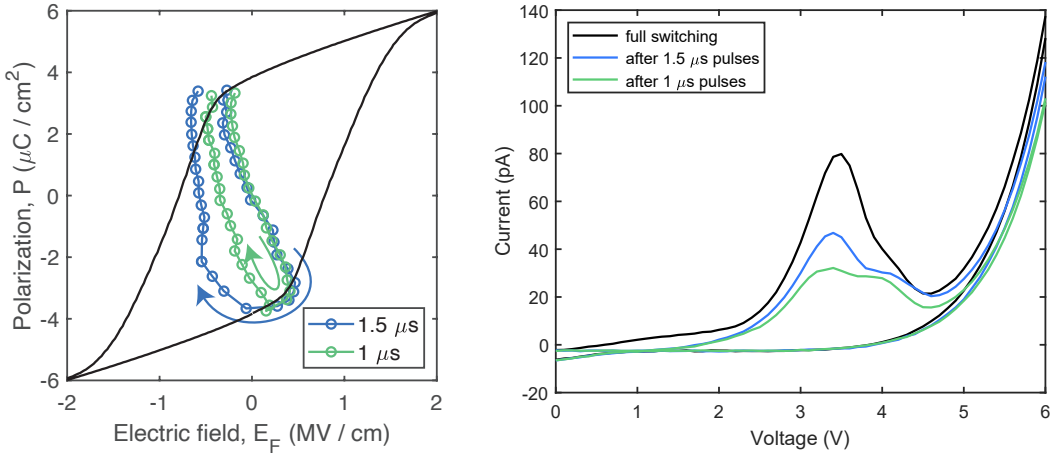
It is worth noting that the ultra-fast pulse measurement voltages applied to the gate are negative therefore, silicon accumulation capacitance is negligible, and we consider just the SiO_2 one. On the contrary, when positive voltages are applied to the gate, the silicon goes into depletion and then inversion. Since we are working around 2 MHz, the inversion layer is not able to follow the short pulses, and the silicon stays in depletion. In conclusion, in the calculation of the electric field across the ferroelectric (Equation 3.2), all the quantities are measured, and none of them is just assumed.

The parasitic capacitances of the set-up were carefully considered and minimized before measuring. The RPM boxes used for the measurements are an external unit of the parameter analyzer connected close to the device to reduce cable capacitance effects, and they contain a pre-amplifier. Before the measurements, to minimize parasitic contributions, the calibration of the set-up was performed in a short and open circuit configuration for ultra-fast pulses.

Once the S-shaped $P-E_f$ curve is obtained by Equation 3.2, it is possible to reconstruct the energy landscape (F) by integrating the electric field with respect to polarization (Figures 3.10(b) and 3.11(b)). The MATLAB code for polarization and energy extraction is presented in Appendix A

Optimization of the pulse width

In this first experiment, 1μs and 1.5μs pulses width were used to check the effect of pulse duration on the polarization. The gate stack used for the optimization was MFMIS. After a positive poling of the device, double sweep pulses from 0V to -9V were applied. The $P-E_F$ characteristic extracted is plotted in Figure 3.9(a). For ascending voltage pulses, the



(a) (b)

Figure 3.9: Effect of the pulse width on the switching. (a) I-V curves extracted after the pulse measurement. (b) $P-E_F$ curves with increasing hysteresis for longer pulse widths.

S-shaped negative slope is approximately not affected. On the other hand, in the case of descending pulses, the negative slope decreases, creating hysteresis in the measurement, which is proportional to the pulse width [26, 110].

To clarify the origin of it, after each set of negative pulse measurements, a positive I-V was measured. Figure 3.9(b) compares the switching current peaks after a negative quasi-static voltage (causing full switch) and after the negative pulse measurements. The trend reveals that the longer the pulses, the higher the switching current peak. It follows that by applying 1μs and 1.5μs pulses, some of the ferroelectric domains switched. To had no hysteresis and repeatedly observe the negative capacitance region, we shortened the pulses to 500 ns, which is the minimum that the set-up could reach.

Experimental observation of the S-shaped polarization curve

Once the pulse width was optimized, the measurement was conducted on the MFMIS and MFIS gate stacks. As a preliminary step, the domains were poled once in the positive state (with the polarization pointing in the direction of the bottom electrode). Then, ascending and descending voltage pulses (in Figure 3.10(a) 1st and 2nd respectively) were applied to check for the absence of any relevant hysteretic switching. From the S-shaped $P-E_f$ curves (Figure 3.10(a)), two negative slopes with a small hysteresis are extracted. The ferroelectric loop (black curve) was acquired on the MFM using an AixACCT TF 2000 tester with FE module at 1kHz and superimposed for comparison. In the beginning, the ferroelectric state is positive, then it encounters the negative capacitance region, and finally, it returns to the positive state. Even though one can observe the Section of the curve with equivalent negative capacitance and negligible hysteresis, the electric field across the ferroelectric does not follow MFM behavior (black curve). The small hysteresis, observable also in the free energy curve (Figure 3.10(b)), and the small coercive field are signatures of the formations of upward-oriented polarization.

The same experiment (positive pre-poling and 500ns pulse width) was repeated on the gate stack without the inner metal plane (MFIS). From the extracted pulse measurements, we can observe a linear negative capacitance region in Figure 3.11(a). The curve reaches the experimental coercive field of the MFM capacitor (black line). The polarization curve has a less steep slope, and therefore, the extracted energy profile (Figure 3.11(b)) has a more pronounced negative curvature and a bigger energy barrier.

In comparing the two gate structures (Figure 3.12), one can observe that the MFIS gate stack shows stronger agreement with the experimental coercive field of the MFM capacitor.

The equivalent differential capacitance is proportional to the slope of the polarization, and it can be calculated as:

$$C_F = \frac{dP}{dE_F}\frac{A}{t_F}, \tag{3.4}$$

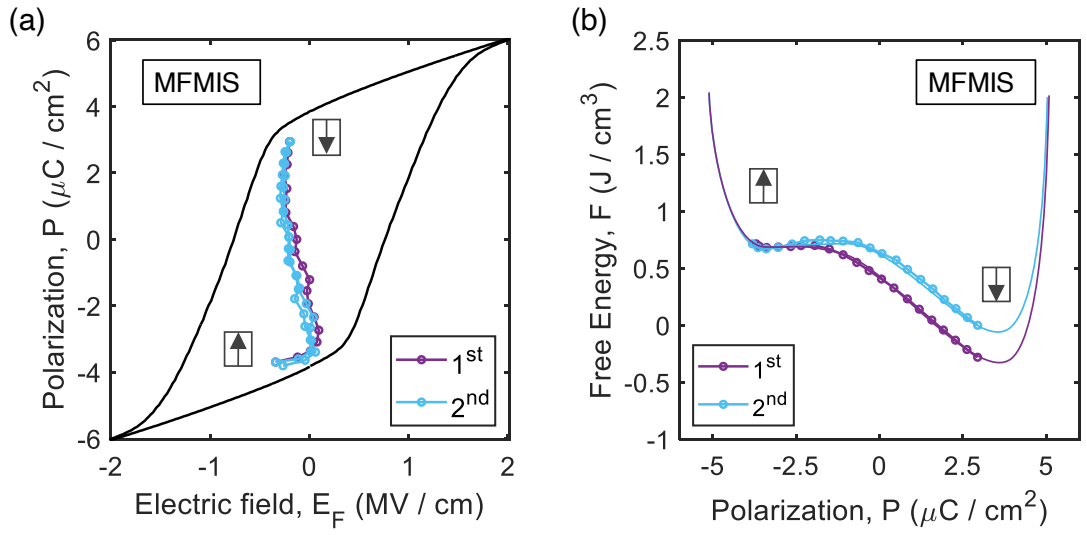


Figure 3.10: (a) MFMIS S-shaped P-Ef curve extracted with the pulse method (b) MFMIS Free energy landscape derived from the P-Ef curve. (Reproduced from [111])

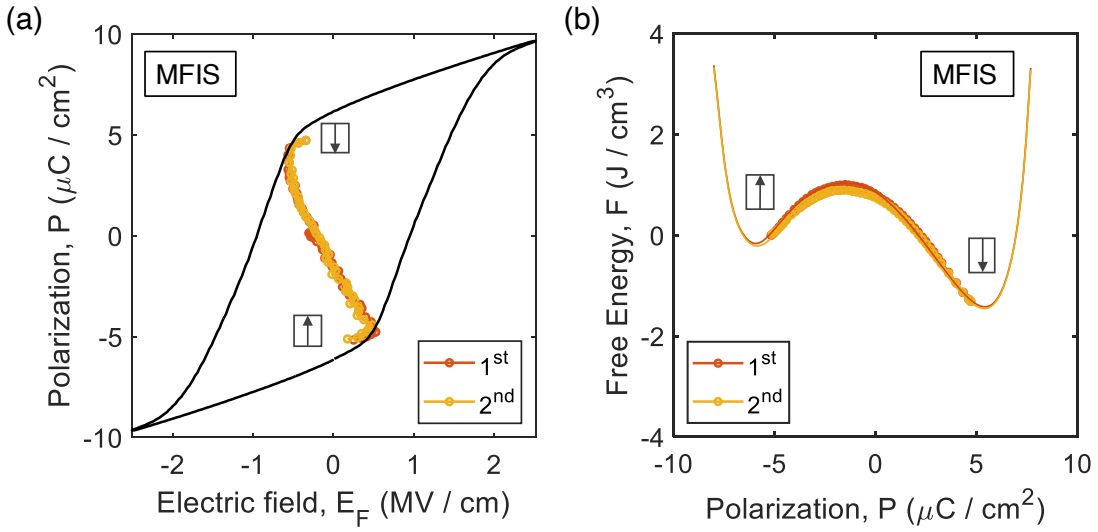


Figure 3.11: (a) MFIS S-shaped P-Ef curve extracted with the pulse method (b) MFIS Free energy landscape derived from the P-Ef curve. (Reproduced from [111])

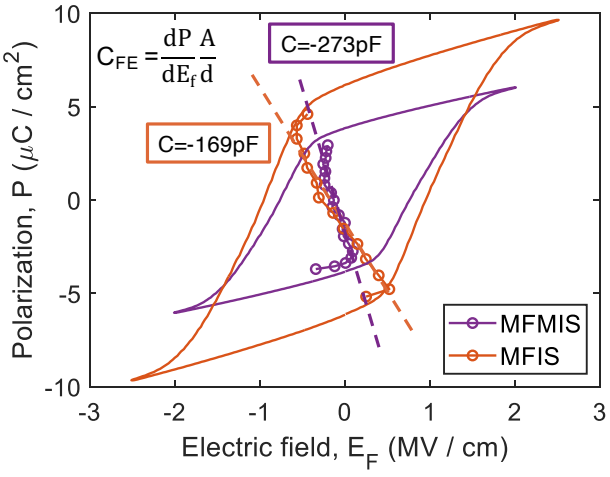


Figure 3.12: Comparison between the S-shaped polarization cure of the MFMIS (purple) and of the MFIS (orange) with an insert showing the equivalent capacitance in the linear NC region. (Reproduced from [111])

where is the area of the device and the thickness of the ferroelectric. The value of the equivalent NC in the MFIS is smaller than the one of MFMIS. Therefore, the differential voltage amplification in the transistor is expected to be smaller. Nevertheless, in the MFIS gate stack, the NC is observed over a larger range of electric field and polarization. This makes it easier to provide a differential bias amplification in the bias range in which the transfer characteristics of a hypothetical FET would need it [123].

It is worth remarking that even if MFMIS and MFIS gate structures seem practically identical, the ferroelectric interface plays an important role. When the ferroelectric is sandwiched by metal electrodes, the polarization is compensated by the charges at the two interfaces. On the other end, in the case of a ferroelectric/insulator interface, the charge compensation is slowed down by the insulator, which gives the possibility of having a uniform non-hysteretic polarization and access to the NC regime. In the case of ferroelectric/metal interfaces, the polarization quickly compensates, and the switching is faster. The presence of symmetrical metal electrodes across the ferroelectric reduces the chances of imprint and traps at the interface. Indeed in the MFMIS gate stack, contrary to MFIS, the polarization curve does not fit the capacitor curve.

To summarize, thanks to short pulse measurements, polarization compensation reduction allowed the observation of a negative slope in the $P - E_F$ in both of the structures. Only the MFIS device yields an extracted coercive field around 0.9 MV/cm^2, which is similar to that of the MFM device. We believe that the behavior observed can be explained by a uniform polarization state, and by applying pulses against it, we can extract hysteresis-free $P - E_f$ without really reversing the polarization. These results revealed the importance of maintaining a uniform polarization state in our experiment to observe the S-shaped curve according to

LGD formalism. So far, we have done our experiment macroscopically, in the next Section, we use PFM on MFIS to verify the ferroelectric imprint and the quasi-static polarization switching microscopically.

3.2.4 PFM evidences of imprint in the MFIS gate structure

Our previous pulse measurements results (Figures 3.12 and 3.15) indicate MFIS to be the more promising candidate for the fabrication of a NC-FET. To enable an insight into the local switching dynamics in MFIS, PFM measurements were performed. The off-resonance technique was used since it was proven to be suitable for probing extremely weak piezoelectric responses with sub-picometer sensitivity [93]. Amplitude and phase of the ferroelectric mechanical were acquired following the approach described in Section 2.4. However, this time, the measurement presents the complication of having a heterostructure with Si bottom electrode.

PFM maps, displaying the amplitude and the phase, were taken on the same area of $1x1\mu m^2$ in different switching stages with an AC bias of 1.3 V at a frequency of 92 kHz. At first, the MFIS device was uniformly pre-poled at +5.5 V, leading to a uniform positive polarization of the ferroelectric (as shown in 3.13(a)). Then the mixed state was induced by applying a voltage equal to -6.5 V (close to the negative coercive field observed in PV measurements). As expected, some of the domains changed the polarization, while others remained fixed (3.13 (b)). Finally, in an effort to induce the opposite state, the maximum voltage allowed by the setup, i.e., -9.5 V, was applied.

A low amplitude response and a noisy phase are observed in 3.13(c). The topography data collected concurrently with the PFM maps indicate that the results are not affected by a cross-talk between topography and electromechanical response. The polarization imprint in the positive state can explain the impossibility of switching the ferroelectric permanently in the negative polarization state. If we consider the current-voltage characteristic (Figure 3.5), switching from positive to negative and from negative to positive both seem to occur, but PFM analysis shows an unstable negative state (with the polarization pointing in the direction of the top electrode). Moreover, from the observation of PFM maps, the polarization seems to switch back to the positive state spontaneously. Indeed, from a first analysis of the phase in 3.13(c), it is possible to observe a polarization gradient in the Y direction, the same as the PFM scan, i.e., from top to bottom. The polarization at the bottom of the map seems to became positive since the full measurement takes more than 4 hours.

Then PFM loops were extracted at 92KHz. The applied DC field reached 8.5 V with an AC of 1.3 V, having AC + DC close to 10 V, which is the maximum voltage allowed by the set-up. The piezoresponse amplitude and phase are shown respectively in Figure 3.14(a) and 3.14(b).

In the plots, DC ON represents the case with non-zero DC voltage applied, while DC OFF represents the case with zero DC voltage applied. The phase shows a complete 180° switch.

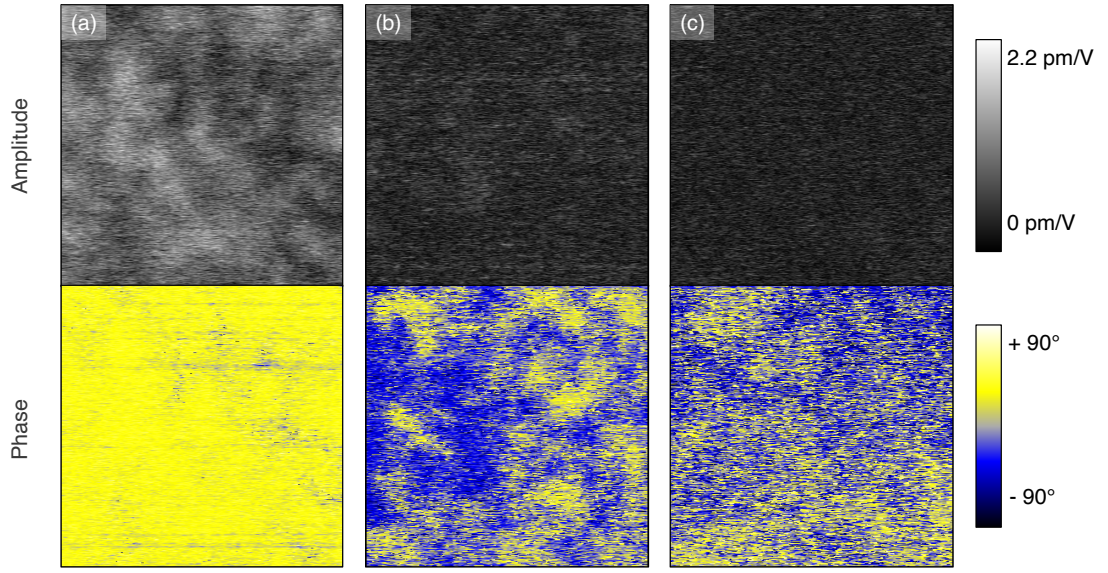


Figure 3.13: PFM maps of the amplitude and the phase of the same area ($1x1\mu m^2$) in different polarization states: (a) positive state (+5.5 V), (b) mixed state (-6.5 V) and (c) negative state (-9.5 V). (Reproduced from [111])

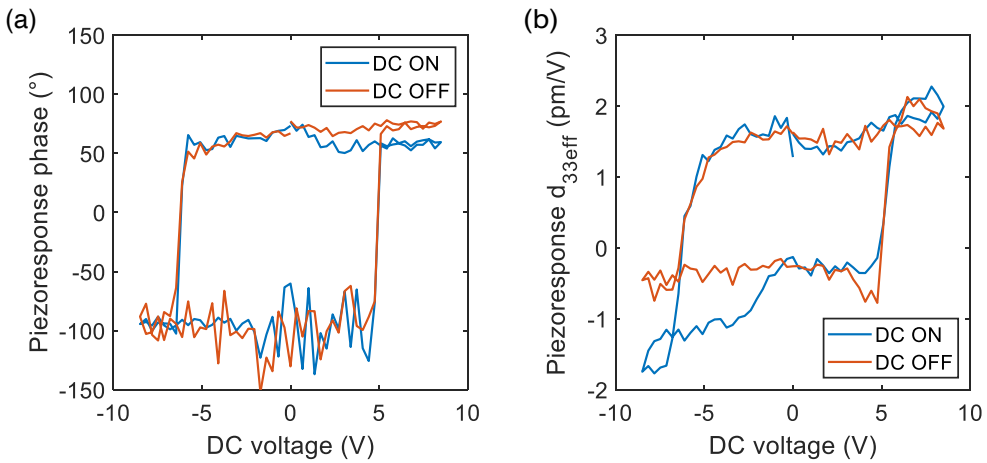


Figure 3.14: Piezoresponse phase (b) and amplitude (c) loops of MFIS gate stack. (Reproduced from [111])

The signal is clean for the positive polarization state but noisy in the negative one and in particular in the case of DC OFF. The amplitude plot shows a significant feature that is in line with what was stated before: when the voltage is applied (DC ON), the signal in the negative state is initially as strong as in the positive state, meaning that the material can be poled and has a proper response. However, when the voltage is not applied (DC OFF), the magnitude of the response drops immediately, meaning that the material does not retain the negative polarization state. Eventually, when the applied voltage is lower than the built-in field, the response under the field also becomes small. It is worth noting that the piezoresponse

amplitude at high fields is not saturated, but some clockwise loops can be visible. This feature indicated charge injection caused by the leakage current at high fields.

The imprinting of the positive state in the MFIS gate stack was indicated by the pulse measurements and then corroborated by PFM maps and loops. The built-in field, which imposes the imprint, can be generated by the work function difference between Si and TiN electrodes, which are sandwiching the ferroelectric material [124]. Another plausible cause is the presence of trapped charges at the Si:HfO_2-SiO_2 interface [125, 126].

Overall, we observed that in MFIS gate stack device, the ferroelectric could switch quasi-statically in both directions. But as pointed out by the PFM analysis, the negative state is not stable, and when no voltage is applied, the polarization value drops, revealing the positive state imprint. This implies the presence of an internal field acting on the ferroelectric, possibly coming from the asymmetrical electrodes.

Before the Fe-FET fabrication (Chapter 4), we performed experimentally calibrated simulations at the transistor level using the values extracted from the short pulse measurement. Both gate stacks were used in the simulation, and a comparative assessment of the FET performance was carried out.

3.2.5 Experimentally calibrated NC-FET simulation

Using the ferroelectric values, extracted on MFMIS and MFIS gate stacks, we investigate the ferroelectric as a performance booster. The simulation was carried out on a 14nm CMOS node ultra-thin body and buried oxide (UTBB) fully depleted silicon-on-insulator (FD-SOI) n-MOSFETs with a nominal gate length of 20 nm. The channel, the buried oxide (BOX), and the gate equivalent oxide thicknesses are 6 nm, 25 nm, and 0.9 nm, respectively. The channel is undoped ($10^{15}/\ cm^{-3}$) and the source and drain doping level is $> 5x10^{20}/\ cm^{-3}$. The saturation current at Vdrain=Vdd is 1.12mA/μm, and the leakage is below 100 nA/μm. The ferroelectric parameters were extracted from the curves in Figures 3.10(a) and 3.11(a).

Figure 3.15 depicts the calibrated simulation results of the corresponding NC transistors versus the reference device. The signature of non-hysteretic NC region was obtained (single-valued transfer characteristic) for the MFIS stack, in total contrast with the MFMIS structure for which an instability appears. The subthreshold swing of the NC-FET with MFIS parameters shows a significant improvement of the swing that can be explained by a surface potential derivative greater than unity. This improvement is apparently more significant in MFMIS structure, but this is because the ferroelectric has a hysteretic behavior and jumps to the other branch of the polarization, showing an almost infinite gain. The transition point is where the structure's total capacitance changes from negative to positive, which is also observed in the gain plot (the gain jumps from positive values to negative, $\beta = C_F/(C_F + C_{MOS})$). This investigation showed the importance of gate stack engineering to distinguish polarization switching from hysteresis-free NC-FETs.

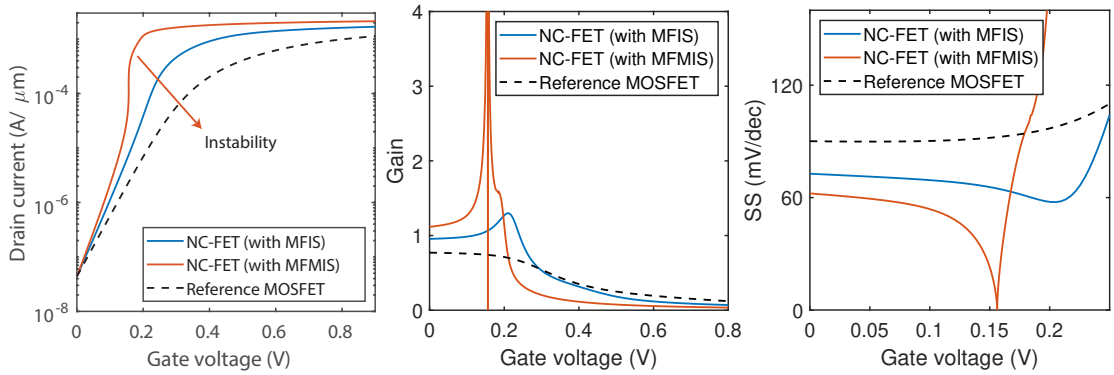


Figure 3.15: Results of Id-Vg calibrated simulations based on the extracted experimental values for MFMIS and MFIS capacitors and using a 14nm CMOS node MOSFET as a reference device showing the transfer characteristic (a) and the extracted gain (b) and SS (c).(Reproduced from [110])

To conclude, the study on MFMIS and MFIS gate stacks was performed with different techniques: simulations, quasi-static measurements, and nanosecond measurements. The devices without internal gates showed low leakage current and one preferred state of polarization, hence no hysteresis. Consequently, MFIS gate stack can be employed for NC-FET. On the other hand, devices with MFMIS gate structure have symmetric electrodes sandwiching the Si:HfO_2, and as a consequence, there imprinted state is less likely, and polarization compensation is faster. Therefore we propose this gate stack for memory application. These results on gate stack structures are the building block for the design of FET with integrated ferroelectric, discussed in Chapter 4.

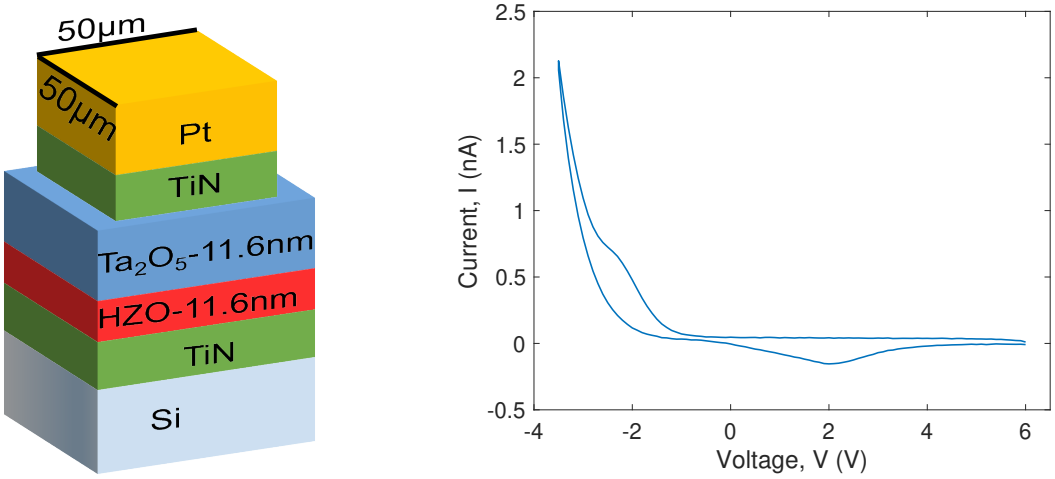
3.3 HZO bilayer structure

This Section analyzes the Metal-Insulator-Ferroelectric-Metal (MIFM) multi-layer device using the same approach followed for the MFIS gate stack in Section 3.2. We carry out quasi-static measurement, i.e., current-voltage curves (Section 3.3.1) and PFM data (Section 3.3.3), and ultra-fast measurements (Section 3.3.2).The aim of this work is to validate the pulse measurement setup and debate the switching mechanism by comparing these different measurement approaches (Section 3.3.4).

3.3.1 Device structure and leakage current considerations

The MIFM device was fabricated by Namlab [26], and it consists of a bi-layer of a linear oxide (Ta_2O_3) and a ferroelectric thin film (HZO) sandwiched by metal layers, as shown in Figure 3.16(a). Here, compared to the MFIS device, the linear oxide is thicker, 13.5 nm instead of 4 nm, and is deposited on top of the ferroelectric instead on the bottom. The higher thickness

could originate lower leakage current and a higher depolarization field [127], favoring the NC observability. Furthermore, having Ta_2O_3 on top of HZO reduces the piezoresponse detected by PFM.



(a) (b)

Figure 3.16: Schematic of MIFM device (a) and quasi-static IV characteristic on $50x50\mu m^2$ (b)

In order to have the first proof of the MIFM electrical characteristic, the I-V was measured between -3.5 V and 6 V. As shown in Figure 3.16(b), the coercive voltage extracted quasi-statically is symmetric, around 2.5 V. However the curve shows a strong current asymmetry, for negative voltages, the device has a much higher leakage current value, which agrees with the observation of easier breakdown for negative voltages [26].

3.3.2 Pulse measurements

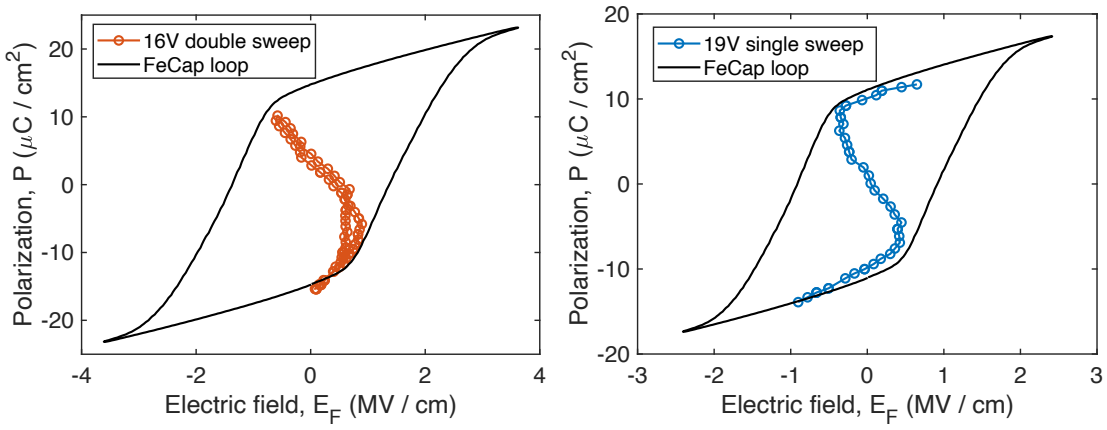
The MIFM device was tested by means of pulse measurement technique following the approach of Section 3.2.3. This characterization aims to validate the pulse measurement set-up and to confirm the behavior observed initially by Hoffmann et al. with the very same MIFM device [26]. The set-up is fundamentally the same, 500 ns pulses with increasing amplitude were applied to the MIFM device connected in series with a resistance ($R = 570\ \Omega$). In this case, however, positive pulses were applied since the stable state of the ferroelectric is the negative one [26].

Figure 3.17(a) is obtained by applying pulses with increasing (from 0 to 16 V) and then decreasing (from 16 V to 0) amplitude, which are modulating the S-shaped polarization from -16 $\mu C/cm^2$ to 10 $\mu C/cm^2$. The S-shaped $P-E_f$ curve shows a little hysteresis, meaning that the charge compensation was slow enough to prohibit the polarization switching.

Then the maximum voltage pulses was increased to 19 V on other MIFM devices. Figure 3.17(b)

shows the only $P-E_f$ curve extracted at such a high electric field. Here we can observe the full S-shape curve, with a polarization value ranging from -15 to 12 $\mu C/cm^2$. This time just a single sweep is applied because the high bias broke the device at 19.5 V. It is worth mentioning again that 16 V and 19 V are the total voltage applied to the whole system, including the resistance connected in series with MIFM.

Based on the $P-E_f$ curve in Figure 3.17, the average intrinsic coercive field is 0.7 MV/cm, which is consistent with the values observed in the MFM capacitors structure.



(a) (b)

Figure 3.17: MIFM S-shaped $P-E_f$ curve extracted with the pulse method with a double sweep, from 0 to 16V and back, (a) and with a single sweep, from 0 to 19V (b).

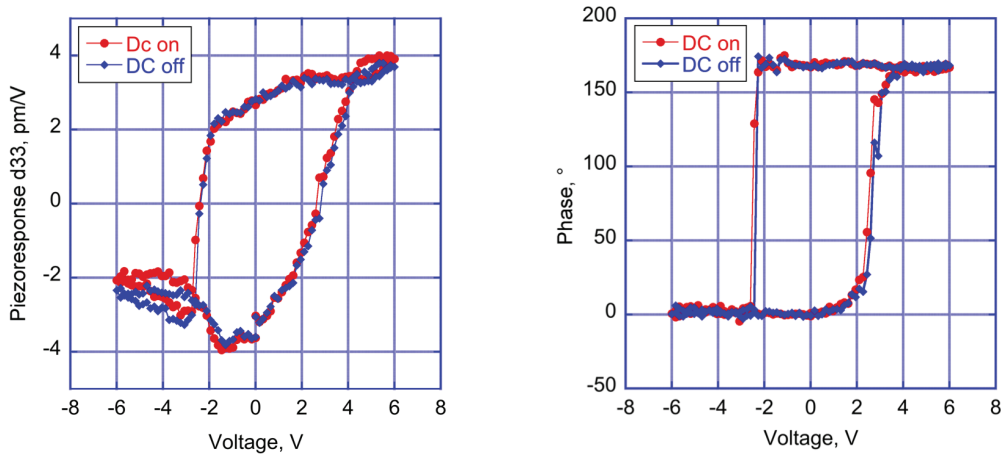
We can conclude that pulse measurement allows extracting the S-shaped characteristic predicted by LGD, and from them, it is possible to extract fundamental quantities like the average intrinsic coercive field. These measurements are closely resembling the work of Hoffmann et al., validating our set-up and our extraction method for the $P-E_f$ S-shaped curve.

3.3.3 Nanoscopic analysis

After looking at the leakage study and the response to 500 ns pulses, which does not allow charge compensation and switching, the local quasi-static PFM technique is used. This is placed at the opposite time scale compared to the pulse measurement method.

At first, the hysteresis loops of amplitude and phase were acquired by applying an AC bias of 1 V at a frequency of 92kHz, as shown respectively in Figure 3.18(a) and (b). The similarity of the loops in the DC-on and DC-off mode demonstrates good polarization retention in HZO film, but it shows asymmetry in the amplitude value. This unusual behavior can be explained by the presence of a thick dielectric on top of the ferroelectric.

As it is observable in Figure 3.18(a), signs of high leakage appear through clock-wise amplitude



(a) (b)

Figure 3.18: Hysteresis loops of amplitude (a) and phase (b) of local piezoelectric response measured through the electrode with the ac signal of 1V at a frequency of 92kHz. (Reproduced from [105])

loops at high fields. The behavior looks more evident for negative bias, which is in line with the observation of the leakage current in Figure 3.3.1. Another similarity with the IV curve can be found in the switching, which occurs at the same voltage, around 2.5 V. Contrary to what was observed for MFIS, the switching of the ferroelectric seems symmetric. This might indicate that the asymmetry observed in MFIS coercive voltage arises from the asymmetry in the top and bottom electrodes.

Then the PFM maps were taken on the same on the same area of $1.5x1.5\mu m^2$, in which three sequential maps are acquired by poling the MIFM device with -6V, then 6V, and finally -6V, as shown in Figure 3.19. From the piezoresponse maps, one can observe the presence of strongly non-uniform patterns: all three images show a mixed polarization state, where one can notice single switching regions of about 30 nm.

Looking more carefully at Figure 3.19(a) and 3.19(c), one can notice that these regions look like independently switched areas rather than domains. The difference is that their growth is limited by clearly defined boundaries, which remain unchanged from one switching cycle to another. Such phenomenon might be explained by non-ferroelectric regions, such as secondary phase or localized charge defects, which are likely to be present in polycrystalline ferroelectric like ALD HfO2-based ones. This result is not predicted by the switching scenario of growing polarization domains, which have boundaries expanding when subjected to the electric field.

In view of these findings, the switching mechanism is investigated in MIFM devices with new experimental results and also by comparing quasi-static measurements with ultra-fast pulse characterization.

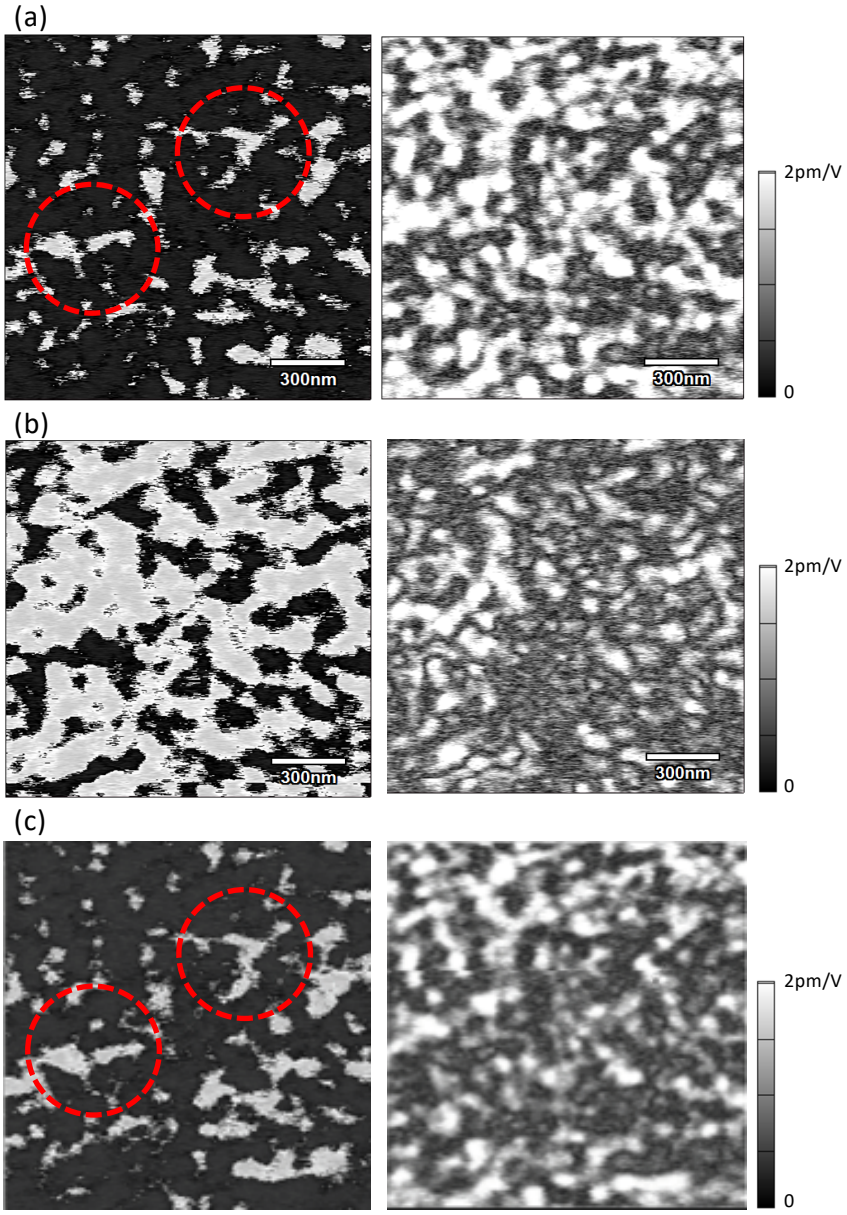


Figure 3.19: PFM maps of the phase (left) and amplitude (right) acquired with an AC voltage of 1V at a frequency of 92kHz showing sequential poling. (Reproduced from [105])

3.3.4 Intrinsic switching: insight from PFM and pulse measurement

The non-hysteretic NC regime can not be achieved if the polarization reversal is controlled by nucleation-limited switching (NLS) [128].This type of polarization reversal mechanism assumes the local nucleation of domains in preferential sites located in areas rich of defects, such as interfaces. Thanks to defect-assisted stabilization, the switching generally occurs at a lower electric field. In thin ferroelectric films, like HfO2-based ones, the interface-related problems become more relevant than in bulk ferroelectrics because the interfacial layer to total thickness ratio is higher. That is why the NLS mechanism is considered predominant in many thin ferroelectrics. Consequently, the dispute of intrinsic/extrinsic switching in HfO2-based ferroelectric films is particularly relevant to NC applications.

PFM measurements are considered a quasi-static characterization method since a single loop takes several seconds. In this time scale, NLS is favorable, and the switching time would depend on the nucleation times of the domain (τ), which it was shown experimentally [129] to depend exponentially on the electric field (E_f):

$$\tau = \tau_0 exp\left(\frac{E_0}{E_f}\right)^2, \tag{3.5}$$

where τ_0 and E_0 are constants. Equation 3.5 indicates that domain nucleation can occur at a lower voltage with quasi-static measurement (seconds) than with ultra-fast pulses (hundreds of nanoseconds). Following this assumption, the switching mechanism in PFM that activates first should be the NLS. To verify this hypothesis, one can compare the coercive voltage extracted by PFM loops and the S-shaped $P-E_f$ curve.

The voltage at which the ferroelectric is switching was extracted from the PFM loop from 5 measurements obtained in different spots, and it is equal to $\pm$ 2.6V. At the coercive voltage, the averaged polarization is null, and the continuity of the electric displacement vector becomes $E_F\varepsilon_F = E_D\varepsilon_D$. In this condition, the coercive field (V_C), such as voltage drop on the ferroelectric, can be calculated with a voltage divider:

$$V_C = V\left(1 + \frac{t_D\varepsilon_F}{t_F\varepsilon_D}\right)^{-1} \tag{3.6}$$

where V is the total applied voltage, t_D, ε_D, t_F, ε_F, are thickness and dielectric constant for the dielectric and ferroelectric layers, respectively. Knowing that the thicknesses of the layers (see Figure 3.16(a)) and the dielectric constants (ε_D = 23.5) and (ε_F = 42 [26]), the extracted coercive voltage is $V_C = 0.84V$, which corresponds to a coercive field $E_C = 0.7MV/cm$. This value agrees with the extraction given by the S-shaped curve analysis. Hence, PFM quasi-static extraction produces the same E_C as one from the ultra-fast pulse measurement method, which is consistent with polarization reversal caused by intrinsic switching but incompatible with

NLS theory, which would predict two different values.

However, in this case, the value extracted by the PFM could be affected by trap charges at the insulator/ferroelectric interface, possibly caused by the leakage current observed in Figure 3.16(b). If this occurs, the subsequent switching would be at a higher electric field because trapped charges will work against the applied field [130]. This means that the stronger the maximum field, the higher the trap charges and the coercive voltage value would be. This would explain why methods working at opposite time scales provide a similar value of E_C even with NLS.

To address the possible influence of the trapped charge, the E_C was measured by PFM loops with different maximum voltages. Figure 3.20(a)-(f) shows phase loops from the same spot, but with a maximum voltage ranging from 5V (3.20(a)) to 7.5V (3.20(f)). The leakage distorts the curve for negative voltages, but the charge seems not to stay at the dielectric/ferroelectric interface and therefore does not affect the coercive voltages, which seem constant throughout the different loops.

The coercive voltages from Figure 3.20(a)-(f) are then measured at the phase of 90° and collected in a dot plot in Figure 3.20(g). For positive voltages, the E_C trend is constant, while for negative voltages, a small shift of +0.5V is detected, which can be caused by the degradation of the loop and not by charge trapping. This, in turn, is coherent with the high leakage observed above for negative voltages (Figure 3.3.1). Overall, the charge seems not to stay at the dielectric/ferroelectric interface and does not influence the measurement of the coercive field. Hence the E_C value obtained by PFM can be considered as intrinsic.

The striking similarity of coercive field measured with two opposite approaches, off-resonance PFM, and ultra-fast pulses, points to the possibility of intrinsic switching in MIFM structures. PFM maps exhibit region by region switching, which is typical of this NLS model. Although this does not necessarily preclude multi-domain intrinsic switching, the two scenarios resemble one another because they both involve switching that takes in independent nanometer-sized regions. The significant difference is that these areas have clearly defined boundaries with a shape not affected by sequential poling. This result is not predicted by the switching scenario of growing polarization domains, which have boundaries expanding when subjected to the electric field.

In conclusion, this work presents pieces of evidence, which are pointing to intrinsic switching as the main mechanism of polarization reversal in MIFM. This has important major repercussions not just for NC applications but also for memory applications. Unlike NLS, intrinsic switching is less temperature-dependent, faster, and depends less on the interface qualities crucial in thin films like HfO_2-based ferroelectric.

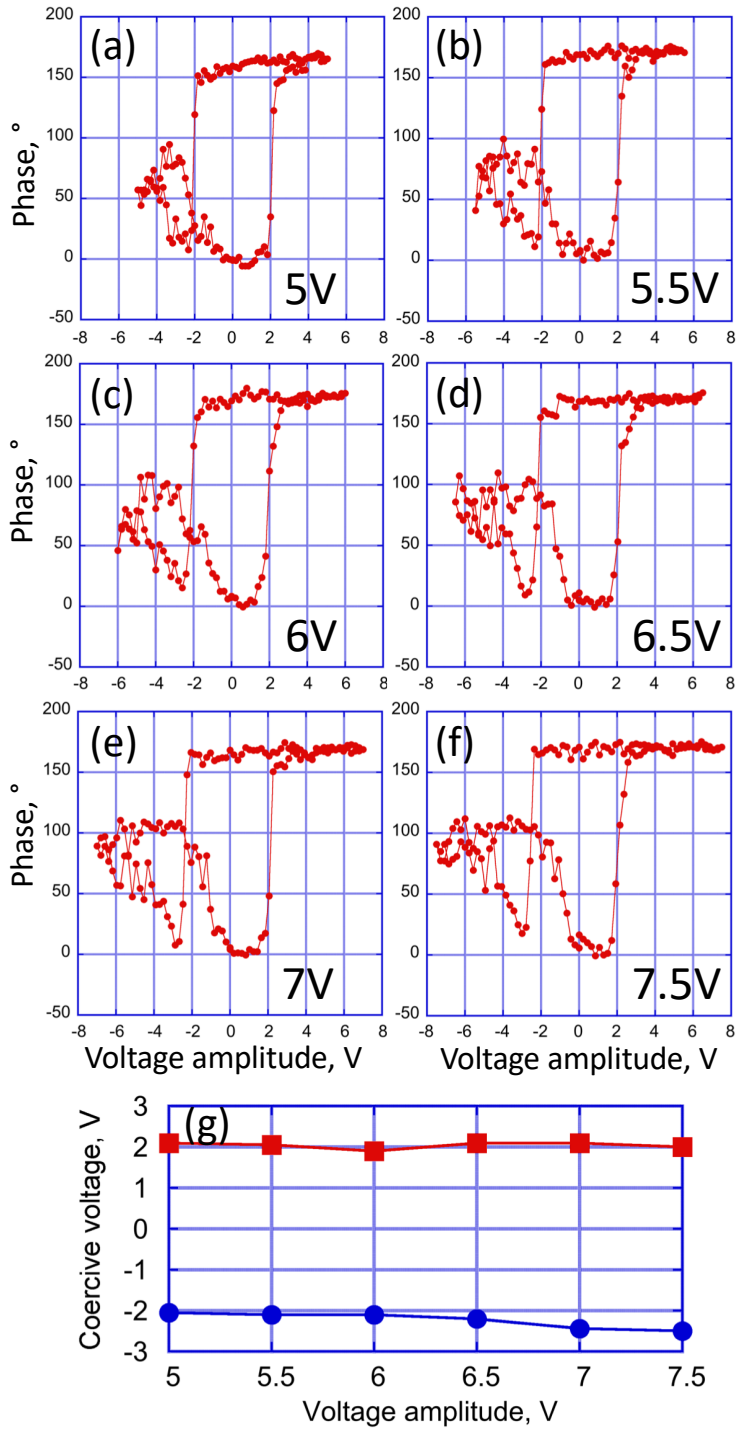


Figure 3.20: From (a) to (f) hysteresis loops of the phase of local piezoelectric response measured on the single spot, with the maximum voltage amplitude increasing from 5V to 7.5V. (g) Coercive field extracted from (a) to (f) and plotted vs. the maximum voltage applied. (Reproduced from [105])

3.4 Summary

In this Chapter, we experimentally explored the NC region in heterostructures containing a linear dielectric and an HfO_2-based ferroelectric.

At first, MFMIS and MFIS gate structures with Si:HfO_2 ferroelectric were analyzed by IV and ultra-fast pulse measurements. This last technique allowed us to reduce the charge leakage, mitigate the screening of polarization charges and, consequently, observe the NC regions in S-shaped $P - E_f$ curve for both MFIS and MFMIS. Our results indicated that the polarization response of the ferroelectric layer in an MFIS device is consistent with LGD theory, since we observed a coercive field similar to the MFM device, measured at lower frequency. On the contrary the MFMIS device showed a little polarization hysteresis and a much smaller coercive field than the MFM capacitor. To enable an insight into the switching dynamics in MFIS, PFM measurements were performed, indicating imprinted uniform polarization of the negative state and imprinted positive state. The root cause can be found in the presence of the built-in field generated by asymmetric electrodes across Si:HfO_2. Therefore, the MFIS gate stack could be engineered to impose one state, leading to a stabilized hysteresis-free NC region. On the other hand, MFMIS gate stack devices have symmetric electrodes sandwiching the Si:HfO_2, and consequently, the imprinted state is less likely, and polarization compensation is faster. Therefore we propose this gate stack for memory application.

Then, a MIFM device with HZO film was studied using the same approach followed before: IV characterization, ultra-fast pulses, and off-resonance PFM. The pulse measurement technique was used to extract the S-shaped P-E_f curve characteristic predicted by LGD, from which it was possible to observe the NC region and obtain fundamental quantities like an intrinsic coercive field. PFM phase loops with different voltage amplitudes corroborated the previous IV results regarding the amplitude and symmetry of the E_C. Furthermore, E_C value showed limited dependence on the maximum applied bias, which signifies that the measurement is not affected by charge injection. PFM maps exhibited region-by-region switching, maintaining defined boundaries, which were not affected by sequential poling. This phenomenon can be explained by intrinsic switching. To obtain information on the switching dynamics, the MIFM E_C value from PFM is compared with the intrinsic one obtained with ultra-fast pulses. Even though the measurements were performed at opposite time scales, the two values showed a remarkable similarity. This result is consistent with intrinsic switching but not with NLS theory, which would have predicted lower E_C for quasi-static PFM characterization.

In conclusion, this Chapter contributed to the understanding of ferroelectric gate stacks by providing an experimental demonstration that the absence of the inner metal plane in the gate structures could beneficial for NC observation in hysteresis-free Fe-FET. Comparing results from conceptually different techniques, such as pulse measurement and off-resonance PFM, gave insights into the switching mechanism and into design paramethers, helpful for the development of our Fe-FETs in Chapter 4 for memory and logic application.

4 Ferroelectric Junctionless FET

This chapter reports Fe-JLFETs with Si:HfO_2 for two different targets: steep slope logic switches and neuromorphic devices. The devices are built on UTBB-SOI with an ultra-thin buried-oxide, which allows us to use it as a bottom gate oxide. For the first targeted application, Fe-JLFETs are fabricated with an MFIS gate stack to reduce polarization compensation and leakage current, fundamental for steep slope logic switches. As discussed in Chapter 3, these conditions favor the observation of the hysteresis-free NC effect. Section 4.2 describes the fabrication (4.2.1), the PFM measurements (4.2.2), and the Fe-JLFET electrical characterization in DC and with pulses (4.2.3 and 4.2.4). PFM measurements are useful for insight into the microscopic behavior of ferroelectric switching and polarization retention. Whereas pulse measurements are carried out to reduce charge trapping and polarization compensation to have a steeper subthreshold swing in the NC-JLFET. On the contrary, the second targeted application of Fe-JLFET exploits ferroelectric hysteresis. The goal is to build a synaptic device making use of the multi-state memory capability of Si:HfO_2, which is integrated into the JLFET gate. Based on the findings in Chapter 3, to improve polarization compensation and observe a stable hysteresis, the ferroelectric was deposited on top of an inner metal plane, separating it from the gate oxide. Section 4.3 reports the device fabrication (4.3.1), the ferroelectric (4.3.2) and Fe-JLFET (4.3.3) electrical characterization. Then the Fe-FET is tested with different synaptic schemes to emulate the synaptic plasticity (4.3.4), and in addition to the current modulation driven by the ferroelectric, the bottom gate is used to amplify the number of states further.

4.1 Fe-JLFET devices on a UTBB-SOI

The FET structure adopted in this work is a JLFET. It consists of a uniformly doped channel from source to drain. This helps to simplify the fabrication process and to significantly avoid issues related to abrupt doping profiles. Moreover, this also allows a simpler integration (deposition and annealing) of the ferroelectric material into the gate stack.

For the fabrication, we selected a highly doped Si channel to get a sufficiently high current (I_{on}) and low resistance at source and drain contact. However, the doping can not be chosen

arbitrarily high since it reduces the maximum depletion width. If the channel is thicker than the maximum depletion width, the transistor can not be switched off whatever magnitude of the gate voltage. In conclusion, one of the main tasks in the JLFET design is finding the trade-off between doping and Si thickness of the channel to reach the full depletion condition.

For this reason, the platform we chose was an ultra-thin body and buried oxide silicon-on-insulator (UTBB-SOI) from SOITEC. The Si body thicknesses was 15 nm, considering that a couple of nanometers would have been lost during the manufacturing in the cleaning step of the Si. Wafers with thinner bodies would have resulted in a higher contact resistance value at the source and drain terminals. Semiconductor manufacturing companies solved the issue by raising contacts. However, these advanced manufacturing steps were not necessary to prove the working principle of the devices shown in this work, and therefore they were not considered The Buried oxide (BOX) was 20 nm thick, to allow proper bottom gate control on the channel and to use the bulk Si as a bottom gate.

The p-type doping value (N_a) was estimated by calculating the relationship between N_a and the maximum depletion region (x_{dM}) obtained from Poisson's equation, considering the following approximations: full depletion, no free carriers and step doping profile. The approximate value of the doping level was chosen considering that the maximum depletion region (x_{dM}) has to be greater than the Si body (T_{Si}):

$$x_{dM} = \sqrt{\frac{4\varepsilon_S}{qN_a} V_t log(N_a/n_i)} > T_{Si} \tag{4.1}$$

where ε_S is the Si dielectric constant, V_t the thermal voltage, n_i the intrinsic carrier concentration, and q the electron charge. Thanks to the Equation 4.1 and modeling and simulation studies [131] the doping level for 15 nm Si body was estimated to be around $5 \cdot 10^{18}$ cm^{-3}.

To validate the design parameter values, we simulated a JLFET with TCAD, as shown in Figure 4.1, using the parameters in Table 4.1. All simulations show the hole density extracted along the cutline shown in Figure. We chose it since it was the further from the top gate and, therefore, the most difficult to fully deplete.

First, we varied the Si body thickness by keeping the doping fixed ($5 \cdot 10^{18}$ cm^{-3}) and by applying a top gate bias of V_{TG}=0V. We can observe that the TiN top gate work function generates a depletion width of approximately 5 nm. Then we simulated a JFEL with a fixed channel thickness of 10 nm, and we changed the doping level in Si to check the depletion efficiency. We can observe that the higher the doping, the more difficult it is to deplete the channel, which is consistent with equation 4.1. To verify if we could turn off the JLFET just using the top gate, we fixed the Si thickness to 15 nm and the doping density to $5 \cdot 10^{18}$ cm^{-3}), and we simulated at different gate biases V_{TG}. As it is shown in Figure 4.3, using positive voltages, it is possible to reach fully deplete the channel (i.e. the hole concentration falls below $10^9 cm^{-3}$ at 2V).

Parameter	Value
Interfacial SiO2 (nm)	0.6
High-k HfO2 (nm)	5
Gate Length TiN (nm)	25
BOX Layer Thickness (nm)	20
Silicon body doping (cm^{-3})	$5x10^{18}$
Substrate Doping (cm^{-3})	$5x10^{15}$
Drain - source voltage (V)	-0.05
Back gate - source voltage (V)	0

Table 4.1: Fixed parameters for TCAD simulation of JLFET.

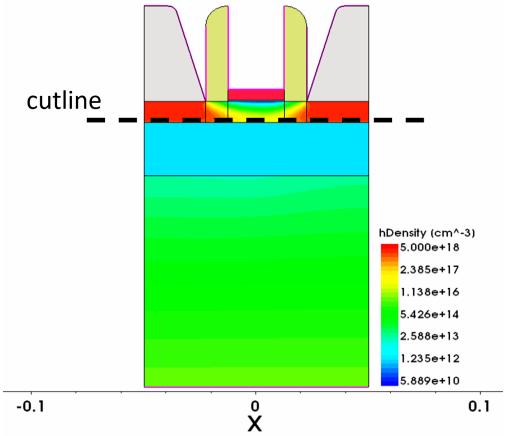
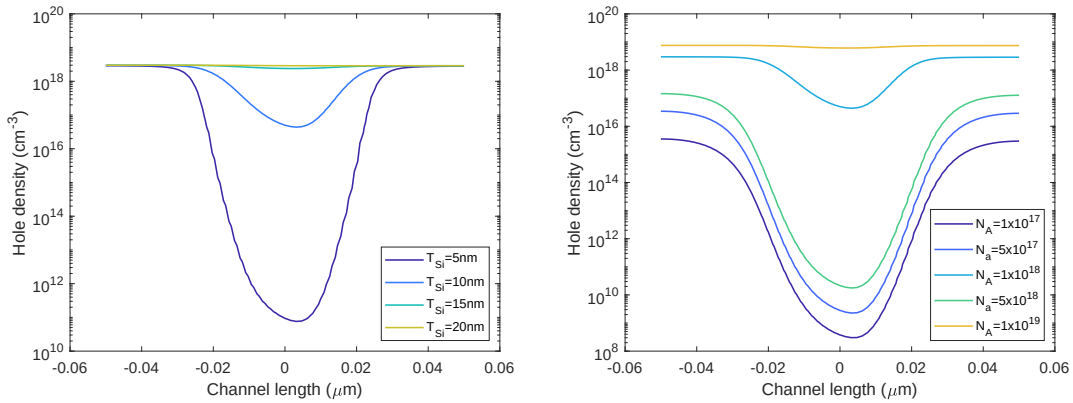
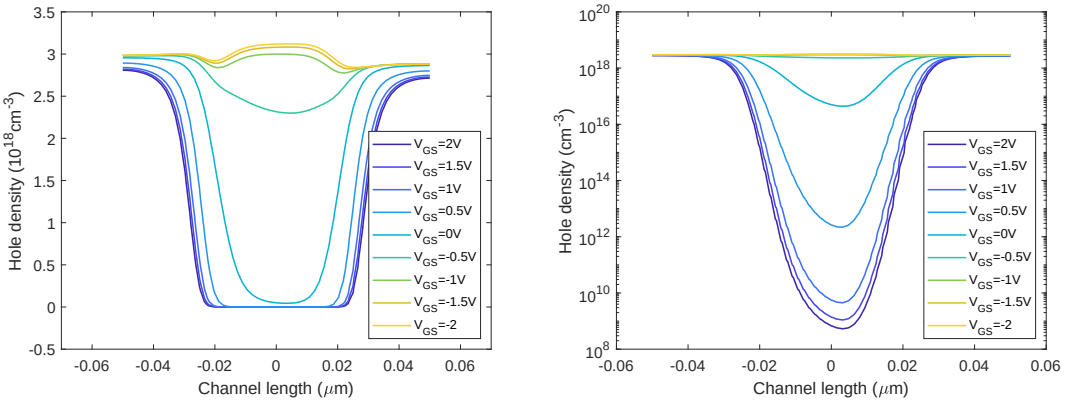


Figure 4.1: Simulated JLFET structure with the cutline in the Si channel with $N_a = 5 \cdot 10^{18}\ cm^{-3}$, T_{Si} = 10nm, V_{TG}=0V, V_{DS}=-0.05V and V_{BG} = 0V.



(a) (b)

Figure 4.2: Hole density at different silicon thicknesses (a) and doping level (b) taken through the cutline in Figure 4.1 with V_{TG}=0V, V_{DS}=-0.05V and V_{BG} = 0V.



(a) (b)

Figure 4.3: Hole density at different V_{TG} with $N_a = 5 \cdot 10^{18}\ cm^{-3}$ and T_{Si} = 10nm in linear (a) and logarithmic scale (b) taken through the cutline in Figure 4.1 with V_{DS}=-0.05V and V_{BG} = 0V.

Once we demonstrated that with a doping density of $5 \cdot 10^{18}\ cm^{-3}$ we could completely deplete the channel of the JLFET, we could proceed with the JLFET fabrication. Wafers were then doped by implantation with phosphorous (P) and boron (B) in the IMEC facility. The wafers with n-type doping present more difficulties in forming ohmic source/drain contact, so further work is required to optimize this step. Consequently, the wafer type employed for JLFET had a 15 nm Si body with p-type doping of $5 \cdot 10^{18}$ cm^{-3}.

By using UTBB-SOI wafers, the JLFETs were fabricated using two different gate stacks, based on the results of Chapter 3. At first in Section 4.2, we analyze the Fe-JLFET with the gate stack composed by SiO_2 in direct contact with Si:HfO_2 (MFIS gate stack). The targeted application is steep-slope logic devices. Based on the findings discussed in Section 3.2 and numerous other studies, MFIS gate structure seems the best suited to observing NC thanks to reduced leakage current, slow down polarization compensation, and reduced charge injection. Subsequently, UTBB-SOI wafers were used in Fe-JLFET with an internal metal between the ferroelectric and the linear insulator, also called MFMIS gate stack. In this case, the targeted application is neuromorphic, the ferroelectric is gradually switched between different states to emulate the synaptic plasticity.

4.2 Fe-JLFET with MFIS gate structure for logic application

In this work, the Fe-JLFET for logic application, also called NC-JLFET, has Si:HfO_2 ferroelectric in direct contact with the SiO_2 linear direct (MFIS), as shown in Figure 4.4. The study performed on the gate stack device (Section 3.2) showed that MFIS gate configuration helps to stabilize the NC. It was possible to extract parameters like Landau coefficients and ferroelectric equivalent negative capacitance from it.

In this section, the fabrication of NC-JLFET is described, and the ferroelectric integrity is confirmed by PFM analysis, which is performed through the gate stack. Then, the DC electrical characterization is carried out to evaluate the performance in DC of the transistor. To conclude, we characterize the NC-JLFET by a pulse measurement technique, which reduces the charge injection and polarization compensation and allows access to the NC regime.

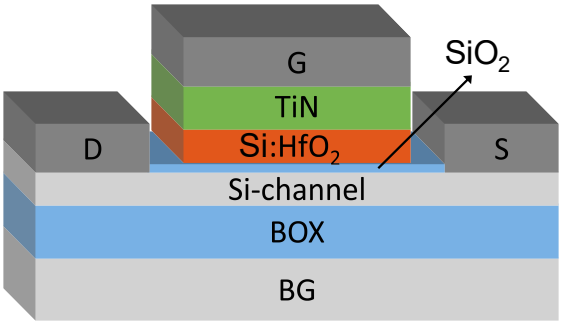


Figure 4.4: Schematic of the Fe-JLFET with MFIS gate stack

4.2.1 MFIS Fe-JLFET fabrication

JLFET capacitor structure was fabricated in CMi facility. The main process steps are visible in Figure 4.6. We started with the etching of the top Si layer by means of deep reactive ion etching (DRIE) to define the channel width (from 700 nm to 20 μm) and the source and drain contacts (80x80 μm^2). Figure 4.5 shows an SEM taken after channel patterning with a thickness of 700 nm.

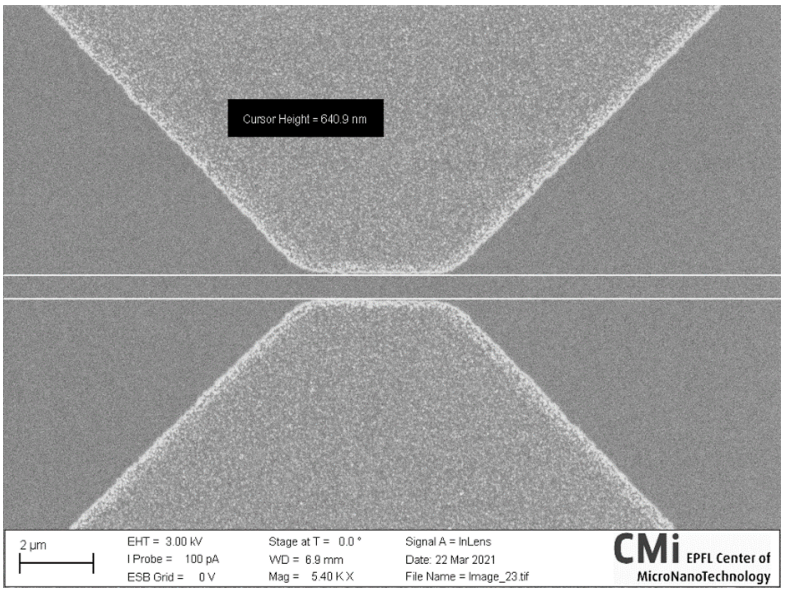


Figure 4.5: SEM taken after channel patterning

Then, the silicon surface was cleaned by a quick RCA cleaning to improve the quality of the interface with the 4 nm SiO_2, deposited by ALD (Figure 4.6(b)). To further improve the Si/SiO_2 interface property, thermal growth is a good alternative, but it presents various drawbacks: the growth would have been difficult to be controlled due to the highly doped thin Si layer, and boron would have diffused into the grown SiO_2, generating traps in the gate oxide. Thant is why ALD is preferable for this solution. These first steps are crucial for the operation of the JLFET because, in the case of a buried oxide over-etch, the current leakage between the top gate and the bottom gate would have spoiled the operation of the device.

Subsequently, as shown in Figure 4.6(c), 12 nm of Si:HfO_2 was deposited by ALD following the recipe described in Section 2.5.2. Then, the Si:HfO_2 film was capped with 10 nm of TiN via sputtering (Figure 4.6(d)). Rapid thermal annealing was performed at 600 °C for 2 min in order to crystallize the Si:HfO_2. Afterward, 20 nm of Pt was deposited as top gate contact, followed by a lift-off (Figure 4.6(e)).

Then, the wet etching of TiN was performed using an NH_4 and H_2O_2-based solution (Figure 4.6(f). After this, the source and drain contacts were opened by SiO_2 wet etching in buffered-HF (Figure 4.6(g)), 30 nm of Pt was deposited and patterned by lift-off (Figure 4.6(h)). This last step is particularly critical since the silicon is only 11 nm thick and, if etched, would not have formed ohmic contacts for source and drain. Furthermore, the choice of the metal is fundamental to obtaining functional JLFET. We tried a double layer of Ti-Pt and Cr-Au, but in the case of $5 \cdot 10^{18}$ p-type silicon, Pt showed to be the best choice. The contact resistance was further decreased by annealing at 350 °C in N_2 which helped smooth down the sputtered Pt. Whereas in the case of n-type silicon, the metal to be chosen is still under study.

Concurrently with UTBB-SOI Fe-JLFET we prepared reference devices, which do not include a ferroelectric layer in the gate, and where all the other processing steps were the same. Comparative analysis of the characteristics of these two devices (Figure 4.7) is essential for the determination of the NC role in the device performance.

The detailed process flow in the form of a run card is displayed in Appendix B; for each step, machines and recipes used in the CMi cleanroom are described.

After the fabrication, the devices were checked using optical microscopy (Figure 4.8) and by AFM for evaluation of their structural integrity. The thickness of the layers and quality of the interfaces were controlled using HR-TEM cross-section and STEM EXD mapping (Figure 4.9). The Si turned out to be 13 nm instead of the 15 nm, which was the starting thickness of the Si in the UTBB-SOI. The thinning down was caused by the RCA cleaning, performed before the gate oxide deposition to improve the quality of the interface.

4.2.2 Electromechanical characterization

The maps of phase and amplitude of the local piezoelectric response and local hysteresis loops in Figure 4.10 were measured by PFM, similarly to what has been done for MFIS gate

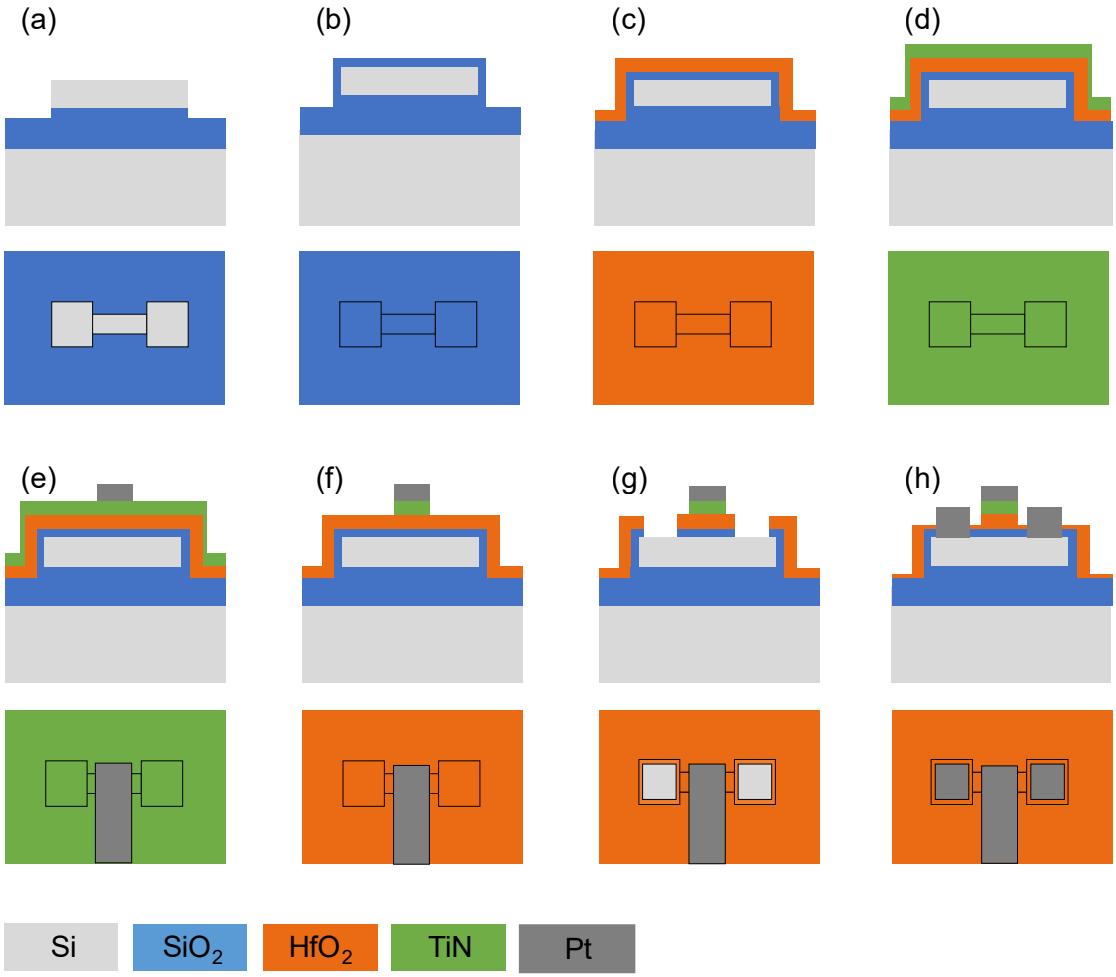
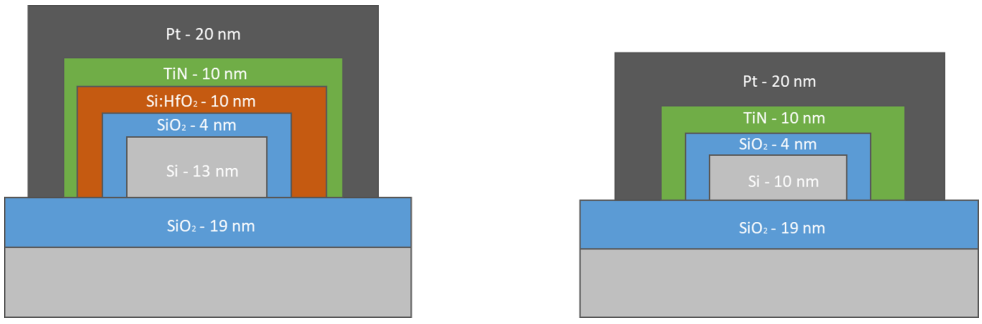


Figure 4.6: Process flow MFIS JLFET



(a) (b)

Figure 4.7: Schematic cross-sections of Fe-JLFET (a) and concurrently fabricated reference JLFET (b).

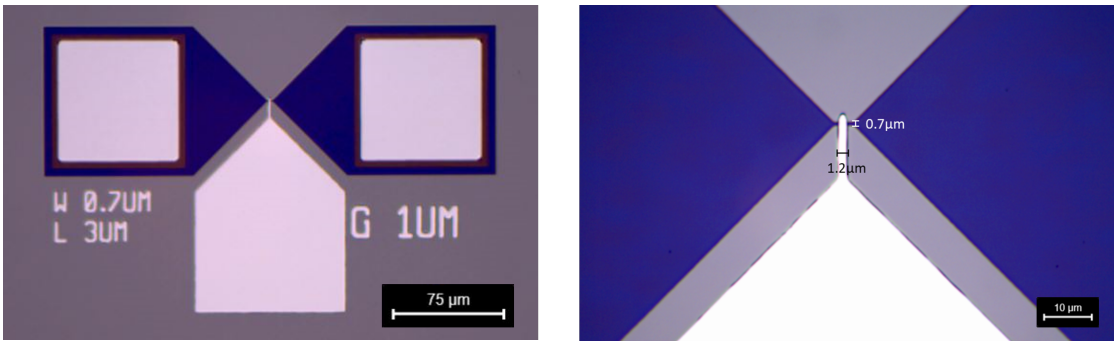
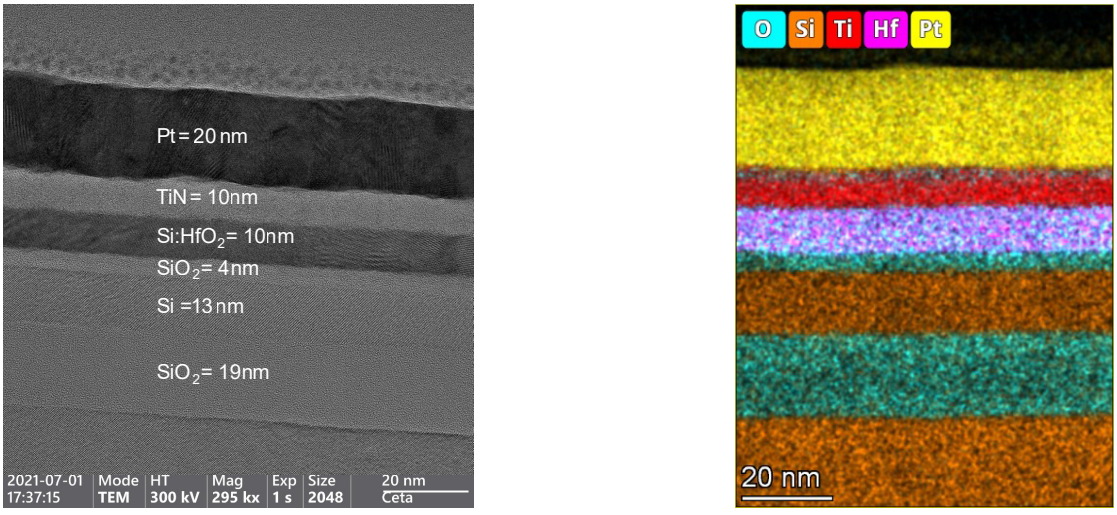


Figure 4.8: Optical images of the device with the gate length of 700nm.



(a) (b)

Figure 4.9: (a) HR-TEM cross-section and (b) STEM EDX elemental mapping of the Fe-FET structure.

stack device in Section 3.2.4. Immediately before the scan, the gate was pre-poled with a single voltage pulse of +8V for 1sec. Then the maps were acquired, and the total duration of the scan was about 60 minutes. The data in Figure 4.10(a),(b) suggest that the polarization state changes during this period. The gradual decrease of amplitude implies the polarization loss presumably due to the depolarizing effects, while the change of the phase shows the preferred (imprinted) polarization direction. According to the amplitude of the piezoresponse, the polarization retention time is less than 20 minutes.

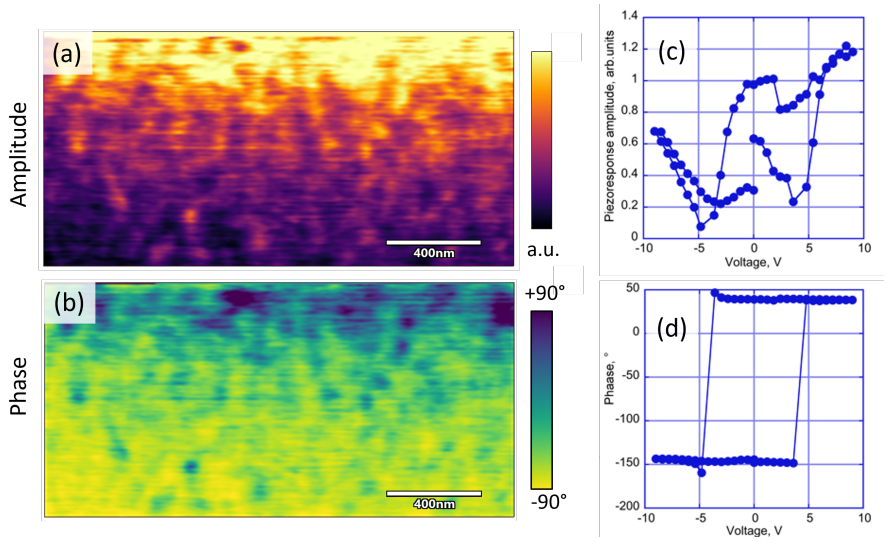


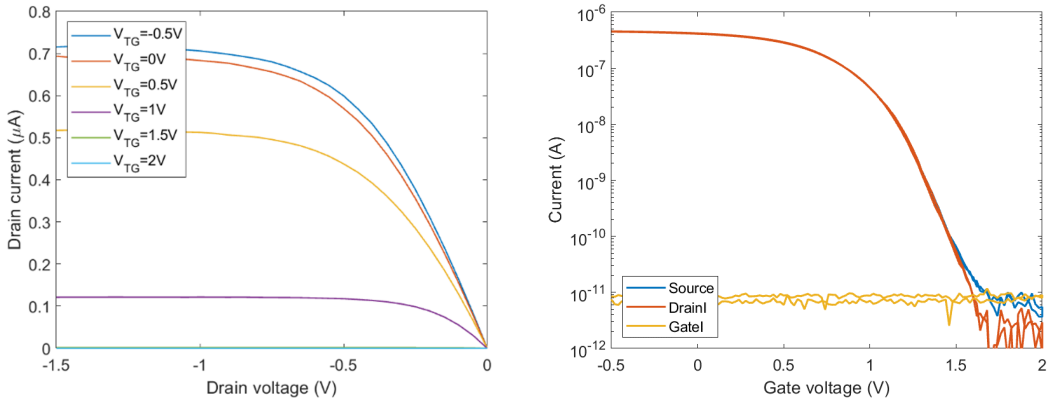
Figure 4.10: PFM maps of amplitude (a) and phase (b) of piezoelectric response measured on the ferroelectric gate through the top electrode. Single point hysteresis of the amplitude (c) and phase (d) of the local piezoelectric response measured in pulse mode (DC OFF) with the pulse/interval duration of 1 second.

Single point loops of the phase and amplitude of the local piezoelectric response, respectively in Figure 4.10 (c) and (d)), show classic hysteresis behavior typical for ferroelectric bilayers [105]. The polarization reversal appears around 4.5 V, which is measured on the ferroelectric/dielectric gate.

In order to estimate the coercive field of the ferroelectric layer, one can use Equation 3.6. Based on the materials characteristics ($d_D = 4nm$, $\varepsilon_D = 4$, $d_F = 12nm$, $\varepsilon_F = 46$) the coercive field of the ferroelectric layer is $V_C = 0.89V$, and the respective coercive voltage is around $E_C = 0.74\ MV/cm$. This value is closer to what was measured in Si:HfO_2 capacitor with a 12 nm ferroelectric layer (Table 2.4). From the PFM data, we conclude that the Si:HfO_2 layer integrated into our UTBB-SOI FET preserved its ferroelectric properties, however, it shows a relatively short retention time. It is worth noting that this short retention concerns the post-poling behavior and does not necessarily impact the device performance in the NC regime, where the as-grown gate imprint conditions play an important role, in helping to observe hysteresis-free NC.

4.2.3 Electrical characterization in DC

The output characteristic ($I_D - V_D$) of the fabbricated UTBB-SOI FET with the gate length of 700 nm is shown in Figure 4.11(a). The JLFET curve is remarkably similar to a regular MOSFET. Close to the origin of $I_D - V_D$, one can notice a linear region sign of ohmic source/drain contact. By modulating the top gate voltage, we can control the current level in the channel, reaching a saturation drain current approaching $1\mu A$ at a bias of $-0.5\ V$.



(a) (b)

Figure 4.11: (a) Output characteristics and (b) transfer characteristics of the produced UTBB-SOI Fe-JLFET with the gate length of 700nm at V_{DS}=-0.2V and V_{BG}=0V.

The actual characteristic, where the NC effect is expected to deliver a performance boost, is the transfer characteristics, representing drain current (I_D) vs. gate voltage (V_G). Figure (4.12)(b) shows the transfer characteristic observed at a drain voltage of $-0.2\ V$. The off-current measured at the drain side is approaching the resolution of the tool, around the 2 pA level. As expected, the off current extracted at the source side (I_S) is higher than the drain one, and it is comparable to the gate current, around 9 pA. The I_{on}/I_{off} ratio, measured at the drain terminal, is approaching 6 decades.

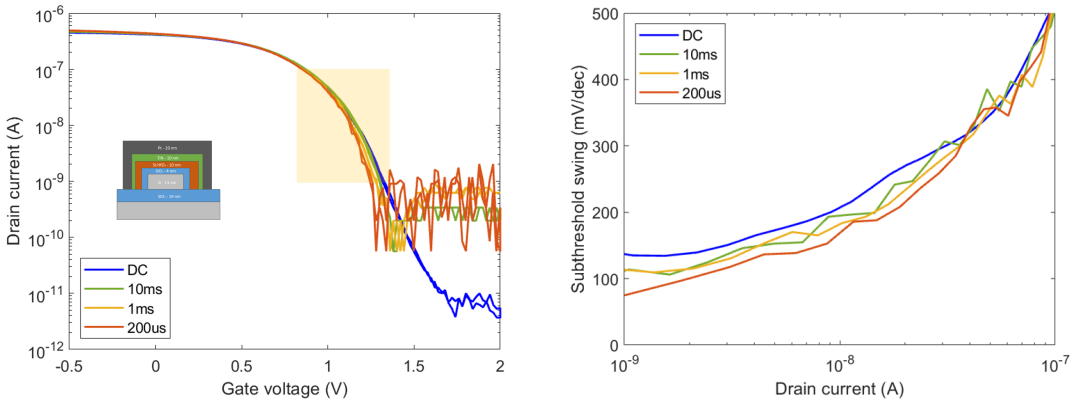
It is worth mentioning that Figures 4.11 (a) and (b) were acquired in DC mode and by grounding the bottom gate ($V_{BG} = 0$), which in this structure is the Si bulk. An additional bottom gate bias can be used for shifting the curve and tuning the I_{on}.

The subthreshold swing in the DC mode (4.12b) is 120 mV/dec measured over 3 decade of current. However, it does not get closer to the ultimate limit of 60 mV/dec imposed by Boltzmann statistics. Therefore, while the fabricated UTBB-SOI Fe-JLFET shows an acceptable performance, no NC-related performance boost was observed for the DC mode. The probable issues responsible for this apparent absence of the NC effect include charge injection in the ferroelectric/dielectric interface, which screens the polarization and suppresses the NC effect.

4.2.4 Pulsed electrical characterization

To overcome the performance limitations due to the charge injection, we tested the same devices in the pulse mode using Keithley 4200a-scs with 4225-RPM remote preamplifiers. To measure the pulced transfer characteristic, the gate was driven with pulses of varying amplitude and fixed duration ranging from 200 μs to 100 ms. The respective pulse mode transfer characteristics in Figure 4.12 show a noticeable improvement of the slope, which approaches $70 mV/dec$ at a drain current 1nA for pulses of $200 \mu s$.

A strong I_{off} noise does not permit correct evaluation of the slope below $1 nA$ in the pulse mode. This is caused by the set-up and can be reduced if measuring at a lower current range. However, that prevents the measurement of the I_{on}, which saturates above the system measurement limit.

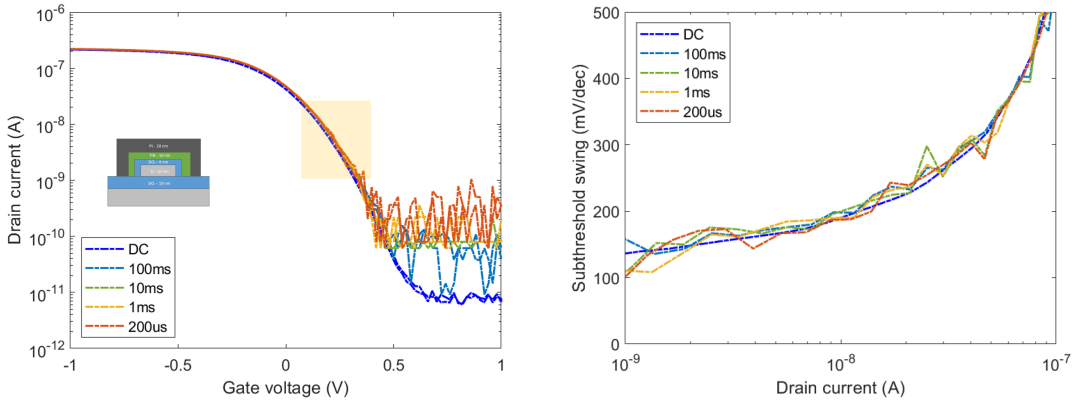


(a) (b)

Figure 4.12: Transfer characteristics of the Fe-JLFET with the gate length of 700 nm at V_{SD}=-0.2V measured in the dc and pulse modes (a), and respective subthreshold slopes measured in mV/dec (b).)

It is worth mentioning that the subthreshold swing slope was calculated using a conservative approach to avoid overestimation of the slope steepness due to the noise-related artifacts. For an accurate and reliable slope evaluation, we used only the drain current higher than $1 nA$, and we performed smoothing with quadratic regression over 10 points, such as on $200 mV$. The resulting slope estimation does not reach the Boltzmann limit of $60 mV/dec$, but it approaches it closely ($70 mV/dec$) in the pulse mode. Overall the NC-JLFET presented a hysteresis-free transfer characteristic and an improved subthreshold swing of 35% (over 1.3 decades of drain current) with 200 μs pulse gate voltages compared to DC. It is worth noting that the effect was reproducible, and no special pre-poling or other conditioning was required for the ferroelectric gate to reach this enhancement.

The improvement of the slope in the pulse mode compared to the DC mode is a remarkable result, which suggests the role of the NC effect in agreement with the earlier reports on



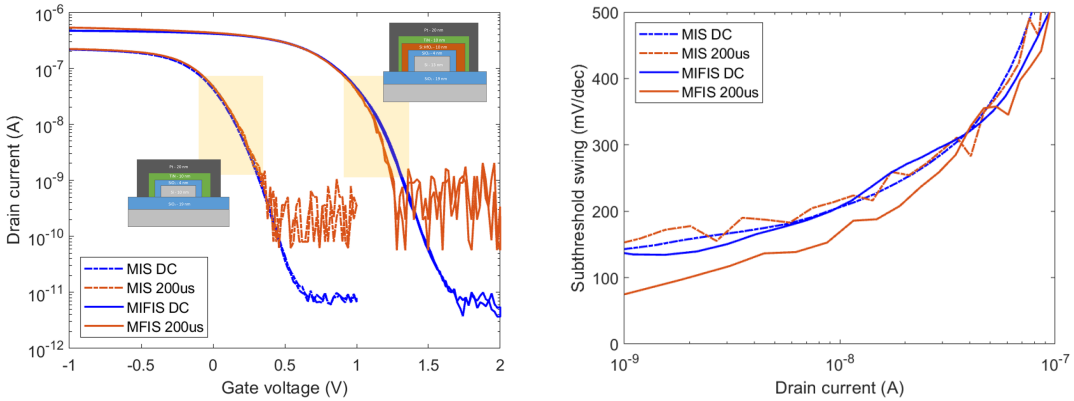
(a) (b)

Figure 4.13: Transfer characteristics of the reference FET with the gate length of 700 nm with V_{SD}=-0.2V measured in the dc and pulse modes (a), and respective subthreshold slopes measured in mV/dec (b).

ferroelectric/dielectric bilayers studies in Chapter 3. To verify that the SS improvement comes from the ferroelectric, the same pulsed study was performed on UTBB-SOI JLFET without ferroelectric. Figure 4.13 shows the transfer characteristic with no improvement given by the pulses. The only difference in this characteristic is the lower I_{on} caused by a thinner Si channel, as visible in Figure 4.7.

Comparison between the transfer characteristics of the UTBB-SOI Fe-JLFET and concurrently fabricated reference UTBB-SOI JLFET (Figure 4.14) further supports the role of the NC effect. In the DC mode, both types of FETs show similar I_{on}/I_{off} ratio and subthreshold slopes. In the pulse mode, the situation is different: the reference FET does not change the subthreshold slope while the Fe-JLFET shows a steeper characteristic. The difference between the DC and pulse mode, which is not seen in the reference JLFET, while clearly observed in Fe-JLFET, is valuable evidence suggesting that the NC effect does play a role in the enhanced transfer characteristics of the studied Fe-JLFET. Overall the fabricated hysteresis-free NC-JLFET showed an enhanced SS with pulses, with a maximum improvement of 35% (over 1.3 decades of drain current) compared to DC condition.

The presented NC-JLFET is, to our knowledge, the first fabrication of a ferroelectric device of this type. PFM investigation of the local piezoelectric response indicated that the ferroelectric gate was successfully integrated. It revealed a short retention period of the ferroelectric gate, which is favourable for operation in the NC mode. It was prooven that the given NC-FET outperforms traditional JLFET without a ferroelectric gate in pulse measurement mode, which supports the role of the NC effect in Fe-JLFETs.



(a) (b)

Figure 4.14: Comparison between the transfer characteristics of Fe-JLFET and reference FET (a) and respective subthreshold slopes (b).

4.3 Fe-JLFET with MFMIS gate structure exploiting gradual switching

Neuromorphic computing, inspired by the low-power operation of the human brain, is a promising emerging field since it can achieve more energy-efficient computing than von Neumann architecture for ultra-low power applications [32]. In bioinspired architecture, synaptic devices are one of the main computing elements: their function is to interconnect massive arrays of neurons (Figure 4.15 (a)). Low power consumption, scalability and multistate capabilities represent critical requirements. In this section, we proposed a tunable Fe-JLFET composed of an MFMIS gate stack for neuromorphic application. The fabricated device emulates a fully tunable synaptic device thanks to the non-volatility characteristic of the Si:HfO_2 ferroelectric. As shown in Figure 4.15 (b), such a synapse exploits the back gate for efficient tuning of the synaptic weight.

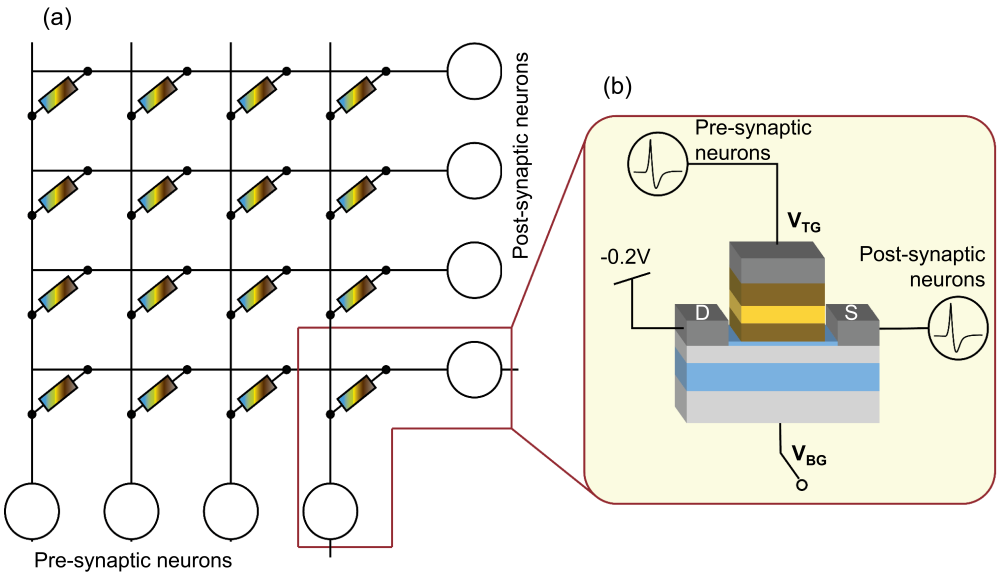


Figure 4.15: (a) Schematic of a neural crossbar architecture with Fe-JLFET synapses (b) Schematic of the synaptic Fe-JL-FET with an addition of a terminal for efficient tuning of the synaptic weight.

4.3.1 Fe-JLFET fabrication

The fabrication of the Fe-JLFET with an MFMIS structure is similar to Fe-JLFET with MFIS, but two extra lithography masks were needed to deposit and contact the inner gate. The Fe-JLFET is fabricated starting from a UTBB-SOI wafer with 15 nm top Si-doped p–type $5x10^8\ cm^{-3}$. The schematic in Figure 4.16 illustrates the main process steps. The detailed process flow in the form of a run card is displayed in Appendix C, including the description of machines and the recipes used in the CMi cleanroom.

At first, the silicon channel was etched by a reactive ion etching technique (Figure 4.16 (a)), then the 4 nm of SiO_2 was deposited by ALD as a linear gate oxide (Figure 4.16 (b)). Afterward, a layer of 12 nm of sputtered TiN was deposited(Figure 4.16 (c)), serving as IG. Then by lift-off, a Pt layer was deposited and patterned on TiN (Figure 4.16 (d)), acting as a metal contact for the IG. On top, 12nm Si:HfO_2 was deposited by ALD (Figure 4.16 (e)), following the recipe described in Section 2.5.2. Subsequently 6nm of TiN were sputtered (Figure 4.16 (f)) and, to reach robust ferroelectricity, 2 min annealing at 600 °C was performed in N_2 environment.

A 30 nm of sputtered Pt was deposited as a top metal gate (Figure 4.16 (g)). Subsequently, IBE was used to pattern the TG and all the top TiN and Si:HfO_2 layers were etched (Figure 4.16 (h)). As shown in Figure 4.16 (i), to get the electrical contact between the TiN in the gate structure and its external metal pad, a lithography step followed by a TiN wet etching (based on H_2O_2 and NH_4OH) was performed. Lastly, source and drain contacts have been opened by HF 1% etching (Figure 4.16 (j)) and on top, sputtered Pt lift-off was performed (Figure 4.16 (k)). To

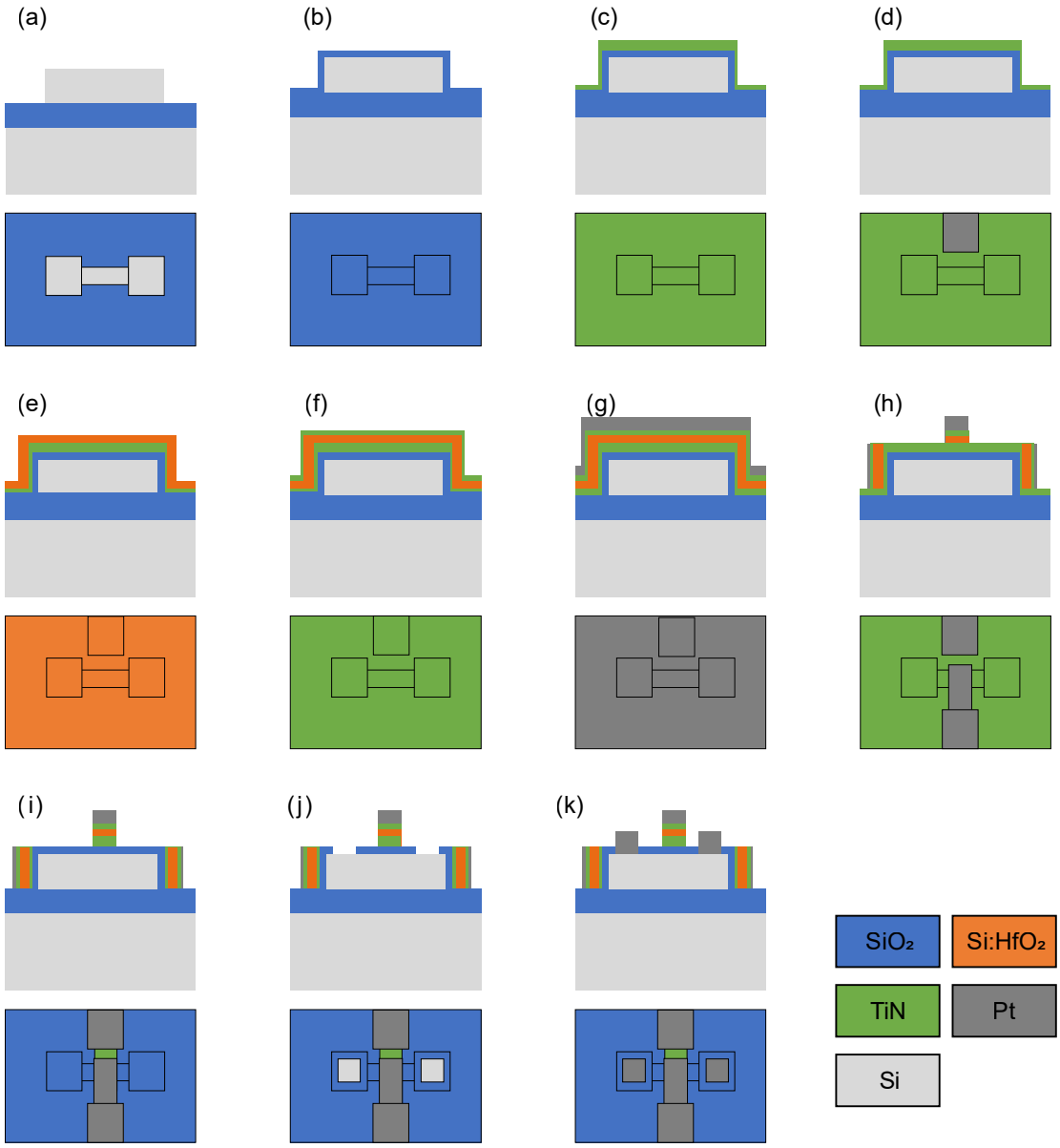


Figure 4.16: Schematic showing the top view and the cross-section of Fe-JLFET with MFMIS gate stack during the fabrication from (a) to (k)

improve the contact of source and drain, annealing at 350 °C was performed in N_2.

Figure 4.17 shows the cross-sectional TEM image, which reveals excellent uniformity of the gate stack layers, and Figure 4.18 an EDX map of the fabricated FET, which indicates the chemical characterization of the gate stack. Also, in this case, we can observe a thinner Si: 11.5 nm instead of 15 nm, mainly caused by the Si cleaning before ALD deposition. The devices characterized and studied in this work have a footprint of around 1.2 μm^2 (with 1.2 μm channel width and 1 μm length).

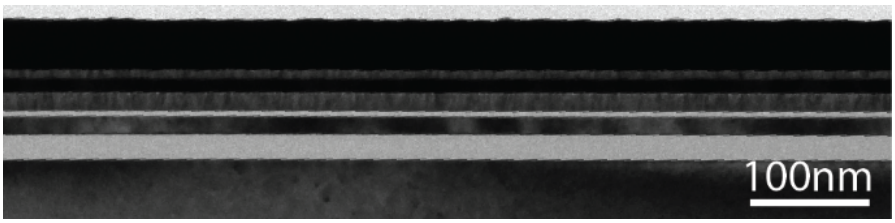


Figure 4.17: Cross-sectional TEM image of a Fe-JLFET

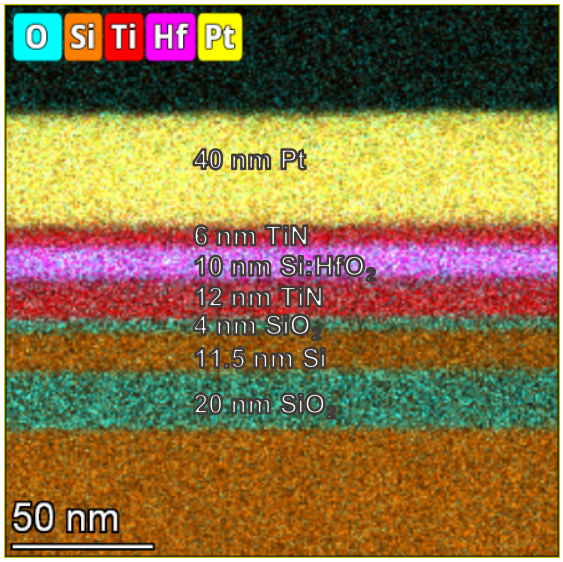
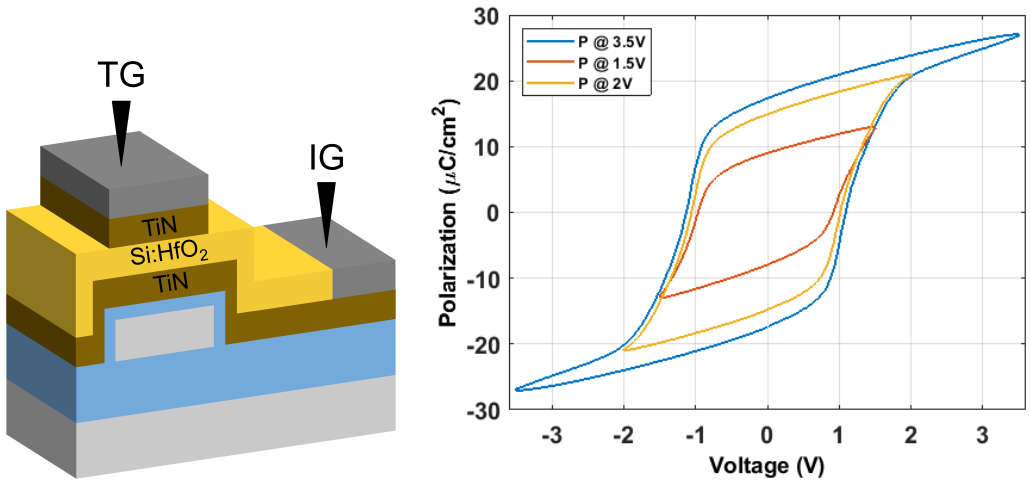


Figure 4.18: Cross-sectional EDX map with the different thin film thicknesses of the gate stack.

4.3.2 Integrated ferroelectric gradual Switching Transistor and its implications on Fe-JLFET functionality

The design and implementation of an internal gate contact allow not only the access to the full device (Fe-JLFET) characterization, but also to the investigation of the non-ferroelectric FET (JLFET), as well as the possibility of studying ferroelectricity effects. Thanks to this, we were able to verify the functionality of the integrated ferroelectric and compare JLFET and Fe-JLFET.

In Figure 4.19 the P-V hysteresis loop, taken between IG and TG, demonstrates that the Si:HfO_2 is switchable between the two fully poled states and that we can obtain multi-states configuration by changing the polarization domain population while tuning the maximum applied voltage.



(a) (b)

Figure 4.19: (a) Fe-JLFET schematic of the device highlighting the contacts for the ferroelectric testing (TG and IG) and (b) P-V hysteresis loops at different maximum bias taken between the TG and the IG

This was demonstrated at the nanometer level by off-resonance PFM in Figure 4.20 (a), which shows multi-domain structure of Si:HfO_2 in the mixed state phase map and fully polarized states in the other maps.

Starting from a positive state (pointing down polarization) and applying negative voltage pulses, the multi-domain ferroelectric gradually switches to the negative state (pointing up polarization), causing a reduction Si depletion region and an increase in the drain current, as illustrated in the qualitative schematic of Figure 4.20 (b). In turn, the Fe-FET transfer characteristic curve shifts to the right, as in the schematic of Figure 4.20 (c).

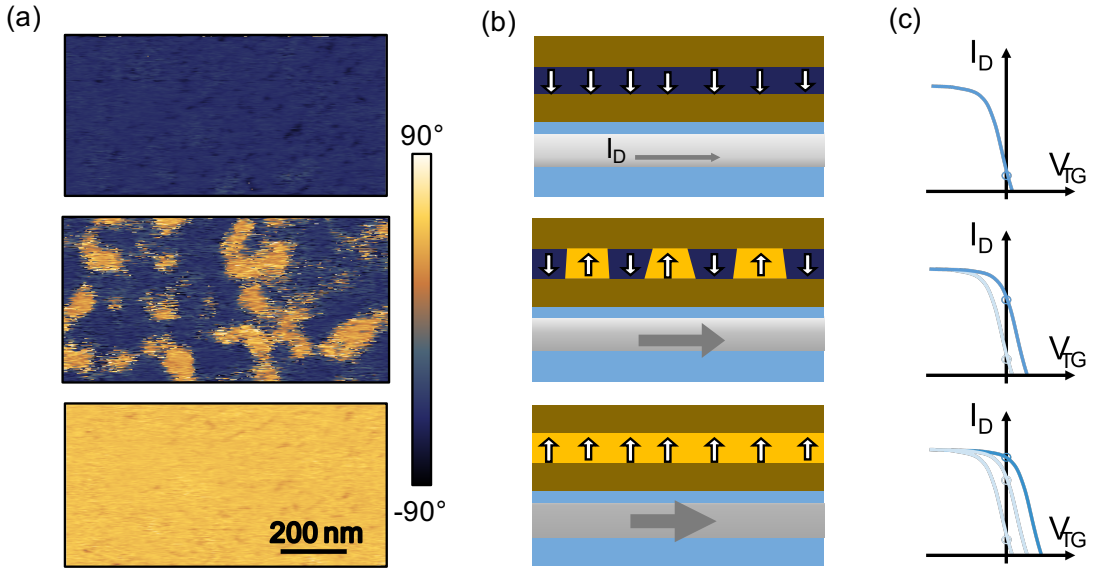


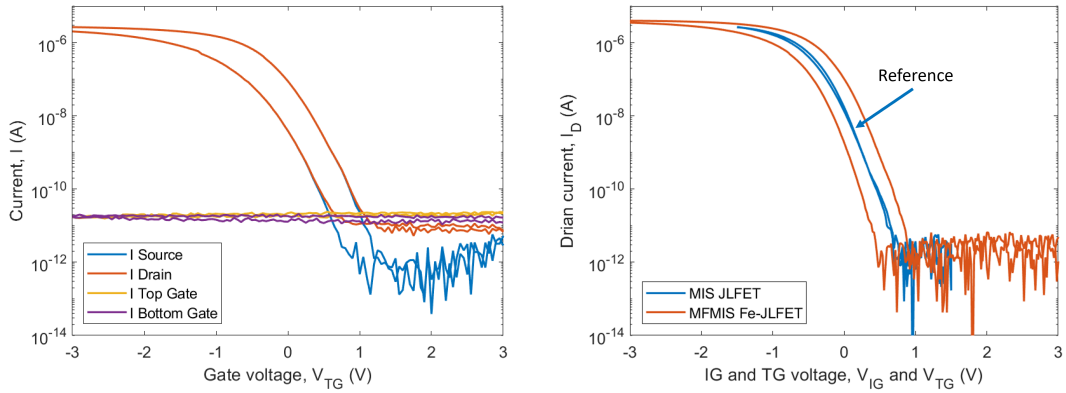
Figure 4.20: (a) Phase PFM maps of domain switching in Si:HfO_2 (positive, mixed and negative state) taken between the TG and the IG. (b) Qualitative schematic with focus on the relationship between ferroelectric and Si channel. (c) Schematic of the current change in the $I_D - V_{TG}$.

4.3.3 Electrical characterization

The Fe-JLFET is characterized by measuring the drain current controlled by the top gate voltage in DC, while having the bottom gate grounded and V_{DS}=-0.2. Figure 4.21 (a) shows has a I_{on}/I_{off} of more than six orders of magnitude with a low top and bottom gate leakage current (around $2pA$). The curve strongly resembles the Fe-JLFET with MFIS gate stack. The major difference is that in Fe-JLFET with MFMIS gate stack, the polarization can be switched permanently, and therefore, the threshold voltage can be shifted. The direction of switching is clockwise, which is in line with polarization switching in the gate stack, as discussed above in Section 4.3.2. Once the Fe-JLFET with MFMIS gate stack was characterized, the non-ferroelectric JLFET (the JLFET with MIS gate stack) was measured. Figure 4.21 (b) compares the two devices and, as expected, the device without the ferroelectric layer does not show any sign of hysteresis.

It is worth mentioning that the hysteresis is lower than what is predicted from Si:HfO_2 capacitor. In the ideal case of a full ferroelectric switch, the maximum hysteresis expected in a FET is equal to two times the coercive voltage, which is almost 1.7V in our case. On the contrary, in Figure 4.21 the hysteresis reaches just 0.5V. This can be explained by two concurrent reasons. We believe that the polarization is not well saturated in Figure 4.21. Indeed if a higher programming bias (around 5V) is applied, an hysteresis of 1V can be reached. However, when operating at these voltages, the transfer characteristic shows degradation, such as SS increase. This is probably provoked by charge injection caused by leakage current. The other reason is that the SiO_2 is thicker than what is usually used for memories, this can cause a higher

depolarization field and lower $I_D - V_{TG}$ hysteresis.



(a) (b)

Figure 4.21: (a) Transfer characteristics controlled by the top gate of the Fe-JLFET with 1.2 μm channel width and 1 μm length. (b) Comparison between the Fe-JLFET (with MFMIS gate) and JLFET (with MIS gate) transfer characteristics.

In view of the fact that our synapse is implemented as JLFET with a TG ferroelectric stack and a BG liner dielectric, hence it is crucial to validate and distinguish the control of the ferroelectric hysteresis in the transfer characteristics by the TG and the BG. Figure 4.22 shows the experimental $I_D - V_{TG}$ characteristic of the Fe-JLFET in the two ferroelectric states controlled by the top gate for different voltages applied on the bottom gate. As one can notice, the BG offers unique tuning of the hysteretic threshold voltages through electrostatic coupling. This offers the possibility to shift the transfer characteristic while keeping the hysteresis constant.

In such non-volatile operation of Fe-JLFET, we observe a hysteresis of 0.5V, which appear to be quasi-independent of the V_{BG} for this range of voltages (inset of Figure 4.22).

In Figure 4.23 we report the BG transfer characteristics tuned by TG. No relevant hysteresis is observed, but just a shift in the threshold voltage caused by TG voltage modulation and the corresponding electrostatic coupling.

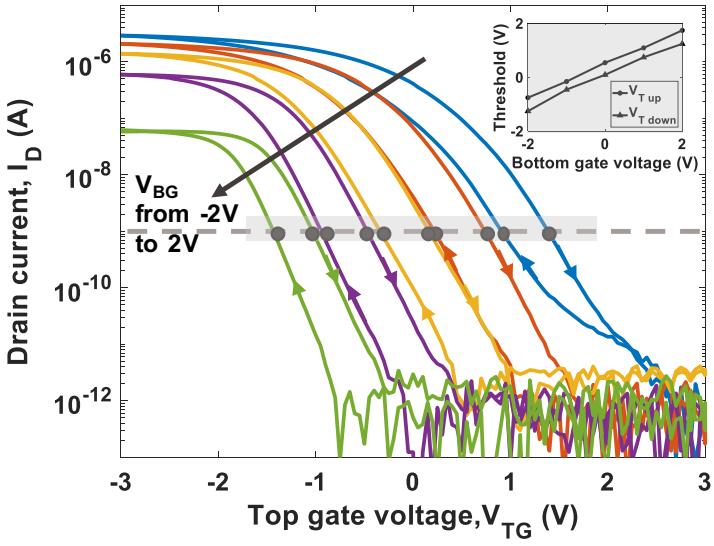


Figure 4.22: Fe-JLFET transfer characteristics by sweeping the TG of the in the two ferroelectric states with BG bias, from -2V to 2V.

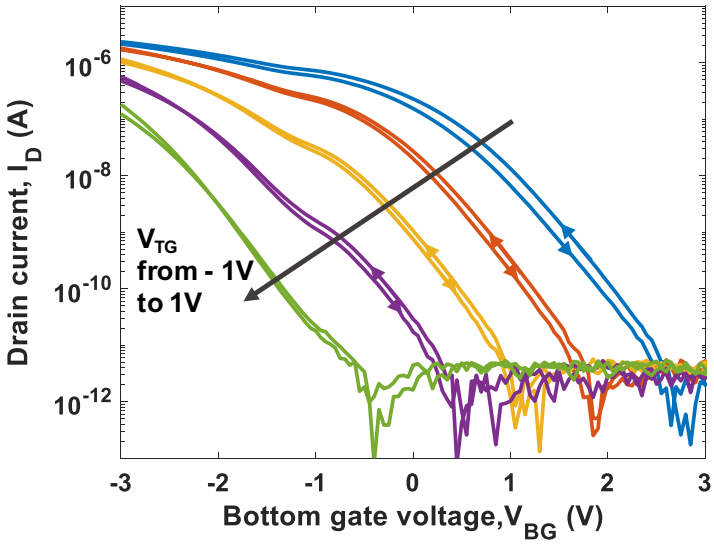


Figure 4.23: Fe-JLFET transfer characteristics by sweeping the BG at different TG bias, from -1V to 1V.

4.3.4 Ferroelectric JL-FET as tripartite synapse

Neuromorphic computing forms a new paradigm of computation, inspired by the human brain's analog operation. Such bioinspired architectures are generally composed of dual terminal synaptic devices, which flexibly and adaptively connect massive arrays of neurons, thanks to the so-called synaptic plasticity. However, it is acknowledged that three-terminal (3-T) synaptic devices would better mimic the biological tripartite synapses, which are composed by pre-synaptic terminal, post-synaptic terminal, and the astrocytes process (Figure 4.24 (a)). This last brain cell does not fire an action potential but surrounds synapses, and it was recently discovered to play an active role in brain function, and information processing [132, 133]. A very small number of works proposed the implementation of such tripartite artificial synapses, the majority of publications dealing with bipartite synaptic devices.

Ferroelectric Si:HfO_2 represents an excellent candidate to mimic the synaptic plasticity due to its CMOS compatibility, high scalability, low power switching, and especially multi-state capabilities [134]. The solution proposed here is to use the fabricated Fe-JLFET on UTBB SOI substrate to emulate a tripartite synaptic device thanks to the presence of the BG, which behaves as artificial neuromodulation emulating the function astrocytes. As shown in Figure 4.24 (b), in such a 3-T artificial synapse, the synaptic weight is stored in the ferroelectric, the pulses are applied at the TG (pre-synaptic neuron), and the output is read at the source terminal (post-synaptic neuron).

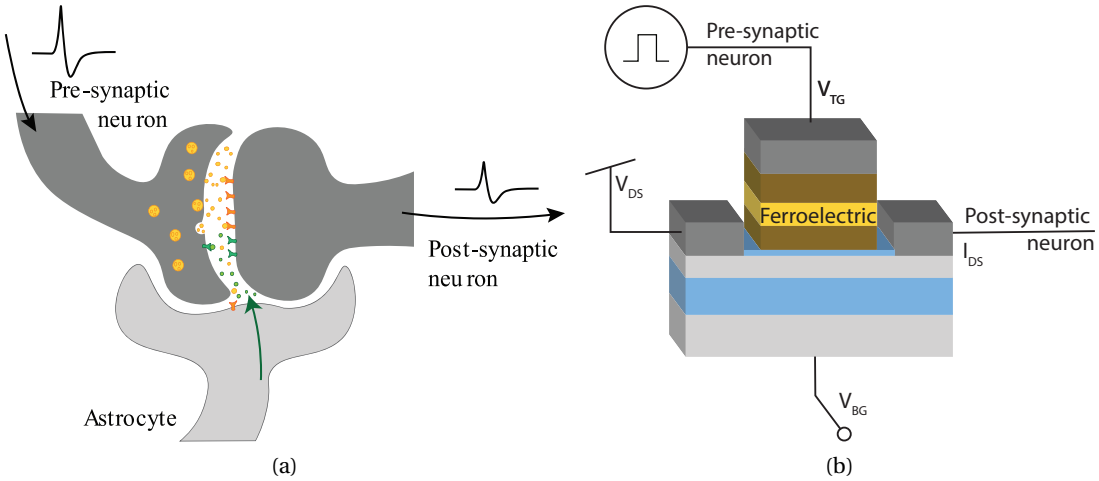


Figure 4.24: (a) Schematic of biological tripartite synapses composed of pre-synaptic and post-synaptic terminals and astrocyte process behaving as a neuromodulator. (b) Synaptic Fe-JL-FET schematic with the input on the gate terminal, the output on the source and a tuning terminal on the bottom gate.

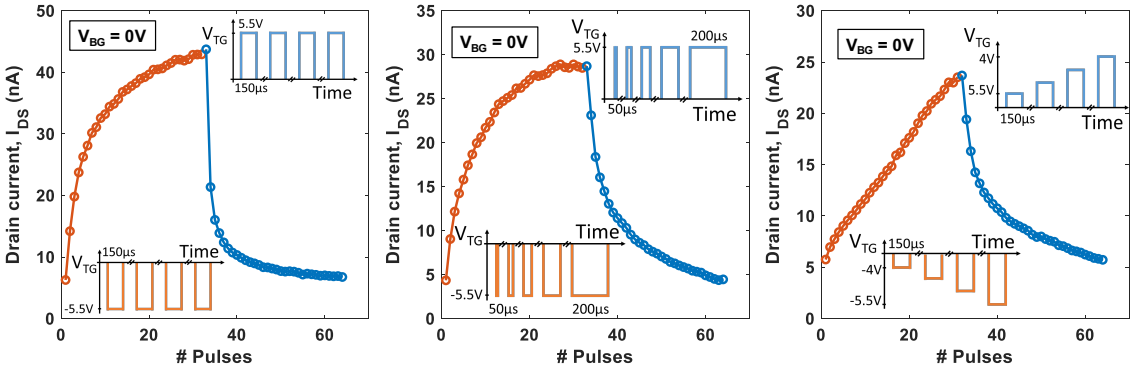
To mimic the continuous synaptic plasticity, we gradually switched the polarization of the ferroelectric, which corresponds to a gradual change in the channel conductivity. In this work, this was enabled by applying rectangular pulses using a Keithley 4200A-SCS PMU with

RPM units to the TG with three different synaptic schemes: pulse train, amplitude, and width modulation. Using the pulse train scheme, we verified the tuning given by the neuromodulator terminal, the BG, and then we proved the robustness and the cycling.

Fe-JL-FET device with different synaptic schemes

In the first scheme (Figure 4.25a), a train of pulses with a width of 150 μs and amplitude of +5.5 V and -5.5 V is applied to mimic potentiation and depression, respectively. The drain current was measured after each pulse at $V_{TG} = 0V$, $V_{DS} = -0.2V$ and $V_{BG} = 0V$. This resulted in gradual drain current (I_D) tuning from a minimum of I_{Dm} to a maximum of I_{DM}, with a ratio of I_{DM}/I_{Dm}=8.

The second scheme (Figure 4.25b) modulates the pulse width, from 50 to 200 μs, which results in potentiation and depression curve with I_{DM}/I_{Dm}= 7. The third scheme consists of the modulation of the amplitude pulse from 4V to 5.5V, as shown in Figure 4.25c. The curve has a smaller I_{DM}/I_{Dm} ratio (=5) than the other two schemes but more equidistant current levels.



(a) (b) (c)

Figure 4.25: Potentiation (orange) and depression (blue) curves using the top gate with V_{BG} = $0V$ with the synaptic pulse scheme shown in the inset: pulse train (a), pulse width modulation (b) and amplitude modulation (c).

BG tunability, robustness, and cycling with pulse train synaptic scheme

The same pulse scheme of Figure 4.25a, which showed the highest I_{DM}/I_{Dm}, was explored for various BG voltages. The BG terminal mimics the functioning of the astrocytes in tripartite synapses: they are able to affect the synaptic weight variation to adapt to different situations. With our artificial synaptic device, the current gets suppressed by applying negative BG voltage, on the contrary, if it is positive, it gets potentiated, as shown in Fig. 4.26 (a). Thanks to BG control, we can affect the current level while keeping I_{DM}/I_{Dm} constant for each set of the potentiation-depression curve, as observed in Fig. 4.22 the ferroelectric hysteresis is independent of the V_{BG} between $-1V$ to $1V$. In total, it is possible to tune the synapse drain

current by more than 400x, from 0.6 to 240nA, and select the desired power working range of the device. The potentiation-depression curves have non-overlapping states, consequently using this strategy, it is possible to quasi-triplicate the number of states.

To test the robustness of the proposed artificial tripartite synaptic device, the same synaptic scheme was repeated at different increasing temperatures, as shown in Figure 4.26b. Remarkably, the potentiation/depression curve shows no sign of degradation up to 85°C, presumably due to a coherent and stable switching of the ferroelectric gate and its excellent control by the junctionless transistor operation.

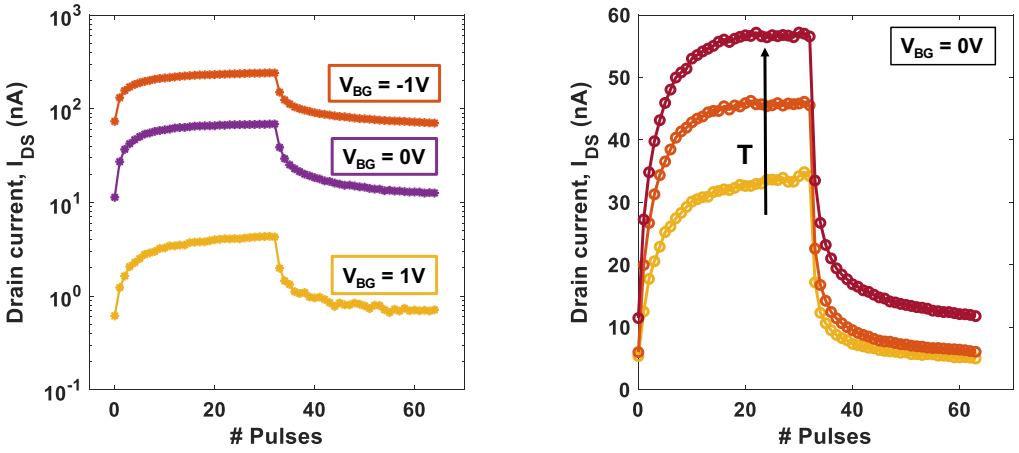


Figure 4.26: (a) Potentiation and depression curve with same condition of Figure 4.25a excellently preserved at different temperatures (85°C, 55° and 20°). (b) Tuning of the potentiation and depression with same TG condition of Figure 4.25a and by also applying voltage on back gate

Additionally, in Figure 4.27 we show a continuous modulation of the conductance between the two extreme states. The cycling was achieved over 2000 consecutive potentiation and depression curves, for up to 128k pulses. The cycling test shows an initial opening attributable to the ferroelectric waking-up and then a gradual degradation of the performance (I_{DM}) but not of the full functionality, possibly caused by polarization fatigue. Therefore, we demonstrated that the proposed 3-T Fe-JLFET synapse device operates up to 2000 cycles with an I_{DM}/I_{Dm} of 4, in significant progress compared to previous reports with the same technology [135].

In conclusion, we demonstrated a CMOS-compatible double-gate Fe-JLFET operating as a novel energy-efficient 3-T synapse with the unique possibility to highly tune the synaptic weight by the back gate, similarly to the astrocyte process in neuromodulation. The ferroelectric functionality of the integrated Si:HfO_2 was firstly verified electrically and then electromechanically by means of PFM. Then synaptic behavior was experimentally proven with different synaptic schemes: amplitude modulation, pulse width modulation and pulse train. Furthermore, we validated the robustness up to 85°C and synaptic plasticity until 2000

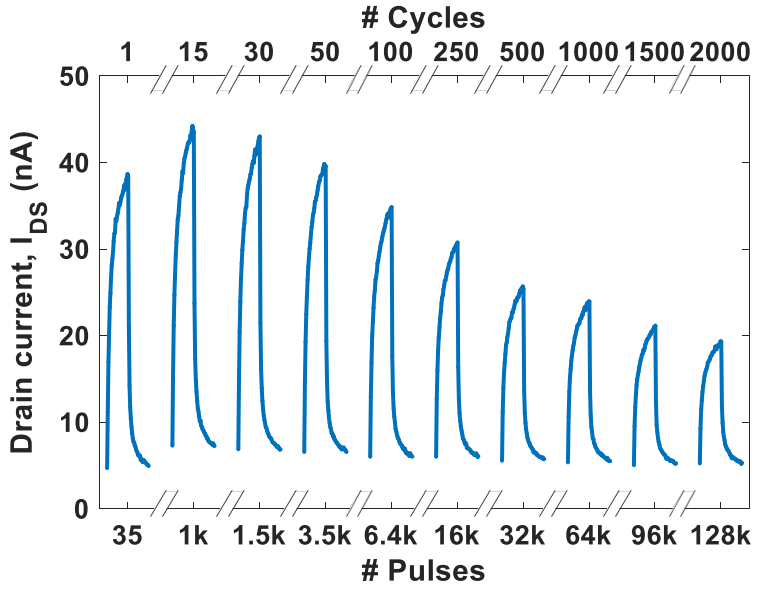


Figure 4.27: Cycling for 2000 cycles, such as 128k, with the same condition of Figure 4.25a, demonstrating the robustness of Fe-JLFET for tunable synapses.

cycles in great advance of previous reports.

4.4 Summary

This chapter reported some of the first ever investigated ferroelectric junctionless devices, a p-type Fe-JLFET fabricated using a UTBB SOI, in which a 10 nm thick Si:HfO2 ferroelectric is integrated into the gate stack. The devices showed a remarkable electrical characteristic with almost six orders of magnitude I_{ON}/I_{OFF} and a I_{OFF} around few pA. The Fe-JLFETs were fabricated with the ferroelectric gate stacks presented in Chapter 3, targeting two main applications: (i) NC steep slope switches with steep SS and no hysteresis, and (ii) neuromorphic devices, where the ferroelectric is gradually switched to mimic the synaptic plasticity.

For steep-slope logic devices, the Fe-JLFET was designed using an MFIS gate stack, which reduces the leakage current and charge compensation. The ferroelectric was successfully integrated, as confirmed by PFM analysis of the local piezoelectric response. Then the NC performance enhancement was observed in the pulse mode with an SS improvement of 35% (over 1.3 decades of drain current) compared to DC. The same technique was applied to JLFET without ferroelectric, showing no SS improvement with pulses, which further supports the role of the NC effect in Fe-JLFETs.

Alternatively, similar UTBB-SOI wafers were used to fabricate Fe-JLFET with an MFMIS gate stack to target neuromorphic applications. Thanks to the presence of the internal gate, it was possible to verify the functionality of the ferroelectric alone and the JLFET without it. The

proposed neuromorphic device consisted of double-gate Fe-JLFET acting as a three-terminal synapse, capable of emulating the functionality of biological tripartite synapses. The back-gate voltage was used to tune the synaptic weight by more than a record factor of 400x. Compared to other implementations of ferroelectric synapses with the same technology, the proposed 3-terminal Fe-JLFET synapse device showed high robustness to temperature until 85 °C and preserved the synaptic plasticity until 2000 cycles of operation, which makes it promising for CMOS-compatible energy-efficient implementation of future neuromorphic ICs.

5 Conclusion and future work

5.1 Summary of Research Topics

This Ph.D. dissertation focused on the investigation of the NC effect and its interaction with the polarization switching dynamics in Si:HfO_2. The work started with the fabrication optimization of the ferroelectric, which was integrated into two different gate stacks devices, one with an internal gate (MFMIS) and one without it (MFIS). Both gate stacks were used in Fe-FET using JL technology, and a comparative assessment of the performance was carried out.

The devices without internal gates showed low leakage current and one preferred state of polarization, hence no hysteresis. We demonstrated that these characteristics contribute to the observation of the NC regime in the gate stack and in the NC-JLFET. In the MFIS gate stack device, we observed the S-shaped P-E_f curve predicted by LGD formalism, and in the JLFET, a steepening of the slope with pulsed measurement.On the other hand, devices with an internal gates structure have symmetric electrodes sandwiching the Si:HfO_2, and as a consequence, there is no imprinted state and polarization compensation is faster. We verified that these conditions are favorable to observe a hysteretic memory behavior by characterizing the Fe-JLFET with MFMIS for neuromorphic application.

The device development was supported by two studies on the polarization switching mechanism, given its high application relevance in NC switches and neuromorphic circuits. The first study in a Si:HfO_2 capacitor revealed that the switching behavior in temperature of Si:HfO_2 follows intrinsic switching, from which it was possible to extract the Curie temperature. The second work was performed in a heterostructure (MIFM) with HZO ferroelectric, in which its coercive field value was studied with different techniques, reviling consistency with intrinsic switching but not with nucleation-based switching mechanism.

Overall, this Ph.D. work verified the feasibility of Fe-JLFETs for both neuromorphic synapses and NC logic devices, as well as studies the role of the internal gate on the ferroelectric properties and switching mechanism.

5.2 Main Achievements

The main contributions to the ferroelectric and electronic field can be summarized as follows:

Application-targeted Si:HfO_2 fabrication optimization

We improved our Si:HfO_2 ferroelectric fabrication to get the optimal recipe for the integration into logic and memory devices. Different Si:HfO_2 thicknesses were considered, 14.5 nm, 10 nm, and 8.5 nm. By means of ANOVA statistical analysis, we examined the effect of cycling (from 10 to 1000), annealing time (from 20 s to 120 s), and temperature (from 600 °C to 800 °C) on the remanent polarization. The results showed that the parameters primarily affecting the polarization are temperature and wake-up cycles. As expected, the analysis confirms a dependence between annealing time and temperature, surprisingly, no relevant correlation was observed between cycling and annealing temperature. Maximizing polarization is not the only target, the leakage current has to be minimized. It is critical for NC switches and ferroelectric memory devices since it reduces endurance and is detrimental to NC stabilization. Overall, the best condition for the targeted applications was found for 10 nm thick Si:HfO_2 annealed at 600 °C for 120 s, which has a remanent polarization of 17 $\mu C/cm^2$, in line with literature value, and remarkably a low current density of 45 $\mu A/cm^2$ at 3 V. This enables the use of ferroelectric in the state of the art devices, such as steep slope switches and neuromorphic devices.

Intrinsic switching: insights from temperature-dependent switching and nanoscopic analysis

Our analysis provided insight into a long-standing and highly application-relevant discussion of the intrinsic or extrinsic switching mechanism. Recent studies reported nucleation-limited extrinsic switching, which does not result in a hysteresis-free NC regime. Intrinsic polarization switching, on the other hand, is implied in the LGD formalism, which formally describes NC. In this context, we presented two studies, one on temperature-dependent switching and the other on nanoscopic analysis.

We successfully investigated the temperature-dependent polarization and the electric field characteristics of Si:HfO_2 film. A set of hysteretic P-V curves acquired at temperatures ranging from 80 to 400 K were analyzed using the LGD formalism. Thanks to this, we observed that the Curie-Weiss law fits the derived coefficients closely, and the extrapolated Curie temperature (536 °C) is close to the values found using other approaches. This investigation supported the use of the LGD model to describe temperature dependency in HfO2-based ferroelectric. This study also indicates a method for estimating the ferroelectric equivalent negative capacitance, hence, helping to engineer a stabilized NC-FET.

In the other study focused on the investigation of the switching mechanism, we studied HZO MIFM multi-layer devices by quasi-static measurements like PFM data and ultra-fast

measurements (500 nm). The striking similarity of coercive field measured with two opposite approaches, PFM loops and ultra-fast pulses, points to the possibility of intrinsic switching in MIFM structures. PFM maps exhibit region-by-region switching, which is as well typical of the nucleation-base model. The significant difference is that these areas have clearly defined boundaries with a shape not affected by sequential poling. This result is not predicted by the switching scenario of growing polarization domains. In conclusion, this work presents evidence that strongly points to intrinsic switching as the main mechanism of polarization reversal in MIFM. This has important major repercussions for NC, which can occur just with intrinsic switching. It also has consequences on memory applications, unlike NLS, intrinsic switching is less temperature-dependent, faster, and depends less on the interface qualities crucial in thin films like HfO_2-based ferroelectric.

Comparison between NC-FET gate stack with and without metal interlayer

In this dissertation, we investigated the NC region in MFMIS and MFIS gate stacks in both quasi-static and short pulse measurements (500 ns) allowing us to limit charge injection and mitigate polarization charge screening. As a result, this approach enabled the observation of NC regions (S-shape polarization-voltage slope) in both MFIS and MFMIS gate stacks. The hysteresis-free polarization response of an MFIS device, acquired with short pulses, is consistent with LGD theory and resembles the quasi-static polarization loop. The low retention of the negative state and the imprinted positive state was deducted using pulse measurements and confirmed using local off-resonance PFM. The existence of fixed charges at the ferroelectric-dielectric interface and the built-in field generated by asymmetric electrodes across Si:HfO_2 seem to be the primary causes of imprint. As a result, the MFIS gate stack can be engineered to stabilize polarization, resulting in a hysteresis-free NC region. These findings advance our understanding of ferroelectric gate stacks by providing experimental evidence that the absence of the inner metal plane in gate structures stabilizes the NC regime favorable for hysteresis-free NC-FETs, paving the way for future developments toward steep slope FETs for logic applications.

Fe-JLFET for logic application (NC-FET)

We fabricated NC-FET with 10 nm Si:HfO_2 integrated on top of the gate oxide. The device shows a remarkable electrical characteristic with almost six orders of magnitude I_{ON}/I_{OFF} and a I_{OFF} of around few pA. PFM investigation of the local piezoelectric response indicated that the ferroelectric gate was successfully integrated. It revealed imprinted polarization, which is favorable for operation in the NC regime. It was proven that the given NC-FET, which is the first fabricated JLFET of this type, outperforms traditional junctionless JLFET without a ferroelectric gate in pulse measurement mode, which supports the role of the NC effect in Fe-JLFETs. Overall the fabricated hysteresis-free NC-JLFET showed an enhanced SS with pulses, with a maximum improvement of 35% (over 1.3 decades of drain current) compared to DC condition.

Fe-JLFET for neuromorphic application

We demonstrated a double-gate Fe-JLFET that works as a novel energy-efficient three-terminal synapse with the unique ability to highly control the synaptic weight via the back gate, similarly to the astrocyte process in neuromodulation. Thanks to the internal metal between the ferroelectric film and gate oxide, the integrated Si:HfO_2 integrity was tested electrically and then electromechanically via PFM. The JLFET without ferroelectric is hysteresis-free and well centered compared to the Fe-JLFET characteristic, this further corroborates the impact of the ferroelectric on the JLFET. Then, synaptic behavior was experimentally demonstrated using diverse synaptic schemes, such as amplitude modulation, pulse width modulation, and pulse train. Furthermore, we validated the retention up to 85°C and synaptic plasticity till 2000 cycles in great advance to previous reports with the same technology. Thanks to the double gate control, we proved that synaptic weight could be tuned by more than 400x. Generally, it can be concluded that the Fe-JLFET synapses show a good emulation of biological synapses, including potentiation and depression, manifesting its ability to be incorporated into neuromorphic computing architectures.

5.3 Future Works

Carried in CMi academic clean room and characterization environment, the presented results are not based on very advanced technology nodes and industrial CMOS fabrication lines but, despite these limitations, they have generated some new research ideas and pathways at different levels: beyond CMOS applications, including neuromorphic functionalities, some novel characterization methods, fabrication optimization, and device modeling. In the following sections, we discuss a variety of potential future research directions originating in the subjects discussed in this thesis:

Study of gate structure with different oxide thicknesses by pulse measurement and DC characterization for junction-less transistors

We demonstrated the fabrication of Fe-JLFET with 4nm SiO_2 with optimized Si:HfO_2 ferroelectric fabrication. We also studied two gate stacks, the MFIS gate stack, which showed SS enhancement, and the MFMIS gate stack, which had a threshold voltage tuned by the ferroelectric polarization. The next step would be studying the effect of gate oxide thickness on the Fe-JLFET. Scaling it down will improve the memory capability (memory window and retention) by reducing the depolarization field. On the contrary, the depolarization field will improve NC stabilization, leading to hysteresis-free steep slope FET. The optimization leads to an ambitious project: investigate if there is a thickness trade-off to target both memory and NC regime.

Double gate Fe-JLFETs for neurons

In this dissertation, artificial synapses were demonstrated using Si:HfO_2 Fe-FET implemented in JLFET technology. To get a complete neuromorphic architecture on the same plane, one should have implemented both synapses and neurons that integrate the weighted synaptic inputs and fire the signal to the next neuron. The next step will demonstrate neurons' integration and firing behavior in ferroelectric junctionless FETs. Having neuron synaptic devices with the same material and a similar (possibly the same) fabrication simplifies their integration and the process flow. This would permit us to evaluate and benchmark the speed and power consumption of Fe-JLFET neuromorphic architecture.

Future platforms with memory and logic using Fe-JLFET tecnology

In this work, we verified the functionality of Fe-JLFET for both logic and memory-like application. A long-term plan is to use the already presented building block to innovate Logic-in-Memory (LiM) circuits and analyze the benefits of a junctionless architecture, if any. A JLFETs LiM circuit is essentially a Fe-JLFETs array with some associated NC-JLFETs combinational logic. To assess the advantage of JLFETs LiM circuit, a scalable compact model of the memory and logic building block can be prepared to simulate the LiM, and calibrate on our experimental data.

Combined approach to measure Fe-FET

The general working method of this thesis is to investigate the functionality of the integrated ferroelectric by PFM and then characterize the entire device. A hybrid approach in which the PFM conductive tip controls the gate and the parameter analyzer simultaneously reads the drain current will allow the microscopic ferroelectric analysis (piezoresponse maps and loops), which can be directly linked with the macroscopic functionality of the device (transfer and output characteristic). This combined approach can help the characterization of sub-10nm nodes Fe-FETs. A hardware update is needed to improve the measurement flexibility. In the case of pulse measurement, several variations should be addressed, among which a new cantilever design and a local pulse generator.

A MATLAB algorithm for S-shaped polarization curve extraxtion

Setting parameters

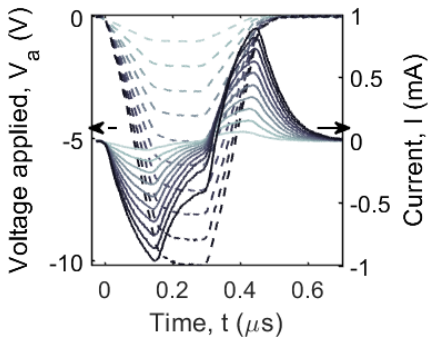
```
R   = 1200;          % Resistance value used [Ω]

Erd = 3.8;           % SiO2 permittivity [-]
E0=8.85e-12;         % Vacuum permittivity [C·V−1·m−1]
td = 4 * 1e-9;       % SiO2 thickness [m]

index_Qres = 180;    % Parameter determining Qres P[m2]

A = 45e-6*45e-6;     % Area of the DUT [m2]

tf = 15*1e-9;        % Ferroelectric thickness [m]
Pcorr = 3.2;         % Correction factior on MFM Pr value [-]
Pr =  +0.031;        % Remanent polarization [C/m2]
```

Load data .mat

```
load("PV_capacitor")      % Load PV of MFM capacitor
name = 'MFMIS';
extention = '.mat';
load([name extention])    % Load pulse data
t=time(1:730,1:60);       % Time
V=Va(1:730,1:60);         % Voltage applied
Vr=Vr(1:730,1:60);        % Voltage drop on the R
```

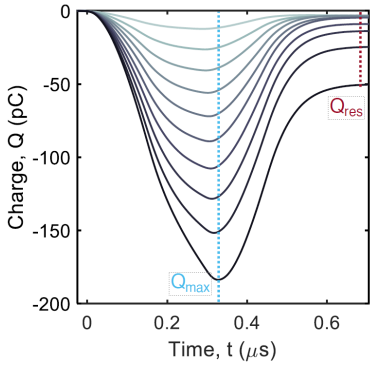
Plot applied voltage vs time (Va-t) and current vs time(I-t)

```
figure
for i=1:10
    yyaxis left
    plot(t(:,i)*1e6,V(:,i),'--');
    hold on
    yyaxis right
    plot(t(:,i)*1e6,I(:,i)*1e3,'-');
    hold on
end
```



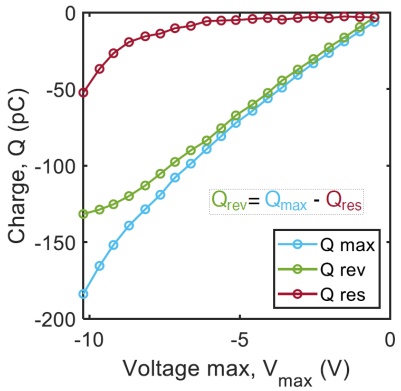
Calculate charge (Q) and plot charge – time (Q-t)

```
[raw,column]=size(t);
figure
for i=1:column
    Q(:,i)=cumtrapz(t(:,i),I(:,i));        % Q(t) calculation
end
for i=1:10
    plot(t(:,i*2)*1e6,Q(:,i*2)*1e12,'-')
    hold on
end
```



Extract charge component (Qres Qrev Qmax) and plot

```
[raw,column]=size(Q);
for i=1:column
    [Qmax(i),index(i)]=min(Q(:,i));        % Qmay extraction
    Vmax(i)=min(V(:,i));                   % Vmax extraction
    Vrmax(i)=Vr(index(i),i);               % Vr extraction
    Qres(i)=Q(index(i)+index_Qres,i);      % Qres calculation
end
Qrev=Qmax-Qres;                            % Qrev calculation

figure
plot(Vmax(:,1:20),Qmax(:,1:20)*1e12,'-o','color',[0.3010 0.7450
0.9330])
hold on
plot(Vmax(:,1:20),Qrev(:,1:20)*1e12,'-o','color',[0.4660 0.6740
0.1880])
hold on
plot(Vmax(:,1:20),Qres(:,1:20)*1e12,'-o','color',[0.6350 0.0780
0.1840])
```

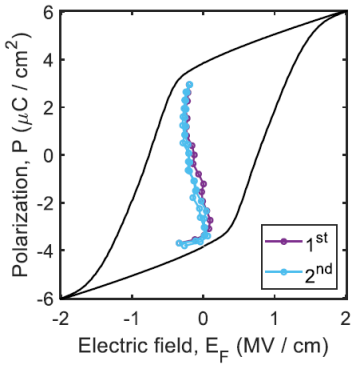


Electric field (Ef) and polarization (P) extraction

```
Cd = Erd * Eo * A / td                     %SiO2 capacitance
E_f = (Vmax - Qrev / Cd - Vrmax)/ tf ;     %Electric field calculation
P = Qrev/A;                          %Polarization calculation
P = P + Pr;                          %Considering remanent polarization
```

Plot P-Ef

```
figure
plot((E_f(:,20:39))*1e-8,P(:,20:39)*1e2,'-
o','MarkerSize',4,'color',color1)
hold on
plot((E_f(:,1:20))*1e-8,P(:,1:20)*1e2,'-
o','MarkerSize',4,'color',color2)
hold on
plot((x/(tf))*1e-8,y/Pcorr,'LineWidth',1.5,'color','k')
```

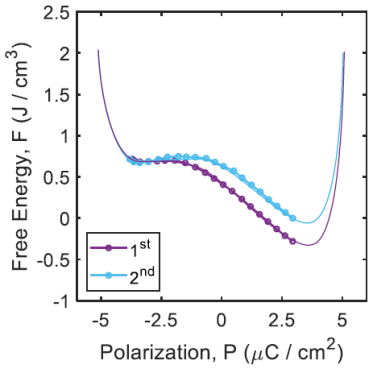


Energy (F) extraction

```
F=cumtrapz(P, E_f);                    % Energy calculation
```

Plot F-P

```
figure
plot(P(:,20:39)*1e2,F(:,20:39)*1e-6,'-
o','MarkerSize',4,'color',color1);
hold on
plot(P(:,1:20)*1e2,F(:,1:20)*1e-6,'-
o','MarkerSize',4,'color',color2);
```



B Runcard of Fe-JLFET with MFIS gate stack

No	Process	Zone/Equipment	Recipe	Target
	Si Patterning			
1.1	Coating	Z1/ACS	HMDS AZ ECI 3007/ 121	0.6um
1.2	Exposure	Z5/VPG	Dose=215 Defoc=0	
1.3	Development	Z1/ACS	AZ 726 MIF/ 821	
1.4	Descum	Z2/tepla gigabatch	Low power 20s	
1.5	Si etching	Z2/AMS 200SE	Si opto nano 0c 19s	
1.6	Oxygen Plasma	Z2/tepla gigabatch	Low power 1min	
1.7	UFT resist	Z2/Wetbench	REM 1165	
	Gate stacking			
2.1	Cleaning	Z14/Wetbench	RCA	
2.2	ALD	Z4/BENEQ	SiO2 - 40 pulses	4nm
2.3	Ellipsometry	Z3/sopra		For inspection
2.4	ALD	Z4/BENEQ	Si:HfO2 - [16:1:16]*4	12nm
2.5	Ellipsometry	Z3/sopra		For inspection
2.6	Deposition	Z11/DP650	TiN	10nm
	Dicing			
3.1	Surface treatment	Z1/Süss hot plates	Thermal dehydration	
3.2	Coating	Z13/ATMsse SB20	AZ 1512/ CHIP 6000	
3.3	Baking	Z1/Süss hot plates	100°C - 63s	
3.4	Dicing			
3.5	UFT resist	Z2/Wetbench	REM 1165	
	Gate deposition			
4.1	Rapid Thermal Process	Z3/JETFIRST 200	600°C - 120s	
4.2	Deposition	Z11/DP650	Pt	20nm

The runcard continues on next page.

No	Process	Zone/Equipment	Recipe	Target
	Dry Etching			
5.1	Surface treatment	Z1/Süss hot plates	Thermal dehydration	
5.2	Coating	Z13/ATMsse SB20	AZ 1512/ CHIP 6000	
5.3	Baking	Z1/Süss hot plates	100°C - 63s	
5.4	Exposure	Z16/MLA	Dose=50 Defoc=-2 laser=405nm	
5.5	Development	Z13/wet bench	AZ 726 MIF 53s	
5.6	Descum	Z2/tepla gigabatch	Low power 20s	
5.7	Etching	Z11/Veeco Nexus	Low IBE 10° 90s	
5.8	Oxygen Plasma	Z2/tepla gigabatch	Low power 30s	
5.9	UFT resist	Z2/Wetbench	REM 1165	
	Lift Off			
6.1	Surface treatment	Z1/Süss hot plates	Thermal dehydration	
6.2	Coating	Z13/ATMsse SB20	LOR Chip 6000/AZ 1512 Chip 4000 - 190°C-4:10/100°C-1:30	0.4um/0.7um
6.3	Exposure	Z16/MLA	Dose=60 Defoc=-2 laser=405nm	
6.4	Development	Z13/wet bench	AZ 726 MIF 75s	
6.5	Inspection			
6.6	Descum	Z2/tepla gigabatch	Low power 20s	
6.7	Etching	Z14/Wetbench	BHF - 10s	
6.8	Inspection			
6.9	Deposition	Z11/DP650	Pt	20nm
6.10	Lift off	Z12/Wetbenche		
6.11	Annealing	Z3/JETFIRST 200	2min/350C	

C Runcard of Fe-JLFET with MFMIS gate stack

No	Process	Zone/Machin	Recipe	Target
	Si Patterning			
1.1	Coating	Z1/ACS	HMDS AZ ECI 3007/ 121	0.6um
1.2	Exposure	Z5/VPG		
1.3	Development	Z1/ACS	AZ 726 MIF/ 821	
1.4	Descum	Z2/tepla gigabatch	Low power 20s	
1.5	Si etching	Z2/AMS 200SE	Si opto nano 0c 22s (Si 15nm)	
1.6	Oxygen Plasma	Z2/tepla gigabatch	Low power 1min	
1.7	UFT resist	Z2/Wetbench	REM 1165	
	Gate Oxide deposition			
2.1	Cleaning	Z14/Wetbench	HF1%	
2.2	ALD	Z4/BENEQ	SiO2 40 pulses	4nm
2.3	Ellipsometry	Z3/Sopra		For inspection
	Inner Gate deposition			
3.1	Deposition	Z11/DP650	TiN	12nm
	Dicing			
4.1	Surface treatment	Z1/Süss hot plates	Thermal dehydration	
4.2	Coating	Z13/ATMsse SB20	AZ 1512/ CHIP 6000	
4.3	Baking	Z1/Süss hot plates	100°C - 63s	
4.4	Dicing			
4.5	UFT resist	Z2/Wetbench	REM 1165	

The runcard continues on next page.

No	Process	Zone/Machin	Recipe	Target
	Inner Gate contacting			
5.1	Surface treatment	Z1/Süss hot plates	Thermal dehydration	
5.2	Coating	Z13/ATMsse SB20	LOR Chip 6000/AZ 1512 Chip 4000 - 190°C-4:10/100°C-1:30	0.4um/0.7um
5.3	Exposure	Z16/MLA	Dose=60 Defoc=-2 laser=405nm	
5.4	Development	Z13/ATMsse SB20	AZ 726 MIF 75s	
5.5	Inspection			
5.6	Descum	Z2/tepla gigabatch	Low power 20s	
5.7	Deposition	Z11/DP650	Pt	20nm
5.8	Lift off	Z12/Wetbenche	REM 1165	
	Gate stacking			
6.1	ALD	Z4/BENEQ	Si:HfO2 [16:1:16]*4	12nm
6.2	Ellipsometry	Z3/sopra		For inspection
6.3	Deposition	Z11/DP650	TiN	6nm
6.4	Rapid Thermal Process	Z3/JETFIRST 200	600°C - 120s	
6.5	Deposition	Z11/DP650	Pt	30nm
	Gate Patterning			
7.1	Surface treatment	Z1/Süss hot plates	Thermal dehydration	
7.2	Coating	Z13/ATMsse SB20	AZ 1512/ CHIP 6000	
7.3	Baking	Z1/Süss hot plates	100°C- 63s	
7.4	Exposure	Z16/MLA	Dose=50 Defoc=-2 laser=405nm	
7.5	Development	Z13/wet bench	AZ 726 MIF 53s	
7.6	Descum	Z2/tepla gigabatch	Low power 20s	
7.7	Etching	Z11/Veeco Nexus	Low IBE -10°	
	TiN Etching			
8.1	Surface treatment	Z1/Süss hot plates	Thermal dehydration	
8.2	Coating	Z13/ATMsse SB20	AZ 1512/ CHIP 6000	
8.3	Baking	Z1/Süss hot plates	100°C - 63s	
8.4	Exposure	Z16/MLA	Dose=50 Defoc=-2 laser=405nm	
8.5	Development	Z13/wet bench	AZ 726 MIF 53s	
8.6	Descum	Z2/tepla gigabatch	Low power 20s	
8.7	Etching	Z14/Wetbench	500ml H2O + 10ml NH4OH 25% + 20ml H2O2 30% @ 50° 5min	
8.8	UFT resist	Z2/Wetbench	REM 1165	

The runcard continues on next page.

No	Process	Zone/Machin	Recipe	Target
	S/D contact lift off			
9.1	Surface treatment	Z1/Süss hot plates	Thermal dehydration	
9.2	Coating	Z13/ATMsse SB20	LOR Chip 6000/AZ 1512 Chip 4000 - 190°C-4:10/100°C-1:30	0.4um/0.7um
9.3	Exposure	Z16/MLA	Dose=60 Defoc=-2 laser=405nm	
9.4	Development	Z13/wet bench	AZ 726 MIF 75s	
9.5	Optical Inspection			
9.6	Descum	Z2/tepla gigabatch	Low power 20s	
9.7	Etching	Z14/Wetbench	HF1% 10s	
9.8	Deposition	Z11/DP650	Pt	20nm
9.9	Lift off	Z12/Wetbenche	REM 1165	
9.10	Annealing	Z3/JETFIRST 200	2min/350C	

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Publications

Journal articles and conference proceedings

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Resume

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Education

2018–2022 **Doctoral Assistant at EPFL**, *Nanoelectronic Devices Laboratory, EPFL*, Switzerland

2016–2017 **Erasmus program in KUL**, *Katholieke Universiteit Leuven*, Belgium

2012–2017 **Bachelor and Master in Electronic Engineering in PoliTo**, *Politecnico di Torino*, Italy

Experiences and Projects

2018–2022 **EPFL**, *Lausanne, Switzerland*, Exploring negative capacitance and neuromorphic devices based on CMOS-compatible ferroelectric HfO_2
Experimental doctoral project with device design, processing in cleanroom and electrical testing with probe station

2016–2017 **IMEC**, *Leuven, Belgium*, Electrical characterization of resistive memory by SPM
Intership with 2D and 3D characterization of VMCO memory by C-AFM and switching failure mechanism study

2016 **KUL**, *Leuven, Belgium*, "CAD project with the use of a Genetic Algorithm"
Algorithm programming MatLab able to design the digital parameter of the PSpice

2015 **Politecnico di Torino**, *Italy*, Digital implementation of a DFT algorithm and of a Digitarl filter
2 different semester university project: digital design through VHDL on FPGA

2014 **Politecnico di Torino**, *Italy*, Digital design of RS232 receiver and transmitter
Semester university project: design hardware (TX and RX) in VHDL on FPGA

Computer skills

Language / software	***Project / application***
MatLab	*Data analysis, genetic algorithm for circuit design, numerical calculus*
Python	*Data analysis, general problem solving*
C	*General problem solving and microcontroller programming*
Simulink	*Modelling of electrode-tissue interface, automatic control*
VHDL	*RS232 receiver and transmitter, numerical digital filter*
Quartus II and ModelSim	*VHDL digital design and simulator*

Publications

C. Gastaldi et al., *IEDM*, 2019, https://doi.org/10.1109/IEDM19573.2019.8993523

C. Gastaldi et al., *APL*, 2021, https://doi.org/10.1063/5.0052129

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Languages

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