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High frequency IGCT operation for DC transformer

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par

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To my lab colleagues

Abstract

In spite of the dominance of ac technology for the vast majority of power transmission and distribution since the late 19^{th} century, the past decades have seen an increase in use of dc electrical power. In particular, this has been the case both in high voltage transmission, and in low voltage islanded dc grids such as shipboard power distributions systems, or dc buildings. The increase in interest for dc electrical power is mainly due to its overall decreased losses compared to its ac counterparts, increased flexibility, and ability to more easily integrate renewable generation and energy storage. In this context, medium voltage dc grids currently lack in standardisation and are still an active research topic.

The dc transformer is expected to be a key technology for the operation of future medium voltage dc systems. Essentially, its function is equivalent to the traditional ac transformer in providing an isolated interface between dc buses at different voltage levels. Yet, unlike the purely passive traditional transformer, the dc transformer is also expected to integrate additional functionality, particularly regarding system protection. Most embodiments of the dc transformer proposed in academic publications are based on the dual active bridge, with IGBTs being the semiconductor of choice and with galvanic isolation provided by a medium frequency transformer. Compared to this solution, alternative technologies have been somewhat overlooked, in terms of topologies and devices. In particular, resonant conversion for dc transformer applications has not gained much popularity.

The focus of this thesis is on a medium voltage dc transformer employing IGCTs as semiconductor devices, in a bidirectional series resonant LLC topology. The principle behind the selection of this topology and device is the synergy between the IGCT, which contributes the lowest conduction losses of any actively controlled semiconductor switch, and the series resonant LLC converter principle of operation, which provides low switching loss through soft turn-on and low current turn-off. With this goal in mind, a significant technical challenge to be overcome is the increase of switching frequency of the IGCT well beyond the sub-kHz level at which it traditionally finds application, and into the multi-kHz range, targeted by dc transformer applications.

This thesis contains three main contributions aiming to acquire sufficient knowledge for the design of dc transformer lab demonstrator. For this purpose, the boundary between zero-voltage and zero-current switching of the IGCT is initially explored to identify the lowest switching loss condition through the variation of turn-off current value. Then, in these low-loss conditions, thermal steady state operation of the IGCT is demonstrated at the frequency of 5 kHz for the first time, proving that the IGCT is a device capable of medium frequency operation. Engineering samples of IGCTs optimised on the technology curve through varying levels of electron irradiation are also explored in order to quantify potential benefits in the dc transformer application. Finally, medium frequency operation of the device is extended to an increased voltage level through series connection of IGCTs, through custom ultra-low capacitance, purely capacitive snubbers, designed for the challenges of 5 kHz operation.

Ultimately, the thesis demonstrates that while the IGCT has traditionally found use in sub-kHz, hard-switched applications, its ruggedness and reliability allow its use well beyond its intended applications, and place it comfortably among devices capable of medium frequency operation.

Keywords medium voltage, dc transformer, series resonant converter, IGCT, series connection, soft switching

Sinossi

A partire dalla fine del diciannovesimo secolo, la quasi totalità della trasmissione e distribuzione di energia elettrica ha avuto luogo corrente alternata. Ciononostante, negli ultimi vent'anni si è assistito ad un aumento della presenza di soluzioni in corrente continua, in particolare nella trasmissione di energia su lunghe distanze ad alta tensione, ed in micro-reti isolate dalla rete elettrica. Alcuni chiari esempio di questo fenomeno risultano essere un crescente numero di edifici alimentati in corrente continua, e diversi sistemi di distribuzione di energia elettrica ad uso navale. Il rinnovato interesse per queste tecnologie è una conseguenza dell'aumento dell'efficienza in trasmissione, flessibilità, e della facilità di integrazione della generazione da fonti rinnovabili e sistemi di stoccaggio di energia. In questo contesto, non esiste al momento uno standard determinante le principali caratteristiche di interesse in reti in corrente continua ed in media tensione, che restano tutt'ora un acceso tema di ricerca.

Il funzionamento di future reti in corrente continua ed in meda tensione richiede la presenza di trasformatori in grado di interfacciare linee a diversi livelli di tensione fornendo isolazione galvanica. In pratica, le funzionalità richieste ad un trasformatore in corrente continua sono equivalenti a quelle di un tradizionale trasformatore, ma con l'aggiunta di funzioni di protezione che sono inevitabilmente assenti nei tradizionali trasformatori, essendo questi ultimi componenti completamente passivi. La maggior parte dei trasformatori in dc presentati in pubblicazioni accademiche consistono in un inverter e raddrizzatore, separati da un trasformatore ac a media frequenza. Sia l'inverter che il raddrizzatore devono essere bidirezionali per garantire in transito di energia nelle due direzioni quando necessario. In termini di topologie e semiconduttori, le tecnologie prese in considerazione sono numerose.

L'attenzione di questa tesi verte in particolare su un trasformatore in dc basato sull'uso dell'IGCT come semiconduttore, in una topologia SRC-LLC. La scelta dei semiconduttori e topologia sono la conseguenza di un lavoro di ricerca già iniziato nel laboratorio negli anni scorsi, sul quale si basa il contenuto presentato in questa tesi. Il criterio che ha determinato questa scelta è il potenziale aumento di efficienza ottenuto grazie al basso livello di energia dissipata in conduzione dall'IGCT, unito al soft-switching offerto dall'SRC-LLC, che offre una riduzione dell'energia dissipata in commutazione.

Questa tesi si divide in sei capitoli, tre dei quali contenenti le sue principali innovazioni. Il loro obiettivo è di acquisire sufficiente comprensione dei fenomeni risultanti dall'utilizzo dell'IGCT nella topologia SRC-LLC per consentire la realizzazione di un prototipo di trasformatore in dc per use in laboratorio. A questo fine, un primo capitolo esplora il confine tra la regione di commutazione in zero-voltage e zero-current per l'IGCT, identificando le condizioni di minima energia dissipata attraverso la variazione della corrente di turn-off. Determinate queste condizioni, si è dimostrata l'operazione continua dell'IGCT alla frequenza di commutazione di 5 kHz nella topologia SRC-LLC. Questo colloca per la prima volta l'IGCT tra i semiconduttori in grado di operare a media frequenza. Questa modalità di operazione viene estesa alla connessione in serie di due IGCT ottenuta con l'ausilio di snubber capacitivi progettati *ad hoc* per la commutazione dell'IGCT in media frequenza.

Questa tesi dimostra quindi che nonstante l'IGCT abbia tradizionalmente trovato applicazione a frequenze inferiori a 1 kHz, il suo uso può essere esteso ben oltre questi livelli, collocandolo tra i semiconduttori capaci di operare in media frequenza.

Parole chiave media tensione, trasformatore dc, LLC-SRC, IGCT, connessione in serie, soft switching

Acknowledgments

Quote me! Quote me!
Amanda Klaeger

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It goes without saying that I am thankful to my family and friends back in Italy (and also Pascal), who were always there for me during the many good (and a few less good) days.

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Lausanne, July 2022
Gabriele Ulissi

List of Abbreviations

DAB	dual active bridge
DCT	dc transformer
DCT	DC transformer
DP	double pulse
DUT	device under test
EMI	electromagnetic interference
EV	electric vehicles
GTO	gate turn-off thyristor
HVdc	high voltage dc
IEGT	injection-enhanced gate transistor
IGBT	insulated-gate bipolar transistor
IGCT	integrated gate-commutated thyristor
LV	low voltage
LVdc	low voltage dc
MFT	medium frequency transformer
MMC	modular multilevel converter
MV	medium voltage
MVac	medium voltage ac
MVdc	medium voltage dc
NPC	neutral point clamped
PDN	power distribution network
PEBB	power electronics building block
PET	power electronics transformer
RC-IGCT	reverse-conducting IGCT
RMS	root mean squared

SCR silicon controller rectifier
SOA safe operating area
SRC series resonant converter
SST solid-state transformer

WCU water cooling unit

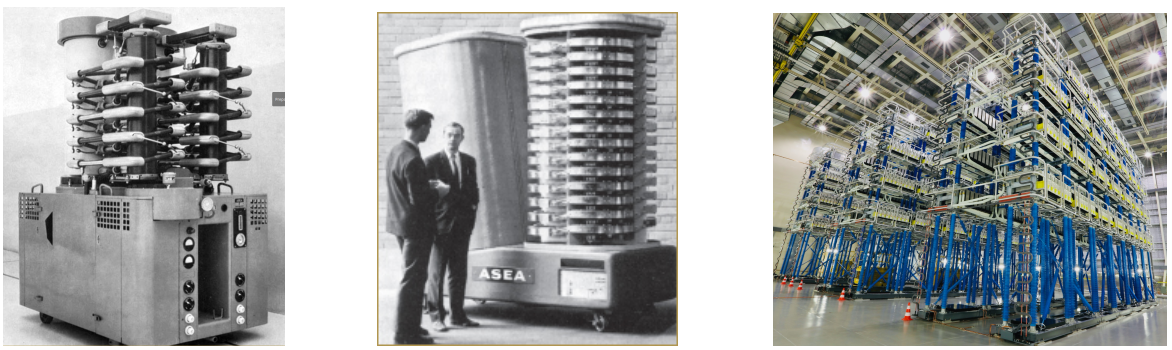
ZCS zero current switching
ZVS zero voltage switching

Contents

1 Introduction

1.1 Background and motivation

The second half of the 19th century saw the beginning of large-scale electrification with both dc and ac systems coexisting in urban and private illumination applications. While dc systems initially gained the upper hand thanks to the availability of dc generators, this advantage was soon lost. The late 1880s saw the advent of both the transformer and the induction generator, two key technologies that enabled transmission of electrical power with smaller losses and over a significantly increased distance compared to the established 110 V dc systems. The reduced operating cost, together with the ease of interruption of ac current, allowed ac systems to definitively prevail over their dc counterparts by the end of the century. To this day, ac power transmission and distribution is by far the prevailing technology, having been well-established for over a century and leveraging vast amounts of accumulated technical know-how. Nevertheless, as early as the 1950s, dc power transmission once again found application in the first commercial long-distance 110 kV high voltage dc (HVdc) line connecting mainland Sweden with Gotland and employing mercury-arc line commutated converters. This installation was the first of its kind and demonstrated the feasibility of HVdc transmission, but the number of new installations remained modest in the following years: the advantages of dc transmission were offset by the comparatively high maintenance, low reliability and high operating temperatures of mercury-arc valves. It was only with the advancements in material sciences and semiconductor technologies that characterised the following decades which allowed lower maintenance solutions based on thyristor technology in the 1970s, and with GTOs and IGBTs later becoming the prevalent devices.



(a) (b) (c)

Fig. 1.1 a) ASEA Mercury-arc valve, 1971 (photo courtesy of ABB); b) Experimental thyristor valve tested in Gotland link, 1967 [1]; c) Contemporary GE IGBT-based MMC valve hall.

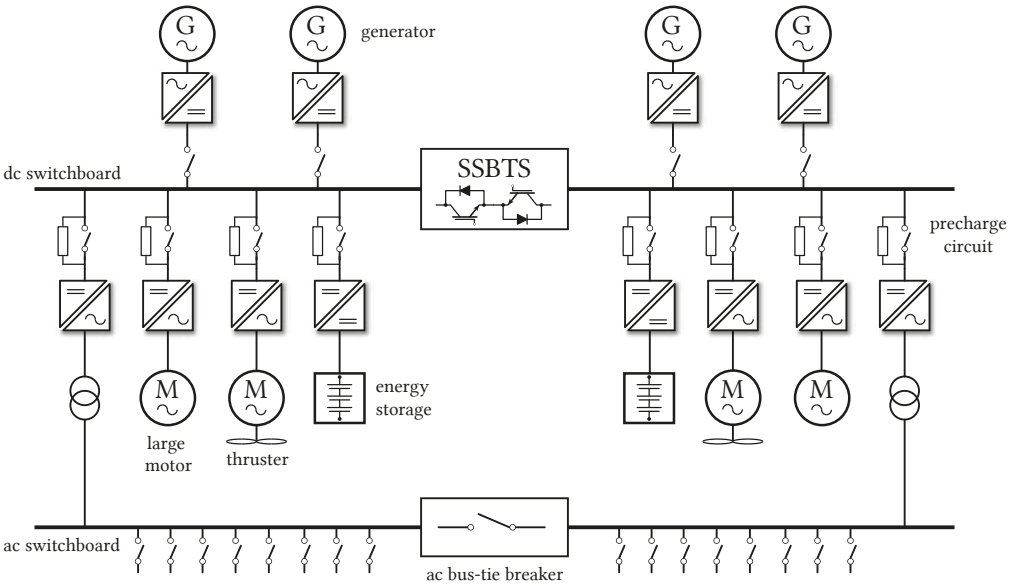


Fig. 1.2 LVdc shipboard PDNs can achieve higher efficiency and operate without the need for bulky low-frequency transformers [6], [7].

With the use new semiconductor devices, the dc transmission of electrical power has numerous advantages over traditional ac systems. First of all, the absence of reactive power transmitted over the lines reduces losses for a given transmitted active power. Additionally, the line voltage at the receiving end of the line will be less sensitive to the operating conditions compared to that of an ac link, as there is no reactive voltage drop, nor capacitive currents providing reactive power and increasing the line voltage in low-load conditions. Finally, the reduced presence of skin and proximity effects mitigates the increase of line resistance due to these phenomena, and ultimately the resulting loss.

Naturally, these benefits are not limited to the voltage levels of several hundreds of kV present in HVdc systems: low voltage dc (LVdc) systems have already become a commercial reality at voltage levels below 1 kV. Such systems are particularly popular in applications which are intrinsically stand-alone installations, and therefore do not suffer from the inertia associated with the adoption of solutions in grid-connected operation, such as marine power distribution networks (PDNs) and offshore applications. As seen in Fig. 1.2, in this context dc distribution has the additional benefits of eliminating the need for bulky line frequency transformers, and of rendering the synchronisation of the micro-grid's generators unnecessary through the rectification of their output [2], [3].

Such LVdc systems leverage well established, efficient, and affordable semiconductor technologies available at the 1 kV voltage level. Nevertheless, they also required the addition of innovative solutions, in particular concerning the protection of the system: fault evolution in dc systems is several orders of magnitude faster than in traditional ac systems due to the significantly reduced inductance levels, and therefore requires the use of ultra-fast solid state protection solutions instead of slow conventional mechanical breakers [4], [5].

With LVdc shipboard PDNs having proved the commercial viability of dc systems, the next step in

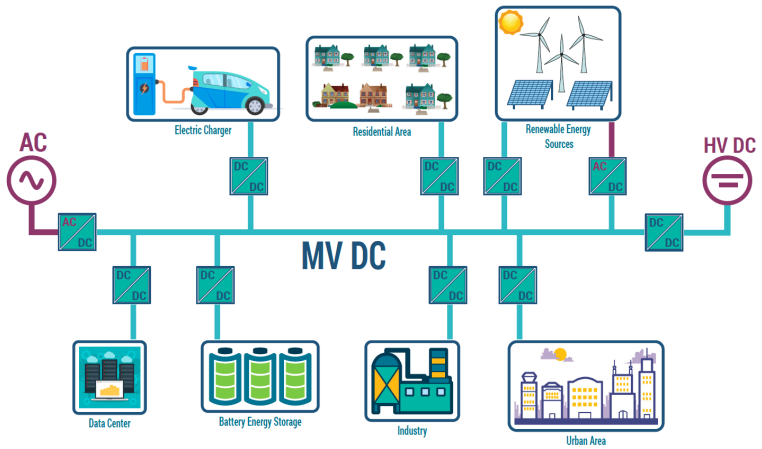


Fig. 1.3 Medium voltage dc distribution networks facilitate the integration of dc loads, generation, and storage.

the drive for ever-increasing efficiency is the increase of the dc PDN voltage to the medium voltage (MV) level, enabling installed power similar to those of medium voltage ac (MVac) shipboard PDNs, but maintaining the increased efficiency and flexibility of dc systems.

While shipboard PDNs lend themselves to innovative solutions thanks to their islanded operation, the replacement of MVac systems with medium voltage dc (MVdc) systems offers significant advantages also in energy distribution. These advantages go beyond system efficiency, in particular thanks to the changing nature of modern electrical loads. Fig. 1.3 displays how an MVdc distribution network can reduce the number of required conversion stages in the integration of dc loads, generation, and energy storage, allowing for more compact and less costly solutions [8], [9].

In spite of these benefits, MVdc networks are not yet a reality. The main impediment in their development and commercial use lies in limitations of existing technologies, with examples being suitable protection devices, and the dc transformer (DCT). The DCT in particular has been the object of much research in the past years, as it is required to perform the crucial function of providing an isolated interface between dc buses at different voltage levels. Currently, no commercial embodiments of a DCT are deployed, and the device exists only as part of research installations, in which various

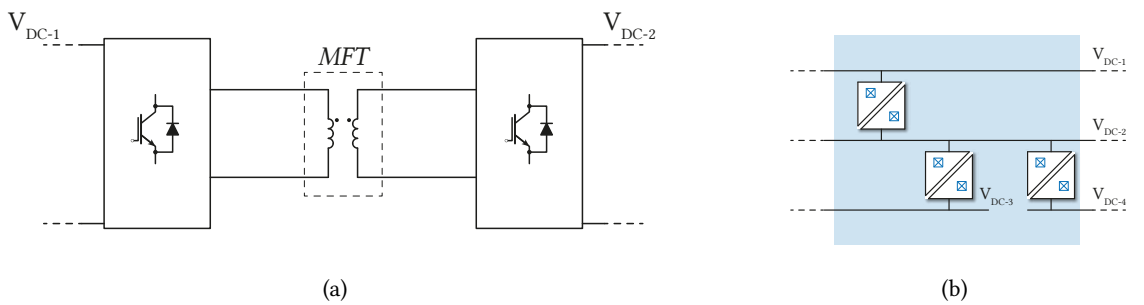


Fig. 1.4 a) A generic dc transformer concept is consituted by a bidirectional inverter and rectifier stage separated by a medium frequency transformer (MFT); b) the role of the dc transformer is to interface buses at different voltage levels in dc networks.

solutions based on different topologies and semiconductor devices have been proposed [10]–[12].

Figs. 1.4(a) and 1.4(b) display a generic concept of DCT and its integration in a dc network, respectively. In principle, the device is composed of bidirectional inverter and rectifier stages separated by a MFT, and is intended to perform a very similar role to that of a conventional transformer in an ac system. More specifically, just like an ac transformer, the device is expected to provide galvanic isolation, bus interconnection at different voltage levels, and, in the context of this thesis, open-loop operation without the need to be externally provided with an operating setpoint. In addition to the functionality of an ac transformer, the DCT is also expected to provide some protection functions and limited ancillary services to the dc grid.

One of the more significant advantages of the use of a DCT with respect to a traditional ac line frequency transformer is the significant decrease in weight and footprint. This is achieved through the reduction in volume of required magnetic material allowed by the increase in fundamental operating frequency. To capitalise on this benefit, switching frequencies in high-power DCT applications are in the range of several kHz (or for SiC devices several tens of kHz). To achieve such switching frequencies, the use of the SiC MOSFET as a semiconductor device has steadily being gaining interest, but the preferred solution remains today the Si IGBT, being widely available and having a demonstrated track record of reliability, good switching characteristics and ease of gate drive [13], [14].

Nevertheless, in spite of the popularity of the IGBT in many applications, the few decades have seen the emergence of an alternative device providing reliable performance at the MV level in the form of the IGCT, but with its application mainly being reserved to the power level of several MW and switching frequencies below 1 kHz [15]–[18]. Compared to the IGBT, the IGCT features comparable switching losses, but being a thyristor-based device it benefits from lowered conduction loss, improved reliability, larger safe operating area (SOA), and lower thermal resistance between junction and case in press packed devices thanks to the excellent utilisation of the silicon wafer area.

It is the IGCT's low conduction loss that highlight it as an interesting candidate for the high-power ratings of DCT applications. This is particularly the case in combination with soft-switched topologies such as the LLC-SRC, which can combine the device's intrinsically low conduction loss with the low switching losses deriving from the topology's operation. The combination of these two technologies has been shown in [19] to allow the operation of IGCTs at unprecedented frequencies for this kind of device.

The work presented in [19] demonstrated through a custom configurable test setup the feasibility of high-frequency IGCT operation in operating conditions equivalent to those witnessed by the device during operation in the LLC-SRC topology. In particular, it has demonstrated that through the reduction of the devices' turn-off current to a very low level, the switching loss can be reduced sufficiently to allow operation at a frequency an order of magnitude higher than what is possible to achieve in traditional hard-switched applications, placing the IGCT comfortably among the suitable semiconductor options for use in DCTs.

1.2 Goals and contributions of the thesis

The goal of this thesis is to expand on the work presented in [19] and lay the groundwork for the prototype realisation of a DCT demonstrator interfacing two dc buses at voltages of 5 kV and 10 kV, respectively. In practise, this implies several steps. First, to increase the IGCTs' switching frequency

to the desired level of 5 kHz. As such a significant increase in switching frequency inevitably results in increased switching loss, the work is started by a comprehensive investigation of the switching behaviour of IGCTs in zero voltage switching (ZVS) and zero current switching (ZCS) conditions. This builds a strong understanding of the IGCT behaviour in various soft-switching conditions, and demonstrates that ZVS operation is advantageous for the minimisation of switching loss in resonant operation. The operation of the IGCT is described as part of the thesis as it is relevant to the understanding of the presented work. Second, to enable operation of the solution at a voltage level of 5 kV, series connection of the employed 4.5 kV IGCTs is required. Therefore, the switching behaviour of the devices in series connection and with low turn-off current is investigated. This is done with particular focus on the sizing of dynamic voltage sharing snubbers and turn-off current values. Finally, steady state operation of the IGCTs at a frequency of 5 kHz is demonstrated for both individual and series connected devices. Therefore, the main contributions of the thesis can be summarised as:

- The identification, through the use of the same test setup presented in [19], of optimal switching conditions resulting in minimised switching loss for 4.5 kV, 68 mm IGCTs having undergone varying level of electron irradiation. ZVS and ZCS switching conditions are compared, and ZVS switching is found to be beneficial as it results in lower overall loss in resonant switching conditions. Optimal turn-off current levels resulting in minimal loss are determined for the varying electron irradiation levels of the devices.
- The demonstration, with the identified optimal turn-off current level and ZVS switching conditions, of steady state soft-switched operation of the devices at a frequency of 5 kHz at a dc link voltage of 2.5 kV, and varying levels of load. The very effective water cooling system available in the laboratory installation allows for safe test conditions for the devices, but junction temperature estimation based on the device losses predicts the feasibility of high frequency operation also with a reduced cooling effort.
- The demonstration of resonant operation in soft-switched conditions at 5 kHz at increased voltage level through the series connection of 4.5 kV, 68 mm devices. This is achieved with the use of purely capacitive dynamic voltage sharing snubbers with ultra-low values of capacitance, which are designed specifically for use with the ultra-low levels of turn-off current characteristic of subresonant LLC operation.

1.3 Outline of the thesis

This thesis is organised in 6 chapters, as follows:

- ***Chapter 2*** covers the state of the art of high power dc converters and their application in MV systems. Existing work on converter topologies by academic and industrial players is presented, together with the most commonly employed semiconductor devices and their applicability to the LLC-SRC topology.
- ***Chapter 3*** discusses in detail the operation of the LLC-SRC topology and justifies the selection of IGCT switching mode between ZVS and ZCS. The switching energy in the two operating conditions is compared and the measured trends justified. GCTs differing by level of electron irradiation are compared and optimal switching conditions for the various devices identified, considering the effect of current pre-flooding.

- ***Chapter 4*** demonstrates the operation of IGCTs at a frequency of 5 kHz in the conditions occurring in a series resonant LLC converter, considering standard, commercially available device, and custom engineering samples optimised on the technology curve through varying levels of electron irradiation. The switching and conduction losses of the devices in these conditions are discussed and compared.
- ***Chapter 5*** deals with series connection of IGCTs under ultra-low turn-off current conditions, allowing for increased operating voltage of the IGCT-based LLC-SRC topology. The effects of such conditions on snubber sizing are analysed and purely capacitive snubbers ensuring adequate voltage sharing of series connected devices at the 5 kV are designed and tested in double-pulse tests. Finally, 5 kHz series connected operation of the devices is demonstrated.
- ***Chapter 6*** concludes the thesis summarising the main obtained results and suggesting future work on the topic.

1.4 List of publications

Journal papers:

J1. G. Ulissi, U. R. Vemulapati, T. Stiasny, and D. Dujic, "High-frequency operation of series-connected igcts for resonant converters," *IEEE Transactions on Power Electronics*, vol. 37, no. 5, pp. 5664–5674, 2022

J2. G. Ulissi, J. Kucka, U. R. Vemulapati, T. Stiasny, and D. Dujic, "Resonant igct soft-switching: Zero-voltage switching or zero-current switching?" *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 10 775–10 783, 2022

Other publications, related to research work carried out during the PhD but not included in this thesis:

J1. G. Ulissi, S.-Y. Lee, and D. Dujic, "Solid-state bus-tie switch for shipboard power distribution networks," *IEEE Transactions on Transportation Electrification*, vol. 6, no. 3, pp. 1253–1264, 2020

J2. G. Ulissi, S.-Y. Lee, and D. Dujic, "Scalable solid-state bus-tie switch for flexible shipboard power systems," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 239–247, 2021

J3. G. Ulissi, S. Kim, and D. Dujic, "Solid-state technology for shipboard dc power distribution networks," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 12, pp. 12 100–12 108, 2021

J4. S. Kim, J. Kucka, G. Ulissi, S.-N. Kim, and D. Dujic, "Solid-state technologies for flexible and efficient marine dc microgrids," *IEEE Transactions on Smart Grid*, vol. 12, no. 4, pp. 2860–2868, 2021

J5. S. Kim, G. Ulissi, S.-N. Kim, and D. Dujic, "Protection coordination for reliable marine dc power distribution networks," *IEEE Access*, vol. 8, pp. 222 813–222 823, 2020

C1. G. Ulissi, S.-Y. Lee, and D. Dujic, "Four quadrant bus-tie switch for protection of shipboard power systems," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, P.1–P.9

C2. G. Ulissi, S.-Y. Lee, and D. Dujic, "Scalable marine bus-tie switch for switchboard interconnections," in *PCIM Europe digital days 2020*, 2020, pp. 1–10

C3. S. Kim, G. Ulissi, S.-N. Kim, and D. Dujic, “Marine dc power distribution networks,” in *PCIM Europe 2019*, 2019, pp. 1–8

Patents:

P1. G. Ulissi, D. Dujic, S. H. Kim, D. Y. You, and S. Y. Lee, *”bus tie switch and bus tie switch apparatus”*, KR Patent 20200138476, 2021

2
State of the Art

High power MVdc applications have seen a number of different solutions being proposed in an equally wide range of use case scenarios. Different concepts, topologies, semiconductors, and operating modes can be combined to tailor the performance of the conversion stage to the application at hand, providing plenty of degrees of freedom in design. This chapter provides an overview of the most frequent technologies considered for MV dc transformers, gradually narrowing down the many possible options and justifying the selection of the technologies discussed in this thesis.

2.1 Introduction

The new solutions offered by MVdc power collection and distribution grids offer a strong alternative to existing ac networks at the same voltage level in several applications. However, the absence of adequate conversion or protection technologies is almost always a hindrance to practical implementations of MVdc, no matter the advantages they can bring [20]. Additionally, and perhaps more importantly, the lack of standardised technologies currently brings the cost of such installations to levels significantly higher than those of their comparable traditional ac counterparts, creating a chicken-and-egg problem which currently has not yet been solved.

In applications such as wind farm collection networks, on- and off-shore, MVdc networks are considered for the collection of energy generated by each turbine, with the whole MVdc collection network then being interfaced to the on-shore grid. The interfacing of the rotating generators in the wind turbines to the MVdc collection network requires rectification and voltage step-up, which can be achieved either in a single ac-dc stage or by cascaded ac-dc and dc-dc stages [21]. Several important advantages have been identified in the use of such connection networks, ranging from increased efficiency and lowered cost, to system scalability and lowered footprint and filtering efforts. Nevertheless, the absence of suitable protection and conversion technologies, together with the absence of standardised dc voltage levels, result in the absence of large scale installations of MVdc collection systems, with photovoltaic installations suffering from the same issues [22]. The replacement of MVac distribution with MVdc distribution in certain applications can be seen to be another example in which MVdc is the next logical step.

The use of all-electric ship power systems has already taken place at the low voltage (LV) level. Many advantages are evident in the application: first and foremost the elimination of bulky MVac transformers resulting in significant space savings and easier integration of alternative energy sources and energy storage, overall resulting in significant expected fuel and therefore cost savings [23], [24]. Additionally, the need to synchronise multiple generators to create an ac power distribution network is removed. But again in this application a large technology gap is still to be bridged, with similar

observations as those applying to on-shore microgrids [25], [26]. Finally, large data centers internally employ LVdc distribution and can be considered as large dc loads, with dc distribution improving overall efficiency and eliminating ac-dc conversion [27]–[30].

MVdc networks can connect various loads and sources to the existing ac system. Existing commercially available technologies such as monolithic multilevel converters and the modular multilevel converter (MMC) can be used for MVdc to MVac interconnection, but dc-dc conversion between different voltage levels is still an open research question both in terms of operating principles and technologies. Modern means of power generation and new loads, such as electric vehicles (EV) charging stations, energy storage systems, and many more require a solution in terms of energy systems power flows and its control. In this context, this thesis proposes an IGCT-based DC transformer (DCT) solution differentiating itself from most of the existing literature by relying on bulk power transfer, as opposed to the more commonly advertised fractional or nowadays popular modular solutions. To achieve this, several choices are made regarding employed topology, devices, and operating mode, which are contextualised and justified as part of this chapter.

2.2 DC-DC Bulk versus Fractional Conversion

The variety of voltage and power levels of MVdc networks impose scalability as a necessary feature of any DCT solution. Such scalability in power processing can be achieved by two radically different approaches: the first considers series or parallel connection of PEBBs, each containing an MFT unit. Each PEBB has a lower power rating than the complete system, but the use of multiple units in the appropriate configuration achieves the rating of the overall system. The second approach uses semiconductor devices specifically sized for the application, resorting to series or parallel connection where necessary and a single MFT, as seen in Fig. 2.1. In practise, this results in a single PEBB rated for the full power of the application. The two methods result in different implications on the overall power electronics system.

Arguably, a significant amount of work carried out on the topic of MVdc conversion stems from the solid-state transformer (SST) concept initially reported in [33]. Over time, numerous embodiments of this concept have been reported, with [34]–[37] being examples resulting from the work of the *UNIFLEX* consortium, *HEART*, *GE*, and *ABB*, respectively. Over time, the concept has found application in both the traction and smart-grid domains, but its idustrial implementations remain few and far inbetween whether in fractional or bulk power processing configurations. Compared to its industrial applications, many more academic examples [34], [38]–[47] exist, with multiple laboratory-scale prototypes having been realised and based on different topologies and control schemes. Among these existing examples, there is a prevalence of modular solutions based on individual PEBBs processing a fraction of the power of the overall converter [48], [49].

Fractional power processing has many benefits, which derive from the necessary underlying modularity of such topologies. The use of several PEBBs to achieve the required power rating allows parallel or series connection of such units, allowing simple scaling of the overall converter voltage and power rating without requiring the redesign of the PEBB. Additionally, redundant units can be employed to reduce the voltage stress on semiconductor devices, and can be bypassed in the event of a fault, allowing uninterrupted operation for the remaining duration of the maintenance interval. Further, depending on the PEBB configuration, plug-and-play functionality can be explored, where the failed PEBB can be replaced by a new unit with minimal effort and in minimal time.

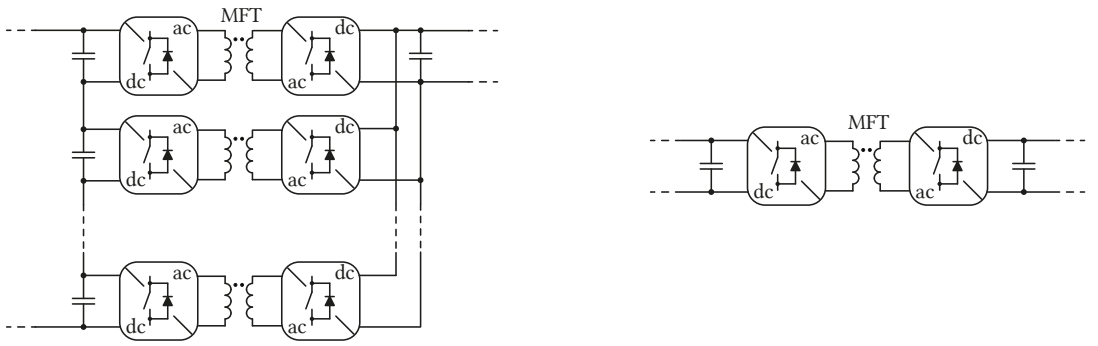


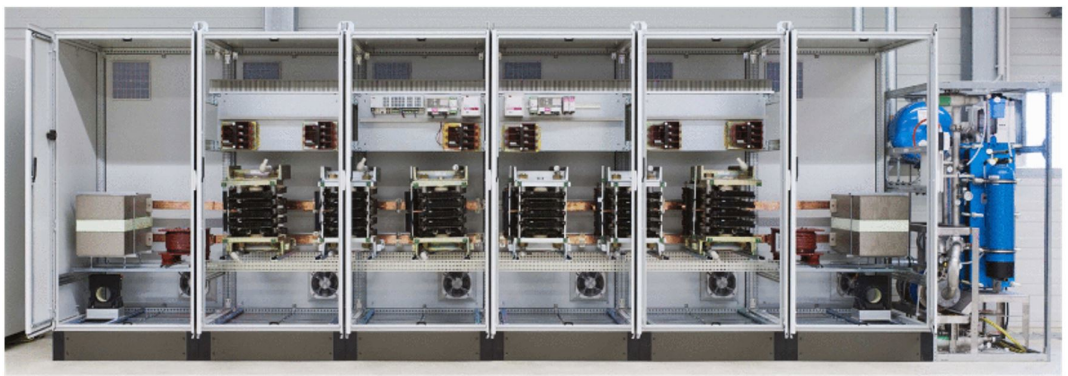
Fig. 2.1 a) In fractional power processing, each ISOP power electronics building blocks (PEBBs) processes a fraction of the total rated power of the converter, while in b) bulk processing a single monolithic structure handles the full power of the topology.

Nevertheless, fractional power processing topologies also have their disadvantages. As each PEBB is a standalone unit, it is equipped with semiconductors, passive, and magnetic components, and will be equipped with its own control unit. This significantly increases the overall component count of the topology with inevitably undesirable consequences both on the overall system reliability, and both electrical and mechanical complexity. Additionally, each employed PEBB must be designed in terms of insulation coordination for the highest system voltage. This results in a component than cannot be employed with higher system voltages, and that is oversized for lower voltage applications. Finally, power sharing between the PEBBs must be addressed either in design or through control, while bypass elements must be added if operation of the topology is to be continued in the event of PEBB failure.

Compared to fractional power processing solutions, configurations providing bulk power processing are simpler, have lower mechanical and electrical component count, and benefit from reduced control complexity. These benefits are nevertheless offset by the need to provide a custom design for each application's voltage and power rating, with limited options for reusing existing solutions. In addition, the effects of a failure in the power stage cannot be contained as easily as in a topology employing multiple PEBBs, and must rely on an increase of the number of employed semiconductors.

Nevertheless, the goal of the DCT is to provide functionality as close as possible to that of a conventional ac transformer. With this in mind, the crucial bus interfacing role of the DCT requires its implementation to achieve high levels of reliability, that benefit from the relatively low component count achieved through the parallel and series connection of individual semiconductor devices. The complexity, high component count, and increased control effort are particularly undesirable in the DCT application, and bulk power processing solutions are therefore preferable in this context and for this reason. Therefore, a bulk power processing solutions is selected in the context of this thesis.

(a)



(b)

Fig. 2.2 a) 1.2 MW power electronics traction transformer prototype described in [31] and employing several power processing units in an ISOP configuration; b) 5 MW, 5 kV monolithic three-phase dual active bridge (DAB) converter from [32].

2.3 Main Topologies for MVdc DCT Applications

Among the suitable topologies to achieve bulk power conversion in MVdc systems, three in particular are promising and have been well-investigated.

2.3.1 Dual Active Bridge

The first considered topology, that has seen the most research effort for DCT applications, is the DAB. The topology has been thoroughly explored both in academic and industrial settings starting with [50]–[52], which first introduced the concept as far back as in 1990. Leveraging improvements in both magnetic and semiconductor components, the DAB is once again at the centre of research attention both in its single-phase and three-phase implementation, as displayed in Fig. 2.3. References [53]–[59] describe the steady state operation, design, control strategies and dynamic modelling of the topology. In essence, its foremost benefit is its simple operating principle of an inverter and active

rectifier interfaced by a medium frequency transformer. This leads to a phase-shift power transfer control similar to well-known ac network principles, which in an ideal case results in active power transfer being described by

$$P = \frac{nV_1V_2}{f_{sw}L}\Phi(1-2\Phi) \tag{2.1}$$

as the two bridges are operated with constant duty cycle approaching 50 %, the phase angle Φ is the only degree of freedom available for control, which is simple and easy to implement.

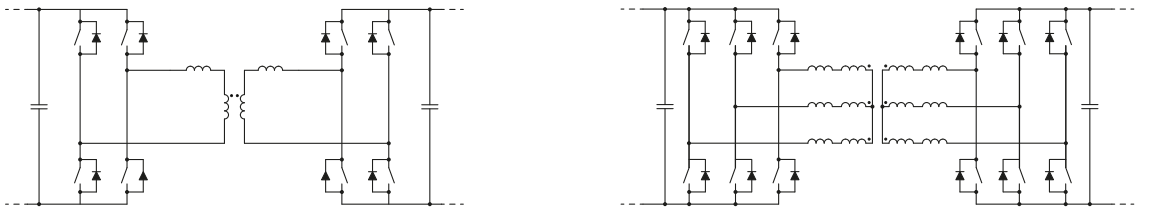
Operation of the converter at medium frequency ensures that the DAB can provide both isolation and voltage transformation through the use of a high power density transformer. For three-phase DAB, continuous active power flow is provided, reducing voltage ripple and therefore allowing for smaller sizing of dc capacitors. The power flow of the topology is regulated through the stray inductance of the transformer by phase shifting the operation of the inverter and rectifier stage that both operate producing square wave voltage waveforms. In such an operating mode, semiconductor devices operate in soft-switched condition (ZVS specifically), reducing switching losses and resulting in high conversion efficiency.

Recently, there have been ongoing research efforts focusing on the improvement of the DAB performance with the purpose of enabling its use in dc grid distribution substations in the role of DCT. By employing three-level inverter and rectifier stages, or by using auxiliary circuitry, the ZVS operation of the topology can be extended, potentially enabling increased switching frequencies by the employed medium voltage semiconductor devices [60]. Additionally, fault ride-through capability and short circuit current control can be achieved through variable duty cycle control [60], [61], which reduced or potentially eliminated the need for additional current breaking componentry in dc grid applications. Nevertheless, the main notable advantage of the topology remains a low component count and relatively small size and weight (depending on the operating frequency).

On the other hand, while the converter can operate in ZVS, its operating range in such a condition is relatively limited. Circulating currents also represent a drawback of the topology, limiting efficiency by causing inevitable losses in both semiconductor components and transformer windings (although this is not exclusive to the DAB topology). Additionally, the topology requires bulky input and output dc-link capacitors to supply the high root mean squared (RMS) values of current, which have the ulterior disadvantage of limiting the power density of the converter [62]. Finally, while the control of the topology based on the power transfer characteristic described through 2.1 is simple, it does not strictly correspond to the description of DCT as intended in this thesis. The power transfer in the DAB topology is determined by an externally provided setpoint, and not by the relative voltages of the interfaced buses, as is the case in a traditional transformer.

2.3.2 Series Resonant LLC

The second considered topology is the LLC variant of the series resonant converter (SRC), which was first introduced in [65], [66] for a galvanically isolated dc transformer-type application. Reference [67] discusses and develops theory for a non-isolated application, but it is relatively straightforward to extend the presented concepts to isolated topologies. The operating principle of the SRC-LLC is to have a three-element series resonant circuit excited by a rectangular input voltage. Due the the impedance of the resonant tank, the square wave voltage excitation results in in quasi-sinusoidal currents. The topology's voltage transfer characteristic is obtained based on the first harmonic



(a) (b)

Fig. 2.3 a) Single and b) three-phase DAB topologies [63], [64].

approximation [68] and is well known in literature. The approximation is based on power transfer happening only at the converter's tank resonant frequency. As discussed in [68]

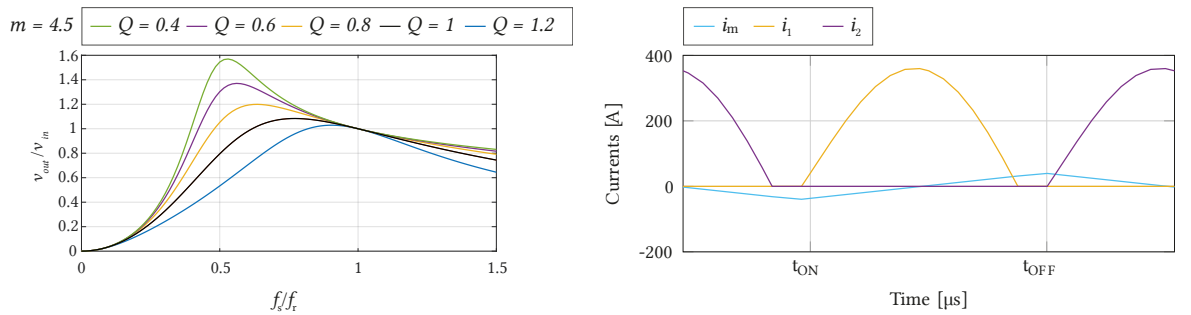
$$\frac{v_{out}}{v_{in}} = \frac{m f_n^2}{(f_n^2(m+1)-1)^2 + (f_n m Q(f_n^2-1))^2} \tag{2.2}$$

where m is the ratio of inductances L_m/L_r, Q is the load parameter given as a the ratio Z_r/n^2R_{ac} between the natural impedance $Z_r = \sqrt{L_r/C_r}$, and the equivalent ac resistance of the load referred to primary. An example of the topology's voltage transfer characteristic is displayed in Fig. 2.5(a). In many low power applications, regulation of output voltage is achieved by varying the switching frequency taking advantage of the relatively linear behaviour of the characteristic around the resonant frequency. The ratio between resonant frequency f_r and switching frequency f_s affects different aspects of the operation of the topology. In many low power application, the ratio between resonant and switchign frequency is used to control output voltage, leveraging the almost linear slope of the transfer characteristic in Fig. 2.5(a) around $f_s = f_r$ [68]–[72]. While this achieves output voltage control, the current level interrupted by the semiconductor devices varies depending on the value of f_s and on load condition. This results in semiconductor switching losses being time-varying and potentially hard to predict, which is not desirable in the envisioned DCT application.

Significantly more interesting for the DCT is the subresonant operating mode. In this mode, the switching frequency is kept constant and such that $f_s < f_r$. Typical waveforms for this operating mode are displayed in Fig. 2.5(b). In subresonant operation, the value of the turn-off current can be set by design and is independent of load, and the transfer characteristic is stiff, guaranteeing almost constant output voltage under load variation. This thesis will only look into subresonant operation of the SRC-LLC, as it is in this condition that turn-off curent is maintained almost constant over the

(a) (b)

Fig. 2.4 a) A bidirectional SRC-LLC topology (shown here with split resonant capacitor) is able to operate in open loop without external setpoint and has a relatively low transformer magnetising inductance compared to the b) LC resonant converter.



(a) (b)

Fig. 2.5 a) An example of SRC-LLC transfer ratio displays has close to unity value in an interval around $f_s = f_r$, which is leveraged in b) subresonant operation of the topology.

operating range of the converter. Of the topologies discussed in this section, the SRC-LLC has the very significant advantage of being capable of leveraging this stiff voltage transfer ratio to allow operation of the converter in open loop. That is to say that no external power setpoint is to be provided to the converter, and the topology's voltage transfer characteristic ensures power transfer similarly to a traditional ac transformer. This is a unique feature of the SRC-LLC and lends itself particularly well to the DCT application which, in principle, is intended to operate without an external power setpoint. Additionally, the topology can operate in ZVS condition across the whole operating range (this is analysed in Chapter 3), resulting in low commutation loss and therefore potentially increased switching frequencies, which are beneficial in terms of reduction of size and weight of the topology's passive component. For this reason, the work of [19] has focused on this topology, which is also further analysed and explored in this thesis.

Although it is particularly well suited to the DCT application, the SRC-LLC has its own drawbacks. First, even in no load condition, a low, constant level of circulating current is present in the topology due to the transformer's magnetising inductance, the value of which is non-negligible. This results in first approximation in constant switching losses over the whole operating range. This results in a minimum level of loss being present in the topology on the primary side even if the load is disconnected, and potentially in relatively low efficiency in low power operation. On the other hand, this represents a trade-off, as this current also allows ZVS operation, which together with the constant turn-off current guarantees almost constant losses over the operating range. Additionally, while for the most part the inductive elements of the resonant tank can be integrated in the MFT, resonant capacitor banks capable of conducting the totality of the load current must be present, increasing the component count.

In spite of these shortcomings, the SRC-LLC still boasts a relatively low component count, simple scalability through series connection of semiconductor devices, and most importantly open loop operation in the DCT application, making it a very viable topology in this context.

2.3.3 Modular Multilevel Converter

The final considered topology is the MMC: initially finding use in the HVdc domain [73], much research effort has been done in the direction of its MVdc applications. One of the main advantages of the topology is how it can be scaled up in voltage by increasing the total number of cells in each branch, and how it can be scaled up in current through the parallel connection of branches [74]. In

ac applications, increasing the number of switching cells has the benefit of allowing the accurate synthetisation of sinusoidal waveforms that significantly reduce, or even eliminate, the filtering needs at the ac terminals of the converter.

As the voltage rating of each cell is significantly lower of that of the overall converter, the use of LV semiconductor devices is possible, without their series connection, which allows the converter to benefit from the strongly reduced switching losses of these devices when compared to discrete MV devices achieving the same blocking voltages. Additionally, when synthesiszing ac waveforms, each cell switches at a frequency significantly lower than what is observed at the converter terminals, with positive impact on its losses. Another benefit is the switching loop being internal to the MMC cell, reducing the amount of electromagnetic interference (EMI) and the required shielding effort.

Finally, the MMC's cell structure guarantees a level of redundancy of the topology. Having additional cells in each converter branch allows for the reduction of the voltage stress on the cells' semiconductors, but additionally allows the bypassing of the cell in the event of a fault, with the remaining cells handling the full dc voltage. The failed cell can then be replaced during the following maintenance cycle [75]. In dc-dc conversion applications, the majority of existing work considers quasi-two-level operation of the topology [76]–[80], where an MFT is induced between an inverter and active rectifier stages generating quasi-square waveforms, therefore resulting in excitation similar to what is present in a DAB topology, as seen in Fig. 2.6. In its quasi-two-level dc-dc conversion arrangement, the MMC can be considered to be a bulk power transfer topology, as it employs a single MFT to achieve power transfer. Nevertheless it still has a highly modular structure, with many of the benefits and drawbacks of fractional power processing topologies.

First and foremost among these, is the topology's complexity, both in terms of hardware and control. In particular, control tasks are split between a central controller for the topology, and individual controllers for each cell, which must independently control each active power device to maintain the dc-link voltage of each cell within safe values. Additionally, the sinusoidal chopped current through each cell's dc-link capacitor is the converter's output current, which at low frequency imposes large capacitance values for each cell [81], [82]. Nevertheless, this is not an issued in the DCT application, as the medium frequency transformer operates at constant frequency, in principle allowing for downsizing of the MMC's cell capacitance. In conclusion, while the MMC is an established solution at the industrial level for HVdc transmission applications, it is not yet a common solution in MVdc contexts [83], [84].

The topology considered for the remaining work presented in this thesis is the SRC-LLC, as in

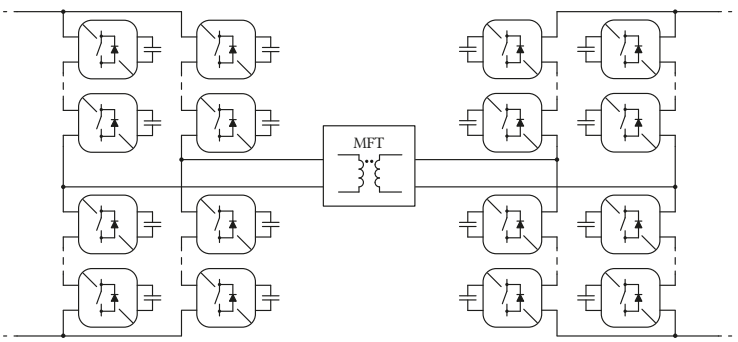


Fig. 2.6 Bidirectional quasi-two level MMC dc transformer.

reference [19] (except for the converter topology, which employs an NPC leg and split resonant capacitor). Thanks to its ability to operate without an externally provided setpoint, the SRC-LLC topology can provide a DCT which can truly perform a role which is equivalent to that of an ac transformer in an ac network.

2.4 MV Semiconductor Devices in DCT Applications

Having identified the SRC-LLC topology as the most beneficial based on the criteria put forward in the above section, the relative advantages and disadvantages of MV semiconductor devices are explored to justify another choice made in this thesis. Over time, many semicondcutors have found application in the field of high-power MV conversion. These have included line-commutated silicon controller rectifiers (SCRs), gate turn-off thyristors (GTOs), and injection-enhanced gate transistors (IEGTs), but two most common devices today are the Si insulated-gate bipolar transistor (IGBT) and integrated gate-commutated thyristor (IGCT).

2.4.1 IGBT

Of the two mentioned devices, the IGBT has been the object of a significantly larger volume of research in the past decades: the device has been considered by many authors [88]–[94], in both hard and soft-switched applications [88]–[90], [95], with voltage ratings of 3.3 kV [95] and 6.5 kV, and with varying levels of electron irradiation to control carrier lifetime in [88], [89], [94]. 6.5 kV devices were also explored in soft-switched applications [90]–[92], with optimisation by means of anode engineering being presented in [93], and resulting in a reduction of switching losses, beneficial for fast-switching applications.

In contrast to BJTs and thyristors, IGBTs are voltage controlled semiconductors switches which can be turned ON and OFF by gate driver action, making them fully controllable devices.

Thanks to its ease of drive and good switching characteristics, the IGBT has progressively found its place among the most popular semiconductor devices nowadays. The device also has the additional benefit of allowing tuning of its switching performance through the alteration of the gate resistance,

(a) (b) (c)

Fig. 2.7 a) IGBT dies [85] leave unused space reducing the total surface in contact with the press-packed device compared to the b) GCT wafer [86]; c) GCT integrated into the drive unit [87].

(a) (b)

Fig. 2.8 a) 6.5 kV rated module containing two IGBTs in common emitter configuration [96]; b) Ceramic press-pack IGBT with top surface being the emitter side of the device [97]

providing an additional degree of freedom in design and allowing for clampless operation in hard switching topologies. GDUs may have different values of gate resistors which can be selected and employed depending on the needed performance altering the duration of switching transition and enabling faster or lower switching, or limitation of short circuit current. In spite of these many advantages, the IGBT performs less favourably than thyristors or IGCTs in the same voltage class in terms of forward voltage in conduction.

In MV applications, the typical voltage classes are 4.5 kV and 6.5 kV, with current ratings of 900 A and 1200 A [98]. These devices allow junction operating temperature of up to of 125 °C and typically occur in module packaged IGBTs with plastic housings with insulation ratings of 7.2kV and 10kV for the respective voltage classes mentioned above.

The module's power terminals lead inside the housing and are at the potential of the emitter and collector of the chips located within the module's housing. Normally, IGBT chips are bonded to the metalized (Cu) ceramic substrate and soldered to an Aluminium Silicon Carbide (AlSiC) baseplate serving as the bottom metallic base of the modules [99]. Depending on requirements, packages can host one or more chips and can exist including or not including antiparallel diode chips.

The chips are supported by AlSiC plates which act both as a hard mechanical support and as a thermal interface between the module and heatsink, which can rely on air or water cooling for lower and higher power levels, respectively [100], [101].

The thermal interface between module and heatsink is always treated with thermal paste to provide improved and uniform heat extraction. The connection of chips to bus bars is achieved through wire bonds which are soldered or sintered to the chip on one side, and to the respective etched copper plating of the substrate on the other [102], [103]. The bus-bars connect to their part of the copper plate, realising a sturdy connection to the terminals. A silicon gel fills the inside of the module to improve electrical field distribution and limit the likelihood of flashovers. It is also possible to integrate other elements such as temperature sensors inside the module.

A relatively common issue in IGBT modules is the failure of wire bond connections related to thermal cycling [104], [105]. Different thermal expansion coefficients may lead to the wire bonds lifting and detaching, damaging connections to the power terminals. The introduction of the press-pack partially solves this problem, and was the package of choice for high power, high voltage thyristor switches and diodes before the introduction of the IGBT. The press-pack is designed for harsh environments like the ones found in smelting plants or mines, and as the application of the IGBT in these environments

became more common, so did IGBTs housed in this package.

The housing is made of insulating hard ceramic with the addition of pressure power contacts on both top and on the bottom. The thermal and electric contacts to the chips is achieved through copper discs in the role of contact plates, extending into the package [106], [107]. Thin Molybdenum (Mb) rectangular plates cover both sides of the chip and this plates come in direct contact with the emitter and collector carved Cu discs. This combination helps to greatly improve the thermal cycling capability of the IGBT chips within, the thermal expansion coefficients of Si and Mb being very similar. The majority of the compression and shear stress is transferred to the Mb. The interior of the package can be filled with inert gases such as SF_6 to improve electrical field distribution.

In contrast to the module package having single-sided heat extraction, both sides of the chips present in press-packs are cooled. Press-pack IGBT are mounted between two heat sinks and the assembly is held together by the pressure provided by the external mechanical clamp. The most common mechanical implementation is in a stack of alternating heat sinks and IGBTs/diodes, at least in the case of a switching bridge or a phase leg of the converter. The pressure terminals help greatly in thermal energy extraction from the chip because of the massive and even contacts realized between Cu, Mb and Si.

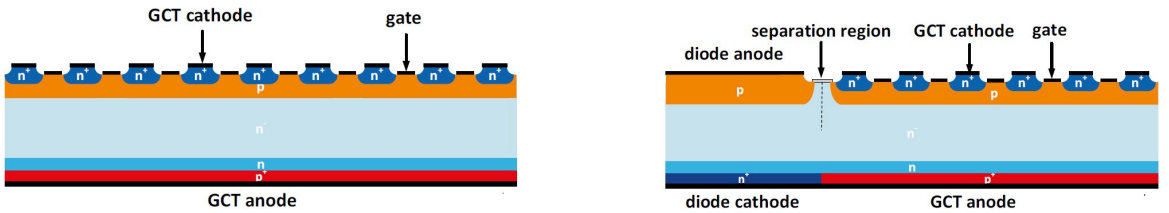
Nevertheless, press-packs also have less advantageous features: firstly, compression forces applied on the housing must not exceed a specified range in both in cold or hot state of the switch, to avoid mechanical damage to the switch. Secondly, pressure on the package must be applied evenly from the centre to the sides to ensure adequate electrical and thermal contact and guarantee that no individual die undergoes excessive stress during thermal cycling. For this reason, extreme care must be taken in the manufacturing of the contact surfaces of the press-pack, specifically the flatness of the finish, which results in increased manufacturing costs. Similarly, this must be achieved also for the heatsink with which the package is interfaces, which are also required to be exactly parallel to each other.

The pressure distribution problem can be tackled by using spring contacts inside the package, which can even out external pressure variations over the surface of the contact. The drawback of this solution is that the thermal interface to the one side of the package is broken, increasing the thermal resistance between the IGBT dies and the heat sink. Due to the prevalence of this package in high power applications, in the vast majority of cases water cooling is employed, with air cooled solutions constituting a small minority of use cases.

Voltage classes higher than 4.5 kV, are not frequent due to the easy series connection achieved through the stacking of devices. Current ratings go up to 3 kA for most IGBT packages, but with relatively low switching frequencies of up to 1 kHz which are typical in high power applications.

ISOP connection of modules resulting in modular topologies are quite common, leveraging the use of relatively affordable LV devices for MV applications. Similarly, the series connection of the IGBTs is also common in order to reach the required voltage ratings, but at the price of reduction efficiency due to snubber circuits. Concerning resonant operation, the IGBT is characterised by increased turn-off energy loss compared to equivalent hard-switching operation. Due to the different profiles of the pre-flooding current of the IGBT, more carriers are generated during the resonant cycle, having to be extracted, as discussed in [93].

Another device leveraging the benefits of the press-pack and with conduction losses comparable to those of the high power thyristor, the IGCT is another device seriously competing with the IGBT in



(a) (b)

Fig. 2.9 a) In asymmetric IGCTs, IGCT fingers cover the full surface of the wafer; b) in reverse conducting IGCTs, the central portion of the wafer is allocated to the device's antiparallel diode [111].

high power MV applications.

2.4.2 IGCT

In comparison to the IGBT, the IGCT exhibits specific advantages over the more popular device in certain applications: its thyristor structure guarantees best-in-class conduction losses among fully controllable devices, and with relatively similar turn-off energies compared to the IGBT.

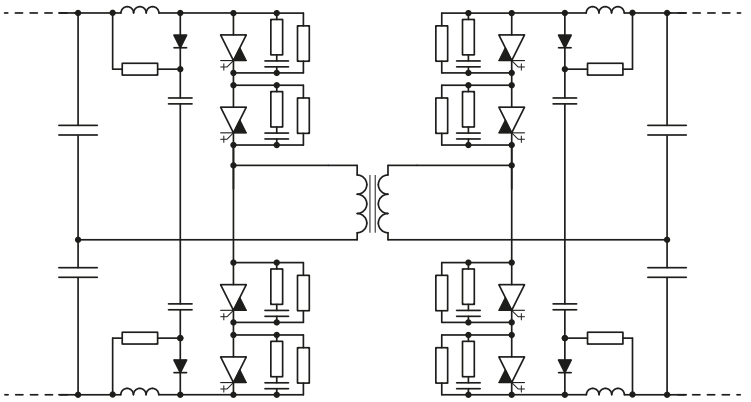
In conventional hard-switched applications, where the IGCT has traditionally found application, turn-on losses are normally neglected due to the use of a clamp circuit that protects the devices' antiparallel diode at the time of commutation, as seen in Fig. 2.10. This shifts the switching loss from the devices themselves to the clamp circuit. In a similar application, the turn-on of the IGBT can be better controlled through gate driver action and therefore a clamp circuit is not needed, therefore with the corresponding energy being dissipated in the device. For this reason the comparison between the devices is not straightforward, even though [108] has not found significant difference in overall system losses by using IGBTs with a clamp circuit.

In terms of rating, traditional uses of the IGCT have leveraged its high surge current capabilities and achieved switching frequencies usually at or below 1 kHz. Reference [109] uses 4.5 kV, 2.1 kA IGCTs, to achieve a rating of 1.5MVA using just two devices in a half-bridge configuration. In more recent years, advances in the technology have focused on increasing the power density by reduction of losses, increase of the maximum operating temperature, and maximisation of the device's peak turn-off current. Additionally blocking voltages of up to 10 kV have been achieved, though not yet in commercially available devices [110].

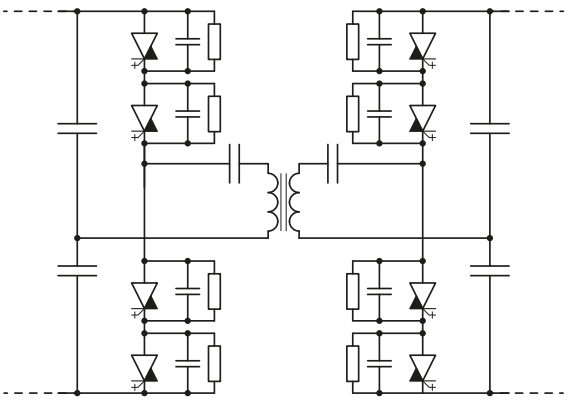
The first commercial application of the IGCT was a 100 MVA back-to-back rail intertie in operation in Germany since 1996 [112]. The device has subsequently found use in a number of high power medium voltage installations and today exists in three distinct types, all of which, due to their high power ratings, are only available in the press-pack form: asymmetric, reverse conducting, and reverse blocking. Typical voltage ratings for all of these devices are of 4.5 kV, 5.5 kV and 6.5 kV.

As described in Fig. 2.9, asymmetric IGCTs are capable of blocking forward voltage, but have very low reverse blocking capability (only around −20 V). This kind of device is intended for use in combination with an external discrete antiparallel diode. Asymmetric IGCTs achieve the highest available current rating: devices up to 6 kA are commercially available.

Reverse conducting IGCTs integrate the anti-parallel diode on the same Si wafer as the IGCT and it is therefore not necessary to employ external discrete diodes, This reduces overall component count,



(a)



(b)

Fig. 2.10 a) In most hard-switched applications both a clamp circuit and snubber resistor are required, but can be omitted in b) a soft-switched SRC-LLC topology.

but since part of the Si wafer area is occupied by the integrated diode, the overall surface available for GCT fingers is reduced when compared to an asymmetric IGCT of the same diameter. As a result, reverse conducting IGCT generally have comparatively lower turn-off current ratings of up to 2 kA. The devices employed in the rest of this thesis are all reverse conducting IGCTs.

Finally, symmetrical IGCT are capable of blocking both forward and reverse voltages, but at the price of decreased current ratings due to the increased wafer thickness needed for this capability resulting in increased conduction losses and more restrictive thermal limitations. The main application of symmetrical IGCTs are current source converters. GCTs are composed of multiple fingers arranged circularly in ring structures over the surface of the wafer. The central ring in the Fig. 2.8(b) is the gate terminal of the switch, while cathode and anode are on the top and bottom, respectively.

The high current rating of the device is in part achieved thanks to the GCT fingers being able to cover the entire surface of the wafer, therefore aiding thermal conduction to the top and bottom Cu package covers, especially compared to the press-pack IGBT. This results in IGCTs generally exhibiting lower

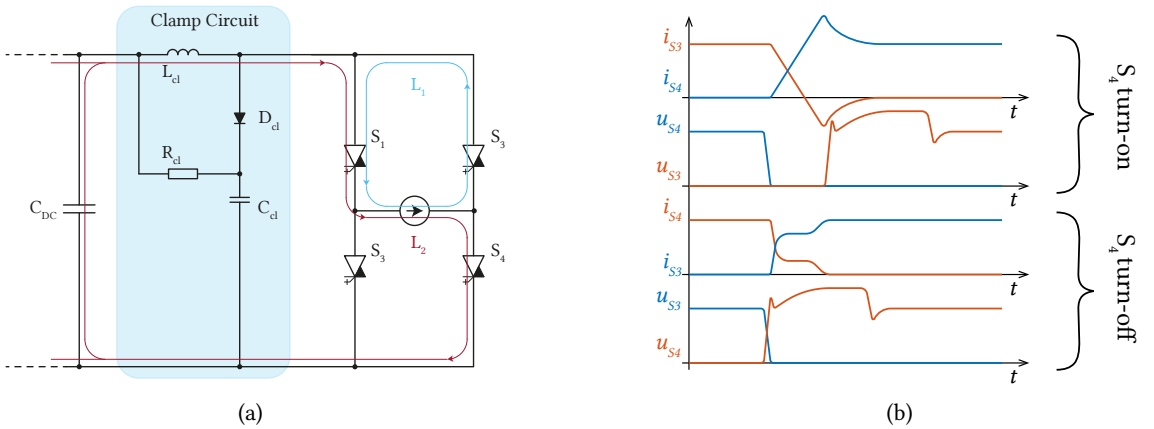


Fig. 2.11 a) IGCT clamp circuit with highlighted current paths and b) waveforms at turn-on and turn-off of S_4 [19].

junction-to-case thermal resistance for the same package size. This allows relaxed cooling constraints or increased the thermal excursion margin of the junction. Cooling is achieved on the both sides of the package through anode and cathode contacts.

An IGCT is a current driven device, owing it to the thyristor structure of the semiconductor. One of the benefits of current drive is an increased resilience to EMI, but at the cost of increased gate driver power consumption. At turn-off, the entire anode current is commutated from the collector to the gate driver. Therefore, increased turn-off current capability corresponds to an increased number of gate driver capacitors, which can be seen in Fig. 2.7(c) in black. These capacitors provide a stable voltage source during turn-off necessary for the commutation of the current. Due to the high current levels involved, it is also necessary that the inductance between the gate driver unit and the GCT is minimised, which can be achieved through wide parallel multilayer traces of the terminals, leading to the integration of the GDU with the GCT. Hence, the name of *Integrated Gate Commutated Thyristor*.

Unlike the IGBT, IGCTs generally cannot turn-off short circuit currents. Nevertheless, IGCTs are characterised by higher short circuit withstand capability and higher limiting load integral. The high thermal tolerance of the device allows relatively slow, external breakers or fuses to be employed for protection in case of short circuit.

Another difference compared to the IGBT is the inability of the rate of change of current in the IGCT to be controlled by the gate driver. For this reason, an external clamp circuit must be present to protect the anti-parallel diodes from damage due to excessive di/dt. Typical clamp circuits are visible in Fig. 2.10(a).

The typical switching process in presence of a clamp circuit is visualised in Fig. 2.11. At the beginning of the process and before the turn-on of S_4, the flow of load current is though the loop L_1 in Fig. 2.11(a). S_1 is on, S_3's antiparallel diode is conducting the load current. The voltage on the load is of 0 V. For the load to be supplied with positive voltage, S_4 is turned on. The voltage on the terminals of the device decreases to 0 V and the clamp inductor current rises with starting value equal to 0 A. The rate of change of the current in the clamp inductor is limited to $U_{C_{dc}}/L_{cl}$, and L_{cl} is designed based on the di/dt capabilities of the antiparallel diodes.

The current in i_{S_3} starts to fall gradually as the current in L_{cl} progressively rises with the safe and

limited di/dt; this can be seen in the top graph of Fig. 2.11(b). The reverse recovery process of the antiparallel diode of S_3 starts after the current in S_3 crosses 0 A. The voltage across S_3 starts to build-up as the junction of the diode is free of charge carriers and the depletion region progressively forms, which is shown in the second graph of Fig. 2.11(b). The effect of the reverse recovery can also be observed in the form of a current overshoot in S_4.

Up until the time when the current i_{S_4} reaches its maximum, currents i_{S_4} and $i_{L_{cl}}$ are equal. After i_{S_4} reaches its maximum, $i_{L_{cl}}$ is greater than the load current and the excess starts flowing into the clamp capacitor C_{cl} through the diode D_{cl} until the $i_{L_{cl}}$ becomes equal to the load current. Observing u_{S_3}, one can see the overvoltage resulting the voltage of C_{cl} exceeding the dc-link voltage during the equalisation of the currents. C_{cl} is later discharged through R_{cl} until the voltage at its terminals reaches the voltage of the dc-link, which is blocked by S_3.

The turn-off of S_4 can be seen in the bottom two graphs of Fig. 2.11(b). Initially, the current decreases, and after it is extinguished the load current is commutated to the antiparallel diode of S_3. Upon S_3 starting to block, the current $i_{L_{cl}}$ is commutated into C_{cl} which stores the magnetic energy initially contained in L_{cl} and returns it to the dc-link. During this process, S_3 experiences an over-voltage up until when the voltage of C_{cl} has returned to the dc-link voltage value.

A significant benefit of the clamping circuit is negligible turn-on energy loss of the IGCT. The overall conversion efficiency benefits greatly from this virtually lossless turn-on process.

Compared to the IGBT, the IGCT has lower voltage drop during conduction due to its thyristor nature, resulting in lower conduction losses. Concerning switching, turn-off energy for the two devices is comparable. The reduction in cooling effort related to the IGCT's reduces conduction losses leads to lower cooling requirements for the final converter in terms of space and cost.

The application of the IGCT in resonant applications has been mostly overlooked, with the work reported in [113], [114] being somewhat unique. Nevertheless the benefits from the use of the device in resonant applications are significant, as discussed in [19]. In particular, in the SRC-LLC discussed in this thesis the IGCT would operate in unique conditions beneficial for the device: the reduction of both turn-on (ZVS) and turn-off (low-current) losses achieved through the soft-switched topology increase the benefit of the device's low conduction loss. Additionally, clampless operation becomes possible thanks to the absence of terminal voltage on the device at the time of turn-on, and finally becasue of the low turn-off current a significant reduction of gate drive effort has been shown to be possible in [115], which sidesteps the high level of energy dissipation in the gate drive circuit that has traditionally been one of the most frequently identified drawbacks of the IGCT.

Therefore, while the IGCT is a less commonly used technology and there is little precedent for its use in MVdc DCT applications, there is relevant research interest in exploring whether the expected benefits of the device can be exploited in such an application. For this reason, the device is selected to be used in the application discussed in the thesis over the IGBT.

2.5 Series Connected Operation of IGCTs

While no standard voltage levels are currently defined, MVdc networks are expected to exist with voltage ratings of up to 50 kV in monopolar networks, and ±50 kV in bipolar networks. Ratings of commercial IGCTs today do not exceed 6.5 kV, and therefore series connection of the device is

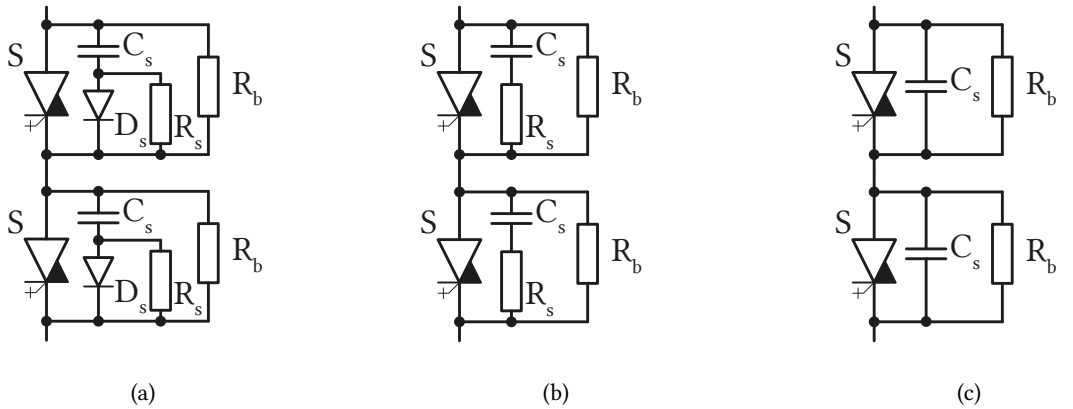


Fig. 2.12 Series connected RC-IGCTs with a) RCD; b) RC; c) C parallel connected snubber for dynamic voltage balancing. Resistor R_b provides static voltage balancing.

required for use in bulk power transfer MV applications.

Indeed, series connection of IGCTs has been of interest almost since the device was first made available, allowing the increase of installed power ratings by a factor similar to that of the number of series connected devices [116]–[118]. In series connection, the most critical part of the period is that of device turn-off, when the dc voltage needs to build up at the terminals of the device and be correctly shared with the other devices connected in series. This is to happen in the limited duration of the dead time.

In traditional hard-switched applications, well-known RCD ot RC snubbers can be employed, as seen in Fig. 2.12(a) and 2.12(b). Upon the turn-off of the IGCT, remaining energy stored in the circuit inductance is transferred to C_s which quickly charges as voltage builds up on the switch terminals. Resistor R_s ensures that as the IGCT is turned *ON* again, the energy stored in C_s is dissipated gradually. If needed, R_s can be bypassed with the use of a diode D_s so as to not affect the charging of C_s. Resistor R_b provides static voltage balancing and as a rule of thumb is sized to conduct a current approximately ten times larger than the IGCT leakage current in its blocking state. In hard switched applications, values of snubber capacitance C_s can reach up to 1 µF [119]. Such relatively high capacitance values are not an issue in this case, since turn-off currents are potentially in the range of several kA and ensure very fast charging of the snubber capacitances. Nevertheless, when the current is reduced as is the case in the proposed LLC topology, large capacitance values are not suitable, as the low turn-off currents are not able to charge the snubber capacitances quickly enough.

A significant part of the work presented in this thesis is motivated by the current lack of publications and documentation on the effect of ultra-low turn-off current on voltage sharing of series connected IGCTs. References [113], [114] have explored the behaviour of the IGCT in soft-switched conditions, but with a focus on the ZVS turn-on aspect, which is not critical in the context of the SRC-LLC topology.

Finally, traditional hard-switched applications also require the use of snubber resistors in series with the snubber capacitance to avoid inrush current due to the snubber capacitor discharge at the moment of the devices' turn-on. Due to the soft switching conditions present in the discussed DCT topology, it is investigated how snubbers can be reduced in both size and cost by omitting resistor R_s and

reducing the snubber capacitance values to the range of a few tens of nF, as seen in Fig. 2.12(c). This is also relevant to the functionality of the topology, as the low turn-off currents present in SRC-LLC operation are insufficient to quickly charge the snubber upon turn-off.

2.6 Soft-Switched MV Applications

As already discussed in this section, MVdc application usually employ semiconductors of voltage ratings at and above 3.3 kV in hard switched operation and at relatively low switching frequencies of a few hundreds of Hz. Nevertheless, in applications involving magnetics components like the DCT, it is attractive to increase the switching frequency so as to reduce their size. But an increase of switching frequency naturally increases the switching losses, if the operating conditions of the device do not change. An effective way of doing so is to achieve soft switched operation, significantly reducing the current or voltage stresses on the device at the time of turn-off and turn-on.

The LLC resonant dc–dc converter discussed in this thesis has been considered in a wide range of applications thanks to its many benefits. Nevertheless, most of the published work focuses on relatively low power applications based on MOSFETs and achieving switching frequencies in the range of hundreds of kHz [69], [120]–[127].

At the MV level, in terms of semiconductor devices, as discussed in 2.4, IGBTs, IGCTs, and more recently SiC MOSFETs are the preferred technologies. The challenge in this context is prevalently the use of semiconductor devices outside of their traditional operating conditions, increased operating frequency being required to achieve high power density. References [128]–[130] have reported on the 1.2 MW power electronics transformer (PET). The converter uses 6.5 kV and 3.3 kV IGBTs and encounters the issue that, as for most MV devices, the IGBTs are optimised for reduced conduction loss, as most applications at this voltage level employ low switching frequencies. The references tackle this issue with a two-pronged approach of the use of a resonant topology in combination with carrier lifetime adaptation to achieve reduced switching loss at the expense of increased forward voltage.

Generally, there is relatively little work on the topic of MV IGBTs used in medium-frequency-operated LLC resonant converters. In addition to [128]–[130], which uses an LLC topology, [88]–[90], [95] present a series resonant LC topology using 3.3 kV IGBTs switching at 8 kHz additionally exploring 6.5 kV IGBTs exhibiting reduced carrier lifetime and reporting a reduction of switching losses of up to 30 % compared to standard devices. Here, ZCS conditions are used due to the natural characteristics of the LC resonant tank, where there is no magnetising inductance small enough to result in a significant device turn-off current at the end of the period. This results in a different loss pattern, where both turn-on and turn-off losses are present in the devices due to the stored charge being cleared at the time of the complementary device turn-on. Additionally, an example of use of 6.5 kV IGBTs in a soft-commutated converter is presented in [131], [132], where non-dissipative snubbers allow the increase of switching frequency.

The use of SiC devices has also been considered as another way of increasing the switching frequency in medium-frequency applications. In [133] and [134], the authors consider the use of SiC diodes and 10 kV SiC MOSFETs, respectively. The work presented in [135] employs SiC MOSFETs in a 1.6 kV laboratory-scale system combining SiC with soft-switch operation, while in [136] experimental results are presented at the 1 kV level achieving soft switching both at turn-on (ZVS), and at turn-off (ZCS).

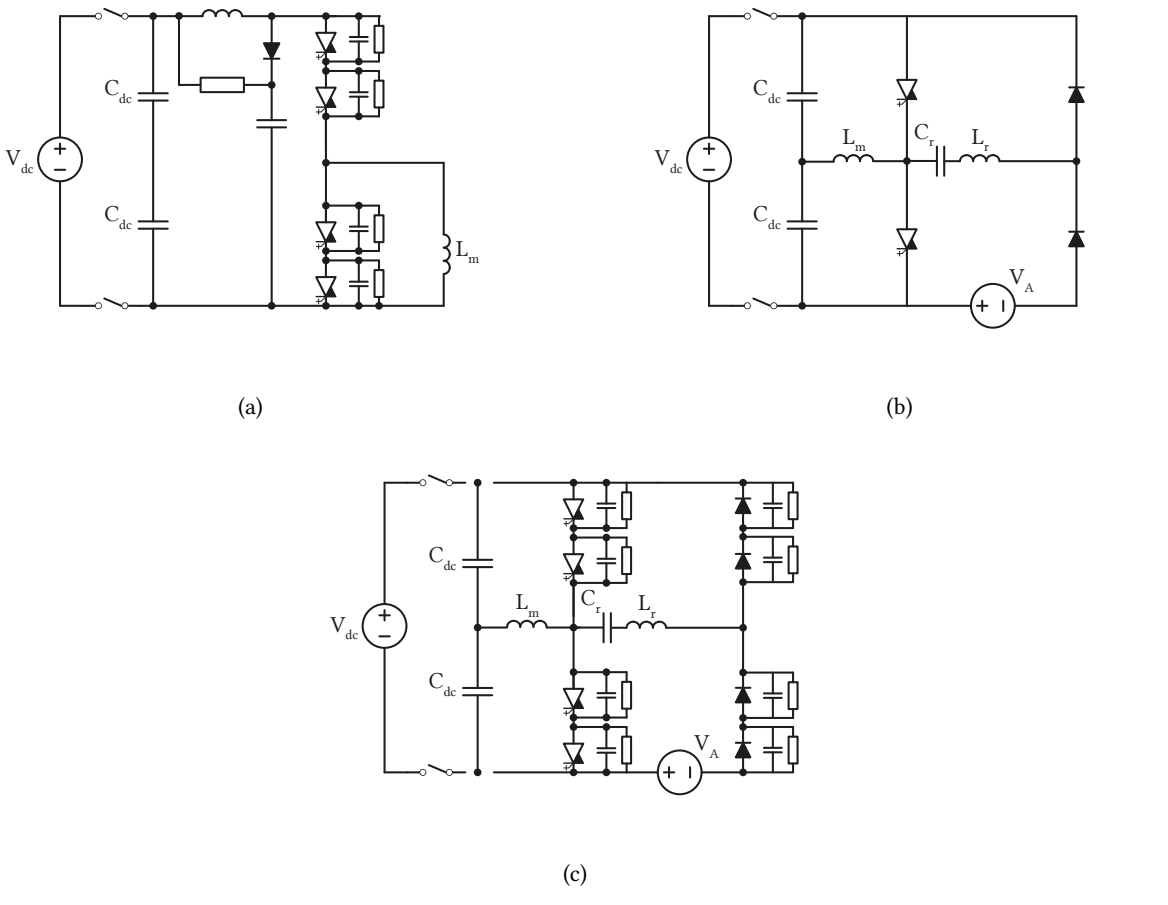


Fig. 2.13 The flexible test setup can be configured to perform a) double pulse (DP) tests, and pulsed and continuous resonant tests with b) individual or c) series connected devices.

Concerning IGCTs, the number of reported soft-switched applications is minimal. Specifically, no industrial applications of such kind are reported, and even in academic environments only a few examples exist. The use of IGCTs in the DAB DCT configuration has been reported in [113], [114] at a power level of 5 MW and voltage of 5 kV. The installation achieves a switching frequency of 1 kHz and due to the nature of the topology achieves soft switching in a significant portion of its operating range, that is to say for a significant amount of the possible load angle to load combinations. The references also specifically explore the soft turn-off of 91 mm asymmetric IGCTs with different devices characterised by varying turn-off energy and forward conduction voltage combinations, and finding loss reduction in both conduction loss and switching loss optimised devices.

In terms of resonant operation of IGCTs, [86], [137] have explored the unique switching conditions characteristic of the SRC-LLC topology and in particular the effect of low-current turn-off on the switching performance of the reverse-conducting IGCT (RC-IGCT). Additionally, the effect of current pre-flooding is considered and the increased duration of the turn-off quantified. Thanks to these results [19] is able to demonstrate operation of the IGCT in resonant conditions in a half-bridge configuration at a frequency of several kHz.

Fig. 2.14 The flexible test setup [19] allows for different configurations to evaluate the performance of the semiconductor devices under varying operating conditions.

This thesis expands on the work of [19] by comparing IGCT turn-off and turn-on in both ZVS and ZCS conditions, extending the result to series connected IGCTs, and demonstrating series connected resonant operation at the unprecedented frequency of 5 kHz and estimating the semiconductor losses in such operating conditions for devices having underwent varying levels of electron irradiation.

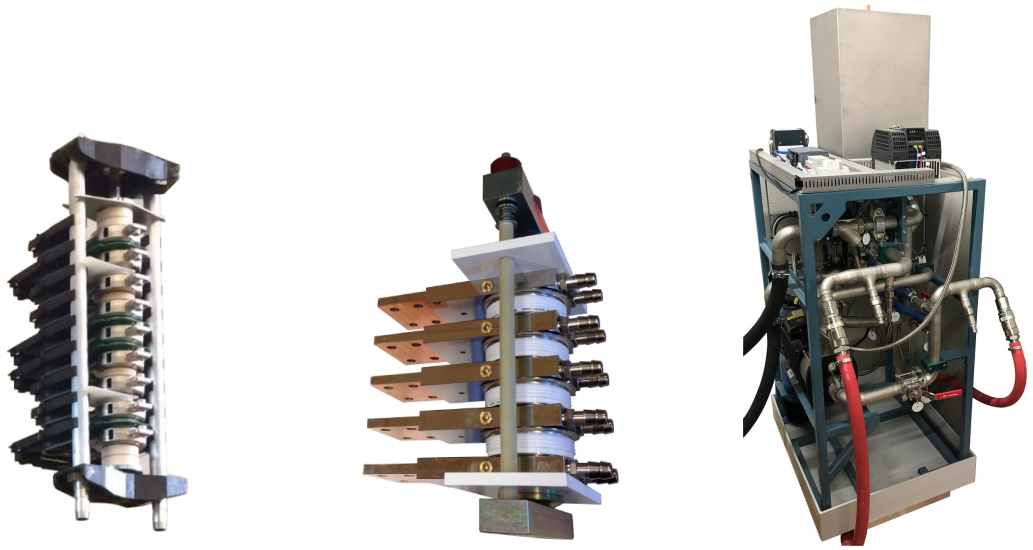
2.7 IGCT Characterisation Test Setup

The experimental verifications presented in the following chapters of this thesis are based on the test setup presented in [19], [86], [137]. This test setup, displayed in Fig. 2.14, is highly flexible and can assume different configurations to achieve different current and voltage stresses on the tested semiconductors. In this thesis, three configurations of the setup are employed, displayed in Figs. 2.13(a), 2.13(b), and 2.13(c). Each of these allows the testing of the semiconductors under specific conditions. Namely, Fig. 2.13(a) is a standard series-connected DP configuration, with the bottom two devices being the devices under test (DUTs), Fig. 2.13(b) allows the operation of the RC-IGCTs under resonant conditions, and can be used for either pulsed resonant tests or continuous resonant operation, and finally Fig. 2.13(c) allows similar resonant operation, but with series connected devices and therefore their relative static and dynamic voltage sharing snubbers. While the operation of each of these configurations is not described in this section, it is discussed in detail at the beginning of the respective chapter where the configuration is employed.

The power semiconductors present in the setup are arranged in two separate stacks. The RC-IGCTs are placed in an NPC stack sourced from a water cooled ABB ACS1000 drive, which is displayed in Fig. 2.15(a). The freewheeling diodes are placed in the custom-built stack in Fig. 2.15(b) and share the deionised cooling water circulated by the water cooling unit (WCU) in Fig. 2.15(c) with the IGCTs. The action of the semiconductors is controlled by an ABB AC 800PEC which is interfaced with multiple digial inputs and outputs, and voltage and current sensors through COMBI IO and PECMI units, respectively, which are displayed in Fig. 2.17. Even though sensing of the device currents and

Tab. 2.1 Design values of main components of the test setup.

V_{dc}	V_A	C_{dc}	L_m	L_r	C_r
2.5 kV-5 kV	0 V-20 V	1.3 mF	0.65 mH-5 mH	3.75 µH-15 µH	85 µF-680 µF



(a) (b) (c)

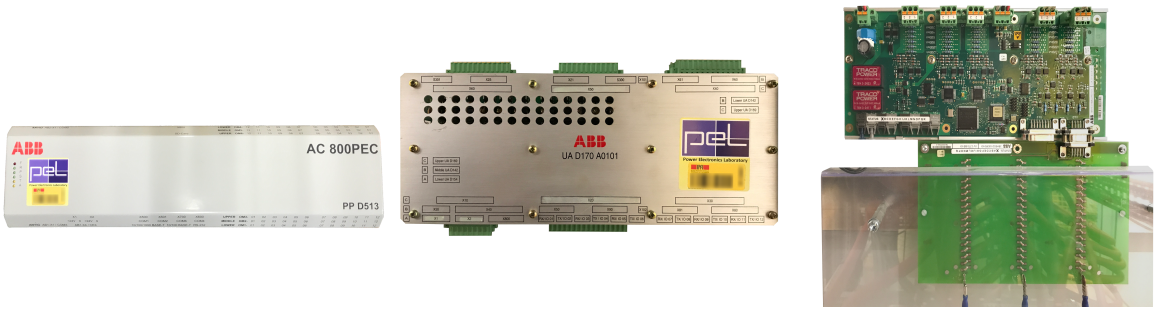
Fig. 2.15 a) *ACS1000* water cooled IGCT stack containing the DUTs; b) Custom-built diodes stack sharing with the IGCTs the deionised cooling water circulated by the c) WCU.

(a) (b) (c)

Fig. 2.16 a) Magnetising inductor employing amorphous alloy core; b) Configurable array of eight air core resonant inductors; c) Resonant capacitor bank with displaceable bus bars.

voltages is available, the setup is operated in open loop during all the testing phase and results are gathered with external voltage and current probes.

To achieve both DP and resonant operation, the setup employs configurable values of magnetising inductance L_m, resonance inductance L_r, and resonant capacitance C_r. These components are displayed in Figs. from 2.16(a) to 2.16(c), respectively. The inductance L_m employs an amorphous alloy core,



(a) (b) (c)

Fig. 2.17 The *AC 800PEC* controller is interfaced to digital inputs and outputs through the b) *COMBI IO* and to voltage and current sensors through the c) *PECMI* unit.

and allows configurable values of inductance depending on the terminals used for connection and the corresponding number of turns. Due to the peak values of resonant current being expected to be significantly larger than the magnetising current, the inductance L_r is obtained by the parallel and series connection of a number of air core inductors. Eight inductors are present and each has a value of inductance of 30 µH. These are connected directly in series with the capacitor back right above them (as see in Fig 2.14), which contains eight high current capacitors which can be paralleled through the displacement of a copper bus bar so as to include the correct amount to achieve the desired resonant frequency, in combination with L_r. The numerical values of the components are listed in Tab. 2.1. Note that these are the design values of the components. The true values do not always coincide with the design values, and this is addressed in the relevant chapters.

2.8 Summary

This chapter has laid out a number of options which can be considered for DCT applications, in terms of topology, semiconductors, and switching behaviour. Among these many options, the SRC-LLC topology has been selected mainly due to its simplicity, low component count, and ability to effectively provide a dc equivalent of the traditional ac transformer in ac networks, operating without being provided with an external setpoint. In terms of semiconductors, RC-IGCTs are selected as the device of choice, with the intent of exploiting the low conduction losses of the device in combination with the soft-switching conditions determined by the use of the SRC-LCC topology. To achieve the required voltage levels, the IGCTs are series connected, with voltage sharing during low current turn-off of the devices being highlighted as a point requiring further investigation. Finally, the flexible test setup presented in [19] is described, anticipating how it will be employed to determine optimal switching conditions for the RC-IGCTs in resonant operation.

3

IGCT Commutation in ZVS and ZCS Conditions

The identification of minimal loss switching conditions is a necessary step to achieve the increase of IGCT switching frequency to the several kHz *required for the targeted DCT application. To this end, the selected SRC-LLC topology offers degrees of freedom in terms of the devices' turn-off current magnitude and the duration of the dead-time. This chapter gives an overview of the subresonant operation of the LLC-SRC topology, and then proceeds to identify the key mechanisms behind the IGCT switching losses in this operating mode, identifying threshold ZVS conditions as resulting in minimal switching losses.*

3.1 Introduction

As devices employed in MV conversion and power levels of several MW, IGCTs have relatively high current and voltage ratings. When the device operates close to the limits of its SOA and in hard-switched conditions, the commutation result in relatively high switching energy due to levels of turn-off current in the range of up to several kA. The LLC-SRC topology operated in subresonant mode provides the device with soft-switching conditions across the whole rated operating range of the converter, therefore very significantly reducing switching losses. The exact nature of these soft-switching conditions is determined by the combination of dc-link voltage and passive components of the converter, and trade-offs exist between soft turn-on and turn-off conditions. The operation of the LLC-SRC topology, and in particular the case of a half-bridge inverter leg, is analysed here. Then, the trade-offs existing between turn-off current level, dead-time duration, device electron irradiation and commutation losses are evaluated.

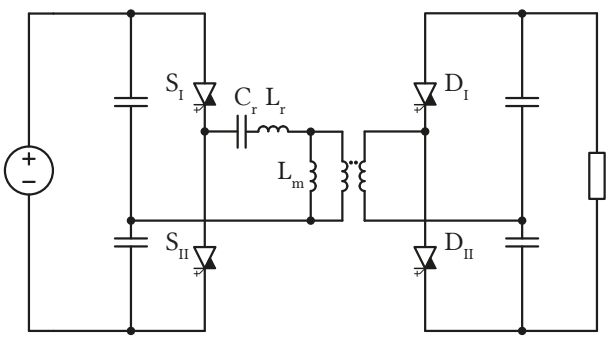


Fig. 3.1 SRC-LLC topology with resonant tank brought to the transformer primary.

3.2 IGCT Switching Frequency Limitations and Employed Devices

As discussed in Section 2.4, the IGCT has traditionally found application in hard-switched topologies operated with low (<kHz) frequencies. In these applications, the limitations that prevent an increase of switching frequency for the device (>1 kHz) can be synthesized as:

1. Minimum turn-on time requirement of the device: it is required to have a minimum t_{on} time (typically >40 µs) to make sure that the device is fully turned-on homogeneously throughout the wafer, which in turn impacts the device turn-off.
2. Minimum transient time requirement of the clamp circuit: a certain minimum time is required (> 10 µs) between switching transients to make sure that the clamp capacitor is discharged, and clamp diode is turned-off completely.
3. Turn-off switching losses: In high switching frequency applications (>1 kHz), relatively high E_{off} causes the device to exceed its operating junction temperature resulting in a thermal limitation.

The first two limitations are intrinsically overcome in LLC-SRC operation. Firstly, there is no minimum turn-on time as the device turn-off occurs at ultra-low current level, and therefore does not affect the turn-off SOA. Secondly, there is no limitation linked to the discharge of the clamp capacitor, as the rate of current increase in the topology is limited by the resonant inductor itself, and therefore no clamp circuit is necessary.

This and the following chapters consider the use of three devices: a commercially available 4.5 kV, 68 mm RC-IGCT device, and two custom engineering samples. The three design variants differ by the homogeneous lifetime control done through electron irradiation. The reference device is the commercial device with standard electron irradiation. This design is optimized for typical hard-switched, sub kHz applications. Devices referred to as *Irraditated A* and *Irradiated B* are subjected to higher electron irradiation to increase the switching speed and to be used in high frequency applications. These devices have 55 % and 95 % higher irradiation than the standard devices, respectively.

The technology trade-off of these three designs is compared under hard-switched conditions (i.e. at high turn-off current and high dc-link voltage) using classical half bridge test configuration with clamp circuit. As shown in Fig. 3.2(a), the increased irradiation reduces the turn-off energy losses at at turn-off current of 1.1 kA by 22 % and 29 % in *Irradiated A* and *Irradiated B*, respectively. However, the on-state voltage at the same current level of 1.1 kA increases by 23 % and 39 % in *Irradiated A* and *Irradiated B*, respectively, compared to standard devices. The improvement in switching performance with higher irradiation (*Irradiated B*) has, as expected, a larger trade-off on the on-state voltage under hard-switched conditions. The effect of these differences in high frequency operation are discussed later in this chapter.

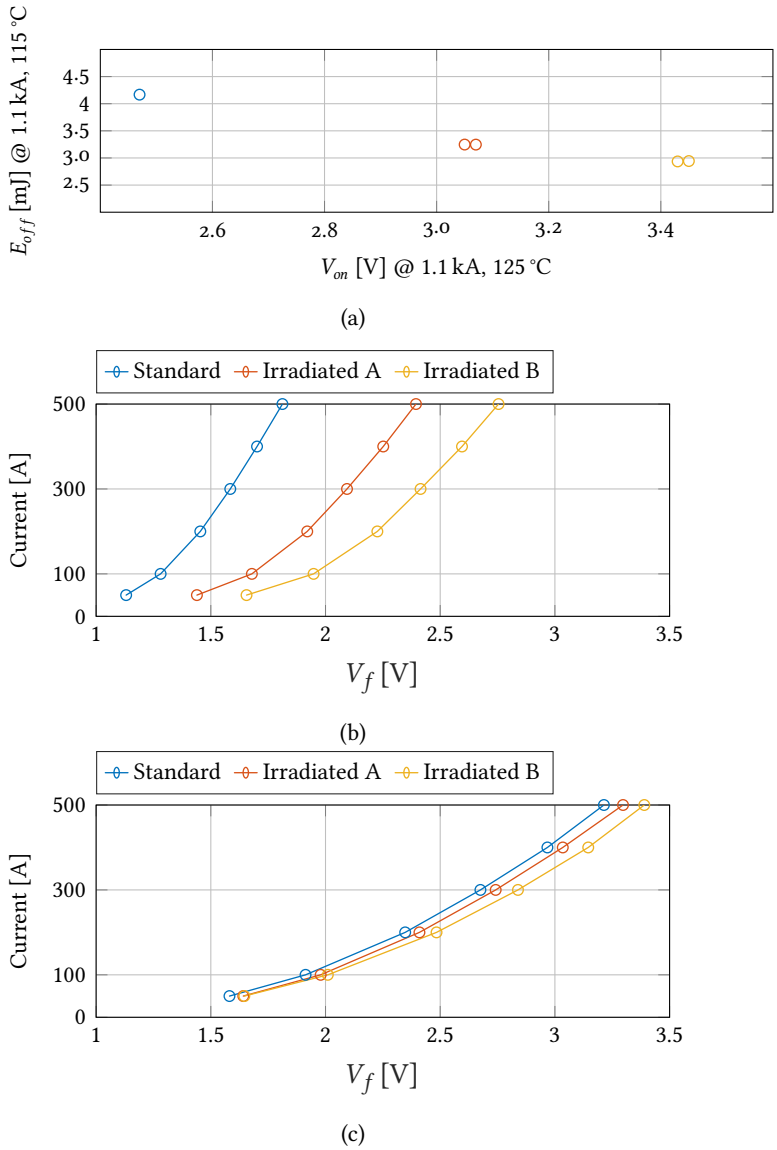


Fig. 3.2 a) Turn-off energy as a function of on-state voltage under hard switched conditions; b) GCT forward voltage, and c) diode forward voltage for ○ standard devices, ○ *Irradiated A*, and ○ *Irradiated B*.

3.3 Series Resonant LLC Operation

For the purpose of discussing the operation of the SRC-LLC, the topology with parameters brought to the transformer primary, as in Fig. 3.1, is considered. In practice, while the topology for DCT applications must be bidirectional, in the open-loop operating mode only one of the two bridges is switching at any one time, depending on the direction of power flow [138].

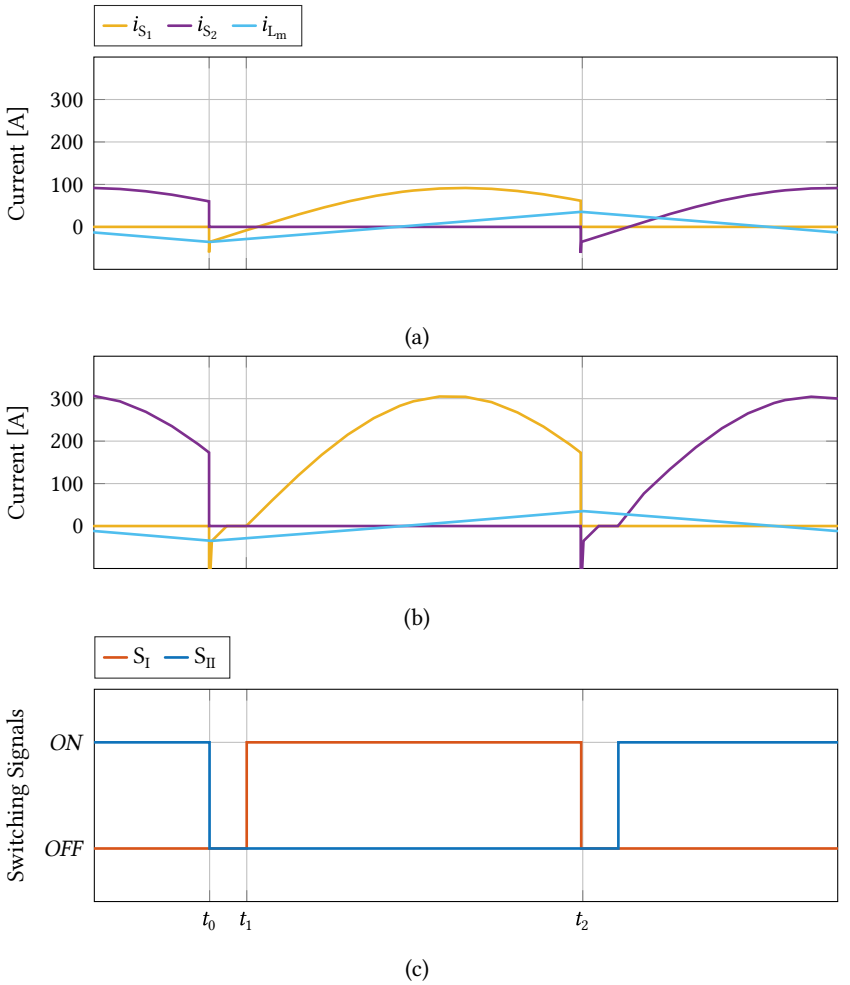


Fig. 3.3 a) Low load superresonant operation operation of the SRC-LLC results in lower turn-off current compared to b) high load operation; c) displays the employed switching signals in simulation.

3.3.1 Superresonant Operation

Superresonant operation of the SRC-LLC takes place when the switching frequency f_{sw} exceeds the resonant frequency f_r of the topology's resonant tank. This can be a consequence of the switching frequency being varied for the purpose of controlling the converter's output voltage by leveraging its voltage transfer characteristic, which was seen in Fig. 2.5(a). For the most part, output voltage regulation through variation of f_{sw} is employed in sub-kW LLC-based power supply applications.

Fig. 3.3 displays typical waveforms for this operating mode. The figure displays a full period of

operation. Times t_0 and t_2 correspond to the turn-off of switches switch S_{II} and S_I, respectively, with power transfer taking place between instants t_1 and t_2. In superresonant operation, the semiconductors must interrupt the sum of both magnetising current i_{L_m}, and load current. For this reason, comparing Fig. 3.3(a) and 3.3(b), it is clear how varying load levels affect the turn-off current level, since a higher load results in higher resonant pulse current.

Keeping in mind the goal of reducing IGCT switching losses to achieve increased switching frequency, the dependency of turn-off loss on load level is undesirable, especially at the high power level of the DCT application. For this reason, superresonant operation is not considered further in this thesis, in favour of subresonant operation.

3.3.2 Subresonant Operation

Contrary to superresonant operation, subresonant operation results in turn-off current level to be almost constant even in the presence of load variations. This is due to the resonant pulse, which is responsible for power transfer from primary to secondary, to be completely extinguished by the time the devices are turned *OFF*. Fig. 3.4 displays typical current and voltage waveforms for this topology, and the relative IGCT switching signals. For the moment, the transition of the device turn-off and turn-on are considered to be ideal and consequences of their non-ideality are addressed later.

3.3.2.1 In ZVS Conditions

Operation in ZVS conditions of the SRC-LLC topology takes place when operating at a relatively light load. Under these conditions, the characteristic waveforms of the topology are as seen in Fig. 3.4, and each half period can be subdivided in three intervals:

- From t_0 to t_1: At t_0 S_{II} is conducting the magnetising current. As it is turned off, the magnetising current stays virtually constant due to the relatively large value of the magnetising inductance, and the path is closed through the antiparallel diode of S_I, which becomes forward biased and enters conduction. This has the additional effect of forward biasing rectifier diode D_{S_I}, which also enters conduction and a resonant current pulse commences. S_1 is turned *ON* before the end of the dead-time (normally $< 10\,\mu s$ for IGCTs in hard-switched operation), resulting in ZVS turn-on.
- From t_1 to t_2: The sum of resonant and magnetising current is conducted by S_I and the main bulk of power transfer takes place from primary to secondary side of the topology. The current through the D_{S_I} at this time is the sum of the magnetising current, the value of which changes slowly, and the rapidly increasing resonant pulse current, flowing towards the load. Once the resonant current has reached its peak amplitude, it slowly starts to decrease until at time t_2 D_I becomes reverse biased the power transfer from primary to secondary ends.
- From t_2 to t_3: At t_2, the magnitude of the resonant current has reached 0 A, and S_I only conducts the remaining magnetising current i_{L_m}. The value of the magnetising current does not increase significantly during this time, as L_m is relatively large. In principle, the duration of this time interval can be very short (or equal to $0\,\mu s$, if $f_{sw} = f_r$), but must still be long enough to allow reverse recovery of diode D_{S_I}. In practise, the duration of the interval is determined by the difference between the resonant and switching periods.

Operation in ZVS conditions is an important feature of the SRC-LLC topology, allowing turn-on

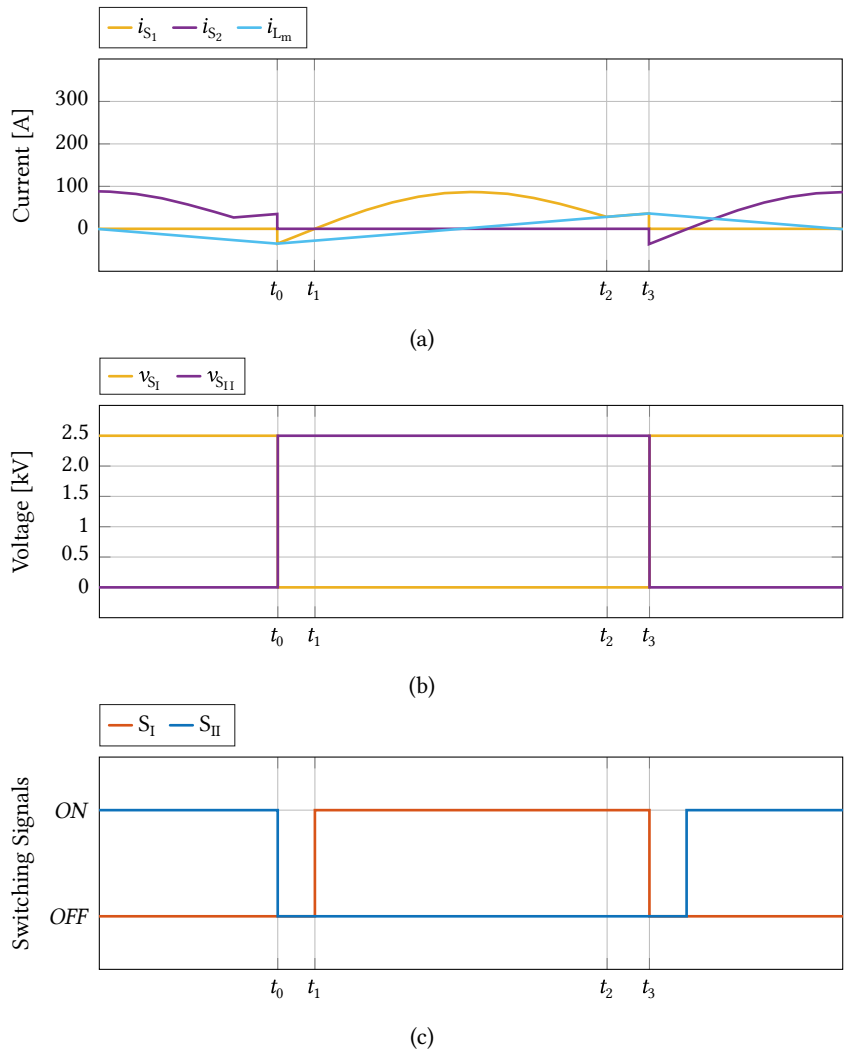


Fig. 3.4 Subresonant operation of the SRC-LLC resulting in constant low current turn-off conditions, which are independent of transferred load. Semiconductor turn-on takes place in ZVS conditions thanks to the magnetising current being conducted by the device's antiparallel diode before turn-on takes place.

losses to be neglected during the converter design phase. Nevertheless, ZVS is not always guaranteed in subresonant operation. As seen in Fig. 3.4, for the turn-on of S_I to take place in ZVS conditions, it must happen while the antiparallel diode of S_I is in conduction. That is to say, the duration of the period during which D_{S_I} conducts must be longer than the dead-time. If the conduction period of D_{S_I} is short, which correspond to high load condition, then D_{S_I} will become reverse biased before S_I is turned *ON*, and the turn-on will not take place in ZVS conditions.

3.3.2.2 In Quasi-ZVS Conditions

Under high load condition, the rate of increase of the resonant pulse current is sufficiently high to cause diode D_I to undergo reverse recovery and be reverse biased before S_I is turned *ON*. The operation under this condition results in the current and voltage waveforms displayed in Fig. 3.5. In the figure it can be seen than at time t_1 a "notch" can be observed in the resonant current profile, corresponding

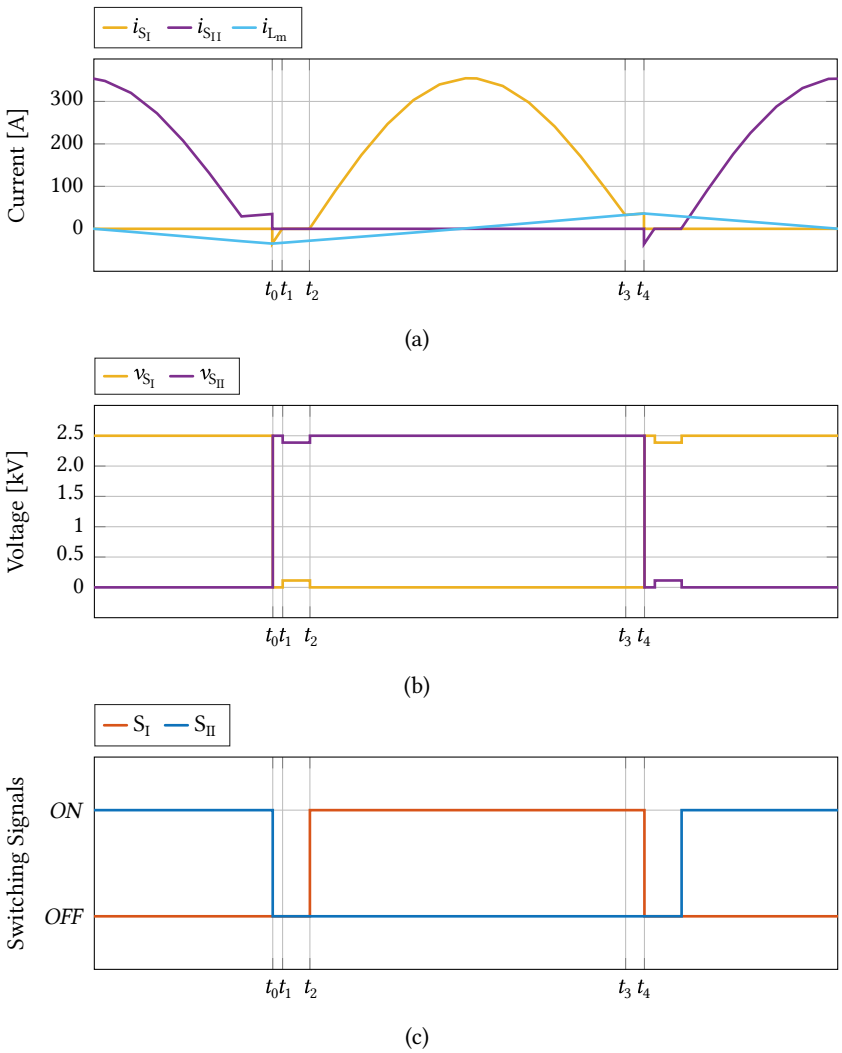


Fig. 3.5 High load operation in subresonant mode may result in loss of ZVS conditions and transition to quasi-ZVS. a) IGCT current exhibits a "notch" at t_1 as the load current value reaches the magnetising current; b) quasi-ZVS operation result in the resonant capacitor voltage being reflected onto the IGCT about to be turned *ON*; c) corresponding switching signals.

to the time when D_{S_I} stops conducting to become reverse biased. Instead of smoothly increasing to its peak value, the resonant pulse can only restart at time t_2, when S_I is turned *ON* allowing for further current flow towards the load. Interval by interval, the topology behaves as follows:

- From t_0 to t_1: At t_0 the behaviour of the topology is identical to the ZVS case. At S_{II} turns *OFF* the magnetising current starts being conducted by the antiparallel diode of S_I, which results in D_{S_I} becoming forward biased itself and a pulse of resonant current starting. Therefore, D_{S_I} conducts the sum of the magnetising current (negative, flowing out of the resonant tank), and the load resonant current (positive, flowing into the resonant tank). In low load conditions, the sum to the two current stays negative well after the turn-on of S_I, resulting in a smooth transition from D_{S_I} conducting to S_I conducting. But in high load condition, due to the fast increase of the load resonant current, at time t_1 the magnetising and resonant current are equal

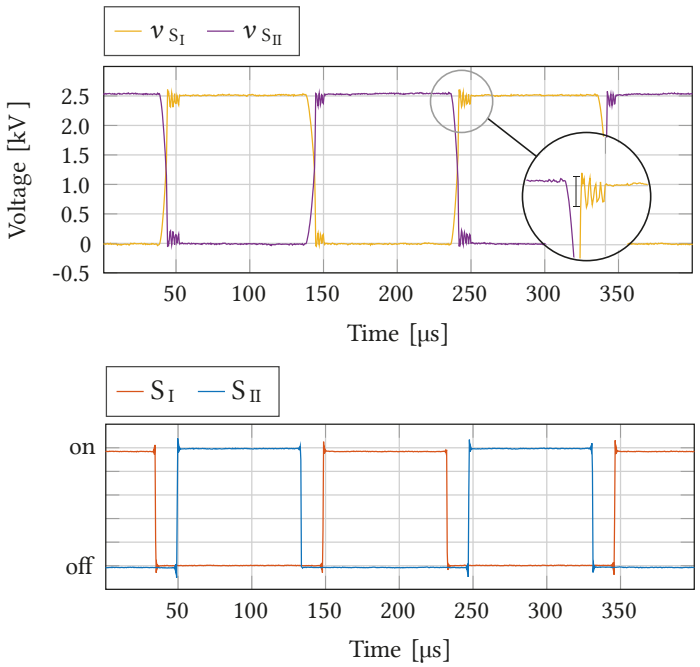


Fig. 3.6 In quasi-ZVS operation, the IGCT turn-on is performed with the resonant capacitor peak voltage being applied at its terminals. Due to the capacitor voltage being very low relative to the dc link voltage, the turn-on losses in this operating mode are still negligible.

in value, and the current in D_{S_I} becomes equal to 0 A and the diode is reverse biased.

- From t_1 to t_2: After D_{S_I} becomes reverse biased, no current flows through D_{S_I} or S_I, and the resonant pulse is temporarily interrupted, as the diode is reverse biased and the GCT is not yet turned *ON*. Nevertheless, the voltage blocked by S_I during this period is only equal to the peak voltage at the terminals of the resonant capacitor C_r, as rectifier diode D_I is forward biased during this phase. The peak voltage of resonant capacitor C_r depends on the design of the resonant tank, but for the vast majority of resonant tank designs the value of of this voltage is significantly smaller than the dc link voltage. For this reason, while the turn-on of S_I does not strictly speaking take place in ZVS condition, this quasi-ZVS turn-on equally results in negligible turn-on losses for the IGCT.
- After the quasi-ZVS turn-on of S_1, the rest of the period proceeds like in the ZVS case.

The current paths during the various subdivisions of the period of quasi-ZVS operation are displayed in Fig. 3.7, and test waveforms displaying voltage at the terminals of the IGCT (showing the peak voltage of C_r being reflected on the IGCT terminals), are displayed in Fig. 3.6.

3.3.2.3 In Non-ZVS Conditions

The second potential cause of loss of ZVS is due to the non-ideality of the switching devices and the duration of their switching transitions. As discussed in [19], decreasing values of turn-off current result in increased IGCT turn-off duration. In the embodiment of the SRC-LLC topology discussed in this thesis, the turn-off current of the device is intentionally low, so as to reduce turn-off losses.

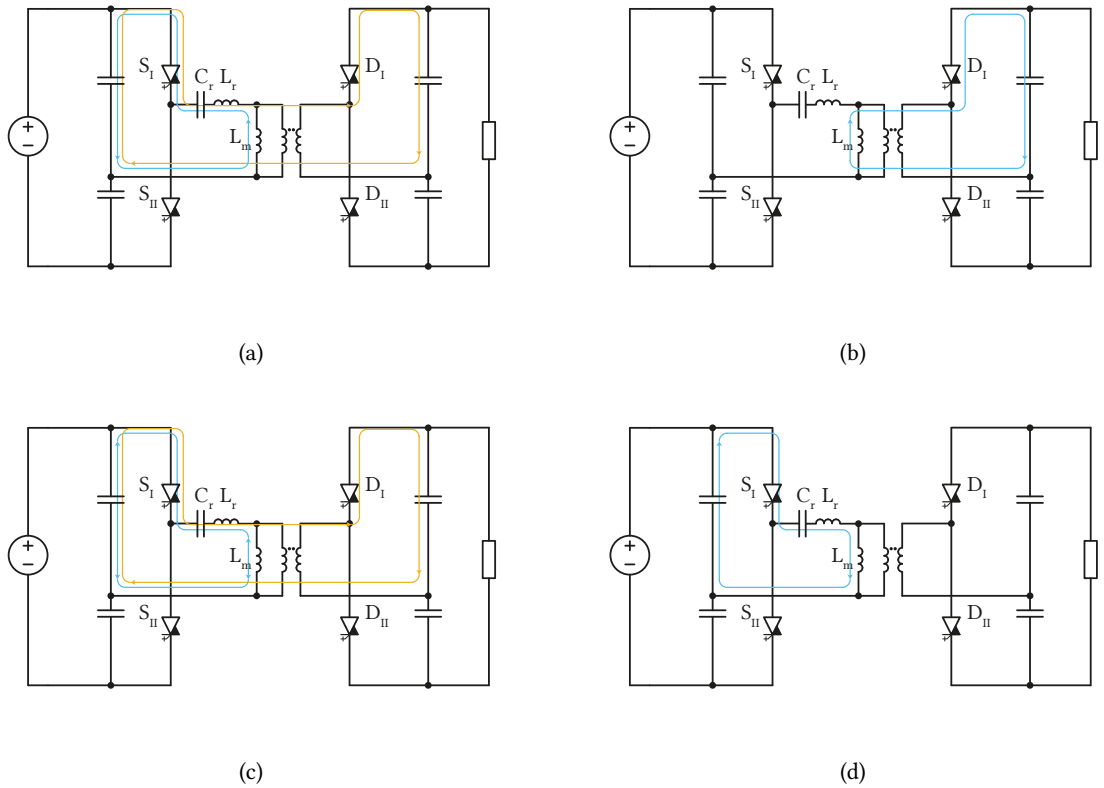


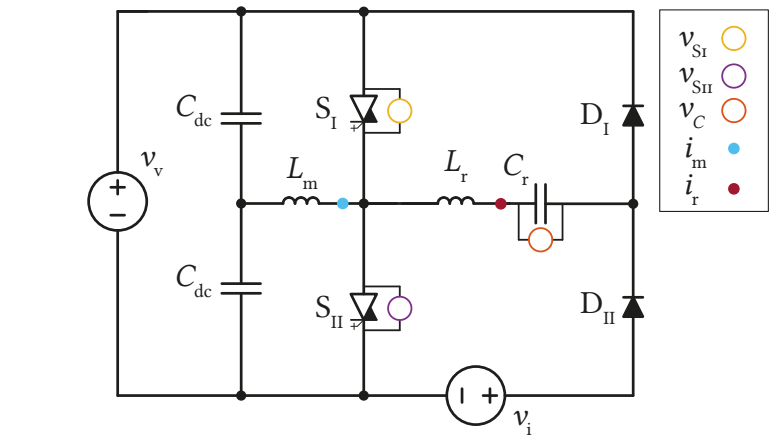
Fig. 3.7 IGCT (yellow) and magnetising (blue) current paths during quasi-resonant operation corresponding to Fig. 3.5 for time intervals a) $t_0 - t_1$; b) $t_1 - t_2$; c) $t_2 - t_3$; and d) $t_3 - t_4$.

But as the turn-off current decreases, the increased turn-off duration increases. This might result in incomplete state transition of the IGCT during the dead time. As a consequence, partial shoot-through may occur, with the relative loss of ZVS and increased losses. Therefore, a trade-off exists between loss reduction through minimisation of IGCT turn-off current, and switching loss increase due to low current resulting in incomplete state transition and loss of ZVS. The rest of this chapter discusses this phenomenon and determines to what level the IGCT turn-off current can be reduced before losses due to partial shoot-through exceed the reduction of losses obtained through the reduction of turn-off current.

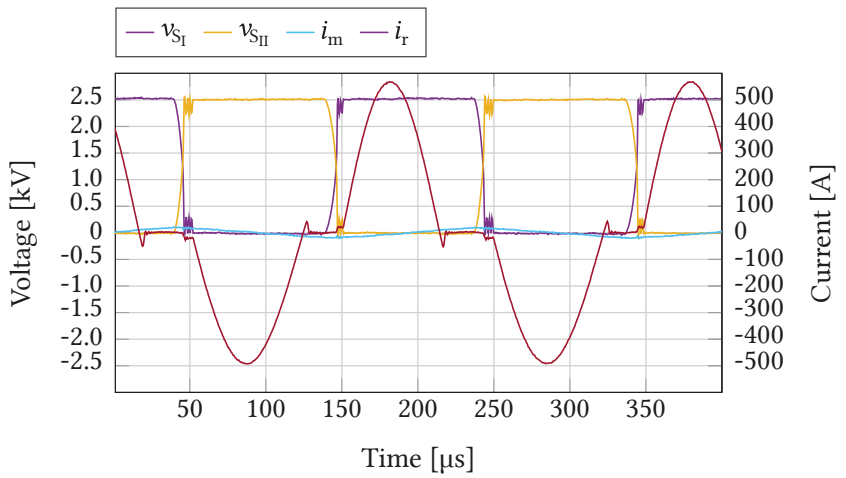
3.4 Configuration of the IGCT Test Setup

The exploration of the limits of quasi-ZVS operation is performed through the IGCT test setup described in 2.7. The test setup emulates the switching conditions observed by the IGCTs during the operation of a SRC-LLC topology, but recirculating power in the same dc link capacitors.

In the configuration displayed in Fig. 3.8(a), the test setup can circulate energy from the DC link capacitors C_{dc} into the IGCTs and resonant tank, and back into the capacitors through the diode rectifier by applying a voltage v_i to the return path of the current emulating a controllable load. This is achieved by creating an artificial voltage difference between the resonant tank input and output.



(a)



(b)

Fig. 3.8 The IGCT flexible test setup [137] is configured to emulate the behaviour of an LLC-SRC converter, as shown in a). Typical waveforms for the setup in this configuration are seen in b).

The voltage generated by v_i can be modified to increase or decrease the value of the load current i_r, effectively simulating load variation in an LLC-SRC. The current i_m emulates the transformer magnetising current and is determined by the DC link voltage and the value of inductor L_m.

The purpose of the test setup in this configuration is to evaluate the effects of varying turn-off current, dead-time duration, and current pre-flooding on IGCT switching losses under resonant conditions. Typical waveforms for the setup as presented in Fig. 3.8(a) are displayed in Fig. 3.8(b). For the purpose of evaluating switching performance under variable switching conditions, the setup is not operated in continuous mode in this chapter, but rather individual switching pulses are executed and the resulting waveforms analysed.

With *5SGX 1445H0001* 4.5 kV RC-IGCTs employed in the setup, the dc link voltage is fixed at 2.5 kV. As the purpose of the tests presented in this chapter is to evaluate switching loss of the IGCTs under various turn-off current levels, the value of inductance L_m, which, as seen previously, determines the value of turn-off current in subresonant SRC-LLC operation, is varied to achieve the desired turn-off currents. The range of inductance values available (as per Table 4.1) allow turn-off current levels down to only 3 A. Additionally, if needed, inductor L_m can be completely removed to achieve zero-current turn-off where required. Finally, the value of peak resonant (modified through the value of v_i) current can be used to evaluate the effect of charge pre-flooding on switching transitions as well as on losses.

Tab. 3.1 Values of IGCT test setup components used in this chapter.

v_v	v_i	C_{dc}	C_r	L_m	L_r
2.5 kV	0 V...20 V	2.6 mF	85 µF	1.5 mH...100 mH	8 µH

3.5 IGCT Switching Losses at Ultra-Low Turn-Off Current

In hard switched applications and for high turn-off current levels, the turn-off losses of the IGCT are proportional to the turn-off current. The lower the turn-off current, the smaller the turn-off energy dissipated in the device. Nevertheless, when significantly reducing the level of turn-off current (<100 A), [19] has shown how the duration of the transition of the IGCT from the *ON* state to the *OFF* state is significantly increased. For the purpose of minimising switching losses, it is essential to understand if and how very low values of turn-off current result in a switching transition slow enough to exceed the dead-time. If this is the case, partial shoot-through will result, where the complementary device in each leg is turned on before the turn-off transition of the conducting device has been completed, resulting in remaining charge carriers begin cleared from the device with a corresponding high current peak and resulting increased switching energy. This is similar to the forward recovery of MV IGBT modules documented in [90], [139]. How partial shoot-though affects IGCT switching losses is explored here.

3.5.1 Understanding the ZVS/ZCS Transition

To explore the boundary between ZVS low-current turn-off and partial shoot-though, the test setup in Fig. 3.8 was configured with a very large value of magnetising inductance $L_m = 100$ mH, and a power supply voltage $v_i = 0$ V (effectively the same behaviour as if the resonant tank was disconnected). In this configuration, the turn-on of IGCT S_I causes a linear increase of the magnetising current i_m up to the desired turn-off level. S_I is then turned *OFF* and after dead-time t_{dt} has passed, S_{II} is turned *ON*. The current and voltage waveforms of S_I are sensed allowing to observe the switching waveforms as a function of the turn-off current. It is also possible to turn-on IGCT S_{II} first, and evaluate the turn-on waveforms of S_I. As there is no resonant current flowing in the setup, the values of elements L_r and C_r are not relevant. The value of the DC link voltage v_v is set to 2500 V.

Fig. 3.9 displays turn-off and turn-on transitions for S_I, with various ultra-low (<20 A) values of switching current: 17 A, 9 A, and 0 A. In the LLC-SRC topology, the turn-off current value is equivalent to the magnetising current in the transformer, while in the test setup in Fig. 3.8 to i_m. For all three subfigures, switching waveforms are presented with the same dead-time of 10 µs.

Three different conditions can be observed: in Fig. 3.9(a), the state transition of S_I happens in ZVS

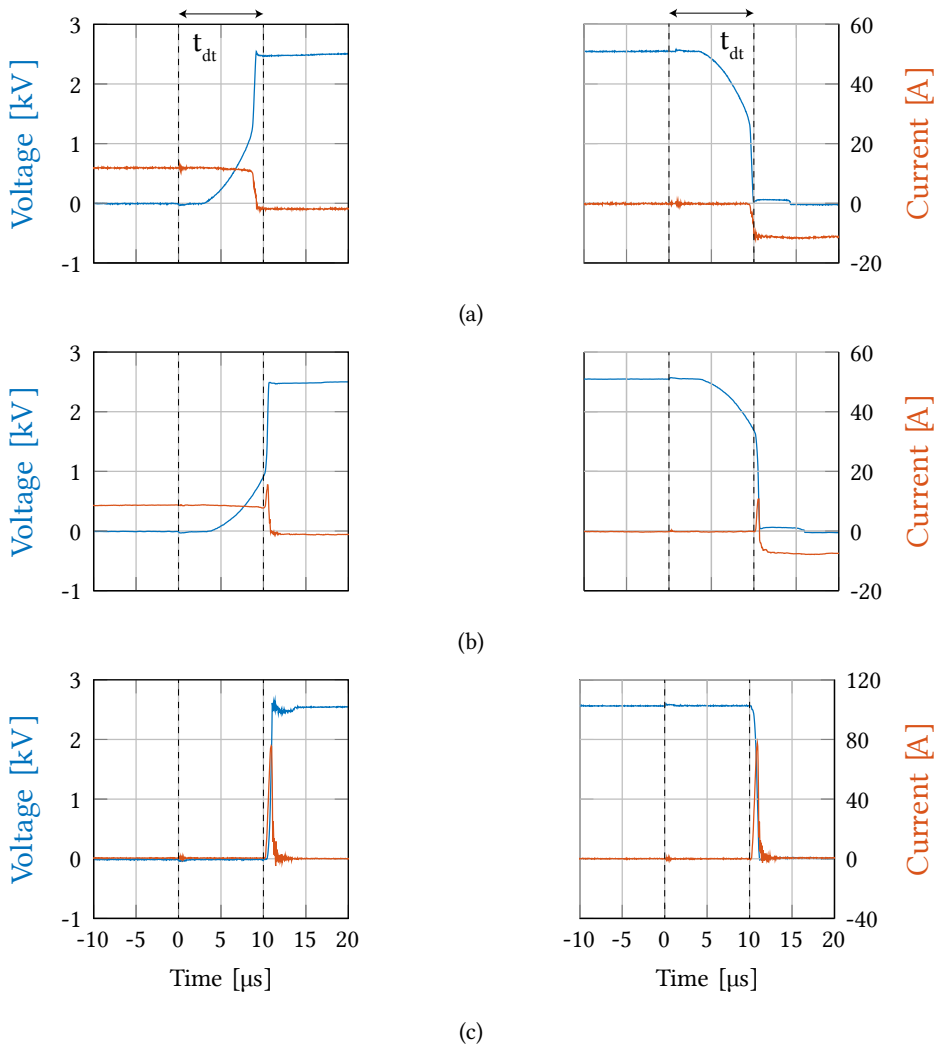


Fig. 3.9 IGCT turn-off and turn-on under a) ZVS, b) non-ZVS, and c) zero-current conditions. The turn-off current values are 17 A, 9 A, and 0 A, respectively. With loss of ZVS partial shoot-though takes place due to incomplete n-base sweep-out.

conditions. That is to say, the turn-off current level is sufficiently high to sweep out the n-base of S_I before the dead-time ends and S_{II} is turned *ON* (and vice-versa for turn-on). Fig. 3.9(b) displays the effect of a lower values of turn-off current (9 A). In such a condition, the current level is insufficient to complete the n-base sweep-out during the dead time, and at the time of turn-on of S_{II}, the turn-off of S_I is incomplete. As S_{II} turns *ON*, a partial shoot through takes place in both devices, as they briefly are both in conduction at the same time. This causes a current peak in both devices, and an increase in the amount of charge conducted through S_{II} during its turn-off. The partial shoot through causes an increase in both turn-off losses for S_I, and turn-on losses for S_{II}.

Finally, the complete disconnection of inductor L_m allows the evaluation of the effect of a turn-off current i_m = 0 A. This is not achievable in a true LLC-SRC topology, as the transformer magnetising inductance is a finite value, nevertheless, the removal of L_m allows the evaluation of the effect of a turn-off current level approaching 0 A.

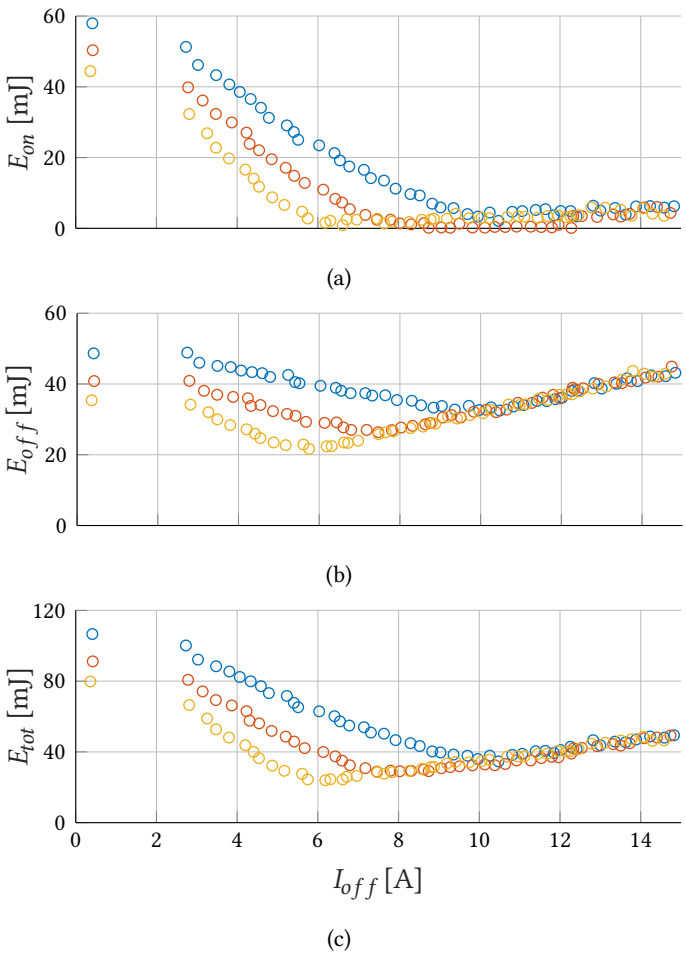


Fig. 3.10 Turn-on a), turn-off b), and total switching energy c) for standard commercial RC-IGCTs with dead-times of ○ 10 µs, ○ 12 µs, and ○ 14 µs.

Fig. 3.9(c) shows the switching transitions under these conditions. The turn-off of S_I does not start as the conducting device is turned *OFF*, as there is no current present in the device to clear charge carries for the n-base. Instead, the state transition takes place only as S_{II} is turned *ON*. This results again in partial shoot-through, but the amount of charge that must be swept out of of S_I is larger in this scenario, resulting in an increased current peak and consequently increased losses in both devices.

Therefore, it is expected that the turn-off current resulting in the minimum switching losses is the minimum current level that allows the full transition of the IGCT during the dead-time. If the dead time is longer, then a lower level of turn-off current can still be used and achieve full state transition of the conducting IGCT before the complementary device is turned *ON*, while if the dead-time is shorter, then a larger turn-off current will be required to complete the sweep-out in the required time. This is assuming the turn-off current is a degree of freedom during design, which is the case in this thesis.

Thanks to the high values of the magnetising inductor in the test setup, the turn-off current can be carefully set by changing the *ON* time of S_I (or S_{II} for turn-on). Fig. 3.10 maps the turn-on and turn-off losses in the standard commercial RC-IGCTs as a function of turn-off current and dead-time (the

leftmost part of the plot is not populated due to limitations on the available L_{m} and GCT minimum turn-on time).

The exhibited trends are coherent with what is expected based on Fig. 3.9. Fig. 3.10(a) shows how turn-on loss is absent as long as ZVS conditions are maintained. This is because in the absence of partial shoot-through, no charge is conducted by the IGCT during its turn-on. Once ZVS conditions are lost (with a reduction of turn-off current, moving left in the plot), partial shoot-through takes place causing turn-on loss, which increases the more the turn-off current is reduced. The lower the turn-off current, the fewer charge carries are removed from the device during turn-off, and therefore the more charge is cleared from the device during the turn-on of the complementary IGCT and the occurrence of partial shoot-through. Turn-on losses progressively increase up to the limit of turn-off current equal to 0 A.

As the transition from *ON* to *OFF* state of the IGCT take place (when under ZVS conditions) during the dead-time, then longer the dead-times result in lower turn-off currents being achievable while still maintaining ZVS conditions. Fig. 3.10(b) shows how the turn-on loss is almost linear with the value of turn-off current when in ZVS conditions. Once ZVS is lost (left side of the plots), turn-off loss also increases due to partial shoot-through, as the resulting current spikes take place both during turn-on and turn-off.

Finally, Fig. 3.10(c) displays the total switching loss. The figure clearly shows how, as expected, the minimum total switching loss happens at the minimum value of turn-off current which guarantees ZVS. At this particular value, the turn-off current level is the minimum level which will result in complete state transition of the IGCT during the dead-time. This result in low turn-off loss, while still guaranteeing ZVS conditions and therefore absence of turn-on loss. The value of current required to completely transition the devices at turn-off increases with a shorter dead-time, resulting in increased minimum switching loss, and conversely decreases with longer values of dead-time.

Applications which can allow extended duration of the dead-time can benefit from lower total switching loss. In the case of SRC-LLC operation for DCT applications, the maximum duration of the dead-time is a compromise between the reduction of switching loss, and the duration of the portion of the switching period available for power transfer.

A significant conclusion of the results presented above is that loss of ZVS, while resulting in increased loss, does not have a catastrophic effect on the devices' switching energy. There is no remarkable increase in switching loss in the vicinity of the operating point where ZVS conditions are lost. Operation close to the optimal point will still result in low switching loss, even if not in ZVS conditions.

3.5.2 Effect of Pre-Flooding and Irradiation

The test results gathered and displayed in Fig. 3.10 show that the optimal turn-off current level for switching loss minimisation is the minimum current that will guarantee ZVS conditions. However, during this phase of testing, the maximum current conducted by the device under test never exceeds the turn-off current level, which is very low. This is not representative of the operating conditions in an LLC-SRC converter, where the resonant current peak can be orders of magnitude larger than the turn-off current value, as seen in Fig. 3.12.

In conducting a significant current level, the IGCT is pre-flooded with charge carriers which will have to be swept out upon turn-off, affecting the duration of the state transition as seen in Fig. 3.11, where

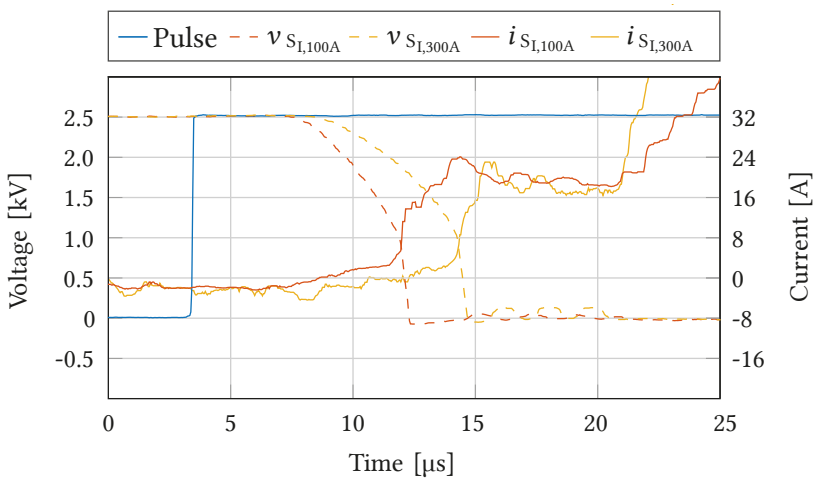


Fig. 3.11 Pre-flooding due to the conduction of resonant current increases IGCT turn-off duration, with consequences on ZVS turn-off conditions.

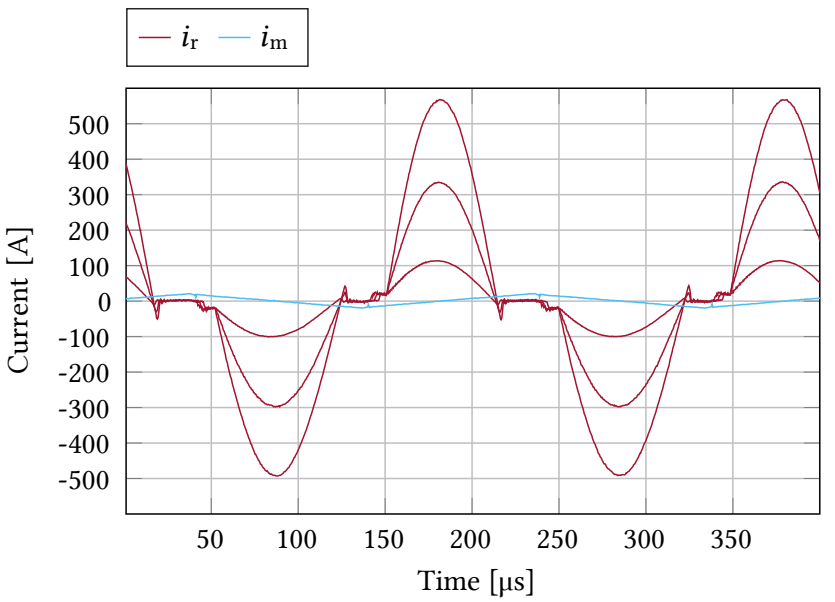


Fig. 3.12 Experimental waveforms show that during SRC-LLC operation the peak resonant current can be several orders of magnitude larger than the peak magnetising current, depending on the load level.

a 200 A difference in peak resonant current conducted results in a turn-off time increase of about 2.5 µs. Consequently, this affects the conditions in which ZVS is achieved, as more time is required to sweep out all charge carriers upon turn *OFF* of the device at the same turn-off current level. Therefore, additional explorations are carried out to quantify the effect of current pre-flooding. Here, devices *Irradiated A* and *Irradiated B* are additionally considered, as their reduced carrier lifetime will be shown to be beneficial during state transitions.

Results detailing the effects of current pre-flooding are gathered and summarised in Fig. 3.13, which displays the turn-on and turn-off energy of standard commercial RC-IGCTs and devices with in-

creased irradiation levels as a function of peak conducted resonant current and turn-off current. The exploration is carried out maintaining a constant value of dead-time set to 14 µs which has been shown in previous tests to guarantee reduced switching losses by allowing ZVS conditions to occur at a decreased level of turn-off current. The resonant frequency of the test setup resonant tank is set to 7.35 kHz and the voltage v_i is altered throughout the test to obtain the desired resonant current peak, while v_v is maintained at 2.5 kV.

The top row of Fig. 3.13 displays the IGCT turn-on energy. In ZCS conditions (L_m inductor disconnected, $I_{off} = 0$ A), turn-on losses are present for all three devices, which is expected since ZVS is not achieved. With an increase of the device's turn-off current, standard devices and both *Irradiated A* and *Irradiated B* devices exhibit different behaviours. Standard devices do not achieve ZVS switching over the whole range of resonant peak current $I_{r,pk}$ until a turn-off current level of 17 A is reached. A lower current level of 9 A is only sufficient to maintain ZVS conditions up to 200 A of peak resonant current.

The turn-off current level of 17 A, which is required for the standard devices to achieve ZVS up to the peak considered resonant current level of 400 A, is significantly higher than the turn-off current of 6 A, which was sufficient without pre-flooding. This illustrated the significance of the consequences of charge pre-flooding and the importance of the exploration of this effect.

Compared to standard devices, the turn-on energy of *Irradiated A* and *Irradiated B* devices is significantly lower, even in ZCS conditions with $I_{off} = 0$ A, when the same level of turn-off current is considered. Additionally, due to a faster turn-off and turn-on state transition, a turn-off current of 6 A is already sufficient to maintain ZVS conditions over the whole operating range for *Irradiated A*, while a turn-off current as low as 3 A is sufficient for *Irradiated B*. This can be concluded by the absence of turn-on losses already at these current levels for the irradiated devices.

Coherently with their faster state transitions, increased irradiation devices exhibit lower turn-off losses than standard devices at the same turn-off current level. The turn-off energy of the *Irradiated B* is as low as half of that of the commercial device for an equivalent turn-off current level. Similarly to what was observed without charge pre-flooding, the turn-off energy of all three devices exhibits different behaviours depending on whether the switching process occurs in ZVS conditions or not. In ZVS switching conditions, the turn-off energy of the device is almost constant over the whole operating range (with different levels of peak resonant current being conducted).

In contrast, if ZVS conditions are not met, the device turn-off energy increases linearly with the peak resonant current level. This is because increased levels of charge pre-flooding result in progressively more charge having to be cleared from the junction upon device turn-off, which results in an increasing total turn-off time. As the turn-off time progressively exceeds the dead-time of 14 µs by an increasing amount, more and more charge is cleared upon the turn-on of the complementary device, again resulting in increased total switching losses.

The total switching energy results from the compounding of the effects of turn-off current and partial shoot-through on the turn-on and turn-off energy. In the absence of ZVS, the total switching energy increases with $I_{r,pk}$ (due to the increasing duration of the turn-off transition), but in ZVS conditions, when the turn-off time does not exceed the dead-time, the switching energy stays constant over the operating range.

To select the appropriate value of turn-off current for each device, the worst-case loss condition is

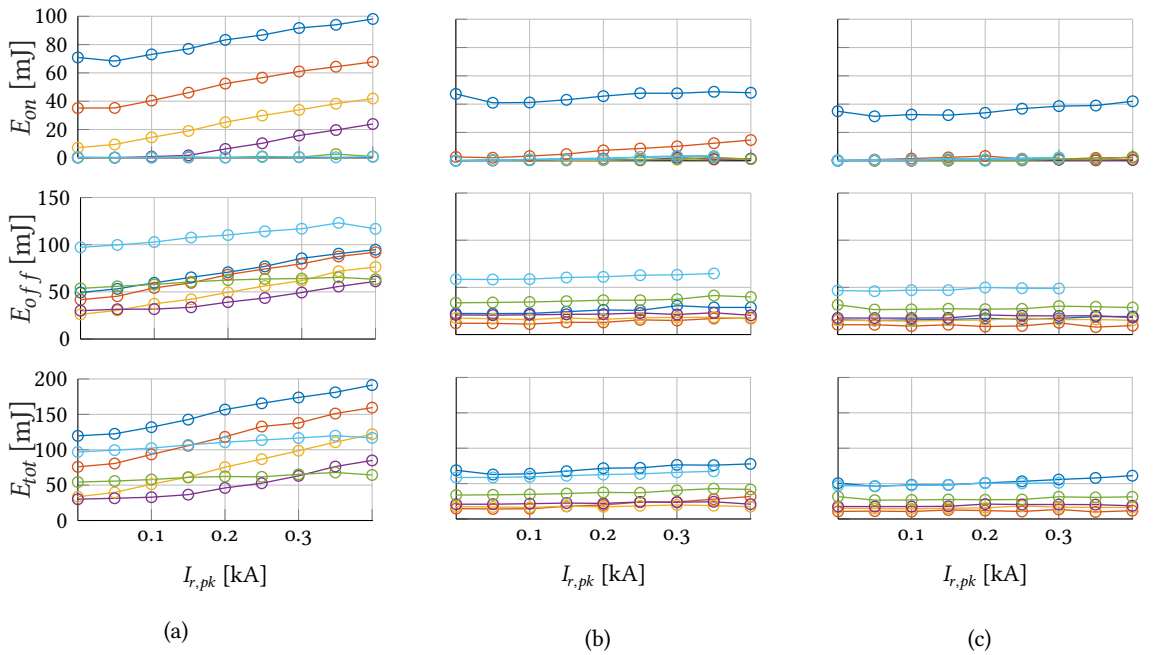


Fig. 3.13 Turn-on, turn-off, and total switching energy for a) standard commercial RC-IGCTs, b) *Irradiated A*, and c) *Irradiated B* devices. The duration of the dead-time is 14 µs and the turn-off current levels are of ○ 0 A, ○ 3 A, ○ 6 A, ○ 9 A, ○ 17 A, and ○ 34 A.

considered. For all three devices, the larger the peak resonant current, the larger are both conduction (evaluated later) and switching losses. Therefore, the suggested turn-off current level is the value of I_{off} for which the total switching losses at the maximum evaluated level of resonant current (maximum load) are the lowest. That is to say the minimum value of turn-off current which guarantees ZVS over the whole operating range. For the specific devices discussed here, this level is around 17 A for standard devices, 6 A for *Irradiated A* devices, and 3 A for *Irradiated B* devices. This highlights how the advantage offered by devices subjected to increased electron irradiation is compounded in the context of switching loss:

- Devices with increased irradiation have lower carrier lifetime, resulting in faster switching transitions and therefore reduced switching loss when compared to standard devices at the same current level.

- While losses for devices with increased irradiation are lower for the same turn-off current level, it is possible to operate these devices at a reduced current level while still maintaining ZVS conditions with a fixed value of dead-time.

Since turn-off current can be reduced for *Irradiated* devices while still maintaining ZVS, the lower turn-off current that can be employed compounds the benefits extracted from these devices in terms of switching losses, making them potentially very beneficial in the application. Nevertheless, this is somewhat offset by their performance in conduction, as will be shown later.

3.6 Summary

This chapter examined the switching behaviour of RC-IGCTs at ultra-low (<20 A) turn-off currents. An optimal turn-off current value for the minimisation of switching loss is determined to exist at the threshold of ZVS conditions: that is to say at the minimum value of turn-off current that will guarantee ZVS operation. This value of current depends on the level of electron irradiation underwent by the device, and is affected both by dead-time duration (reduces the current value), and by semiconductor pre-flooding (increases the current value). With a fixed value of dead-time, increased levels of semiconductor pre-flooding resulting from an increased peak conducted current result in slower turn-off, and therefore in loss of ZVS a turn-off current values which guarantee ZVS operation in no-load conditions. The loss of ZVS causes an increase in IGCT switching loss, but the increase is progressive and does not result in immediate failure of the devices, but merely in less efficient operation. Devices having underwent increased levels of electron irradiation (*Irradiated A* and *Irradiated B*) have reduced switching losses both because of their faster turn-off, and because of the resulting reduced turn-off current that this allows while still maintaining ZVS conditions. Ultimately, this chapter concludes that operation in ZVS conditions is preferable to ZCS conditions in terms of the reduction of switching losses in the devices, which is a conclusion used in the following chapters of this thesis.

4

Steady State Operation at 5 kHz

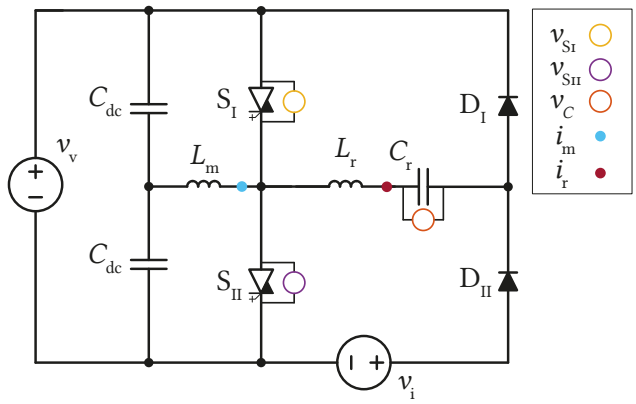
Having determined optimal switching conditions for the considered standard devices and devices exposed to increased electron irradiation, high frequency continuous operation of the IGCTs is demonstrated in this chapter. The low switching loss in the identified threshold ZVS conditions combined with the low RC-IGCT conduction loss allows operation at a switching frequency of 5 kHz *under varying levels of load, which is unprecedented for the IGCT. The total operating loss of the IGCTs is calculated, quantifying the advantage resulting from the use of increased irradiation devices. The IGCT junction temperature is estimated based on the measured case temperature and the computed loss, concluding that the tested operating mode is well within the capabilities of the device.*

4.1 Introduction

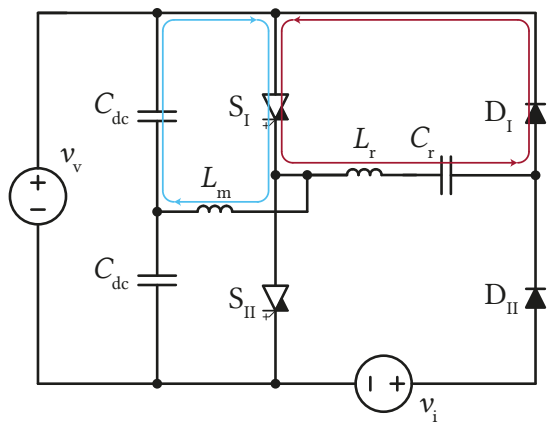
In the several LV applications in which dc systems have found use, a significant benefit they offer compared to their ac counterparts is the removal of heavy and voluminous ac transformers, with this advantage being particularly significant in the transport sector. While transformers in traditional ac systems mostly operate at grid frequency, DCTs allow great freedom in the selection of semiconductor switching frequency and the corresponding MFT design. By operating at frequencies several orders of magnitude higher compared to ac transformers, the DCT can offer solutions significantly reducing size and weight of the required passive components. So far, switching frequencies in the range of multiple kHz are commonly used in academic work. As DCT applications operate in the power range of several MW, such switching frequencies require excellent switching performance on the part of the employed semiconductors in order to manage the associated losses.

For this reason, Si IGBTs and SiC MOSFETs have so far been identified as the preferred semiconductor solution. In comparison, the IGCT is traditionally employed at significantly lower switching frequencies. In these traditional low frequency applications, the lack of controllability of the turn-on and turn-off processes through gate driver action and results in the need for clamp circuitry. This partially negates the potential benefits in size and weight reduction of the DCT compared to the traditional ac transformer. Nevertheless, the work documented in Chapter 3 has demonstrated that an optimal turn-off current level exists for clampless use of the 4.5 kV IGCT in the SRC-LLC topology which depends on:

- Selected dead-time
- Device electron irradiation level
- Application voltage and power ratings



(a)



(b)

Fig. 4.1 a) The IGCT flexible test setup is configured similarly to Chapter 3. The voltage the the terminals of the IGCTs and resonant capacitor is sensed, together with both magnetising and resonant currents; b) In continuous operation magnetising and resonant current paths are similar to SRC-LLC operation.

and that at this turn-off current level the device exhibits very low values of turn-off and turn-on energies.

Based on this result and the well-known excellent conduction characteristics of the IGCT, this chapter demonstrates operation of the device at a frequency of 5 kHz, which proves that with appropriate design and device selection the IGCT is capable of operation at medium frequency in DCT applications.

4.2 Configuration of the IGCT Test Setup

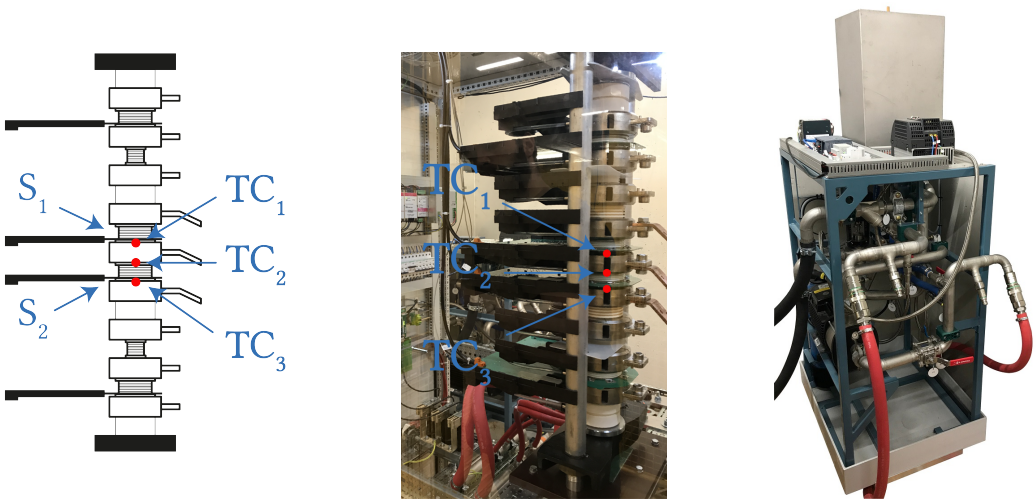
The configuration of the IGCT test setup displayed in Fig. 4.1(a) with the relative current paths being displayed in Fig. 4.1(b). The configuration is virtually identical to that used in Chapter 3. For the devices to undergo the same electrical stresses as during operation in the SRC-LLC topology, the test setup circulates energy through the resonant tank by the application of voltage v_i, which by imitating a controllable load ensures the maintaining of charge in the resonant capacitor C_r. The voltage v_i is modified to vary the peak level of resonant current i_r, from 0 A, to 100 A, 300 A, and finally 500 A. The inductor L_m is kept at a constant value of 3.1 mH to maintain a turn-off current level of 17 A, which was identified as near optimal for the standard commercial IGCTs. This turn-off current value is maintained also for devices with increased irradiation level. The tank's resonant frequency is of 7.35 kHz, which is a relatively high value compared to the tested switching frequency of 5 kHz. Ideally, the resonant frequency could be lowered and be made closer to the switching frequency, but due to the discrete nature of the available components, this was not possible.

To demonstrate the device's ability to sustain steady state operation at 5 kHz, active water cooling through the WCU in Fig. 4.2(c) and thermocouples sensing the temperature of the IGCT case during operation are added to the test setup as described in Chapter 3. The WCU circulates deionised cooling water in the IGCTs and rectifier diodes, which is interfaced through a heat exchanger to a separate water circuit containing cold water from the EPFL internal cooling system. While the WCU cannot provide closed-loop control of the deionised water temperature, it is possible to manually adjust the amount of deionised water bypassing the heat exchanger through the three-way valve and therefore modify the deionised water temperature.

To sense the operating temperature of the IGCTs during operation, wireless thermocouple probes (*Omega* UW Series wireless transmitters and receivers) are placed in heatsink grooves as seen in Fig. 4.2. The placement of the thermocouples allows them to access the IGCT case, the evolution of which is logged on a personal computer connected to a radio receiver. The thermocouples allow a sampling frequency of 1 Hz, which is sufficient for the large thermal time constants of the setup.

Tab. 4.1 Values of IGCT test setup components in testing 5 kHz steady-state operation.

v_v	v_i	C_{dc}	C_r	L_m	L_r
2.5 kV	0 V…20 V	2.6 mF	85 µF	3.1 mH	8 µH



(a) (b) (c)

Fig. 4.2 a), b) The placement of radio thermocouples in heatsink grooves allows the sensing of the IGCT case temperature; c) the WCU exchanges heat between the deionised semiconductor cooling water and the water from the EPFL cooling infrastructure.

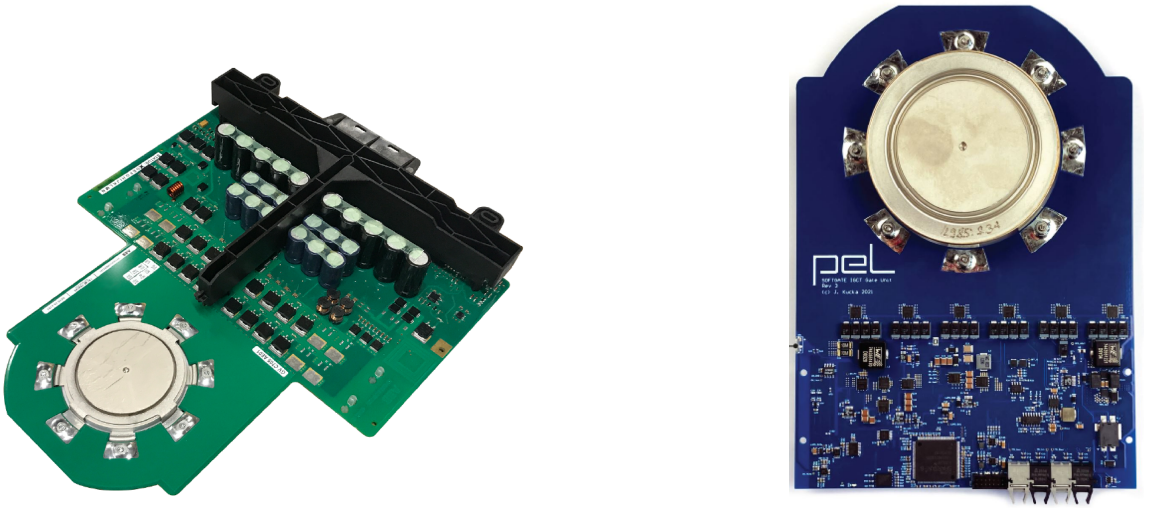
4.3 Demonstration of 5 kHz Operation

As discussed in Chapter 3, the main issues in this operating mode are increased switching loss and variation of the duration of switching transition due to current preflooding during the resonant pulse, which becomes relevant due to the slow switching transition associated to ultra-low turn-off current. Also relevant, but not in the scope of this thesis, is the stress to which the gate driver unit is subjected, considering that the standard circuit displayed in Fig. 4.3(a) is used, which is not optimised in any way for the presented operation. This was later addressed by the development of a novel gate driver unit in the laboratory, presented in [115] and displayed in Fig. 4.3(b). While the results presented in this chapter only cover 5 kHz operation, lower frequencies were also tested and progressively increased.

4.3.1 Steady-State Operation

Operation of the test setup at a switching frequency of 5 kHz is achieved for all three presented IGCT devices. Fig. 4.4 displays the sensed currents and voltages during testing at different operating points employing standard commercial devices. The setup is initially operated in no load condition and then resonant current is progressively increased to 100 A, 300 A, and finally 500 A at the peak of the resonant pulse. All the while, the IGCT case temperature is monitored. While the switching losses generated in this operating mode have been quantified in the previous chapter, conduction loss is estimated based on the device's conducted current waveform and conduction characteristic, discussed later in this chapter.

The load variation from 0 A to 500 A peak resonant current is achieved by increasing the voltage of V_i. Due to limitations of the power supply V_i, it was not possible to increase the circulated current in the setup above the level of 500 A. The setup is operated for 1 h in each of the operating points displayed in Fig. 4.4. This is sufficient time for the setup to reach a thermal steady state and ensure that the operating points are sustainable over time. Section 4.5 presents thermal measurement results and



(a) (b)

Fig. 4.3 a) The gate driver unit employed for all tests presented in this chapter is intended for conventional, sub-kHz operation of the GCTs; b) a gate driver unit optimised for soft-switched operation at several kHz has been documented in [115].

their discussion in more details.

Fig. 4.5 highlights the effect of the relatively large difference between resonant frequency and switching frequency (7.35 kHz and 5 kHz, respectively), which as previously discussed is a consequence of component availability. The measurement of the resonant current clearly allows the identification of the reverse recovery process in the rectifier diodes. Ideally, the duration of the resonant pulse would be such that the turn-off of the IGCT would take place right after this reverse recovery has come to an end. This would allow to maximise the portion of the switching period available for power transfer, minimising the peak value of the resonant current and therefore resulting in reduced conduction loss. In the test setup, the duration of the power transfer could be increased by approximately 30 µs, which is the difference between the resonant and switching half-periods: $(T_{sw} - T_r)/2$.

Additionally, it can also be seen in Fig. 4.5 see the that the peak resonant current value is different during the positive and negative pulses. This is due to the insertion of v_i in the negative current loop, which requires relatively long cables adding additional inductance, in the range of 1 µH to 2 µH, and therefore results in a lower resonant frequency for the negative current pulse. The slightly decreased resonant frequency of the negative half-period is beneficial in terms of conduction loss reduction and therefore there was no effort made to decrease the inductance of this loop, as this has no major impact on the validity of the presented results. The peak current of the negative pulse is considered when discussing the peak value of the resonant current.

4.3.2 Switching Transients

As seen in Fig. 4.4, during testing the setup is operated with a 50 % duty cycle. Open loop operation with a constant duty cycle of 50 % can be considered to be one of the main advantages of SRC-LLC based DCTs. The selected dead-time in this operating mode is of t_{dt} =15 µs, which has been seen in Chapter 3 to be the considered value resulting in the lowest switching losses while still allowing

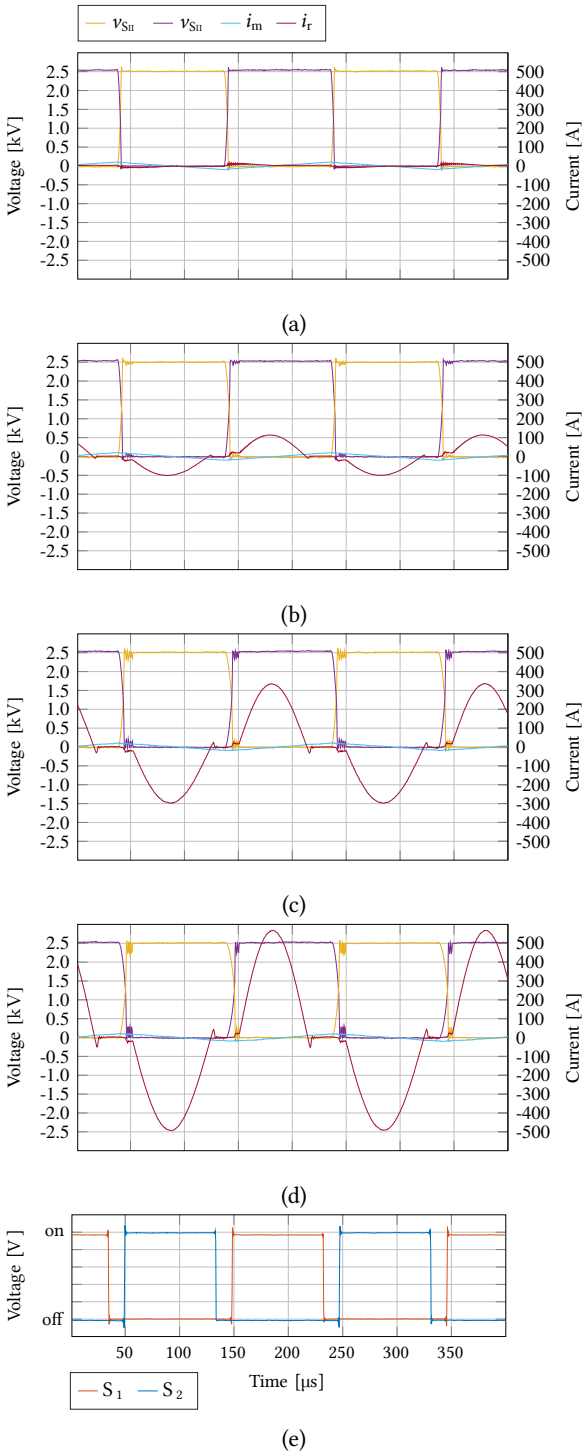


Fig. 4.4 5 kHz is achieved with levels of peak resonant current of a) 0 A, b) 100 A, c) 300 A and d) 500 A. Subfigure e) displays the corresponding switching pulses. All waveforms presented in this figure are obtained with the use of standard commercial devices.

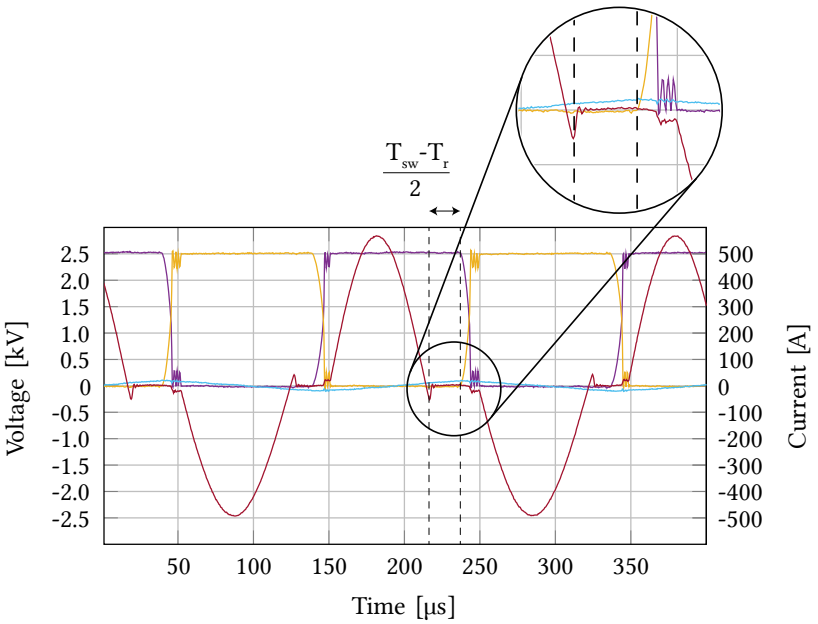


Fig. 4.5 The relatively large difference between the resonant and switching period durations causes the resonant current pulse to end several tens of µs before the GCT turn-off, resulting in increased resonant current peak.

sufficient time for power transfer during the remainder of the period.

In the particular context of the this test setup, the duration of the dead-time could be increased even further, due to the large difference between resonant and switching frequencies. Nevertheless this option is not used as with custom design of resonant tank components this possibility would not be present. Due to charge pre-flooding, the switching losses have been seen to be affected by the peak resonant current conducted by the device during the resonant pulse. Figs. 4.6 shows the turn-off of S_{II} followed by the turn-on of S_I, when the peak resonant current is of 100 A and of 300 A, respectively. This provides a visualisation of the effects resulting in increased switching loss quantified in the previous chapter. In the figures, the switching transition of devices having conducted a peak resonant current of 100 A and 300 A are compared. It can be also seen how while devices *Irradiated A* and *Irradiated B* display significantly shorter switching transitions compared to the standard device, the switching transition of all devices is affected by the peak resonant current value.

It can also be seen in Fig. 4.6 how the switching takes place in quasi-ZVS conditions. This can be concluded by observing the resonant currents for all three devices. The value of the resonant current begins at 0 A, as the resonant pulse is already extinguished before the turn-off of S_{II}. As S_{II} turns *off*, a new resonant pulse begins and the resonant current can be observed to quickly increase. The increase of the current is limited by the value of the magnetising current, which is at its peak after S_{II} is turned *off*. Once the resonant current is equal to the magnetising current, the antiparallel diode of S_I is reverse biased, and the resonant and magnetising current become equal to one another. At this point, ZVS is no longer guaranteed. However, one can see in the figures that in spite of the antiparallel diode of S_I turning *off*, the voltage at the terminals of the IGCT does not dramatically increase. A small oscillatory behaviour takes place, due to the resonance between the resonant inductor and

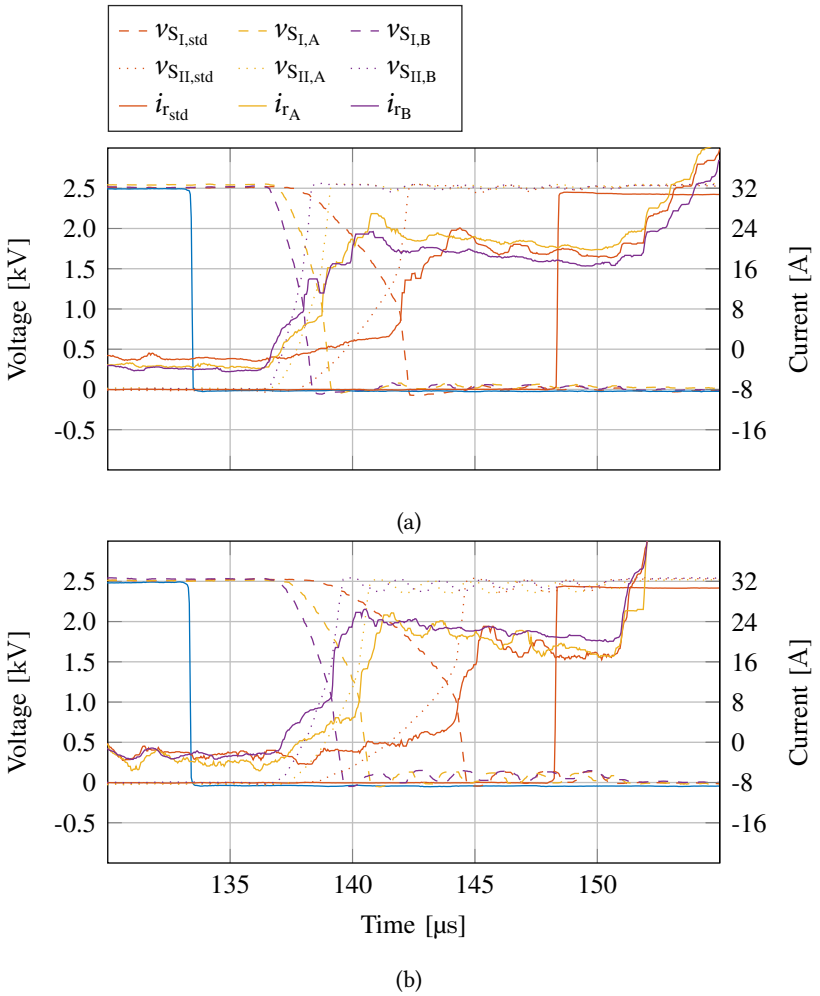


Fig. 4.6 S_{II} turn-off followed by S_I turn-on at a) 100 A and b) 300 A peak resonant current for standard, *Irradiated A*, and *Irradiated B* devices. The increased pre-flooding due to higher resonant current peak results in increased switching times for all three devices.

the IGCT output capacitance, but this does not result in a significant voltage change at the device terminals, as the oscillation takes place around the average value of the resonant capacitor voltage, which is low compared to the dc-link voltage. Note that for the larger value of peak resonant current of 300 A, the voltage on C_r is larger, due to increased conducted charge, resulting in a higher voltage at its terminals. At the end of the dead-time, S_I is turned *on* and the resonant current can be seen to increase again as the resonant pulse continues towards its peak, with the rate of current increase depending on the load. Therefore, while the demonstrated 5 kHz of the devices does not take place in ZVS conditions, the quasi-ZVS conditions present still result in low-loss, safe operation, as was seen in Chapter 3.

4.4 Computation of Losses in Target Application

The test results reported in Fig. 4.4 that display waveforms for 5 kHz IGCT operations were all gathered with the WCU maintaining the deionised water that cools the devices at the very low

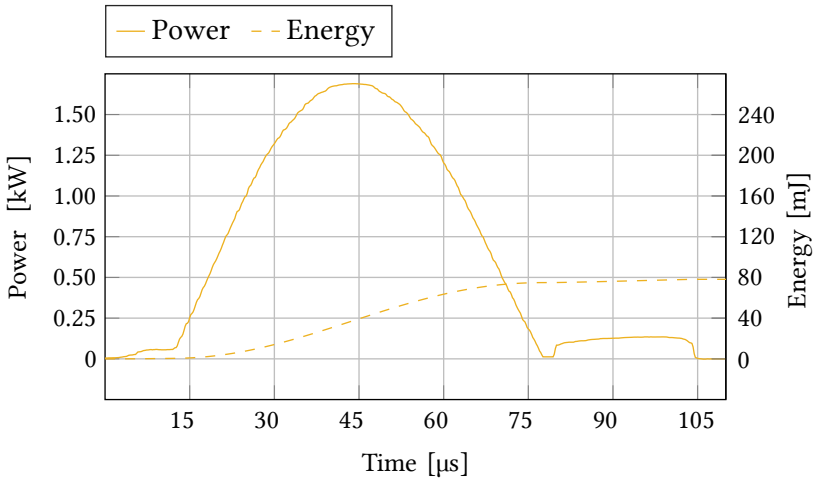


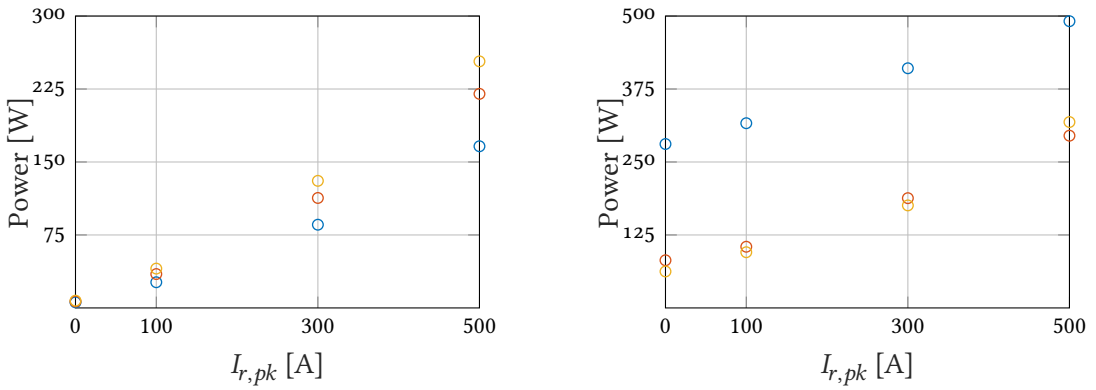
Fig. 4.7 The estimation of conduction loss uses the measured IGCT and diode waveforms combined with the devices' conduction characteristics. The figure displays an example of 300 A peak resonant current waveform conducted by standard devices.

temperature of only 10 °C. Maintaining this low cooling water temperature proved to be possible in the laboratory installation, but in practise this represents an unrealistically optimistic scenario for most industrial applications. Therefore, the evaluation of the junction temperature of the IGCTs under the advantageous laboratory conditions is necessary to estimate the increase in deionised cooling water temperature that would still result in safe operation of the devices. For this purpose, the calculation of the total losses at 5 kHz is the first necessary step.

With the switching losses of the various considered devices having been evaluated in Chapter 3, the conduction losses occurring in the IGCTs under varying levels of load remain to be calculated. To this end, the forward voltage of the RC-IGCTs and their antiparallel diodes are characterised by circulating a varying level of DC current through the device. Precision multimeters are employed for this task. The results of the measurement have been displayed in Figs. 3.2(b) and 3.2(c). Unsurprisingly, the higher irradiation level devices exhibit higher forward voltage at all current levels, both for the GCT and the antiparallel diode.

The devices' forward characteristic is combined with current waveforms as seen in Fig. 4.7, recorded in 5 kHz pulsed operation (tested before continuous operation), resulting in the calculation of conduction loss for each device. Fig. 4.8 displays the loss breakdown in this operating mode. In particular, Fig. 4.8(a) shows that, as expected, conduction losses increase with the irradiation level of the device and with the peak resonant current level. For low resonant current levels (low load), a higher level of irradiation is advantageous as it results in reduced switching losses, while conduction losses remain low due to the low current peak level. The opposite is also true, in that with high resonant current levels (high load), a lower level of irradiation is beneficial as increased switching losses are offset by an advantage in conduction loss.

In Fig. 4.8(b) the sum of the total calculated conduction and switching loss for the three devices is presented. For all three devices, the minimum turn-off current level guaranteeing ZVS conditions is considered to evaluate the switching loss (3 A, 6 A, and 17 A for standard devices, *Irradiated A*, and *Irradiated B*). Note that the total losses of the standard devices are significantly larger than the



(a) (b)

Fig. 4.8 Loss breakdown comparing conduction loss a) and total loss b) during 5 kHz operating with the computed ideal turn-off current value for ○ standard commercial devices, ○ *Irradiated A* devices, and ○ *Irradiated B* devices.

corresponding losses of higher irradiation samples over all the considered peak resonant current range. It can be then concluded that for the considered load levels, the *Irradiated A* and *Irradiated B* devices are preferable. Nevertheless, it should be noted that already at a peak resonant current of 500 A, the total losses of device *Irradiated A* (lower irradiation) are lower than those of device *Irradiated B* (higher irradiation), as conduction losses become more prevalent with the increase of circulated current. Though it was not possible to test higher operating points, it is expected that this trend would continue for increasing test setup loads, favouring devices with lower irradiation levels. Based on this result one could make the assumption that there will exist a peak resonant current level high enough that standard devices are going to outperform increased irradiation devices in terms of total loss.

In fact, this conclusion is not easily drawn based on the presented data: the total switching and conduction losses as summarised in Fig. 4.8(b) assume that the lowest value of turn-off current that maintains quasi-ZVS conditions at 500 A peak resonant current is being employed. If the peak resonant current is increased above 500 A, then loss of quasi-ZVS conditions will occur due do increased levels of charge pre-flooding and switching losses will progressively increase with load level. Therefore it is concluded that while it it possible to predict that devices with lower electron irradiation levels as progressively better suited to the DCT application as power levels increase, it is not possible to estimate the total losses that will be incurred based on the limited data presented in this context.

4.5 Test Setup Thermal Modelling and Junction Temperatures

Since sensing the IGCT case temperature through thermocouples inserted between the case and heatsink is significantly simpler than directly sensing the device's junction temperature, a thermal model of the test setup is employed to estimate the latter.

A simplified drawing of the employed ACS 1000 stack displayed in Fig. 4.2 is shown in Fig. 4.9(a). In total, the stack contains four IGCTs and two diodes (the diodes are not used in the context of this thesis). Due to its intended use in an neutral point clamped (NPC) topology, two additional positions

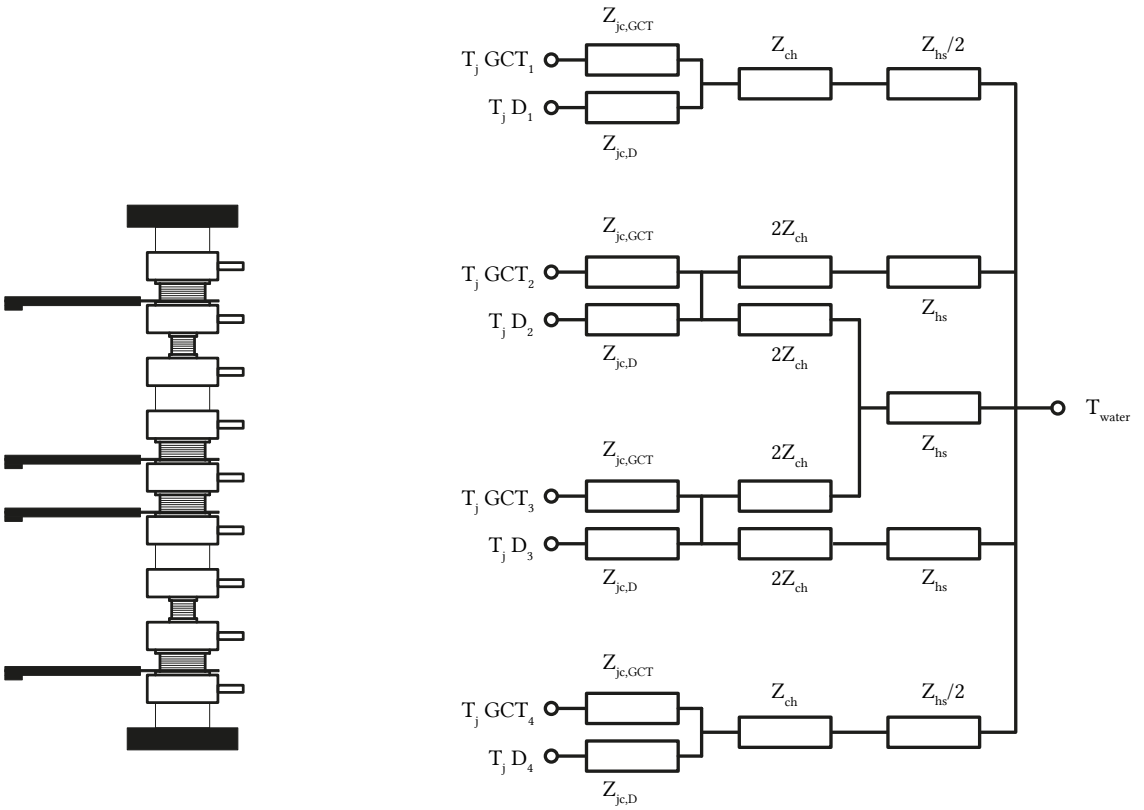


Fig. 4.9 a) The ACS 1000 stack in which 5 kHz IGCT operation is achieved is intended as an NPC stack. It contains 8 totals positions of which two are occupied by clamp diodes, two by spaces, and four by IGCTs; b) the employed thermal model only considers the IGCT devices for the estimation of the GCT and diode junction temperatures.

are occupied by spacers. For this reason, the Foster thermal model in Fig. 4.9(b) only considers GCT and diode temperatures for the four IGCT devices. In the figure, the considered thermal impedances are $Z_{jc,IGCT/D}$, the thermal impedance between GCT or diode junction and case, Z_{ch}, between case and heatsink (assuming double sided cooling), and Z_{hc}, between heatsink and deionised cooling water.

The ACS 1000 stack provides double sided water cooling to each position, where each device is clamped between two heatsinks containing parallel connected water conducts in which deionised water is circulated by the WCU in Fig. 2.15(c). In the model, it is assumed that heat transfer out of the semiconductor devices only takes place through these heatsinks, and all other forms of heat evacuation from the device are not accounted for.

As represented in the drawing in Fig. 4.9(a), the amount of thermal energy provided to each heatsink in the stack is not the same. This is true both for the intended operation of the stack as an NPC stack, and for the resonant SRC-LLC operation discussed in this chapter. Different heatsinks are in contact either with IGCTs (on only one side or both), diodes, or spacers. The different amounts of dissipated energy in these devices result in different thermal conditions in the various heatsinks.

In the specific case of the 5 kHz SRC-LLC operation discussed in this chapter, only the two central

IGCTs are generating thermal losses. For this reason, this section considers a simplified thermal model of the stack that only accounts for these two devices, and the heatsinks which are in contact with them. This simplified model is shown in Fig. 4.10. Note that in this model, the entirety of the energy dissipation that takes place inside the press-pack device is assumed to originate from the GCT, and none from the diode. While this is not a conservative hypothesis, as the junction-to-case thermal resistance of the diode is higher, it is still assumed to be a valid assumption due to the very small conduction time of the diode with the low values of turn-off current employed in SRC-LLC operation.

Most of the parameters required for the thermal model can be easily found. Specifically, thermal impedance between junction and heatsink is provided in the device datasheet an summarised in Tables 4.2 and 4.2, and thermal impedance between heatsink and deionised cooling water is computed by polynomial fitting to data provided by the stack manufacturer and summarised in Table 4.4. The device datasheet also provides data pertaining to the case to heatsink thermal resistance, but not on the thermal capacitance. In practise, the value of thermal capacitance is not necessary to evaluate steady state junction temperature of the IGCTs, but it is still chosen to measure the device case temperature as a function of time under known loss conditions to estimate this last value.

The resulting values are of a resistance of 9.5 K/kW and a time constant of 50 s. Compared to the datasheet value of resistance of 8 K/kW, the result of the measurement is slightly higher. This is not surprising as during testing the stack has been manipulated several times by inserting and removing semiconductor devices, which no doubt will have had consequences on the quality of the thermal interface between device case and heatsink.

Having estimated the parameters of the stack thermal model, the next step consists of the estimation of GCT junction temperatures during 5 kHz operation.

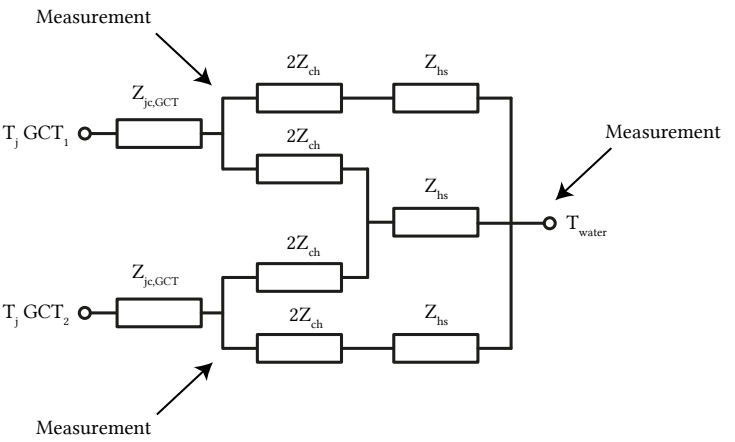


Fig. 4.10 The simplified thermal model used for the estimation of junction temperatures during 5 kHz operation of the setup assumes that only the two employed IGCTs are located in the stack, and that all heat dissipation during operation happens in the GCT, and none in the diode portion of the Si wafer.

4.5.1 Junction Temperature Estimation

With the IGCT operating losses in the specific application having been calculated, these can be combined with the thermal model and the sensed IGCT case temperature to provide an estimation of the junction temperature of the devices, and evaluate whether sufficient margin for safe operation

Tab. 4.2 Foster model values for $Z_{jc,GCT}$ [140].

i	1	2	3	4
R_i K/kW	15.295	5.736	2.684	1.289
τ_i s	0.4820	0.0758	0.0076	0.0023

Tab. 4.3 Foster model values for $Z_{jc,D}$ [140].

i	1	2	3	4
R_i K/kW	25.199	9.964	4.491	2.347
τ_i s	0.4963	0.0802	0.0076	0.0023

i	1	2
R_i K/kW	6.752	7.190
τ_i s	11.324	39.700

Tab. 4.4 A two element Foster thermal model is obtained for the Z_{hs} thermal impedance through polynomial fittig of experimental data provided by the manufacturer.

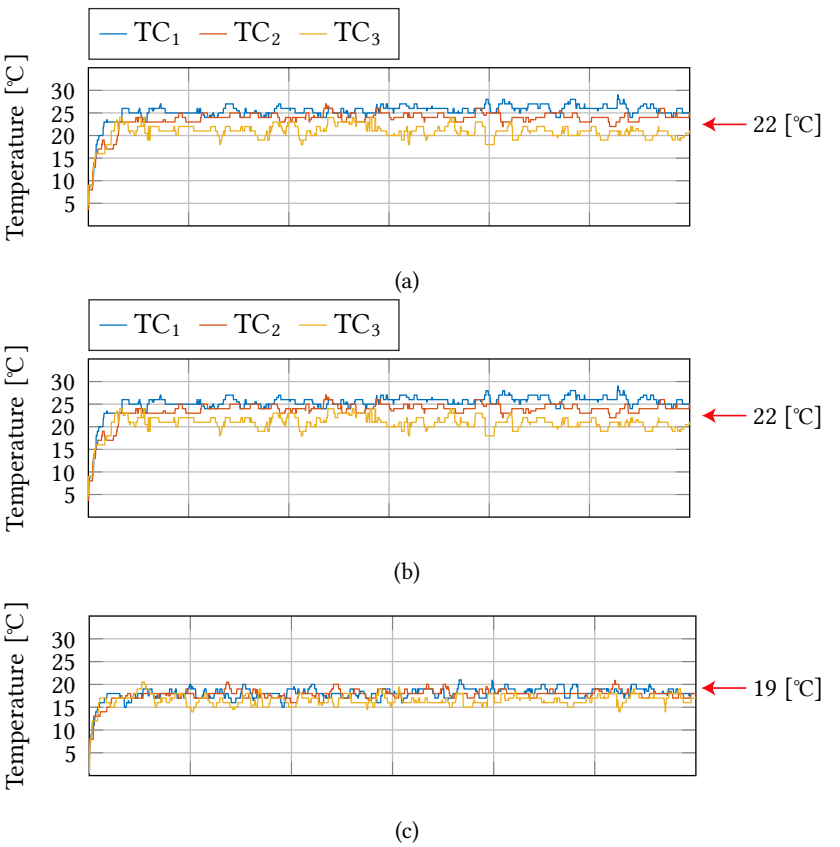


Fig. 4.11 IGCT case temperature during testing with 300 A peak resonant current for a) standard, b) *Irradiated A*, and c) *Irradiated B* devices. The estimated average IGCT case temperature based on the simplified model in Fig. 4.10 is displayed on the right.

exists. With the positioning of the thermocouples in Figs. 4.2(a) and 4.2 being placed in grooves between the device case and heatsink, it is assumed that the sensed values correspond to the case temperature [141].

For this reason, the portion of the thermal model included between the sensed case temperature and

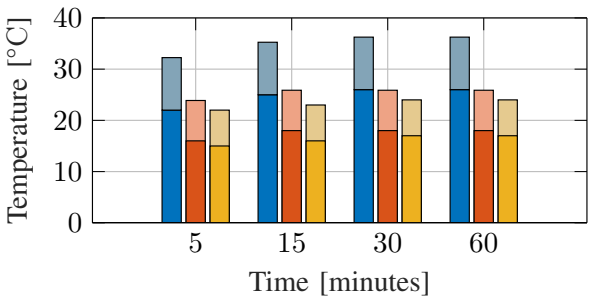


Fig. 4.12 Sensed IGCT case temperature (dark bar) and corresponding estimated junction temperature (light bar) for ○ standard commercial devices, ○ *Irradiated A* devices, and ○ *Irradiated B* devices.

the deionised water temperature is not of interest in this context, and only the thermal impedance between junction and case is considered, as provided by the device datasheet. Once 5 kHz IGCT switching was achieved in short pulses, several hour-long thermal runs of the test setup under these conditions were performed, with the sensed case temperatures being plotted in Figs. from 4.11(a) to 4.11(c), for standards, *Irradiated A*, and *Irradiated B* devices, respectively.

For the mentioned thermal runs, the turn-off current level is set to 17 A for all three tested devices. This turn-off current level is near ideal for the standard devices, but larger than needed for both *Irradiated A* and *Irradiated B*. The sensed case temperature for all three devices during thermal runs is displayed in Fig. 4.11. The figures also display the average estimated case temperature based on the simplified thermal model displayed in Fig. 4.10. This confirms that the thermal model provides satisfactory steady-state estimations at least up to the case temperature values. The estimated losses of the devices at this operating point are of 410 W, 315 W, and 280 W for standard devices, *Irradiated A*, and *Irradiated B*, respectively. For all three devices, the peak resonant current level is of 300 A, which is the value employed for the computation of the losses. As mentioned, the temperature of the deionised water circulated by the WCU is kept at only 10 °C, thanks to the heat exchange with the very cold water from the EPFL cooling system, which is available in the laboratory. While, once again, such a low cooling water temperature is unrealistic for industrial applications, it nevertheless allows to observe the junction temperature gain over that of the WCU, which can then be extended to estimate the junction temperature under different cooling conditions.

Fig. 4.12 shows the sensed case temperatures in the aforementioned operating considerations for standard, *Irradiated A*, and *Irradiated B* devices, respectively, together with the estimated junction temperatures. The estimation of the junction temperature is based on datasheet values of junction to case thermal resistance (25 K/kW) under the assumption that all power dissipation takes place in the GCT portion of the Si wafer, and non in the diode portion. As can be seen in the figure, under the presented operating conditions the estimated junction temperature for all devices is extremely low, leaving significant margin for operation with respect to the junction thermal limit of 115 °C. Neglecting the effect of increased junction temperature on semiconductor losses, in first approximation it is estimated that a WCU temperature of up to 70 °C is acceptable for standard devices. Higher values can be tolerated by increased irradiation devices thanks to their overall lower losses at this operating point.

However, the value of 70 °C is estimated assuming that the turn-off losses of the devices stay constant with an increase of deionised water temperature. In reality, increased junction temperature will

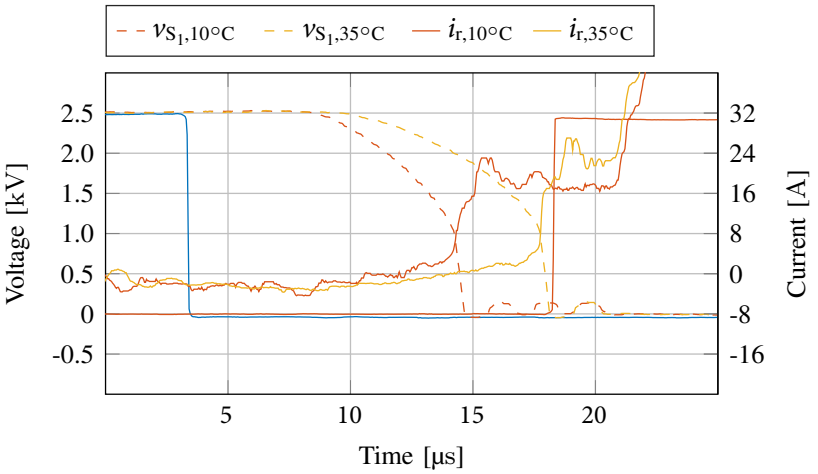


Fig. 4.13 Switching transitions for a single standard device with cooling water temperature of 10 °C and 35 °C. An increase in junction temperature causes an increase in the duration of the switching transition, benefiting voltage sharing between series connected IGCTs.

increase the duration of switching transients, therefore again potentially resulting in partial shoot-through and increased switching losses, in particular for the slower-switching standard devices. The IGCT test setup considered in this thesis does not have the ability to accurately regulate case temperature to provide repeatable testing conditions for the devices, and for this reason thermal effects are not explored further in this context. Nevertheless, thermal runs with a cooling water temperature of 35 °C, which is deemed to be significantly more realistic, were also carried out for standard devices and did not result in failure. Fig. 4.13 displays the different in switching transients associated to increased WCU deionised water temperature, which shows an increase in switching transition duration of close to 3 µs with 35 °C deionised water.

4.6 Summary

This chapter has demonstrated 5 kHz operation of RC-IGCTs in a resonant IGCT test setup emulating the electric stresses to which the devices are submitted in the operation of a resonant LLC topology. Steady state operation is achieved both with standard commercial devices and increased electron irradiation engineering samples. Conclusions from chapter 3 are used to calibrate the appropriate levels of turn-off current, and various values of resonant current are circulated in the setup. Through the combination of current measurement and determination of the conduction characteristics of the devices, conduction losses are computed for the varying operating points, resulting in an evaluation of total loss during operation. Thermocouples are used during testing to sense the case temperature of the devices, which is used together with the calculated power loss and datasheet parameters to estimate the junction temperature of the devices. Thanks to the very efficient cooling system available in the laboratory, the junction temperature of the devices is kept well within safe levels. Nevertheless, the effect of varying junction temperature on turn-off duration, and therefore switching losses, is not evaluated. Having demonstrated 5 kHz operation of the devices, the next chapter presents the extension of this operating mode to series connected IGCTs to achieved increased voltage capability.

5
Resonant Operation of Series Connected IGCTs

With the ability of RC-IGCTs to operate at a frequency of 5 kHz *having been demonstrated in the previous chapter, and with the junction temperature of the devices having been estimated to be well below their thermal capabilities, this chapter focuses on the extension of high frequency resonant operation to the* 5 kV *level by series connection of the IGCTs. The main challenge in this operating mode is the sizing of snubbers of low enough capacitance to be charged by the ultra-low turn-off current during the dead-time, while simultaneously being sufficiently large to guarantee effective voltage sharing between series connected devices. Snubber capacitance values are evaluated, and high frequency series connected operation is again demonstrated in thermal steady state, proving the feasibility of power scaling through increased system voltage, an idea which is the foundation of the bulk power transfer topology considered in this thesis.*

5.1 Introduction

To support the adoption of MVdc power systems on a large scale through the use of SRC-LLC based DCTs, the scalability of the solution to increased voltage levels, which are beyond the capabilities of a single device, must be proven. In particular, the demonstration of the feasibility of such voltage scaling through the series connection of 4.5 kV RC-IGCT devices is a fundamental part of this thesis. In this context, the focus is on the ability of such devices to effectively share voltage in series connection with turn-off taking place under the very low current conditions occurring in the SRC-LLC topology employing series connected devices as in Fig. 5.1. Through thorough experimental characterization, ultra-low snubber capacitor values are evaluated and compared directly, in terms of their impact on the voltage sharing during switching transitions. The changes of behaviour resulting from the use of RC-IGCT engineering samples with increased irradiation levels are also reported in this chapter. These engineering samples exhibit reduced values of turn-off energy at the expense on increased conduction loss, as was discussed in previous chapters. Operation of the IGCTs in series connection at 5 kHz is demonstrated with both standard devices and engineering samples.

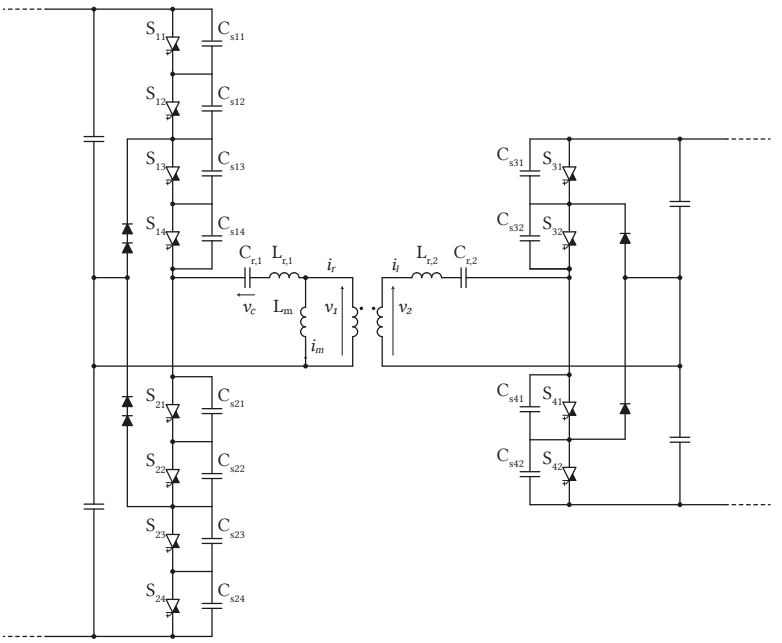


Fig. 5.1 The increased in power and voltage rating for IGCT-based SRC-LLC topology for bulk power transfer can be achieved by using 4.5 kV devices in series connection. NPC topology is employed on both high (10 kV) and low (5 kV) side, with each position being occupied by two series connected devices.

5.2 IGCT series connection in SRC-LLC

One of the options to achieve increased voltage and power rating for an IGCT based SRC-LLC DCT solution is the use of series connected devices. Differently from the IGBT, which can benefit from active voltage balancing, the dynamic and static voltage sharing between series connected IGCTs is guaranteed by snubbers and balancing resistors, respectively, such as those shown in Fig. 5.2.

As the turn-off process of an IGCT is quite similar to that of a traditional GTO, it is for the most part the characteristics of the device itself that determine its switching behaviour, rather than gate driver action. In order for the device to be turned *OFF*, the anode current must be commutated from the cathode to the gate. This is achieved through the application of negative voltage at the gate-cathode junction by the gate drive unit. The applied negative gate voltage sweeps charge carriers from the junction which undergoes reverse recovery and becomes reverse biased. While this portion of the process is under the control of the gate driver unit, the voltage increase at the device's terminals only takes place during the sweep-out of the n-base, which only takes place later in the turn-off process and is affected only by the characteristics of the device. The gate driver unit does not affect this second portion of the turn-off process.

5.2.1 Static Voltage Balancing

The series connection of RC-IGCTs in hard switched applications and the relative snubber sizing is well documented in academic publications and employed in industrial products [142]–[146]. Contrarily, series connection of RC-IGCTs in soft switched applications has rarely been investigated and poses some challenges. While the principles employed are the same as in hard-switched applications,

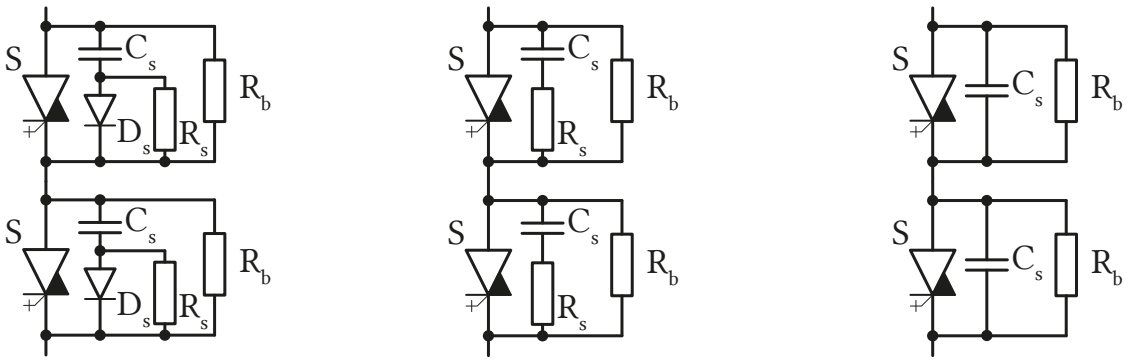


Fig. 5.2 Voltage sharing of series connected RC-IGCTs is for the most part not affected by gate driver action. To ensure reliable static and dynamic voltage sharing between series connected devices, snubber are used. These can employ a) RCD, b) RC, and c) C configurations.

soft-switched conditions present in resonant converters potentially allow for significant simplification of the dynamic voltage balancing snubbers.

Concerning the static voltage balancing resistors (R_b in Fig. 5.2), these achieve their goal by conducting a larger current than the worst-case leakage current of the RC-IGCTs and their antiparallel diodes while the IGCTs are *OFF*. Reference [118] provides a sizing rule in the form of

$$\frac{\frac{V_{dc}}{n}-\frac{\Delta V}{n-1}}{R_b-\Delta R_b}+I_{l0,max}\sqrt{\frac{\frac{V_{dc}}{n}-\frac{\Delta V}{n-1}}{V_{IGCT,0}}}=\frac{\frac{V_{dc}}{n}+\Delta V}{R_b+\Delta R_b}, \tag{5.1}$$

where n is the number of series connected devices, $I_{l0,max}$ is the maximum leakage current of the devices at voltage $V_{IGCT,0}$, R_b and ΔR_b are the values of the balancing resistor and its tolerance, and ΔV is the maximum voltage deviation between the series connected devices. The equation can be solved numerically to calculate the required value of balancing resistors based on the acceptable level of voltage deviation, which is up to the designer. For standard devices, the leakage current $I_{l0,max}$ is of 20 mA at $V_{IGCT,0}$ of 5.5 kV. The corresponding plots displaying expected voltage unbalance and dissipated power as a function of balancing resistor R_b value and tolerance are displayed in Figs. 5.3(a) and 5.3(b), respectively.

The presented plots refer to the worst case scenario in terms of voltage unbalance, which is to say that the balancing resistor R_b of the highest possible value ($R_b + \Delta R_b$) is in parallel with the IGCT with the highest leakage current (20 mA, for the devices in question), while the balancing resistor with the lowest possible value ($R_b - \Delta R_b$) is in parallel with the IGCT with the lowest possible leakage current (0 A). The plots also refer to a constant voltage of 5 kV being applied to the terminals of the devices, without accounting for the $\approx 50\,\%$ duty cycle used in practise.

With the goal of maintaining the difference between the terminal voltage of series connected devices below 500 V (or 10 % of the 5 kV dc link voltage) a value of 10 kΩ is selected for resistors R_b, with a 5 % tolerance. Such resistors are easily available and the reduced voltage imbalance associated with the use of 1 % tolerance resistor is not deemed to be worth the increased cost in this context.

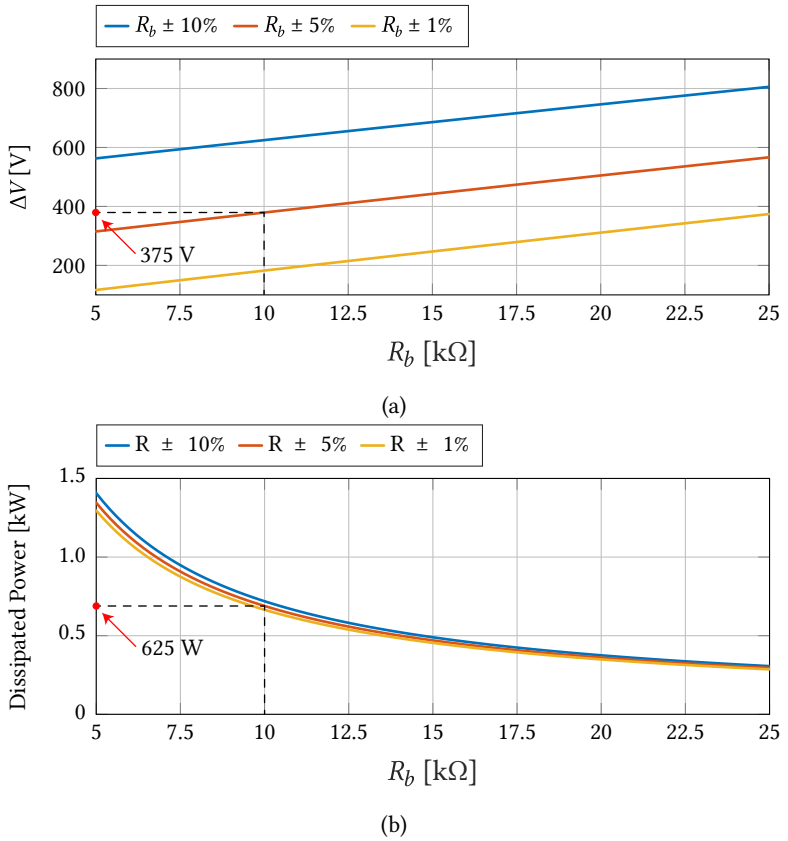


Fig. 5.3 a) A value of static balancing resistor R_b of 10 kΩ ± 5 % maintains the static voltage difference between series connected standard IGCTs below 500 V during blocking; b) The corresponding power dissipated per position is of ≈ 600 W when the devices are blocking.

In practice, there is no difference between the sizing of static voltage sharing snubber in hard- or soft-switched applications.

5.2.2 Dynamic Voltage Balancing

On the other hand, the sizing of dynamic voltage sharing snubbers of the series connected RC-IGCTs is affected both by the maximum acceptable dynamic voltage imbalance, and by the expected turn-off current level. In a conventional LLC-SRC converter, the transmission of power from the primary to secondary side takes place during the resonant pulse, the duration of which is determined by the resonant frequency of the converter's tank. The resonant current pulse and its relatively slow di/dt rise are what allows the turn-on of devices in the LLC-SRC topology to take place in ZVS or quasi-ZVS conditions.

To evaluate the peak dynamic voltage difference between two series connected devices, reference [118] has proposed

$$\Delta V_{dyn} = \frac{V_{dc}}{2} \frac{\Delta C_s}{2C_s + \Delta C_s} \tag{5.2}$$

for hard switched applications, with Fig. 5.4 displaying expected values for tolerances up to 20 % and the employed 5 kV dc link voltage. This is the case as the IGCT output capacitance, typically in the

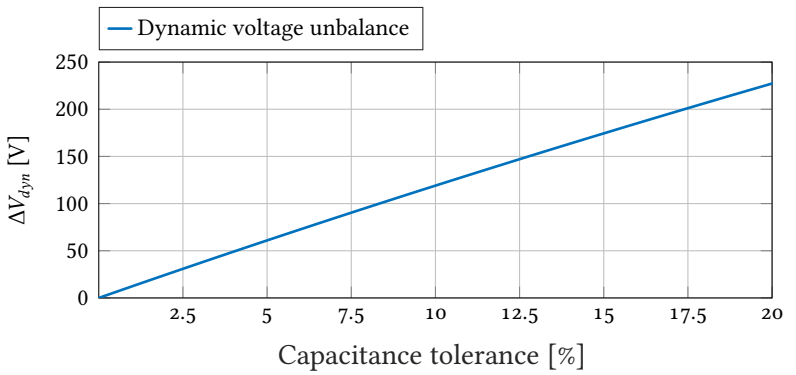


Fig. 5.4 Under the assumption of negligible output capacitance value of the IGCTs, the maximum dynamic voltage imbalance can be estimated based on the dc link voltage and capacitance tolerances.

range 0.8 nF to 1 nF (for 68 mm RC-IGCTs), can be neglected with respect to that of the snubbers. In hard switched applications, the IGCT turn-off current can be in the range of several kA with examples in literature of snubber capacitors in the range of 200 nF to 1 µF. The voltage rise time can therefore be approximated to be equal to the time necessary for the turn-off current to charge the IGCT snubber capacitance. The switching period in hard switching application is usually above 1 ms. Therefore, even with large snubbers, the duration of the dead-time during which the voltage transition must be completed is small with respect to the switching period.

The low current turn-off in the SRC-LLC poses a more significant challenge in terms of dynamic voltage balancing. The sum of the gate driver delay t_{delay} and the voltage rise time t_{rise} must be lower that the selected dead-time t_{dt} to avoid losses linked to partial shoot-through and loss of quasi-ZVS conditions. While a low turn-off current has a relatively small impact on the gate driver delay t_{delay}, the duration of the voltage rise is significantly extended by a reduction in turn-off current when compared to hard-switched applications. This is potentially exacerbated by the presence of a capacitive snubber in parallel with each device.

An increased voltage rise time due to slow snubber capacitance charging is incompatible with the desired increase in switching frequency that can be achieved with a low turn-off current. An increase in dead-time duration to ensure low-loss commutation is not acceptable at the considered 5 kHz switching frequency, as the dead-time and total switching period durations of 15 µs and 200 µs, respectively, are already in a comparable range.

Therefore, to prevent the switching transition with series connected devices from exceeding the dead-time and resulting in loss of quasi-ZVS conditions, the snubber design must be such that the IGCT transitions are as fast as possible. To this end, a reduction in snubber capacitance size is required for high frequency operation in series to be possible. Still under the assumption that the IGCT output capacitance is negligible, a very simple sizing rule is established as

$$C_{max} = \frac{i_{off} \cdot t_{dt} \cdot n}{4V_{dc}}, \tag{5.3}$$

where i_{off} is the IGCT turn-off current, t_{dt} is the dead-time, V_{dc} is the dc bus voltage and n is the number of series connected IGCTs per position. As an example, for two series connected devices with a 5 kV dc link voltage, 50 A turn-off current and a dead-time of 15 µs, this results in a maximum snubber capacitance of 75 nF.

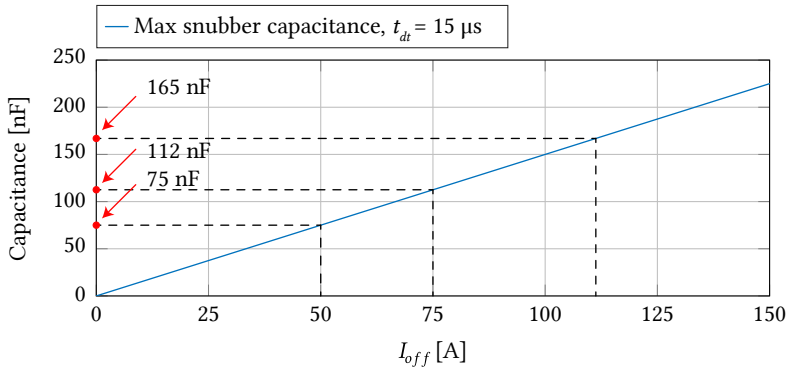


Fig. 5.5 The selected snubber capacitance value must be lower than the computed maximum value according to 5.3. The figure displays the maximum capacitance values for a dead-time duration of 15 µs. The actual employed values must remain below the maximum values, and are selected to be 40 nF, 70 nF, and 100 nF.

Due to the ultra-low snubber capacitance values employed, it will be seen that 5.2 does not hold true in this context. The estimation is intended to be applied to hard-switching applications, and ultra-low values of turn-off current and capacitances will be shown to perform differently.

In spite of the challenges associated with low current turn-off of series connected IGCTs, it should be reiterated that operation in a soft switched topology also brings very significant advantages. In particular, almost independently from the load condition, the turn-on of the IGCTs is performed in ZVS or quasi-ZVS conditions. Because of this, there is no danger linked to the discharge of the snubber capacitance into the device as it turns *ON*, and therefore, in principle, no need for the typically employed snubber resistor shown in Figs. 5.2(a) and 5.2(b). This makes the turn-on process non-critical and allows the use of purely capacitive snubbers in soft-switched topologies with significant advantages in terms of snubber physical size, cost and efficiency. Additionally, the current rate of increase at the time of IGCT turn-on is limited by the resonant tank inductive elements to a few A/µs. This eliminates the risk of high di/dt reverse recovery of the GCT antiparallel diode and therefore the need for di/dt clamp circuitry. These two factors significantly simplify the converter structure, as discussed in Chapter 2.

This chapter focuses on series connected turn-off characterisation with turn-off current values of 50 A, 75 A and 110 A to identify relevant trends through DP tests. Snubber capacitance values of 40 nF, 70 nF, and 100 nF, respectively, are selected. These are below the maximum values corresponding to the set turn-off currents, as seen in Fig. 5.5.

In addition to voltage sharing, device losses are also measured as a function both of turn-off current and snubber capacitance values. The interest here is to evaluate whether the addition of snubber capacitance might negatively affect switching losses and therefore result in less favourable conditions for operation at 5 kHz compared to devices operating with no parallel capacitance.

5.3 Configuration of the Test Setup for Series Connected DP Tests

To test low current IGCT turn-off in series connection, the test setup is configured with two series connected devices per position, both on the IGCT and rectifier diode sides. This is displayed in Fig. 5.6. The values of the employed components is listed in Table 5.1. The objective of the tests is to

Tab. 5.1 Values of passive component of the test setup.

C_{dc}	L_{cl}	R_{cl}	C_{cl}	C_s	R_s	R_b	L_m
1.3 mF	18 µH	2 Ω	7.4 µF	40 nF, 70 nF, 100 nF	0 Ω, 5 Ω	10 kΩ	6.3 mH

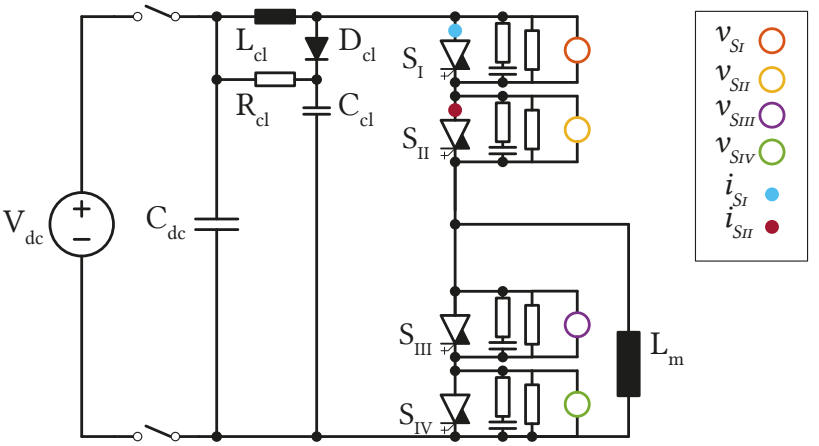


Fig. 5.6 Test setup configuration and for DP testing, with two RC-IGCTs per position. Each GCT is provided with an RC snubber for dynamic voltage sharing, and a balancing resistor for static voltage sharing.

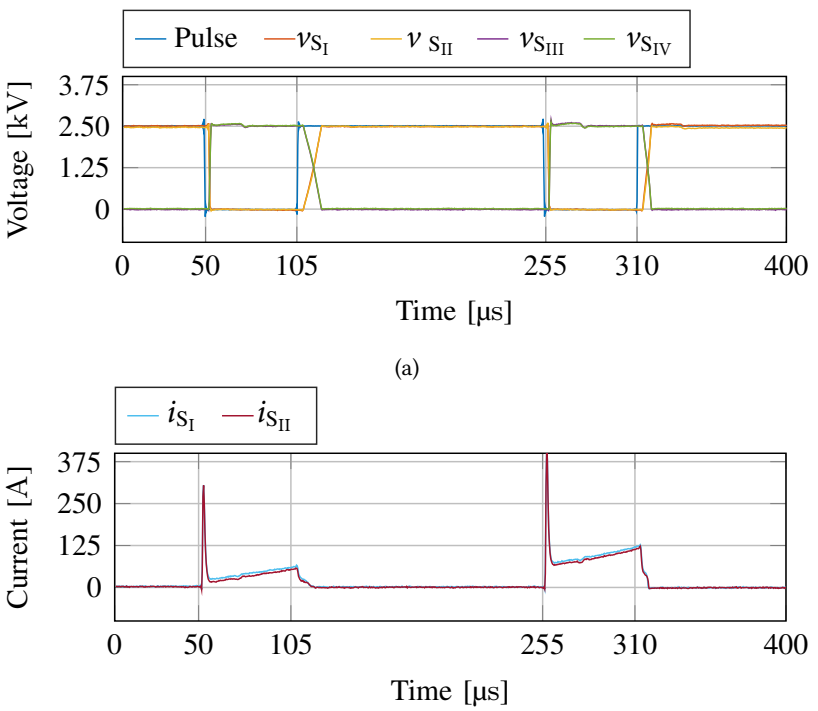


Fig. 5.7 a) The turn-off voltage and b) turn-off current level at the end of each pulse is determined by the pulse duration, which is of 55 µs in the test results.

characterise three crucial parameters, as a function of the turn-off current and snubber capacitance. The first is the voltage rise time, which is relevant for the purpose of ensuring quasi-ZVS operation. Considering the low values of the turn-off current, the duration of the voltage rise is expected to be increased compared to hard switched conditions. The second, is the turn-off energy in series connection, ensuring equal distribution between the two series connected devices. Thanks to the measurement of terminal voltage and current in each of the DUTs, as displayed in Fig. 5.6, the switching energy is calculated as the integral over time of the power dissipated in the device. Finally, the difference in voltage between the two DUTs is monitored, as the use of small snubbers increases the risk of dynamic voltage unbalance. An example of a typical test result in this configuration is shown in Figs. 5.7(a) and 5.7(b) in terms of sensed voltages and currents, respectively.

5.4 IGCT Low Current Turn-Off

Standard, *Irradiated A*, and *Irradiated B* devices are methodically tested in series connected operation through DP tests, and their turn-off is characterised with varying levels of turn-off current and snubber components. The same commercial gate driver units are employed in all tests, and only the GCTs are replaced.

5.4.1 Commercial RC-IGCTs

Figs. 5.8 and 5.9 display the measured electrical quantities of the test setup during turn-off with 5 Ω and 0 Ω snubber resistance, respectively. Both figures display on the left side results for S_1 and on the right side results for S_2. The values of turn-off current used are, from top to bottom, 55 A, 75 A and 110 A. Small discrepancies in the values of turn-off current are due to sensing with high-current 3 kA probes, which are the only ones available during measurements.

To summarise the results in a concise fashion, Fig. 5.10 displays the values of the voltage rise times, turn-off energies and maximum voltage difference between the DUTs during the turn-off process. Based on the figure, two expected effects are observed:

- A larger snubber capacitance (while still very low) results in slower voltage rise, but better voltage sharing and lower turn-off energy in the DUTs.
- A larger turn-off current results in faster voltage rise, higher turn-off energy and larger voltage imbalance between series connected devices.

There are multiple observations that are relevant to series connected SRC-LLC operation. First and foremost, comparing Fig. 5.8 and Fig. 5.9, one can see that the main observable difference is the oscillations in current before turn-off that are present in the case of $R_s = 0\,\Omega$. This is not due to the turn-off process itself, but rather the turn-on of the device, which takes place in hard-switched conditions, with voltage present on the devices' terminals.

Because of the hard turn-on, the snubber capacitance quickly discharges in the device, causing large current oscillations that are damped over time. A longer duration of the *ON* time for S_I and S_{II} would have allowed further damping of these oscillations, but the constant *ON* times that are maintained throughout the tests do not allow this. It is important to note that the presence of snubber resistance does not affect low-current turn-off of the device.

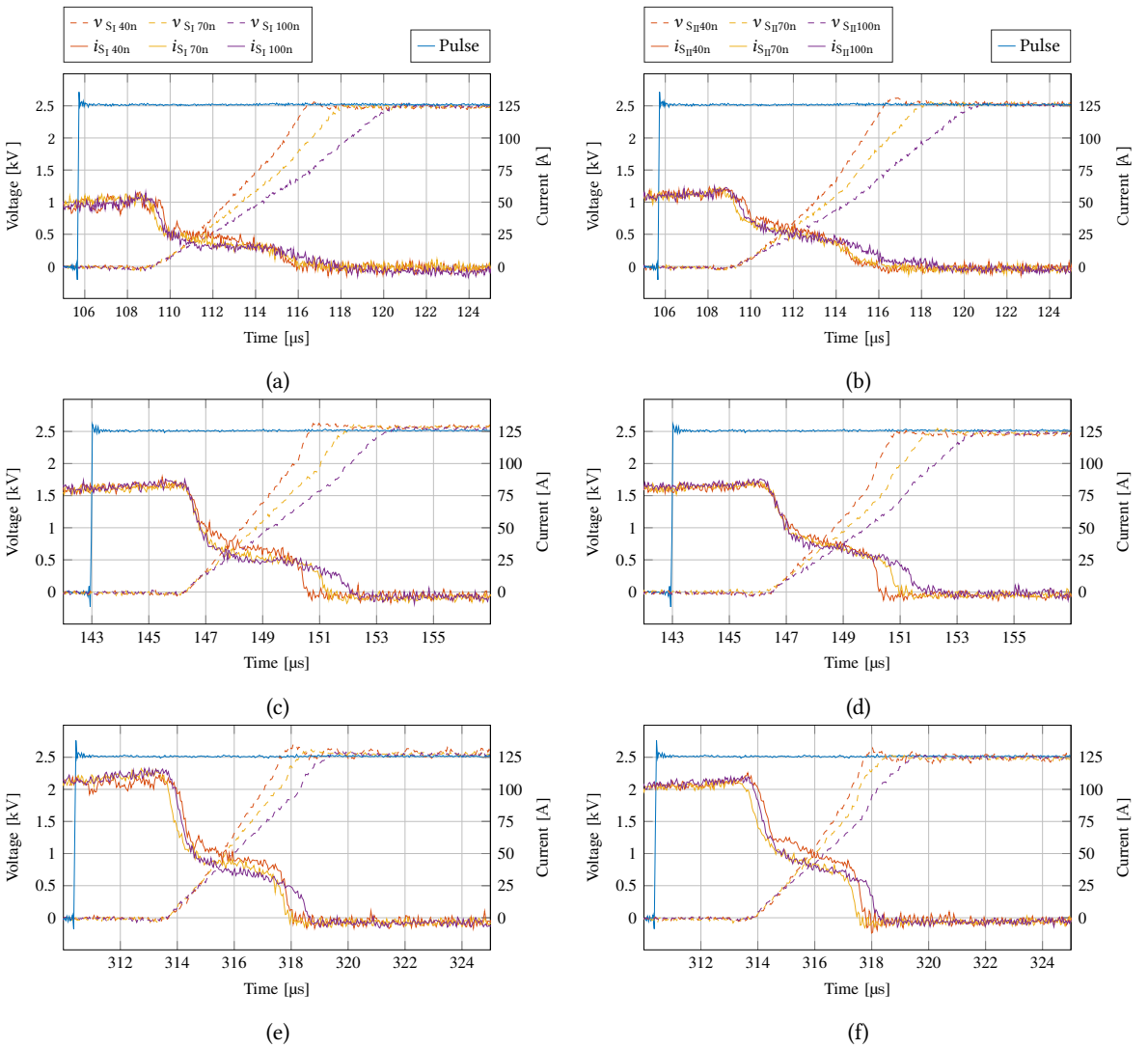


Fig. 5.8 Low current standard RC-IGCT turn-off with $R_s = 5\,\Omega$. From top to bottom, the turn-off current level is increased from 55 A to 75 A to 110 A. Figs. (a), (c) and (e) refer to S_1, while Figs. (b), (d) and (f) refer to S_2. The switching pulse is shown in blue and using inverse logic in all of the subfigures.

The maximum voltage difference between the series connected devices never exceeds 300 V, with this value only being reached for the very small snubber capacitance of 40 nF and the largest considered turn-off current of 100 A. This is due to higher turn-off current and the smallest snubber capacitance resulting in higher dv/dt and therefore exacerbating any asymmetry in switching delay or gate driver action. All other combinations of snubber capacitance and turn-off current result in smaller peak dynamic voltage imbalances. Note that this is in contrast with what was expected from 5.2, therefore showing how the assumption of the turn-off voltage sharing being only dependent on relative snubber tolerances cannot be applied to ultra-low snubber capacitance values. Nevertheless, the result provides the important information that the difference in voltage between the two devices can be kept below 10 % of the device dc voltage, which is relevant considering this is the tolerance of the employed snubber capacitors.

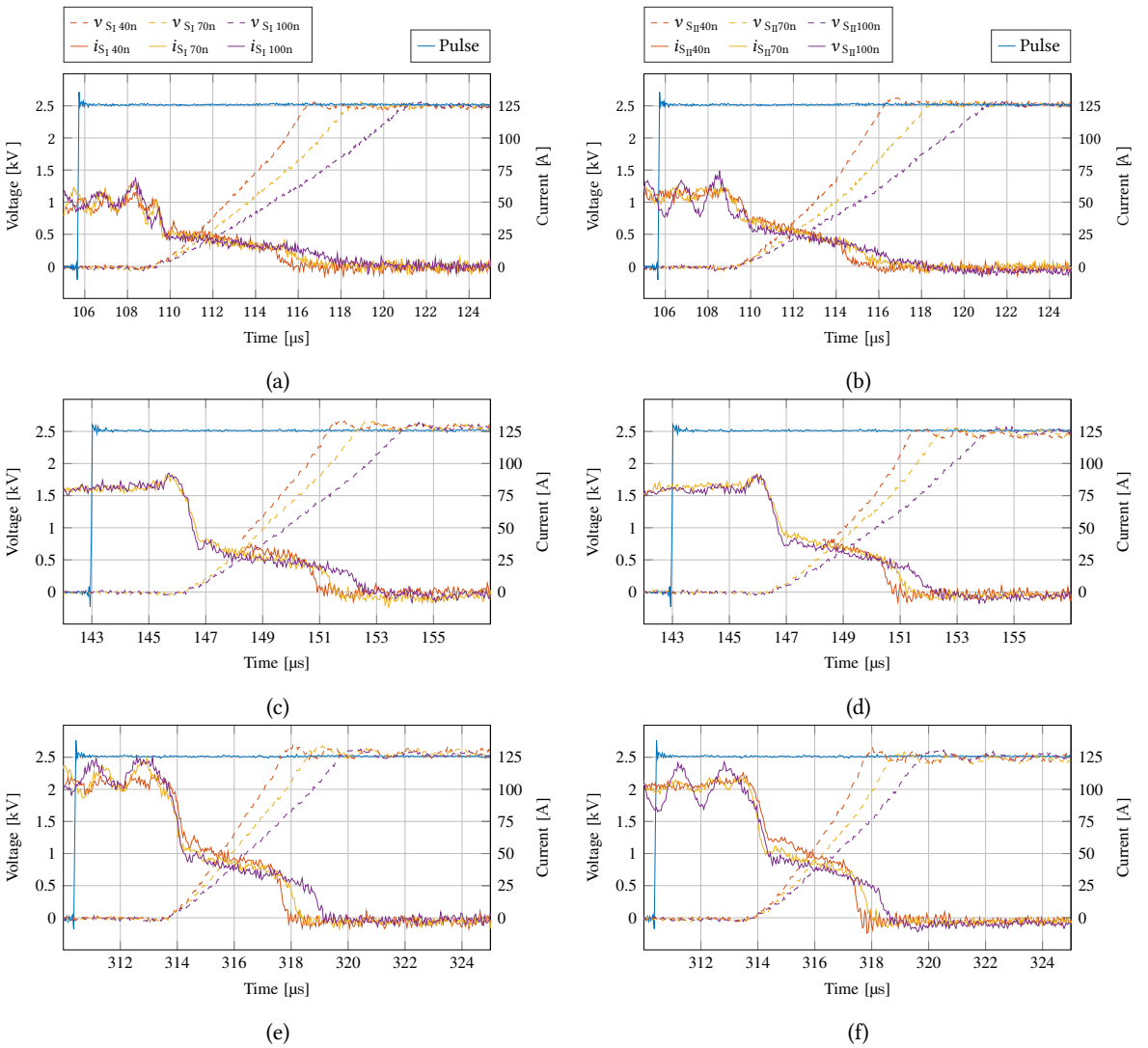


Fig. 5.9 Low current standard RC-IGCT turn-off with $R_s = 0\,\Omega$. From top to bottom, turn-off current level of 55 A, 75 A and 110 A. Figs. (a), (c) and (e) refer to S_1, while Figs. (b), (d) and (f) refer to S_2. The turn-off with $R_s = 0\,\Omega$ is similar to $R_s = 5\,\Omega$, except for current oscillations due the turn-on.

In all the combinations of turn-off current and snubber capacitance, the voltage rise time remains well below 10 µs. This is again significant since, as discussed, with an increased dc transformer switching frequency a fast transition between conducting and blocking state is necessary to maximise the portion of the period available for power transfer. Considering it has been shown that turn-off duration is significantly affected by the peak resonant current conducted during the period, it is desirable to have margin to the 15 µs dead-time duration.

From a general perspective, as different applications have different requirements in terms of admissible dead-time, turn-off energy, and dynamic voltage imbalance, it is not possible to provide a broad recommendation for the optimal value of snubber capacitance under low current switching conditions.

Nevertheless, based on the tests that have been carried out, a suggestion can be made as to which

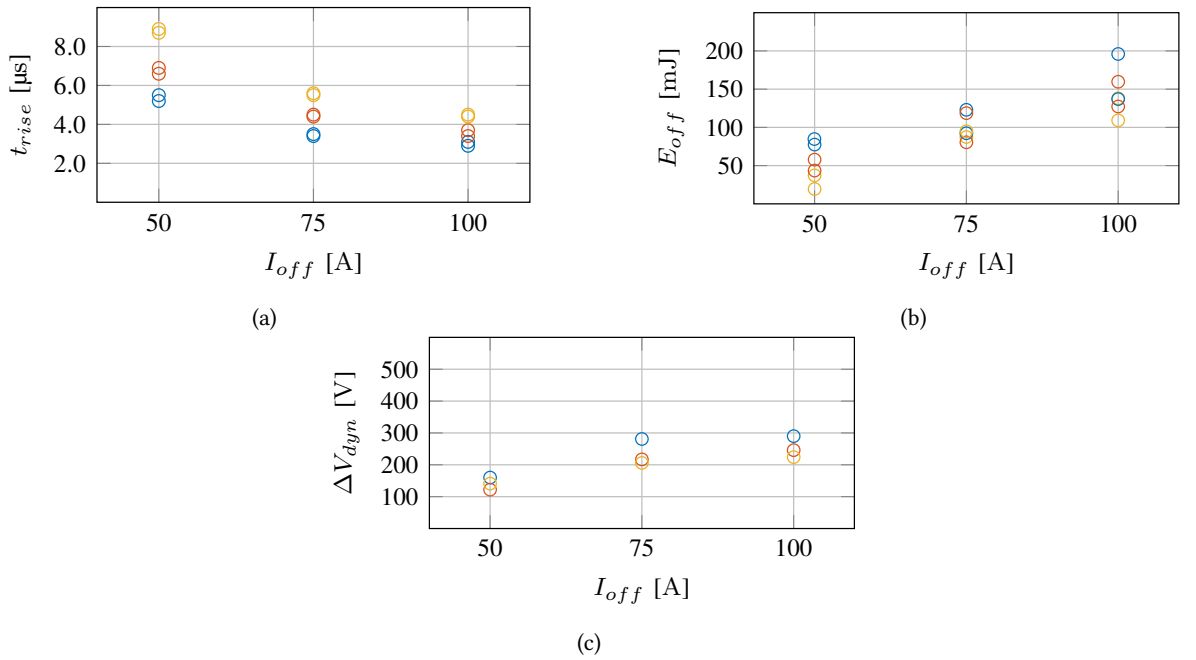


Fig. 5.10 Rise time, switching energy and ΔV_{dyn} during turn-off of standard RC-IGCTs as a function of I_{off} for: ○ $C_s = 40$ nF, ○ 70 nF, and ○ 100 nF, respectively.

criteria to use with the goal of selecting an appropriate value of turn-off current and snubber capacitance in a given application. First, the he maximum duration of the dead-time must be determined, based on the portion of the period required for power transfer, and the relative considerations related to the associated losses. With the duration of the dead-time set, several combinations of turn-off current and snubber capacitance will allows to complete the switching transition within the selected dead-time. Combinations of low values of turn-off current and low snubber capacitance will provide lower switching losses, but risk increased voltage unbalance between series connected devices due the the snubber capacitance being comparable to the output capacitance of the devices. If a combination of higher turn-off current and snubber capacitance are selected, turn-off loss is increased, but so is the prevalence of the snubber capacitance value over that of the devices'. When snubber capacitance becomes large enough that the effect of the devices becomes negligible, then the maximum voltage imbalance is determined by the capacitance tolerance and 5.2 applies. This discussion is based on limited considerations concerning turn-off energy and voltage balancing, but additional factors such as device reliability, operating temperature, and others, should be accounted for to have a complete picture. Finally, it should be highlighted that the removal of the snubber capacitance is also not a feasible option, as further tests have shown that in the absence of snubbers the voltage sharing between series connected devices is not adequate for safe operation.

5.4.2 Higher Electron Irradiated RC-IGCTs

Having established the performance of standard IGCTs in low turn-off current and low snubber capacitance conditions as a benchmark, the performance of *Irradiated A* and *Irradiated B* engineering samples can be tested and compared. The devices are made to perform the same tests as the commercial GCTs. An example of direct comparison of the switching waveforms is shown in Fig. 5.11 for a turn-off

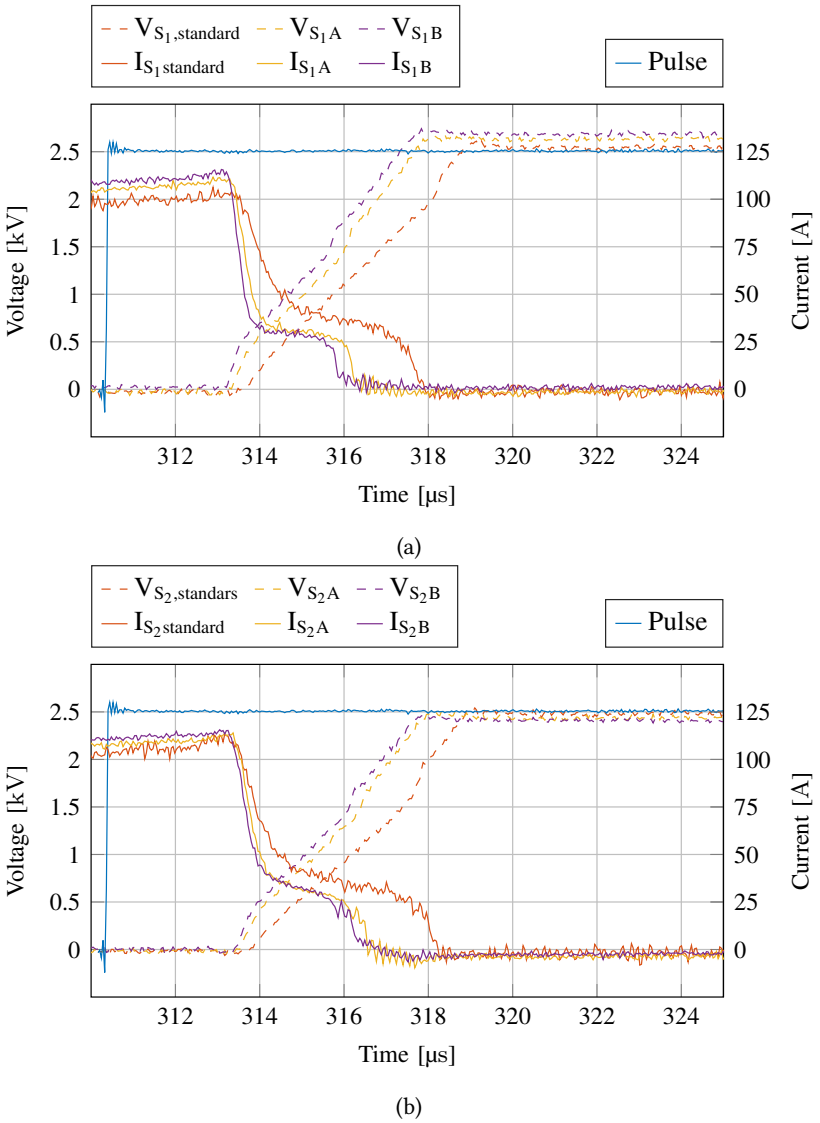


Fig. 5.11 Comparison of turn-off of (a) S_1 and (b) S_2 at 110 A for standard, *Irradiated A* and *Irradiated B* devices, with a $C_s = 100$ nF.

current level of 110 A and a snubber capacitance value of 100 nF, and the difference in performance is summarised in Fig. 5.12. This figure compares the devices in terms of turn-off energy, voltage rise times and peak dynamic voltage imbalance. For each value of snubber capacitance, one plot in Fig. 5.12 is presented. From left to right, values of 40 nF, 70 nF and 100 nF are used.

The first row of the figure, pertaining to turn-off energy, shows a clear distinction in behaviour between the commercial and *Irradiated A* and *Irradiated B* GCTs. The difference between device performance is more pronounced the lower the snubber capacitance value. For the *A* and *B* devices, no matter the turn-off current value, the turn-off energy never exceeds 100 mJ. In contrast, the turn-off energy in the standard GCTs reaches almost double this level end exhibits strong variations with turn-off current value, ultimately due to the longer carrier lifetime and increased junction sweep-out time of the standard devices. One can also see by comparing the plots how an increase in snubber

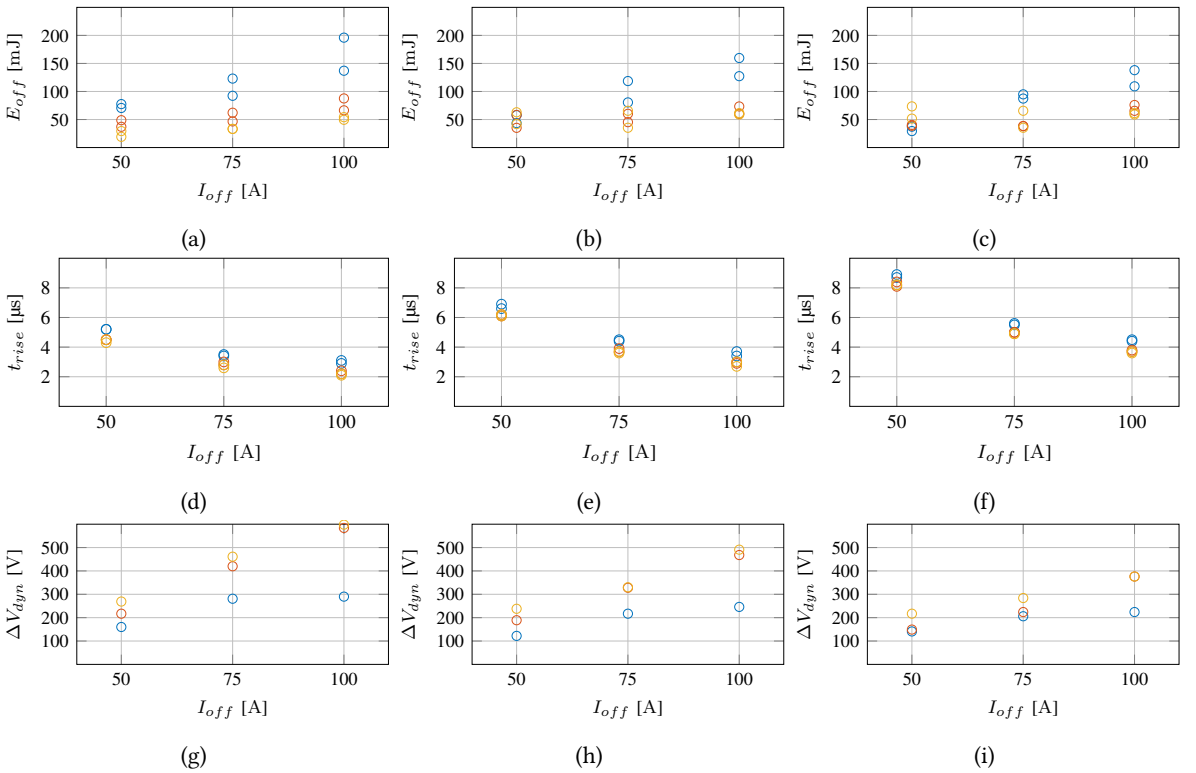


Fig. 5.12 Comparison of switching energy (top), voltage rise time (center) and ΔV_{dyn} (bottom) during turn-off as a function of I_{off}. The snubber capacitance is of 40 nF, 70 nF, and 100 nF in each column from left to right. The employed GCTs are: ○ standard commercial devices, ○ *Irradiated A*, and ○ *Irradiated B*.

capacitance value, while it does not significantly affect the switching energy for irradiated devices, does reduce the difference in switching energies between S_I and S_{II} for all tested GCTs. This is because as the dynamic voltage sharing improves, so does the sharing of the turn-off energy, since the current in the devices is the same due to their series connection.

The second row of Fig. 5.12 displays the trends in voltage rise time between the tested GCTs, which are as expected. The figure shows how the voltage rise time is a for the most part a function of turn-off current and snubber capacitance values. This is desired, as the purpose of the addition of snubbers in parallel to the devices is for the snubber to be the primary factor determining the GCT voltage sharing. It can be clearly seen how increased levels of turn-off current result in faster voltage rise, and also how increased snubber capacitance values result in a slower voltage rise. While standard GCTs are slightly slower than their irradiated counterparts across the board, this difference is small compared to that determined by snubber capacitances.

Finally, the last row of the figure displays the peak voltage differences between S_I and S_{II} during turn-off. Here, one can again see a difference in trends between the commercial and *Irradiated A* and *Irradiated B* devices. While the commercial devices exhibit a clear increase in voltage difference between a turn-off current of 50 A and 75 A, this difference is proportionally much less significant when stepping up from a turn-off current of 75 A to 100 A. This is not the case with *A* and *B* GCTs, which increase their peak voltage difference almost linearly with the increase of the turn-off current, likely due to the better turn-off delay matching of standard devices. On the other hand, all devices

Tab. 5.2 Values of passive component of the test setup.

C_{dc}	L_r	C_r	C_s	R_s	R_b	L_m
2.6 mF	8 µH	85 µF	20 nF	0 Ω	10 kΩ	6.3 mH

exhibit the desired reduction in voltage difference with the use of a larger snubber capacitance, with the irradiated devices reducing the peak voltage difference further than standard devices, especially at higher turn-off current levels. The characterisation of RC-IGCTs that underwent increased irradiation levels yields the expected results, and the comparison with standard commercial devices highlights a case for their employment in the the proposed SRC-LLC based DCT application, also in series connection. The devices provide a reduction in turn-off loss in the device of up to 50 % compared to standard devices with the use of snubbers, at the cost of an increased, but still safe, voltage unbalance. Ultimately, as the conduction losses of increased irradiation devices are also higher, this trade-off needs to be carefully examined in difference applications and power ratings.

The DP tests described in this chapter are used to characterise only the low current turn-off behaviour of the series-connected IGCTs under test. While the DP test would usually provide useful information concerning the device turn-on as well as turn-off, this stage of operation is not critical in ZVS and quasi-ZVS operation. Additionally, the DP test does not provide equivalent turn-on conditions to those witnessed by the devices in resonant operation: in the DP test setup, the DUTs are turned on with the full DC link voltage being applied to the terminals of the series connection of S_I and S_II, and the current rate of increase is limited by the clamp circuit. This results in the snubbers in parallel with these two devices being charged, and the snubbers in parallel with S_{III} and S_{IV} being completely discharged. At the time of turn-on, the snubbers in parallel with S_I and S_{II} quickly discharge into the device and the snubber resistor (if present), while the snubbers in parallel with S_{III} and S_{IV} provide a current path bypassing L_m and resulting in a large current spike limited only by the clamp inductor L_{cl}, as can be seen in Fig. 5.7(b). Soft turn-on would instead result in a virtually lossless commutation. It is for this reason that tests are also carried out also with no snubber resistor ($R_s = 0\,\Omega$). While this would lead to high current peaks during turn-on under hard switched conditions, under soft turn-on the snubbers are naturally discharged before the turn-on of the device, leading to lower losses and smaller snubbers.

5.5 Resonant Operation

By combining the low current IGCT series connected turn-off characterisation presented in this chapter with the resonant 5 kHz operation demonstrated in Chapter 4, the high frequency operation of the devices can be extended to the 5 kV voltage level. For this purpose, the setup is configured as shown in Fig. 5.13. The operating principle in this context is the same as that employed in Chapter 4: the setup imitates the operation of the SRC-LLC through the addition of a resonant tank and rectifier stage, which allows the circulation of power through the tested IGCTs and back to the input capacitors. The resonant tank is composed by L_r, C_r, and L_m, with the latter conducting the equivalent of the transformer magnetising current i_m. A first voltage source V_{dc} charges the dc-link capacitors, while a second voltage source v_A (*MAGNA* 20 V, 2.2 kA) provides the simulated converter load resonant current i_r by simulating a voltage difference between the terminals of the rectifier and IGCTs. Tab.

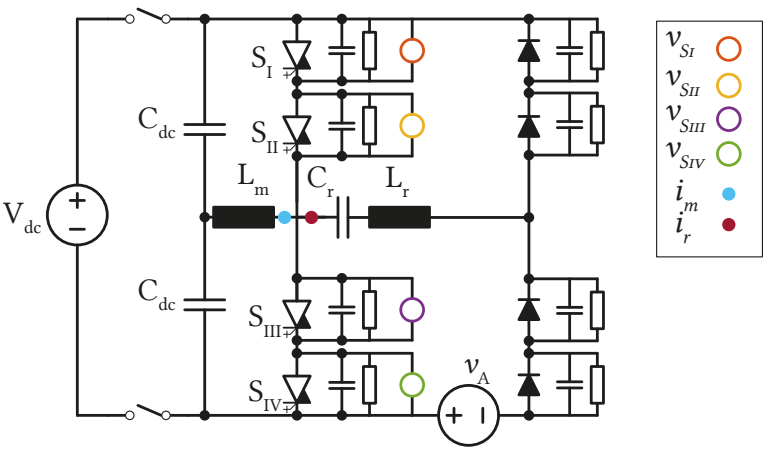


Fig. 5.13 Test setup configured for resonant operation. C_{dc} = 1.3 mF, L_m = 6.3 mH, C_r = 85 µF, L_r = 5.5 µH, f_r = 7.35 kHz.

5.2 displays the component values in this context.

During testing, the setup is operated at the maximum possible circulated power by setting v_A = 20 V. Fig. 5.14 displays the sensed voltages and currents. Compared to operation without series connected devices, the peak resonant current achieved is lower because of the increased forward voltage drop due to the series connection of both IGCTs and rectifier diodes. The resonant frequency of the tank is the same as that of Chapter 4, that is to say 7.35 kHz. In this chapter, the minimum turn-off current level tested for series connected devices has been of 50 A, corresponding to snubber capacitance value of 40 nF. Nevertheless, in Chapter 3 the ideal turn-off current for standard IGCT turn-off has been identified to be equal to 17 A for the employed standard commercial devices and a dead-time duration of 15 µs. The incoherence between the choices adopted in these two different chapters is due to the work in the present chapter having been carried out before what was presented in Chapter 3. Before identifying the ideal turn-off current level, it was deemed necessary to evaluate whether series connected IGCT turn-off was at all possible at the desired low value of turn-off current, with the corresponding very lo levels of snubber capacitance. At the time, it was thought to be unlikely that a turn-off current value lower than 17 A would be suitable, due to the large rated turn-off current of the devices under test. Nevertheless, the trends identified in this chapter, and in particular the advantageous correlation between further decreased turn-off current and improved dynamic voltage sharing (considering a constant snubber capacitance value) have pointed toward a reduction of the devices' turn-off current as being a viable and even advantageous option.

For this reason, the resonant operation presented in this section uses a snubber capacitance C_s of only 20 nF, coupled with a turn-off current level of 17 A. The dead-time is increased from the value of 15 µs, used with individual devices, to 20 µs, as the increased capacitance due to the presence of capacitive snubbers caused partial shoot-though and increased losses at a dead-time level of only 15 µs, which was used for the 5 kHz operation of non series connected devices. Note also that this section discussed only standard commercial devices, as the four required devices for series connected resonant operation were not available in the case of irradiated engineering samples. Nevertheless the extensibility of the presented result to irradiated devices is ensured by the standard devices representing a worst case scenario for resonant operation, as irradiated devices would result in faster switching transition and potentially a reduction of dead-time.

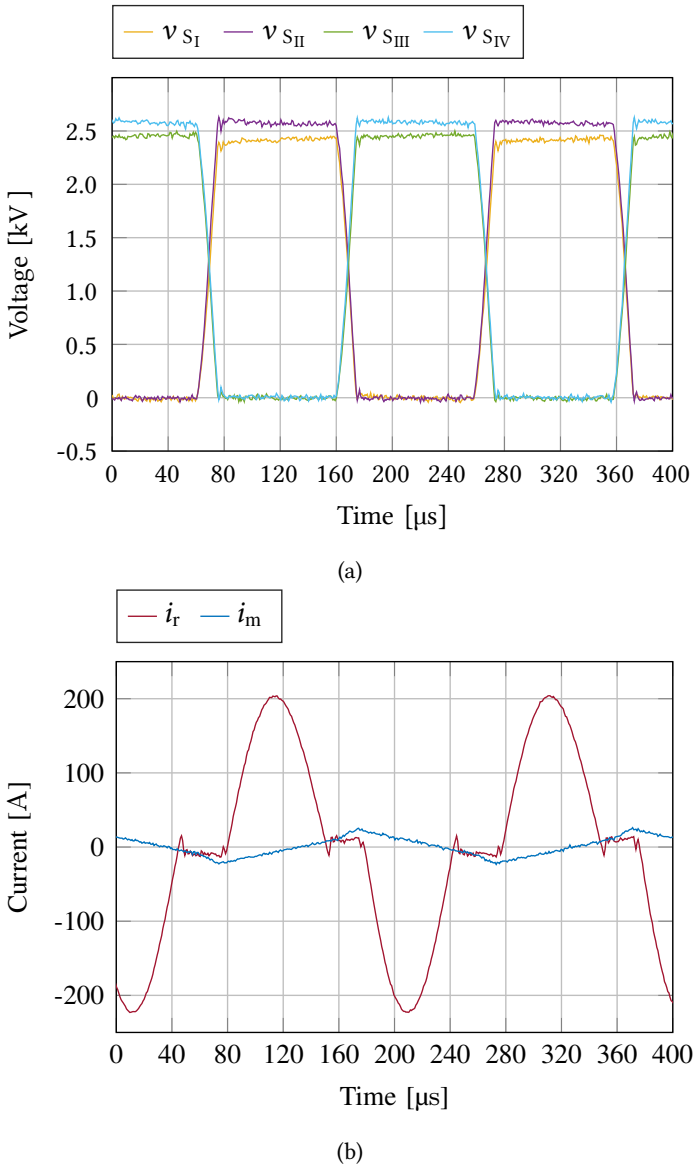


Fig. 5.14 a) Device voltage and b) current during 5 kHz RC-IGCT series connected resonant operation employing a 17 A turn-off current level and only 20 nF snubber capacitance. The peak dynamic voltage difference between series connected devices is maintained below the value of 500 V despite the ultra-low capacitance value, but with dead-time duration having been increased to 20 µs.

The voltage waveforms displayed in Fig. 5.14(b) display the IGCT terminal voltage under there operating conditions. As can be clearly seen, there exists a discrepancy between the blocking voltage of series connected devices. This voltage difference is maximum when the device has just ended the turn-off transition (the portion of the process governed by capacitive snubbers), and reduces itself as the balancing resistors R_b gradually limit the discrepancy by exceeding the devices' leakage current during blocking.

The increased peak dynamic voltage difference between series connected devices, which has increased up to the value of almost 400 V for S_I and S_{II}, is expected with a further reduced value of snubber

capacitance. While still able to maintain the peak dynamic voltage difference below 500 V due to the reduced turn-off current, it is likely that a further decrease of snubber capacitance would not result in safely distributed blocking voltage between the series connected devices.

The waveforms presented in this section correspond to the standard devices operating in the same cooling conditions as described in Chapter 4. Therefore, once again the effect of increased junction temperature is not accounted for in this context. With this in mind, the section still demonstrates the feasibility of kHz series connected IGCT operation with purely capacitive, ultra low capacitance snubbers. In practise, this enables the extension of the power level of the envisioned DCT prototype through the increase of the dc-link voltage.

5.6 Conclusion

To provide the basis for the extension of IGCT high frequency resonant operation to increased levels of dc-link voltage, beyond what is safe for a single device, this chapter has explored series-connected low current turn-off of standard and increased electron irradiation devices. Various expected and well understood correlations are observed relating turn-off current level, snubber capacitance, and device irradiation. Considering turn-off current ranges of 50 A to 100 A, it is found that with the use of snubber capacitances as low as 40 nF, dynamic voltage sharing between series connected IGCTs at a voltage level of 5 kV is adequate, and within the snubber capacitance tolerance. This includes the case of fast-switching irradiated devices. Series-connected 5 kHz operation of the tested IGCTs is demonstrated at the previously identified optimal turn-off current level of 17 A, adjusting the dead-time to 20 µs to account for the increased capacitance due to the presence of snubbers, when compared to operation of a single device at a dc link voltage of 2.5 kV. In resonant operation, the quasi-ZVS switching conditions maintained throughout the operating range are shown to allows the use of purely capacitive snubbers, simplifying the design of such devices compared to hard-switched alternatives.

6 Summary and Future Work

This chapter concludes the thesis by summarizing its main findings in a compact manner and pointing back to the appropriate chapters where required. An outline of the remaining explorations to be performed to realise a prototype of a DCT demonstrator is provided.

6.1 Summary

The goal of this thesis was to tackle part of the challenges related to the laboratory realisation of an IGCT-based DCT prototype demonstrator. Broadly speaking, such a demonstrator is composed of three parts:

- Two IGCT-based bidirectional inverter/rectifier stages
- An MFT interface integrating the inductive resonant tank elements, and discrete resonant capacitors
- A control and protection strategy

The scope of the presented work has been only on the power semiconductor portion of the envisioned DCT, and its main contributions are summarised in the following sections.

6.1.1 1: Optimal Turn-Off Current

Chapter 3 has compared the switching losses for 68 mm, 4.5 kV RC-IGCTs under different low current turn-off conditions. The purpose of this comparison was to identify optimal switching conditions that would result in minimum switching losses. The reduction of switching loss is achieved thanks to an ultra-low turn-off current level resulting from the SRC-LLC topology's operating principle, which allows low current turn-off while still retaining significant power transfer capabilities. The purpose of the reduction of switching loss was the increase of switching frequency to the medium frequency range (more precisely 5 kHz).

In the chapter it is shown how the main factors affecting switching loss in the SRC-LLC topology operated at a constant 50 % duty cycle are:

- Selected dead-time
- Peak conducted current during the period (charge pre-flooding)
- Device electron irradiation level

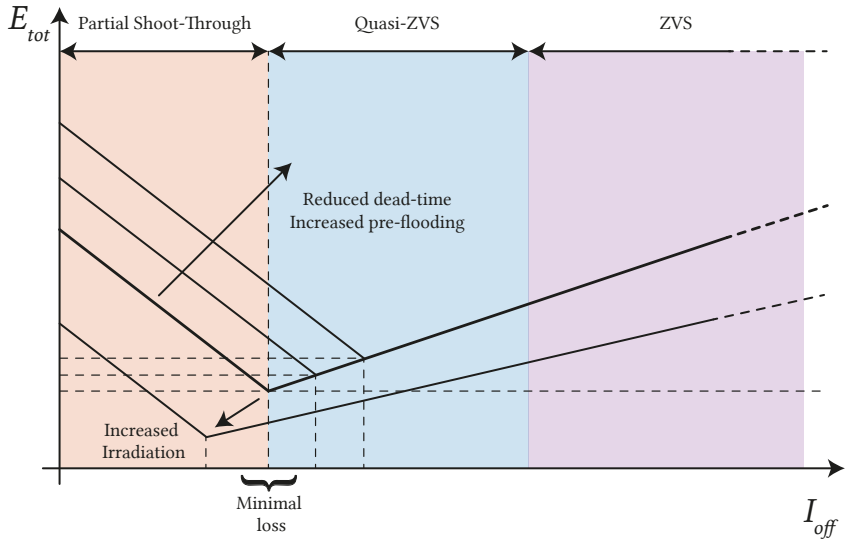


Fig. 6.1 Depending on turn-off current level, the SRC-LLC topology can operate in ZVS conditions (at high turn-off current levels), quasi-ZVS conditions, or with partial shoot-though occurring at the time of commutation. The total switching energy is affected by these operating conditions, both in terms of turn-on energy, and turn-off energy.

Fig. 6.1 provides a graphical summary of these findings. The x-axis of the figure is the IGCT's turn-off current, while the y-axis is the total switching energy of the device at that turn-off current level. The total energy is the sum of turn-on and turn-off energy. The thickest line in the figure represents the simplified characteristic of a standard GCT. At high levels of turn-off current, the device operates in ZVS conditions. This leads to turn-on loss being equal to 0 mJ, but large turn-off loss due to the high current level. As the turn-off current decreases, the device operates in quasi-ZVS conditions. These conditions are described in Chapter 3 and are characteristic of the SRC-LLC topology in low turn-off current conditions. In quasi-ZVS conditions, the turn-on loss is almost equal to 0 mJ, and the turn-off loss is reduced with respect to ZVS conditions. This yields an overall reduced level of total switching energy. Finally, as the turn-off current is further reduced, overall switching losses again increase up to a maximum level which is had at $I_{off} = 0$ A, that is to say ZCS conditions. In this portion of the figure the increase in losses is due to an increase in the device's turn-on energy. With such low levels of turn-off current, the state of the device does not transition fully to the *OFF* state during the dead-time, and part of the charge carriers are swept out of the device's junction by the turn-on of the complementary device, leading to increased switching loss. The minimum switching loss is had the the border between the quasi-ZVS region and the partial shoot-though region.

A reduced value of dead-time limits the time available for the device's state transition. This affects the turn-off current level that achieves full device turn-off during the dead-time. A shorter dead-time will require a higher turn-off current level for the device to be fully turned *OFF* before the complementary device is turned *ON*. Conversely, an increased dead-time duration will have the opposite effect. Therefore, a reduced dead-time duration results in a higher value of minimum switching loss, as the transition between quasi-ZVS and partial shoot-though will occur at a higher turn-off current level. An increase in peak conducted resonant current has a similar effect of a reduction in dead-time.

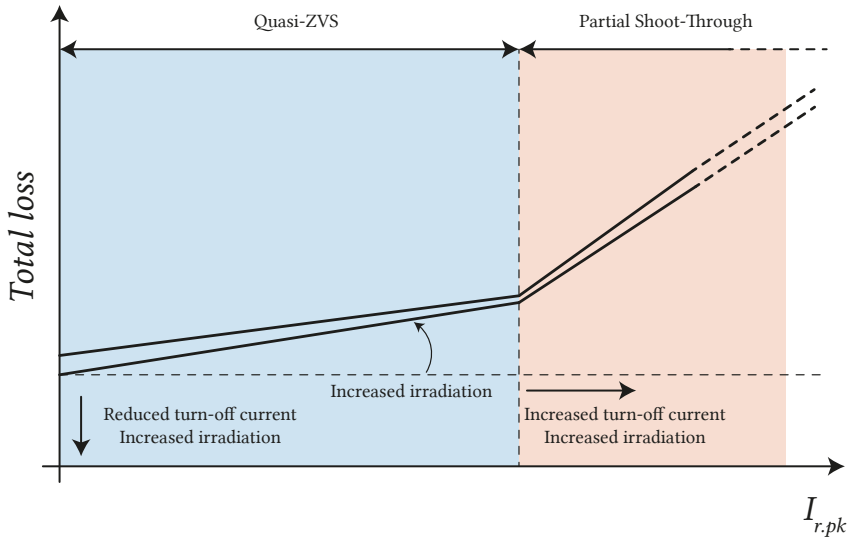


Fig. 6.2 The dependency of total loss on peak resonant current during SRC-LLC operation depends on device irradiation level and turn-off current. As long as quasi-ZVS switching conditions are maintained, switching loss is independent of load level. In the event of loss of quasi-ZVS conditions due to increased load, switching losses increase with further load increases.

The amount of charge carriers in the junction is increased causing device turn-off to have a longer duration, for the same turn-off current level. Therefore again the transition between quasi-ZVS and partial shoot-though regions occurs at higher turn-off current levels.

The level of the device's electron irradiation affects both the turn-off losses at a given turn-off current level, and the turn-off current level at which operation transitions from quasi-ZVS to partial shoot-through. When a turn-off current level is fixed, increased device irradiation will provide lower switching losses due to the faster state transition resulting from faster recombination. Simulataneously, a faster switching transition means that with the same value of dead-time, the turn-off current can be further reduced while still achieving a full state transition during t_{dt}. The combination of these two effect results in increased irradiation devices offering significant benefits in terms of switching losses compared to devices with lower irradiation levels.

Finally, it is noted that the ideal turn-off current level depends on load condition and therefore it is in practise impossible to achieve it. Nevertheless, operation with turn-off current values which are close to the minimal loss value still result in very small losses.

6.1.2 2: Demonstration of 5 kHz Operation

Chapter 4 has demonstrated for the first time steady state operation of RC-IGCTs at a frequency of 5 kHz. This was possible thanks to the identification and use of the optimal turn-off current level from the previous chapter.

As expected, the use of devices differing by their electron irradiation level results in different loss distribution between switching and conduction loss, with higher irradiation level leaning more

towards high conduction loss, and lower levels resulting in higher switching loss. Fig. 6.2 summarises this.

With increased electron irradiation levels, losses in load conditions are lower. As the load level increases, the increased forward voltage drop of these devices causes the total loss to increase faster compared to devices exposed to lower levels of irradiation (slope of the loss characteristic in quasi-ZVS conditions). Increased irradiation devices also maintain quasi-ZVS operation at higher levels of $I_{r,pk}$ compared to standard devices, due to their faster switching transitions.

A simple thermal model of the employed test setup allows the calculation of the IGCT junction temperatures, which are found to be well below their maximum 115 °C limit. This means that the same operation is likely possible with reduced cooling effort (deionised cooling water is kept at maximum 35 °C during testing), or with increased load. Due to test setup limitations, the peak conducted resonant current in testing was only of 500 A.

Because of the relatively low values of load current achievable in the test setup, loss-of quasi-ZVS conditions never occurred during testing, but with a sufficient increase in load current this will eventually occur. With loss of quasi-ZVS conditions, turn-off losses are no longer constant, but dependant on the peak resonant current level, which is expected to accentuate the rate of increase of total losses with the peak resonant current level (as both switching and conduction loss will depend on $I_{r,pk}$, and not only conduction loss).

6.1.3 3: Ultra-Low Snubber Capacitance

Chapter 5 has selected ultra-low snubber capacitance values for IGCT series connection in SRC-LLC operation. The snubbers were then used to achieve 5 kHz series connected operation of the IGCT in resonant conditions and under load, demonstrating the feasibility of an increase in power and voltage level in the envisioned DCT demonstrator through the use of series connected IGCTs. The operating principle of the SRC-LLC ensure that ZVS or quasi-ZVS conditions are present in the majority of the operating range. In ZVS or quasi-ZVS turn-on, there is no (or very low) voltage present at the terminals of the device when it is switched *ON*. For this reason, if a snubber capacitance is present in parallel with the device, there is no risk of such a capacitance discharging into the IGCT, causing turn-on losses. This renders the presence of a snubber resistor in series with the snubber capacitance unnecessary, and allows for a simplification of the snubber circuit.

In addition to its ZVS conditions, resonant LLC operation is also characterised by low levels of turn-off current. This is exacerbated in the context of this thesis, where the turn-off current is reduced to very low levels to reduce switching loss. With such low levels of turn-off current, snubber capacitance has to be significantly reduced compared to the 200 nF-1 µF values which are employed in traditional hard-switched applications.

For snubber capacitance to provide effective dynamic voltage balancing between series connected devices, its value must be significantly larger than that of the output capacitance of the devices. In Chapter 5 it is found that snubber capacitances of 40 nF, 70 nF, and 100 nF are sufficient to provide adequate voltage sharing between series connected IGCTs, with turn-off currents in the range of 50 A to 100 A. The sizing of static voltage balancing resistors can be performed in the same way as with traditional hard-switched applications.

The addition of snubber capacitances in parallel with the devices have in practise the same effect on

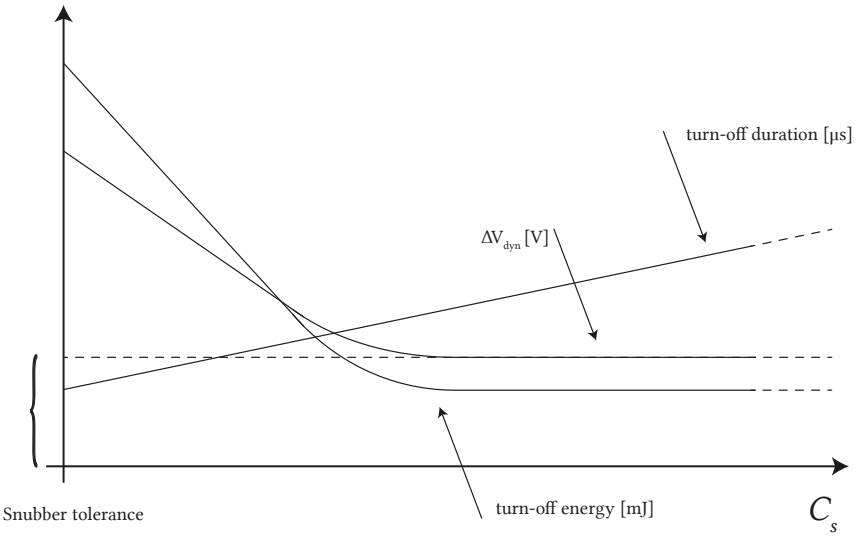


Fig. 6.3 The increase of snubber capacitance improves dynamic voltage sharing up to a limit determined by the tolerance of the employed snubber capacitors. Larger values of snubber capacitance are also beneficial in terms of energy dissipated in the GCT itself, but increase the overall state transition time, potentially leading to partial shoot-though.

switching transitions as a lower irradiation level, as seen in Fig. 6.3. State transitions are slower for the same level of turn-off current, and therefore loss of quasi-ZVS conditions occurs at lower load, for the same devices. To obviate for this, 5 kHz operation with series connected devices is achieved with an extended dead-time of 20 µs, increased from the 15 µs for individual devices. Additionally, the snubber capacitance is reduced further to 20 nF in parallel with each device. The voltage sharing under these conditions is still satisfactory and the peak voltage difference between devices is maintained below 10 % of the dc link voltage.

6.2 Conclusion

This thesis has demonstrated that operation at medium frequency of series connected RC-IGCTs with purely capacitive snubbers is possible in an SRC-LLC topology with low turn-off current level. With this operating mode having been proven, the IGCT has been shown to be a device suitable for DCT applications, together with the more common IGBTs and emerging HV SiC MOSFETs. The thesis has discussed the main parameters affecting conduction and switching losses in this operating mode. Among these are:

- Turn-off current
- Peak resonant current
- Dead-time duration
- Snubber capacitance
- Device irradiation level

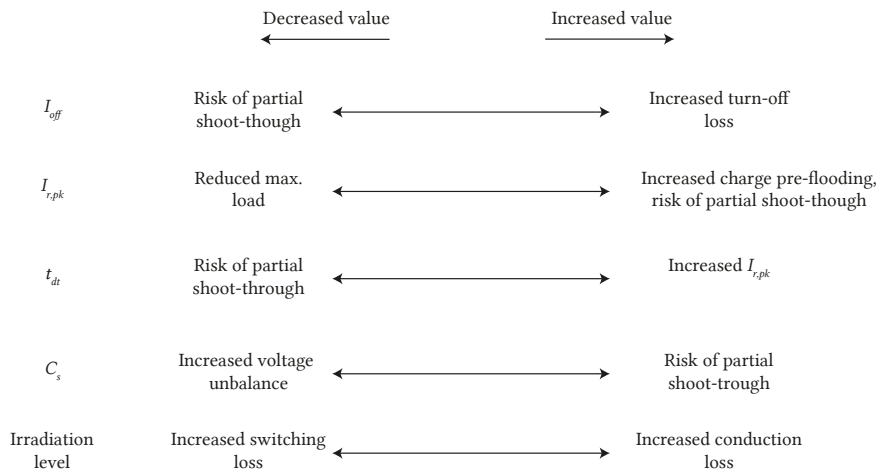


Fig. 6.4 Trends in IGCT series connected resonant operation depending on the variation of the main parameters.

The trends and effects which result as a consequence of the variation of these parameters have been described and are summarised in Fig. 6.4. No effort was made to find a combination of the parameters which is optimal for the DCT application. While low operating losses are of great important to ensure safe operation of the semiconductor devices, an optimal set of parameters of DCT embodiment for a specific use will depend on considerations going well beyond this.

6.3 Future Work

Concerning only the semiconductor stage of the envisioned DCT prototype demonstrator, the main challenges still to be addressed reside mainly in the operation of the 10 kV side of the converter, and in the protection of the topology.

6.3.1 10 kV Side

The work presented in this thesis has focused on the primary side of the SRC-LLC based DCT, operating at a voltage of 5 kV. At this voltage, the operation of a half-bridge leg employing two series connected RC-IGCTs per position has been demonstrated. The operation of the DCT secondary at the voltage of 10 kV required a higher blocking voltage on the part of the employed semiconductors, which cab be achieved by:

- Increased number of series connected devices
- Increased rated voltage of the device (10 kV RC-IGCTs provided by Hitachi Energy - former ABB Semiconductors)

with both options being characterised by their own set of challenges. Nevertheless, regardless of the elected solution, the 2:1 winding ratio of the MFT will in any case result in a decreased level of

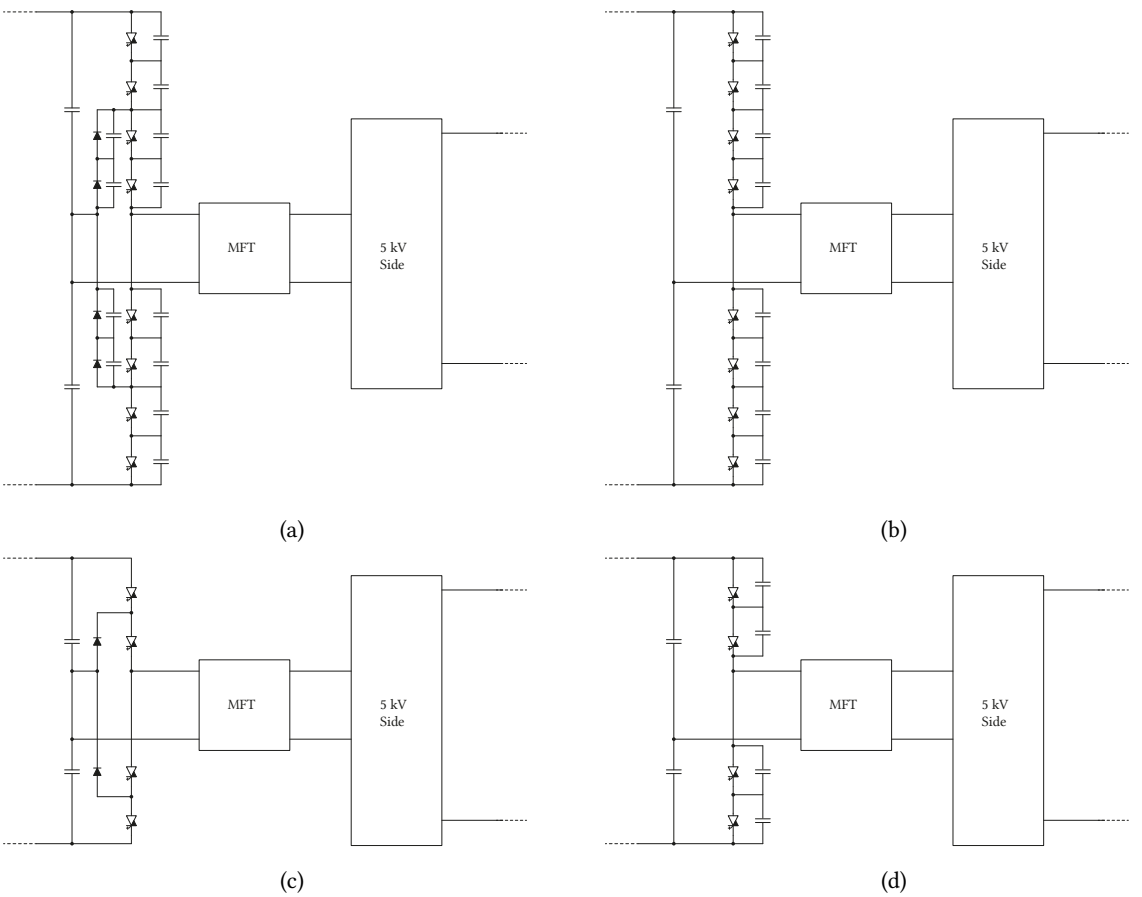


Fig. 6.5 The considered topologies for the 10 kV side are the a) NPC and b) half-bridge, employing series connected 4.5 kV devices, and c) NPC and half-bridge employing 10 kV RC-IGCTs.

turn-off current (half) on the secondary side compared to the primary side. The demonstrated series connected operation of the 5 kV side at a frequency of 5 kHz with a turn-off current of 17 A would result in a turn-off current of only approximately 8.5 A on the 10 kV side. This is expected to result in increased turn-off duration, which is undesirable in 5 kHz operation.

The considered topologies for the 10 kV side are displayed in Fig. 6.5. Both NPC and half-bridge topologies are considered, employing 4.5 kV and 10 kV devices. The topology presented in Fig. 6.5(a) is excluded as in practise the device count exceeds what can be contained in a single ACS 1000 stack, increasing the complication of mechanical integration.

While the half-bridge topologies in Figs. 6.5(b) and 6.5(d) would operate similarly to the 5 kV primary, the NPC solution of Fig. 6.5(c) eliminates the need of dynamic voltage balancing snubbers by transitioning through the capacitor midpoint. The selection of the most desirable solution is expected to be based on which of the considered option ensures the fastest transition between the $+V_{dc}/2$ state, and $-V_{dc}/2$. Ideally, this would be achieved in during the same 20 µs dead-time that was employed during the series connected 5 kHz operation of the low side. Nevertheless, this is expected to be unlikely. The solution in Fig. 6.5(b) employs the same devices used on the low side, but with 4 devices in series connection per position (instead of 2), and with half the turn-off current. As capacitive

snubbers need to be employed to ensure satisfactory dynamic voltage sharing, it is expected that state transitions will be slow.

Similarly, the solution in Fig. 6.5(b) employs 10 kV devices (which are associated with slower switching transitions), together with parallel capacitive snubbers for dynamic voltage sharing. Again, due to both the increased voltage ratings of the devices and the reduced turn-off current, state transitions are expected to be significantly slower compared to the 5 kV side.

Finally, Fig. 6.5(c) displays 10 kV devices in an NPC configuration. In this case, two state transitions are required to move from the $+V_{dc}/2$ state to the $-V_{dc}/2$ state. While each individual transition will likely be faster thanks to the absence of capacitive snubbers, their increased number together with the high voltage rating of the devices and low turn-off current levels is still expected to result in a relatively slow process.

The selection of the solution therefore requires characterisation of the performance of 10 kV devices, and the comparison of their performance in the half-bridge and NPC configurations with their 4.5 kV counterparts in the half-bridge configuration, with 4 series connected devices per position.

6.3.2 Protection

As discussed in this thesis, one of the advantages of the use of the SRC-LLC topology is the combination of soft-switching conditions and limitation on load current di/dt, which is provided by the inductive elements of the resonant tank. Thanks to these conditions, operation of the IGCTs in this topology does not require the use of clamp circuitry, reducing the overall volume, complexity, and component count.

On the other hand the absence of clamp circuitry can be challenging from the perspective of protection. As IGCTs are designed to fail in short circuit, in the event of such a failure there is no device providing limitation of the rate of current increase once the complementary device had been turned *ON*. The very small stray inductance of the current path, which is in the order of few hundreds of nH, is very likely insufficient for control action to take place in time to protect the affected devices.

The use of gate driver units including anode to cathode voltage measurement has been proposed in [115] for use in IGCT resonant operation to prevent turn-on of the IGCTs in the event of a short circuit fault of the complementary device, which can prevent the issue of extremely rapid rate of fault current increase. Nevertheless, the use of such purpose-designed gate driver units remains to be tested in fault conditions.

6.3.3 Thermal Effects

The work presented in this thesis has demonstrated operation at 5 kHz of standard commercial IGCTs and estimation of the junction temperatures of the devices in various operating conditions have been provided. The test setup employed to gather these results can take advantage of very effective cooling thanks to the employed WCU having access to cold lake water (around 10 °C) which is used to extract heat out of the deionised cooling water in contact with the stack heatsinks.

By controlling the water flow in the WCU heat exchanger, it was possible to vary the cooling water temperature from a very low 10 °C to a more realistic 35 °C. Nevertheless, the setup does not allow accurate closed-loop regulation of the temperature of the heatsinks. For this reason, while trends in

switching waveforms associated with changing cooling water temperatures were identified, it was not possible to characterise them in detail.

The precise quantification of thermal effect on the switching and conduction characteristics of the tested devices is not of utmost importance for the limited range of operating conditions in which the envisioned laboratory DCT prototype demonstrator will operate. Nevertheless, any real-world uses of such a solution would have to carefully investigate these effects, as the limited results seen so far display non-negligible degradation of semiconductor performance as it's junction temperature increase, rendering switching transitions slower and moving the operating point of the topology close to the loss of quasi-ZVS switching conditions.

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