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Condition Health Monitoring for Medium-Voltage High-Power Modular Multilevel Converter

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Abstract

Among the policies to reduce the consequences of greenhohuse gas missions, the decarbonization of the electrical, transport, and manufacturing sectors has profoundly changed how the electricity is produced, transmitted, distributed, and consumed, particularly imposing several complex technical challenges to power electronics-based technologies. Future power converter solutions are called to fulfill increasingly demanding requirements of efficiency, power quality, cost, volume, and reliability, foreseeing that next generation of high-power converters might be based on modern concepts such as the modular multilevel converter (MMC).

Although the MMC exhibits extraordinary characteristics, namely, full modularity, voltage-current scalability, and high efficiency, its development is still in an early stage of maturity, and different topics such as reliability improvement are still research subjects. Around 40000 parts composing the 96 submodules (SMs) used in the two medium voltage (MV) 250 kVA MMCs to form the power electronics laboratory (PEL) MMC research platform illustrates the reasonable concern about technology reliability. Condition health monitoring (CHM) arises as an attractive concept to prevent failure events improving reliability and availability of power electronics-based converters. When intended for MMC, CHM development and deployment face several challenges, mainly due to the existing technique's demand for additional hardware, modification of control schemes, particular operating conditions, and complex algorithms. Consequently, MMC CHM state-of-the-art is narrowed to SM power capacitors and power semiconductors.

This thesis aims to provoke and contribute to the CHM body of knowledge by investigating three alternatives applied to the PEL medium-voltage MMC. The first is a simple, accurate, and costless online strategy to monitor the SM electrolytic capacitor's condition. The method is based on the relationship between the capacitor's degradation and capacitance level. Thus, the SM capacitance is estimated by employing measurements commonly used for necessary control and protection algorithms and the recursive weight least squares (RWLS) technique. Real-time hardware-in-the-loop (RT-HIL) simulations and experimental results show the method's performance under different capacitor aging levels and converter operating conditions.

A second alternative responds to the difficulties in gathering information about components other than power capacitors and power semiconductors, as cost, space, and data processing restrictions are common barriers. The strategy uses the single switch flyback-based auxiliary submodule power supply (ASPS) consumption monitoring to observe simultaneously different SM sub-circuits instead of a particular component and the fault dictionary concept to detect the SMs drifting from expected healthy conditions. The scheme settles on the idea that small changes in the circuits loading the ASPS secondaries can be seen and used to evaluate their deterioration level. A practical example is provided based on the developed SM and experimental data. It is demonstrated that minor and significant power consumption variations can be noticed and used for health monitoring.

Envisioned in future MMCs, the handling, processing and extraction of valuable information from massive amounts of data coming from different CHM techniques is an open issue and certainly a challenge for the health assessment. Inspired by the data fusion framework and multi-criteria decision-making (MCDM) problems, a scheme to integrate various SM health indicators is proposed to compose a comprehensive health index. Systematic approaches considering objective data from the SM and subjective information from expert knowledge are presented and verified through numerical examples based on experimental data. It is demonstrated that entropy, fuzzy-TOPSIS, and game theory-based methods are superior solutions for the SM and converter-level health assessment in the context of multiple information sources.

Keywords reliability, condition health monitoring, medium-voltage, high-power, modular multilevel converter.

Résumé

Parmi les politiques visant à réduire les conséquences des émissions de GES, la décarbonation des secteurs de l'électricité, des transports et de la fabrication a profondément modifié la façon dont l'électricité est produite, transportée, distribuée et consommée, imposant notamment plusieurs défis techniques complexes aux technologies basées sur l'électronique de puissance. . Les futures solutions de convertisseurs de puissance sont appelées à répondre à des exigences de plus en plus exigeantes en matière d'efficacité, de qualité de l'énergie, de coût, de volume et de fiabilité, prévoyant que la prochaine génération de convertisseurs haute puissance pourrait être basée sur des concepts modernes tels que le convertisseur modulaire multi-niveaux (MMC).

Bien que le MMC présente des caractéristiques extraordinaires, à savoir une modularité complète, une évolutivité tension-courant et un rendement élevé, son développement est encore à un stade précoce et différents aspects tels que l'amélioration de la fiabilité sont encore des sujets de recherche. Environ 40000 pièces composant les 96 cellules (SMs) utilisé dans les deux MMC MV 250 kVA pour former la plate-forme de recherche laboratoire d'électronique de puissance (PEL) MMC illustrent le souci raisonnable de la fiabilité de la technologie. Le surveillance de l'état de santé (CHM) apparaît comme un concept attrayant pour prévenir les événements de défaillance, améliorant la fiabilité et la disponibilité des convertisseurs basés sur l'électronique de puissance. Lorsqu'ils sont destinés à MMC, le développement et le déploiement de CHM sont confrontés à plusieurs défis, principalement la nécessité de matériel supplémentaire pour la technique existante, la modification des schémas de contrôle, des conditions de fonctionnement particulières ainsi que des algorithmes complexes. Par conséquent, la technologie de pointe du CHM de MMC se limite aux condensateurs de puissance SM et aux semi-conducteurs de puissance.

Cette thèse vise à provoquer et à contribuer au corpus de connaissances du CHM en étudiant trois alternatives appliquées au PEL MV MMC. La première est une stratégie en ligne simple, précise et gratuite pour surveiller l'état du condensateur électrolytique SM. Cette méthode repose sur la relation entre la dégradation du condensateur et le niveau de capacité. Ainsi, la capacité SM est estimée en utilisant des mesures couramment utilisées pour les algorithmes de contrôle et de protection nécessaires et la technique moindres carrés pondérés récursifs (RWLS). Les simulations matériel dans la boucle en temps réel (RT-HIL) et les résultats expérimentaux montrent les performances de la méthode sous différents niveaux de vieillissement des condensateurs et conditions de fonctionnement du convertisseur.

Une deuxième alternative répond aux difficultés de collecte d'informations sur les composants autres que les condensateurs de puissance et les semi-conducteurs de puissance, car les restrictions de coût, d'espace et de traitement des données sont des obstacles courants. La stratégie utilise la surveillance de la consommation alimentation du cellules auxiliaire (ASPS) basée sur le flyback à commutateur unique pour observer simultanément différents sous-circuits du SM au lieu d'un composant particulier et le concept de dictionnaire de défauts pour détecter un changement du SM par rapport aux conditions saines attendues. Le schéma repose sur l'idée que de petits changements dans les circuits chargeant les secondaires ASPS peuvent être vus et utilisés pour évaluer leur niveau de détérioration. Un exemple pratique est fourni sur la base du SM développé et des données expérimentales. Il est démontré que des variations de consommation d'énergie mineures et significatives peuvent être remarquées et utilisées pour la surveillance de la santé.

Envisagé dans le futur MMC, la manipulation, le traitement et l'extraction d'informations précieuses à partir de quantités massives de données provenant de différentes techniques CHM est un problème ouvert et certainement un défi pour l'évaluation de la santé. Inspiré du cadre de fusion de données et

des problèmes prise de décision multicritères (MCDM), un schéma d'intégration de divers indicateurs de santé SM est proposé pour composer un indice de santé complet. Des approches systématiques prenant en compte des données objectives du SM et des informations subjectives issues de connaissances d'experts sont présentées et vérifiées à l'aide d'exemples numériques basés sur des données expérimentales. Il est démontré que l'entropie, le TOPSIS flou et les méthodes basées sur la théorie des jeux sont des solutions supérieures pour l'évaluation de la santé au niveau du SM et du convertisseur dans le contexte de multiples sources d'information.

Mots clés fiabilité, surveillance de l'état de santé, moyenne tension, haute puissance, convertisseur modulaire multi-niveaux.

Resumen

Entre las medidas para reducir las consecuencias de las emisiones de gases de efecto invernadero a nivel mundial, las políticas de descarbonización del sector eléctrico, transporte y manufactura han cambiado profundamente la manera en que la electricidad es generada, transmitida, distribuida y utilizada, imponiendo una variedad de desafíos técnicos a los sistemas eléctricos, particularmente, a aquellos que utilizan intensivamente dispositivos de electrónica de potencia. Las actuales y futuras soluciones basadas en electrónica de potencia están cada vez más presionadas a cumplir exigentes estándares y requerimientos de eficiencia, calidad de la potencia y confiabilidad, mientras aspectos como costos, volumen y peso se intentan mantener al mínimo. En consecuencia, se espera que el mercado de convertidores de media tensión y alta potencia evolucione de la mano de conceptos modernos como los convertidores modulares multi-nivel (MMCs).

Aun cuando los MMCs presentan extraordinarias características técnicas, como por ejemplo, alta modularidad, fácil escalabilidad en tensión y corriente, y alta eficiencia, el desarrollo de esta tecnología aún está en una etapa temprana de madurez. Por lo tanto, aspectos como la reducción de costos y volumen, su utilización en nuevas aplicaciones o, de particular interés para este trabajo, el incremento de su confiabilidad, despiertan una alta atención por parte de la comunidad científica y la industria especializada. Una de las razones principales para investigar la confiabilidad de de este tipo de equipos radica en el alto número componentes necesarios para su construcción. Por ejemplo, y a modo de ilustración, la plataforma de investigación desarrollada en el *Power Electronics Laboratory* (PEL) requiere de 40000 partes para formar sus 96 submódulos (SMs) y así componer dos unidades MMC de 250 kVA cada una. En virtud de lo expuesto anteriormente, se ha vuelto especialmente atractivo utilizar conceptos como monitoreo del estado de salud (CHM) para alertar tempranamente la degradación de componentes específicos y, así, prevenir fallos catastróficos, permitiendo mejorar considerablemente los indicadores de confiabilidad y disponibilidad de las unidades de potencia. Ahora bien, cuando el concepto CHM es aplicado a MMC, su desarrollo e implementación enfrentan diversos desafíos técnicos, principalmente, debido a que los métodos desarrollados hasta la fecha usualmente requieren la adición de hardware (sensores y circuitos), modificaciones en los esquemas de control, condiciones particulares de operación del conversor y algoritmos con un alto número de instrucciones. En consecuencia, las técnicas más comunes de CHM aplicado a MMC están fuertemente enfocadas en los condensadores y semiconductores de potencia de los SMs, cuya tasa de fallas es relativamente alta comparada con otros componentes utilizados en este tipo de aplicaciones.

El objetivo de esta tesis, por lo tanto, es estimular y contribuir en el desarrollo de la tecnología MMC mediante la investigación y desarrollo de tres estrategias de CHM aplicadas al MMC desarrollado en PEL. La primera estrategia se enfoca en los condensadores de potencia y busca proponer una mejora respecto a otros métodos existentes. La idea se basa en la estrecha relación que existe entre el nivel de degradación de un condensador y su cambio en la capacitancia, por lo que se propone un método en línea, de relativo bajo costo computacional, con buenas características de precisión, y sin la necesidad de componentes adicionales para estimar la capacitancia del banco de condensadores de potencia del SM. El método se lleva a cabo utilizando las mediciones comúnmente encontradas en el SM para las acciones de control y protección, en conjunto con la técnica *recursive weight least squares* para mejorar la precisión de la estimación. A través de simulaciones en tiempo real y resultados de laboratorio se demuestra el desempeño de esta idea bajo diferentes condiciones de degradación de los condensadores y operación del conversor.

La segunda estrategia responde a las restricciones existentes de costo, espacio y capacidad de procesamiento para obtener información útil sobre la degradación de componentes diferentes a los condensadores y semiconductores de potencia. El esquema se basa en la idea de que cambios en los circuitos

conectados en los secundarios de la fuente de poder auxiliar del SM (ASPS), producto de una falla o la degradación de uno o varios componentes, pueden ser detectados y monitoreados en el lado primario, permitiendo, finalmente, evaluar su nivel de deterioro. De esta manera, el método planteado consiste en la estimacón del consumo de potencia de la ASPS y la utilización del concepto de diccionario de fallas para detectar los SMs cuyas ASPS muestran un consumo de potencia diferente a lo esperado para un SM no deteriorado. Un ejemplo práctico aplicado al SM desarrollado en este trabajo y en conjunto con datos obtenidos experimentalmente es presentado y analizado detalladamente, concluyendo que esta idea es viable para desarrollar nuevas e interesantes estrategias de CHM aplicados a MMC.

A través de la experiencia obtenida de este trabajo y bajo el supuesto de que los futuros MMCs presenten diversas técnicas de CHM, es de esperar que el manejo, procesamiento y extración de información relevante sea un problema abierto y desafiante para la evaluación del estado de salud de este tipo de conversores. Inspirado en el concepto de fusión de datos y en los problemas de toma de decisión con múltiples criterios (MCDM), se propone un esquema para integrar diferentes indicadores de salud con el objetivo de componer un único y representativo indicador a nivel de SM y/o conversor. Diferentes técnicas que consideran información cuantitativa, desde los sensores del SM, e información cualitativa, proveniente de una evaluación experta, son presentados y verificados a través de ejemplos numéricos alimentados con datos obtenidos experimentalmente. Se concluye que los metodos basados en entropía, *fuzzy-TOPSIS* y teoría de juegos son soluciones suficientes para unificar múltiples indicadores de salud y evaluar el estado de salud del conversor.

Palabras clave confiabilidad, monitoreo del estado de salud, media tensión, alta potencia, conversor modular multi-nivel.

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List of Abbreviations

ADC	analog-to-digital converter
Al-cap	aluminum electrolytic capacitor
ANN	artificial neural network
ASPS	auxiliary submodule power supply
CHM	condition health monitoring
COMBI-IO	combined input-output
CRITIC	criteria importance through inter-criteria correlation
CW	combined weight
DSP	digital signal processor
EMF	electromotive force
ESL	equivalent series inductance
ESR	equivalent series resistance
FACTS	flexible ac transmission systems
FB	full-bridge
FOL	fibre optic link
FPGA	field-programmable gate array
GCC	grid current control
GHG	greenhouse gas
HB	half-bridge
HV	high voltage
HVdc	high voltage dc
IC	integrated circuit
IGBT	insulated gate bipolar transistor
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law

LED	light emitting diode
MCDM	multi-criteria decision-making
MLC-cap	multilayer ceramic capacitor
MMC	modular multilevel converter
MPPF-cap	metallized polypropylene film capacitor
MV	medium voltage
MVdc	medium voltage dc
OVDC	overvoltage detection circuit
OW	objective weight
PCB	printed circuit board
PEC-MI	power electronics controller measurement interface
PEL	power electronics laboratory
PHM	prognosis and health management
PI	proportional integral
PoF	physics-of-failure
PR	proportional resonant
PS-PWM	phase-shifted carrier PWM
PV	photovoltaics
PWM	pulse-width modulation
REL	electromechanical relay
RES	renewable energy sources
RLS	recursive least squares
RT-HIL	real-time hardware-in-the-loop
RUL	remaining useful life
RWLS	recursive weight least squares
SM	submodule
SRF	synchronous reference frame
STATCOM	static synchronous compensator
SW	subjective weight
THY	thyristors in antiparallel connection

TOPSIS	the-order-preference-by-similarity-to-an-ideal-solution
TSEP	temperature sensitive electrical parameter
UART	universal asynchronous receiver-transmitter
VSC	voltage-source converter

Contents

1 Introduction

1.1 Renewable energy transition

The adverse effects of climate change on a global scale have led to unprecedented transversal agreements among country leaders, the scientific community, the private sector, and society, in general, to tackle greenhouse gas (GHG) emissions and mitigate the effects of climate change over the population. The Paris Agreement in 2015, the most recent and important country-level agreement, congregated 195 nations to accord reducing global GHG emissions to limit the global temperature increase during this century to 2 °C above pre-industrial levels [1]. Since then, different country policies towards accomplishing the Paris Agreement have been implemented, mostly related to the energy sector as it is responsible for around three-quarters of global CO_2 emissions (transport, heat and electricity sectors) [2]. Example of actions have been decarbonization of energy systems through economic incentives for the incorporation of renewable energy sources (RES) [3]; the introduction of energy storage systems to manage volatility in the electrical systems [4]; and the electrification of the energy used by transport [5] and industrial sectors [6].

The transition from oil & gas-based system to a RES-based as a primary energy source, together with the electrification of different carbon-based applications is already happening, it is widely recognized that to move forward into a completely sustainable system is not a simple task and it comes with complex emerging economic and technical challenges. The current and expected increment of RES and the connection of complex loads such as prosumers and electric vehicles in the electrical system brings with it one of the most challenging issues during frequency regulation as generation and consumption present an inherent stochastic intermittent nature. Other aspects of concern are: low short-circuit levels, which increases voltage instability and complicates fault detection/protection systems; power quality at the point of connection, as RES generators are feed-in via power electronics-based converters; and low-inertia as RES generators provide significantly less inertia compared with synchronous solutions [7], [8]. When electricity is understood as a commodity produced in multiple points spread on a vast geographical surface with different sources and technologies, transmitted through long power lines interconnected between them and served into various applications, the power system has to be as reliable as possible. The reliability concept applied to power networks might be understood as the ability to deliver electricity to all consumption points and receive electricity from all supply points within accepted technical standards and in the desired amount. For a power system to be reliable, it must comply with adequacy requirements, i.e., the ability to meet the electric power and energy requirements within acceptable technical limits, and security, i.e., the ability to withstand disturbances [9].

It is becoming clear that the transition to a sustainable energy system is not an easy task, involving different actors from power system regulators, planners and operators to power plants owners and

operators. During the past two decades, many of these challenges have been faced employing the power electronics-based converters operating as an interface between a power source or load and the grid and operating as grid support for stability improvement and power quality. However, present and future challenges in large-scale RES integration require that current power converter technology evolve to address system reliability adequately, transforming it into a key technology.

1.2 Modular multilevel converter reliability

The next generation of high-power converters for large-scale RES, massive transportation, and storage systems integration is expected to employ an increasing number of modular multilevel converters (MMCs) [10]. A MMC is a modern concept in which several modular (small power) units are interconnected to form a whole converter, exhibiting several advantages such as full modularity, voltage scalability, current scalability, high efficiency, low harmonic voltage distortion, redundancy, control flexibility, and transformer-less operation [11]. The modular units, namely submodules (SMs), can be connected in series with an inductor forming a branch [11]–[13]. Depending on how the branches are connected, different topologies for various applications are devised. For instance, a three-phase dc-ac MMC is formed with a set of three legs in parallel, being a leg the series connection of two branches as it is depicted in **Fig. 1.1** [14]. On the other hand, an ac-ac MMC (also known as direct MMC, matrix MMC or triple-star bridge cells) can be formed with nine branches interfacing two three-phase ac systems (cf. **Fig. 1.1**) [15].

Since the introduction of the MMC concept [10], different studies have presented new configurations and control schemes, being some of them suitable and promising solutions not only for high-power wind [16] and photovoltaics (PV) energy conversion [17] but also for other relevant applications needed for further advances in the sustainable energy transition such as solid-state transformers [18], flexible distribution networks [19], railway interties [20], medium voltage (MV) motor drives [21], flexible ac transmission systems (FACTS) [22], and hydropower applications [23].

Even more, some of these ideas have made their way to the industry, finding practical applications.

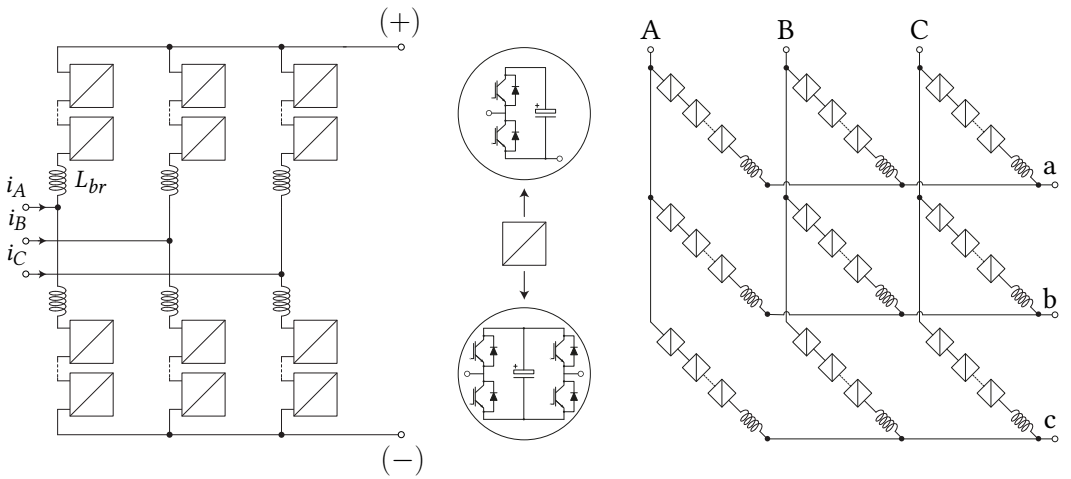


Fig. 1.1 Generic MMC structure. Left side: rectifier/inverter ac-dc configuration. Right side: ac-ac direct MMC configuration. Building block might be full-bridge (FB), half-bridge (HB) or a combination of them.

(a) (b) (c)

Fig. 1.2 Commercial MMC HVdc solutions. a) Siemens HVDC PLUS [27], b) ABB HVDC LIGHT [28], c) GE HVDC VSC [29].

For instance, in 2021, Hitachi ABB commissioned the first two MV direct-MMC units, each rated for 80 MW, intended for converter-fed synchronous machine pumped-hydro power plant in Austria [24]. In 2020, Siemens commissioned a ±300 MVA MMC-based static synchronous compensator (STATCOM) in Haltern am See, Germany [25]. In 2017 Hitachi Energy commissioned a 916 MW MMC-based high voltage dc (HVdc) offshore wind connection in Germany [26].

Despite the extraordinary characteristics of the MMCs, the amount of research done around them and the industry transformation willing to invest in this solution, the MMC technology is still in an early stage of maturity, and different topics such as control schemes [30], power scalability [31], and more importantly reliability [32]–[34] are still under investigation.

In general, a power electronics converter is an electronic device that uses power semiconductors operating in switching mode to convert and control the electrical power to meet a specific needs efficiently [35]. The latest advancements in power semiconductor devices, digital control systems, and communication have accelerated the evolution of this technology, becoming highly attractive not only for RES power conversion but also for other broad range of applications.

In the power electronics field, reliability might be understood as the ability of an item to perform a required function under stated conditions for a stated period [36]. Historically, reliability has been assessed using statistical curve fitting of field failure rate; however, this approach has proven to be not very effective [37]. The drawback of this method is that those past failure events might not be repeated in the future as stress environments, material properties, product quality, and product use and misuse vary widely between applications. Instead, the new understandings of components and materials root-cause of failure mechanisms, failure sites, failure modes, and failure-causing stresses have allowed developing more accurate degradation models to prevent, detect effectively, and correct failures associated with the design, manufacturing, and operation of a device [38]. Despite such improvements in the field and its application to the reliability prediction and assessment in power electronics, latest reliability studies have suggested that more research effort has to be done in order to improve power converters reliability [39]. Different unexpected situations related to the operating or environmental conditions, not necessarily considered during the design phase, might increase the accumulated damage of some components, decreasing their expected lifetime; or lead converter failure, increasing converter failure rate. For example, different experimental data sets, surveys, and studies have concluded that the most critical components with the highest failure rates in a power converter are the controllable power semiconductors (switches) and capacitors, contributing to more than 50% of the faults [39], [40]. These components' leading causes of failure are their exposition

to thermal, electrical, and mechanical stress, e.g., due to long-term or frequent transient overload conditions or heavy environmental conditions, such as extreme temperatures, moisture, mechanical vibration, and chemical erosion radiation, and lightning [41].

As the majority of the power electronics-based converters, several power capacitors and switches are used; however, in the MMC, due to a large number of SMs the number of these components and many other electronic devices are dramatically higher compare with traditional converters. The EPFL power electronics laboratory (PEL) MMC research platform made of several SMs is not the exception. The **Fig. 1.3** shows the EPFL PEL SM, which comprises a full-bridge 1.2 kV 70 A insulated gate bipolar transistor (IGBT) module, six 1.5 mF electrolytic capacitors, a 20 W (peak power) auxiliary submodule power supply (ASPS) with multiple isolated outputs, a digital signal processor (DSP)-based local controller and a variety of low power integrated circuits, resistors, capacitors, semiconductors and connectors for measurement, protection, communication and control, which will be described in detail on **Chap. 3**. Consequently, it is a complex power electronics circuit with many elements that require comprehensive studies, holistic design considerations, and proper operation under various operating conditions to achieve a more reliable MMC functioning while working in the field.

The probability of failure in an MMC depends on the reliability of its subsystems (e.g., branches) and SMs [42], which depends on converter topology, operation mode, maintenance, SM structure and number, components quality, among other factors. Commonly, MMC reliability is addressed at the production level by considering proper electric circuit design and strict quality control procedures performed before and after the converter is installed [37]. At the operational level, reliability is faced through active fault-tolerant control systems, in which a fault is detected and localized using fault-detection methods [43], [44]. Once a fault is detected, the damaged SM is isolated to reduce consecutive failure and extra damage to the converter. Depending on the fault-tolerant method, the converter may operate with reduced voltage and power quality [45] or at full capacity if redundant SMs are available [46]. From the reliability and availability point of view, SM redundancy is visibly more favorable; nevertheless, it represents a higher investment cost and increases converter volume [33].

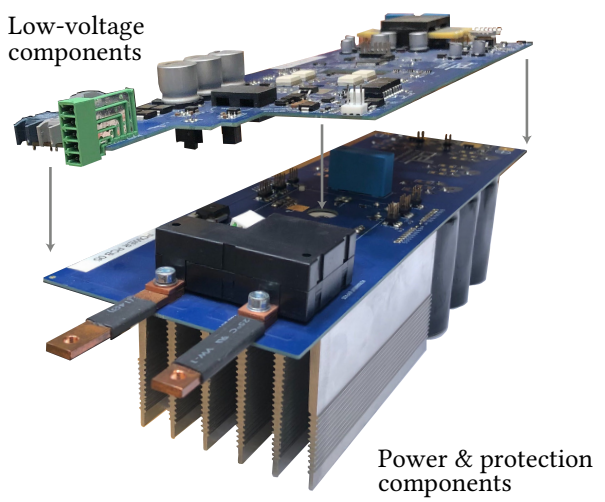


Fig. 1.3 EPFL PEL MMC SM. Upper board contains all the low-voltage components while the lower part contains power and protection components.

Up to this point, it is important to stress that the ideas behind fault-tolerant methods propose a post-fault reaction, allowing to manage the fault situations up to some extent to keep the converter operating. However, reliability might be improved further if, in addition, other preventive techniques of some sort could indicate the deterioration at the components or SMs or converter-level in order to decide a course of actions such that a fault might be avoided.

1.3 Condition health monitoring and its application to MMCs

Condition health monitoring (CHM) arises as an attractive strategy to predict and prevent failures to improve the reliability of power electronics-based converters, particularly of MMCs. The main idea behind CHM concept is to periodically monitor selected critical components utilizing failure precursor parameters monitoring in such a way that changes and trends of the monitored characteristic can be used to estimate the component health condition (or state of deterioration) and trigger preventive maintenance alarms before severe deterioration, or significant failure occurs [47].

Before condition monitoring techniques, scheduled maintenance was the primary maintenance strategy. Scheduled maintenance refers to inspecting and fixing a device during a non-operating time, either according to schedule or running hours. This idea might prevent many failures; however, it causes unnecessary shutdowns, and unexpected events will still happen between two maintenance periods.

In general, in power electronics applications, condition monitoring has been implemented through the following three approaches: 1) device parameters indicative of degradation and captured through the changes in the operational characteristic at a device or converter system level, for instance, ON-state voltage $V_{ce,sat}$ or resistance R_{on}, threshold gate voltage $V_{ge,th}$, and internal thermal resistance R_{th} using thermo sensitive electrical parameters in the case of the IGBTs; 2) dedicated sensors embedded in the device to monitor the physical degradation directly, for example, mechanical stress monitored using strain gauges or local resistance measurement to detect bonding wire off in IGBTs; and 3) model-based condition monitoring, in which the expected response of the converter to the stimulus, applied externally or available internally during regular operation, is dependent on the device condition, and degradation can be detected by comparing the measured response to the predicted by the model [48].

Despite that condition health monitoring ideas have been used in the power systems and power electronics field, the limitations of the existing condition monitoring techniques are still significant and have largely prevented its adoption in the field. The main limitations are summarized hereafter [47]:

- significant research is needed to reduce or avoid the use of internal-device sensors or sensors beyond those required for regular control and protection, as in new high-density power modules the available space is very tight, and additional hardware might be in opposition to reliability improvement and cost reduction,
- considerable research is needed to improve the condition monitoring techniques, mainly to increase their sensitivity to aging indicators signals due to the fast-switching transient and the relatively insignificant changes of device characteristics due to degradation. The research has to address several challenges regarding sensor techniques and signal processing,
- additional effort is needed to capture the collective effect of aging indicators over a significant

period, for example, the effect on converter efficiency and level of harmonics or electromagnetic emissions.

Similar conclusions are raised regarding CHM techniques in MMCs as the research in this area is recent and limited. In fact, the authors of [49] presented the first work where a CHM technique was used in an MMC just eight years ago. Consequently, several challenges remain still open implementing a reliable CHM technique on MMCs and that are addressed in this thesis.

1.4 Objectives and contributions of the thesis

Efficiency, power quality, power density, and voltage/current levels, among other characteristics of power electronics converter, have led to the developing and adoption of promising conversion technologies such as the MMC. Despite its several advantages and research, reliability issues related to the number of components, significantly those more sensitive such as power capacitors and IGBT, place the MMC as an immature technology. The early estimation of the degradation of the converter and its components using CHM techniques of some sort might improve its reliability, allowing alarms are triggered before a catastrophic fault occurs. Hence, this thesis focuses on developing CHM strategies applied to the MMC-level, SM-level, and SM components-level and their experimental validation using the PEL MMC research platform. Its main objectives and contributions can be summarized as:

- some of the existing CHM strategies found in MMC applications require either additional hardware (sensors or SMs) or modifications on control algorithms or specific operating conditions of the converter such as start-up or shut-down. In some applications, where these conditions are not allowed, it is of great interest to have a simple, accurate, and costless CHM method to monitor a specific component. This work proposes a feasible online CHM to monitor the SM electrolytic capacitors as they are some of the most critical and expensive components in the converter,

- even though typical SM contains two sensitive components (IGBTs and power capacitors), there is the need to monitor other components/circuits equally crucial for the proper operation of the converter, such as the SM local controller hardware, IGBT gate-drivers, and power supplies. This thesis aims to fill this gap by developing a CHM strategy using the ASPS power consumption as a means to estimate the health status of the whole SM,

- to assess the health status of an SM, it is common that different CHM strategies are performed for some particular components; however, specific research efforts is required toward integrating that available information to build a unique health indicator. In consequence, this thesis proposes a systematic approach in which all the existing CHM of an SM are integrated to create an indicator that comprehensively represents the health status of all the SMs.

- development of a SM and test platform so that all results are experimentally validated. One of the major difficulties in developing CHM methods for MMCs is the lack of a test setup in which experimental validation can be carried out, as its design and construction are complex and expensive. This work's contribution is the development of two 250 kVA MMC units based on the SM from **Fig. 1.1**, as par of medium voltage dc (MVdc) power supply.

1.5 Outline of the thesis

Following the Chapter 1, the thesis is structured as follow:

Chapter 2 discusses widely the CHM concept and how it has been applied in power electronics field. Particular emphasis is put in CHM strategies developed to assess health state of MMC at converter, SM and components level. Through a thorough literature review, the concept and a variety of approaches are presented, classified and compared, providing a complete overview of the state-of-the-art.

Chapter 3 introduces the main principles and equations that rule the operation of studied MMC, providing the basis for the development of this work. From simple voltage and current loop equations to more complex description of how energy is transferred, distributed and controled during converter operation. In addition, complete description is presented of the achieved PEL SM, emphasizing main components sizing and overall functionality. Experimental test results of its operation during the charging / operating and discharging process, protection actuators, and ASPS output regulation are provided.

Chapter 4 presents a CHM strategy for the MMC SM power capacitors. The method leans in the idea that capacitance reduction reflects the degradation level of the device, thus the proposed technique aims for the SM dc-link capacitance estimation. The strategy is deployed in the SM local controller. In each sampling period, the capacitance is estimated using the typically available SM terminal current, dc-link voltage, and the IGBT control signals, together with the recursive weight least squares (RWLS) parameter estimation technique. The method is introduced and validated thoroughly through offline and real-time hardware-in-the-loop (RT-HIL) simulations and experimental tests, showing its effectiveness in identifying actual and changes in the SM capacitance.

Chapter 5 introduces a new approach for a SM-level CHM. The strategy is based on observing different SM subcircuits by monitoring its single switch flyback-based ASPS consumption. The method settles on the idea that small changes in the circuits loading the ASPS secondary side can be detected and used to assess the deterioration level of an important portion of the SM circuits instead of a particular component. The ASPS consumption is estimated considering a simplified ASPS model, the SM dc-link voltage measurement and the ASPS switch pulses. Then, input power estimation at SM-level is compared against a fault dictionary to assess the SM (or a set of them) drifting from expected operation. The presented concept is deployed in a SM and validated experimentally.

Chapter 6 discusses and proposes a MMC CHM concept based on the integration of existing SM local CHM methods to compose a comprehensive converter or SM-level CHM strategy. A systematic approach to consider both expert and objective information coming from the SMs is presented. Through collected experimental data, numerical examples and offline simulations, it is discussed and demonstrated method performance and viability for its deployment on the PEL MMC research platform.

Chapter 7 summarizes the findings, contributions, and future work related to this thesis.

1.6 List of publications

Journal papers:

J1. **Polanco, Ignacio** and D. Dujić, "Condition health monitoring of modular multilevel converter submodule capacitors," *IEEE Transactions on Power Electronics*, vol. 37, no. 3, pp. 3544–3554, 2022

J2. S. Milovanovic, **Polanco, Ignacio**, M. Utvic, and D. Dujic, "Flexible and efficient mmc digital twin realized with small-scale real-Time simulators," *IEEE Power Electronics Magazine*, vol. 8, no. 2, pp. 24–33, Jun. 2021

J3. A. Christe, M. Petkovic, **Polanco, Ignacio**, M. Utvic, and D. Dujic, "Auxiliary Submodule Power Supply for a Medium Voltage Modular Multilevel Converter," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 3, pp. 204–218, Sep. 2019

Conference papers:

C1. **Polanco, Ignacio** and D. Dujic, "Estimating Auxiliary Power Supply Consumption of the Modular Multilevel Converter Submodule for the Condition Health Monitoring," in *PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2022, pp. 1–9

C2. **Polanco, Ignacio** and D. Dujic, "Thermal Study of a Modular Multilevel Converter Submodule," in *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2020, pp. 1–8

C3. M. Utvic, **Polanco, Ignacio**, and D. Dujic, "Low Voltage Modular Multilevel Converter Submodule for Medium Voltage Applications," in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2019, pp. 1–8

2

Condition Health Monitoring and its Application to MMCs

This chapter presents the state of research on the condition health monitoring techniques in the modular multilevel converter. Key concepts such as degradation, reliability, and prognosis and health management are introduced and used to present the main characteristics of the condition health monitoring concept and how it has been utilized to improve the reliability of power electronics devices and, particularly, the modular multilevel converter.

2.1 Devices degradation

In general, human-engineered artifacts, devices or system are conceived to fulfill one or multiple purposes. From a simple metallic knife to cut a piece of bread to very complex spacecraft rockets to support interplanetary exploration. Artifacts construction demand for particular materials or compounds to build their forming parts and sustain the required tasks. Intuitively and by everyday experience, materials present phenomena of loss of some quality or functionality along time and under certain conditions. For instance, the car tire wear due to its friction with road or the performance reduction in the photovoltaic modules due to thermal cycling. This phenomenon has been labeled as degradation, aging, deterioration, devolution, or wear-out [50]. Fundamentally, degradation is described by the second law of thermodynamics, where entropy, a measure of disorder, tends to increase with time in a closed system. The initial order created during device manufacturing (so that the device might be useful) decreases in a random manner (entropy increase) and becomes visible in the macroscopic world (aging) due to irreversible dissipative processes and forces, such as friction, chemical reactions, plasticity, dislocation movements, and corrosion [51]. If no external action is done to reduce or stop this process, eventually the degraded material fails and not useful work is able to perform.

Engineers and many other specialists, therefore, are confronted with a challenging situation in which they must manage the degradation rate of a device to prevent failure. For instance, aeronautic engineers have to ensure that aircraft do not fail during flying through extensive designing, testing, and quality manufacturing. Similarly, medical doctors are encouraged to maintain, restore, improve and prolong human health by administrating and performing appropriate treatment and counsel to patients. By recognizing that inevitably materials age with time calls up to quantify if a specific device will be able to perform the intended task it was made for, allowing, for instance that its design and/or the manner in which it is used might be corrected. This quantification has been made through the concept of reliability, i.e., the probability than an object system will perform its intended function for a specific interval under stated conditions [52]. Historically, reliability engineering emerged

as a military or space oriented discipline where long lifetime and harsh environmental conditions are expected, and in which is usually expensive to replace or repair a faulty component. Through test-to-pass approach based on standardized stress-based tests, devices were examined to withstand a set of specific conditions (application characteristics) for a specific period of time (expected lifetime) with no performance reduction (expectation). Then, characterized from several test resulted from test-to-pass approach, the first version of the US Military-Handbook-217 was published by the US Navy in 1962. It became quickly the standard by which reliability analysis was performed based on constant failure rate models [53]. After 1990s, an important amount of evidence suggested that reliability prediction of complex systems e.g., electronics circuits made of several integrated circuits (ICs), was not appropiate described by using constant failure rate models [38] so new releases of the US Military-Handbook-217 were officially canceled in 1995. Consequently, during 1990s, the concept of physics-of-failure (PoF), first presented in the 1960s, started to gain attention shifting the reliability assessment from pure empirical-based method to more scientific-based approach. The idea behind PoF is to reveal and analysis the root-cause of failure mechanism of components [54] by the analytic development of degradation models.

As per today, PoF concept is highly accepted in both industry and academy to assess devices reliability, however the idea of developing degradation model for each device part (or selected ones) is not sufficient neither advantageous when highly complex system is considered. Thus, three other concepts have been taken into account when one talks about reliability in power electronics as it was presented in [37]: Design for reliability (DFR), in which during the design phase of a component or system the required reliability level is ensured using mission profile technique (i.e., to use accumulated field experience, operating data and multiphysics-based simulation tools to simulate device degradation process); verification methods, such as accelerated tests (i.e., investigated component is overestressed in order to characterize its lifetime in the shortest period of time); and prognosis and health management (PHM).

2.2 Prognostic and health management

PHM, as it is presented in [55], can be understood as an engineering discipline to provide users/decision-makers with an integrated view of the health state of a device, machine or a system, focusing on assessing and minimizing the operational impact of failures. An effective PHM system is expected to provide early detection and isolation of the precursor and/or incipient fault of components or sub-elements; to have the means to monitor and predict the progression of the fault; and to autonomously trigger maintenance schedule and asset management decisions or actions. The detected, incipient fault condition should be monitored, trended from a small fault as it progresses to a larger fault, until it warrants some maintenance action and/or replacement. By employing such a system, the health of observed element can be known at any point in time, and the eventual occurrence of a failure can be predicted and prevented, enabling the achievement of near-zero downtime performance, avoidance of unnecessary and costly preventive maintenance, maintenance scheduling can be optimized, and lead-time for spare parts and resources can be reduced — all of which can result in significant cost savings. Please note that in this work the meaning of fault is the same as found in [52], i.e., an anomalous condition that can cause a device failure (unacceptable reduction in the required function).

Despite the idea of PHM seems very broad, it comes from merging two topics that are interesting in their own right, health management and prognostics (also known as prognosis). Health management

has been described by several authors [56], [57]; however, a complete and up to date definition can be found in the IEEE Std 1856-2017 [52]. It is stated that health management is the process of decision-making and implementation of actions based on the estimate of the state of health derived from health monitoring (current condition) and expected future use of the system, and includes the decision of what response actions to take and the actions themselves, which may include continuing operating, repair, replacement, reallocation of resources, re-prioritize functions/change system goals, and remove/ shutdown device.

On the other hand, the concept of prognostics, which feed-in the health management system, is known for coming from the medicine field and stand for the doctor's judgment of the likely or expected development of a disease or of the chances of getting better [56]. In the electrical engineering field, for instance, prognostics is considered as the process of forecasting for an object or system the time (or alternatively the remaining useful life (RUL)) at which will not longer perform its intended function within the desired specification, by means of predicting the progression of a fault given the historical available information, the current degree of degradation, and the anticipated future operational and environmental conditions. Deeper analysis and explanation of PHM, prognostics and health management can be found in [58]–[60].

What is relevant for this work is to recognize that implicit in the definitions of PHM, health management and prognostic, two foundational concepts, diagnostics (also known as diagnosis) and condition monitoring, are encountered. The term diagnostics refers to the action of determining the cause of an error in location (fault isolation) and nature (fault identification). Conversely, condition monitoring concept, which is the main topic of this thesis, is presented in detail in the following section.

An illustration of how each main concept operate is presented in **Fig. 2.1**, while **Fig. 2.2** shows PHM framework.

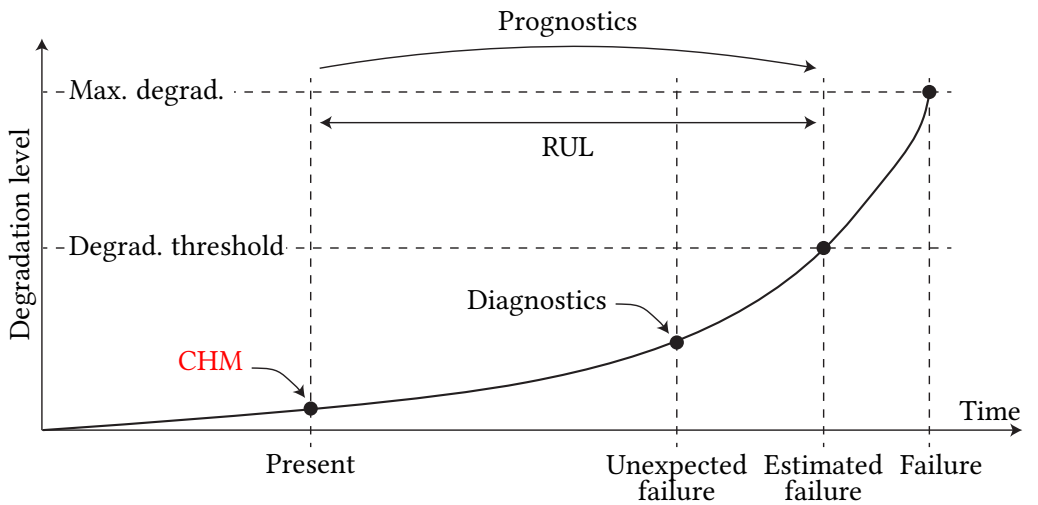


Fig. 2.1 Main concept differences with respect to time. CHM estimates the current degradation level of a component and result is compared with a degradation threshold to trigger an alarm. Prognostics uses CHM to perform a prediction of the future degradation state of a device. Ideally, prediction time is before the maximum degradation level of the component is reached. Diagnostics recognizes the cause and source of failure.

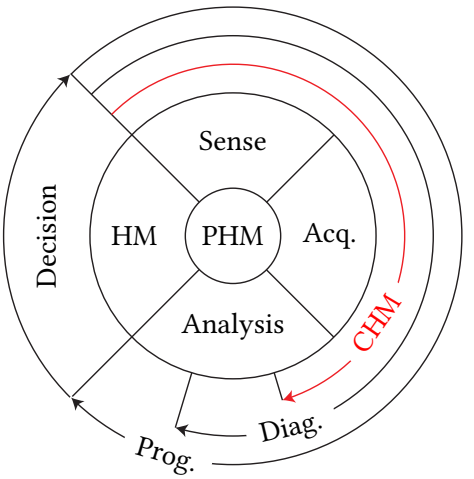


Fig. 2.2 PHM framework, adapted from [52]. Physical sensors convert real-world phenomena into electrical signals that are digitalized by an acquisition unit (data capture and processing). Then, information is analyzed at different levels: CHM uses a parameter threshold comparison; diagnostics detects, identifies, and isolates a failure; and prognostics predicts the future state. The analysis block outcome feeds the health management unit that defines and executes a response.

2.3 Condition health monitoring

According to [47], [52], [61] condition monitoring or condition health monitoring CHM concept is described as a technique or process of supervising the operating characteristic of a device in order that changes and or trends of the monitored characteristics can be used to predict the need for maintenance before serious/catastrophic deterioration or breakdown occurs.

The importance of CHM might be well understood from maintenance philosophies [62]. Typically, maintenance can be broadly classified as reactive (unplanned or unscheduled) and proactive (also known as scheduled or planned). Historically, reactive maintenance is performed mainly after device failure; however, logistic issues due to spare parts storage, highly trained labor force requirement, and downtime costs make this strategy economically non-attractive. Instead, proactive perspectives, such as preventive maintenance, i.e., to perform maintenance actions at predetermined intervals to reduce the probability of failure or performance reduction, are more convenient. The problem with the preventive maintenance philosophy is that considering past failure events will repeat in the future, used to determine maintenance intervals, is not necessarily true. Some of these events are random and highly affected by new and unexpected operating conditions. Thus, the PHM concept, driven by the idea of CHM, fills the uncertainty gap by constantly monitoring the device's health condition.

For this reason, the concept of condition monitoring is highly investigated and has gained relevancy in the electrical engineering field as well as in other scientific and industry areas. For instance, in the railway industry, condition monitoring techniques based on wireless sensor are employed to observe the state of bridges and tunnels (structural cracks and fatigue, static and dynamic loads, and ambient conditions), rail tracks and track beds (metal crack, displacement, twist and tilt), track equipment (e.g., fixations of actuators and sensors) along with vehicle health monitoring such as chassis, bogies, wheels, wagons (vibration) and locomotive engines (internal sensors) [63]. Another interesting example is the condition monitoring in wind farms, in which, vibration, acoustic emission,

strain, torque, temperature, and lubrication oil sensors along with electrical and supervisory data are used to estimated the mechanical and electrical state of wind turbines [64], [65]. It has been proposed to use fiber-optic acoustic sensor array for partial discharge monitoring in SiC-based MV converters as potential change of air properties and insulation degradation might happen [66]. In [66] it has been reported different strategies for condition monitoring of high voltage (HV) circuit breakers, namely, coil current during tripping, tracking of travel curve of breaker contacts, dynamic resistance measurement in main terminals, contacts mass loss estimation based on energy measurement during current interruption and mechanical vibration. In the healthcare field, it is possible to find examples where the human body is the observed "device". For instance, in [67]–[69], biomedical parameters e.g, body temperature, heart rate, respiration, and blood pressure to estimate medical conditions such as heart attack, tachycardia, bradycardia, myocardial infarction, atrial, ventricular fibrillation, atrial ventricular flutters and premature ventricular contractions. Similarly, in [70] by using a wearable acoustic sensor, diseases recognition, post-treatmeant monitoring and healthy habits improvement are achieved in children at day-care centers. Finally, authors in [70] presents a monitoring and prediction scheme of driver fatigue based on facial recognition (eyelid and gaze movement, head movement, and facial expression).

In order to achieve CHM goals, commonly found strategies are formed by the following sections [61], [71]:

- **Sensor technology** to convert a physical quantity (thermal, electrical, mechanical, chemical, humidity, biological, magnetic, or optical) to an electrical signal. Selection of sensor types and numbers depends on monitoring strategy, and vice verse, available sensors might define monitoring method. In addition, sensors should be suitable for online measurement (for instance, embedded in the observed system) and present good accuracy, sensitivity, precision, resolution, range, linearity, response time, stabilization time, size, weight, shape, and cost. Other forms of indirect sensing, such as duty cycles and pulse-width modulation (PWM) pulses in the case of power electronics-based converters, can be considered in this classification.

- **Data acquisition unit** to perform amplification and pre-processing of sensor's output signal, for instance, analog filtering, scaling and offsetting, analog-to-digital conversion, and digital signal processing. Data acquisition is commonly performed in DSP, field-programmable gate array (FPGA), or a combination.

- **Data analysis tool** to recognize degradation signs appearing in the device so that alarm can be triggered and further analysis can be exerted. There are two significant streams for data analysis method classification, model-based [62], and data-driven.

  Model-based methods focus on constructing mathematical models to comprehend systems' behaviors using physical laws or probability theories. Using such a model, a comparison between estimated and measured systems fed by the same input provides a residual or difference. How residual is created and analyzed will indicate the information to track the system degradation. For instance, using an observer-based approach such as Kalman filters, the system is considered aged-free if the discrepancy between the actual system state and estimated is zero. In another case, if parameter estimation techniques such as recursive least-square estimation are used, the system is considered degraded if the estimated parameter drifts from the expected value.

  On the other hand, data-driven methods are preferred when there is a lack of understanding of the dynamics of the observed system; thus, black-box modeling schemes fed by input/output

data are usually adopted, such as neural networks.

- **Failure mechanisms knowledge** so that abnormal behavior of observed degradation signals are post-processed, outcoming a clear indication of whether to perform a maintenance event or continue operating.

A CHM strategy should consider following aspects:

- Gathered information should ideally be acquired without disturbing regular device/system operation.
- depending on the application, online methods, i.e., performed during device operation, or offline methods, i.e., that require that device is completely off, starting up or shutting down is possible; however, the former is considered less practical as usually devices are required to operate uninterrupted;
- usability of existing hardware (sensors) and processing power units, generally utilized for system control and protection, should be preferred over the addition of extra components, as simple, cheaper, lighter, and smaller systems are preferable, mainly, for instance, in high-power density applications; and
- CHM method performance should be insensitive to the device operating conditions such as temperature, mechanical vibration, or electrical load so that related PHM sub-systems, for instance, prognostics, can be performed accurately at any given condition.

2.3.1 Major challenges

Even though CHM is a promising alternative to detect the early degradation state of a component, it still presents some challenges that have delayed its massive adoption, especially in industry. These challenges are summarized in this section.

Previously presented, CHM strategy relies on one or more parameters accounting for component degradation; however, this condition does not always hold as it might be that some degradation mechanisms are still not fully validated, complete, or are not applicable in every application. One example is the collector-emitter voltage in IGBTs. It is affected not only by the semiconductor junction temperature but gate oxide integrity, the quality of electrical connections, and metallization. [72].

For those applications that have overcome the previous scenario, numerous CHM implementations proposed in the literature have not found their way to be adopted in field applications. Complexity, cost, design constrictions, accessibility, and effectiveness under field operation environment might explain this behavior. Particularly, sensors technology or any other indirect measurement technique are challenging as several proposed CHM strategies are based on detecting relatively insignificant changes of device characteristics. Consequently, the acquired information is either not helpful or requires a considerable effort in signal conditioning (complex algorithms to process large amounts of data), requiring more powerful processing units. Thus, robust, cost-effective and straightforward condition monitoring methods are required.

Interestingly, little effort has been seen to capture the collective effect of the degradation process of a device, e.g., efficiency, consumption, harmonic content, delays, or electromagnetic emissions in the electrical engineering field. Most condition monitoring methods are limited to a single type of component or an individual component [72]. Nevertheless, simultaneous degradation could occur at

the application level on multiple components. Therefore, CHM methods based on the assumption that a single component degrades at a time might not reflect the actual device condition. Moreover, in some cases, a complete device is replaced in the presence of component fault or failure, which is not economically convenient as the remaining parts are still functional. Thus, further development of ideas such as system-level health precursors, system-level signal measurements [73], and data fusion techniques [74] might be required.

2.4 Condition health monitoring in power electronics

Previous examples illustrate that despite power electronics-based converters have been widely used, and technology is mature, scientific evidence of reliability issues can still be found in specialized literature.

In 2007 the Institut fur Solare Energieversorgungstechnik (ISET) released a study comprising the downtime caused by the malfunction of 1500 wind generators in Germany during 15 years of operation. The study concluded that for medium (rated power between 500 kW and 999 kW) and high-power generators (rated power above 1 MW) the annual failure rate is significantly higher than low-power generators (rated power below 500 kW) even though for those with more than ten years of operation (half of the expected lifetime). This is especially true for early failures in the first years of operation. Moreover, the study pointed out that half of the failures were due to mechanical malfunctions and the other half were due to electrical component issues distributed between sensors (10%), electronic controllers (18%), and electrical systems (23%) [34].

In [75] authors analyzed the failure information collected during 27 months between 2010 and 2012 from more than 600 PV plants installed in four continents operated by SunEdison. These systems range from a few kW to 70 MW, with more than 1500 power converters from 16 vendors. The study showed that 43% of failure events were from power inverters.

The problems with power converters might be even worse, as a study carried out in Chile, one of the countries with significant RES adoption in South America (around 10% of its energy mix in 2020) [76]. It is shown that PV plants comprising the 42% of the total installed capacity at the time of the study (around 585 MW in 2016), 85% of the failures were originated in the main power converters mainly due to the environmental and climate conditions, specially for the plants located in the Atacama desert where extreme weather, high solar radiation, high UV index and the salinity are present.

As suggested in [39], 56 responders of a survey carried out among component manufacturer, aerospace, automotive, motor drives and utility power companies identified power devices (31%) and capacitors (≈17%) as the most fragile components. The likely causes are environment (ambient temperature, moisture, lighting, humidity, and mechanical vibration), system transient and overload (severe electrical or thermal stress), and component design/manufacturing (packaging) [77], [78]. Thus, it can be recognized that most research about CHM (as well as many other reliability improvement techniques) applied to power electronics focuses on IGBT (and modules) and power capacitors.

The following part of this chapter focuses on the most classical failure precursors used for IGBT and power capacitors CHM.

2.4.1 CHM in IGBT technology

In IGBT (multichip and modules) technology, failure mechanisms are predominantly due to thermomechanical stress. Therefore, die-attach and bond wires are usually degraded; however, direct detection of these faults (due to encapsulated chips or detectable at microscopical level) is possible mainly by very invasive techniques such as scanning electron microscopy. Thus, more practical strategies considering monitoring key-sensitive parameter variation are needed and described hereafter.

- **On-state collector-emitter voltage-based strategy**: Bond wire fatigue (bond lift-off and flexure of wire heel) and die-attach are recognized as significant failure sites in wire-bond power modules as well as multichip IGBT modules for high-power applications. The leading cause is a significant coefficient of thermal expansion mismatch and temperature swings imposed both by the power dissipation in the silicon and by the ohmic self-heating of the wires. Several authors have investigated the relationship between $V_{CE,on}$, die-attach degradation and bond wire fatigue, resulting in different levels and trends of the device being considered degraded. For instance, in [79] $V_{CE,on}$ drops during the thermal overstress test (accelerated aging test) due to die-attach degradation. A $V_{CE,on}$ decrease of 8-25% range is considered a degraded device, and it should be replaced before latch-up failure mechanism triggering (i.e., parasitic p-n-p-n thyristor structure inherent in the device is activated, producing loss of collector current control by the gate). On the other hand, a 3% $V_{CE,on}$ increase was identified as a fault, being the aging of wire bonds during power cycle tests as its primary cause [80]. Even though $V_{CE,on}$ can reflect the degradation state of the IGBT module, its use as a failure precursor is still challenging due to measuring complexity (signal noise or disturbance during switching might lead to uncertainties in the range of the parameter variation) and because at least two failure mechanisms may compete, nullifying overall effect.

- **Gate-emitter threshold voltage-based methods**: $V_{GE,th}$ is the gate voltage at which the IGBT turns on, and the collector current starts flowing. Its increase has been observed during thermal stress tests, attributed to the gate oxide degradation. Authors in [79] detected threshold voltage increases during tests and claimed that a maximum rise of 11% is considered a fault. Similarly, in [81], a 300 mV increase variation was found. In [82], several experimental tests were carried out for different IGBT technologies, validating the increasing trend found before. Authors suggested that $V_{GE,th}$ is a more stable parameter to detect IGBT degradation than $V_{CE,on}$. However, it is worth mentioning that $V_{GE,th}$ measurement at the chip level is very impractical due to the closed encapsulation of the IGBT module.

- **Switching time-based methods**: use the change of waveforms, namely V_{CE}, V_{GE}, I_{CE}, and or I_{GE}, during IGBT turn-on or turn-off [83]–[85] to detect device degradation. In [84] is monitored V_{GE} during turn-on to detect bond wire failure. It was shown that already failed components present a faster rise rate of V_{GE} than healthy devices, limiting its application as a failure precursor. Similarly, in [85], the gate current I_{GE} is observed, showing little variation during the degradation test (bond wire lift-off). However, both proposals might be applicable in high-power modules where several IGBT chips are present. In [86], t_{off} is defined as the amount of time for V_{CE} to increase from 10% to 90% of its final value during turn-off. The study demonstrated the ability to distinguish the difference between aged and healthy IGBTs using measurements of t_{off} within an operating temperature range of 305 K to 315 K. V_{CE} rising slope is bigger for healthy components, allowing the authors to claim that t_{off} value might be considered an early indicator of latch-up failure caused by damage in the die attach layer.

- **Temperature-based methods**: rely on the idea that device thermal resistance R_{th} raises due to cracks and voids between the silicon die and base plate (heatsink), reducing the effective area for heat dissipation produced during the repetitive thermomechanical load application, and leading to junction temperature increment. Thus, at higher junction temperature, the die becomes susceptible to secondary breakdown, delamination of the metallization layers on the ceramic substrate and brittle fracture of the substrate itself [87]. The challenge with this approach is that measurement of the crack or void sizes, device thermal resistance, and exact junction temperature is not easy to address. Instead, their indirect monitoring by measuring other available parameters is more convenient. A simple way to estimate the junction temperature is to use a temperature sensor near the junction with a thermal model [88]. This approach enables online measurement without interrupting IGBT operation; however, it is invasive, and the sensor location affects the measurements' accuracy. Another method is to deduce the junction temperature from measurements of a temperature sensitive electrical parameter (TSEP) such as $V_{CE,on}$. This approach consists of two steps, an offline characterization of IGBT under test ($V_{CE,on}$ versus junction temperature); and an online estimation using $V_{CE,on}$ measurements to retrieve junction temperature [88]. As stated before, real-time measurement of $V_{CE,on}$ is challenging, especially in cases where the switching frequency is high. Another more feasible approach was presented in [89]. The die attache damage was monitored by measuring the device case and the ambient temperatures. The power loss producing the temperature gradient is estimated from a thermal model. A lookup table that provided power loss information of healthy IGBT modules was subsequently incorporated, enabling the estimation of solder layer damage under various operating conditions. In the analysis, thermal transient within the module was assumed to be much faster than the variation of the electrical operating point. This assumption may limit the use of the method in, for instance, wind power and traction applications, where the environmental and operating conditions can change faster than the duration required for IGBT dies to reach their steady-state temperature. Authors in [90] propose a technique for real-time monitoring of power module thermal response through a thermal observer structure that combined with a loss injection algorithm, manipulates gate resistance and switching frequency for small signal device loss excitation, creates a device self-sensing unit, i.e., it enables the adaptive calibration of the device loss model, and it can conduct in-situ thermal impedance spectroscopy of the power module over multiple frequency decades.

- **Others**: Alternatively, several works have proposed using application-level measurements to identify semiconductors' state of health. For instance, in [91], the authors proposed that non-ideal switching (affected by device junction temperature) in a voltage source inverter, is reflected in the output low-order harmonic content. Similarly, the authors in [92] observed high-order oscillatory responses in the voltage amplitudes and currents during switching. This response was related to the changes in parasitic capacitances in IGBTs after thermoelectrical aging. In [93], a spread spectrum time domain reflectometry-based approach was described. The idea is to use the reflectometry approach to measure IGBT collector-emitter impedance (an indirect measurement of $V_{CE,on}$).

Additional interesting information about the IGBT failure mechanism and related parameters can be found in [77], [94], [95], while **Tab. 2.1** summarizes main employed IGBT parameters for CHM.

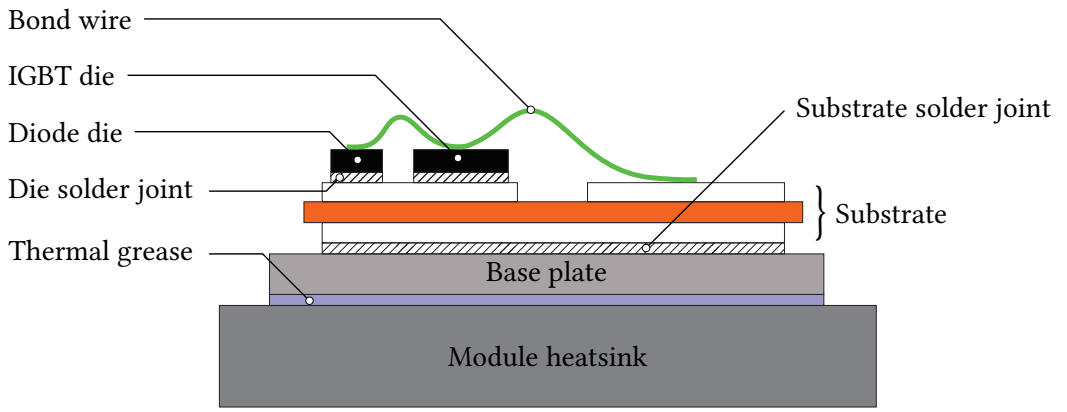


Fig. 2.3 Cross-section of the structural scheme of a bond wire IGBT module. Please note that module heatsink and thermal grease are elements commonly added by the user.

Tab. 2.1 Overview of main IGBT CHM parameters

CHM parameter	Degrad. threshold	Main stressor	Site	Failure mechanism	Failure mode
$V_{CE,on}$	↓8-25%	Electrical overstress, high temperature	Silicon die-attach	Latch-up, secondary breakdown	Loss of gate control, short circuit
	↑3%	Thermomechanical	Bond wire fatigue	Mechanical fatigue	Open circuit
$V_{GE,th}$	↑11%, 300 mV	Over voltage, high temperature, high electric field	Gate oxide layer	Time dependent dielectric breakdown	Increase leakeage current, loss of gate control, short circuit
$\frac{d}{dt}V_{GE}(t_{on})$, $\frac{d}{dt}I_{GE}(t_{on})$	↑	Thermomechanical	Bond wire fatigue	Mechanical fatigue	Open circuit
$\frac{d}{dt}V_{CE}(t_{off})$	↑	Electrical overstress, high temperature	Silicon die attach	Latch-up, secondary breakdown	Loss of gate control, short circuit
R_{th}	↑20%	High temperature	Silicon die attach, solder layer	Secondary breakdown, thermal runaway	Short circuit, delamitacion of metallization

↑: increase, ↓: decrease

2.4.2 CHM in power capacitors

Power capacitors in power electronics-based applications are extensively and mainly used in converters dc-link to balance the instantaneous power difference between input/output terminals [78]. The most common technologies are aluminum electrolytic capacitor (Al-cap), metallized polypropylene film capacitor (MPPF-cap), and multilayer ceramic capacitor (MLC-cap). The three types exhibit different advantages and disadvantages. The Al-caps achieve the highest energy density and lower cost per Joule; however, relatively high equivalent series resistance (ESR) (cf. **Fig. 2.4**), low ripple current levels, and wear out problems due to electrolyte evaporation. The MLC-caps have smaller sizes, a wider frequency range, and higher operating temperatures; however, they present higher cost and mechanical sensitivity. The MPPF-caps present an excellent performance for HV applications in cost and ESR, capacitance, ripple current, and reliability. Nevertheless, they present large volume and moderate high operating temperature. Authors in [96] thoroughly described and compared these three technologies.

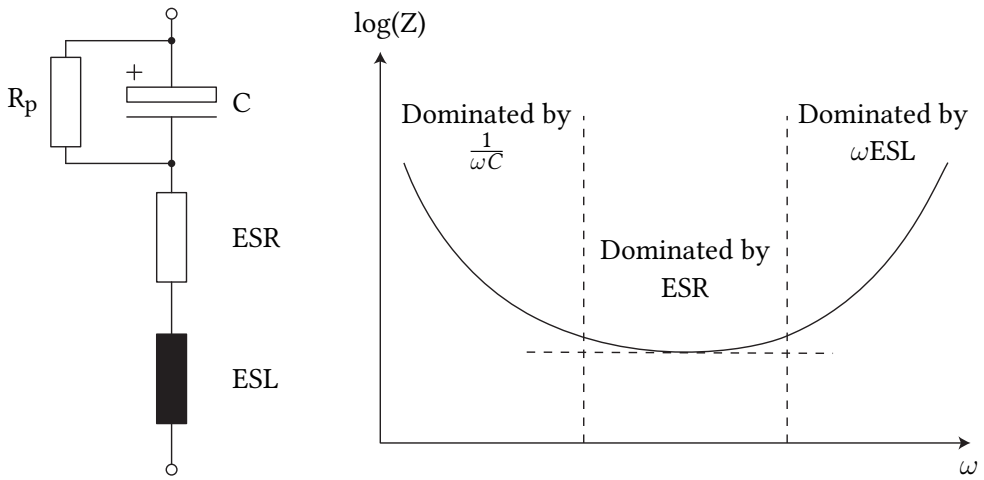


Fig. 2.4 Capacitor lumped model and its impedance characteristic. C is the ideal capacitance; R_p is the insulation resistance; ESR is the equivalent series resistance and represents all ohmic losses ; and equivalent series inductance (ESL) is the equivalent series inductance due to capacitor's leads connection path.

As power capacitors are considered the second most sensitive (i.e., present higher failure rate compared to other elements) component found in power converters, this section focuses on presenting major failure precursor parameters used for capacitor CHM strategies.

Due to intrinsic and extrinsic factors, such as design defects, the material wearing out, operating temperature, voltage and current, moisture, and mechanical stress, capacitors could fail. In the case of MLC-caps, the primary failure mechanisms are dielectric breakdown due to microcracks, delaminations, and impurities in the ceramic and flex cracking [78], [97]. In the case of MPPF-caps, dielectric breakdown and reduction in electrode area due to electrical overstress (e.g., overvoltage) and corrosion (e.g., atmospheric moisture) are the principal mechanisms of failure. In Al-caps, the primary failure mechanism is the electrolyte vaporization, caused by their relatively high ESR and limited heat dissipation surface (small size capacitors), and an increase of leaking current flowing in the electrolyte due to cathode foil deterioration (big size capacitors) [98]. Even though the capacitor technologies are quite different, it is expected that all these three types of devices degrade in a regular application, showing similar failure precursors: capacitance reduction, ESR increment, and dissipation factor increment. The only exception is MLC-caps, which instead of ESR variation, it is the insulation resistance R_p found to change while the device degrades (cf. **Fig. 2.4**). **Tab. 2.2** summarizes the failure precursor, degradation threshold, primary stressors, failure mechanisms, and failure mode for all three technologies.

From the CHM point of view, as the failure precursors and their trend and threshold values are well established theoretically and experimentally, the primary challenge is to identify the most practical strategy to measure or estimate those parameters. Several strategies have been proposed depending on the converter topology, capacitor technology, failure precursor target, sensor availability, and computational power. For instance,[99] presented an offline method, i.e., the operation of the observed system has to be interrupted, to estimate the ESR and C of the output capacitor of a buck converter. A signal generator exciting the device and a scope measuring its response is used to calculate the capacitor impedance at 120 Hz and 1 kHz to estimate the capacitance and ESR, respectively. Despite the promising results provided for this method, the converter has to be not operating, and the

Tab. 2.2 Overview of main capacitor CHM parameters

Technology	CHM parameter	Degrad. threshold	Main stressor	Failure mechanism	Failure mode
Al-caps	C	↓20%	V_{cap}, T_{amb}, I_{cap}	Self-healing dielectric breakdown	Open circuit
	ESR	↑200-250%	Vibration	Disconnection of terminals	
	DF	↑200 %	V_{cap}, T_{amb}, I_{cap}	Dielectric breakdown of oxide layer	Short circuit
			T_{amb}, I_{cap}	Electrolyte vaporization	Parameter drift
			V_{cap}, T_{amb}, I_{cap}	Electrochemical reaction	
MPPF-caps	C	↓5%	V_{cap}, T_{amb}, $\frac{d}{dt}V_{cap}$	Self-healing dielectric breakdown	Open circuit
	ESR	↑150%	T_{amb}, I_{cap}	Connection instability by heat contraction of a dielectric film	
	DF	↑300%	Humidity	Reduction in electrode area (moisture)	
			V_{cap}, $\frac{d}{dt}V_{cap}$	Dielectric film breakdown	Short circuit (with resistance)
			Humidity	Moisture absorption by film	
			V_{cap}, T_{amb}, I_{cap}, humidity	Dielectric loss	Parameter drift
MLC-caps	C	↓10%	V_{cap}, T_{amb}, I_{cap}	Dielectric breakdown	Short circuit
	DF	↑200%	Vibration	Cracking, body damange	
	R_p	$<10^7\Omega$	V_{cap}, T_{amb}, I_{cap}, vibration	Oxide vacancy migration, dielectric puncture, insulation degradation	Parameter drift

↑: increase, ↓: decrease, V_{cap}: capacitor voltage stress, I_{cap}: capacitor ripple current stress, T_{amb}: ambient temperature, DF: dissipation factor

procedure has to be repeated for each capacitor; thus, it is not practical for continuous operation applications and those with a large number of capacitors such as MMC.

On the contrary, online methods, i.e., the monitored system operating while health indicators are obtained, are considerably more convenient. In this case, precursor failure extraction is relatively more complex as electrical noise conditions, sensor availability/addition, system modeling, and computational power play an important role. For instance, authors in [100] proposed an online strategy to estimate the capacitance of the dc-link of a three-phase ac-ac converter in a back-to-back configuration. By injecting a 30 Hz voltage component in the dc-link using the converter control algorithm, knowing the system's input/output active power, and using the recursive least squares (RLS) method, the capacitance was estimated with less than 0.4 % error. The result and concept are auspicious; however, two main drawbacks might be considered further. The first is that input/output power in such a system is not always accurate (two ac current sensors, assuming balanced currents) or available (ac voltage measurement or current in the dc-link). The second issue is that additional voltage harmonic injection might increase dc-link voltage and current ripple, increasing losses and voltage stress in the device.

A similar approach is proposed in [101]; however, no harmonic injection is employed. Instead, it is used the dc-link voltage and current harmonics that naturally appear due to the input/output power transfer in a single-phase grid-connected PV inverter. The authors claim that capacitance can be estimated by simply dividing the integral of dc-link current and associated voltage ripple during half of a fundamental period, obtaining a maximum error of 2.56%.

The main characteristic of previously presented strategies is that they are model-based methods, i.e., a minimum knowledge of the system dynamics and its operation is required. When this condition is impossible to meet, approaches like [102] and [103] are attractive. In [102], it is proposed to use an artificial neural network (ANN) for the condition monitoring, and its application is illustrated using a FB diode rectifier. The ANNs are intelligent tools that view the circuit as a black box and do not consider the circuit level details. Well-established training algorithms enable these intelligent systems to map the input(s) of the circuit to the corresponding output(s) at any point in time, over a wide range of operating conditions. By using this method, in particular, it is possible to recognize a 0.5 Ω resistance placed in series connection with the dc-link capacitor. In [103], the authors propose an ANN to estimate the dc-link capacitance of the same topology tested in [100] (back-to-back converter). Simulation results show that a maximum error of 0.5% is achievable. This technique's challenges are the amount of training data used to adjust the ANN gains and the extra computational burden.

2.5 Condition health monitoring in modular multilevel converter

As will be extensively introduced in the following chapter, the MMC is formed by several SMs, each made of power semiconductors devices, power capacitors, printed circuit boards (PCBs), ICs, magnetics, mechanics, connectors and passive components. Thus, due to the large number of parts, among other factors such as operating conditions, design considerations, and control strategy, it is that MMC reliability might be of concern and the use of a CHM strategy of some sort becomes a highly desirable feature. This section presents the latest advances in CHM methods applied to the MMC.

Despite the MMC concept is known for more than 20 years, the development of CHM techniques

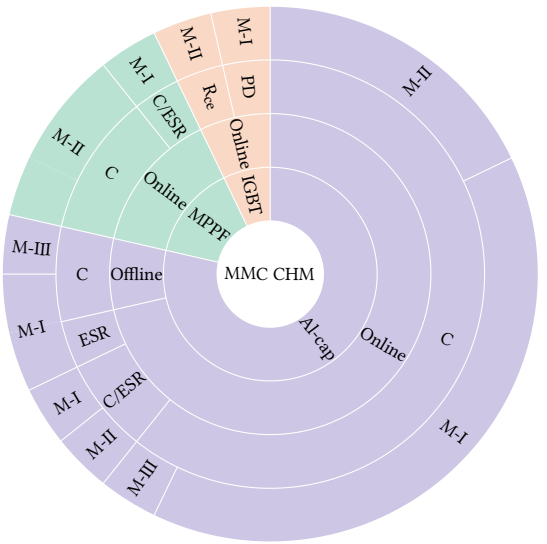


Fig. 2.5 State-of-the-art summary of the CHM concept applied to MMCs. Each layer represents a method classification category. From the inner layer: component/technology (Al-cap, MPPF-cap and IGBT); availability (online/offline); precursor parameter (Capacitance (C), ESR, IGBT collector-emitter resistance (R_{ce}), and partial discharge event (PD); and data analysis strategy (M-I, M-II, and M-III).

applied to its components is relatively recent and modest. Based on the IEEE Xplore database, only 28 scientific publications were found addressing the topic, the first published in 2014 [49]. A complete cadastre of found publications is presented in **App. A** and summarized in **Fig. 2.5**.

Aligned with the development of CHM in other power electronics-based applications, the two most sensitive components, the SM power semiconductors, typically IGBT (7%) and, notably, power capacitors, typically Al-cap (79%), and MPPF-cap (14%), are those of the most interest. Introduced early in this chapter, CHM strategies can be broadly classified online and offline. In this sense, only [104] is considered offline as it estimates the SM capacitance during the system start-up. During the passive charging of the SMs, the branch current, the SM dc-link voltages, and charging time are used to solve the well-established circuit formed by the converter dc-port, the pre-charge resistor and the SMs within a leg. This idea achieves high accuracy (1% estimation error); however, in some applications, where the converter requires permanent operation, it is not practical.

Observed failure precursors are capacitance (C) and ESR for capacitors, collector-emitter resistance (R_{ce}), and partial discharge events in the case of IGBT. For instance, in [105], a tunnel magnetoresistance is used to estimate the capacitance of the MPPF-cap. The idea consists of measuring the capacitor current in an HB SM through this sensor technology. Then, the parameter is extracted using the well-known capacitor model and RLS method. The advantage of the proposed sensor is high current capacity, high response (it can feed a current protection scheme), and low cost (10% of equivalent commercial solution).

Authors in [49] estimate the HB SM Al-cap capacitance by injecting a second harmonic current component in the leg circulating current path, inducing the same voltage and current frequency component in the SMs capacitors. Then, a band-pass filter and the RLS methods are employed to extract the impedance and the capacitance, respectively. Even though the proposed idea achieves a 1.3% estimation error, the required injected signal and digital filters might impose additional losses

and computational burden, respectively. In [106], both C and ESR are estimated. The idea is based on measuring capacitor voltage and current (reconstructed from switches state) during SM inserted period. To deal with short inserted periods, the authors selected consecutive periods to apply the method. It is achieved a 3.3% and 0.01% estimation error for ESR and C, respectively. The presented idea promises high accuracy and estimation time (1.5 ms); however, it is validated only by simulations, and limited to control strategies based on sorting algorithms.

In the case of IGBT, in [107] is proposed to estimate on state resistance (R_{ce}). The parameters are calculated from branch voltage and current, SMs switches states, and diodes forward voltages, corrected by junction temperature. Finally, a Kalman filter is utilized to improve estimation accuracy. Authors claim a 3% estimation error; however, the method relies on junction temperature, voltage sensor accuracy, and the assumption that diode forward voltage is constant; in addition, results are validated only through simulations. On the other hand, in [108], the authors propose a method to detect partial discharge events to monitor the IGBT state of health. By sensing the capacitor current of an HB SM and employing wavelet analysis, the current associated with a partial discharge event in the turned-off IGBT is recognized. The idea seems novel in this context; however, sensors and acquisition units with high bandwidth, accuracy, and sensitivity are required. A further experimental investigation should be done to validate this idea entirely.

The last layer of **Fig. 2.5** classifies the publications according to the employed data analysis strategy. Three categories are presented: model-based with direct calculation (M-I), model-based with parameter identification technique (M-II), and data-driven (M-III). Model-based methods, as introduced before, mean that mathematical models to comprehend the system's behavior are known. In particular, M-I is an estimation using analytic equations that are solved using parameters (assumed constant) and variables from the acquisition system. On the other hand, in M-II classification it is considered the use of a more advanced technique to manage the uncertainties produced by the inherent noise in the measurements, such as the Kalman filter. On the contrary, M-III refers to methods that do not use mathematical models but input/output data.

An example of M-I classification is found in [109], where the voltage difference during the charging process of a reference and observed SM is used to compute the capacitance difference between them. This method is straightforward; however, it presents several implementation drawbacks. For instance, the capacitance of the reference SM has to be known beforehand, typically estimated by a different method. Additionally, twelve SMs (the reference and observed SM per branch) must be shut down for several hours (as the capacitors discharging process is time consuming) to perform the method.

Work presented in [110] is an example of M-II classification. Like other publications, capacitance is first calculated by integrating reconstructed capacitor current (using switches state) divided by voltage variation. Due to inherent noise in both acquired current and voltage, capacitance estimation can be significantly distorted; thus, the RLS method is employed for parameter identification, reducing estimation error to 0.86% (a substantial improvement compared with a 1.7% obtained using a low-pass filter).

Finally, [111] and [112] are examples of M-III classification. Authors in [111] propose using a back propagation neural network to recognize SM capacitance variations as a function of switching frequencies (a consequence of nearest level modulation). A maximum estimation error of 1% is achieved, and the authors claim that implementation is simple. However, significant data training is required and centralized switching frequency measurement (at least per branch). In the case of

[112], the reliability-guided one-class classification method is introduced, in which, after training, the classifier computes the probability of the current system operation being within the normal range (capacitance).

Considering the presented state-of-the-art works, it is interesting to highlight the following conclusions:

- M-III methods are slowly entering the field, promising fast, accurate and straightforward solutions for CHM. The bottleneck might reside in the limited available computational power, especially in those methods implemented locally in the SM (main tasks are data acquisition, protection scheme, and communication) and the amount of data required to train and test the methods. It is expected that future M-III methods will consider more than just capacitors and semiconductors, providing a more comprehensive indication of the state of the SM.
- Just little effort has seen monitoring the power semiconductor and technologies different than IGBT, despite the important number of publications covering this topic in other applications. A reason might be the technical limitations of the commonly available sensors in the SM, as parameters such as V_{ce} present slight variations while component degrades. In addition, with the improvement of mathematical tools, for instance, state observers, the trend is to use fewer sensors, mainly to perform control strategies, interfering even more with the CHM development.
- MMC CHM is completely focused on nothing more than capacitors and IGBTs, even though several other components exist at the SM and converter level. This trend might be explained considering the evidence of the relatively high failure rate of capacitors and power semiconductors compared with other components such as gate-drivers or DSP, despite failing and producing converter shut-down.
- No effort was found to monitor the state of health at the SM level, by integrating existing CHM indicators or using a different approach to observe the whole unit. A similar conclusion might be found at the converter level.
- More than 50% of revised methods were validated only by simulations, neglecting the non-ideal conditions and practical issues detected during laboratory experiments and inducing the idea that some schemes are highly accurate. For instance, the minimum estimation error claimed using simulation was 0.01% [106], [113], 26 times better than the minimum found using laboratory experiments [105].
- Current state-of-the-art does not reflect the application of other related topics such as PHM and prognostics applied to MMC, which might be explained considering the lack of maturity in developing CHM techniques. This observation matches MMC technology's maturity and encourages further investigation into this topic.

2.6 Summary

In this chapter, the CHM concept is thoroughly presented, starting from a comprehensive contextualization through introducing the ideas of PHM, prognostics, health management, and diagnostics. A variety of cases in which CHM is applied are presented in electrical engineering, power electronics, and other areas to illustrate and demonstrate the importance and complexity of the concept.

In particular, a complete review is presented and discussed on how different CHM strategies are formulated and implemented in the MMC. It is shown that the topic of this thesis still is an early stage of development and, therefore, additional research has to be made on proposing and validating novel CHM strategies, for instance, at components, SM, and converter level. Following chapter presents the fundamental principles that explain classical MMC operation, and it is introduced the PEL MMC research platform where MMC CHM research is carried out.

3
Modular Multilevel Converter and Submodule

Although MMC can be found in different applications and topologies or modeled and controlled using various techniques, this chapter focuses on the classic three-phase ac-dc MMC and the full-bridge SM as its building block. Theoretical description of these two elements with particular stress on SM description, main characteristics and functionalities, and selected illustrative experimental results expose the hardware conditions and assumptions in which this thesis is elaborated.

3.1 MMC operating principles

The MMC, first introduced in [114], belongs to the high-power MV cascaded topologies and it is founded in the use of multiple low-voltage low-power power electronics building blocks, namely SMs, with a single-phase ac terminal and an energy storage element, commonly capacitors. The ac-dc MMC depifcted in **Fig. 3.1** is the classical configuration in which bidirectional ac-dc conversion is possible.

The series connection of the SMs with an inductor form a branch. The inductor is needed to filter the high order harmonics of branch current, to allow parallel branch connection, and to limit branch

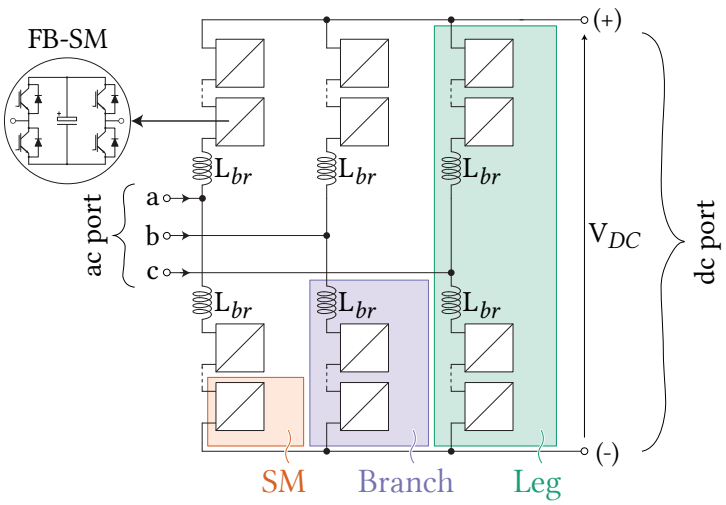


Fig. 3.1 Classical ac-dc MMC scheme and common nomenclature. Highlighted in red, the SM is the building block of the converter. The series connection of several SMs with an inductor form a branch (highlighted purple), and finally, the connection of two branches form a leg (highlighted green). The three-phase port can be recognized in the picture's left side while in the right side is the dc port (for the sake of completeness, the dc port also can operate as ac port).

short circuit current in case of faults. Two series-connected branches form a leg whose midpoint is connected to the converter ac port. Finally, the three legs connected in parallel form the converter. The main advantage of this idea is that employing an arbitrary number of identical SMs within a branch (modularity) it is possible to achieve an arbitrary output voltage while harmonic performance and efficiency are high.

The MMC operation is based on controlling the six branches such that the MMC ac and dc port voltage magnitudes are as desired, irrespectively of current polarity or magnitude; thus, the converter might operate as a rectifier or inverter with leading or lagging power factor. The sum of branch voltages (upper and lower) is approximately equal to the dc port voltage, while the voltage difference can be set at any point within dc port voltage. Thus, the three legs can provide a set of three symmetrical alternating voltages while the dc port is kept constant, meaning that the MMC can act as voltage-source converter (VSC) in both the ac and dc terminals.

In order to derive the MMC main equations and without loss of generality, one can consider the simplified scheme of **Fig. 3.2**, where only leg 1 is detailed and used hereafter for analysis purposes. For simplicity, it is assumed that all the SMs are identical, and the branch inductors have the same value L_{br} without any magnetic coupling between them. In addition, it is considered that the converter's ac port terminals are connected to a three-phase source with neutral point n and without source impedance, while the dc port is represented by two series connected dc sources with a midpoint O and without source impedance. Accordingly, Loop 1 and Loop 2 circuits can be identified. Loop 1 comprises the upper or positive branch, the positive dc source (v_{dc1}), and the ac source. Loop 2 comprises the lower or negative branch, the ac source, and the negative dc source (v_{dc2}). Then, using the Kirchhoff's voltage law (KVL) for each loop yields

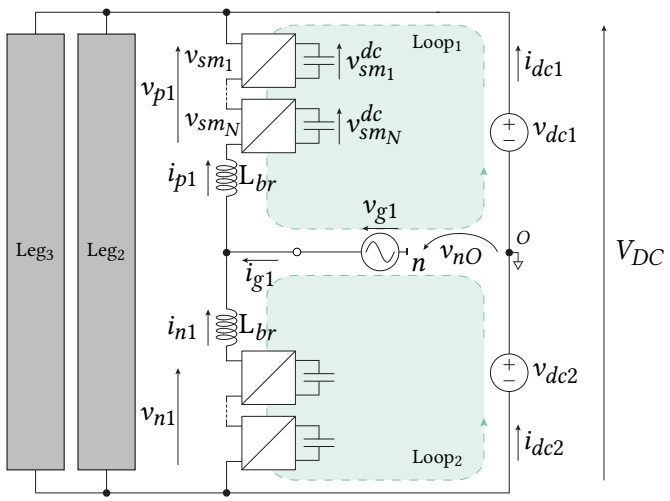


Fig. 3.2 MMC leg 1 equivalent circuit and nomenclature. N series connected SMs with the inductor L_{br} form the positive branch. Similarly, another set of N SMs and an inductor in the bottom part form the negative branch. The i-th SM synthesizes a voltage v_{sm_i} using its dc-link voltage $v^{dc}_{sm_i}$, with $i = \{1, ..., 2N\}$. The leg 1 midpoint is connected to the line source voltage v_{g1}, while the other two terminals are connected to the dc port of the converter. In order to facilitate the mathematical analysis, the dc port is modeled by the two dc sources v_{dc1} and v_{dc2}, with midpoint O.

$$-v_{dc1} + v_{p1} + L_{br}\frac{di_{p1}}{dt} + v_{g1} + v_{nO} = 0 \tag{3.1}$$

$$-v_{dc2} + v_{n1} + L_{br}\frac{di_{n1}}{dt} - v_{g1} - v_{nO} = 0 \tag{3.2}$$

By summing and subtracting these two equations it is obtained

$$v_{dc1} + v_{dc2} = v_{p1} + v_{n1} + L_{br}\frac{d(i_{p1} + i_{n1})}{dt} \tag{3.3}$$

$$v_{dc1} - v_{dc2} = v_{p1} - v_{n1} + 2v_{g1} + 2v_{no} + L_{br}\frac{d(i_{p1} - i_{n1})}{dt} \tag{3.4}$$

On the other hand, applying the Kirchhoff's current law (KCL) in the dc positive and negative terminals yields

$$i_{dc1} = i_{p1} + i_{p2} + i_{p3} \tag{3.5}$$

$$i_{dc2} = i_{n1} + i_{n2} + i_{n3} \tag{3.6}$$

In order to simplify the following analysis, it is common to utilize the linear transformation (3.7) for the branch voltages and (3.8) for the branch currents

$$\begin{aligned} v_{s1} &= \frac{v_{n1} - v_{p1}}{2} \\ v_{c1} &= \frac{v_{p1} + v_{n1}}{2} \end{aligned} \quad \Longleftrightarrow \quad \begin{aligned} v_{p1} &= v_{c1} - v_{s1} \\ v_{n1} &= v_{c1} + v_{s1} \end{aligned} \tag{3.7}$$

$$\begin{aligned} i_{s1} &= i_{p1} - i_{n1} \\ i_{c1} &= \frac{i_{p1} + i_{n1}}{2} \end{aligned} \quad \Longleftrightarrow \quad \begin{aligned} i_{p1} &= i_{c1} + \frac{i_{s1}}{2} \\ i_{n1} &= i_{c1} - \frac{i_{s1}}{2} \end{aligned} \tag{3.8}$$

then, equations (3.5) and (3.6) can be rewritten as

$$\frac{v_{dc1} + v_{dc2}}{2} = v_{c1} + L_{br}\frac{di_{c1}}{dt} \tag{3.9}$$

$$\frac{v_{dc1} - v_{dc2}}{2} = -v_{s1} + v_{g1} + v_{no} + \frac{L_{br}}{2}\frac{di_{s1}}{dt} \tag{3.10}$$

where i_{s1} is the leg 1 ac terminal current (equivalently i_{g1}) and v_{s1} is the inner electromotive force (EMF) of leg 1 driving this current. Correspondingly, i_{c1} is the current that flows through the leg

1, whereas v_{c1} is the voltage driving this current. It is important to highlight that i_{c1} is found with different names and interpretations among scientific publications, thus to avoid misleading concepts, in this work, the current i_{c1} already considers one-third of the dc port current and the circulating current of the leg 1 named i_{circ1} as it will be addressed in more detail later in this chapter.
In most practical cases, there is no dc port midpoint connection, implying that $v_{dc1} + v_{dc2}$ is equal to the dc port voltage V_{DC}, and $v_{dc1} - v_{dc2}$ equals zero, thus $v_{dc1} = v_{dc2} = \frac{V_{DC}}{2}$, and $i_{dc1} = i_{dc2} = I_{DC}$. Then, by observing equations (3.9) and (3.10) can be concluded:

- for a constant value of V_{DC} the current i_{c1} is controllable by the voltage v_{c1}. This can be extended to the legs 2 and 3,
- for a constant magnitude of the voltage v_{g1}, the current i_{s1} is controllable by the voltage v_{s1}. This can be extended to the legs 2 and 3,
- the voltage v_{no}, also known as common-mode voltage, accounts for any imbalance between the upper and lower dc side voltages. It is considered zero in this work, but it might be used for 3$^{\text{rd}}$ harmonic injection.
- equation (3.9) describes all the dc side magnitudes, while equation (3.10) the ac side magnitudes, implying that both ac and dc port power can be controlled independently, as it is illustrated in the equivalent circuits of **Fig. 3.3(a)** and **Fig. 3.3(b)**.

3.1.1 Steady-state analysis

Considering the previous derived equations, resulted from the converter voltages and currents analysis, this section focuses on the energy transfer mechanisms between converter ports, branches and SMs.

Let consider the simplified case where the converter is in steady-state and $v_{no} = 0$, then the expressions (3.9) and (3.10) simplify to $v_{c1} = \frac{V_{DC}}{2}$ and $v_{s1} = v_{g1}$, respectively. By retrieving the linear transformations (3.7) and (3.8), the branches voltage and current can be written as

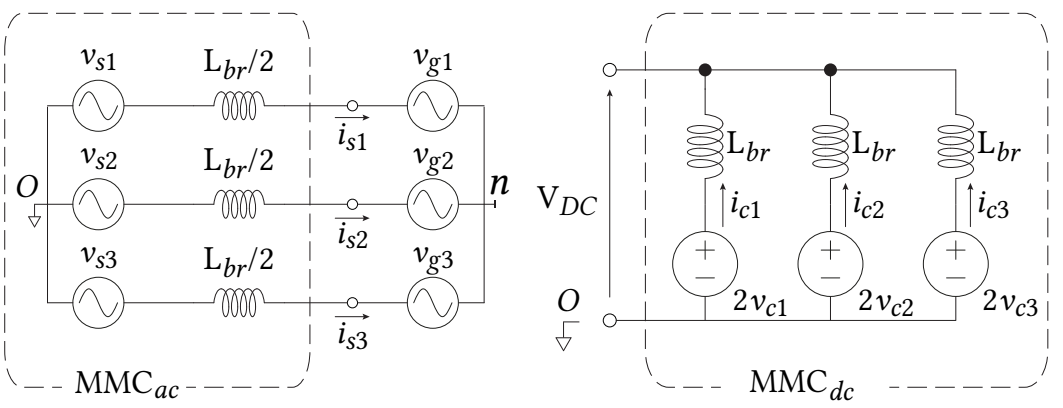


Fig. 3.3 (a) represents the MMC equivalent ac circuit. It is recognized that the converter behaves as a controllable three-phase source with half of the branch inductance connected to the three-phase grid. (b) represents the MMC equivalent dc circuit, where the converter dc port output is the parallel connection of three dc sources with series inductance L_{br}.

$$v_{p1} = \frac{V_{DC}}{2} - v_{s1} \tag{3.11}$$

$$v_{n1} = \frac{V_{DC}}{2} + v_{s1} \tag{3.12}$$

$$i_{p1} = \frac{I_{DC}}{3} + \frac{i_{s1}}{2} + i_{circ1} \tag{3.13}$$

$$i_{n1} = \frac{I_{DC}}{3} - \frac{i_{s1}}{2} + i_{circ1} \tag{3.14}$$

Previous expressions show that both branches within the leg 1 can provide simultaneously ac and dc voltage and current components. Similar result is found for the legs 2 and 3. Evidently, the magnitude of these components are bounded by the capacities and limitations of the SMs as they synthesize the branch voltage using their dc-link. This can observed better by deriving the maximum ac and dc voltage components that a branch can produce. Let consider N FB SMs within a branch, with dc-link voltages $v^{dc}_{sm_{i=1..N}}$ then, ideally, the branch equivalent dc voltage is the sum of the SM dc-link voltages $\sum_i^N v^{dc}_{sm_i}$. Consequently, one branch can produce a maximum dc component $\pm\sum_i^N v^{dc}_{sm_i}$ while the ac component is zero and, vice versa, the magnitude of the ac component is maximum when the dc component is zero. In addition, both components ($\hat{v}_{c1}$ and $\hat{v}_{s1}$) get their maximum when $\hat{v}_{c1} = \frac{\sum_i^N v^{dc}_{sm_i}}{2}$ and $\hat{v}_{s1} = \frac{\sum_i^N v^{dc}_{sm_i}}{2}$. Since both, positive and negative branches have to operate simultaneously, it can be deduced that the maximum converter dc terminals output is $\sum_i^N v^{dc}_{sm_i}$ and the maximum converter ac phase-voltage magnitude is $\frac{\sum_i^N v^{dc}_{sm_i}}{2}$ (cf. 3.7). Similar analysis can be done in the case of HB SMs. Both analyses are illustrated in **Fig. 3.4**. Additional details about how the SM synthesizes terminal voltage is provided later in this chapter. Please note that the hat symbol $\hat{x}$ represents the magnitude of x.

Having defined an expression for the branch voltage and current, let us turn to derive an expression for its energy in terms of its evolution between branches and within a leg (as energy analysis might be more intuitive in that form).

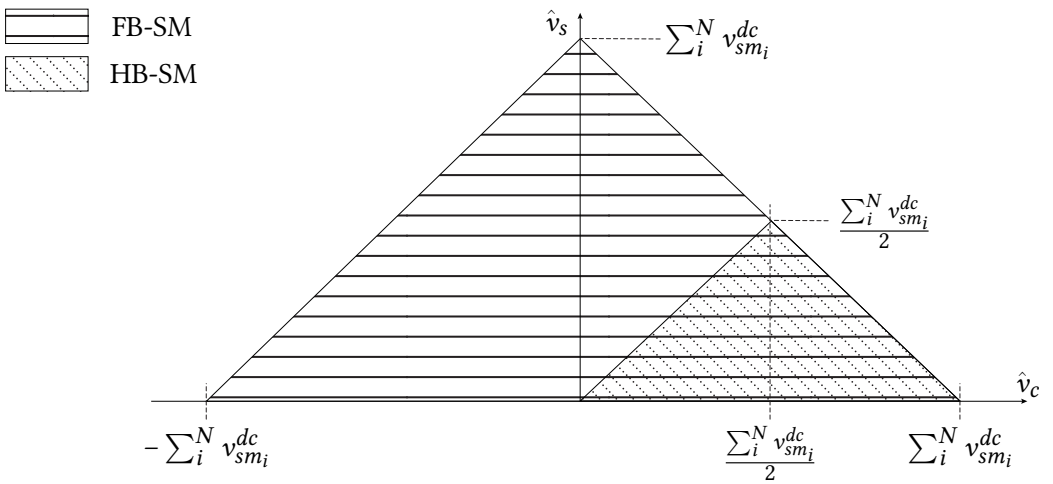


Fig. 3.4 Comparison of the branch voltage generation boundaries for the HB and FB SM.

One can define the total leg 1 energy $W_{\Sigma 1}$ and the differential leg 1 energy $W_{\Delta 1}$ as:

$$W_{\Sigma 1} \equiv \Delta W_{p1} + \Delta W_{n1} = \int_{t=0}^{T} P_{p1}(t)dt + \int_{t=0}^{T} P_{n1}(t)dt \tag{3.15}$$

$$W_{\Delta 1} \equiv \Delta W_{p1} - \Delta W_{n1} = \int_{t=0}^{T} P_{p1}(t)dt - \int_{t=0}^{T} P_{n1}(t)dt \tag{3.16}$$

Where p_{p1} (calculated multiplying (3.11) and (3.13)) and p_{n1} (calculated multiplying (3.12) and (3.14)) are the positive (upper) and negative (lower) branch power, respectively; and T is a fundamental period. Assuming that the three-phase voltage and current of the ac grid at which the converter is connected are balanced and without distortion, then v_{s1} can be considered pure sinusoidal of magnitude $\hat{v}_{s1}$ and angular frequency ω (system angular frequency) as in (3.17). On the other hand, by considering a three-phase balanced and without distortion current flowing between the converter ac port and the ac grid, then, in particular, i_{s1} can be expressed as (3.18), where φ is the phase-shift between v_{s1} and i_{s1}. It is important to note that this angle can take any value.

$$v_{s1} = \hat{v}_{s1} cos(\omega t) \tag{3.17}$$

$$i_{s1} = \hat{i}_{s1} cos(\omega t - \varphi) \tag{3.18}$$

Then, the time evolution of the total and differential leg energy is

$$\frac{dW_{\Sigma 1}}{dt} = P_{p1} + P_{n1} = \underbrace{\frac{V_{DC} I_{DC}}{3} - \frac{\hat{v}_{s1}\hat{i}_{s1}}{2}\cos(\varphi)}_{\text{dc component}} - \underbrace{\frac{\hat{v}_{s1}\hat{i}_{s1}}{2}\cos(2\omega t - \varphi)}_{\text{second-harmonic component}} + V_{DC} i_{circ1} \tag{3.19}$$

$$\frac{dW_{\Delta 1}}{dt} = P_{p1} - P_{n1} = \underbrace{\frac{V_{DC}\hat{i}_{s1}}{2}\cos(\omega t - \varphi) - \frac{2}{3} I_{DC}\hat{v}_{s1}\cos(\omega t)}_{\text{fundamental component}} - 2\hat{v}_{s1}\cos(\omega t) i_{circ1} \tag{3.20}$$

Please note that terms $V_{DC} i_{circ1}$ in (3.19) and $2\hat{v}_{s1}\cos(\omega t) i_{circ1}$ in (3.20) are described in detail later in this section. For now, let assume the circulating current i_{circ1} is zero. Then, the dc component of (3.19) might be positive or negative, thus to avoid the energy storage elements being over-discharged or over-charged, the mean value of (3.19) within a fundamental period must be controlled to zero. In the analyzed case, the zero mean value of (3.19) retrieves the power balance equation between the ac and dc port of the converter (3.21), and a constant term $W_{\Sigma 1}^{0}$ (a constant term resulted from the integration 3.19), which represents the initial o previous amount of energy stored in the leg SM capacitors, the only meaning of energy storage in the converter. $W_{\Sigma 1}^{0}$ can take any positive value; however, in practical applications, this value is chosen as the nominal energy stored in a leg or, in other words, a third of the nominal total stored energy in the converter (the same conclusion can be deduced for legs 2 and 3).

$$\frac{V_{DC}I_{DC}}{3} = \frac{\hat{v}_{s1}\hat{i}_{s1}}{2}\cos(\varphi) \tag{3.21}$$

The fundamental component in (3.20) and the second-harmonic term in (3.19) show the inherent power oscillation within the leg 1 due to the interaction between the ac and dc ports. It is important to note that the magnitude of the oscillating energy components has to be stored/delivered by the branch SM capacitors within a fundamental period, directly impacting its size and cost. This relationship will be covered in more detail later in this chapter.

Up to this point, the main equations governing the MMC and the natural mechanisms in which the energy is transferred between the ac and dc ports have been presented. Furthermore, it was concluded that the primary condition so that the SMs can operate adequately is that the total energy stored within the converter has to be kept stable accordingly to the storage technical limitations by achieving power balance between the converter ac and dc ports. However, it is not difficult to notice that the total energy stored in the converter might be unevenly distributed among legs, branches and SMs due to the inherent impedance differences between them. In addition, the oscillating energy components derived in (3.19) and (3.20) produce extra power losses [115] and higher SM capacitor voltage/capacitance requirements, especially at low frequency as it has been pointed out in [116] and illustrated later in this chapter. In technical literature, it is commonly found that some of these issues are addressed through the mitigation, elimination or manipulation of the circulating currents, omitted in the previous analysis. For instance, some authors have proposed methods for circulating current suppression [117], [118] in order to reduce converter losses and improve SM capacitor voltage stabilization. Other authors have proposed the circulating current optimization to mitigate/shape the branch energy oscillations to a certain extent to reduce the SM capacitance requirement, thus reducing capacitors' size and cost [119]–[121]. Authors in [115], [122] proposed that circulating current can be used to achieve the internal energy balancing of the converter, i.e energy balancing between branches within a leg and between legs. This last strategy is considered in this work and used for MMC simulations and experimental results validation, so its main principle is presented hereafter.

The internal energy balancing is based on the idea that even though the dc component in (3.19) could be controlled to zero so that $W_{\Sigma 1} = W_{\Sigma 1}^{0}$ and, in average, the oscillating components of (3.19) and (3.20) do not contribute to the energy unbalance, small energy re-balancing action between legs and between branches might be required due their inherent impedance differences. Let consider that the circulating current can be freely chosen (as no particular restriction has been imposed to it so far), in particular, it can be expressed as (3.22), where $\bar{i}_{circ1}$ and $\tilde{i}_{circ1}$ are the magnitude of its dc and ac component, respectively, and θ its phase-shift angle chosen to be in phase with v_{s1}, so $\theta = 0$. Then, the mean value of (3.19) and (3.20) results in (3.23) and (3.24).

$$i_{circ1} = \bar{i}_{circ1} + \tilde{i}_{circ1}\cos(\omega t - \theta) \tag{3.22}$$

$$\frac{d\overline{W}_{\Sigma 1}}{dt} = V_{DC}\bar{i}_{circ1} \tag{3.23}$$

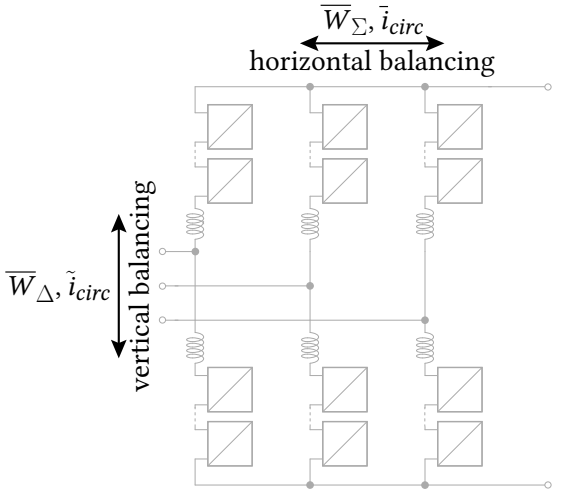


Fig. 3.5 MMC vertical and horizontal energy balancing action of circulating currents. The magnitude of the ac component of the circulating current is proportional to the differential leg energy and can be controlled to exchange energy between branches withing a leg. The the dc component of the circulating current is proportional to the total leg energy and can be controlled to exchange energy between legs. To avoid any disturbance of the circulating currents in the dc ports terminals, it is required that $i_{circ1} + i_{circ2} + i_{circ3} = 0$.

$$\frac{d\overline{W}_{\Delta 1}}{dt} = -\hat{v}_{s1}\tilde{i}_{circ1} \tag{3.24}$$

From expressions (3.23) and (3.24), it can be concluded that only by means of controlling the circulating current, both the total and differential leg energy can be manipulated to perform energy balancing correction actions. As it is shown in **Fig. 3.5**, while the dc component of the circulating current achieves energy transfer within the converter dc port, commonly known as horizontal energy balancing, the ac component allows energy transfer within the leg, commonly known as vertical energy balancing. Finally, it is important to stress that to maintain the circulating current of each leg within the converter (not seen by the converter dc port terminals), it is necessary that the three circulating currents sum zero. This condition is achieved by the proper circulating current reference selection and control, as it has been proposed in [123], [124] and [125].

Despite the details about MMC control strategy are beyond the scope of this thesis, **Fig. 3.6** presents a overview of the control layers commonly used in the considered converter. **Fig. 3.6**, shows five main control blocks, divided in two main levels:

- Higher-level control
  - ac port control, that achieves power exchange with the grid, and
  - dc port control, that achieves power exchange with the dc port through dc current or voltage control.
- Internal MMC control
  - total energy control, used to keep the energy balance between the ac port, dc port and the converter,

– internal energy control, to perform the horizontal and vertical energy distribution among branches and legs,

– circulating control, used for energy balancing actions.

For the MMC operating as a rectifier, the main goal of the control strategy is to deliver the desired dc power and voltage while the converter operates within its limits and does not affect the grid power quality. Firstly, the higher-level control contains the ac port control which internal structure is the well-known synchronous reference frame (SRF) current control, and the dc port control performs the actions to deliver the required dc voltage or current. The second level, the internal MMC control, contains all the control loops to assure constant converter total energy, i.e., the power balance between the ac and dc port, and the horizontal and vertical energy balancing actions to keep the legs and branches energy within the desired levels. The total energy block outputs the ac port control block reference so that the required ac active power P^*_{AC} equals the dc port output power P^*_{DC} plus the power to maintain the MMC total energy $E^*_{MMC} \approx q\left(\frac{C}{2}\sum_i^N {v^{dc*}_{sm_i}}^2\right)$, where q is the number of branches. The internal energy control block outputs the circulating current references so that $\overline{W}^*_{\Sigma\{1,2,3\}} = \frac{E^*_{MMC}}{3}$ and $\overline{W}^*_{\Delta\{1,2,3\}} = 0$. Then, the circulating current control is achieved utilizing a proportional integral (PI) regulator for the dc component and a proportional resonant (PR) regulator for the ac component, in the circulating current control block. The calculated control actions for the ac port, dc port and circulating current control block are used to retrieve the voltage references for each branch. Finally, the modulation technique adopted in this work is the phase-shifted carrier PWM (PS-PWM), introduced in [126] which details are omitted as they are out of the scope of this thesis.

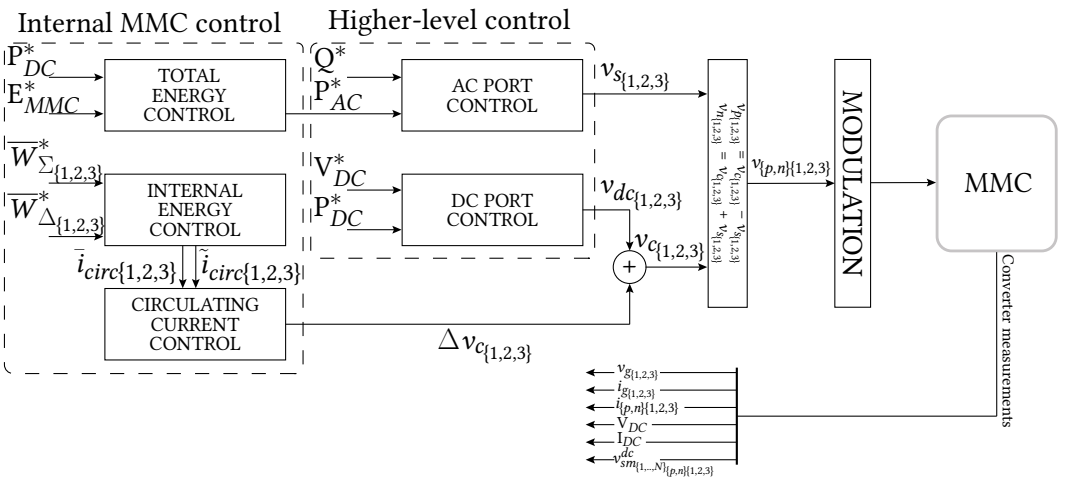


Fig. 3.6 Rectifier MMC control scheme overview and required measurements at the converter level. Two main levels are highlighted, the higher-level control, related to the converter ac and dc port control, and the internal MMC control, which covers the converter total and internal energy, and the circulating current regulation.

3.2 MMC research platform description

3.2.1 Overview

A multipurpose MMC research platform based on the classic ac-dc MMC topology and FB SMs, depicted in **Fig. 3.1**, was envisioned and built for the PEL research-related topic activities. In this section, a description of the MMC research platform is presented with particular emphasis on the SM's main characteristics and functionalities.

The MMC research platform is a PEL development made of two 250 kVA MMCs. Each converter comprises 48 FB SMs with rated voltage of 650 V and 73 A nominal current, allowing operation at 3.3 kV phase-voltage in the ac port and ±5 kV in the dc port. By re-configuring the dc port connections enables combined operation: 3.3 kV/3.3 kV ac-ac conversion in a back-to-back configuration, 500 kVA 3.3 kV/±10 kV ac-dc rectifier/inverter or 500 kVA 3.3 kV/±5 kV ac-dc rectifier/inverter. In any case, the ac side of the converters are interfaced to the grid by a twelve pulse transformer with star-delta secondary windings, as it is shown in **Fig. 3.7**.

As it is depicted in **Fig. 3.8**, the branches are made of 8 SMs in series connection while the legs are formed using two coupled air-core inductors rated at 2.5 mH. Each converter has an ABB AC 800PEC controller, where the converter-level control strategy, protection and monitoring are performed. The ABB power electronics controller measurement interface (PEC-MI) acquires converter-level measurements such as grid voltage ($v_{g\{1,2,3\}}$), grid current ($i_{s\{1,2,3\}}$), and dc port voltage (V_{DC}) and current (I_{DC}), while the ABB combined input-output (COMBI-IO) is in charge of operate relays, switches and other user-defined auxiliary signals. Both devices communicate with the controller employing a proprietary protocol through fibre optic link (FOL). On the other hand, the Control Hub unit handles the communication between the controller and each SM using a FOL and universal asynchronous receiver-transmitter (UART)-based protocol to exchange SM status signals, operating reference, parameter values, PWM synchronization signals, and local measurements. This configuration allows the controller to send/receive information to each SM every 25 µs. Another AC 800PEC unit works as a master controller (subordinating the AC 800PEC of each converter) to handle general (application)

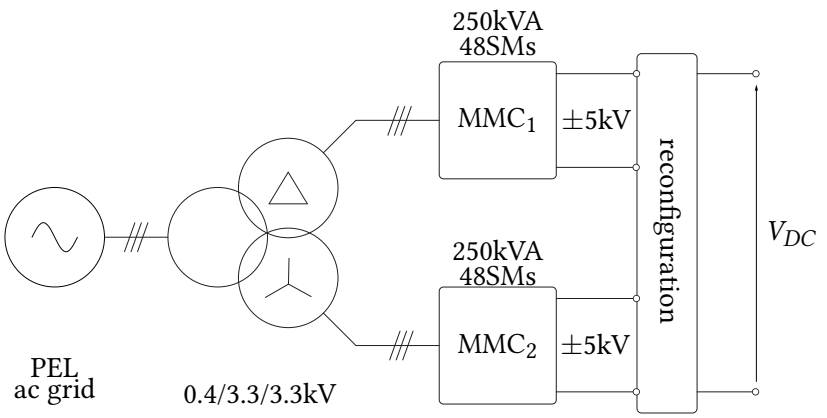


Fig. 3.7 MMC research platform scheme. Two 250 kV A three-phase ac-dc MMCs are interfaced to the PEL ac grid by a twelve pulse transformer with star-delta secondary windings. The ac port of each unit is rated to 3.3 kV phase-voltage while each dc port is rated to ±5 kV. Each converter is made of 48 FB SMs, rated at 73 A, 650 V.

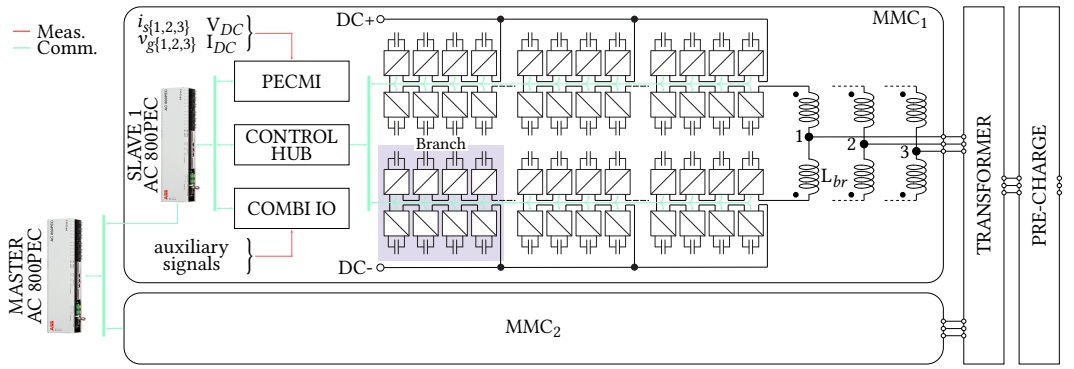


Fig. 3.8 MMC research platform scheme, detailing control, measurement and communication units. Each converter possess the industrial-level controller unit ABB AC 80oPEC, which performs the control strategies depicted in **Fig. 3.6**. The PEC-MI acquires all the converter-level measurements and transmits them to the controller unit. The COMBI-IO handles all the auxiliary signals. The control hub manages the communication between the controller and each SM. Finally, a third AC 80oPEC works as a master unit monitoring and setting the references for each MMC controller unit (slave).

state machine and references for each MMC. Finally, it is important to mention that a pre-charge system connected between the PEL ac grid and the MMC research platform transformer allows to passively charge each SM dc-link enough to power up their local controllers and be ready to start the active charge process in which each SM gets a nominal charge (additional details about MMC start-up are provided in the following section). Main electric parameters of the converters are summarized in **Tab. 3.1**.

Tab. 3.1 Single MMC characteristics

Parameter	Symbol	Value
Rated power	S	250 kV A
Grid voltage	v_g	3.3 kV
Fundamental frequency	f	50 Hz
Branch inductance	L_{br}	2.5 mH
Max. output voltage	V_{DC}	5 kV
Number of SMs per branch	N	8

3.2.2 SM description

The SM is the basic building block of the MMC and can be found in a variety of configurations [127], however, the HB and FB SMs are the most commonly used due to their simplicity. In this work, the FB SM is preferred over the HB as it can produce more levels and negative voltage at its terminals. In the following part of this section, the developed PEL SM is presented, highlighting technical choices, electrical and mechanical characteristics as well as main functionalities.

In its basic form, the FB SM is composed of four semiconductor power switches, forming an H-bridge topology and an energy storage component, commonly a capacitor (or an array of them forming a bank), as it is depicted in **Fig. 3.9**. The technological choice of these components depends of different factors such as the application, voltage/current rating, switching frequency, cost, volume,

Tab. 3.2 FB SM switch states, possible output and capacitor status.

S1	S2	S3	S4	v_{sm}	$i_{p1} > 0$	$i_{p1} \leq 0$	SM (capacitor) status
0	0	0	0	$sgn(i_{p1})v_{sm}^{dc}$	$v_{sm}^{dc} \uparrow$	$v_{sm}^{dc} \uparrow$	IDLE (passive charge)
1	0	0	1	v_{sm}^{dc}	$v_{sm}^{dc} \downarrow$	$v_{sm}^{dc} \uparrow$	INSERTED (active charge/discharge)
0	1	1	0	$-v_{sm}^{dc}$	$v_{sm}^{dc} \uparrow$	$v_{sm}^{dc} \downarrow$	INSERTED (active charge/discharge)
1	0	1	0	0	$v_{sm}^{dc} \approx$	$v_{sm}^{dc} \approx$	BYPASSED (passive discharge)
0	1	0	1	0	$v_{sm}^{dc} \approx$	$v_{sm}^{dc} \approx$	BYPASSED (passive discharge)
1	1	0	0				
0	0	1	1		forbidden		
1	1	1	1				

↑:charge, ↓:discharge , ≈:no change, *sgn* :sign function

availability, among others. However, in this project the selected semiconductor device is IGBTs, while the electrolytic capacitors are selected.

When the semiconductor devices or switches are ”on” or ”closed” it is denoted by a logic ”1”, whereas ”off” or ”open” is denoted by logic ”0”. Thus, the FB SM can be found in only eight admissible states since the switches forming a terminal have to operate in complementary mode, i.e., when the switch S1 is 1, S2 must be 0, and when S3 is 1, S4 must be 0. The SM switch states are presented in **Tab. 3.2**.

According to the above possible states, the SM can be inserted, bypassed or idle. The inserted state refers to the SM voltage terminals and the current flow are consequence of the active action of the power switches. The bypass state means that the SM output voltage is zero and the SM capacitor is passively discharged by internal losses (or any other load connected to it) and connected loads such as the ASPS. The idle state refers to the SM output voltage determined by the direction of the observed terminal current, producing the SM capacitor to be charged by the free-wheeling diodes acting as a passive rectifier.

It is important to highlight that unipolar PWM scheme [128] is adopted in this work and occurs locally in the SM driven by a local digital controller.

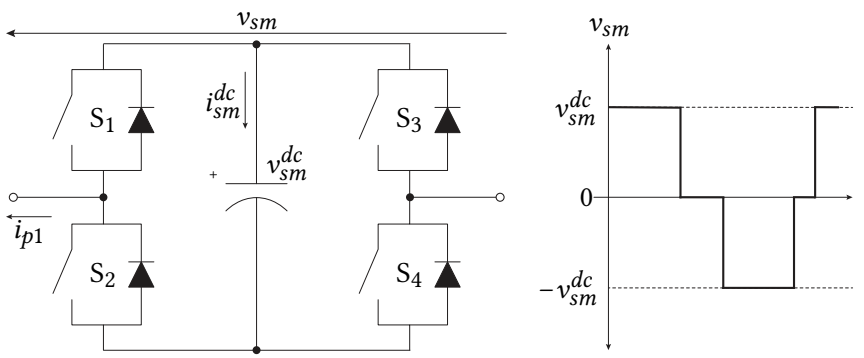


Fig. 3.9 Left: FB SM electrical scheme. Right: the three-level feasible output voltage. When no voltage drop is considered, the SM can be either $v_{sm} = \pm v_{sm}^{dc}$ or $v_{sm} = 0$. S_x is the set $IGBT_x$ and corresponding freewheeling diode, where $x = \{1, 2, 3, 4\}$

Tab. 3.3 H-bridge module selected

Parameter	Value	Unit
IGBT		
V_{ces}	1200	V
I_c @ T_j =175 °C	73	A
$Rth_{(j-s)}$	0.55	K W^{-1}
DIODE		
V_f @ I_f = 75 A, T_j =150 °C	2.1	V
$Rth_{(j-s)}$	0.75	K W^{-1}

3.2.2.1 Power semiconductors

The power semiconductors are actively responsible for the power transfer between the SM capacitor and its terminals. Their selection depends mainly on the voltage, current, and thermal capability matching the operating conditions in the converter. In addition, other considerations such as dimension, terminals connection, cost, and market availability also play an important role in determining the best power device. In some practical applications, power semiconductors are used in the form of a module to provide electrical connection between one or more devices and the circuit, reducing cost and size. A standard IGBT module comprises a direct cooper bonded substrate soldered to a base plate. The substrate provides insulation between power components and cooling system and contains cooper tracks to conduct the current and connect IGBTs and diodes. Bond wires commonly connect IGBT chips to the substrate and substrate to module terminals. Finally, all these elements are covered by silicone gel or epoxy resin for protection and insulation [129]. Bond wire fatigue is one of the common failure mechanisms in power IGBT modules. The presence of elements with various coefficients of thermal expansion, heat sources due to semiconductor losses during operation (switching and conducting), and ambient conditions produce thermomechanical stress in bond wires, leading to bond wire lift-off or crack failures [77]. Similarly, solder joint fatigue is another dominant failure mechanism. IGBT to substrate and substrate to base-plate solders are degraded due to the coefficient of thermal expansion mismatch between the two materials and temperature variations, producing solder cracks, delamination, and voids. Both failure modes might lead to module malfunction, wear-out, or accelerate other failure modes. The following part of this section demonstrates that the H-bridge IGBT-based SEMIKRON module SKiiP26GH12T4V11, which main characteristics are presented in **Tab. 3.3**, fits the designed SM, and no voltage, current or thermal limits are exceeded.

The first part of this analysis starts considering that the current flowing through the IGBTs of a SM within a branch is the branch current (3.13) (positive branch current of the leg 1) following the possible paths described in **Tab. 3.2**. Assuming the converter line current as in (3.18), the branch current can be expressed as (3.25), which is illustrated in **Fig. 3.10** for different phase-shift angles, and considering the converter operating at rated values and zero circulating current.

$$i_{p1} = \frac{I_{DC}}{3} + \frac{\hat{i}_{s1}}{2}\cos\left(\omega t - \varphi\right) + i_{circ1} \tag{3.25}$$

A maximum SM terminal current of 47.6 A is achieved at φ =0°, demonstrating that selected module

(cf. **Tab. 3.3**) is a good choice. In addition, it is noted that at least 30% of current limit is available for the circulating current during energy balancing correction actions.

The open question now is to assess that power semiconductors' thermal limit will not be exceeded during expected operation. A simple manner is to verify that power switches (IGBTs and diodes) junction temperature T_j is limited to below 150 °C or 175 °C, depending on the manufacturer recommendation, using an IGBT module thermal model fed by semiconductors power losses.

Semiconductor power losses are calculated considering the commutation process (switching losses) and the conduction period (conduction losses) [130]. Mathematically, the set IGBT + diode power losses are expressed as

$$P_{losses} = \underbrace{\frac{1}{T}\int_0^T \left(v_{CE(sat)} i_{CE} + v_F i_F\right) dt}_{\text{IGBT+diode conduction losses}} + \underbrace{(E_{on} + E_{off} + E_{rr}) \frac{v_{sm}^{dc}}{v_{CE}^{ref}} f_{sw}}_{\text{IGBT+diode switching losses}} \tag{3.26}$$

where $v_{CE_{sat}}$ and i_{CE} are the IGBT collector-emitter voltage and current during conduction, respectively; v_F and i_F are the diode forward voltage and current, respectively; T is the fundamental period; E_{on} and E_{off} are the IGBT energy loss during the turn-on and turn-off, respectively; E_{rr} is the diode energy loss during the turn-off; v_{CE}^{ref} is the IGBT collector-emitter voltage at which the switching energy losses were defined. Then, the SM power losses can be calculated as:

$$P_{losses}^{SM} = P_{losses}^{S_1} + P_{losses}^{S_2} + P_{losses}^{S_3} + P_{losses}^{S_4} \tag{3.27}$$

A classical approach for thermal modeling is the use of a Cauer model in steady-state, as it is presented in **Fig. 3.11**.

In practice, junction temperature might differ among the devices as power losses and thermal resistors differ; thus, a conservative thermal criterion during thermal analysis it to consider the maximum junction temperature among them. Another approach derives from the fact that commonly IGBT manufacturers provide a thermal-resistor embedded in the module so that a reference temperature T_s (representative of the devices' junction temperature) can be measured and used, for instance, for

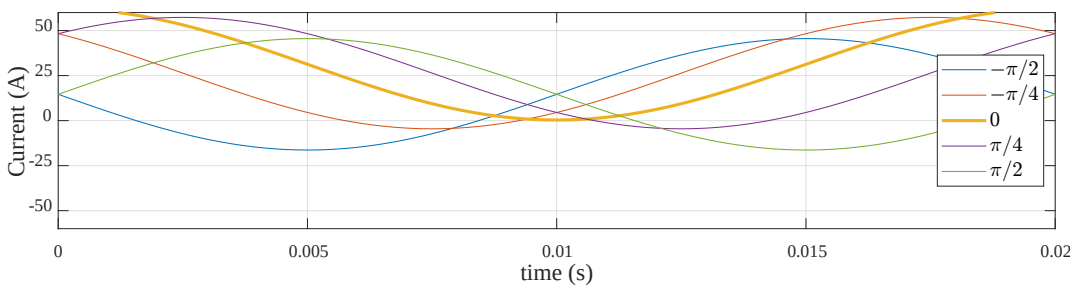


Fig. 3.10 MMC positive branch current (or equivalently SM terminals current) for different current phase-shift angles. A maximum current of 47.6 A is achieved at φ =0°.

thermal protection. In addition, manufacturers provide module thermal limit with respect to T_s, which significantly simplifies the thermal assessment when total power losses are known. In the case of the studied module, the manufacturer recommends $T_s \leq 150°C$ and $T_s \leq 70°C$ to operate up to 50 A and 70 A collector-emitter current, respectively. From **Fig. 3.11**, T_s is easily calculated using the expression (3.28).

$$T_s = Rth_{s-a} P_{losses}^{SM} + T_a \tag{3.28}$$

Where Rth_{s-a} counts for the thermal resistance of all the thermal interfaces between the thermal-resistor and the ambient, and T_a is the ambient or room temperature. In this work, the Fischer Elektronik SK135 aluminum heatsink is considered as the only interface between the thermal-resistor and the ambient, with a thermal resistance of $Rth_{s-a} = 0.65\,\mathrm{K/W}$. A PLECS simulation considering the parameters of the IGBT module, the converter operation, and expressions (3.26), (3.27) and (3.28) resulted in the plot of **Fig. 3.12**.

With the converter operating at nominal voltage and $\varphi = 0°$, different SM operating currents were studied to estimate module power losses and resulting temperature T_s. At $i_{p1} = 47.6\,\mathrm{A}$, no extra effort has to be done to dissipate the module heat as it operates under manufacturer recommendation ($T_s \approx 123\,°\mathrm{C}$ and $T_j^{max} \approx 149\,°\mathrm{C}$). Conversely, if module nominal current is required, Rth_{s-a} has to be decreased to $0.1\,\mathrm{K/W}$, which can be achieved by adding a forced-air cooling system. The conservative decision is to install a $1865\,\mathrm{m^3\,h^{-1}}$ fan per branch so that each SM can dissipate its losses under any circumstances.

3.2.2.2 Power capacitors

The SM capacitors are the main energy storage component required to mitigate any energy fluctuations between converter dc and ac ports. Depending on the converter topology, technical characteristics, operating point and environmental conditions, SM capacitor capacitance, voltage rating, and technology among other characteristics can be found. Typically in power electronics applications, three

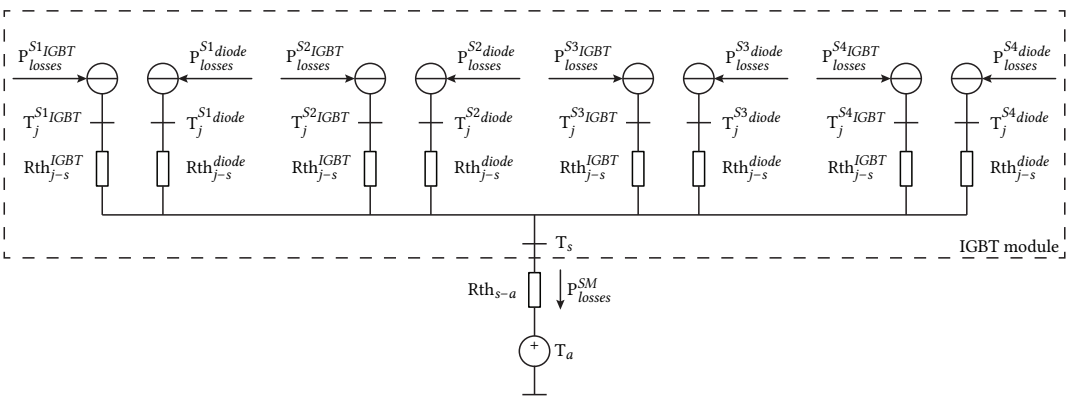


Fig. 3.11 Considered thermal model of the IGBT module. The diagram represents the main thermal components in the module. Each power switch is composed of an IGBT and a diode. The heat produced by the IGBT and diode power losses is transmitted to the module case through the thermal resistance Rth_{j-s}^{IGBT} and Rth_{j-s}^{diode}, respectively. Then, the heat is transferred to the ambient through the thermal resistance Rth_{s-a}. The ambient temperature T_a is considered constant.

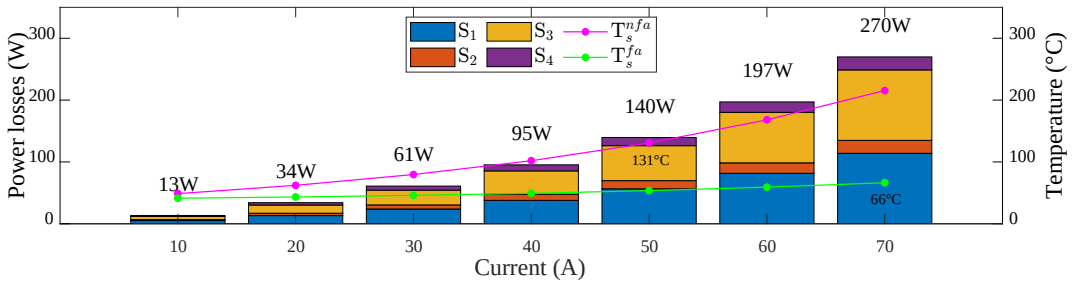


Fig. 3.12 Module power losses estimation for different operating peak current at $\varphi = 0°$. In addition, T_s estimation is presented considering the module heatsink with forced-air cooling system (T_s^{fa}) and without (T_s^{nfa}). The SM to operate at the required 47.6 A almost no forced-air cooling system is required ($T_s^{nfa} = 123\,°C$ @ 47.6 A and $T_s^{nfa} = 131\,°C$ @ 50 A), however to operate at 70 A (module nominal current, $T_s^{nfa} = 200\,°C$, $T_s^{fa} = 66\,°C$) forced-air must flow so that the thermal resistance Rth_{s-a} has to decrease to 0.1 K/W.

types of capacitor technologies are used: Al-cap, MPPF-cap and MLC-cap. Despite in MV and HV MMC applications the MPPF-caps are largely preferred [131], [132], in this work it is considered the Al-cap technology due cost and volume restrictions.

From the leg total and differential energy expression found in (3.19) and (3.20) it was stated that in steady state, an arbitrary amount of energy $W_{\Sigma 1}^0$ has to be stored in the leg capacitors. In addition, a first and second harmonic energy components oscillate between branches within a leg and between legs, respectively, whose magnitudes depend of converter operating point, having an effect on capacitors voltage and current ripple. Thus, proper SM capacitor sizing is fundamental so the converter can operate as required and capacitors can operate within their technical limits avoiding premature catastrophic or wear out failures. Several publications have dealt with MMC capacitor sizing using different mathematical expressions and assumptions. There is a general agreement that the converter required stored energy is approximately 45 kJ/MVA with a voltage ripple factor $\epsilon_{vrf} = 10\%$, which is mostly true when neither common mode voltage and circulating current are considered, representing the worst case scenario besides transient or anomalous operation [133]–[136]. A simple approach to capacitor sizing is to deduce SM dc-link voltage and current expressions so that capacitance can be found as a function of converter operating conditions and ripple requirements. The analysis starts assuming zero power losses within a SM during a fundamental period so that ac and dc power are equal, condition expressed as (3.29).

$$v_{sm} i_{sm} = v_{sm}^{dc} i_{sm}^{dc} \tag{3.29}$$

Then, considering N SMs within a branch, and adding both sides of the previous equation, it turns in

$$\sum_{i=1}^{N} \left(v_{sm_i} i_{sm_i} \right) = \sum_{i=1}^{N} \left(v_{sm_i}^{dc} i_{sm_i}^{dc} \right) \tag{3.30}$$

As the SMs are series connected, their terminal current i_{sm} equals the branch current i_{p1}. On the other hand, if it is assumed that the branch power is equally distributed among the SMs, then $\sum_{i=1}^{N} \left(v_{sm_i}^{dc} i_{sm_i}^{dc} \right) = N v_{sm}^{dc} i_{sm}^{dc}$, yielding

$$i_{p1}\sum_{i=1}^{N} v_{sm_i} = N v_{sm}^{dc} i_{sm}^{dc} \tag{3.31}$$

Expression (3.31) can be rewritten as (3.32), considering that Nv_{sm}^{dc} can be approximated by V_{DC}, and using (3.11) and (3.13) for branch power p_{p1}.

$$\frac{i_{p1}v_{p1}}{V_{DC}} = \frac{p_{p1}}{V_{DC}} = i_{sm}^{dc} = \frac{I_{DC}}{6} - \frac{\hat{v}_{s1}\hat{i}_{s1}}{4V_{DC}}\cos\varphi + \frac{\hat{i}_{s1}}{4}\cos\big(\omega t-\varphi\big) - \frac{I_{DC}\hat{v}_{s1}}{3V_{DC}}\cos(\omega t) - \frac{\hat{v}_{s1}\hat{i}_{s1}}{4V_{DC}}\cos\big(2\omega t-\varphi\big) \tag{3.32}$$

Then, using ideal capacitor equation (3.33), it is obtained (3.34).

$$v_{sm}^{dc} = \frac{1}{C}\int_0^t i_{sm}^{dc}dt \tag{3.33}$$

$$v_{sm}^{dc} = \frac{1}{C}\left(\frac{\hat{i}_{s1}}{4\omega}\sin\big(\omega t-\varphi\big) - \frac{\hat{v}_{s1}I_{DC}}{3\omega V_{DC}}\sin(\omega t) + \frac{\hat{v}_{s1}\hat{i}_{s1}}{8\omega V_{DC}}\sin\big(2\omega t-\varphi\big)\right) + v_{sm0}^{dc} \tag{3.34}$$

Where C is the SM capacitance and v_{sm0}^{dc} is the SM dc-link initial voltage. Please note that previous expressions were found considering both zero common mode voltage and zero circulating currents, power balance between converter ports and no ESR (first order approximation). Finally, to retrieve the capacitance requirement, it is considered that during a fundamental period T, v_{sm0}^{dc} is the SM dc-link mean voltage so that $v_{sm}^{dc} = (1+\epsilon_{vrf})v_{sm0}^{dc}$, with $\epsilon_{vrf} \in (0,1)$, thus

$$C_{min} \geq \max\left(\left|\frac{\frac{\hat{i}_s}{4\omega}\sin\big(\omega t-\varphi\big) - \frac{\hat{v}_s I_{DC}}{3\omega V_{DC}}\sin(\omega t) + \frac{\hat{v}_s\hat{i}_s}{8\omega V_{DC}}\sin\big(2\omega t-\varphi\big)}{\epsilon_{vrf}v_{sm0}^{dc}}\right|\right) \tag{3.35}$$

Fig. 3.13 presents the SM minimum required capacitance with respect to converter phase-shift, so that desired voltage ripple factor is met. The cases ϵ_{vrf5} in which $\epsilon_{vrf} = 5\%$ and ϵ_{vrf10} in which $\epsilon_{vrf} = 10\%$, and converter nominal operation were considered.

Fig. 3.14 shows SM estimated current ripple for different power factors and nominal operation of the converter. From (3.32) it can be noted that current ripple does not depend on capacitance, but converter input/output voltage, power factor and power levels. It is found that maximum ripple current (circulating in the SM dc-link) is 20.6 A.

A conservative design strategy is to select the maximum value of the case ϵ_{vrf5}, i.e., $C_{\epsilon_{vrf5}}$ =1.92 mF and a minimum of 15% extra capacitance margin to take into account modeling simplifications and transients during operation. Accordingly, it was chosen the Al-cap A714272 from Exxelia which main characteristics are listed in **Tab. 3.4**. Using this selection, the SM dc-link is made of six units configured 2s3p (three groups in parallel of two series connected capacitors) as it is shown in **Fig. 3.15**,

Tab. 3.4 Chosen SM capacitor (single unit) characteristics

Characteristic	Value	Unit
Part number	A714272	-
Capacitance	1500	µF
Voltage (rated/peak)	400/450	V
Current ripple @100 Hz, 40 °C	12	A
ESR @100 Hz, 20 °C	100	mΩ
Dimension (diam/height)	40/75	mm

Tab. 3.5 SM capacitor (bank) characteristics

	Value	Unit
Capacitance	2.25	mF
Voltage (rated/peak/max)	650/800/900	V
Max. current ripple @100 Hz, 40 °C	36	A
ESR @100 Hz, 20 °C	66.7	mΩ

and achieved the parameters presented in **Tab. 3.5**. In addition, **Fig. 3.15** shows the scheme of the active balancing circuit in charge of keeping voltage distribution between series connected capacitors.

Fig. 3.16 presents the SM dc-link voltage simulated for different converter power factor and capacitance. **Fig. 3.16(a)** is the simulation results with the chosen capacitance, resulting a voltage

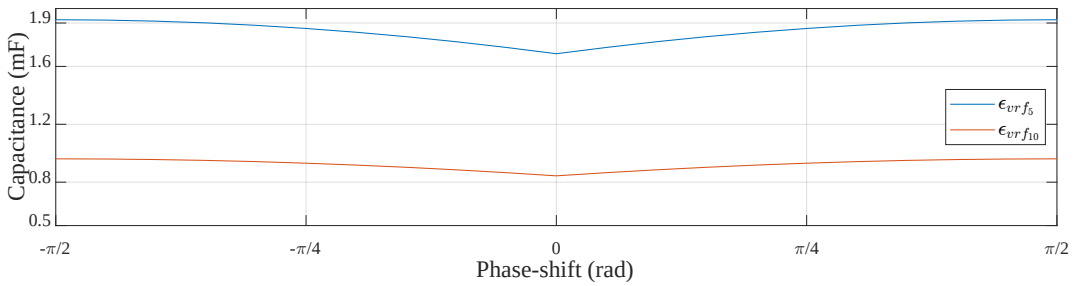


Fig. 3.13 SM minimum capacitance requirement for ϵ_{vrf5} and ϵ_{vrf10}, the voltage ripple factor set at 5% and 10%, respectively. MMC parameters at nominal value.

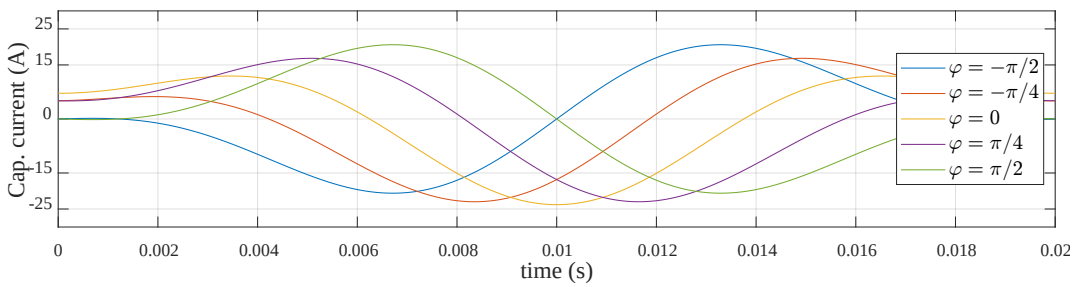


Fig. 3.14 SM dc-link current ripple simulation results. Converter is set at nominal values while results are shown for different power factors. Absolute maximum value is the same for all cases.

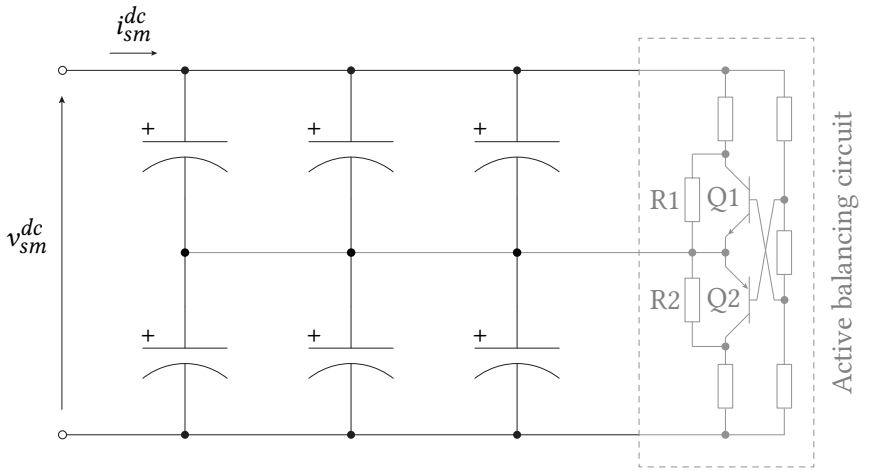


Fig. 3.15 SM capacitor dc-link scheme. Three groups in parallel connection, each one made of two series connected units form a 2.25 mF, 36 A current ripple and 900 V maximum voltage. The series connected capacitors are kept balanced using an active balancing circuit.

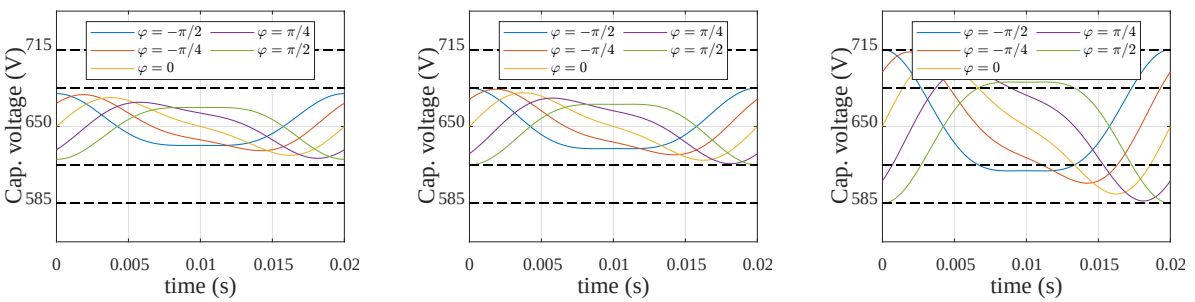


Fig. 3.16 SM capacitor voltage for different power factors and capacitance. (a) capacitance chosen C =2.25 mF, (b) capacitance calculated at ϵ_{vrf5}, and (c) capacitance calculated at ϵ_{vrf10}.

ripple factor below 5%. On the other hand, **Fig. 3.16(b)** and **Fig. 3.16(c)** show the SM voltage for the capacitance resulted for ϵ_{vrf5} and ϵ_{vrf10}, respectively. It is not difficult to deduce that a more restrictive voltage ripple factor will demand a bigger capacitance and a lower voltage requirement, while a more permissive voltage ripple factor will reduce capacitance needs but increasing voltage requirement. The fundamental frequency is another factor with an important effect on capacitance sizing, as frequency close to zero implies prohibitive capacitance values. This topic is of special interest in machine drives applications. Thus, an optimal capacitor selection might be made by weighting factors such as voltage/current ripple performance, cost, size, weight and insulation, in addition to, for instance, voltage ripple reduction by circulating current optimization [119]–[121]; however, further discussion about this topic is beyond the scope of this work.

3.2.2.3 Sensing

Different circuits and sensors are required locally in the SM so that control strategies, protection logic and CHM methods can be feed-in. As surface and cost were design constraints, the simple and

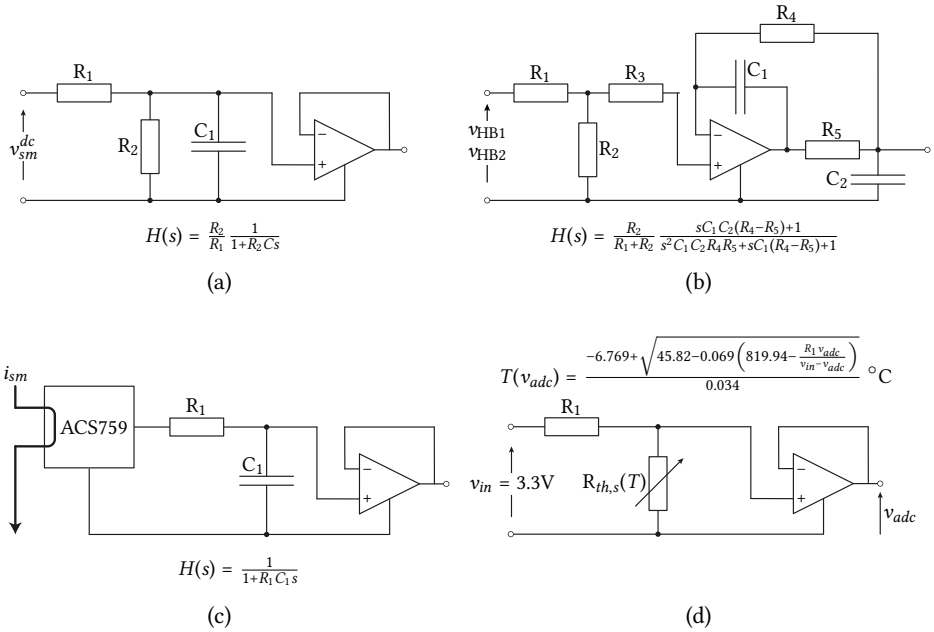


Fig. 3.17 SM sensing circuits and their transfer function. Circuit (a): for the SM dc-link voltage is used a voltage divider and a capacitor forming a first order low-pass filter. Circuit (b): for the SM terminal voltage, two voltage divider in cascade to a second-order low-pass filter is used. One circuit per terminal with respect to ground. Circuit (c): for SM current, it is used a first order low-pass filter. Circuit (d): for the SM IGBT module temperature T_s, it is used a voltage divider which input is fixed at 3.3 V and the variable resistor $R_{th,s}(T)$ is the thermal-resistor provided by the manufacturer.

effective solutions depicted in **Fig. 3.17** were selected.

The SM dc-link voltage measurement circuit is presented in **Fig. 3.17(a)**, which is composed of a voltage divider and a first-order low-pass filter. The input voltage is up to 900 V while the output voltage is in the 0 V to 3.3 V range. The cut off frequency is set at 1.5 kHz. The SM terminal voltage measurement circuit is shown in **Fig. 3.17(b)**. Two identical circuits are employed to measure each terminal voltage with respect to the local ground (the negative pole of the SM dc-link). Similar to the dc-link voltage measurement, this circuit is able to measure up to 900 V while the output voltage is in the 0 V to 3.3 V range. In addition, this configuration is a second-order low-pass filter at 16 kHz, thus pulses with cleaner rising/falling edges are obtained at the output. It is important to mention that these measurements take part in the protection strategy as they allow to determine if, for example, SM terminal voltage is present when bypass protection has been triggered. The circuit of the **Fig. 3.17(c)** is used to measure the SM terminal current. It is employed the Hall-effect-based linear current sensor ACS759 from Allegro, which converts the primary current (−100 A to 100 A) to 0 V to 3.3 V range. In addition, the signal is filtered by a low-pass filter set to 30 kHz cut off frequency. Finally, **Fig. 3.17(d)** depicts the circuit to measure the SM IGBT module temperature. The module has embedded a thermal-resistor which characteristic with respect to the temperature, is provided by the manufacturer. Accordingly, this circuit allows to measure temperature in the −190 °C to 200 °C range, converting it to the 0.16 V to 1.61 V range.

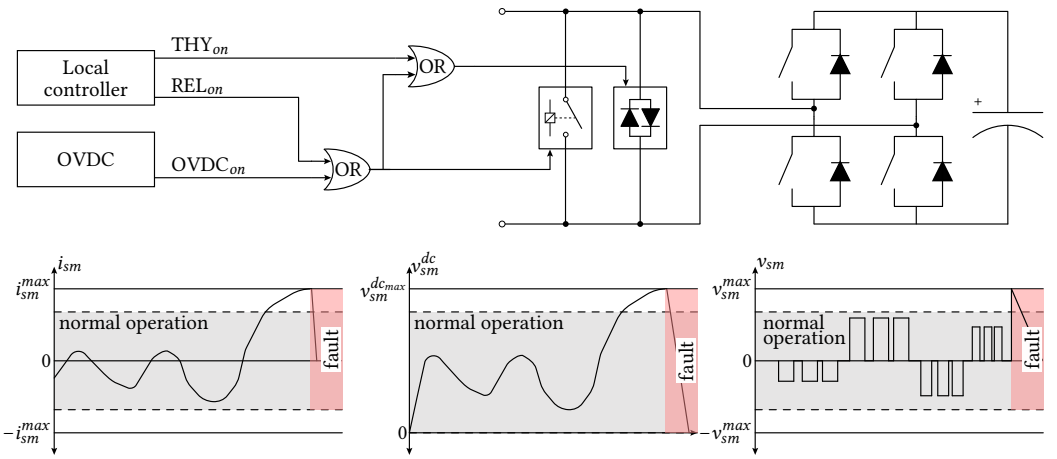


Fig. 3.18 SM protection logic scheme. Once the monitored value overpasses the set maximum value, a trigger signal to activate THY and/or REL is released. Local controller triggers the thyristor (THY$_{on}$) when $\pm i_{sm}^{max}$ or $v_{sm}^{dc_{max}}$ are reached. On the other hand, an independent OVDC triggers the REL and THY when $\pm v_{sm}^{max}$ is overpassed in SM terminals. At any case, the SM will be completely discharged.

3.2.2.4 Protection devices

The SM protection scheme is composed of two main parts: protection devices and protection logic. The protection devices aim to bypass the SM (terminals short circuit) so that the branch current might continuing flowing but the SM stops exchanging power with the rest of the system. Two devices are used for this purpose: two thyristors in antiparallel connection (THY) pulsed with 10 kHz, 10% duty cycle current pulses once activated, and a bi-stable electromechanical relay (REL). As the bypass process is expected to occur fast, the THY reacts first within µs providing temporary path to the branch current. The REL takes longer to close (in the order of several ms), however, will permanently bypass the SM even though after some time the SM is completely discharged. On the other hand, the protection logic is configured in the software of the local controller and by hardware using an overvoltage detection circuit (OVDC). By software, the THY is triggered when $v_{sm}^{dc} \geq v_{sm}^{dc_{max}}$ or $|i_{sm}| \geq i_{sm}^{max}$, while the REL is triggered when it is detected a malfunction in the THY. On the other hand, the OVDC uses analog components to detect SM terminals overvoltage (either positive or negative value) to trigger REL. Under any protection logic, when the REL is triggered, automatically the THY is triggered as well. The protection scheme is depicted in **Fig. 3.18**.

The protection devices used in this work are the Semikron SK70KQ12 antiparallel thyristor module, rated for 1200 V and 72 A at 125 °C junction temperature, and the Hongfa miniature latching relay HFE22, rated for 100 A. It is important to mention that the THY is mounted on the same IGBT module heatsink, however, since it is expected to operate only under fault condition, any extra heat due to THY losses can be totally absorbed by the heatsink without impacting the thermal behavior of the IGBT module.

3.2.2.5 Local controller and communication

As in the majority of the modern power electronics based converters a digital means to carry out control calculation and acquire measurement signal is found. Common choices are DSP and/or FPGA along with other specialized ICs to perform control calculations, analog-to-digital conversion,

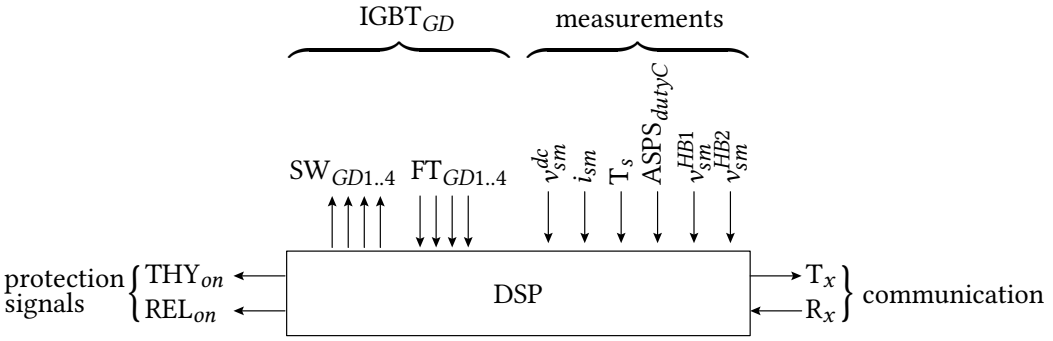


Fig. 3.19 SM local controller main signals. Four groups are recognized: IGBT gate-drivers comprising four switching signals and four fault signals, six measurements, two protection commands and communication.

protection logic, system monitoring, communication among other application-related activities. In this work, the SM was envisioned having its own processor unit so that some critical task can be handled locally. The DSP TMS320F28069PN from Texas Instrument was chosen to support this purpose. The main activities of the SM local controller are:

- State machine management (power up, active charging, operating, fault detection, testing and new code deployment),
- sensors and digital signals acquisition, monitoring and protection triggering,
- condition health monitoring,
- SM capacitor balancing controller,
- PWM generation, and
- upper layer communication

The main signals involved on previous tasks are depicted in **Fig. 3.19**.

The communication is one of the key element of the SM as it is used to, besides of exchange information with the MMC upper layer controller (Control hub and ABB AC 800PEC), synchronize the PWM carrier, analog-to-digital converter (ADC) and tasks execution as it is depicted in **Fig. 3.20**. Using this strategy, 40 kHz sampling frequency, PS-PWM implementation and fast protection actions are allowed. The physical medium to transmit information is a FOL, the protocol was chosen UART operating at 5 Mbps and the information allocation in every package responds to an ABB proprietary protocol.

3.2.2.6 Auxiliary submodule power supply

As presented in this section, the SM comprises different mechanisms and circuits to operate within the converter. Moreover, circuits need to be supplied with different voltage and power levels while high voltage isolation, reliability, safety, practicality, efficiency and cost-effectiveness requirements have to be achieved. A variety of solutions have been proposed to supply the SM [137]–[139], however, the isolated, non-centralized internal power supply based on the flyback converter is a popular choice [140]–[142]. In particular, it was chosen an isolated, flyback-based ASPS with planar magnetic, PCB with integrated windings and multiple isolated outputs as the solution to supply with low power

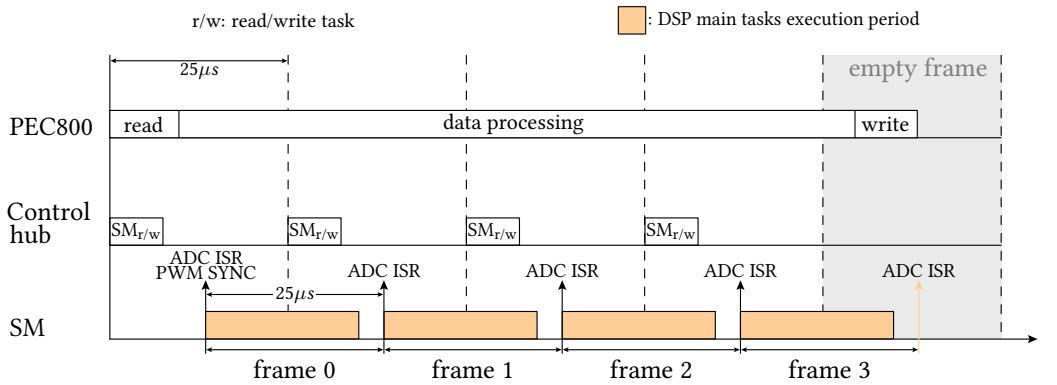


Fig. 3.20 SM communication diagram. All the information exchanged is divided in four frames, each one executed every 25 µs. An additional empty frame of 25 µs is used to synchronize the communication with control hub thus, a total of 125 µs is required to transmit/receive new information with the control hub.

and low voltage the SM sub-circuits. A scheme of the designed ASPS is presented in **Fig. 3.21**, while **Tab. 3.6** presents its main parameters.

The ASPS primary side is supplied from the SM dc-link, implying a 900 V isolation between the primary and each secondary winding. The UCC28C44 low-power current mode PWM controller regulates the flyback switch (MOSFET) duty cycle based on the current (i_{sense}) and $V_{out,5V}$ feedback. The MOSFET pulses are sensed and sent to the SM local controller (S_{MOSFET}) for monitoring purpose. As only one output is controlled, the other outputs are cross-regulated. A minimum of 290 V in the SM dc-link is required so that the PWM controller can be initially supplied through a series R-C bias circuit, allowing output regulation and self-supplying operation from the $V_{out,15V}$ terminal. The

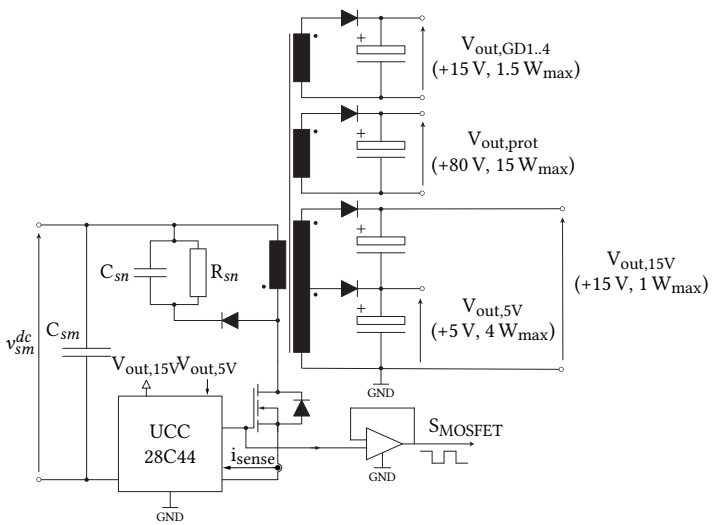


Fig. 3.21 Flyback-based ASPS scheme. Five outputs are completely isolated from the primary side (protection and gate-drivers outputs), while $V_{out,15V}$ and $V_{out,5V}$ share the same ground with the primary side (SM dc-link negative pole). On this way, the UCC28C44 low-power current mode PWM controller is self supplied from $V_{out,15V}$, and $V_{out,5V}$ is used as voltage feedback. The remaining outputs are cross-regulated through the magnetic coupling.

Tab. 3.6 ASPS main parameters

Parameter	Value	Unit
Primary winding voltage	200 – 900	V
Primary winding turns	120	-
Primary magnetizing ind.	12.5	mH
MOSFET switching freq.	20	kH
Snubber C_{sn}	2.7	nF
Snubber R_{sn}	196	kΩ
Sec. wind. turns $V_{out,15V}$	9	-
Sec. wind. turns $V_{out,5V}$	3	-
Sec. wind. turns $V_{out,GD}$	9	-
Sec. wind. turns $V_{out,prot}$	48	-

initial SM charge is achieved by the converter pre-charge system depicted in **Fig. 3.8**. Each secondary winding comprises a rectifying diode and an electrolytic capacitor as part of a low-pass filter, and their function are summarize as follow:

- 1 x 5 V, 4 W_{max} for the local controller and communication.
- 4 x 15 V, 1.5 W_{max} for the IGBT gate drivers ($V_{GD1..4}$). An additional 900 V isolation is required between the upper and lower GDs windings.
- 1 x 80 V, 15 W_{max} for 15 s operation when protection circuit is activated. The voltage is on purpose high in order to obtain a sufficiently large energy buffer with a relatively low storage capacitance.

As the required ASPS is specific for the developed SM, the coupled inductor was designed, built and tested at PEL. A planar multiwinding coupled inductor with PCB integrated windings was chosen over a wound one to minimize the electrical parameters drifting among the SMs. Two E-shape ferrites, custom gapped and glued by hand formed the magnetic core. Every coupled inductor was tested to verify final impedance and dielectric properties. The impedance was measured with an Omicron Bode 100 network analyzer and it was found a main resonance at 228 kHz (which corresponds to a capacitance of 37.6 pF) and mean value magnetizing inductance of 12.9 mH. On the other hand, the PCB with the integrated windings was tested in a Faraday cage with a single-phase high step-up line frequency test transformer and an Omicron MPD600 partial discharge measurement system in order to assess if any breakdown occurs in the substrate. A trapezoidal voltage profile test according to the IEC 61800-5 standard was applied and tests were passed.

3.2.2.7 Enclosure

Decided all the main electrical components of the SM, a proper metallic enclosure was designed. The main considerations were:

- electric shielding, as PCBs contain parts with sharp edges that might be sensitive to partial discharge (PD),
- shaping of the surrounding E-field to avoid air breakdown between the enclosure and other close elements,
- mechanical support for PCBs and heatsink,
- air-flow path definition, as forced-air has to be used to operate the SM at full current capacity, and
- access to SM terminals and connectors.

Due to the SM is a low voltage device, both UL 840 and IEC 61800-5-1 were considered. By assuming a maximum expected voltage inside of the SM enclosure of 1 kV, OVC2 and FR-14 (glass-reinforced epoxy laminated material) for PCBs, the minimum clearance and creepage distances are 3 mm and 6.3 mm, respectively. To reduce the electrical field intensity along the enclosure, the sharp angles were avoided. Considering a maximum theoretical air breakdown threshold of $3\,\mathrm{kV\,mm^{-1}}$, all the enclosure corners were restricted to a minimum of 3 mm radius (value obtained by FEM simulations). This value also complains with manufacturer limitations. The heatsink, dc-link capacitors and PCBs are the elements with the biggest weight and volume in the designed SM. Thus, to keep the enclosure design in simple, it is decided to organize these components to match a rectangular shape. Two stacked rectangular PCBs of same total dimension hold the low-voltage components and the power and protection devices, respectively. The PCB containing the IGBT module, the power capacitors and the THY, it is hold by the enclosure (internal rails) and the heatsink (mechanically connected to the bottom PCB through the IGBT and THY body). Similarly, the heatsink lies down in the enclosure. Due to the heatsink is inside of the enclosure, and the enclosure has a rectangular shape, the air to flow through the heatsink needs proper openings in both the inlet and outlet sections. Finally, the leads containing the air-flow openings consider the aperture for SM terminals, FOL, status LED and auxiliary connector. The designed enclosure is presented in **Fig. 3.22**. Additional information about enclosure design and test can be found in [143].

3.2.3 Submodule - final design

Having presented the SM's main characteristics, it is shown built device and experimental results of its operation. A total of 120 units were fully assembled and tested before final placement of 96 of them into the MMC research platform; however, this section is focused on illustrating a single unit's final appearance and main functionality.

Different perspectives of constructed SM are presented in **Fig. 3.23** and **Fig. 3.24**, highlighting the main parts. The left side of **Fig. 3.23** shows an exploded view of the bottom section of the SM where power components are revealed. The heatsink and power capacitors (heaviest elements) can be recognized from bottom to top, then the THY and IGBT modules. As THY heat contribution during protection triggering is modest, it is screwed on the heatsink due to mechanical reasons rather than thermal. The THY, IGBT module, and power capacitors are electrically connected through a PCB,

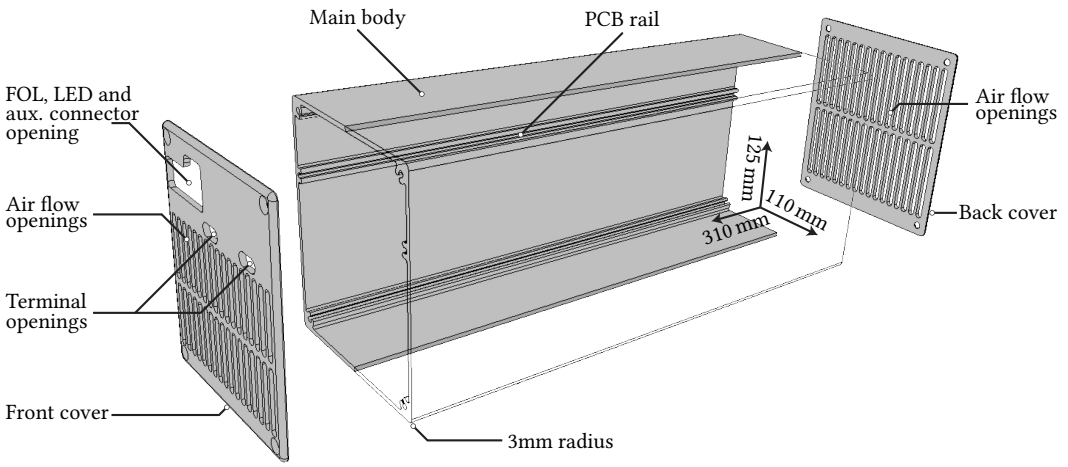


Fig. 3.22 Exploded view of a three dimensional SM metallic enclosure model. Three main parts are presented: the front cover, the main body and the back cover. In the front and back covers are highlighted the openings functionality, while the main body presents main dimensions.

which holds, in addition, the REL, a film capacitor (for dc-link straight inductance decoupling), active balancing circuit, voltage divider resistors for voltage measurements, current sensor (placed in the bottom side of the PCB), a section of the OVDC and terminals (cf. right side of **Fig. 3.23**). On top of the bottom PCB, it is found a second PCB which holds the low-voltage components (cf. right side of **Fig. 3.23**), namely, the ASPS circuitry, the four gate-drivers circuitry, the protection circuitry, and the DSP-based local controller, formed by the DSP, logical ICs, passives components, an auxiliary connector and FOL connectors.

It is worth highlighting three aspects of the presented design:

- the SM internal ground reference is the negative pole of its dc-link. Although the heatsink touches the enclosure (internal enclosure floor), the ground connection is improved by connecting the dc-link negative pole with the THY screw (using a wire) and with the enclosure rail (using a naked copper trace in the bottom PCB);
- after the enclosure is assembled (SM inside and front and back covers are in place), only four elements are visible/accessible from the front cover: the FOL connectors, status light emitting diodes (LEDs), auxiliary connector, and terminals. The FOL is used to communicate the SM with the control hub; the status LEDs are used to indicate, visually, basic SM states, e.g., $V_{out,5V}$ output is active, SM operating (switching), and SM in fault; the auxiliary connector is a five-pins component to provide fast access to the SM specific features and parts. A pin is used to DSP reboot (usually needed during debug and flashing process), two pins are employed to REL opening (mechanically permanent bypass that can be reset using an external power supply), and another two pins are used to supply the DSP-based local controller ($V_{out,5V}$ circuit) externally. The two copper terminals are strategically placed in the front of the enclosure so that external measurements and connections can be easily made; and
- the front and back cover openings and main body shape allow the air to flow through the IGBT module heatsink and between power capacitors and top PCB components, improving overall heat dissipation.

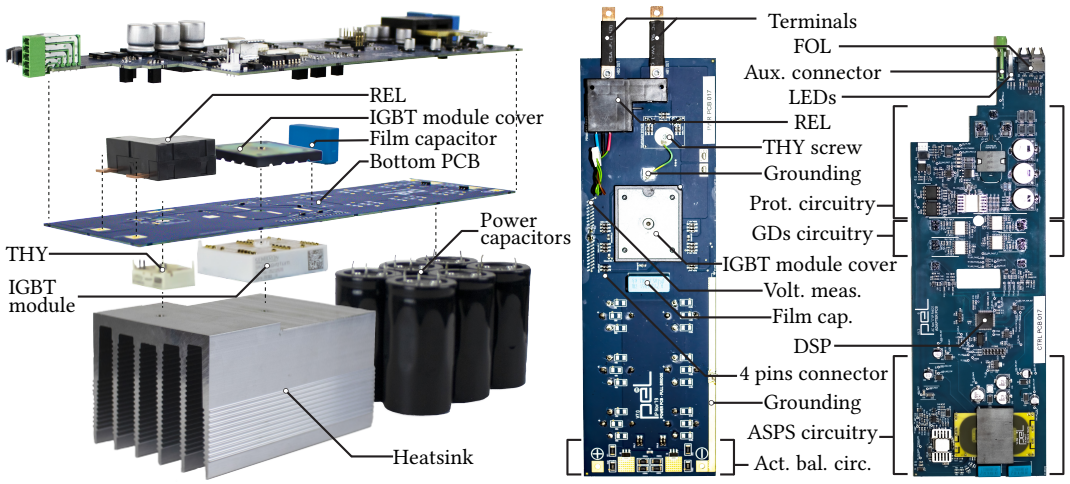


Fig. 3.23 Left side: SM exploded view, revealing power and protection devices. In addition, the PCB containing the low-power components is shown on top. Right side: top view of the low and high-power components PCBs. It is highlighted specific components and circuitry sections.

Results for a single SM mimicking an operating cycle within the converter, i.e., passive charging (start-up), operating (steady-state), and shutdown process, are presented in **Fig. 3.25**. These experimental tests do not precisely reproduce the SM operating conditions within the MMC; however, they illustrate SM main circuits and components functionality. Joined results with respect to time are shown in **Fig. 3.25** for SM dc-link voltage (v_{sm}^{dc}), terminal voltage (v_{sm}), terminal current (i_{sm}), ASPS $V_{out,15V}$ (ASPS IC controller self-supply voltage), and $V_{out,5V}$ (ASPS regulated output voltage).

At the start-up, the MMC is connected to the grid through precharge resistors, allowing the passive charging of the SM using their freewheeling diodes. The experiment was performed supplying the SM terminals with dc 300 V and a limited current, emulating the expected voltage of the slow charge process. During this period, the $V_{out,15V}$ circuitry is supplied directly from the SM dc-link through a bias R-C circuit which output is clamped to 15 V, allowing the ASPS PWM IC controller to activate at $v_{sm}^{dc} = 298$ V or equivalently $V_{out,15V}$ =14.54 V. At this point, the ASPS regulates the $V_{out,5V}$ output while the remaining outputs are cross-regulated, enabling the DSP-based local controller

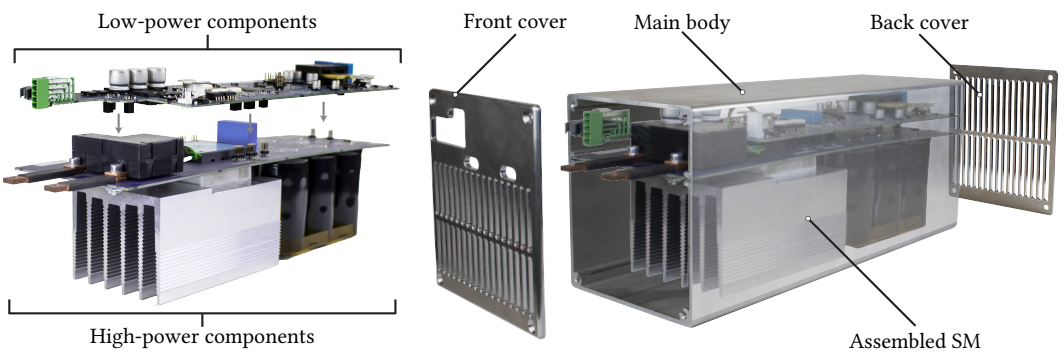


Fig. 3.24 Left side: side view of the SM showing the assembling procedure of the low and high-power components PCBs. Both PCBs are stacked through several low-voltage connectors. Right side: side view of the assembled SM inside of the metal enclosure, and closing procedure of the front and back covers.

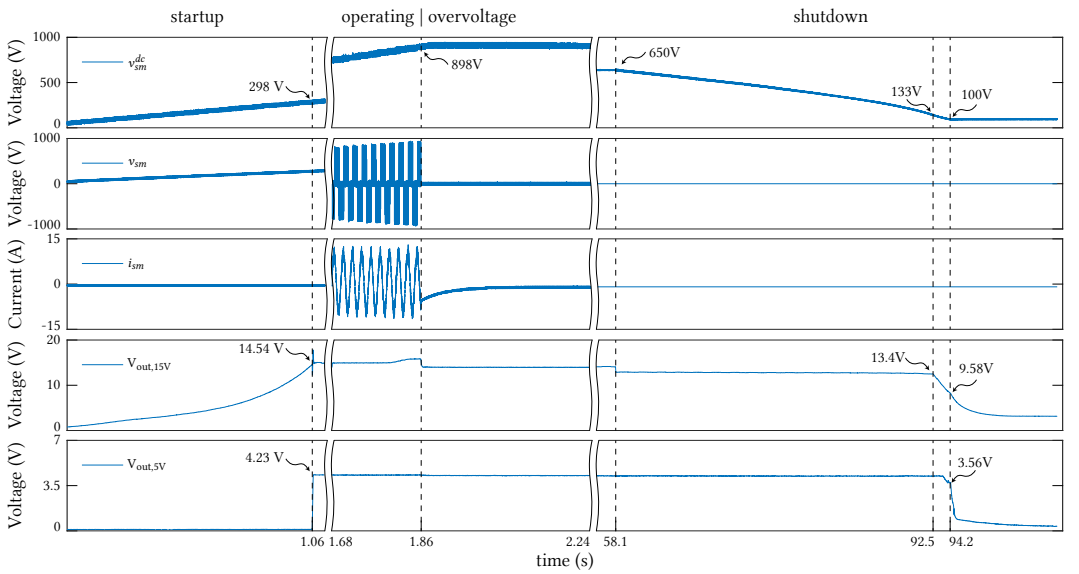


Fig. 3.25 SM functional experimental test results. From top to bottom: SM dc-link voltage v_{sm}^{dc}, terminal voltage v_{sm}, terminal current i_{sm}, ASPS $V_{out,15V}$ output voltage and regulated $V_{out,5V}$ output voltage. From left to right, passive charge process, operating state and discharge process.

(measurements, logic, and communication), ASPS self-supplied operation ($V_{out,15V}$), gate-drivers, and protection circuit.

The SM can continue in the passively charged state while terminal voltage is present, thus to get operating state, the active charging process has to be employed, i.e., to use the SM power switches so that a small and controlled amount of power can be absorbed from ac terminals. In the presented experiment, this process is skipped by connecting the dc power supply in the SM auxiliary dc terminals and setting voltage to $v_{sm}^{dc} = 650\,V$, reaching the operating state where PWM is activated. This state allows checking the gate-drivers and their supply circuits, and current sensor functionality. In addition, the OVDC, protection devices, and their supply were tested by increasing the dc-link voltage up to 900 V, the level at which they are expected to operate. The OVDC detected overvoltage at 898 V, triggering both THY and REL.

Finally, the last section shows SM discharging after the active power source (dc power supply) is disconnected. Through the ASPS consumption (loading the dc-link), the SM is discharged in less than a minute. At approximately v_{sm}^{dc} =133 V, the $V_{out,15V}$ output reduces its voltage, making it difficult to regulate $V_{out,5V}$ output. At 9.58 V, the ASPS PWM IC controller is turned off, and all the outputs. It is important to mention that the shutdown process is about safely discharging the dc-link and having enough time to the DSP communicate upstream status or any other relevant information to the converter controller before SM is entirely off.

3.3 Summary

In this chapter, the classical ac-dc MMC configuration is presented along with the derivation of its main mathematical operating principles. The MMC to be able to serve desired terminals' voltage and current, total and internal energy has to be controlled to a specific range while power is transferred

between the ac and dc ports. Moreover, the fundamental principles governing the MMC impose several technical challenges in SM sizing, designing, and manufacturing process, as well as in its operation, topics that have been comprehensively presented, explained, and illustrated.

The built MMC research platform, a PEL effort to contribute with further research on this topic, has been largely presented, paying particular attention to the power semiconductors and capacitors; sensing, protection, DSP-based local controller, communication, ASPS circuitry, and metallic enclosure that forms the SM.

Inspired by the complexity of the MMC, its large number of SMs (and forming components), and the aim to improve its reliability, the developed SM is used as a subject of study to investigate and elaborate different CHM strategies. Notably, the following chapter deals with SM capacitor aging supervision by estimating and monitoring its capacitance changes.

4
SM Capacitance Estimation

In the modular multilevel converter, the submodule capacitors represent one of the most critical components, strongly impacting the overall converter cost and performance. This chapter presents a method for the submodule capacitor condition health monitoring, which is deployed directly on the local submodule controller and operates without disturbing or impacting the regular converter operation. Mathematical derivation, offline and real-time simulations, and experimental results introduce, illustrate, and demonstrate the effectiveness of the proposed strategy.

4.1 Motivation

Already presented in **Chap. 2**, power electronics-based equipment reliability, particularly the MMCs, can be improved further by utilizing different strategies such as those proposed in the PHM framework. CHM, prognostics, diagnostics, and health management concepts allow the converter owner to have valuable information about its current and future health state and guidelines or procedures actions if an incipient fault or failure occurs. Specifically, CHM methods are relevant as they fed in PHM units and enable the triggering of preventive maintenance alarms before severe deterioration or major failure occurs [47].

The power capacitor's failure rate is higher compared to other power electronics devices [39]. This is particularly important in MMC SM, where dc-link power capacitors are put under different stressors, for instance, high current and voltage ripple and high temperature, among other degradation factors related to environmental conditions such as humidity and mechanical vibrations high ambient temperature [78]. Several publications have addressed the MMC SM power capacitor CHM proposing online methods to monitor capacitance reduction of the Al-cap using model-based methods with parameter identification techniques; however, as was concluded in **Chap. 2**, more effort has to be made to simplify and demonstrate through experiments new CHM strategies.

This chapter presents an alternative and simple approach for the MMC SM dc-link capacitor CHM based on the RWLS technique to estimate and track its capacitance value and changes within time. Such a technique assures relatively high accuracy when sensors, acquisition systems, power switching events, and other sources of noise and error are present. In contrast with the previous works based on RLS methods and capacitance monitoring, the proposed idea does not require current injection (control modification or external device) or band-pass filters, significantly reducing complexity and processing burden. Also, the proposed scheme does not need to modify the MMC or the SM's existing control strategy, no SM is bypassed, no extra hardware is required as the branch current, and the SM dc-link voltage measurements are commonly available.

The proposed method is introduced by first presenting preliminary considerations about SM dc-link

current and impedance. Then, the strategy is fully described and validated through simulation studies, RT-HIL simulations, and experimental tests.

4.2 SM dc-link capacitor current

Already presented in (3.32), the SM dc-link current i_{sm}^{dc} is a direct consequence of the MMC control strategy keeping its terminal voltages (or currents) as the desired reference. Simultaneously, the energy stored in the SM dc-link capacitors is kept constant within a fundamental period and equally balanced between SMs within a branch, between branches belonging to the same leg, and between legs. In addition, expression (3.32) reveals that its frequency component's amplitudes depend on the converter operating point. Assuming power balance between the converter's ac and dc terminals, i.e., the dc component in (3.32) is zero, the dc-link current can be rewritten as a function of the converter's active and reactive power as:

$$V_{DC}I_{DC} = P_{DC} = \frac{3}{2}v_{g1}i_{g1}\cos\varphi = S_{3\phi}\cos\varphi = P_{3\phi} \tag{4.1}$$

$$i_{sm}^{dc}(P_{3\phi}, Q_{3\phi}) = \frac{\sqrt{Q_{3\phi}^2 + P_{3\phi}^2}}{6}\left(\frac{\cos\Big(\omega t + \arctan\big(Q_{3\phi}/P_{3\phi}\big)\Big)}{v_{g1}} - \frac{\cos\Big(2\omega t + \arctan\big(Q_{3\phi}/P_{3\phi}\big)\Big)}{V_{DC}}\right) - \frac{P_{3\phi}v_{g1}\cos\omega t}{3V_{DC}^2} \tag{4.2}$$

Where $S_{3\phi}$, $P_{3\phi}$ and $Q_{3\phi}$ are the converter apparent, active, and reactive power, respectively. As an illustration, **Fig. 4.1** shows the dependency of the i_{sm}^{dc} maximum amplitude with respect to the

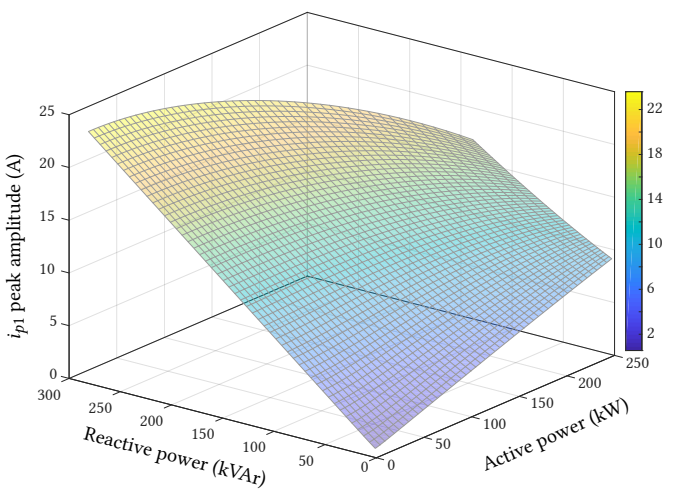


Fig. 4.1 The SM dc-link peak current with respect to considered MMC active and reactive power. The current is maximum when the active power is zero, and the reactive power is maximum. The bigger the current (first and second harmonic), the bigger the extractable information to estimate the capacitance.

converter's active and reactive power, where it is used the parameters of the considered converter (cf. **Tab. 3.1**). It becomes straightforward that the lower the load, the lower the SM dc-link current amplitude. This analysis is relevant to consider since presented strategy uses, in part, dc-link current to extract information about the SM capacitance, suggesting that the MMC operating point might be considered in the decision process related to activation of the calculations of the method.

As the considered SM does not possess a sensor to measure its dc-link current and expression (3.32) does not take into account its switching nature, i_{sm}^{dc} can be reconstructed from the measured i_{p1} (for the SMs in the positive branch 1) and the SM switch states presented in **Tab. 3.2** (available in the DSP registers), yielding:

$$i_{sm}^{dc}(t) = i_{p1}(t)(S_2 \wedge S_3) \vee -i_{p1}(t)(S_1 \wedge S_4) \tag{4.3}$$

An illustration of the signals involved in the reconstruction of i_{sm}^{dc} is presented in **Fig. 4.2**. During MMC operation each SM within a branch receive the corresponding voltage reference which is compared with the DSP-based local controller PWM carrier signal, producing the pulse signals S_1, S_2, S_3 and S_4. Accordingly to **Tab. 3.2**, only two switch states allow to the SM to be actively charged or discharged, depending of branch current sign. When $S_1 = S_4 = 1$ (consequently $S_2 = S_3 = 0$), if i_{p1} is positive (leaving the SM), i_{sm}^{dc} is negative, discharging the SM. If i_{p1} is negative, the SM is charged. On the other hand, when $S_2 = S_3 = 1$ (consequently $S_1 = S_4 = 0$), if i_{p1} is positive, the SM is charged and when negative, the SM is discharged. An example is highlighted green in **Fig. 4.2**. Plot d) shows current i_{p1}. While positive, $S_2 = S_3 = 1$ state charges the SM capacitors, and $S_1 = S_4 = 1$ state discharge it.

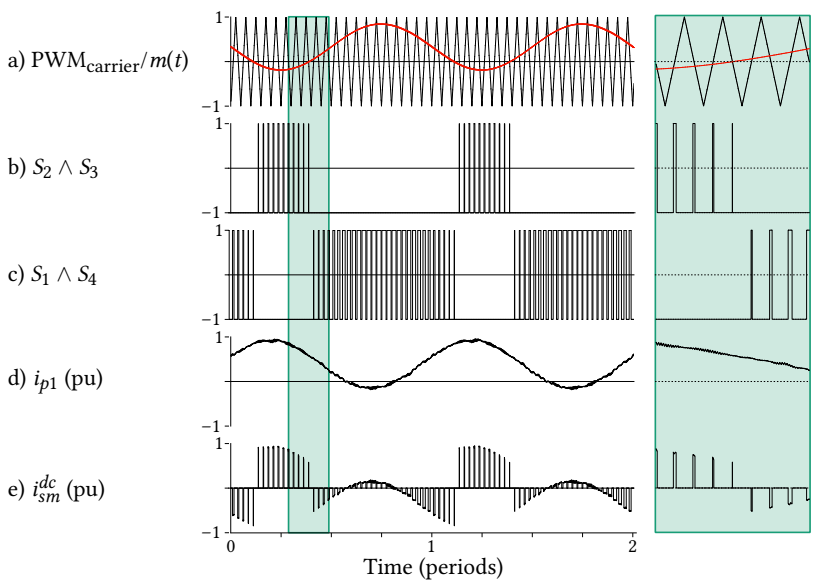


Fig. 4.2 SM main waveforms during two fundamental periods. From top to bottom: a) SM PWM triangular carrier at f_{sw} and the corresponding output voltage reference signal (red) coming from the MMC main controller, b) the term $S_2 \wedge S_3$ from (4.3), c) the term $S_1 \wedge S_4$ from (4.3), d) the SM ac terminal current i_{p1} sampled at $f_s \gg f_{sw}$, and e) SM dc-link current reconstructed i_{sm}^{dc}. Highlighted green, a zoom of the involved signals.

4.3 SM dc-link impedance

The capacitance estimation problem based on the impedance measurement, as it is proposed in this work, faces not only the issue related to its parameters changing due to the aging process but also the effect of the surrounding components connected to the SM dc-link and the frequency response of the current flowing through it. Let us start analyzing the SM dc-link impedance considering the scheme depicted in **Fig. 4.3**. Z_c represents the power capacitors impedance, and Z_{aux} represents the impedance of the auxiliary components connected to it, such as the ASPS (cf. **Fig. 3.15** and **Fig. 3.21**). Z_c can be modeled as (4.4) (cf. **Fig. 2.4**).

$$Z_c(s) = \frac{1}{sC} + \mathrm{ESR} + s\mathrm{ESL} \tag{4.4}$$

When the SM is operating, Z_{aux} can be modeled as a constant power load P_{aux} since the ASPS keeps its output voltage regulated while its input voltage might change; thus, the dc-link equivalent load can be represented by (4.5).

$$Z_{aux} = \frac{P_{aux}}{i_{aux}^2} \tag{4.5}$$

Where i_{aux} is the ASPS primary-side power supply current consumption. In consequence, the SM dc-link impedance Z_{SM} can be written as

$$Z_{SM}(s) = \frac{(C \cdot \mathrm{ESL} \cdot P_{aux})s^2 + (C \cdot P_{aux} \cdot \mathrm{ESR})s + P_{aux}}{(C \cdot \mathrm{ESL} \cdot i_{aux}^2)s^2 + C(\mathrm{ESR} \cdot i_{aux}^2 + P_{aux})s + i_{aux}^2} \tag{4.6}$$

Fig. 4.4 shows the bode diagram of Z_{SM}. The continuous black line is the impedance magnitude (top plot) and phase-shift (bottom plot) curve using $P_{aux} = P_s$, $C = C_{nom} = 2.25\,\mathrm{mF}$, $\mathrm{ESR} = \mathrm{ESR}_{nom} = 66.6\,\mathrm{m\Omega}$, and $\mathrm{ESL} = \mathrm{ESL}_{nom} = 66.6\,\mathrm{nH}$ values. Color-dashed lines illustrate the sensitivity of the nominal curve when those parameters vary. As expected, Z_{aux} behaves as a linear high-impedance in the zero-frequency range. In the low-frequency range (few Hz to few hundred Hz), Z_{SM} is dominated by the ideal capacitor impedance. In the medium-frequency range (few kHz to few MHz), Z_{SM} is influenced by the ESR. Finally, in the high-frequency range (above a few tens of MHz) ESL, dominates Z_{SM}. This diagram shows that the extractable information is limited to the SM dc-link current frequency components that excite the SM dc-link impedance. The expression (3.32) exposes the oscillating nature of i_{sm}^{dc} at fundamental $\omega = 2\pi f_0$ and $2f_0$, while the previous section, together with the unipolar modulation scheme adopted, reveals the oscillating component in the SM dc-link current at the switching frequency f_{sw}, and the $2f_{sw} \pm f_0$ side-band components around the $2f_{sw}$ apparent switching frequency component (vertical green lines in the frequency axis). Consequently, the primary information extractable is likely the C value due to the f_0 and $2f_0$ current components close to the ideal-capacitive zone. On the other hand, the ESR estimation is theoretically possible to carry out but challenging to implement since it needs both high measurements sampling frequency and high accuracy measurement, especially the $2f_{sw} \pm f_0$ SM dc-link voltage component due to it is

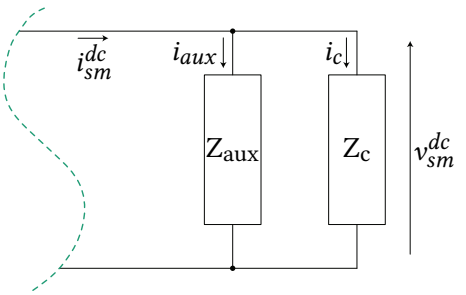


Fig. 4.3 The SM dc-link impedance scheme. Two impedances parallel connected represent the capacitor bank (Z_c), and any additional load connected to the dc-link (Z_{aux}), respectively.

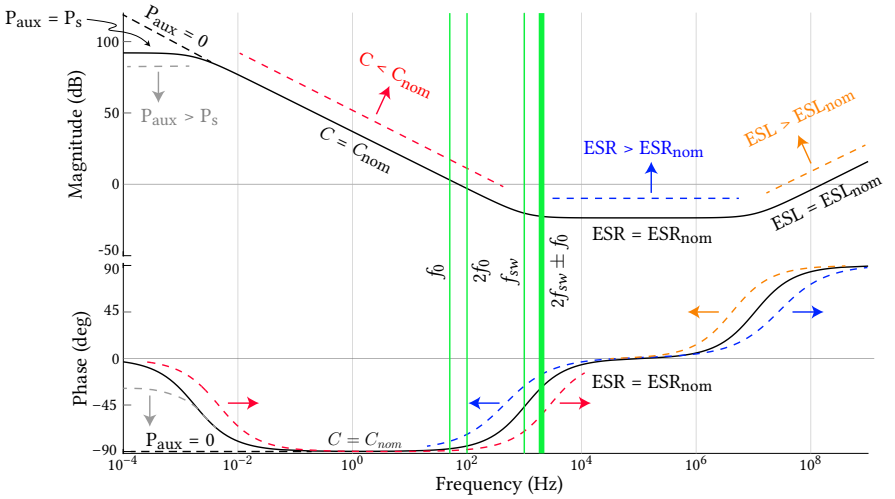


Fig. 4.4 The SM dc-link impedance in the frequency domain. The top plot presents the magnitude and bottom plot the phase. The nominal curves (continuous black line) are created considering dc-link nominal parameters, while the color curves show the trend when those parameters are changed.

highly attenuated. Even more, with the considered P_s and ESL_{nom}, it is deduced that Z_{aux} and ESL do not play an essential role in the capacitance estimation. It is important to mention that when the SM dc-link capacitor bank ages or some of its components fail, the C value will be reduced, increasing the impedance magnitude and moving the phase-shift curve to the right, improving the C estimation even though, at the same time, the ESR increases its participation in the impedance composition since $ESR \ll 1/sC$. In consequence, Z_{SM} for the estimation can be re-written as:

$$\frac{v_{sm}^{dc}(s)}{i_{sm}^{dc}(s)} = Z_{SM}(s) = \frac{1}{sC} \tag{4.7}$$

4.4 Proposed SM capacitor CHM method

In the previous chapter and sections, all the considerations and operating principles related to the converter and the SM were presented as they are needed to analyze and describe the proposed scheme. The MMC SM dc-link capacitor CHM method relies on extracting the capacitance value from the

low-frequency SM dc-link impedance, taking advantage of the existing sensed variables of the SM and the oscillating nature of the SM dc-link current. **Fig. 4.5** shows the scheme of the proposed method. In each sampling period the DSP discretizes the sensed v_{sm}^{dc} and i_{p1} and retrieves the switching signals $S_1(k)$ and $S_3(k)$ (or equivalent $S_2(k)$ and $S_4(k)$) calculated in the unipolar modulation. The dc-link current $i_{sm}^{dc}(k)$ is reconstructed using the discrete quantities $i_{p1}(k)$, $S_1(k)$ and $S_3(k)$ in (4.3). Then, both $i_{sm}^{dc}(k)$ and $v_{sm}^{dc}(k)$ together with the same signals from the previous iteration $(k-1)$ are used to estimate a new parameter $\hat{C}(k)$, using the RWLS technique. This procedure is repeated M iterations or until the difference between two consecutive found parameters is less than a defined limit, as expressed in (4.8).

$$\text{SC} = k \leq M \vee |\hat{C}(k) - \hat{C}(k-1)| \leq \varepsilon \tag{4.8}$$

When the stop condition is met, the parameter estimated is sent to the MMC main controller.

Generally, the RWLS is a mathematical tool used in the parameters estimation problem of gray-box models that can handle the measurement uncertainties introduced by sensors and the digitalization process. Given a system that can be modeled as a linear function of a set of unknown parameters in general, the main principle of any least-squares method is to determine the unknown parameters by minimizing the sum of the squared error between the actual system output (measured) and linear system model output (calculated) while they are stimulated with the same input. In particular, the RWLS solves the minimization problem recursively, advantageous in a field application where computing capacities might be limited. Please, see **App. B** for more details about the mathematical development of the RWLS algorithm. For the case of the presented method, the RWLS is applied as described hereafter:

Using the Bilinear transform the transfer function proposed in (4.7) is discretized, yielding

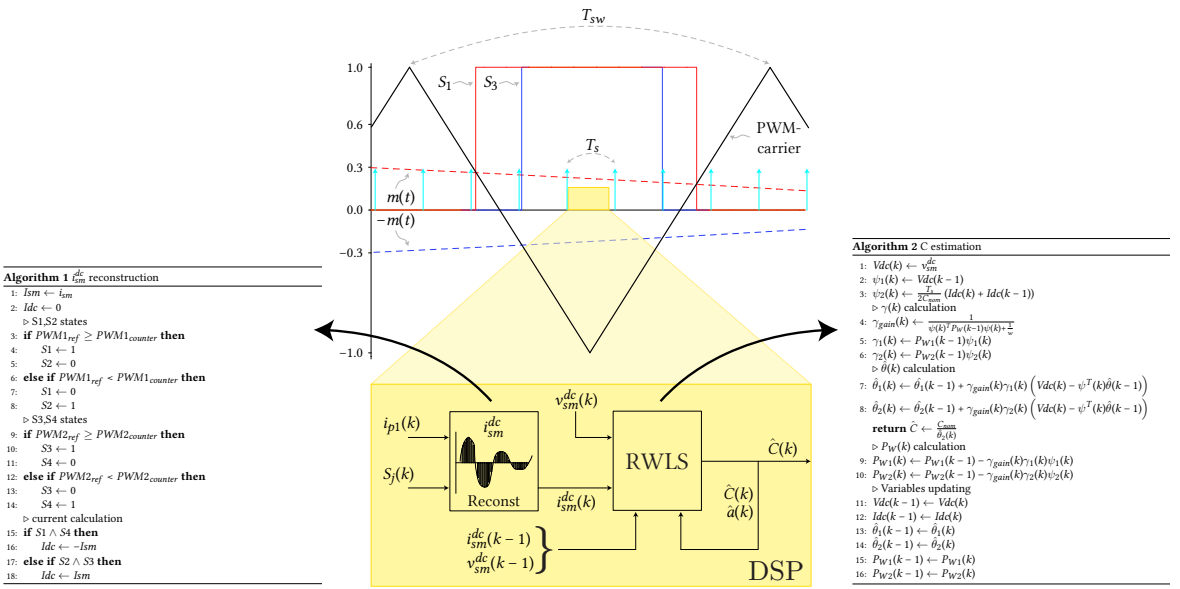
$$G(z^{-1}) = \frac{v_{sm}^{dc}}{i_{sm}^{dc}} = \frac{\frac{T_s}{2C}(z^{-1}+1)}{1-z^{-1}} \tag{4.9}$$

which resembles (B.1) in **App. B**. Then, the data vector $\psi^T(k)$ and the parameter vector $\hat{\theta}^T(k)$ are written as:

$$\psi^T(k) = \begin{bmatrix} v_{sm}^{dc}(k-1) & \dfrac{T_s}{2C_{nom}}\left(i_{sm}^{dc}(k) + i_{sm}^{dc}(k-1)\right) \end{bmatrix} \tag{4.10}$$

$$\hat{\theta}^T(k) = \begin{bmatrix} a(k) & \dfrac{1}{\hat{C}(k)} \end{bmatrix} \tag{4.11}$$

Please note that the estimated $\hat{C}(k)$ from the above equation, represents the normalized values respect to C_{nom} and $a(k)$ reflects the past value of v_{sm}^{dc}. Finally, one has to calculate iteratively (B.4), (B.5) and (B.6) as it is explained in **App. B**.



Algorithm 1 $\frac{dc}{ism}$ reconstruction

$Ism \leftarrow i_{sm}$
$Idc \leftarrow 0$
▷ $S1$,$S2$ states
if $PWM1_{ref} \geq PWM1_{counter}$ **then**
  $S1 \leftarrow 1$
  $S2 \leftarrow 0$
else if $PWM1_{ref} < PWM1_{counter}$ **then**
  $S1 \leftarrow 0$
  $S2 \leftarrow 1$
▷ $S3$,$S4$ states
if $PWM2_{ref} \geq PWM2_{counter}$ **then**
  $S3 \leftarrow 1$
  $S4 \leftarrow 0$
else if $PWM2_{ref} < PWM2_{counter}$ **then**
  $S3 \leftarrow 0$
  $S4 \leftarrow 1$
▷ current calculation
if $S1 \wedge S4$ **then**
  $Idc \leftarrow -Ism$
else if $S2 \wedge S3$ **then**
  $Idc \leftarrow Ism$

Algorithm 2 C estimation

$Vdc(k) \leftarrow v_{sm}^{dc}$
$\psi_1(k) \leftarrow Vdc(k-1)$
$\psi_2(k) \leftarrow \frac{T_s}{2C_{sm}^{nom}}(Idc(k) + Idc(k-1))$
▷ $\gamma(k)$ calculation
$\gamma_{gain}(k) \leftarrow \frac{1}{\psi(k)^T P_W(k-1)\psi(k)+\frac{1}{\omega}}$
$\gamma_1(k) \leftarrow P_{W1}(k-1)\psi_1(k)$
$\gamma_2(k) \leftarrow P_{W2}(k-1)\psi_2(k)$
▷ $\hat{\theta}(k)$ calculation
$\hat{\theta}_1(k) \leftarrow \hat{\theta}_1(k-1) + \gamma_{gain}(k)\gamma_1(k)\left(Vdc(k) - \psi^T(k)\hat{\theta}(k-1)\right)$
$\hat{\theta}_2(k) \leftarrow \hat{\theta}_2(k-1) + \gamma_{gain}(k)\gamma_2(k)\left(Vdc(k) - \psi^T(k)\hat{\theta}(k-1)\right)$
return $\hat{C} \leftarrow \frac{C_{nom}}{\hat{\theta}_2(k)}$
▷ $P_W(k)$ calculation
$P_{W1}(k) \leftarrow P_{W1}(k-1) - \gamma_{gain}(k)\gamma_1(k)\psi_1(k)$
$P_{W2}(k) \leftarrow P_{W2}(k-1) - \gamma_{gain}(k)\gamma_2(k)\psi_2(k)$
▷ Variables updating
$Vdc(k-1) \leftarrow Vdc(k)$
$Idc(k-1) \leftarrow Idc(k)$
$\hat{\theta}_1(k-1) \leftarrow \hat{\theta}_1(k)$
$\hat{\theta}_2(k-1) \leftarrow \hat{\theta}_2(k)$
$P_{W1}(k-1) \leftarrow P_{W1}(k)$
$P_{W2}(k-1) \leftarrow P_{W2}(k)$

Fig. 4.5 Proposed method scheme respect the main time-events in the SM. The top picture shows the S_1 and S_3 DSP PWM output signals as a consequence of the comparison of the modulation index $m(t)$ (S_1) and $-m(t)$ (S_3) respect to the PWM triangular-waveform carrier signal. The straight arrows represent the DSP sampling instant, where i_{p1} and v_{sm}^{dc} are acquired. During this period (T_s) one iteration of the RWLS is performed resulting in a preliminary $\hat{C}(k)$ estimation. This procedure is repeated until the stop condition (4.8) is met.

4.5 Method validation

In order to validate the proposed CHM method, three different steps are followed: a) offline simulations considering the MMC model from **Fig. 3.2**, b) MMC RT-HIL simulations where the method is deployed in the actual SM's control and communication environment (hardware and software) while the power components are simulated in real-time (cf. top scheme in **Fig. 4.7**), and c) MMC test setup where the method is deployed in the developed SMs (cf. bottom scheme in **Fig. 4.7**).

4.5.1 Practical considerations

Independently of the validation method, the proposed method is validated considering the following details:

1. Both MMC RT-HIL and MMC test setup aim to make the SMs and its controller operate under similar conditions as they would be exposed to during a regular MMC operation. To do so, an MMC reduced branch circuit is considered and presented in the central part of **Fig. 4.7**. Four SMs and an inductor are connected in series to form the reduced MMC branch (MMC-branch). The MMC-branch is connected to an external voltage source, made of four series-connected SMs forming the so-called source-branch (S-branch). Each SM of the S-branch has available dc-link terminals, and they are connected to four isolated dc sources. The S-branch operates as a voltage source; thus, the MMC-branch operates by modifying its terminal voltage (3.11) to induce the desired current through the SM terminals (3.13).

2. All the measurements used in the offline and MMC RT-HIL simulations were distorted using

additive white Gaussian noise $\sim \mathcal{N}(\mu = 0, \sigma = 0.5)$.

3. Parameter vector initial condition: It is chosen as the result of the previous estimation process. When previous result does not exist then the parameter vector initial condition is chosen as $\hat{\theta}^T(0) = [1 \quad 1]$. In other words, the RWLS assumes C_{nom} as initial guess of the first iteration and previous v_{sm}^{dc}.

4. Covariance matrix initial condition: Choosing a large covariance value for each unknown parameter can be interpreted as the RWLS assumes that the parameters initial condition are not close to the real values, increasing the parameters' searching range and the convergence speed. However, large covariance values might cause numeric instability as the calculated variables might overflow or underflow in a limited data type size implementation. Thus, the initial covariance was chosen as $P_w(0) = 10^{-4} I_{2x2}$.

5. Solving the capacitance estimation problem:

   5.1. First it is reconstructed i_{sm}^{dc} using i_{p1} and the switching signals S_1 and S_3 in (4.3). S_1 and S_3 are retrieved from the DSP's PWM module.

   5.2. Using i_{sm}^{dc} and v_{sm}^{dc} together with (4.10) and (4.11) it is applied the RWLS technique presented in **App. B**, following the next order of the equations: (B.4) → (B.5) → (B.6).

   5.3. Check the stop condition considering $M = 4x10^3$ (approximately 5 s at f_s) and $\varepsilon = 10^{-3}$.

   5.4. Retrieves the estimated capacitance physical values using $\hat{C}(mF) = C_{nom}\hat{C}(k)$.

   5.5. Report found parameter value to the MMC main controller.

4.5.2 Offline simulation studies

Parameters of the simulated MMC were already presented in **Tab. 3.1**. The modeled MMC utilizes the classical d-q frame grid current control (GCC) and outer layer controller for the dc terminals (cf. **Fig. 3.6**). The total energy control and the internal energy balancing control are based on [144]. Then, the simulation is carried out considering the next scenario:

- The SM dc-link capacitance CHM is performed while the MMC operates as a rectifier fully loaded on its dc side.
- Each SM dc-link actual capacitance is initialized randomly in the range of $C_{nom} \pm 20\%$ (to simulate the manufacturing tolerance). On the other hand, ESR is set nominal.
- Between t =5 s and t =5.5 s the CHM method is stopped, each dc-link capacitance is reduced to 80% of its initial condition, and ESR is increased 2.5 times.
- At t = 5.5 s the method is started again using the last estimated parameters as starting point.

The top part of **Fig. 4.6** shows the parameter estimation results for each SM expressed as the error with respect to their real value, while the bottom part presents the result for the SM1 expressed in physical units. The error is calculated using $error(\%) = 100\left|\hat{C} - C_{real}\right|/C_{real}$. At the beginning of the simulation the error is high due to the initial conditions and the simulation start transient. After 100 ms it starts to converge and after 2 s it settles down. At t =5 s the method is stopped and initialized at t =5.5 s finding a big error as the real capacitance was reduced 20%. The maximum error found is 4.6%.

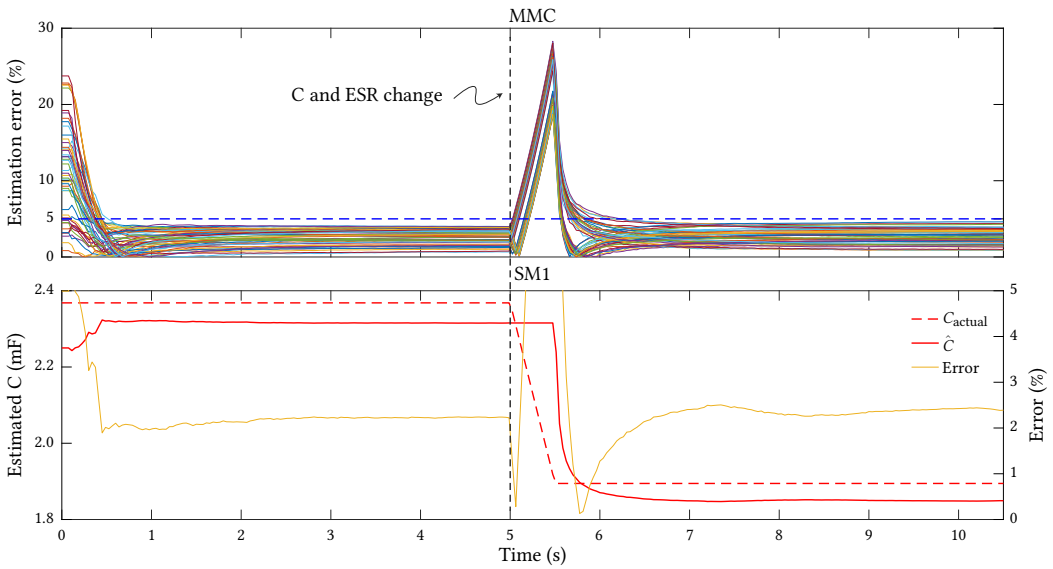


Fig. 4.6 Offline simulation results. Top plot: estimation error for each SM dc-link capacitance. In the first part of the simulation (t <5 s) the real capacitance for each SM is set randomly and ESR is set nominal. In the second part (t >5.5 s) the real capacitance is set to 80% of its initial value and ESR is set 2.5 times its nominal value. Bottom plot: the estimated parameter for the SM_1 (leg A, upper branch). The continuous red line is the estimated capacitance $\hat{C}_1$ while the dashed red line is the real value.

4.5.3 MMC RT-HIL simulations

Following successful verification of the model in offline simulations, the complete algorithm is deployed on the DSP of the actual MMC SM. In order to extensively verify its performances under various test cases that are not easy to achieve in the experimental setup, the RT-HIL system is developed. The MMC RT-HIL simulator, depicted in the top part of **Fig. 4.7**, comprises eight SM control boards, each with a replica of the prototype SM local controller, a Plexim real-time simulator RT-Box 1, and an interface board to adapt the signals between them. Consequently, the RT-Box simulates the MMC-branch SMs power components, S-branch SMs power components, inductors between them and S-branch dc sources. In order to show the method's capability to estimate the SM dc-link capacitance under different capacitor aging states, each SM capacitor impedance was set with different values and time dependency. Also, each initial capacitance condition was set randomly in the range $C_{nom} \pm 20\%$, and ESR initial condition was set ESR_{nom}, thus:

- SM1: Both parameters are kept constant along with the simulation as it would be the case with capacitor parameters at the beginning of its lifespan,
- SM2: The capacitance and ESR are set at 80% and 250% of its initial condition, respectively, as it would be the case with capacitor parameters at the end of its lifespan,
- SM3: capacitor bank is reduced one third at t =2000 s as emulating artificially loss of capacitance in order to verify performance of the method, representing a 33.3% capacitance reduction and 50.1% ESR increase,
- SM4: capacitance and ESR are linearly changed to 80% and 250% from their initial condition respectively, emulating ageing.

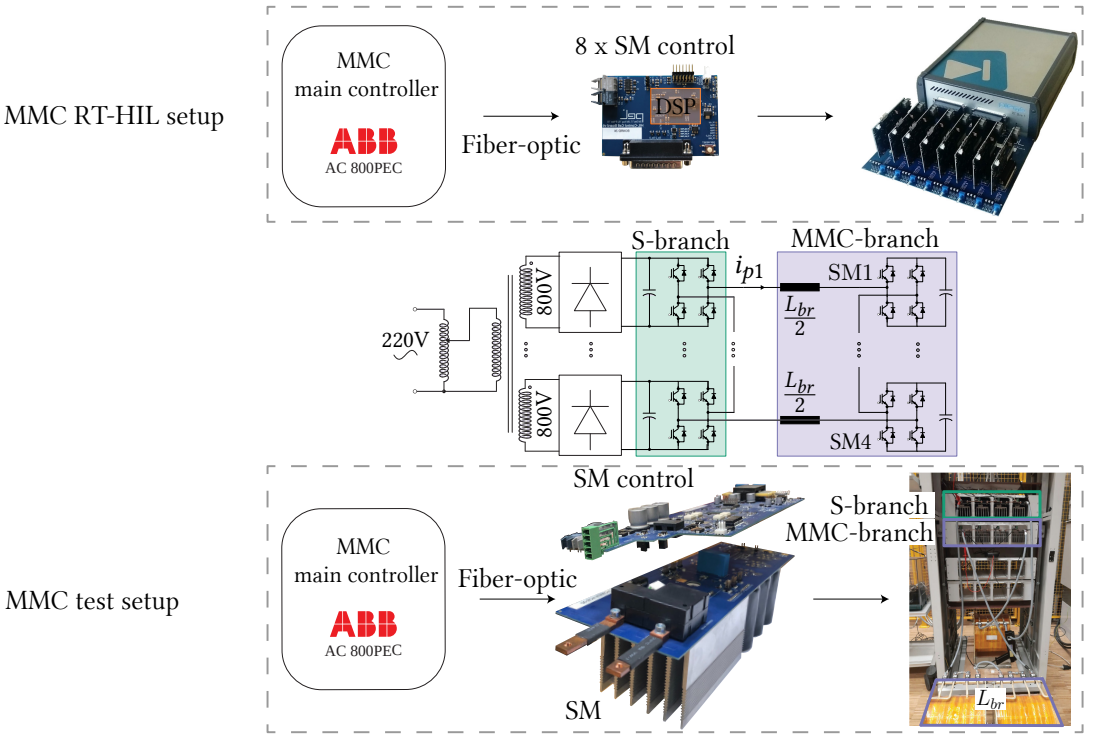


Fig. 4.7 Central picture shows the scheme of the MMC reduced branch. The top part presents the elements of the MMC RT-HIL setup. The DSP in each SM control board receives and sends the same signals as it would be operating in the SM prototype. Four DSP are loaded with the proposed CHM method as they are emulating the MMC-branch SMs controller. The RT-box simulates in the real-time the power components such as the IGBTs, dc-link capacitors, branch inductance and S-branch dc sources. The bottom part presents the components of the MMC test setup, where four SMs, loaded with the proposed CHM method, form the MMC-branch and other four SMs prototype form the S-branch.

It is important to highlight that ohmic losses in the capacitors foils, tabs, terminals, and electrolytes, mainly responsible for their temperature rise, are included in the ESR term, and its effect in the proposed method is taken into account as ESR is considered in the simulation conditions.

The MMC RT-HIL simulator was set at the equivalent MMC rated values, and the experiment was performed during 60 min. Every 5 s, a new capacitance estimation was available to be sent to the MMC main controller. **Fig. 4.8** presents the parameter estimation results for the conditions mentioned above, while **Fig. 4.9** presents the parameter estimation results for the equivalent MMC operating at different switching and ac port frequencies.

Results show that the CHM method performs satisfactorily for the different capacitors states, even when applied to a capacitance step-change. It is observed that variations in the switching and terminals frequencies have a moderate impact on the performance of the estimation, being the worst case when the switching frequency is reduced to half and the terminals frequency is double. In addition, it can be deduced that the switching frequency reduction has less impact than ac terminals frequency increase. This outcome can be explained by observing **Fig. 4.4**. As the fundamental frequency increases, the ESR component of the impedance increases while the capacitive part decreases, and the impedance

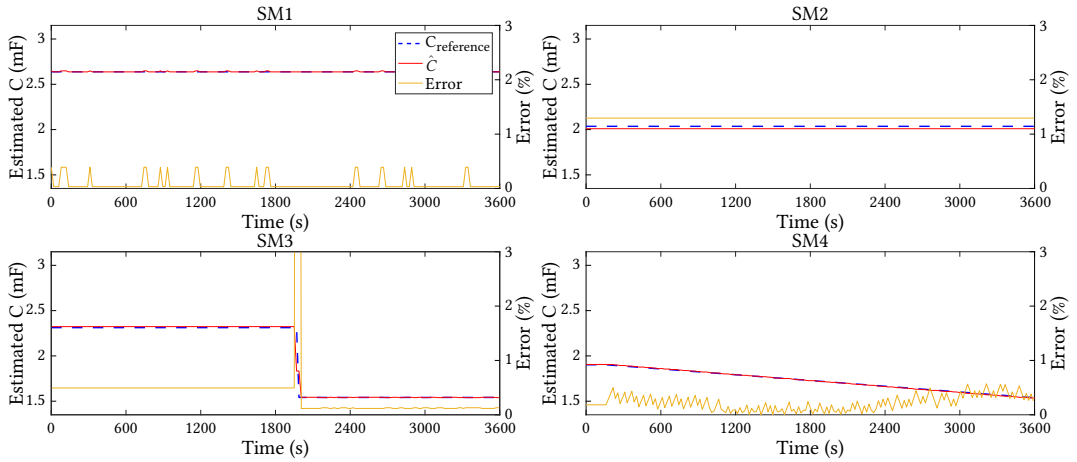


Fig. 4.8 Parameter estimation results for the MMC RT-HIL simulator. The dashed red lines is the reference capacitance value. The continuous red lines is the estimated capacitance, respectively. The continuous yellow line is the estimated percentage error. Each SM is set with different reference capacitance and ESR to demonstrate the proposed method capacitance track capability.

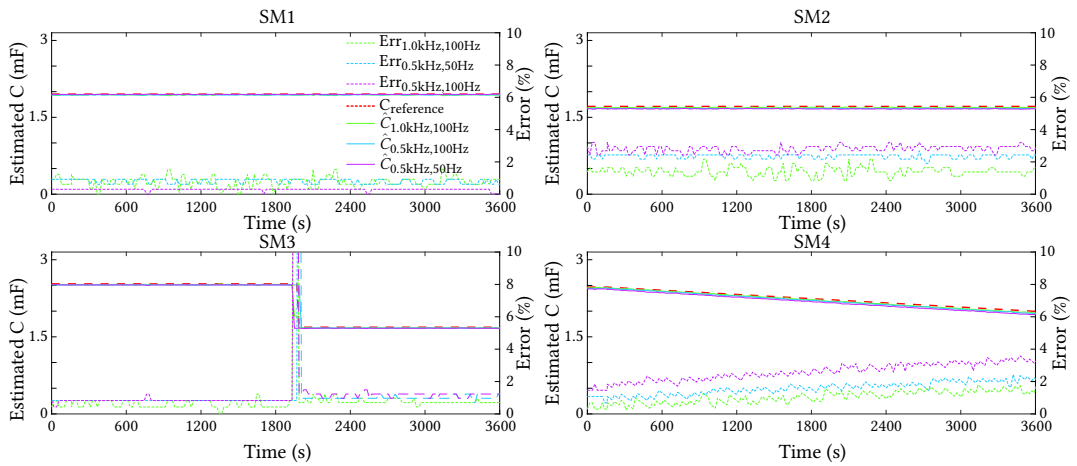


Fig. 4.9 Parameter estimation results for the MMC RT-HIL simulator under different MMC switching and equivalent ac terminals frequencies. The dashed red line is the reference capacitance value. The colored continuous and dashed lines are the estimated capacitance, and its error, respectively.

magnitude is reduced. On the other hand, a reduction in the switching frequency increases the ESR component; however, the impedance magnitude is still highly attenuated. Finally, the presented results prove that the proposed method does not interfere with other routines running in the SM local controller, and it is numerically stable within time, frequency, and impedance variations, as no divergence nor undefined values were found.

4.5.4 MMC experimental test

The MMC test setup, depicted in the bottom part of **Fig. 4.7**, comprises four series-connected SMs in series with a 2.5 mH inductor to form the MMC-branch. The S-branch is made of four SMs series-connected. The S-branch dc sources are made of an isolating transformer with one primary and four

secondary windings supplying four full-wave diode rectifiers. The primary side of the transformer is supplied by a single-phase autotransformer (VARIAC). The MMC main controller is based on the industrial controller ABB AC 800PEC, a custom-made serial protocol and a fiber-optical link to exchange information with either the developed SMs or SM control boards.

Four experiments were conducted with the SMs operating close to nominal. In the first two experiments, all the SMs were with the full dc-link capacitor bank; however, one experiment was carried out with $\varphi = 90°$ and the other with φ varying from 0° to 90°. In the last two experiments, one-third of the capacitors were removed from the SM1 dc-link. In addition, to reduce the temperature effect on the measurements, the experiment was running for an hour prior to the data being taken. **Fig. 4.10** shows the parameter estimation results for the MMC test setup. Plot a) presents the S-branch and MMC-branch voltage, and the branch current waveforms. Plot b) presents v_{sm}^{dc} measurement and reconstructed i_{sm}^{dc} retrieved from SM1. Plots c) and e) show the results considering all the SMs capacitor bank fully populated, while plots d) and f) show the results considering that one-third of the SM1 capacitor bank was removed. Plots c) and d) show the results with $\varphi = 90°$, while plots e) and f) the results with φ varying from 0° to 90°.

Consistent with the results found in the MMC RT-HIL simulator, the proposed CHM detected, in average, 32% capacitance drop which matches with the one-third of capacitors removed (plot d)). On

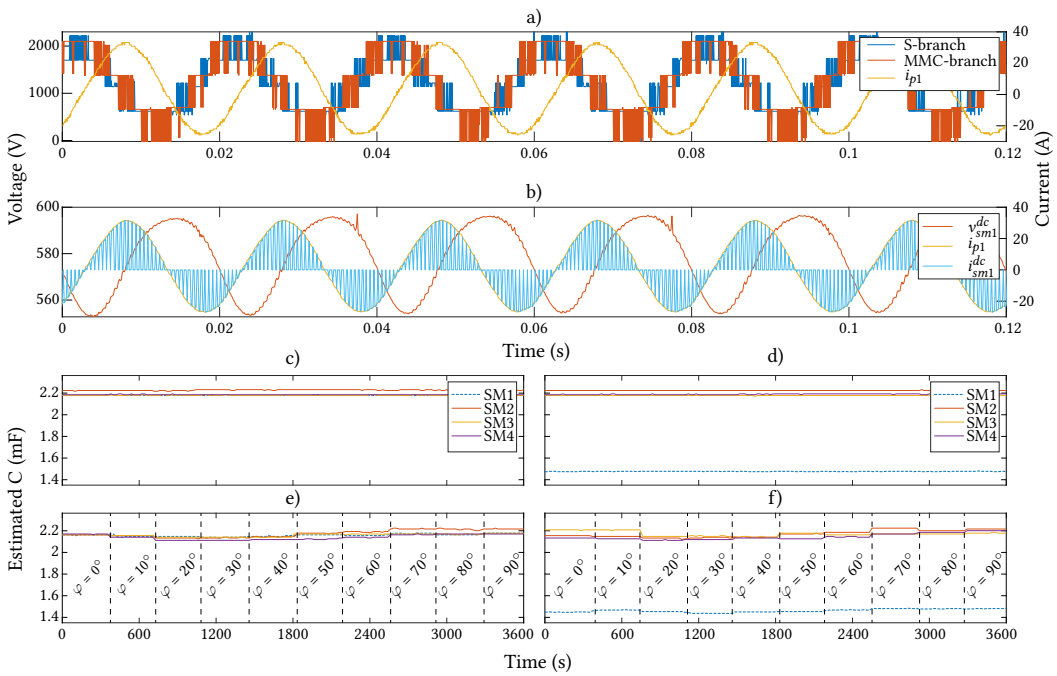


Fig. 4.10 MMC test setup results. Tests were carried out during 60 min, branch current set at 65 A peak-to-peak, $m(t) = 0.7$ and $v_{sm}^{dc} = 600$ V. a), the S-branch, MMC-branch and branch current waveforms recorded from scope with the SMs capacitor bank fully populated. b), the measured v_{sm}^{dc} and reconstructed i_{sm}^{dc} retrieved from SM1 DSP, with the capacitor bank fully populated. c), the SMs dc-link capacitance estimation results for capacitor bank fully populated and $\varphi = 90°$. d), the SMs dc-link capacitance estimation results for capacitor bank reduced one-third and with $\varphi = 90°$. e), the SMs dc-link capacitance estimation results for capacitor bank fully populated and φ varying from 0° to 90°. f) presents SMs dc-link capacitance estimation results for capacitor bank reduced one-third and with φ varying from 0° to 90°.

the other hand, when the power factor is changed, it can be seen that the capacitance estimation reduces its accuracy, specially when $\varphi < 60°$ as was suggested in **Sec. 4.2**; however, the error concerning the cases where $\varphi = 90°$ is less than 5 %.

4.6 Conclusions

Despite the extraordinary features of MMC topology, reliability could be of concern since several sensitive and expensive components are present in the SM. The CHM technique might improve converter reliability by monitoring state conditions over selected critical components before severe deterioration or significant failure occurs. This chapter presented an MMC SM dc-link capacitor CHM method, addressing its mathematical development, application scope, and practical considerations. In addition, offline simulations and MMC RT-HIL and MMC experiments were carried out to validate the proposed scheme under different SM dc-link impedance conditions and power factors. Results showed that using available SM measurements and the RWLS simple technique, it is possible to extract the SM dc-link capacitance with a maximum error below 5%, even under extreme capacitance change conditions and different converter power factors.

Continuing with the goals of this thesis, the following chapter presents a strategy to extract relevant information about SM sub-circuit states, enabling the path toward new SM-level CHM methods.

5
Estimating the ASPS Power Consumption

The previous chapter presented a method for the MMC SM CHM of power capacitors to improve converter reliability, as capacitors are usually considered one of the most sensitive components in power electronics applications. However, despite the FB SM is a well-known and straightforward power converter topology, in practice, it is a complex device composed of several parts presenting perhaps, lower failure rates compared to capacitors and power semiconductors, but equally important for the SM to operate appropriately. The limitations to monitoring their health conditions are, at least, the volume/cost impediments to consider more sensors/acquisition system, and computational power resources. Thus, exploring alternatives in which valuable information can be extracted from the SM using the same existing means becomes interesting for increasing CHM value when applied to MMC. This chapter presents a novel strategy to observe simultaneously different SM sub-circuits condition through the ASPS power consumption monitoring. The fundamental idea is that ASPS secondary circuitry changes produce a power signature different from the one during regular operation in the primary side. A CHM strategy using this information is proposed, illustrating how new prospective condition health monitoring schemes might be created. Presented ideas are mathematically developed, simulated and experimentally tested in the context of the considered MMC.

5.1 Motivation

As presented in **Chap. 2**, CHM applied to power electronics devices is mainly focused on power semiconductors and capacitors, leaving out of the scope many other electronic components that are less sensitive; however, of the same importance for the proper operation of any equipment. In the case of MMC, this trend is not different and can be illustrated considering the SM presented in **Chap. 3** (cf. **Fig. 3.23** and **Fig. 3.24**). Apart from the IGBT module and six power capacitors, the SM comprises an electromechanical component (REL), several low-voltage capacitors (electrolytic and tantalum), resistors, low-current inductors, low-power semiconductors (MOSFET, thyristors, transistors and diodes), optical-based (optoisolators, gate-driver ICs), LEDs, magnetics (ASPS multi-windings coupled inductor and THY pulse transformer), ICs (processor, memory, OPAMPs, logic-gates and PWM controller), oscillator (DSP clock), connectors (connection between PCBs and from PCB to components, e.g., REL), mechanics (screws and cooper terminals), and PCBs (ASPS multi-windings coupled inductor, power PCB and control PCB). As summarized in **Tab. 5.1**, the elements per SM sum 414 and approximately 20000 parts per MMC (considering only SM's parts).

The fundamental reason these components not being monitored might be the extra cost, volume, and complexity of adding more elements to the SM to gather and process information about them. Moreover, reliability may worsen due to the counter-effect of having more parts prone to failure. On the other hand, seeking cheap and straightforward solutions, classical MMC SM (either HB or FB) usually considers a minimum set of electronics (sensors and computational power) such that

Tab. 5.1 Summary electronics components per SM

Component/circuitry	Full-bridge	Dc-link	Balancing	Protection	Gate-drivers	Local controller	Measurement	ASPS
Power semiconductors	4			1				
Power capacitors		6						
Electro-mechanics				1				
Low-power capacitors		1		20	20	46	9	25
Resistors			9	38	24	24	37	45
Low-current inductors						2		4
Low-power semiconductors			2	27				14
Optical-based				2	4			
LEDs						3		
Magnetics				1				1
ICs				1		10	6	1
Oscillator						1		
Connectors				3	4	5	2	2
Mechanics	5			1				
PCBs	1					1		1
N° components	10	7	11	95	52	92	54	93
N° components per SM	414							
N° components per MMC (48 SMs)	**19872**							

the device performs as expected, limiting drastically what can be done regarding CHM. In this scenario, it is interesting to explore alternatives to improve CHM techniques considering acquiring new and valuable information about the SM condition, ideally, using common available SM resources (sensors and computational power), and then processing it accordingly to correctly recognize that a degradation threshold is over passed.

In this chapter, the presented problem is addressed considering two layers. The first layer is an alternative to procure SM sub-circuits information that can be linked to to their component's degradation level. It is proposed to use the power consumption of the ASPS as a measurable signature able to reflect the parametric fault of the circuits being supplied by it. The parametric fault (also known as soft fault or parametric shifting) is the deviation in circuit component parameters from their initial values and beyond their acceptable tolerance range [145], [146]. As discussed later in this chapter, the potential use of the first layer outcome to create a CHM method is explored and implemented as the second layer. Depending of chosen technique to analyze first layer output, different second layer solutions might be provided. In particular, to illustrate second layer options, a CHM method is developed using a tailored fault dictionary at the SM level to recognize that observed SM is degraded.

In what follows, both layers are introduced in detail and validated through offline simulations and experimental results in the developed SM.

5.2 First layer: ASPS power consumption estimation

As a recourse to fully utilize the available SM sensing and processing hardware, it is proposed to use the ASPS power consumption as a measurable signal able to capture the parametric changes of the circuits connected to its outputs, enabling that several components might be monitored at the same time. Already presented in **Chap. 3**, the considered ASPS is a single switch flyback-based converter

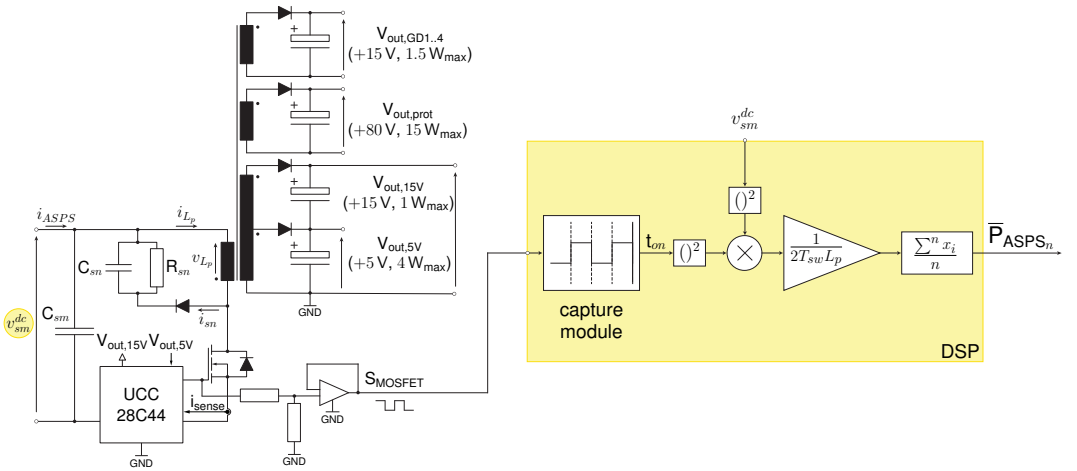


Fig. 5.1 Highlighted yellow, the proposed method for ASPS power consumption estimation and its integration to the ASPS. Available v_{sm}^{dc} measurement and MOSFET gate pulses (scaled/adapted with a few low-cost extra components and acquired with the DSP ECAP) are utilized. Result is the mean power $\overline{P}_{\text{ASPS}}$.

with multiple isolated outputs. This section introduces a simple strategy to estimate changes in the ASPS power consumption and its validity as first layer is demonstrated through several experimental tests.

The principles of flyback converter operation are well known, and it is not difficult to establish a link between control duty cycle, supply voltage and input power. When the flyback power switch is conducting, the ASPS input voltage v_{sm}^{dc} produces a voltage v_{L_p} in the primary inductor (cf. **Fig. 5.1**). As a consequence, a current i_{L_p} flows through the primary coil, which is limited by its magnetizing inductance L_p and increases linearly with $v_{L_p}(t)/L_p$ slope (cf. **Fig. 5.2**). As it is intended to detect power consumption changes and for the sake of analysis simplicity, it is assumed that flyback primary side power losses and voltage drop due to input filters and MOSFET are negligible then ,v_{L_p} and i_{L_p} can be approximated by v_{sm}^{dc} and the ASPS input current i_{ASPS}, respectively. Then, i_{ASPS} can be written as (5.1).

$$i_{\text{ASPS}} \approx \frac{v_{sm}^{dc}}{L_p} t, \quad t \in [0, t_{on}], \tag{5.1}$$

where t_{on} is the total time the MOSFET is conducting. Due to SM dc-link large capacitance C_{sm}, $v_{sm}^{dc}(t)$ can be considered constant during the whole MOSFET switching period T_{sw}. Until $t = t_{on}$, the output diodes are reverse polarized, preventing the current to flow from the secondary windings to the output capacitors, thus an input energy $E_p = 0.5 L_p i_p^2$ is delivered to the magnetic circuit and stored, mainly, in the core air gap, where i_p is i_{L_p} at $t = t_{on}$. Considering discontinous conduction mode, when the MOSFET is off, the secondary windings reverse their polarity and a large portion of the energy stored in the magnetic circuit is transferred to the secondaries before the MOSFET switching period is reached, charging the output capacitors and supplying the load. Then, the ASPS stored energy can be approximated by

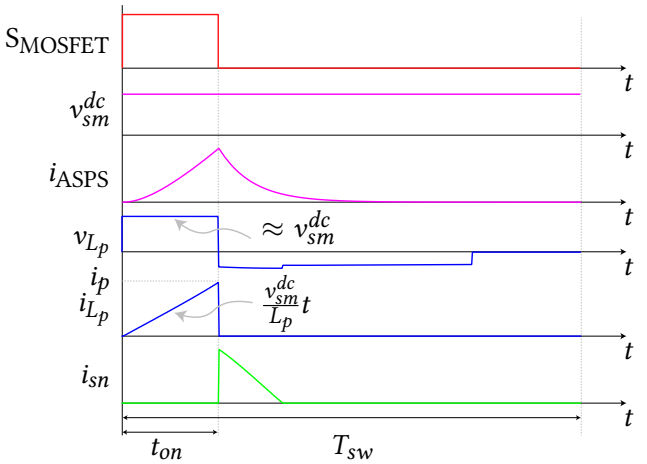


Fig. 5.2 Main ASPS primary waveforms. Secondary side waveforms are not shown as they are not used for power consumption calculation. Once MOSFET starts conducting ($S_{MOSFET} = 1$), a voltage v_{L_p} is applied to the inductor primary side and, consequently, a current i_{Lp} flows through it until $t = t_{on}$. v_{L_p} and i_{ASPS} can be approximated by v_{sm}^{dc} and i_{L_p}, respectively.

$$E_p = \frac{1}{2}L_p i_p^2 \approx \frac{1}{2}L_p\left(\frac{v_{sm}^{dc}}{L_p}t_{on}\right)^2 \approx \overline{P}_{ASPS}T_{sw} \tag{5.2}$$

where $\overline{P}_{ASPS}$ is the ASPS mean input power over the switching period T_{sw}. Finally, rewriting (5.2) yields

$$\overline{P}_{ASPS} \approx \frac{1}{2}\frac{(v_{sm}^{dc}t_{on})^2}{T_{sw}Lp}. \tag{5.3}$$

Due to the imperfect magnetic coupling between the primary and secondary coils, a small portion of the energy transferred to the magnetic core during t_{on} is not captured by the output windings, but it is still present in the magnetic circuit. This is represented through a leakage inductor in series with the primary coil. Then, right after the MOSFET stops conducting, this leakage magnetic energy is returned to the primary side, reflected as a negative v_{L_p} and the current i_{sn}, and dissipated by the R_{sn}-C_{sn} snubber circuit. Thus, expression (5.3) already considers this effect and no extra energy has to be taken into account.

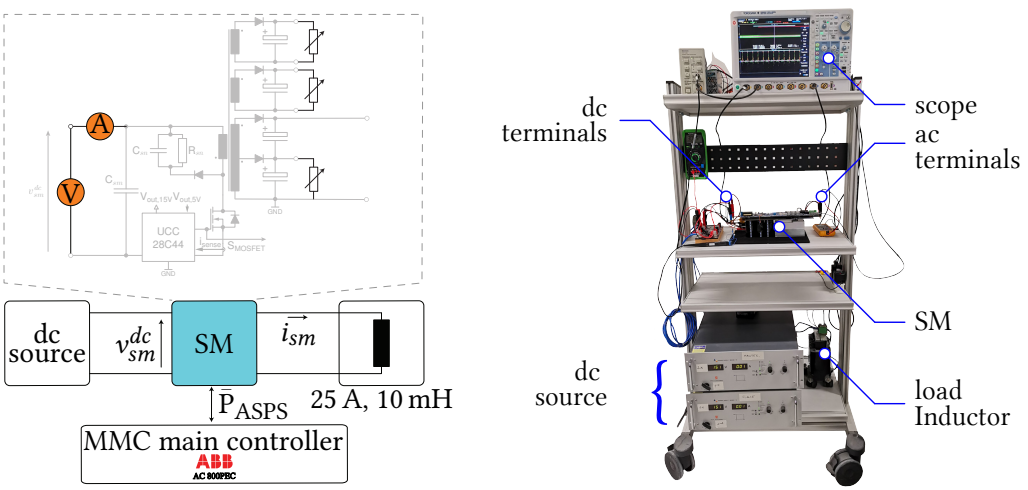
It is important to mention that despite the signal i_{sense} is measured through a shunt resistor and might help estimating the ASPS consumption, it is only used as a feedback by the PWM controller and the DSP does not acquire it. Instead, v_{sm}^{dc} (available in the SM local controller for specific control and protection actions), and t_{on}, are used to estimate the ASPS consumption according to (5.3). t_{on} is estimated measuring the active time of the MOSFET firing pulse (S_{MOSFET}) using the DSP capture module (ECAP) (cf. **Fig. 5.1**). Please note that the MOSFET pulse measurement circuit is not commonly available in the SM designs, however can be easily implemented with few low-cost components.

5.2.1 Method validation

To validate proposed ASPS consumption estimation method, it is considered the experimental setup presented in **Fig. 5.3**. A single SM whose dc-link is connected to two series connected Delta Elektronika SM600-10 dc power supplies through auxiliary dc terminals, and a 10 mH inductor, connected to its ac terminals. The SM synthesizes terminal voltage using unipolar modulation at 1 kHz switching frequency, and the output current is not controlled, but simply circulates through the inductor. It is considered that the equivalent converter operates at nominal values, balanced and without distortion ac port currents, input/output steady-state power balance and zero circulating currents. In addition, due to the pure inductive load in the experimental setup, no active power can be delivered, thus the current flowing through the SMs terminal within a branch of any leg, e.g., a of the upper branch, (3.13) (derived in **Chap. 3**), contains only the ac component and φ is close to $\pi/2$.

The MOSFET firing pulses are acquired every 50 µs (20 kHz) by the DSP-based local controller using its ECAP and used to estimate t_{on}, while the SM dc-link voltage is sampled at 40 kHz by the DSP. Despite the DSP ADC and ECAP sampling time are not the same and results are not necessarily synchronized, the difference between the voltage value during T_{sw} and the one stored in the memory is negligible as v_{sm}^{dc} variation is much slower compared to S_{MOSFET} duty cycle changes. Once t_{on} is available, $n = 10$ $\overline{\mathrm{P}}_{\mathrm{ASPS}}$ estimations are performed, averaged and sent to the main controller through the communication system. On the other hand, a scope monitoring the ASPS input voltage (v_{sm}^{dc}) and current is used to compare actual and estimated consumption.

The presented configuration allows to the SM to operate in the states depicted in **Fig. 5.4**. During passive charging none of the sub-circuits can operate as the ASPS has not reached the minimum input voltage to turn on. Once $v_{sm}^{dc} \geq v_{sm_{\min}}^{dc}$, the SM is in passively charged state, allowing the ASPS to



(a) (b)

Fig. 5.3 Experimental setup. (a) electrical diagram: a single SM supplied through auxiliary dc terminals and loaded with an inductor at the ac terminals. Highlighted in orange, the scope voltage (V) and current (A) probes. The ASPS power consumption is varied choosing different SM states and connecting a resistive load in the $V_{\mathrm{out,5V}}$. (b) laboratory experimental setup: two series connected Delta Elektronika SM600-10 as dc power supply, SM, a 10 mH inductive load and an ABB AC 800PEC controller (not visible in the picture).

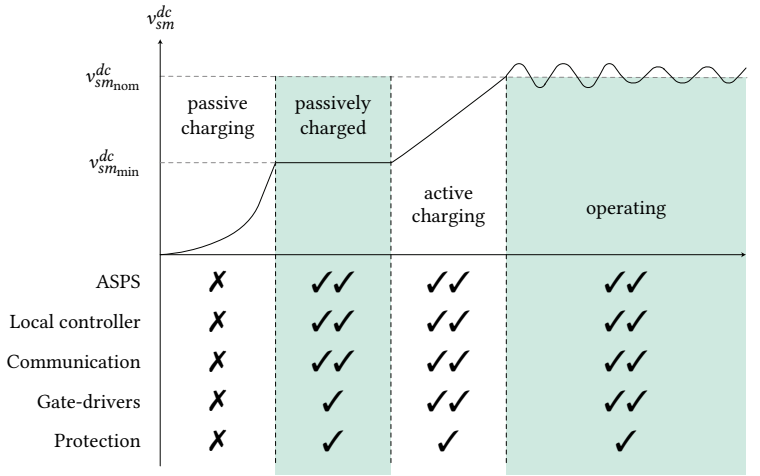


Fig. 5.4 SM sub-circuits use with respect to its state and dc-link voltage. A single check mark means the associate sub-circuit is available for operation. The double check mark means the associate sub-circuit is operating. During converter start-up, the pre-charge system allows the SMs to reach $v_{sm}^{dc} \approx v_{sm_{\text{min}}}^{dc}$ (passively charged state), powering up the ASPS. The ASPS supplies the DSP-based local controller and enables protection and gate drivers circuits. By using the power switches, the SM is actively charged, taking power from the associated branch until $v_{sm}^{dc} \approx v_{sm_{\text{nom}}}^{dc}$, and activating the operating state in which the SM is ready to follow voltage references from MMC main controller.

supply the DSP-based local controller and the communication circuitry (gate-drivers and protection circuitry are available). Afterward, SM modulation, and basic control actions are enabled permitting the active charging of its dc-link until $v_{sm_{\text{nom}}}^{dc}$ is reached. Then, the SM is in operating state, ready to receive a voltage reference and operates exchanging power within the converter. It is important to mention that protection circuitry is considered as it can be triggered any time during the SM operation.

It is important to mention that this experimental setup does not mimic precisely the conditions of the SM operating in the MMC; however, for what is sought to be demonstrated, any difference can be neglected.

5.2.2 Results

In order to assess the ASPS power consumption variation when electrical changes occur in its secondary windings, and taking into consideration the presented experimental setup, the following conditions are investigated:

① $\bar{\text{P}}_{\text{ASPS}}$ at baseline condition. DSP-based local controller and communication are active,

② $\bar{\text{P}}_{\text{ASPS}}$ when a small resistive load is added to the $\text{V}_{\text{out,5V}}$ circuit,

③ $\bar{\text{P}}_{\text{ASPS}}$ when the PWM is activated and i_{sm} =10 A, and

④ $\bar{\text{P}}_{\text{ASPS}}$ when protection is triggered (THY and both THY + REL).

Each one of these conditions is explored in passively charged and operating states. In passively charged, $v_{sm_{min}}^{dc}$ is set to 300 V, while in the operating state, $v_{sm_{nom}}^{dc}$ is set to 650 V. **Fig. 5.5** and **Fig. 5.6** present the results for both conditions. The cases from ① to ③ are concatenated to show the difference

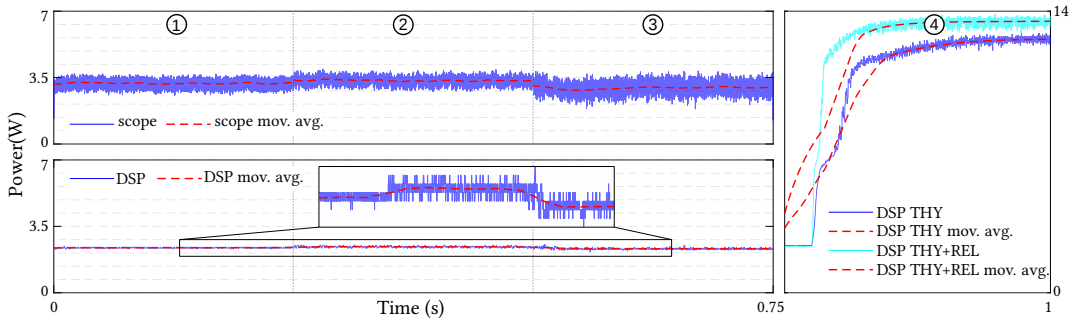


Fig. 5.5 Experimental results at passively charged state (300 V) for each studied case. Top left plot shows the ASPS average input power measured with the scope. Bottom left and right plots show the DSP ASPS average input power estimated using the explained method. The results are presented as a raw data (blue) and moving average (dash red line).

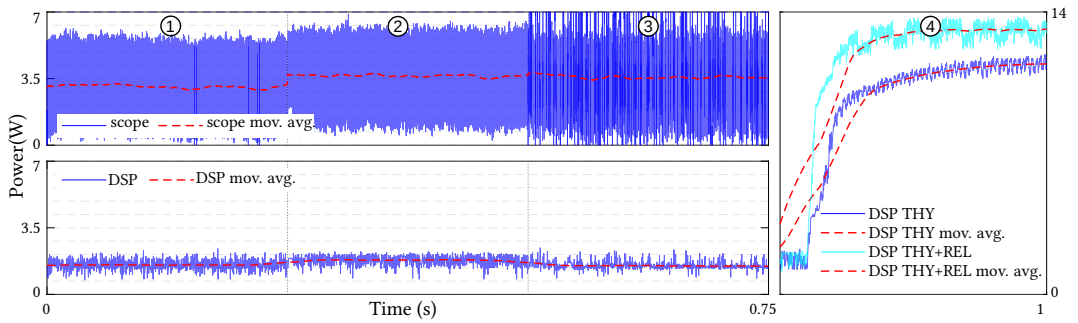


Fig. 5.6 Experimental results at operating state (650 V) for each studied case. Top left plot shows the ASPS average input power measured with the scope. Bottom left and right plots show the DSP ASPS average input power estimated using the explained method. The results are presented as a raw data (blue) and moving average (dash red line).

between them, while case ④ is presented in a different plot for clarity. Due to the characteristics of SM protection devices, case ④ shows results for THY and THY + REL activation. In addition, results are presented together with their moving average.

In the passively charged state (cf. **Fig. 5.5**), on average, the power measured by the scope is approximately 1 W larger than the estimated by the method, representing a relative error between 22% and 28% (cf. **Tab. 5.2**). Notably, the relative error in case ④ decreases considerably to less than 6% during THY or THY+REL activation. Another important observation is the sensitivity of the proposed idea in case ②, where a resistive load of 48 mW was added to the $V_{out,5V}$, and case ③, where the $V_{out,GD1..4}$ outputs supply the IGBT gate driver circuits while the IGBTs are switching and supplying the inductive load with 10 A. According to **Tab. 5.2**, the power difference between cases ② and ① matches the connected load in the $V_{out,5V}$.

Concerning case ③, interestingly, when PWM is activated, DSP measures slight power reduction, which is consistent with scope measurements. The gate driver consumption is generally very low at 1 kHz switching, and noise appears to impact calculations performed in the DSP.

For operating state results, similar observations are found (power estimation trend with the proposed idea for each case); however, a particular situation is highlighted. The proposed method results for

Tab. 5.2 Results summary. Average value per case.

State	Case	①	②	③	④	
Pas. charged	$\bar{P}_{ASPS}$ scope (W)	3.20	3.34	2.95	THY	13.05
					THY+REL	14.30
	$\bar{P}_{ASPS}$ DSP (W)	2.37	2.42	2.31	THY	12.59
					THY+REL	13.49
	Abs. error (W)	0.83	0.92	1.04	THY	0.46
					THY+REL	0.81
	Rel. error (%)	25.94	27.54	21.69	THY	3.52
					THY+REL	5.66
Operating	$\bar{P}_{ASPS}$ scope (W)	3.07	3.64	3.58	THY	13.39
					THY+REL	14.38
	$\bar{P}_{ASPS}$ DSP (W)	1.54	1.80	1.50	THY	11.40
					THY+REL	13.08
	Abs. error (W)	1.53	1.84	2.08	THY	1.99
					THY+REL	1.30
	Rel. Error (%)	49.84	50.55	58.10	THY	14.86
					THY+REL	9.04

the operating state, cases ①, ②, and ③, are up to 58% lower than scope results, which combined with up to 28% difference found in the previous state, make one considers two leading causes. The first is that the proposed method does not consider primary side losses, especially those dependent on the voltage, such as capacitor ESR, primary coil and snubber network. The second cause is the S_{MOSFET} duty cycle reduction due to primary inductor current reduction when ASPS input voltage increases. According to (5.2), t_{on} has to be half when v_{sm}^{dc} is double to transfer the same power. Then, shorter pulses are more challenging to acquire by the DSP, especially when the duty cycle is lower than 5% and switching noise, coming from MOSFET (higher dv/dt) and IGBT operation, distort the S_{MOSFET} signal. Once ASPS load increases, as when protection devices are triggered (③), power estimation improves considerably, showing that the method is, in fact, sensitive to duty-cycle.

Despite the considerable difference between the scope and method results, it can be claimed that $\bar{P}_{ASPS}$ estimation tracks the actual ASPS consumption trend reasonably well, recognizing a specific power signature for each observed SM operating state. In the light of this outcome, more elaborated SM monitoring strategies performed locally in the SM or at the MMC-level fed by the SMs information might be explored, enabling the second layer of the complete CHM scheme. Evidently, a second layer might take different forms depending of the strategy to analyze the first layer outcome. For instance, local strategies based on detecting abnormal ASPS consumption during passively charged or operating state can help to detect incipient SM deterioration (or failure) before any power is actively exchanged within the converter or during regular operation, respectively. Moreover, advanced approaches based on machine learning techniques might recognize and provide specific information for each secondary winding load, focusing on and facilitating maintenance and repairing of SM particular circuits or components. On the other hand, a MMC-level approach, where simple information collected by the SMs is sent to the converter controller, or a specialized processing unit to perform complex algorithms, might be a solution as well. For instance, considering the 48 SMs of presented research platform, each

one sending back the ASPS estimated consumption. Then, for a given SM state, one might expect that the ASPS present a similar consumption signature, making it not difficult to recognize, employing an appropriate mathematical tool, the SM or a set of them operating differently.

Independently of the selected strategy to analyze first layer outcome, one should consider, at least, three aspects to elaborate the second part of the CHM scheme: **a)** first layer outcome threshold level at which the SM is considered degraded, as ASPS secondary winding circuits present parameter tolerances, **b)** ASPS consumption estimation noise, as direct comparison between threshold level and noisy consumption estimation might result in a false alarm, and **c)** method complexity, so that chosen strategy can be deployed in the SM or MMC controller.

Following section proposes an alternative to construct the second layer in order to complete the CHM strategy.

5.3 Second layer: ASPS consumption based CHM

The construction of the second layer, for this case, might be compared with the analysis of an analog circuit for fault detection. The study of parametric and hard faults in analog circuits has been largely investigated since the 1970s, as analog circuits were considered the most unreliable and least testable elements in electronics products [147]. Today, despite digital components dominating electronic systems, analog elements are highly used, creating complex mixed devices that are difficult to analyze, especially during manufacturing [146], [148]. The challenges settle in, similarly to power electronics devices, measurement restriction (e.g., testing points and or appropriate sensing capacity), component tolerances, the lack of proper fault models, and the non-linearity nature of circuits [147]. Proposed approaches are mainly based on circuit theory and signal processing [148]–[150], various branches of mathematics [151]–[153] and artificial intelligence concepts [154]–[156]. For instance, the authors in [148] propose a method for a single fault diagnostic of different linear analog circuits, including both parametric and catastrophic faults. The deviations of the parameters of the passive and active faulty elements are represented by extra current and voltage sources. The unknown sources are determined in the frequency domain using measurements of two circuit nodes at two different frequencies. Then, parameters deviation are derived and compared with the nominal (healthy) circuit. In [151], a technique for degradation detection in an electronic product's performance is proposed using Mahalanobis distance. The Mahalanobis distance is a classification technique capable of system-level anomaly detection in multivariate, data-rich environments [157] which uses normalized performance parameters of a healthy system to create a correlation matrix (Mahalanobis space) representing a baseline for comparison with the Mahalanobis distance of the observed system. Using this mathematical approach, a small Mahalanobis distance value represents a healthy system. On the other hand, an ANN seems more appealing to deal with circuit modeling issues, component tolerances and nonlinear effects as no circuit model or comprehensive understanding are required. Presented in [154], a neural network is used for fault diagnosis, which has been previously trained with an optimal set of information obtained from the wavelet decomposition [157] of the circuit output, reducing the training and testing data considerably.

Despite the wide variety of techniques to detect circuit faults, the majority of them require conditions and assumptions not necessarily available in the case of studied ASPS, for instance, a minimum number of testing points, circuit reconfiguration, input/output signal injection, or enough computational power to run complex algorithms, making these strategies not suitable solutions for the described

Tab. 5.3 ASPS consumption analysis

ASPS sub-circuit	Component type	Quantity	Voltage (V)	Current (mA)			Power (mW)		
				Min.	Typical	Max.	Min.	Typical	Max.
$V_{Vout,5V}$	DSP_{IC}	5	5	19	20	21	475	500	525
	DSP_{EEPROM}	1		0.9	1	1.1	5	5	6
	DSP	1		206	242	277	1030	1210	1385
	COM_{TX}	1		15	20	30	75	100	150
	COM_{RX}	1		15	20	30	75	100	150
	COM_{IC}	1		19	20	21	95	100	105
$V_{out,GD1..4}$	GD_{IC}^{prim}	4	5	0	2.5	5	0	50	100
	GD_{IC}^{sec}	4	16	0	2.5	5	0	160	320
Total ASPS consumption (mW)							1755	2225	2741

problem. However, the presented ideas are interesting and inspiring. For instance, in [145], [152], [158], different methods have been used to extract abnormal circuit signal patterns and compare them with values or patterns stored in a fault dictionary to recognize component/circuit faults and failure. A fault dictionary is a look-up table consisting of fault-free and or faulty cases of the observed circuit, created by simulations and or experimental tests [159]. The advantage of the fault dictionary approach is that expert knowledge of the analyzed circuit might be used to recognize likely fault situations, facilitating dictionary construction. However, pattern recognition is more challenging as, for instance, parameter variation of single or multiple components might result in slightly or non-linear changes in the analyzed signal, requiring complex mathematical techniques. In the case of studied ASPS, the idea of a fault dictionary can be easily introduced since analyzed signal ($\bar{P}_{ASPS}$), compared with common analog circuit fault detection state-of-the-art, is quite simple (dc) and contaminated mostly with electrical noise coming from the SM power stage and ASPS flyback switching events (high frequency). Moreover, a fault dictionary, for instance, might be constructed directly from sensitivity analysis of studied circuits and states.

Therefore, the first example of a second layer for the ASPS consumption estimation consists of its direct comparison to a threshold level. The $\bar{P}_{ASPS}$ is first filtered using a moving average filter (pattern recognition equivalent) and compared to a predefined limit (fault dictionary equivalent). Then, the second layer reduces to find a reasonable ASPS consumption range in which the SM can be considered operating normal (or degraded). The ASPS consumption range might be found through testing the SMs (as presented in the previous section, where power consumption estimation is not accurate but similar among SMs) or using the technical documentation of the components and assuming power consumption estimation is accurate as it is explained hereafter. Let us consider the ASPS extended circuit in **Fig. 5.7**. The $V_{Vout,5V}$ output supplies two sections: DSP and communication (COM). Both sections possess ICs (e.g., logic gates) and passive components. In the DSP section, the DSP is the element consuming the most power. As one might expect, its consumption is strongly related to the peripherals and settings defined for a specific application. According to its technical documentation, the DSP current consumption range is 236 mA to 307 mA; however, in the studied case, a more acceptable range is 206 mA to 277 mA due to, for instance, CAN, USB, I2C, eQEP along other modules are not used. ICs, on the other hand, can be considered in the 19 mA to 21 mA range, which is typical consumption for CMOS logic gates. FOL connectors (COM_{TX} and COM_{RX}) operate in

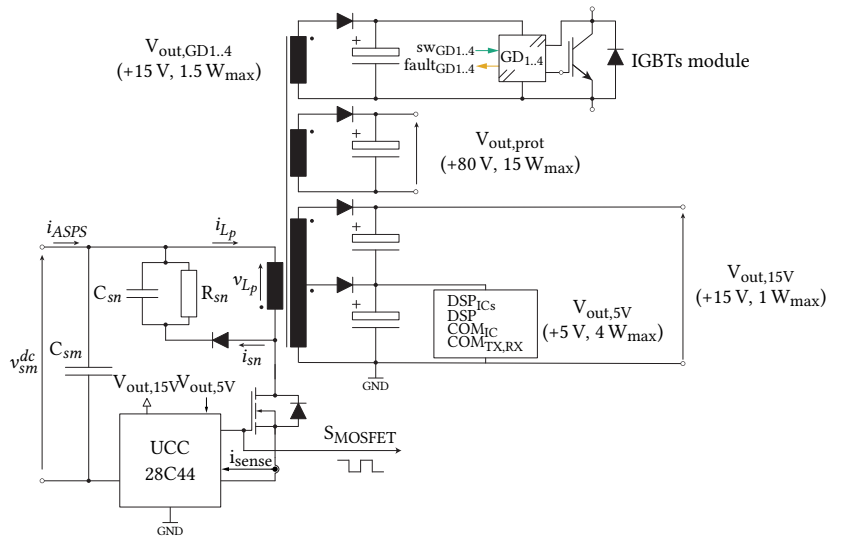


Fig. 5.7 ASPS scheme with $V_{out,5V}$ and $V_{Vout,GD1..4}$ simplified sub-circuits connected. In the $V_{out,GD1..4}$ circuits, the gate-driver IC is supplied on its primary (5 V) and secondary (15 V) sides. When switching, an extra consumption exists due to primary side pulses and gate charging. Both effects are negligible compared to DSP consumption. On the other hand, the $V_{Vout,5V}$ circuit is loaded with ICs, FOL terminals and, DSP. The protection circuit in the $V_{Vout,prot}$ output is not considered during regular operation.

the range 15 mA to 30 mA. Then, the power seen from the $V_{Vout,5V}$ output ranges from 1755 mW to 2321 mW. In the case of $V_{Vout,GD1..4}$ circuits, each possess a gate-driver IC which supply consumption (whether is switching or not) is in the range of 0 mA to 5 mA for both primary (at 5 V) and secondary (16 V) sides. By assuming that power transfer from ASPS primary to secondary side is lossless, the calculated ASPS consumption at the primary side is in the range of 1700 mW to 2700 mW, with a typical consumption of 2208 mW, consistent with **Tab. 5.2** in the passively charged state. In the case of the operating state, it is considered that two gate-driver circuits are extra loading the circuit with the corresponding IGBT gate power (average). In the designed SM, the average gate power per IGBT is approximately 6.5 mW (considering 1 kHz switching frequency, V_{GE} =16 V gate-emitter voltage, and Q_G =410 nC gate charge), which is marginal compared with the other components' consumption and difficult to estimate when SM is in the operating state.

Finally, it is commonly utilized in circuit analysis that a 50% parameter value drifts from its nominal value, irrespective of its tolerance range, is considered degraded [160]. Similar logic is applied in this case, as presented in **Tab. 5.4** and depicted in **Fig. 5.8**, where an hypothetical situation is shown. From $t = 0$ to $t = t_1$, $\bar{P}_{ASPS}$ is close to the expected (typical) value within its tolerance range. At $t = t_1$, a component in the SM starts degrading. At $t = t_2$, estimated consumption enters a warning zone where maintenance might be not mandatory but desirable. At $t = t_3$, scheduled maintenance is performed, and the damaged component is replaced, returning $\bar{P}_{ASPS}$ to its initial condition. At $t = t_4$,

Tab. 5.4 ASPS consumption thresholds

	Deg. $Threshold_{min}$	$Tolerance_{min}$	Typical	$Tolerance_{max}$	Deg. $Threshold_{max}$
$\bar{P}_{ASPS}$ (mW)	1113	1755	2225	2741	3338

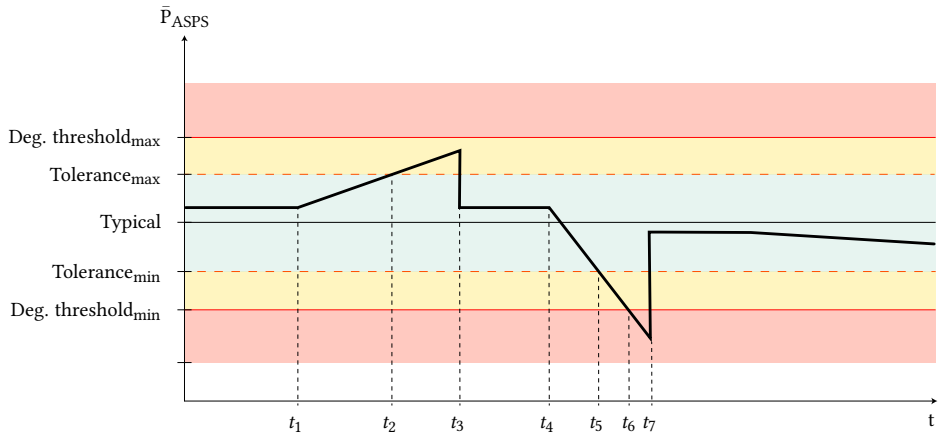


Fig. 5.8 Fault dictionary-based second layer illustration. Highlighted green is the $\bar{P}_{ASPS}$ tolerance range (device operating as expected). In the highlighted red section, the device is considered degraded. In between, highlighted yellow, is a warning zone that might be considered during preventive maintenance. Device starts degrading at $t = t_1$ and enters the warning zone at $t = t_2$. At $t = t_3$ device is repaired during scheduled maintenance before maximum degradation threshold is reached returning to original consumption. At $t = t_4$ device degrades again; however, maintenance was delayed until $t = t_7$ as no scheduled one was performed between $t = t_5$ and $t = t_6$. In both situations, failure was avoided.

a similar situation occurs; however, the damaged element is replaced at $t = t_7$ as no maintenance was scheduled between $t = t_5$ and $t = t_6$. In both cases, SM failure was avoided. Considering the presented approach, the following conclusions can be made:

- Proposed idea is simple and easy to implement as ASPS consumption is a constant value for a given SM state.
- Presented degradation thresholds allow to have a warning range in which SM is not considered degraded but out of expected operation range, providing additional information, for instance, to plane next maintenance task.
- A parametric fault in the $V_{out,5V}$ circuit is more likely to be detected compared to fault in one of the gate-driver circuits. This observation does not mean that, by means of another analysis technique, parametric fault detection in the gate-driver circuits might be performed with good results.
- The proposed idea does not provide degradation information about ASPS condition; however, might provide information whether it is operating or not using S_{MOSFET} pulses. Early detection of pulses loss gives enough time to the SM, for instance, to trigger local protections and or inform MMC main controller.
- Although protection circuit consumption is easily recognized by the proposed method, it only can happen when protection devices are triggered, making difficult to use this information as part of a preventive method. Instead, similarly to previous point, information collected during protection devices activation might be used to improve SM protection scheme. For instance, from the SM controller point of view, there is no means to judge whether the THY, REL or both where activated when the DSP or OVDC triggers the REL (please, keep in mind that the REL is always fired together with the THY).

5.4 Summary

CHM techniques applied to converter SM are gaining attention as monitoring failure precursor parameters can help estimate some selected components' deterioration state. Nevertheless, monitoring components usually require additional hardware and processing power, thus increasing the SM's cost, volume, and complexity, unless existing hardware and measurement capabilities are used differently.

This chapter presented a new approach to monitor the MMC SM condition based on observing the power consumption of the ASPS. A simple methodology was implemented in the SM DSP-based local controller and tested under different SM operating conditions. It was found that the proposed idea can recognize ASPS secondary power change satisfactorily. The method takes full advantage of observing the flyback regulator control pulses directly to recognize even small ASPS output power variations.

Compared with more classical alternatives such as adding a current sensor at the ASPS input or in series with the primary coil, this idea might represent a lower cost option and less processing power requirement as no digital filter to remove commutation noise or no extra calculations have to be done to remove ASPS primary side losses effect.

By using this information, a CHM strategy is proposed based on the concept of fault dictionary, where a look-up table consisting of fault-free and or faulty cases of the observed circuit is created. Through this simple example, it is claim that ASPS power consumption estimation to detect changes in the circuits loading its secondary side might enable new MMC SM CHM methods.

6
Towards MMC Condition Health Monitoring

Along with this thesis, it has been argued that CHM applied to MMC is mainly focused on selected components such as capacitors or power semiconductors. In order to utilize better measurement and processing power, the previous chapter presented a strategy to gather new information about the SM sub-circuits by monitoring the ASPS consumption, opening new CHM perspectives at the SM-level at a meager cost of hardware addition and computational burden. However, although existing methods provide valuable information about the SM condition, it is insufficient to assess the overall SM state of degradation as their nature, range, dynamic, and relevance, among other characteristics, are not subject to direct comparison. This chapter addresses the integration of existing health indicators to create a comprehensive converter and SM-level CHM strategy. The topic is tackled considering that health indicators merging is a featured-level data fusion problem that can be solved using multi-criteria decision-making techniques. Different methods are introduced and evaluated through collected experimental data, numerical examples, and offline simulations.

6.1 Motivation

Capturing weak light and waves with high resolution (sharpness and clarity) has been a centuries-long astronomers' problem, forcing them to seek telescopes with larger apertures. However, there are technical limitations in making large size telescopes as materials and mechanical constraints make the problem unaffordable beyond a certain diameter. One of the ideas to break through such impediments is to spread out multiple small-sized antennas over a large area and make them work together to function as a giant unit. A remarkable example is found at 5000 m over the sea level in the Chajnantor plateau in the Atacama desert, Chile, where the Atacama large millimeter/submillimeter array (ALMA) project, the most expensive ground-based telescope in operation, takes place. It uses 66 radio telescopes (54 twelve-meter antennas and 12 seven-meter antennas) to jointly observe electromagnetic radiation at millimeter and submillimeter wavelength under the principle of interferometry. When two antennas observe an object in the sky, they view it slightly differently, i.e., light from the object reaches one antenna before it reaches the other. When combined, they would overlap or interfere, blurring the signal. Nevertheless, by precisely timing the signal from each antenna, astronomers can correlate them, avoiding interference and allowing signals unification from many antennas and even many telescopes to create an image that is considerably brighter and sharper than what is possible from a single dish [161].

Like astronomers collect and integrate information from different sources (antennas) to achieve and improve observations of a distant object, this chapter seeks to present and discuss different techniques to merge multiple data sources (health indicators) to improve the assessment of SMs and or converter's health condition, providing a new condition monitoring perspective. Along with

this thesis, different health indicators have been introduced and investigated, such as the V_{ce}, T_j, C, and ASPS consumption, providing a rich set of data about observed devices. However, a single indicator or several of them without a proper analysis strategy is not necessarily sufficient to assess SM or converter's condition. This concern comes from the indicators presenting different natures and representing components (or sections of a device) whose degradation level might have different impacts on the device performance, making their comparison and merging a challenging problem (cf. **Fig. 6.1(a)**). For instance, a simple comparison between capacitor (capacitance) and IGBT (collector-emitter voltage) health indicators reveals that their sampling time, dynamic, trend, and threshold can differ. Capacitance is expected to decrease with time, its estimation might be performed once per day, and the degradation threshold is a 20% reduction. On the other hand, V_{ce} measuring could be performed every switching period, and, depending on the failure mechanism, its value might increase or decrease by just a few mV. Now, consider that capacitor and IGBT module health indicators are 50% and 80%, respectively (after normalization, 100% means healthy and 0% degraded). In this case, it is not clear if the SM-level health indicator is 65% (average), 50% (worst case), or another metric that might reflect that IGBT degradation has a higher impact on the system than capacitors (or vice versa). Another example is when information that can not be measured in the field, such as experience from technicians, operators, or suppliers, is considered. For instance, let one consider the case where the health indicator of an IGBT is 50% and, at the same time, the dc-link capacitor health indicator is just at 80%, but there is a global shortage that makes it difficult to buy new parts. In this context, it might be convenient to assign to the capacitor a health status lower than the IGBT module or, at the SM-level, a health indicator lower compared with the other SMs so that degradation alarm could be triggered earlier, prioritizing capacitor replacement.

The previous line of reasoning suggests that concentrated component-level health indicators in a single SM-level index can considerably improve and facilitate the decision-making process of an operator or the health management system. A complex multi-variable decision problem (e.g., under which indicators and circumstances trigger the degradation alarm or plan the next maintenance is convenient?) is converted to a simple single variable problem (cf. **Fig. 6.1(b)**). Similarly, the converter-level health assessment also might be simplified as it could be, for instance, just the sum of the SM-level health indicators weighted by the number of SM (each one has the same importance for the converter operation).

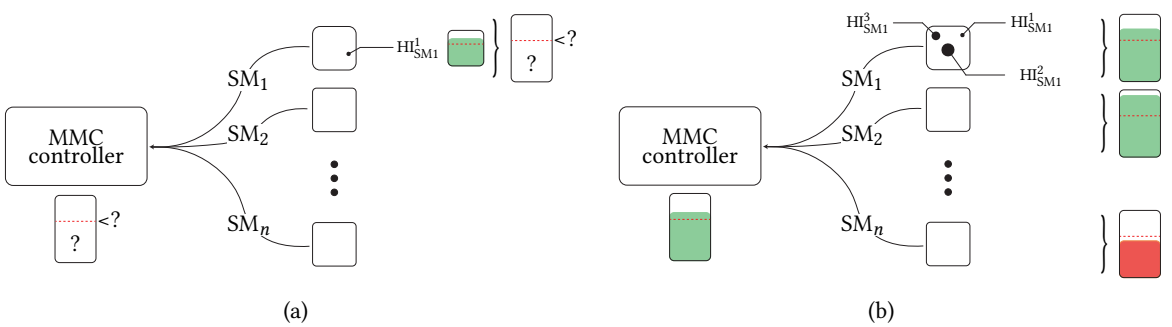


Fig. 6.1 Envisioned SM and converter-level CHM strategy. Scheme a) shows the current situation in which CHM methods is focused in a single component and it is not possible or highly difficult to assess the SM health condition. Scheme b) shows envisioned situation where one or more component-level and comprehensive health indicators coexist and are utilized to create SM and converter-level health indicators.

In the case of electrical engineering, the concept of data fusion arises as an interesting conceptual framework to develop this topic. Data fusion techniques combine data from multiple sources and or sensors (raw and processed data) and related information from databases to improve accuracy and achieve more specific inferences than a single origin [162]. For a multi-sensor system, data fusion can be categorized into three types or levels: data-level fusion, feature-level fusion, and decision-level fusion. In data-level fusion, also called low-level fusion, the raw data from multiple sensors are combined to produce a new set of more informative information than data from a single sensor. Feature-level fusion, also known as intermediate-level fusion, uses features from various sensors or the same sensor (applying different feature extraction techniques) so that the most relevant ones contribute more to the fused outcome. Finally, decision-level fusion is the highest level of data fusion. Each source can provide an independent decision based on its raw data and features.

There are numerous engineering cases in which this framework has been applied, but it is trendy in fields where high reliability and accuracy resulting from fused information is required, namely, aircraft, medical diagnostics, and environmental monitoring [162]. For instance, authors in [163] propose a data-level fusion model to construct a health index for prognostic analysis of a turbofan engine. The method basis on the idea that data is filtered such that the outcome health indicator must be monotonic. In [164] is presented a feature-level data fusion approach for an aircraft gas-turbine engine health management system. Multiple sensor data, such as inlet debris, engine distress, stress wave, and the high-frequency mechanical vibration, extract gas path anomalies using ANN. Then, features are sent to a fusion layer where fuzzy belief networks combine them. In the case of [165], the authors use decision-level fusion to assess the health condition of a vehicle. Vibration signals are processed using power spectrum, wavelet analysis, and entropy spectrum, while oil debris information analysis uses spectrographic and particle distribution data changing rate. Then, normal/abnormal operation is recognized by employing neural networks. Once the decision of whether the vehicle is healthy or not, Bayesian inference, Dempster-Shafer evidence inference, and neural networks are used to fuse them, providing the final condition of the vehicle.

It is well accepted that a data-level fusion structure could produce more accurate results; however, large data systems (several sensors and or high sampling rate) require more processing power. On the other hand, higher-level structures such as feature and decision level data fusion are simpler to process, but the outcome might be less accurate as noise and information loss may affect feature extraction or health level decision. Therefore, several data fusion techniques have been proposed for the three different structure types [166]–[169]; however, there is no clear evidence on choosing the best fusion scheme and data fusion technique. Instead, experience and testing are common approaches [170]. To the best of the author's knowledge, in the case of MMC, there are no previous works addressing this problem, and neither are experiences on the framework, structures, or method selection and application.

Considering revised state-of-the-art and studied SM health indicators, this work investigates the feature-level fusion structure, and it is proposed to solve the information fusion as a multi-criteria decision-making (MCDM) problem. In what follows in this chapter, the concept of MCDM is introduced, and different methods are presented and tested through offline simulations.

6.2 Multi-criteria decision making concept

People deal with MCDM problems in daily life (at work, at home, or even on vacation) whenever a choice has to be made. Usually, the choice is performed by considering the available alternatives against multiple criteria rather than a single criterion. Sometimes, unimportant criteria are eliminated to consider the available options against the most important criterion, with a potential decision error risk. The certain is that the more alternatives and criteria, the more difficult it is to decide. In scientific or industry fields, one person rarely does such practices. Even deciding with a group of experts might be difficult, especially when high-impact decisions are at stake, suggesting a need for a multiple criteria decision-making tool or strategy to come up with the best possible decision [171].

MCDM refers to choosing the best alternative from a finite set of decision alternatives in terms of multiple, usually conflicting, criteria [172], using a collection of methodologies for comparison, ranking, or selection [173]. The use of MCDM methods has been highly reported in the literature, namely, in material selection [174], environmental analysis [175], financial and economics [176] among other applications in the engineering field. In the case of conditions monitoring is less common but of increasing interest. For instance, in [177], the authors use a hierarchical MCDM approach to assess patients' health conditions. Linguistic attributes organized as a hierarchical model, such as oxygenation, body temperature, nutrition, and physical activity, can be evaluated from bad to good (with five different levels). Then, a set of rules are used to calculate the final health score. In [178] is used evidential reasoning approach to decide between different condition monitoring techniques for ship turbines. The work presented in [179] shows the use of entropy to weigh different health indicators to assess a power transformer's condition.

So far and to the best of the author knowledge, there is no specific research reported in the case of CHM applied to MMC; nevertheless, its application can be understood as ranking the SM (alternatives) based on their health level. The health condition comes from different sources, namely, CHM strategies at component and or sub-circuit level (criteria) and expert experience. Each health indicator provides a fraction of the SM condition; however, not necessarily can be considered that each provides the same amount of information for the health assessment. In the case of the experience-based source, it is also interesting to consider that a more comprehensive assessment might be done if information not measured in the field is taken into account, for instance, historical failure and cost and time of repairment.

In typical MCDM approaches, criteria weights reflect relative importance in the decision-making process. Because the evaluation of criteria entails diverse opinions, meanings, and quantities, it can not be assumed that each evaluation criterion is of equal importance. There are two categories of weighting methods: subjective and objective methods. The subjective methods determine weights solely according to the preference or judgments of decision-makers, for instance, from experience. Then, some mathematical methods such as the SMART, Simos, fuzzy, MDL, AHP, eigenvector, or weighted least square models are applied to calculate the overall evaluation of each decision-maker. The objective methods, on the contrary, determine weights by solving mathematical models without any consideration of the decision maker's preferences, for instance, mean weighting, standard deviation, criteria importance through inter-criteria correlation (CRITIC), or entropy method [180]. Moreover, combined weighting methods outcomes (objective and subjective) are claimed by some authors that provide more reliable results in the selection of weights and the final decision process [181].

In what follows in this chapter, two objective weighting methods, CRITIC and entropy; a subjective weighting method, fuzzy the-order-preference-by-similarity-to-an-ideal-solution (TOPSIS); and two merging methods based on game theory and least-squares strategies, are introduced and applied to solve the SM health indicators fusion at feature-level as it would be a MCDM problem.

6.3 Objective weighting methods

The objective weight (OW) methods are mathematical techniques to quantify the importance of an alternative based on system inherent information and behavior; therefore, no human opinion is considered. In order to introduce the OW methods, let us start defining the decision matrix $\mathrm{X}_{i,j}(k)$, whose components represent the numerical value of the criteria j assigned to the alternative i at the instant k, as:

$$\mathrm{X}_{i,j}(k) = \begin{pmatrix} x_{1,1} & x_{1,2} & \cdots & x_{1,j} \\ x_{2,1} & x_{2,2} & \cdots & x_{2,j} \\ \vdots & \vdots & \ddots & \vdots \\ x_{i,1} & x_{i,2} & \cdots & x_{i,j} \end{pmatrix} \tag{6.1}$$

where $x_{i,j} \in \mathbb{R}^{axc}$, $i = \{1, \dots, a\}$ the alternatives, $j = \{1, \dots, c\}$ the criteria, and $k = \{1, 2, ..., t\}$ the sampled periods. To clarify the terms alternative and criteria, let us consider the problem of choosing a car as an example. In this case, the different models are the alternatives, and the features, such as color, number of seats, performance (e.g., liters per 100 km in Europe), safety and cost, are the criteria. In the case of this work, the alternatives are the SMs, and the criteria are their health indicators.

6.3.1 Criteria importance through inter-criteria method

The CRITIC method determines the weights by applying the standard-deviation concept combined with the Pearson [182] correlation between a given set of criteria. The OW for the criterion j is defined as:

$$\mathrm{OW}^{j}_{\mathrm{CRITIC}} = \frac{\beta_j}{\sum_{j=1}^{c} \beta_j} \tag{6.2}$$

where the following expressions are used:

$$\beta_j = \sigma_j \sum_{r=1}^{c} \left(1 - \mathrm{Cor}_{j,r}\right) \tag{6.3}$$

$$\mathrm{Cor}_{j,r} = \frac{\sum_{i=1}^{a} \left(x_{i,j} - \mu_j\right)\left(x_{i,r} - \mu_r\right)}{\sqrt{\sum_{i=1}^{a} \left(x_{i,j} - \mu_j\right)^2 \sum_{i=1}^{a} \left(x_{i,r} - \mu_r\right)^2}} \tag{6.4}$$

$$\sigma_j = \sqrt{\frac{\sum_{i=1}^{a} \left(x_{i,j} - \mu_j\right)^2}{a}} \tag{6.5}$$

$$\mu_j = \frac{\sum_{i=1}^{a} x_{i,j}}{a} \tag{6.6}$$

and it is considered $i = \{1, \dots, a\}$, $j = \{1, \dots, c\}$, and $r = \{1, \dots, c\}$. The Pearson correlation measures the linear correlation between two sets of data, and yields a number in the range -1 to 1. The correlation increases the closer the value is to 1 or -1. If positive, both data sets have a positive slope. If negative, both sets of data have a negative slope. If correlation equals 0, there is no agreement between the information set. Then, the larger β_j is, the more information the criterion j contains; thus, the weight of this criterion is greater than that of other criteria. Finally, the weighted health indicator is calculated as (6.7).

$$\mathrm{HI}^{i}_{\mathrm{CRITIC}} = \sum_{j=1}^{c} x_{i,j} \mathrm{OW}^{j}_{\mathrm{CRITIC}} \tag{6.7}$$

6.3.2 Entropy-based method

In information theory, the information entropy or Shannon's entropy reflects how much information there is in a data source. Used first for telecommunication purposes, it was derived in different fields such as cryptography, economy, and image recognition, among others, and it is one of the most used and oldest OW methods [183]. The OW for the criterion j is defined as:

$$\mathrm{OW}^{j}_{\mathrm{ENTROPY}} = \frac{1 - \mathrm{E}_j}{c - \sum_{j=1}^{c} \mathrm{E}_j} \tag{6.8}$$

where E is the entropy of the criterion j and is defined as follow:

$$\mathrm{E}_j = \frac{-1}{\ln(a)} \sum_{i=1}^{a} f_{i,j} \ln\left(f_{i,j}\right) \tag{6.9}$$

$$f_{i,j} = \frac{x_{i,j}}{\sum_{i=1}^{a} x_{i,j}} \tag{6.10}$$

Suppose the information provided by criterion j is the same among all the alternatives; then the entropy reaches 1, and the associated weight is zero, indicating that criterion j does not provide any useful information and can be canceled from the decision making process. On the contrary, if entropy is small, the associated criterion provides relatively more information and should be considered with a higher weight. Finally, the weighted health indicator is calculated as (6.11).

$$\mathrm{HI}^{i}_{\mathrm{ENTROPY}} = \sum_{j=1}^{c} x_{i,j} \mathrm{OW}^{j}_{\mathrm{ENTROPY}} \tag{6.11}$$

6.4 Subjective weighting method

Subjective weight (SW) methods are purely based on expert opinion. In order to perform a subjective analysis, there is one or more experts who evaluate a set of alternatives among different criteria. The assessment can be provided/extracted, for instance, from a survey or by filling a decision matrix using linguistic terms (e.g., low, medium, or high). In this case, a strategy would be for an expert to assess the health condition of each SM; however, this approach might present more difficulties as an expert would require to perform some additional tests, such as visual inspection. For this reason, the subjective analysis in this work is focused on an additional weighting of the health indicators (criteria) provided by experience-based and or measurable information that is not measured in the field, such as the historical failure, replacement cost, and performance effect of the associated component/sub-circuit. Hereafter, the fuzzy TOPSIS method is presented as the SW strategy.

6.4.1 Fuzzy TOPSIS

TOPSIS is one of the most classic methods for solving MCDM problems and is based on the principle that the chosen alternative should have the shortest distance from the positive-ideal solution and the longest distance from the negative ideal solution. The positive solution is the solution that maximizes the benefit criteria (i.e., the larger the value, the greater the preference) and minimizes the cost criteria (the smaller the value, the greater the preference), while the negative-ideal solution is the opposite, it maximizes the cost criteria and minimizes the benefits criteria [184].

Let us start the method by creating the mapping between linguistic ratings for the alternatives concerning the criteria. Fuzzy numbers and their membership functions provide the semantics of the elements of the linguistic terms. The fuzzy numbers come from Fuzzy theory [185] to represent vague, imprecise, and uncertain information that can be handled using fuzzy rules. In this work, a fuzzy number is defined as the set $z = \{a, b, c\}$, with $a, b, c \in$ and $a \leq b \leq c$. Then, the preference is represented by the membership function depicted in **Fig. 6.2(a)**.

The linguistic variable for preferences are represented as follow: very low (VL)(0,1,3), low (L)(1,3,5), medium (M)(3,5,7), high (H)(5,7,9) and very high (VH)(7,9,10), and it is depicted in **Fig. 6.2(b)**.

Then, similarly to the matrix defined in (6.1) for the OW methods, in (6.12) is defined $X_{i,j}^{\text{FUZZY}}$ the

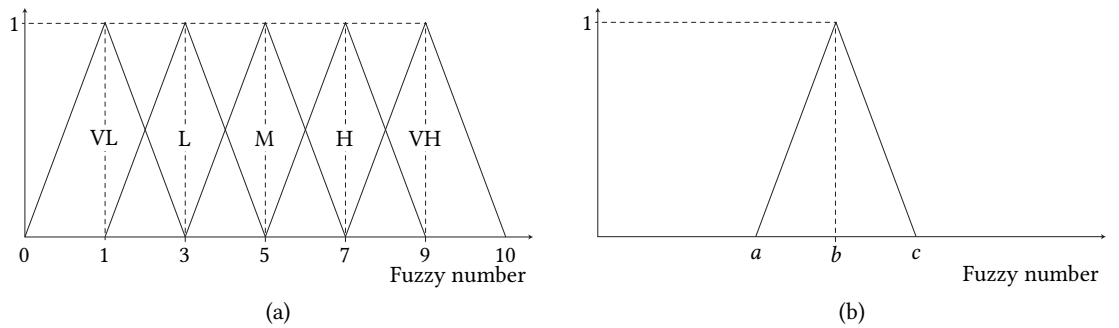


Fig. 6.2 Fuzzy number represented by a triangular membership function. The smallest preference for a given alternative with respect to a given criterion is represented by the value *a*, while the highest preference is represented by the value *c*.

fuzzy decision matrix, where the rows represent the alternatives ($i = \{1, \dots, a_f\}$), the columns the criteria ($j = \{1, \dots, c_f\}$), $x_{i,j}$ is the rating of the alternative i with respect to the criterion j and it is a fuzzy number. In addition, it is defined $\mathrm{W} = \{\omega_1, \omega_2, \dots, \omega_{c_f}\}$ the normalized weight of the criterion j. Both, the elements of $\mathrm{X}_{i,j}^{\mathrm{FUZZY}}$ and W can be represented by fuzzy numbers.

$$\mathrm{X}_{i,j}^{\mathrm{FUZZY}} = \begin{pmatrix} x_{1,1} & x_{1,2} & \cdots & x_{1,j} \\ x_{2,1} & x_{2,2} & \cdots & x_{2,j} \\ \vdots & \vdots & \ddots & \vdots \\ x_{i,1} & x_{i,2} & \cdots & x_{i,j} \end{pmatrix} \tag{6.12}$$

It follows that raw data is normalized to reduce the irregularities due to different units of measurement and scales. To avoid complicated normalization formulas, linear scale transformation is used in this work. Thus, the normalized fuzzy decision matrix is $\mathrm{R}^{\mathrm{FUZZY}} = [r_{i,j}]_{a_f x c_f}$, $i = \{1, \dots, a_f\}$, and $j = \{1, \dots, c_f\}$, where $r_{i,j}$ is defined in (6.13).

$$r_{i,j} = \begin{cases} \left(\frac{a_{i,j}}{c_j^*}, \frac{b_{i,j}}{c_j^*}, \frac{c_{i,j}}{c_j^*} \right), \; c_j^* = \max\limits_i c_{i,j} & \text{benefit criteria} \\ \left(\frac{a_j^-}{c_{i,j}}, \frac{a_j^-}{b_{i,j}}, \frac{a_j^-}{a_{i,j}} \right), \; a_j^- = \min\limits_i a_{i,j} & \text{cost criteria} \end{cases} \tag{6.13}$$

Please note that with the benefits and cost attributes it can be discriminated between criteria that the decision-maker aims to maximize or minimize, respectively. Now, having a normalized fuzzy decision matrix and the different weights for each criterion j (vector W), it is calculated the weighted normalized fuzzy decision matrix $\mathrm{V} = [v_{i,j}]_{a_f x c_f}$, $v_{i,j} = r_{i,j} \otimes \omega_j$. The operator $\otimes$ accounts for the multiplication of two fuzzy numbers and it is defined in (6.14).

$$g \otimes h = (g_1, g_2, g_3) \otimes (h_1, h_2, h_3) = (g_1 h_1, g_2 h_2, g_3 h_3) \tag{6.14}$$

As $\mathrm{V} = [v_{i,j}]_{a_f x c_f}$ is normalized, the distance between each alternative from the fuzzy positive-ideal solution ($v_j^+ = (1, 1, 1)$) and fuzzy negative-ideal solution ($v_j^- = (0, 0, 0)$) is given by (6.15) and (6.16), respectively.

$$d_i^+ = \sum_{j=1}^{c_f} d(v_{i,j}, v_j^+), \; i = 1, 2, \dots, a_f \tag{6.15}$$

$$d_i^- = \sum_{j=1}^{c_f} d(v_{i,j}, v_j^-), \; i = 1, 2, \dots, a_f \tag{6.16}$$

where $d(\cdot, \cdot)$ is the distance measured between two fuzzy numbers, defined in (6.17).

$$d(g,h) = \sqrt{\frac{1}{3}\left(\left(g_1 - h_1\right)^2 + \left(g_2 - h_2\right)^2 + \left(g_3 - h_3\right)^2\right)} \tag{6.17}$$

The ranking of the alternatives is determined by calculating the closeness coefficient CC_i as:

$$\mathrm{CC}_i = \frac{d_i^-}{d_i^+ + d_i^-} \tag{6.18}$$

An alternative with a closeness coefficient close to one is close to the fuzzy ideal-positive solution and far from the fuzzy ideal-negative solution. The subjective weighting values for the criterion j is provided by (6.19).

$$\mathrm{SW}^j_{\text{F-TOPSIS}} = \frac{\mathrm{CC}_i}{\sum_{i=1}^{a_f} \mathrm{CC}_i},\ j = 1, 2, \ldots, c \tag{6.19}$$

Finally, for completeness, the weighted health indicator for the alternative i is calculated using (6.19).

$$\mathrm{HI}^i_{\text{F-TOPSIS}} = \sum_{j=1}^{c} x_{i,j} \mathrm{SW}^j_{\text{F-TOPSIS}} \tag{6.20}$$

It is important to emphasize that despite (6.19) being an expression reflecting expert knowledge weighting the health indicators of the decision matrix presented in (6.1), in this work, the SWs are intended to soften or enhance the OW found in the previous section. This is because calculated SW are based on information not directly from a health assessment of the SMs but from sources that might affect the decisions made only considering OW. Therefore, to fully utilize this new information, it is necessary to combine OWs and SWs, an issue that is addressed in the next section.

6.5 Merging methods

The subjective weighting assignment methods and the objective weighting assignment methods are based on different principles and calculation methods. Therefore, the weighting assignment of attributes from the same problem may be quite different, and the results comprehensively calculated by simple arithmetic or weighted average may significantly differ from the actual situation. Hereafter, least squares-based and game theory-based methods are presented to solve the merging of OWs and SWs.

6.5.1 Least squares-based method

The determination of the combined weights (CWs) can be seen as an optimization problem where its square distance to OWs and SWs has to be minimized; subject to that, found weights have to add one to retrieve the health indicator associated with the alternative. Mathematically, it is expressed as:

$$\min \sum_{j=1}^{c} \left(\left(\mathrm{CW}_j - \mathrm{OW}_j \right)^2 + \left(\mathrm{CW}_j - \mathrm{SW}_j \right)^2 \right) \quad s.t. \sum_{j=1}^{c} \mathrm{CW}_j = 1 \text{ and } \mathrm{CW}_j \geq 0 \tag{6.21}$$

This optimization problem can be solved using Lagrange multipliers, and the solution is given in (6.22)

$$\mathrm{CW}_j^{\mathrm{LS}} = \frac{2 - \sum_{j=1}^{c} \left(\mathrm{OW}_j + \mathrm{SW}_j \right) + c \left(\mathrm{OW}_j + \mathrm{SW}_j \right)}{2c} \tag{6.22}$$

with $j = \{1, \ldots, c\}$, the number of criteria. Finally, the weighted health indicator for the alternative i is calculated using (6.30).

$$\mathrm{HI}_{\mathrm{LS}}^{i} = \sum_{j=1}^{c} x_{i,j} \mathrm{CW}_j^{\mathrm{LS}} \tag{6.23}$$

6.5.2 Game theory-based method

A second approach to finding a compromise between OW and SW might be found in game theory. Game theory is a mathematical framework to address problems with conflicting or cooperating parties who can make rational decisions. In particular, the problem of finding the CWs might be understood as a zero-sum game, in which choices by players can neither increase nor decrease the available resources. In other words, considering OW and SW as players, each one will try to maximize its participation in the final weight until an equilibrium is reached, maximizing the expected payoff of both participants (also known as Nash equilibrium). For mathematical derivation, let us consider the matrix $\Omega = [\omega_{j,k}]_{cxd} = [\omega_{j,1}, \omega_{j,2}, \ldots, \omega_{j,k}]$, with c the number of criteria and d the number of weighting method results (players); then, the result R of the game can be written as a linear combination of the vectors in Ω, where α_k represents the decision of the $k - th$ participant:

$$\mathrm{R} = \sum_{k=1}^{d} \alpha_k \omega_{j,k}, \;\; j = 1, \ldots, c \tag{6.24}$$

In order to find the Nash equilibrium, the result of the game R has to be such that its distance to the result of each participant is minimum. This can be expressed as the optimization problem stated in (6.25).

$$\min \left\| \sum_{k=1}^{d} \left(\alpha_k \omega_{j,k} \right) - \omega_{j,r} \right\|_2, \;\; r = 1, \ldots, d \tag{6.25}$$

The minimization can be solved by applying the first derivative equals zero and using differential property of the matrix, resulting in:

$$\sum_{k=1}^{d} \left(\alpha_k \omega_{j,k} \omega_{j,k}^T \right) = \omega_{j,k} \omega_{j,k}^T \tag{6.26}$$

or equivalently, to solve the liner equations of (6.27).

$$\begin{pmatrix} \omega_{j,1}\omega_{j,1}^T & \omega_{j,1}\omega_{j,2}^T & \cdots & \omega_{j,1}\omega_{j,d}^T \\ \omega_{j,2}\omega_{j,1}^T & \omega_{j,2}\omega_{j,2}^T & \cdots & \omega_{j,2}\omega_{j,d}^T \\ \vdots & \vdots & \ddots & \vdots \\ \omega_{j,d}\omega_{j,1}^T & \omega_{j,d}\omega_{j,2}^T & \cdots & \omega_{j,d}\omega_{j,d}^T \end{pmatrix} \begin{pmatrix} \alpha_1 \\ \alpha_2 \\ \vdots \\ \alpha_d \end{pmatrix} = \begin{pmatrix} \omega_{j,1}\omega_{j,1}^T \\ \omega_{j,2}\omega_{j,2}^T \\ \vdots \\ \omega_{j,d}\omega_{j,d}^T \end{pmatrix} \tag{6.27}$$

Then, the result (decision of each player) is normalized using (6.28).

$$\alpha_k^n = \frac{\alpha_k}{\sum_{k=1}^{d} \alpha_k} \tag{6.28}$$

Finally, the combined weights are calculated using (6.29), and the weighted health indicator for the alternative i is computed using (6.30).

$$\mathrm{CW}_j^{\mathrm{GT}} = \sum_{k=1}^{d} \alpha_k^n \omega_{j,k} \tag{6.29}$$

$$\mathrm{HI}_{\mathrm{GT}}^i = \sum_{j=1}^{c} x_{i,j} \mathrm{CW}_j^{\mathrm{GT}} \tag{6.30}$$

6.6 Methods validation

Having introduced different approaches to calculating OWs, SWs, and CWs, this section investigates their advantages and disadvantages through simulations. The hypothetical scenario is presented where the studied converter is operating, and each SM computes two health indicators, the capacitance and ASPS consumption. In addition, it is assumed that an expert provides information about the health indicators and related components. A complete scheme of the proposed idea is provided in **Fig. 6.3**.

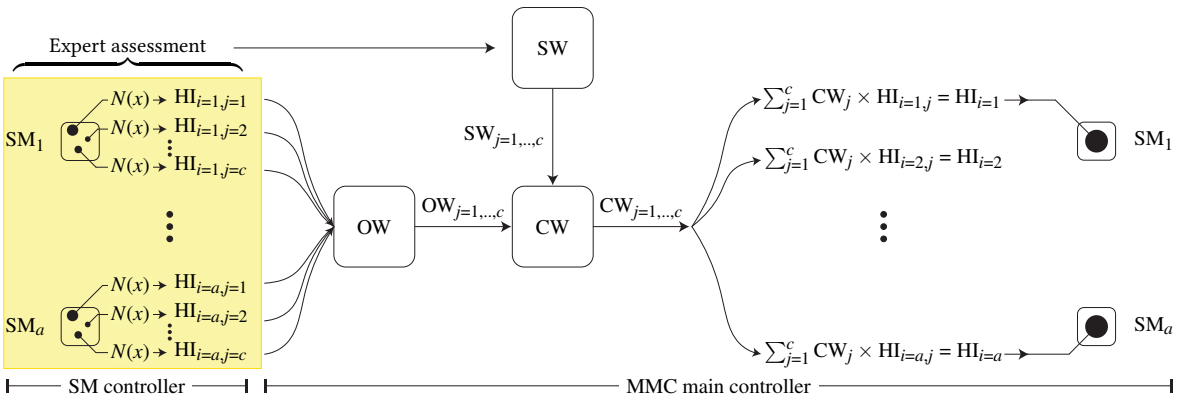


Fig. 6.3 Proposed method scheme. Highlighted in yellow is the calculation and normalization of the different health indicators expected to exist in each SM (e.g., performed in the SM local controller). Normalized health indicators are first weighted using an objective weighting method. On the other hand, the expert assessment is performed offline (once), resulting in the weighting of the health indicators calculated in the SM (weighting of the criteria). Then, both OWs and SWs are combined using a merging strategy resulting in the CWs. The found CWs are utilized to create a weighted sum along all the health indicators of each SM, yielding an integrated SM health indicator.

6.6.1 Input data and normalization

The input data is based on studied health indicators presented in **Chap. 4** and **Chap. 5**, and converter presented in **Chap. 3**. As depicted in **Fig. 6.4(a)**, the 48 SMs are initialized with a capacitance which value is a random number in the range $[1.2 * C_{\text{nom}}, 0.8C_{\text{nom}}]$, with $C_{\text{nom}} = 2.25\,\text{mF}$. Along with the 1000 samples, the capacitance decreases to 70%. At $t = 250$, the C_{SM_6}, the capacitance of the $6th$ SM reaches 75%, simulating premature failure of its capacitors. At $t = 350$, C_{SM_6} is reset to 100% assuming the SM capacitors were replaced. Note that in this case, the new C_{SM_6} at $t = 350$ might be different from the value at $t = 0$.

On the other hand, as depicted in **Fig. 6.4(c)**, each SM is initialized with a value of $\bar{\text{P}}_{\text{ASPS}}$ that takes a random number in the range $[\text{Tolerance}_{\text{min}}, \text{Tolerance}_{\text{max}}]$, with $\text{Tolerance}_{\text{min}}$ =1755 mW and $\text{Tolerance}_{\text{max}} = 2741\,\text{mW}$, accordingly to **Tab. 5.4**. Along with the 1000 samples, the power is assumed constant with the exception of the $12th$ and $24th$ SMs. At $t = 500$, the ASPS consumption of the $12th$ SM increases linearly, entering to the warning zone described in **Fig. 5.8**. On the other hand, the ASPS consumption of the $24th$ SM decreases linearly at $t = 700$, crossing Deg. $\text{Threshold}_{\text{min}} = 1113\,\text{mW}$, the minimum degradation threshold. At $t = 800$, the SM is repaired, returning the ASPS consumption to the typical range (cf. **Fig. 5.8**), not necessarily the same as at $t = 0$.

Once raw data is set, the information is normalized to be comparable. In MCDM problems is common practice to use the max-min method, a linear scale transformation defined in (6.31).

$$x'_{i,j} = \begin{cases} 1 - \dfrac{X^i_{\text{max}} - x_{i,j}}{X^i_{\text{max}} - X^i_{\text{min}}}, & \text{negative trend} \\ 1 - \dfrac{\left\| \bar{X}^i - x_{i,j} \right\|}{\left\| \bar{X}^i - \bar{X}_{\text{max}} \right\|}, & \text{average trend} \end{cases} \tag{6.31}$$

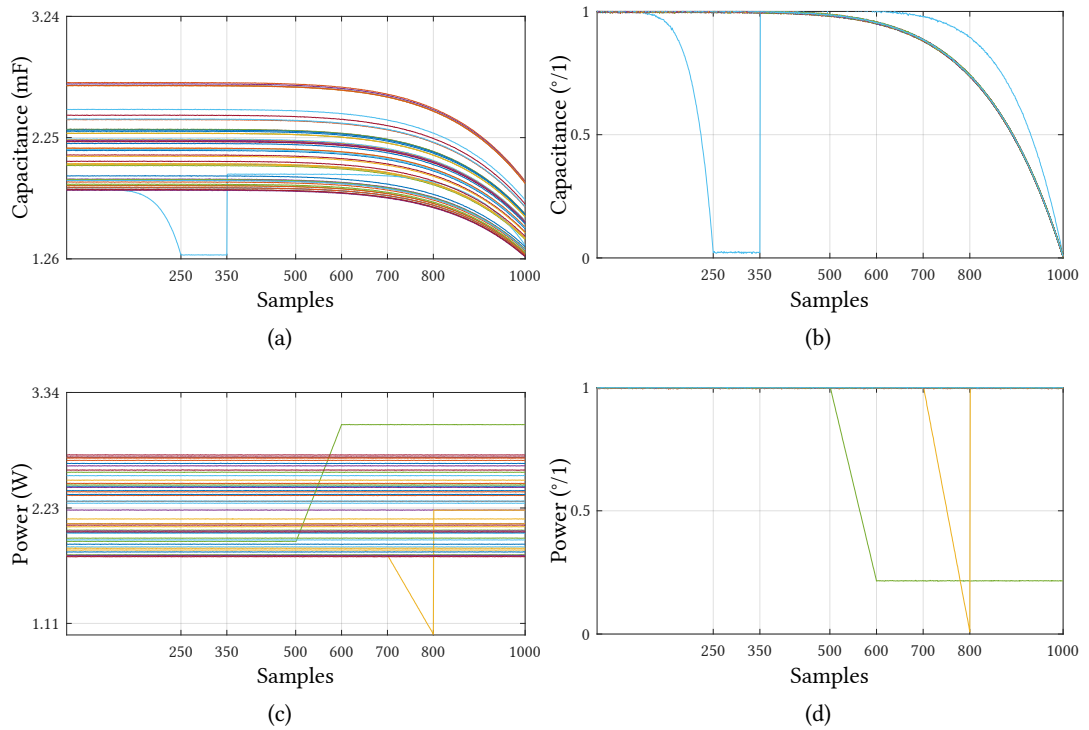


Fig. 6.4 Simulated raw and normalized data for each health indicator. Figures a) and b) show the capacitance raw and normalized information, respectively. Figures c) and d) show the ASPS consumption raw and normalized information, respectively. For both normalized plots, 1 represents a healthy component, while 0 is a degraded component.

The negative trend is used for capacitance data, while the average trend for ASPS consumption. In addition, to represent each health indicator correctly, the normalization is with respect to its initial value (including reset after component repairment or replacement). Thus, $X^i_{\max} = C^i_{\text{SM0}}$ and $X^i_{\min} = 0.7C^i_{\text{SM0}}$ the initial and minimum capacitance values of the *ith* SM, respectively. On the other hand, $\bar{X}^i = \bar{P}^i_{\text{ASPS0}}$, the initial ASPS consumption of the *ith* SM and $\bar{X}_{\max} = \text{Deg.Threshold}_{\max} = 3338\,\text{mW}$ if $x_{i,j} \geq \bar{X}^i$ or $\bar{X}_{\max} = \text{Deg.Threshold}_{\min} = 1113\,\text{mW}$ otherwise. Please note that the initial values for the capacitance and ASPS consumption are calculated by their respective CHM methods and easily stored in either the SM local controller or converter main controller. Normalization results are presented in **Fig. 6.4(b)** and **Fig. 6.4(d)** for the capacitance and ASPS consumption, respectively.

In the case of the subjective assessment, input information is assumed to come from an expert evaluating two alternatives based on three criteria. **Tab. 6.1** shows the expert's preferences related to capacitance and ASPS consumption-based condition monitoring methods, with respect to historical failure (SM control board has been reported to fail more frequently than capacitors), replacement cost (SM control board components are more expensive and challenging to acquire than capacitors), and performance effect (degradation in the SM control board has a more significant impact in the SM operation than capacitor degradation). Additionally, **Tab. 6.2** presents the expert opinion regarding the proposed criteria; in this case, all criteria are of the highest importance. Please note that the three criteria are benefit criteria, i.e., the highest the preference, the more importance is expected to be assigned.

Tab. 6.1 Subjective assessment of components associated to both health indicators

Alternative/criterion	Historical failure	Replacement cost	Performance effect
HI_1 (capacitance-based)	VL(0,1,3)	L(1,3,5)	L(1,3,5)
HI_2 (ASPS-based)	VH(7,9,10)	VH(7,9,10)	VH(7,9,10)

Tab. 6.2 Subjective assessment of proposed criteria

	Historical failure	Replacement cost	Performance effect
Criterion assessment	VH(0.7,0.9,1.0)	VH(0.7,0.9,1.0)	VH(0.7,0.9,1.0)

6.6.2 Objective assessment

The objective assessment is performed based on calculating the weighting factors (OWs) using CRITIC and entropy methods. In this case, each method computes two weights that add one in every sample. The OWs represent the preference for each criterion (capacitance and ASPS consumption-based CHM methods) to evaluate each alternative (SM health). Based on input data presented in the previous part, **Fig. 6.5** shows the resulted OWs and health indicators for each strategy.

In the first part of the simulation, the capacitance of the $6th$ SM is reduced to 75%, while the health indicators in the other SMs are held constant. Both weighting methods recognize the pattern by assigning a higher weight to the capacitance-based indicator, which reaches 1 at $t = 250$ when the capacitor is completely degraded. It is important to highlight two aspects of observed results during non-fault situations ($t < 100$ and $350 < t < 380$). The first aspect is that the capacitance-based indicator is assigned with a higher weight compared to ASPS consumption-based method, while intuition suggests that both weights should be similar (close to 0.5) as nothing out of normal is happening. This behavior might be explained due to the nature of the health indicators. In the case of ASPS consumption-based, the data in the non-fault period is constant, which does not provide new information, while the capacitance-based indicator is slowly dropping for each SM, producing newly detected information. The second aspect is the assigned weighting value. It is clear that both methods recognize capacitance changes; however, it is not straightforward why entropy weight is higher than the CRITIC result. This might find an explanation in the nature of the methods. During the non-fault periods, both health indicators present similar numerical values and trends, which are recognized by the CRITIC method as highly correlated information, meaning a small weighting factor. On the other hand, entropy measures the level of new information on each health indicator, which is particularly high (low entropy) in the case of capacitance, represented with a high weighting value.

In the second part of the simulation ($t > 500$), the ASPS consumption of the $12th$ SM is reduced linearly to the warning zone (power value suited between deg. $\text{Threshold}_{\text{min}}$ and $\text{Tolerance}_{\text{min}}$). In this case, despite the capacitance-based indicator is constantly changing, the variation of the ASPS consumption is higher, producing a more prominent weight for this indicator; however, similarly to the previous analysis, entropy's weight is more significant than CRITIC, as it is focusing mainly in the indicator with more information. It draws the attention that for $600 < t < 700$, the CRITIC weighting factor related to ASPS presents a negative slope (reduces its value) instead of maintaining it, as the indicator has not changed. The problem with this trend can be recognized better in the associated health indicator (cf. **Fig. 6.5(b)**), which increases, meaning that the associated components are improving their health. For the period $700 < t < 800$, where the $24th$ SM is degraded, both

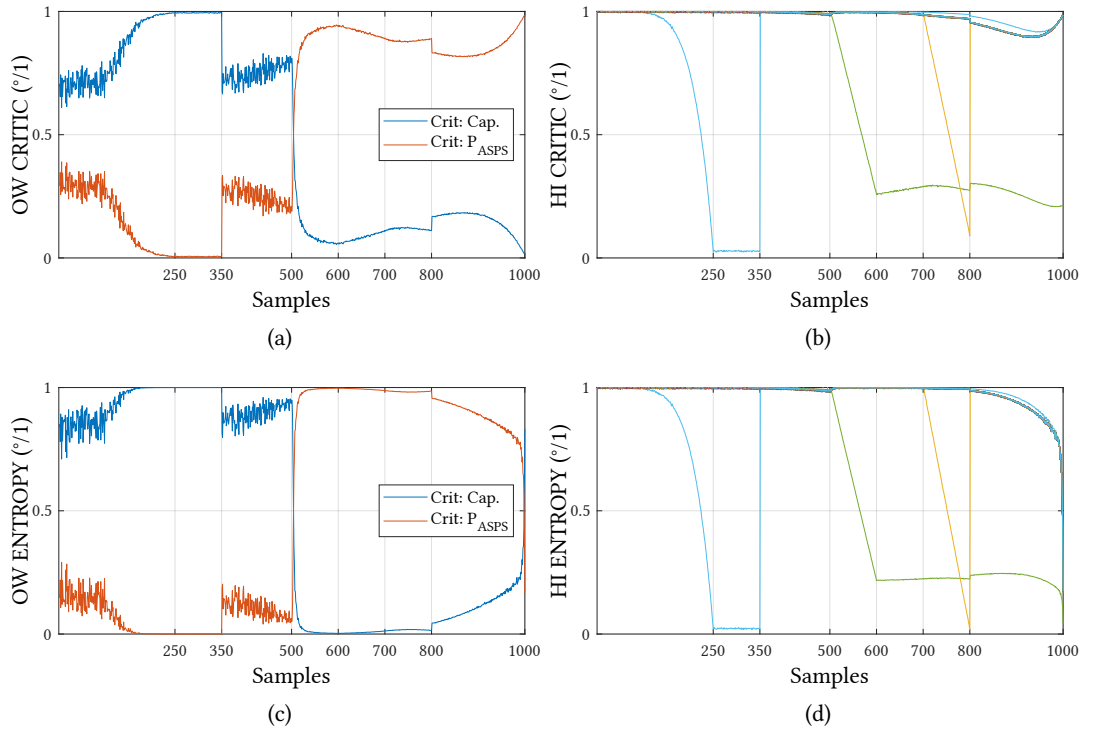


Fig. 6.5 Resulted OWs and associated health indicators for each SM. Plots a) and c) depict the OWs using CRITIC and entropy, respectively, while plots b) and d) their respective health indicators.

methods recognize it and, consistent with previous cases, CRITIC weight is less than entropy, related to ASPS indicator. This behavior is emphasized considering that capacitors are also degrading, so CRITIC assigns a higher weight to capacitance-based indicator, reducing the importance of ASPS consumption-based indicators. Such behavior might be considered correct; however, as the $24th$ SM is degraded and the others are partial, it makes more sense to reflect this as entropy does. Finally, for $t > 800$, only the capacitance-based indicator starts reducing, which is recognized by both methods, but differently. While entropy reduces the ASPS-related weight and increases the capacitance-related as previous analysis and intuition suggest, CRITIC increases ASPS weight, despite the $12th$ and $24th$ SMs are partially degraded and healthy, respectively, producing, again, the wrong result of **Fig. 6.5(b)** where components are recovering.

6.6.3 Expert assessment

The expert assessment was performed considering the linguist preferences for two alternatives (capacitance and ASPS consumption-based indicators) with respect to three criteria (historical failure, replacement cost, and performance effect). First, it is revised that proposed method reflect correctly the expert preferences. This is done by considering three scenarios:

- Scenario a), the alternatives are preferred equally with to respect all the criteria.
- Scenario b), one alternative is preferred maximum with respect all the criteria and the other minimum.

- Scenario c), the alternatives present same preferences (assigned to different criteria), but criteria weights are different.

The results for the scenario a) are presented in **Tab. 6.3**. Independently of the preference values and the criteria weights, both alternatives are weighted 0.5, indicating that share the same importance.

Tab. 6.3 Results for scenario a), W = $[Y, Y, Y]$ and $X, Y \in \{VL, L, M, H, VH\}$

Alternative/Criterion	Historical failure	Replacement cost	Performance effect	SW
HI_1 (capacitance-based)	X	X	X	0.5
HI_2 (ASPS-based)	X	X	X	0.5

In the case of the scenario b), the results (cf. **Tab. 6.4**) show that the maximum weight that can be assigned to an alternative is 0.808 (and 0.192, the minimum). It can not be 1 and the complementary 0 as the membership function is 0 for the first component of the preference VL (0,1,3) and the last component of the preference VH (7,9,10).

Tab. 6.4 Results for scenario b), W = $[VH(0.7, 0.9, 1.0), VH(0.7, 0.9, 1.0), VH(0.7, 0.9, 1.0)]$

Alternative/Criterion	Historical failure	Replacement cost	Performance effect	SW
HI_1 (capacitance-based)	VL	VL	VL	0.192
HI_2 (ASPS-based)	VH	VH	VH	0.808

Finally, results of scenario c) (cf. **Tab. 6.5**) show the effect of the criteria weights. Both alternatives present same preferences (organized in different criteria); however, as the criterion historical fault has a higher weight, it is assigned a higher importance to the alternative HI_1. Otherwise, if criteria weights would be the same, both alternatives would be 0.5.

Tab. 6.5 Results for scenario c), W = $[L(0.1, 0.3, 0.5), VL(0.0, 0.1, 0.3), VL(0.0, 0.1, 0.3)]$

Alternative/Criterion	Historical failure	Replacement cost	Performance effect	SW
HI_1 (capacitance-based)	VH	VL	VL	0.557
HI_2 (ASPS-based)	VL	VH	VL	0.443

Presented scenarios, indicate that fuzzy TOPSIS outcomes is coherent to expected results and, reflect properly the expert assessment. Then, for the considered input data (cf. **Tab. 6.1** and **Tab. 6.2**), resulted SWs are presented in **Tab. 6.6**. The ASPS consumption-based health indicator received a higher value as preferences for all criteria were VH, as well as for criteria weights.

6.6.4 Merged assessment

The merged assessment was performed through two different methods. The first was based on the least-squares method, and the second was on game theory. Each technique was utilized to combine results from OW strategies and SW strategy, resulting in the plots of **Fig. 6.6**.

Tab. 6.6 SWs based on fuzzy TOPSIS method

SW	HI_1 (capacitance-based)	HI_2 (ASPS-based)
	0.268	0.732

Two main observations are worth highlighting. The first one is that neither of the CW methods distorts nor shifts the OW outcomes, resulting in their mere amplitude amplification or compression. The second observation is the weights attenuation observed along with all the samples. On the contrary of results presented in **Fig. 6.5**, weighting factors are lower, which is clear observing that, for instance, CWs do not reach 1 (or 0) in any case. Moreover, a reversion in the CRITIC weights is observed during the non-faulty periods (cf. **Fig. 6.5(a)** and **Fig. 6.5(c)**). This is because both methods search for an agreement between the OWs and SW. For instance, in $250 < t < 350$, where capacitance related weight was 1 and ASPS-related 0 for both objective weighting methods, the compromise is in the 1 to 0.268 and 0.732 to 0 range for the capacitance and ASPS consumption-based health indicators, respectively, producing a reduction in the first case and a rise in the second. In the case of the reversion, the explanation is the same; however, as the lower OW presents the higher SW and is close to 1, the CW is positioned above 0.5, forcing the other indicator to be placed below 0.5. In order to corroborate previous observation, it is sufficient to invert the SW, i.e., HI_1(capacitance-based) = 0.732 and HI_2(ASPS-based) = 0.268 as it is depicted in **Fig. 6.7**.

From the SM-level health indicator perspective, the capacitance-based index is attenuated, showing less degradation for $250 < t < 350$, being coherent with the intuition as subjective assessment assigned less importance to this indicator. On the other hand, ASPS consumption-based health indicators are slightly higher than objective assessment methods but close to 0 as associated SW is preferred. Regarding the differences between least-squares and game theory-based combined weighting strategies, it is straightforward to observe that the game theory-based method yields a higher difference between CWs (cf. **Fig. 6.6(c)** and **Fig. 6.6(g)**), reducing the attenuating effect of the SWs. This is mainly due to the different optimization problems solved. In the least squares-based method, it is searched for the minimum square distance between SWs and OWs, which in this case is the middle point between SW and OW; however, using game theory, the Nash equilibrium is found where the distance to SWs and OWs assures that the result of the game is zero, providing a more extensive excursion range to the CWs.

From the converter-level perspective, when comparing the four CW results as depicted in **Fig. 6.8**, it is noted that no significant difference exists until $t > 800$, where CRITIC-based OWs combined with the SWs show a recover that actually does not occur. In addition, it is important to highlight that converter-level health indicators based on entropy resulted similar to either using least squares or game theory merging method and, as was suggested previously, there is not a significant reason to choose one over the other. In such a case, other characteristics such as computing time might be a decision point. Considering that both methods used the same input data and were executed using the same processor, the elapsed processing time for the least squares-based strategy was 0.128 s, while for game theory-based was 0.077 s, positioning the latter as the best option.

In light of previous results and analysis, it can be concluded that:

- The entropy-based method to calculate the OWs is able to represent properly the importance of each health indicator accordingly to its information.

- The fuzzy-TOPSIS method demonstrated to capture adequately the expert knowledge, converting vague linguistic information into numerical preferences.
- Both least-squares and game theory-based methods were able to find an acceptable agreement between objective and subjective information sources; however, game theory-based strategy is preferred to calculate the CWs as requires less computation power.
- It is important to highlight that when resulted weights from the expert assessment are close to 0.5, the preference for the criteria is similar, and the merged assessment loses importance (could be avoided).
- By means of presented techniques and the created SM-level health indicators, it is possible to consider a converter-level indicator that represents in simple the actual condition of the unit, allowing precise and quick actions when deterioration is detected.
- The converter level health indicator can be formulated in different manners; however, it should be contemplated at least to have a well-defined degradation threshold indicating when the converter might be considered degraded or prone to failure. A suitable approach to tackle this problem is considering two aspects. The first is the converter-level health reduction $\Delta \mathrm{HI}_{\mathrm{MMC}}$ when a SM-level indicator is a minimum (individual worst case scenario). The second aspect is to consider the number of SMs $N_{\mathrm{SM}}^{\mathrm{bp}}$ that can be bypassed without needing to stop the converter. For instance, if $N_{\mathrm{SM}}^{\mathrm{bp}}$ equals zero, the maximum degradation level the converter can withstand is $\Delta \mathrm{HI}_{\mathrm{MMC}}$, which is the case of studied MMC. However, different fault-tolerant methods allow the converter to operate with two or more SMs bypassed, suggesting that it might be more convenient to address the indicator definition considering the branch. The authors in [186] proposed a fault-tolerant strategy where two SMs are bypassed per branch. Then, $N_{\mathrm{SM}}^{\mathrm{bp}}$ equals two and the maximum degradation level the converter can withstand would be $3\Delta \mathrm{HI}_{\mathrm{MMC}}$ per branch, as the worst case is two SMs bypassed and a third degraded. Therefore, the converter-level health indicator can be written as (6.32), and the degradation threshold is zero.

$$\mathrm{HI}_{\mathrm{branch}}^{m} = 1 - \frac{\sum_{n=1}^{N_{\mathrm{SM}}} \left(1 - \mathrm{HI}_{n}\right)}{N_{\mathrm{SM}}^{\mathrm{bp}} + 1} \tag{6.32}$$

$$\mathrm{HI}_{\mathrm{MMC}} = \prod_{m=1}^{N_{\mathrm{branch}}} \mathrm{HI}_{\mathrm{branch}}^{m} \tag{6.33}$$

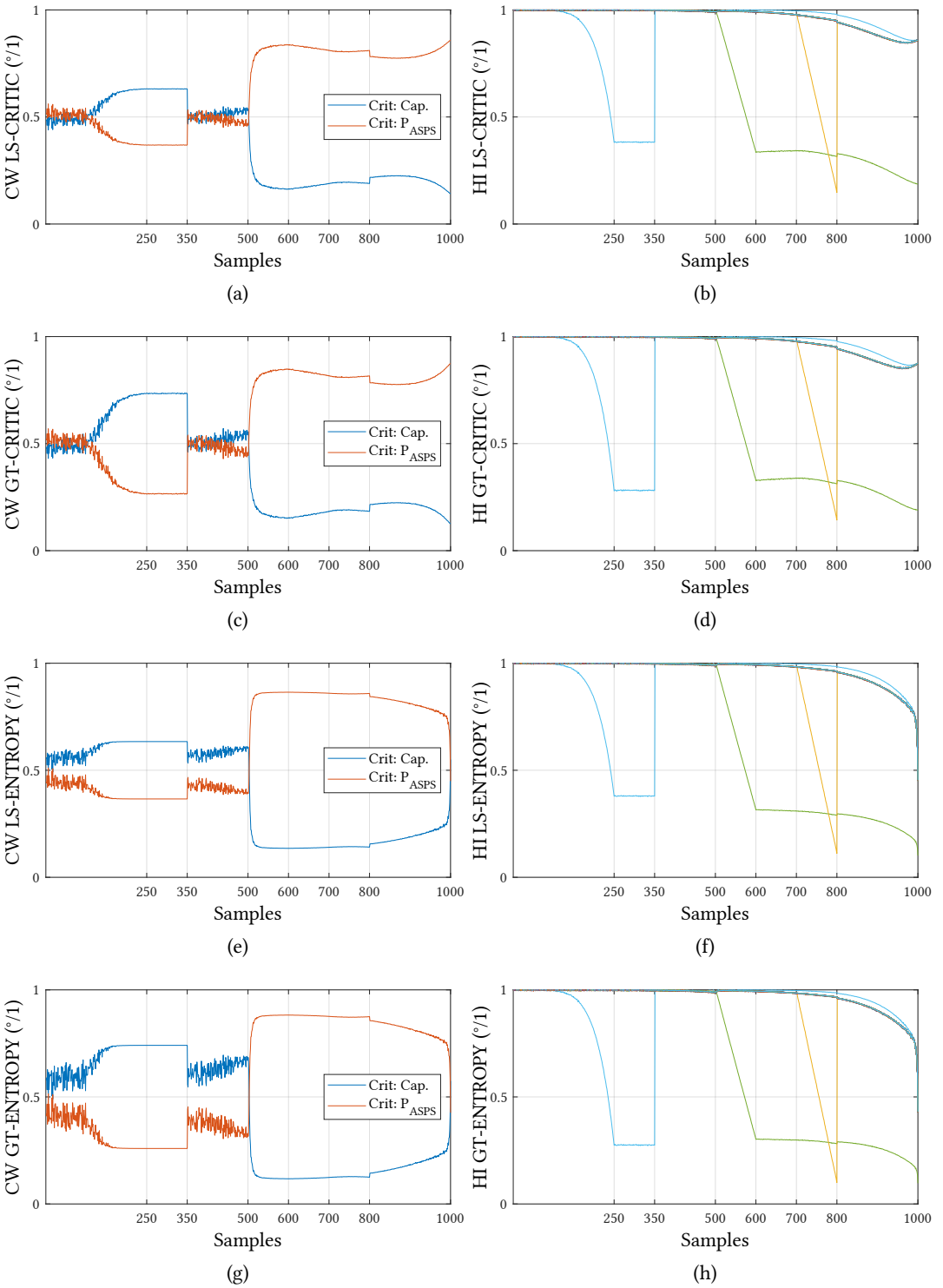


Fig. 6.6 CWs and health indicators using least squares and game theory-based methods applied to OWs calculated using CRITIC and entropy techniques, and SW from expert assessment (cf. **Tab. 6.6**). The goal of the combined assessment is to find CWsreflecting a compromise between the OWs and SW, translated as an amplification/compression of the OWs. Basically, the excursion range of the CW was modified to a value between the SW of the preferred criterion and the related OW.

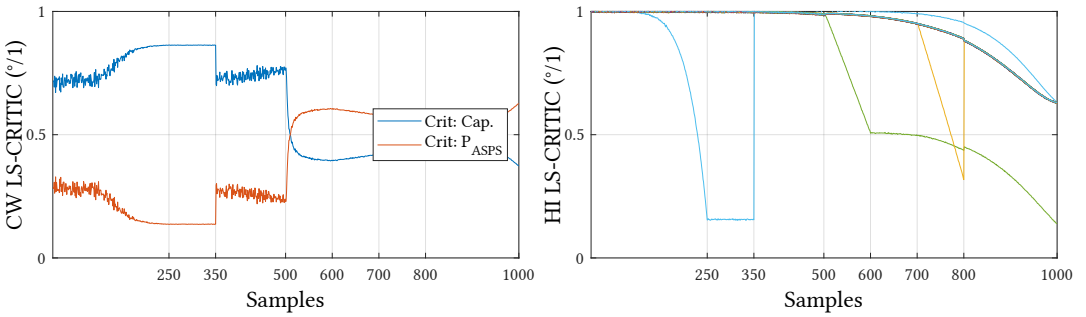


Fig. 6.7 CWs and health indicators using least-squares method applied to the CRITIC-based OWs and reversed SWs. As expected, during the non-faulty periods, there is no reversion, and ASPS consumption-based CW for $t > 500$ is highly attenuated as the expert assessment prefers the capacitance-based indicator.

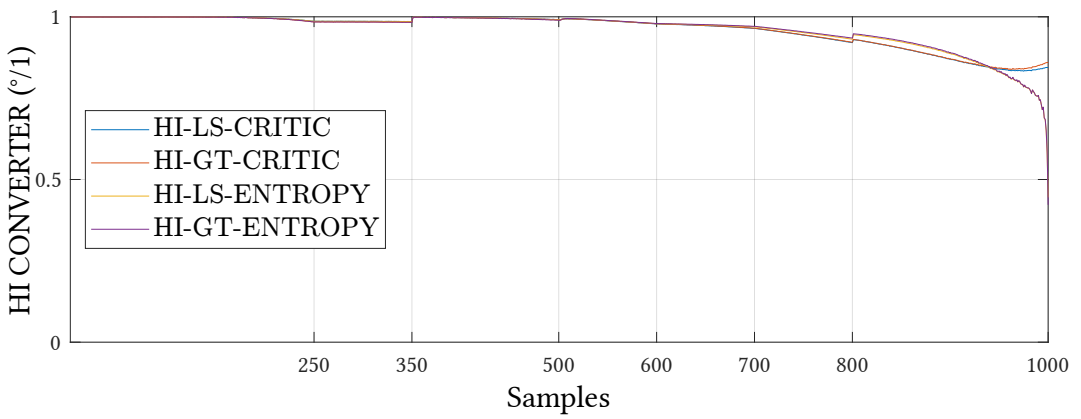


Fig. 6.8 Converter-level health indicator based on combined assessment results. The indicator is calculated assuming that the composite indicator for each SM has the same importance, i.e., each is multiplied by 1/48. This simple strategy reflects the convenience of having a single health indicator per SM. The four methods do not present a significant difference in the results until $t > 800$, where CRITIC-based curves show that the converter is recovering while it is actually showing signs of major degradation.

6.7 Summary

The new sensor technologies and digital tools have made it possible to acquire a massive amount of data to develop PHM to manage power electronics-based assets. Notably, the CHM concept appears as an attractive strategy for gathering factual health information about electronics devices, allowing that early degradation state to be easily recognized, avoiding major faults or failure. CHM techniques applied to MMC are in an early stage of development, and until now, little research has been found to develop and apply condition monitoring strategies to components different from SM capacitors and semiconductors. However, as this work claims, this scenario is expected to evolve into a situation where other components or sections of the SM are monitored, as presented in **Chap. 5**, enabling new CHM strategies. In this scenario, rich in degradation information, a new problem arises. The more information and data sources are available; the more difficult it is to assess the current state of the SMs and or the converter as future health indicators might present a variety of characteristics, such as dynamics, scale, sampling time, importance, and interpretation, among others, making difficult their comparison.

Along with this chapter, the mentioned problem is addressed by introducing and investigating different merging data techniques, inspired by the feature-level data fusion framework stated as a multi-criteria decision-making problem. In this case, ranking the SMs' health level (alternatives) considering the existing health indicators (criteria) and expert knowledge can be solved by employing objective, subjective, and combined weighting methods. It is found that the most prominent results are reached using entropy as an objective weighting strategy and least-squares to merge the OWs and SWs coming from subjective assessment. Consequently, this chapter comprehensively introduces a new perspective to estimate the SM and converter-level health status.

7

Summary, Overall Conclusions and Future Works

This closing chapter aims to summarize and stress the main findings and conclusions of this work, giving way to some light for future work.

7.1 Summary and contributions

Power electronics-based solutions are considered driving technologies for present and future electrical systems. Apart from manipulating electrical energy using power switches and passive components, power converters must fulfill various requirements such as high efficiency, high power quality, low cost, low volume, and reliability, among others. Notably, the interesting structure of the MMC allows for compliance with many of these needs; however, due to its exceptional large count of components, reliability might be of concern, transforming it in a relevant research topic. The concept of CHM appears as a central idea to improve the converter's reliability further by monitoring a parameter trend related to the degradation level of a selected component and or device. If observed parameter traverses a degradation threshold, an alarm indicating the need for maintenance actions is activated, avoiding or reducing the risk of failure. This simple but effective idea applied to MMC is the driving force of this thesis and it has been developed as presented hereafter:

Chap. 2 presented and discussed the PHM framework, in which the idea of CHM takes its relevance and characteristics. In order to predict future component's state of health and define the best course of actions to assure high reliability and availability of monitored asset, present health condition knowledge is crucial. Consequently, through a thorough literature review, it is reviewed extensively how CHM has been applied in the power electronics field, putting particular emphasis on strategies developed to evaluate the health level of MMC. The idea and various approaches are presented, classified, and compared, leading to the conclusion that majority of CHM research related to studied topology had paid attention to the SM, specifically at the components level. Power semiconductors and capacitors are the main monitored devices owing to the scientific evidence indicating that those elements are the most sensitive and essential for the system, as well as, the cost-effective design solutions reducing budget and volume to add measurement and computational means to monitor additional components. Motivated by the PEL MMC research platform and its constrains, the scientific interrogative formulated in this thesis is what achievable alternatives can be found to improve existing CHM strategies and or propose novel techniques to observe the health condition of those devices less sensitive but equally important for the proper function of the converter.

Step by step, the studied converter and its SM are dissected in **Chap. 3**. The main principles governing the MMC are introduced, and a complete description of the achieved PEL SM is presented, emphasizing

main components sizing, and overall functionality. Experimental test results of its operation during the charging / operating and discharging process, protection actuators, and ASPS output regulation are provided, pointing out that available components and software might be used strategically different from the ideas presented in **Chap. 2** to reveal new CHM opportunities.

Despite SM capacitance estimation for the capacitor CHM is a popular research choice, the development of simple, efficient and effective methods can largely reduce its implementation barriers, especially in commercial solutions. In **Chap. 4**, a CHM strategy for the MMC SM power capacitors is introduced based on typically available SM terminal current, dc-link voltage, the IGBT control signals, and the RWLS parameter estimation technique to estimate the SM dc-link capacitance. The well known relationship between capacitance decreasing and degradation increment provides a reliable health indicator of the capacitors. The strategy was deployed in the SM local controller and validated thoroughly through offline and RT-HIL simulations and experimental tests. Its effectiveness in identifying actual SM capacitance and changes is shown and an error of less than 5% is achieved for different operating cases.

Considering that existing measurement hardware and processing power are intended to support fundamental control and protection actions of the SM, their availability for additional purposes is very limited, specially keeping in mind that methods as the one presented in **Chap. 4** might be implemented. Therefore, remaining resources must be carefully recognized and assigned and, in order to monitor non-classical components, non-classical solutions should be considered. **Chap. 5** presented a novel alternative for the MMC CHM but focused on SM sub-circuits instead a single component. The proposed strategy estimates the flyback-based ASPS consumption to observe simultaneously different SM subcircuits instead of a particular component, settling on the idea that small changes in the circuits loading the ASPS secondaries can be detected and used to assess their deterioration level. The ASPS consumption is first estimated considering a simplified ASPS model, the SM dc-link voltage measurement, and the ASPS switch pulses signals.

Experimental results showed that ASPS secondary consumption produces a recognizable signature in the ASPS primary side; however, with a significant inaccuracy (up to 58% error with respect to scope measurement). Thus, it is recognized that having this information, different strategies to determine the faulty behavior of the SM can be implemented as the introduced fault dictionary, allowing the easy recognition of the SM drifting from expected to degraded state.

Claimed along with this work, the envisioned future for the CHM applied to MMC considers, in addition to power semiconductors and capacitors, observing other equally important components present in the SM, as reduced resources utilization, and ideally no extra hardware requirements can be achieved. Thus, a new problem and innovation opportunity arises as massive amount of information coming from different techniques used to estimate the SM condition might be gathered at the SM or converter control level, making its processing and the extraction of valuable information difficult for the correct health assessment and asset management. Inspired by mathematical techniques able to merge different measurements and observations to come up with an encompassing of a particular phenomena, **Chap. 6** discussed and proposed a CHM concept based on the integration of existing SM local CHM methods to compose a comprehensive health monitoring strategy. Systematic approaches to considering objective information from the SM and subjective knowledge, e.g., from expert experiences, are presented and verified through numerical examples, and offline simulations using collected experimental data and acquired experience though this work. Methods performance, and characteristics were analyzed and discussed, demonstrating that entropy, fuzzy-TOPSIS and game

theory-based methods to extract objective, subjective and combined information, respectively, are the most prominent solutions to assess SM and converter-level health level.

7.2 Future work

Along with this thesis different MMC CHM strategies have been introduced, proposed and verified. From more classical component-level capacitance estimation-based, to a more comprehensive and wider strategy involving different data analysis techniques for the converter-level CHM, much more effort has to be done in order to move forward this research topic. Thanks to the experience gained during this work, some guidelines for future work are proposed hereafter:

- As presented in **Chap. 2**, majority of CHM research is focused on power semiconductors and capacitors. Particularly, in MMC the investigation is limited to power capacitors, leaving aside semiconductors. One of the main reasons is that CHM in IGBT technology, for instance, observes parameters difficult to acquire with regular hardware available in the SM, such as on-state collector-emitter voltage, gate-emitter threshold voltage, switching time and junction temperature. However, for protection reasons, it is usual that SM terminal pulses, ambient temperature, IGBT case temperature and other convenient measurements are available at the local controller, as in the case of developed converter. Despite accuracy and precision of those signals might be of concern, certainly they can not be discarded without the corresponding research.

- Capacitance estimation for the CHM is a proven method to detect capacitors degradation. However, there are two aspects worth to explore in this regard. The first is revisiting the method proposed in **Chap. 4** to search for an alternative to estimate, in addition to capacitance, the ESR, as a jointly result could provide a better assessment of capacitor damage. The main limitation is in the dc-link voltage measurement accuracy and bandwidth, impeding to observe its high frequency components (close to f_{sw} and $2f_{sw} \pm f_0$). Work might start focusing on minimizing systematically source of errors in the acquisition system e.g., sensors calibration, anti-aliasing filters, data-type handling, among others. The second aspect is related to the fundamental principle used to estimate the capacitance. Majority of works, including the one presented here, are based on $V_c = Cdi_c/dt$, the relationship between current and voltage in the capacitor. Thus, by the measuring the capacitor response (V_c) to the variations of i_c, C is estimated. The disadvantage of this idea is that either a current sensor or a current estimation of the dc-link capacitor is needed, consuming space and computing power. Instead, a plausible research path might be considering energy and voltage relationship $\Delta E_c = 0.5C\Delta V_c^2$. During steady-state, converter controller aims to maintain SMs average energy constant during a fundamental cycle; however, it is not difficult to conceive a modification in the total or internal energy control so that SM stored energy can be modified temporarily. Even more, a similar perturbation might be achieved by considering changes in the SM local balancing control.

- The CHM scheme proposed in **Chap. 5** was intended to embrace several components with a single measurement method (first layer) and a fault dictionary (second layer). The fault dictionary is a valid and simple option to recognize or set a clear degradation threshold; however, other options might be considered. Having presented an alternative to acquire new degradation information of the SM, processing this data is clearly challenging and depending of the sought goal, more elaborated alternatives can be investigated. For instance, an ANN

can be trained to recognize not only faulty SMs but also the specific sub-circuit and or the component presenting problems; however, taking in consideration converter or SM processing power limitations, ANN configuration, training data requirement and performance. A second research path might be aimed by considering an accelerated degradation test. Even though, consumption drifting is a recognized strategy to detect component fault, the particular case of the PEL SM might be validated through an accelerated degradation test, looking for establishing a relationship between proposed health indicator and actual health condition.

- The combination of subjective and objective information based on entropy, fuzzy-TOPSIS and game theory method showed to be a reasonable strategy to solve the feature-level fusion problem described in **Chap. 6**, tracking and reflecting the different health indicators trend and importance to produce a comprehensive CHM strategy; however, a thorough comparison of the scheme with a SM and converter degradation model might reinforce its applicability as condition health strategy.
- Despite capacitance and ASPS-based CHM methods were validated experimentally, still remains open to confirm that both ideas along with the combined health assessment presented in **Chap. 6** give the same promissory results shown in this work when they are deployed at the converter, i.e., on each SM and at converter main controller. The PEL MMC research platform is a unit whose firmware and software are industrial level, making it a convenient environment for testing characteristics such as performance, noise sensibility and software conflict with other routines. Following the same argumentative line, it is suggested to consider deployment of the presented ideas in other than ac-dc MMC topology, such as the matrix-MMC.

Appendices

A

MMC CHM State-of-the-art summary

Tab. A.1 MMC CHM state-of-the-art summary: part I

Number	Publication	Year	Country	University	Main author	Component type	Precursor parameter	Availability	Classification	Extraction method	Method description	Validation	Error %	Limitations	Advantages
1	[49]	2014	Korea	Yeungman, Univ.	Dong-Choon Lee	Al-cap	C	Online	M-II	MB/Param. Identification	Current injection, low-pass filtering and RLS	Simulation	1.3	Complexity	Accurate
2	[187]	2016	UK	Newcastle University	D. Atkinson	Al-cap	C	Online	M-II	MB/Param. Identification	Observer/Kalman filter	Simulation	-	Complexity of Kalman filter implementation	Accurate
3	[188]	2018	USA	Univer. Of Ontario	S. Williamson	Al-cap	C	Online	M-I	MB/D. calculation	second harmonic impedance extraction/calculation	Simulation	3.5	It needs filtering	Simple
4	[105]	2018	China	Zhejiang Univer. City College	Hui Chen	MPPF-cap	C	Online	M-II	MB/Param. Identification	Additionla sensor/Tunnel Magnetoresistance / RLS (capacitor equation)	Experiment	0.26	Requires additional hardware	Accurate
5	[107]	2019	China	Jiaotong Univer.	Lingyu Zhu	IGBT	R_{ce}	Online	M-II	MB/Param. Identification	Model based to estimate Rce/Kalman filter	Simulation	0.3	Requires junction temperature estimation	Accurate, simple to implement if Tj is available
6	[189]	2019	China	Chongqing Univer.	Li Ran	MPPF-cap	C	Online	M-II	MB/Param. Identification	Model reference adaptive control observer	Simulation/Experiment	1	Complex	Accurate
7	[190]	2019	China	Huazhong Univer. of Science and Technology	Yong Kang	Al-cap	C	Online	M-I	MB/D. calculation	By bypassing observed SM bypass and discharging cap. It used the R-C circuit and time to estimated C.	Simulation/Experiment	5	System is intervened. Redundancy strategy is needed, discharge time depends of capacitance and bleeding resistor	Simple
8	[106]	2019	UK	Newcastle Univer.	Hamza Khalfalla	Al-cap	C/ESR	Online	M-II	MB/Param. Identification	Fast affine projection	Simulation	C:0.01/ESR:3.3	It works only with NLM	
9	[191]	2019	China	Wuhan Univer.	Kaipei Liu	Al-cap	C	Online	M-I	MB/D. calculation	Using switching event and comparing with a reference SM, capacitance difference is detected. In a NLM scheme, aged cap are inserted more frequently.	Simulation	2	It works only with NLM	Simple
10	[192]	2019	China	Southeast Univer.	Zhe Chen	Al-cap	C	Online	M-I	MB/D. calculation	Model, comparisson between a known SM capacitance and the observed	Simulation	0.5	It requires another method to estimate first capacitance, difference between two SM voltage might be small	Simple
11	[193]	2019	USA	Univer. of Ontario	S. Williamson	Al-cap	C	Online	M-I	MB/D. calculation	second harmonic impedance extraction/calculation	Simulation/Experiment	2.5	Low-pass filter, signal injection	Simple
12	[194]	2019	Spain	Universitat Rovira i Virgili	Josep Pou	Al-cap	C	Online	M-II	MB/Param. Identification	Adaptive observer	Simulation	-	It needs centralized measurements to feed-in the observer	No need for capacitor current or estimation
13	[104]	2020	Denmark	Aalborg University	Frede Blaabjerg	Al-cap	C	Offline	M-I	MB/D. calculation	Capacitance is estimated based on the R-C circuit formed by the converter pre-charge system	Simulation/Experiment	1	Only during start up	Simple
14	[195]	2020	Denmark	Aalborg University	Wu Chen	Al-cap	C/ESR	Online	M-I	MB/D. calculation	Model based/sorting algorithm	Simulation/Experiment	C:0.7/ESR:2.4	Computationl burden	Capture both ESR and C

Tab. A.2 MMC CHM state-of-the-art summary: part II

Number	Publication	Year	Country	University	Main author	Component type	Precursor parameter	Availability	Classification	Extraction method	Method description	Validation	Error %	Limitations	Advantages
15	[109]	2020	Denmark	Aalborg University	Frede Blaabjerg	Al-cap	C	Online	M-I	MB/D. calculation	Model based	Simulation/Experiment	0.3	It needs reference SM (2 SMs are off, per branch)	Accurate
16	[196]	2020	China	Zhejiang Univer City College	Xiangning He	Al-cap	C	Online	M-I	MB/D. calculation	Model based	Simulation/Experiment	2	It needs centralized measurements to feed-in the observer, steady state opreation	Accurate
17	[197]	2020	China	Shanghai Jiao Tong University	Bin He	Al-cap	C	Online	M-I	MB/D. calculation	Model based	Simulation/HIL	0.6	It needs centralized measurements	Simple
18	[198]	2020	USA	University of Ontario	S. Williamson	Al-cap	C	Online	M-I	MB/D. calculation	Low frequency impedance (120Hz) estimation.	Simulation/Experiment	2.5	Rely on the second harmonic of the dc-link (it might be removed by 2nd harmonic injection)	Simple
19	[108]	2020	China	China Southern Power Grid	Ting Hou	IGBT	PD	Online	M-I	MB/D. calculation	Partial discharge detection, using terminal current, switchihng events and wavelet decomposition	Simulation	-	Requires high sampling rate sensors	Simple
20	[199]	2021	China	Southeast University	Qiang Yu	Al-cap	C	Online	M-I	MB/D. calculation	Modulation intervention so that capacitor voltage is increased to improve accuracy	Simulation/Experiment	2	Capacitor stressed by the method	-
21	[200]	2021	Sweden	KTH Royal Institute of Technology	Hans-Peter Nee	MPPF-cap	C	Online	M-II	MB/Param. Identification	Impedance estimation. Parameter is extracted with RLS. Estimation is improved with temp. model	Simulation	0	Additional ambient temp. Sensor	Accurate
22	[111]	2021	China	Shanghai Jiao Tong University	Huaping Jiang	Al-cap	C	Online	M-III	DD/ANN	Swtiching frequencies/Back propagation neural network	Simulation	0.01	It needs centralized measurements	Accurate
23	[110]	2021	Sweden	KTH Royal Institute of Technology	Hans-Peter Nee	Al-cap	C	Online	M-II	MB/Param. Identification	Impedance estimation. Parameter is extracted with RLS.	Simulation/Experiment	1	-	Accurate
24	[113]	2021	China	North China Electric Power Univer.	Guangyang Zhou	Al-cap	C	Online	M-I	MB/D. calculation	Using switching event and comparing with a reference SM, capacitance difference is detected. In a NLC scheme, aged cap are inserted more frequently.	Simulation	0.01	Switching signals have to be known. It assumes SM capacitor voltage are exactly the same within a branch	If conditions are met, then it is easy to implement
25	[201]	2021	China	Huazhong Univer. of Science and Technology	Li Peng	Al-cap	C	Online	M-II	MB/Param. Identification	Grouping capacitor voltage observer	Simulation/Experiment	1	It needs centralized measurements	Requires less voltage sensors (SMs are grouped). Method feed in fault detection and isolation methods
26	[112]	2022	Germany	Ruhr Univer. Bochum	Dorothea Kolossa	Al-cap	C	Online	M-III	DD/Mach. Learning	machine-learning-based classifier	Experiment	-	It requires training data. Data post-processed. It is not clear if method has practical application	No model is required (black box assumption)
27	[202]	2021	China	Chongqing Univer.	Yulong Hu	Al-cap	ESR	Online	M-I	MB/D. calculation	Capacitance impedance estimation, extraction with wavelet analysis	Simulation	6.8	Not clear sensor requirements. Vulnerable to noise and sampling freq. Method results are not conclusive	Based on high freq. components, so it does not depend on operating conditions.
28	[203]	2022	China	State Grid Jiangsu Electric Power	Yuting Sun	MPPF-cap	C/ESR	Online	M-I	MB/D. calculation	Capacitance impedance estimation, extraction with FFT	Simulation	1.5	No noise treatment, not clear experimental conditions	Middle complexity

B

Recursive weight least square method summary

Considering the following discrete-time transfer function that represents a system

$$G(z^{-1}) = \frac{y(z)}{u(z)} = \frac{b_1 z^{-}1 + ... + b_m z^{-m}}{1 + a_1 z^{-}1 + ... + a_m z^{-m}} \tag{B.1}$$

it is defined the data vector $\psi^T(k)$ as

$$\psi^T(k) = (-y(k-1)... - y(k-m)|u(k-1)...u(k-m)) \tag{B.2}$$

and, the parameter vector $\theta^T(k)$

$$\hat{\theta}^T(k) = (\hat{a}_1...\hat{a}_m|\hat{b}_1...\hat{b}_m) \tag{B.3}$$

then, it is calculated the updating factor $\gamma(k)$

$$\gamma(k) = \frac{1}{\psi^T(k)P_W(k-1)\psi(k) + \frac{1}{w}} P_W(k-1)\psi(k) \tag{B.4}$$

where $P_W(k-1)$ is the previous measurement covariance matrix and it reflects how reliable are the measurements. W is the weight factor that reflects how reliable the parameters are estimated, and it is chosen constant for this application. Then, the new parameter estimated $\hat{\theta}(k)$ is given by

$$\hat{\theta}(k) = \hat{\theta}(k-1) + \gamma(k)(y(k) - \psi^T(k)\hat{\theta}(k-1)) \tag{B.5}$$

finally, the covariance matrix $P_W(k)$ for the next iteration is calculated as follow

$$P_W(k) = (I - \gamma(k)\psi^T(k))P_W(k-1) \tag{B.6}$$

It is important to note that RWLS method performs optimum if the following conditions are met

- the input signal $u(k)$ is perfectly measurable (no noise, no error) and linearly independent,
- the input signal is such that it can excite the system to obtain sufficient information about itself.
- the perturbation is a zero-mean, constant variance, uncorrelated random variable.

Bibliography

[1] Unfccc, "ADOPTION OF THE PARIS AGREEMENT - Paris Agreement text English,"

[2] H. Ritchie and M. Roser, "CO2 and Greenhouse Gas Emissions," *Our World in Data*, May 2020.

[3] H. Holttinen, A. Groom, E. Kennedy, *et al.*, "Variable Renewable Energy Integration: Status Around the World," *IEEE Power and Energy Magazine*, vol. 19, no. 6, pp. 86–96, Oct. 2021.

[4] *Energy Storage Analysis IEA*.

[5] *A strategy to decarbonize the global transport sector by 2050, explained | International Council on Clean Transportation*.

[6] *Decarbonization of industrial sectors: The next frontier | Sustainability | McKinsey*.

[7] H. Holttinen, J. Kiviluoma, D. Flynn, *et al.*, "System impact studies for near 100% renewable energy systems dominated by inverter based variable generation," *IEEE Transactions on Power Systems*, pp. 1–1, Oct. 2020.

[8] S. R. Sinsel, R. L. Riemke, and V. H. Hoffmann, "Challenges and solution technologies for the integration of variable renewable energy sources a review," *Renewable Energy*, vol. 145, pp. 2271–2285, Jan. 2020.

[9] *Definition of reliability in light of new developments in various devices and services which offer customers and system operators new levels of flexibility*.

[10] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings,*, vol. 3, 2003, 6 pp. Vol.3–-.

[11] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37–53, 2015.

[12] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, 2010.

[13] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1631–1656, Dec. 2017.

[14] R. José, L. G. Franquelo, K. Samir, J. I. León, R. C. Portillo, M. Á. M. Prats, and M. A. Pérez, "Multilevel converters: An enabling technology for high-power applications," *Proceedings of the IEEE*, vol. 97, no. 11, pp. 1786–1817, 2009.

[15] P. Wheeler, X. Lie, Y. L. Meng, L. Empringham, C. Klumpner, and J. Clare, "A review of multi-level matrix converter topologies," *IET Conference Publications*, no. 538 CP, pp. 286–290, 2008.

[16] M. Diaz, R. Cardenas, M. Espinoza, F. Rojas, A. Mora, J. C. Clare, and P. Wheeler, "Control of Wind Energy Conversion Systems Based on the Modular Multilevel Matrix Converter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8799–8810, Nov. 2017.

[17] A. I. Elsanabary, G. Konstantinou, S. Mekhilef, C. D. Townsend, M. Seyedmahmoudian, and A. Stojcevski, "Medium Voltage Large-Scale Grid-Connected Photovoltaic Systems Using Cascaded H-Bridge and Modular Multilevel Converters: A Review," *IEEE Access*, vol. 8, pp. 223 686–223 699, 2020.

[18] R. K. Paul, M. N. Ansary, M. A. Rokib, I. Khan, and M. S. Reza, "Analysis of modular multilevel converter based solid state transformer implementing hybrid control," *ICECE 2018 - 10th International Conference on Electrical and Computer Engineering*, pp. 121–124, Feb. 2019.

[19] J. Pereda and T. C. Green, "Direct Modular Multilevel Converter with Six Branches for Flexible Distribution Networks," *IEEE Transactions on Power Delivery*, vol. 31, no. 4, pp. 1728–1737, Aug. 2016.

[20] M. Winkelnkemper, A. Korn, and P. Steimer, "A modular direct converter for transformerless rail interties," *IEEE International Symposium on Industrial Electronics*, pp. 562–567, 2010.

[21] W. Kawamura, K. L. Chen, M. Hagiwara, and H. Akagi, "A low-speed, high-torque motor drive using the modular multilevel cascade converter based on triple-star bridge cells (MMCC-TSBC)," *2014 IEEE Energy Conversion Congress and Exposition, ECCE 2014*, pp. 1631–1638, Nov. 2014.

[22] Q. Hao, J. Man, F. Gao, and M. Guan, "Voltage Limit Control of Modular Multilevel Converter Based Unified Power Flow Controller under Unbalanced Grid Conditions," *IEEE Transactions on Power Delivery*, vol. 33, no. 3, pp. 1319–1327, Jun. 2018.

[23] M. Vasiladiotis, R. Baumann, C. Haderli, and J. Steinke, "IGCT-Based Direct AC/AC Modular Multilevel Converters for Pumped Hydro Storage Plants," *2018 IEEE Energy Conversion Congress and Exposition, ECCE 2018*, pp. 4837–4844, Dec. 2018.

[24] "HITACHI ABB POWER GRIDS Direct MMC for Converter-Fed Synchronous Machines Control Requirements and First Field Results POWERING GOOD FOR SUSTAINABLE ENERGY," 2021.

[25] Siemens AG, Noethling, and Timo, "STATCOMs: stable voltage for future proof networks," 2020.

[26] *DolWin2 | Hitachi Energy*.

[27] *HVDC PLUS (VSC) – HVDC | IGBT, MMC | High-voltage direct current (HVDC) | Siemens Energy Global.*
[28] *HVDC Light® (VSC) | Hitachi Energy.*
[29] *HVDC Systems.*
[30] J. Li, G. Konstantinou, H. R. Wickramasinghe, and J. Pou, "Operation and Control Methods of Modular Multilevel Converters in Unbalanced AC Grids: A Review," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 1258–1271, 2019.
[31] S. Milovanovic and D. Dujic, "On Power Scalability of Modular Multilevel Converters: Increasing Current Ratings through Branch Paralleling," *IEEE Power Electronics Magazine*, vol. 7, no. 2, pp. 53–63, Jun. 2020.
[32] J. V. M. Farias, A. F. Cupertino, V. D. N. Ferreira, H. A. Pereira, S. I. Seleme, and R. Teodorescu, "Reliability Oriented Design of Modular Multilevel Converters for Medium Voltage STATCOM," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 8, pp. 6206–6214, Aug. 2020.
[33] P. Tu, S. Yang, and P. Wang, "Reliability and cost based redundancy design for modular multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2333–2342, Mar. 2019.
[34] J. Kucka, D. Karwatzki, and A. Mertens, "Enhancing the Reliability of Modular Multilevel Converters Using Neutral Shift," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 8953–8957, Dec. 2017.
[35] L. M. Tolbert, T. J. King, B. Ozpineci, *et al.*, "POWER ELECTRONICS FOR DISTRIBUTED ENERGY SYSTEMS AND TRANSMISSION AND DISTRIBUTION APPLICATIONS," 2005.
[36] *1413-2010 IEEE Standard Framework for Reliability Prediction of Hardware.* 2018.
[37] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Industrial Electronics Magazine*, vol. 7, no. 2, pp. 17–26, 2013.
[38] M. G. Pecht and F. R. Nash, "Predicting the Reliability of Electronic Equipment," *Proceedings of the IEEE*, vol. 82, no. 7, pp. 992–1004, 1994.
[39] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Transactions on Industry Applications*, vol. 47, no. 3, pp. 1441–1451, May 2011.
[40] Y. Song and B. Wang, "Survey on reliability of power electronic systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 591–604, 2013.
[41] U. M. Choi, F. Blaabjerg, and K. B. Lee, "Study and handling methods of power IGBT Module failures in power electronic converter systems," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2517–2533, May 2015.
[42] T. Zheng, M. Huang, L. Zhu, and X. Zha, "Reliability evaluation of MMC system considering working conditions," *The Journal of Engineering*, vol. 2019, no. 16, pp. 1877–1881, Oct. 2018.
[43] F. Deng, Z. Chen, M. R. Khan, and R. Zhu, "Fault detection and localization method for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2721–2732, May 2015.
[44] B. Li, S. Shi, B. Wang, G. Wang, W. Wang, and D. Xu, "Fault diagnosis and tolerant control of single IGBT open-circuit failure in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3165–3176, Apr. 2016.
[45] Q. Yang, J. Qin, and M. Saeedifard, "A Postfault Strategy to Control the Modular Multilevel Converter under Submodule Failure," *IEEE Transactions on Power Delivery*, vol. 31, no. 6, pp. 2453–2463, Dec. 2016.
[46] J. V. M. Farias, A. F. Cupertino, H. A. Pereira, S. I. S. Junior, and R. Teodorescu, "On the Redundancy Strategies of Modular Multilevel Converters," *IEEE Transactions on Power Delivery*, vol. 33, no. 2, pp. 851–860, Apr. 2018.
[47] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, *Condition monitoring for device reliability in power electronic converters: A review*, 2010.
[48] Y. Han and Y. H. Song, "Condition monitoring techniques for electrical equipment - A literature survey," *IEEE Transactions on Power Delivery*, vol. 18, no. 1, pp. 4–13, Jan. 2003.
[49] Y. J. Jo, T. H. Nguyen, and D. C. Lee, "Condition monitoring of submodule capacitors in modular multilevel converters," in *2014 IEEE Energy Conversion Congress and Exposition, ECCE 2014*, Institute of Electrical and Electronics Engineers Inc., Nov. 2014, pp. 2121–2126.
[50] R. Ross and G. Koopmans, "Reliability and Degradation of Power Electronic Materials," *Reliability of Organic Compounds in Microelectronics and Optoelectronics*, pp. 449–478, 2022.
[51] A. A. Feinberg and A. Widom, "On thermodynamic reliability engineering," *IEEE Transactions on Reliability*, vol. 49, no. 2, pp. 136–146, Jun. 2000.
[52] "1856-2017 - IEEE Standard Framework for Prognostics and Health Management of Electronic Systems," 2017.
[53] W. Denson, "The History of Reliability Prediction," *IEEE Transactions on Reliability*, vol. 47, no. 3, sp–321–sp–328, 1998.
[54] M. Pecht and A. Dasgupta, "Physics-of-failure: an approach to reliable product development," *IEEE 1995 International Integrated Reliability Workshop. Final Report*, pp. 1–4,

[55] J. Lee, F. Wu, W. Zhao, M. Ghaffari, L. Liao, and D. Siegel, "Prognostics and health management design for rotary machinery systems—Reviews, methodology and applications," *Mechanical Systems and Signal Processing*, vol. 42, no. 1-2, pp. 314–334, Jan. 2014.

[56] *PROGNOSTIC | significado, definición en el Cambridge English Dictionary*.

[57] O. Fink, Q. Wang, M. Svensén, P. Dersin, W. J. Lee, and M. Ducoffe, "Potential, challenges and future directions for deep learning in prognostics and health management applications," *Engineering Applications of Artificial Intelligence*, vol. 92, p. 103 678, Jun. 2020. arXiv: 2005.02144.

[58] B. Sun, S. Zeng, R. Kang, and M. G. Pecht, "Benefits and challenges of system prognostics," *IEEE Transactions on Reliability*, vol. 61, no. 2, pp. 323–335, 2012.

[59] Y. Hu, X. Miao, Y. Si, E. Pan, and E. Zio, "Prognostics and health management: A review from the perspectives of design, development and decision," *Reliability Engineering & System Safety*, vol. 217, p. 108 063, Jan. 2022.

[60] P. Vrignat, F. Kratz, and M. Avila, "Sustainable manufacturing, maintenance policies, prognostics and health management: A literature review," *Reliability Engineering & System Safety*, vol. 218, p. 108 140, Feb. 2022.

[61] Y. Han and Y. H. Song, *Condition monitoring techniques for electrical equipment - A literature survey*, Jan. 2003.

[62] R. Kothamasu, S. H. Huang, W. H. Verduin, R. Kothamasu, .-. H. Huang, and W. H. Verduin, "System health monitoring and prognostics — a review of current paradigms and practices," *The International Journal of Advanced Manufacturing Technology 2006 28:9*, vol. 28, no. 9, pp. 1012–1024, Apr. 2006.

[63] V. J. Hodge, S. O'Keefe, M. Weeks, and A. Moulds, "Wireless sensor networks for condition monitoring in the railway industry: A survey," *IEEE Transactions on Intelligent Transportation Systems*, vol. 16, no. 3, pp. 1088–1106, Jun. 2015.

[64] W. Qiao and D. Lu, "A Survey on Wind Turbine Condition Monitoring and Fault Diagnosis - Part II: Signals and Signal Processing Methods," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 10, pp. 6546–6557, Oct. 2015.

[65] A. Stetco, F. Dinmohammadi, X. Zhao, V. Robu, D. Flynn, M. Barnes, J. Keane, and G. Nenadic, "Machine learning methods for wind turbine condition monitoring: A review," *Renewable Energy*, vol. 133, pp. 620–635, Apr. 2019.

[66] C. Gao, Y. Xu, J. Wang, R. Burgos, D. Boroyevich, and W. Wang, "Partial discharge online monitoring and localization for critical air gaps among SiC-based medium-voltage converter prototype," *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 11 725–11 735, Dec. 2019.

[67] A. A. Razi-Kazemi and K. Niayesh, "Condition monitoring of high voltage circuit breakers: Past to future," *IEEE Transactions on Power Delivery*, vol. 36, no. 2, pp. 740–750, Apr. 2021.

[68] D. K. Ravish, K. J. Shanthi, N. R. Shenoy, and S. Nisargh, "Heart function monitoring, prediction and prevention of heart attacks: Using artificial neural networks," *Proceedings of 2014 International Conference on Contemporary Computing and Informatics, IC3I 2014*, pp. 1–6, Jan. 2014.

[69] A. Pantelopoulos and N. G. Bourbakis, "A survey on wearable sensor-based systems for health monitoring and prognosis," *IEEE Transactions on Systems, Man and Cybernetics Part C: Applications and Reviews*, vol. 40, no. 1, pp. 1–12, 2010.

[70] A. Basak, S. Narasimhan, and S. Bhunia, "KiMS: Kids' health monitoring system at day-care centers using wearable sensors and vocabulary-based acoustic signal processing," *2011 IEEE 13th International Conference on e-Health Networking, Applications and Services, HEALTHCOM 2011*, pp. 1–8, 2011.

[71] J. C. Steed, "Condition monitoring applied to power transformers - an REC experience," *IEE Colloquium (Digest)*, no. 86, Jan. 1997.

[72] Y. Avenas, L. Dupont, N. Baker, H. Zara, and F. Barruel, "Condition Monitoring: A Decade of Proposed Techniques," *IEEE Industrial Electronics Magazine*, vol. 9, no. 4, pp. 22–36, Dec. 2015.

[73] H. Wang and F. Blaabjerg, "Power Electronics Reliability: State of the Art and Outlook," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 6476–6493, Dec. 2021.

[74] K. Liu, N. Z. Gebraeel, and J. Shi, "A Data-level fusion model for developing composite health indices for degradation modeling and prognostic analysis," *IEEE Transactions on Automation Science and Engineering*, vol. 10, no. 3, pp. 652–664, Jul. 2013.

[75] A. Golnas, "PV system reliability: An operator's perspective," *IEEE Journal of Photovoltaics*, vol. 3, no. 1, pp. 416–421, 2013.

[76] *Informe Benchmarking Plantas Solares Fotovoltaicas Actualización | PDF | Fotovoltaica | Energía solar*.

[77] A. Hanif, Y. Yu, D. Devoto, and F. Khan, "A Comprehensive Review Toward the State-of-the-Art in Failure and Lifetime Predictions of Power Electronic Devices," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4729–4746, May 2019.

[78] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters - An overview," in *IEEE Transactions on Industry Applications*, vol. 50, Institute of Electrical and Electronics Engineers Inc., Sep. 2014, pp. 3569–3578.

[79] N. Patil, J. Celaya, D. Das, K. Goebel, and M. Pecht, "Precursor parameter identification for insulated gate bipolar transistor (IGBT) prognostics," *IEEE Transactions on Reliability*, vol. 58, no. 2, pp. 271–276, 2009.

[80] V. Smet, F. Forest, J. J. Huselstein, A. Rashed, and F. Richardeau, "Evaluation of Vce monitoring as a real-time method to estimate aging of bond wire-IGBT modules stressed by power cycling," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 7, pp. 2760–2770, 2013.

[81] M. Bouarroudj, Z. Khatir, J. P. Ousten, F. Badel, L. Dupont, and S. Lefebvre, "Degradation behavior of 600 V–200 A IGBT modules under power cycling and high temperature environment conditions," *Microelectronics Reliability*, vol. 47, no. 9-11, pp. 1719–1724, Sep. 2007.

[82] S. H. Ali, E. Ugur, and B. Akin, "Analysis of Vth Variations in IGBTs under thermal stress for improved condition monitoring in automotive power conversion systems," *IEEE Transactions on Vehicular Technology*, vol. 68, no. 1, pp. 193–202, Jan. 2019.

[83] M. Tounsi, A. Oukaour, B. Tala-Ighil, H. Gualous, B. Boudart, and D. Aissani, "Characterization of high-voltage IGBT module degradations under PWM power cycling test at high ambient temperature," *Microelectronics Reliability*, vol. 50, no. 9-11, pp. 1810–1814, Sep. 2010.

[84] L. Zhou, S. Zhou, and M. Xu, "Investigation of gate voltage oscillations in an IGBT module after partial bond wires lift-off," *Microelectronics Reliability*, vol. 53, no. 2, pp. 282–287, Feb. 2013.

[85] S. Zhou, L. Zhou, and P. Sun, "Monitoring potential defects in an IGBT module based on dynamic changes of the gate current," *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1479–1487, 2013.

[86] D. W. Brown, M. Abbas, A. Ginart, I. N. Ali, P. W. Kalgren, and G. J. Vachtsevanos, "Turn-off time as an early indicator of insulated gate bipolar transistor latch-up," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 479–489, 2012.

[87] H. Oh, B. Han, P. McCluskey, C. Han, and B. D. Youn, "Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2413–2426, May 2015.

[88] Y. S. Kim and S. K. Sul, "On-line estimation of IGBT junction temperature using on-state voltage drop," *Conference Record - IAS Annual Meeting (IEEE Industry Applications Society)*, vol. 2, pp. 853–859, 1998.

[89] D. Xiang, L. Ran, P. Tavner, A. Bryant, S. Yang, and P. Mawby, "Monitoring solder fatigue in a power module using case-above-ambient temperature rise," *IEEE Transactions on Industry Applications*, vol. 47, no. 6, pp. 2578–2591, Nov. 2011.

[90] C. H. Van Der Broeck, T. Polom, R. D. Lorenz, and R. W. De Doncker, "Thermal Monitoring of Power Electronic Modules Using Device Self-Sensing," *2018 IEEE Energy Conversion Congress and Exposition, ECCE 2018*, pp. 4699–4706, Dec. 2018.

[91] D. Xiang, L. Ran, P. Tavner, S. Yang, A. Bryant, and P. Mawby, "Condition monitoring power module solder fatigue using inverter harmonic identification," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 235–247, 2012.

[92] A. E. Ginart, D. W. Brown, P. W. Kalgren, and M. J. Roemer, "Online ringing characterization as a diagnostic technique for IGBTs in power drives," *IEEE Transactions on Instrumentation and Measurement*, vol. 58, no. 7, pp. 2290–2299, 2009.

[93] M. S. Nasrin and F. H. Khan, "Real time monitoring of aging process in power converters using the SSTDR generated impedance matrix," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, pp. 1199–1205, 2013.

[94] M. Ciappa, "Selected failure mechanisms of modern power modules,"

[95] W. Huai, M. Liserre, F. Blaabjerg, P. De Place Rimmen, J. B. Jacobsen, T. Kvisgaard, and J. Landkildehus, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 1, pp. 97–114, Mar. 2014.

[96] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters - An overview," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3569–3578, Sep. 2014.

[97] H. Ikeo, S. Sakamoto, K. Satot, H. Nishiurata, and K. Ohvo, "Failure mechanisms that cause high electrical leakage in multilayer ceramic capacitors," *ElectroComponent Science and Technology*, vol. 8, no. 3-4, pp. 175–180, 1981.

[98] J. L. Stevens, J. S. Shaffer, and J. T. Vandenham, "The service life of large aluminum electrolytic capacitors: Effects of construction and application," *IEEE Transactions on Industry Applications*, vol. 38, no. 5, pp. 1441–1446, 2002.

[99] A. J. Cardoso, "A simple offline technique for evaluating the condition of aluminum-electrolytic-capacitors," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 8, pp. 3230–3237, 2009.

[100] A. G. Abo-Khalil and D. C. Lee, "DC-link capacitance estimation in AC/DC/AC PWM converters using voltage injection," *IEEE Transactions on Industry Applications*, vol. 44, no. 5, pp. 1631–1637, 2008.

[101] M. W. Ahmad, P. N. Kumar, A. Arya, and S. Anand, "Noninvasive technique for DC-link capacitance estimation in single-phase inverters," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3693–3696, May 2018.

[102] S. Mohagheghi, R. G. Harley, T. G. Habetler, and D. Divan, "Condition monitoring of power electronic circuits using artificial neural networks," *IEEE Transactions on Power Electronics*, vol. 24, no. 10, pp. 2363–2367, 2009.

[103] H. Soliman, H. Wang, B. Gadalla, and F. Blaabjerg, "Condition monitoring for DC-link capacitors based on artificial neural network algorithm," *International Conference on Power Engineering, Energy and Electrical Drives*, vol. 2015-Septe, pp. 587–591, Sep. 2015.

[104] Z. Wang, Y. Zhang, H. Wang, and F. Blaabjerg, "Capacitor Condition Monitoring Based on the DC-Side Start-Up of Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5589–5593, Jun. 2020.

[105] N. Yu, S. Shao, X. Wu, J. Zhang, and H. Chen, "Application of Tunnel Magnetoresistance to Health Monitoring of Modular Multilevel Converter Submodules," *Proceedings - 2018 IEEE International Power Electronics and Application Conference and Exposition, PEAC 2018*, Dec. 2018.

[106] C. Zhang, W. Zhang, S. Ethni, M. Dahidah, V. Pickert, and H. Khalfalla, "Online Condition Monitoring of Sub-module Capacitors in MMC Enabled by Reduced Switching Frequency Sorting Scheme," in *2019 10th International Renewable Energy Congress, IREC 2019*, Institute of Electrical and Electronics Engineers Inc., Mar. 2019.

[107] S. Chen, S. Ji, L. Pan, C. Liu, and L. Zhu, "An ON-State Voltage Calculation Scheme of MMC Submodule IGBT," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 7996–8007, Aug. 2019.

[108] C. Liu, Z. Liu, C. Zhan, L. Zhu, and T. Hou, "An online monitoring scheme for partial discharge signal of sub-module igbts used in mmc," *Proceeding - 8th International Conference on Condition Monitoring and Diagnosis, CMD 2020*, pp. 230–233, Oct. 2020.

[109] Z. Wang, Y. Zhang, H. Wang, and F. Blaabjerg, "A Reference Submodule Based Capacitor Condition Monitoring Method for Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6691–6696, Jul. 2020.

[110] M. Asoodar, M. Nahalparvari, C. Danielsson, R. Soderstrom, and H. P. Nee, "Online Health Monitoring of DC-Link Capacitors in Modular Multilevel Converters for FACTS and HVDC Applications," *IEEE Transactions on Power Electronics*, vol. 36, no. 12, pp. 13 489–13 503, Dec. 2021.

[111] J. Hu, G. Qiu, W. Wang, L. Ran, K. Ma, and H. Jiang, "An On-line Capacitor Condition Monitoring Method Based on Switching Frequencies for Modular Multilevel Converters," *2021 4th International Conference on Energy, Electrical and Power Engineering, CEEPE 2021*, pp. 183–187, Apr. 2021.

[112] N. Markovic, D. Vahle, V. Staudt, and D. Kolossa, "Condition Monitoring for Power Converters via Deep One-Class Classification," pp. 1513–1520, Jan. 2022.

[113] Z. Geng, M. Han, and G. Zhou, "Switching Signals Based Condition Monitoring for Submodule Capacitors in Modular Multilevel Converters," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 6, pp. 2017–2021, Jun. 2021.

[114] R. Marquardt, "Stromrichterschaltungen mit verteilten energiespeichern," *German Patent DE10103031A1*, vol. 24, 2001.

[115] A. Antonopoulos, L. Angquist, and H.-P. Nee, "On dynamics and voltage control of the Modular Multilevel Converter | IEEE Conference Publication | IEEE Xplore," in *2009 13th European Conference on Power Electronics and Applications*.

[116] A. J. Korn, M. Winkelnkemper, and P. Steimer, "Low output frequency operation of the Modular Multi-Level Converter," *2010 IEEE Energy Conversion Congress and Exposition, ECCE 2010 - Proceedings*, pp. 3993–3997, 2010.

[117] Q. Tu, Z. Xu, and L. Xu, "Reduced Switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Transactions on Power Delivery*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[118] X. She, A. Huang, X. Ni, and R. Burgos, "AC circulating currents suppression in modular multilevel converter," *IECON Proceedings (Industrial Electronics Conference)*, pp. 191–196, 2012.

[119] *Control of the Modular Multi-Level Converter for minimized cell capacitance | IEEE Conference Publication | IEEE Xplore*.

[120] M. Vasiladiotis, N. Cherix, and A. Rufer, "Accurate capacitor voltage ripple estimation and current control considerations for grid-connected modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4568–4579, 2014.

[121] R. Picas, J. Pou, S. Ceballos, V. G. Agelidis, and M. Saeedifard, "Minimization of the capacitor voltage fluctuations of a modular multilevel converter by circulating current control," *IECON Proceedings (Industrial Electronics Conference)*, pp. 4985–4991, 2012.

[122] G. Bergna-DIaz, J. A. Suul, E. Berne, J. C. Vannier, and M. Molinas, "Optimal Shaping of the MMC Circulating Currents for Preventing AC-Side Power Oscillations from Propagating into HVdc Grids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 1015–1030, Jun. 2019.

[123] A. J. Korn, M. Winkelnkemper, P. Steimer, and J. W. Kolar, "Capacitor voltage balancing in modular multilevel converters," *IET Conference Publications*, vol. 2012, no. 592 CP, 2012.

[124] P. Münch, D. Görges, M. Izák, and S. Liu, "Integrated current control, energy control and energy balancing of modular multilevel converters," *IECON Proceedings (Industrial Electronics Conference)*, pp. 150–155, 2010.

[125] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded control system of the modular multilevel converter for feeding variable-speed drives," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 349–357, 2015.

[126] R. Naderi and A. Rahmati, "Phase-shifted carrier PWM technique for general cascaded inverters," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1257–1269, May 2008.

[127] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, 2015.

[128] A. Dubey and A. K. Bansal, "Cascaded H-bridge multilevel inverter," *International Journal of Control Theory and Applications*, vol. 9, no. 7, pp. 3029–3036, 2016.

[129] U. M. Choi, F. Blaabjerg, S. Jorgensen, S. Munk-Nielsen, and B. Rannestad, "Reliability Improvement of Power Converters by Means of Condition Monitoring of IGBT Modules," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7990–7997, Oct. 2017.

[130] J. Goncalves, D. J. Rogers, and J. Liang, "Submodule Temperature Regulation and Balancing in Modular Multilevel Converters," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 9, pp. 7085–7094, Sep. 2018.

[131] Y. Sun, M. Wang, and L. Ran, "Capacitance Monitoring Method for Metallized Polypropylene Film Capacitor in MMC," in *iSPEC 2019 - 2019 IEEE Sustainable Power and Energy Conference: Grid Modernization for Energy Revolution, Proceedings*, Institute of Electrical and Electronics Engineers Inc., Nov. 2019, pp. 2431–2436.

[132] R. Yao, H. Li, W. Lai, A. S. Bahman, and F. Iannuzzo, "Lifetime Analysis of Metallized Polypropylene Capacitors in Modular Multilevel Converter Based on Finite Element Method," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, Mar. 2020.

[133] K. Ilves, S. Norrga, L. Harnefors, and H. P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 77–88, 2014.

[134] M. Vasiladiotis, N. Cherix, and A. Rufer, "Accurate capacitor voltage ripple estimation and current control considerations for grid-connected modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4568–4579, 2014.

[135] J. Kolb, F. Kammerer, and M. Braun, "Dimensioning and design of a modular multilevel converter for drive applications," *15th International Power Electronics and Motion Control Conference and Exposition, EPE-PEMC 2012 ECCE Europe*, 2012.

[136] M. Zygmanowski, B. Grzesik, and R. Nalepa, "Capacitance and inductance selection of the modular multilevel converter," *2013 15th European Conference on Power Electronics and Applications, EPE 2013*, 2013.

[137] A. Blinov, S. Norrga, G. Tibola, and G. Velotto, "Cell-level power supply for high-voltage modular multilevel converters," *2017 19th European Conference on Power Electronics and Applications, EPE 2017 ECCE Europe*, vol. 2017-Janua, Nov. 2017.

[138] D. Peftitsis, M. Antivachis, and J. Biela, "Auxiliary power supply for medium-voltage modular multilevel converters," *2015 17th European Conference on Power Electronics and Applications, EPE-ECCE Europe 2015*, Oct. 2015.

[139] O. S. Senturk, T. Maerki, P. Steimer, and S. McLaughlin, "High voltage cell power supply for modular multilevel converters," *2014 IEEE Energy Conversion Congress and Exposition, ECCE 2014*, pp. 4416–4420, Nov. 2014.

[140] J. Liu, X. Yang, X. Hao, T. Liu, and M. Zhao, "Design of auxiliary power supply for high voltage power electronics devices," *Conference Proceedings - 2012 IEEE 7th International Power Electronics and Motion Control Conference - ECCE Asia, IPEMC 2012*, vol. 3, pp. 1661–1665, 2012.

[141] D. Kong, X. Liu, Z. Ying, W. Sun, G. Li, K. Wang, J. Peng, and Q. Zhang, "Wide-range high voltage input auxiliary power supply for modular multi-level converters," *ICEMPE 2017 - 1st International Conference on Electrical Materials and Power Equipment*, pp. 133–136, Jul. 2017.

[142] G. Rizzoli, L. Zarri, J. Wang, Z. Shen, R. Burgos, and D. Boroyevich, "Design of a two-switch flyback power supply using 1.7 kV SiC devices for ultra-wide input-voltage range applications," *ECCE 2016 - IEEE Energy Conversion Congress and Exposition, Proceedings*, 2016.

[143] A. Christe, E. Coulinge, and D. Dujic, "Insulation coordination for a modular multilevel converter prototype," *2016 18th European Conference on Power Electronics and Applications, EPE 2016 ECCE Europe*, Oct. 2016.

[144] S. Milovanovic and D. Dujic, "Comprehensive Comparison of Modular Multilevel Converter Internal Energy Balancing Methods," *IEEE Transactions on Power Electronics*, vol. 36, no. 8, pp. 8962–8977, Aug. 2021.

[145] A. S. S. Vasan and M. G. Pecht, "Electronic circuit health estimation through kernel learning," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1585–1594, 2018.

[146] A. E. Salama, "Fault Diagnosis of Analog Circuits," *Proceedings of the IEEE*, vol. 73, no. 8, pp. 1279–1325, 1985.

[147] M. Aminian and F. Aminian, "Neural-network based analog-circuit fault diagnosis using wavelet transform as preprocessor," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 2, pp. 151–156, 2000.

[148] M. Tadeusiewicz and S. Halgas, "A Method for Parametric and Catastrophic Fault Diagnosis of Analog Linear Circuits," *IEEE Access*, vol. 10, pp. 27 002–27 013, 2022.

[149] P. N. Variyam, S. Cherubal, and A. Chatterjee, "Prediction of analog performance parameters using fast transient testing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, no. 3, pp. 349–361, Mar. 2002.

[150] J. B. Cloete, T. Stander, and D. N. Wilke, "Parametric Circuit Fault Diagnosis Through Oscillation-Based Testing in Analogue Circuits: Statistical and Deep Learning Approaches," *IEEE Access*, vol. 10, pp. 15 671–15 680, 2022.

[151] S. Kumar, N. M. Vichare, E. Dolev, and M. Pecht, "A health indicator method for degradation detection of electronic products," *Microelectronics Reliability*, vol. 52, no. 2, pp. 439–445, Feb. 2012.

[152] Q. Z. Zhou, Y. L. Xie, X. F. Li, D. J. Bi, X. Xie, and S. S. Xie, "Methodology and Equipments for Analog Circuit Parametric Faults Diagnosis Based on Matrix Eigenvalues," *IEEE Transactions on Applied Superconductivity*, vol. 24, no. 5, Oct. 2014.

[153] C. Zhang, Y. He, L. Yuan, and F. Deng, "A Novel Approach for Analog Circuit Fault Prognostics Based on Improved RVM," *Journal of Electronic Testing: Theory and Applications*, vol. 30, no. 3, pp. 343–356, Jun. 2014.

[154] F. Aminian, M. Aminian, and H. W. Collins, "Analog fault diagnosis of actual circuits using neural networks," *IEEE Transactions on Instrumentation and Measurement*, vol. 51, no. 3, pp. 544–550, Jun. 2002.

[155] Y. Tan, Y. He, C. Cui, and G. Qiu, "A novel method for analog fault diagnosis based on neural networks and genetic algorithms," *IEEE Transactions on Instrumentation and Measurement*, vol. 57, no. 11, pp. 2631–2639, 2008.

[156] L. Yuan, Y. He, J. Huang, and Y. Sun, "A new neural-network-based fault diagnosis approach for analog circuits by using kurtosis and entropy as a preprocessor," *IEEE Transactions on Instrumentation and Measurement*, vol. 59, no. 3, pp. 586–595, Mar. 2010.

[157] S. Kumar, V. Sotiris, and M. Pecht, "Mahalanobis Distance and Projection pursuit analysis for health assessment of electronic systems," *IEEE Aerospace Conference Proceedings*, 2008.

[158] M. Vetterli and C. Herley, "Wavelets and Filter Banks: Theory and Design," *IEEE Transactions on Signal Processing*, vol. 40, no. 9, pp. 2207–2232, 1992.

[159] D. Binu and B. S. Kariyappa, "A survey on fault diagnosis of analog circuits: Taxonomy and state of the art," *AEU - International Journal of Electronics and Communications*, vol. 73, pp. 68–83, Mar. 2017.

[160] Z. Liu, Z. Jia, C. M. Vong, S. Bu, J. Han, and X. Tang, "Capturing High-Discriminative Fault Features for Electronics-Rich Analog System via Deep Learning," *IEEE Transactions on Industrial Informatics*, vol. 13, no. 3, pp. 1213–1226, Jun. 2017.

[161] *Atacama Large Millimeter/submillimeter Array | ALMA*.

[162] D. L. Hall and J. Llinas, "An introduction to multisensor data fusion," *Proceedings of the IEEE*, vol. 85, no. 1, pp. 6–23, 1997.

[163] K. Liu, N. Z. Gebraeel, and J. Shi, "A Data-level fusion model for developing composite health indices for degradation modeling and prognostic analysis," *IEEE Transactions on Automation Science and Engineering*, vol. 10, no. 3, pp. 652–664, Jul. 2013.

[164] A. J. Volponi, T. Brotherton, and R. Luppold, "Development of an information fusion system for engine diagnostics and health management," *Collection of Technical Papers - AIAA 1st Intelligent Systems Technical Conference*, vol. 2, pp. 873–886, 2004.

[165] Q. Sun, "Sensor fusion for vehicle health monitoring and degradation detection," *Proceedings of the 5th International Conference on Information Fusion, FUSION 2002*, vol. 2, pp. 1422–1427, 2002.

[166] B. Khaleghi, A. Khamis, and F. O. Karray, "Multisensor data fusion: A review of the state-of-the-art," 2011.

[167] Z. Liu and Y. Kleiner, "State-of-the-art review of technologies for pipe structural health monitoring," *IEEE Sensors Journal*, vol. 12, no. 6, pp. 1987–1992, 2012.

[168] J. Xu, Y. Wang, and L. Xu, "PHM-oriented integrated fusion prognostics for aircraft engines based on sensor data," *IEEE Sensors Journal*, vol. 14, no. 4, pp. 1124–1132, Apr. 2014.

[169] C. Song, K. Liu, and X. Zhang, "Integration of Data-Level Fusion Model and Kernel Methods for Degradation Modeling and Prognostic Analysis," *IEEE Transactions on Reliability*, vol. 67, no. 2, pp. 640–650, Jun. 2018.

[170] M. J. Roemer, G. J. Kacprzynski, and R. F. Orsagh, "Assessment of data and knowledge fusion strategies for prognostics and health management," *IEEE Aerospace Conference Proceedings*, vol. 6, pp. 62 979–62 988, 2001.

[171] Van Bolin, "A multi-criteria decision-making model and its application in system solution engineering," *Bell Labs Technical Journal*, vol. 7, no. 1, pp. 197–214, 2002.

[172] E. Roszkowska, "Multi-Criteria Decision Making Models By Applying the TOPSIS Method To Crisp and Interval Data," *International Scientific Journal*, vol. 6, no. 1, pp. 200–230, 2011.

[173] Umm-E-habiba and S. Asghar, "A survey on Multi-criteria decision making approaches," *2009 International Conference on Emerging Technologies, ICET 2009*, pp. 321–325, Dec. 2009.

[174] I. Emovon and O. S. Oghenenyerovwho, "Application of MCDM method in material selection for optimal design: A review," *Results in Materials*, vol. 7, p. 100 115, Sep. 2020.

[175] G. A. Kiker, T. S. Bridges, A. Varghese, P. T. P. Seager, and I. Linkov, "Application of multicriteria decision analysis in environmental decision making," *Integrated Environmental Assessment and Management*, vol. 1, no. 2, pp. 95–108, Apr. 2005.

[176] J. Černevičienė and A. Kabašinskas, "Review of Multi-Criteria Decision-Making Methods in Finance Using Explainable Artificial Intelligence," *Frontiers in Artificial Intelligence*, vol. 0, p. 35, Mar. 2022.

[177] O. Sustersic, U. Rajkovič, V. Prijatelj, and V. Rajkovič, "Evaluating patient's health by a hierarchical decision model," *Proceedings - International Conference on eHealth, Telemedicine, and Social Medicine, eTELEMED 2009*, pp. 136–139, 2009.

[178] R. S. Prabhu Gaonkar, M. Xie, A. K. Verma, and R. Peng, "Using evidential reasoning approach for ship turbine's condition monitoring techniques ranking," *IEEM2010 - IEEE International Conference on Industrial Engineering and Engineering Management*, pp. 2398–2402, 2010.

[179] Y. Zhou, L. Ma, J. Yang, and C. Xia, "Entropy Weight Health Index method of power transformer condition assessment," *ICRMS'2011 - Safety First, Reliability Primary: Proceedings of 2011 9th International Conference on Reliability, Maintainability and Safety*, pp. 426–431, 2011.

[180] T. C. Wang and H. D. Lee, "Developing a fuzzy TOPSIS approach based on subjective weights and objective weights," *Expert Systems with Applications*, vol. 36, no. 5, pp. 8980–8985, Jul. 2009.

[181] L. Ai, S. Liu, L. Ma, and K. Huang, "A Multi-attribute Decision Making Method Based on Combination of Subjective and Objective Weighting," *2019 5th International Conference on Control, Automation and Robotics, ICCAR 2019*, pp. 576–580, Apr. 2019.

[182] J. L. Rodgers and ; W. A. Nicewander, "Thirteen Ways to Look at the Correlation Coefficient," *The American Statistician*, vol. 42, no. 1, pp. 59–66, 1988.

[183] C. E. Shannon, "A Mathematical Theory of Communication," *The Bell System Technical Journal*, vol. 27, pp. 623–656,

[184] F. Cavallaro, "Fuzzy TOPSIS approach for assessing thermal-energy storage in concentrated solar power (CSP) systems," *Applied Energy*, vol. 87, no. 2, pp. 496–503, Feb. 2010.

[185] L. A. Zadeh, "Fuzzy sets," *Information and Control*, vol. 8, no. 3, pp. 338–353, Jun. 1965.

[186] B. Li, Z. Xu, J. Ding, and D. Xu, "Fault-Tolerant Control of Medium-Voltage Modular Multilevel Converters with Minimum Performance Degradation under Submodule Failures," *IEEE Access*, vol. 6, pp. 11 772–11 781, Mar. 2018.

[187] O. Abushafa, S. Gadoue, M. Dahidah, and D. Atkinson, "A new scheme for monitoring submodule capacitance in modular multilevel converter," in *IET Conference Publications*, vol. 2016, Institution of Engineering and Technology, 2016.

[188] D. Ronanki and S. S. Williamson, "Health monitoring scheme for submodule capacitors in modular multilevel converter utilizing capacitor voltage fluctuations," in *Proceedings: IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, Institute of Electrical and Electronics Engineers Inc., Dec. 2018, pp. 2068–2073.

[189] Y. Sun, M. Wang, and L. Ran, "Capacitance Monitoring Method for Metallized Polypropylene Film Capacitor in MMC," *iSPEC 2019 - 2019 IEEE Sustainable Power and Energy Conference: Grid Modernization for Energy Revolution, Proceedings*, pp. 2431–2436, Nov. 2019.

[190] H. Wang, H. Wang, Z. Wang, Y. Zhang, X. Pei, and Y. Kang, "Condition monitoring for submodule capacitors in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 10 403–10 407, Nov. 2019.

[191] Q. Pu, L. Qin, Q. Wang, J. Le, and K. Liu, "Online Monitoring and Balancing for MMC Capacitor Aging," in *2019 4th IEEE Workshop on the Electronic Grid, eGRID 2019*, Institute of Electrical and Electronics Engineers Inc., Nov. 2019.

[192] F. Deng, Q. Wang, D. Liu, Y. Wang, M. Cheng, and Z. Chen, "Reference Submodule Based Capacitor Monitoring Strategy for Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4711–4721, May 2019.

[193] D. Ronanki and S. S. Williamson, "Quasi-online low-frequency impedance monitoring scheme for submodule capacitors in modular multilevel converters," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, vol. 2019-March, Institute of Electrical and Electronics Engineers Inc., May 2019, pp. 83–90.

[194] E. Rodriguez, L. Gaowen, G. G. Farivar, H. Dehghani Tafti, C. D. Townsend, R. Leyva, and J. Pou, "Capacitor Condition Monitoring Based on an Adaptive Observer of the Low-Frequency Capacitor Voltage Ripples for Modular Multilevel Converters," in *2019 IEEE 4th International Future Energy Electronics Conference, IFEEC 2019*, Institute of Electrical and Electronics Engineers Inc., Nov. 2019.

[195] F. Deng, Q. Heng, C. Liu, X. Cai, R. Zhu, Z. Chen, and W. Chen, "Capacitor ESR and C Monitoring in Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 4063–4075, Apr. 2020.

[196] K. Wang, L. Jin, G. Li, Y. Deng, and X. He, "Online Capacitance Estimation of Submodule Capacitors for Modular Multilevel Converter with Nearest Level Modulation," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6678–6681, Jul. 2020.

[197] X. Xin, Y. Yang, K. Ma, and B. He, "Online Monitoring for Sub-module Capacitance in Modular Multilevel Converter with Four Sampling Points of Capacitor Voltage," *2020 IEEE 9th International Power Electronics and Motion Control Conference, IPEMC 2020 ECCE Asia*, pp. 935–939, Nov. 2020.

[198] D. Ronanki and S. S. Williamson, "Failure Prediction of Submodule Capacitors in Modular Multilevel Converter by Monitoring the Intrinsic Capacitor Voltage Fluctuations," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 4, pp. 2585–2594, Apr. 2020.

[199] C. Yin, F. Deng, F. Zhao, and Q. Yu, "Condition Monitoring Strategy for Modular Multilevel Converters with Improved Accuracy," pp. 762–770, Dec. 2021.

[200] M. Asoodar, M. Nahalparvari, C. Danielsson, and H. P. Nee, "Temperature Considerations for Online Health Monitoring of DC-Link Capacitors in Modular Multilevel Converters," in *2021 23rd European Conference on Power Electronics and Applications, EPE 2021 ECCE Europe*, 2021.

[201] Z. Wang and L. Peng, "Grouping Capacitor Voltage Estimation and Fault Diagnosis with Capacitance Self-Updating in Modular Multilevel Converters," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1532–1543, Feb. 2021.

[202] H. Xia, Y. Zhang, H. Wang, M. Chen, W. Lai, D. Luo, and Y. Hu, "Condition Monitoring for Capacitors in Modular Multilevel Converter based on High-frequency Transient Analysis," *2021 IEEE Energy Conversion Congress and Exposition, ECCE 2021 - Proceedings*, pp. 5342–5347, 2021.

[203] Y. Sun, "Metallized Polypropylene Film Capacitor Condition Monitoring in MMC Based on Impedance Measurement," pp. 69–73, Feb. 2022.

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