Enhancement-mode Multi-channel AlGaN/GaN Transistors with LiNiO Junction Tri-Gate

Taifang Wang, Yuan Zong, Luca Nela, and Elison Matioli, *Senior Member, IEEE*

Abstract – Multi-channel GaN power device, consisting of stacking multiple two-dimensional-electron-gas (2DEG) channels, has been demonstrated to achieve unprecedented on-state performance while maintaining high breakdown voltage (V_{BR}). However, the large carrier density (Ns) makes it more challenging to achieve high positive threshold voltages (V_{TH}) on multi-channel epitaxies. In this work, we demonstrate enhancement-mode (e-mode) multi-channel GaN transistors based on conformally deposited p-type LiNiO over tri-gates to form a multi-channel junction gate structure. Compared to the normal MOS gate, the p-type LiNiO junction gate provides an additional depletion of the channels to yield a more positive V_{TH}, reaching a maximum V_{TH} of 1.2 V (defined at 1 μA/mm). Moreover, high-quality LiNiO provided excellent on-state performance in multi-channel tri-gate devices with a stable operation at high temperature, which present small V_{TH} shift and hysteresis, and low off-state leakage current. The e-mode devices in this work presented a small specific R_{ON} ($R_{ON,\ sp}$) of 0.62 mΩ·cm^{-2} along with a hard breakdown voltage (V_{BR}) of 920 V. This work demonstrates the potential of LiNiO for high-performance e-mode power devices.

Index Terms – **GaN, HEMT, Enhancement-mode, LiNiO, Tri-Gate, Multi-channel.**

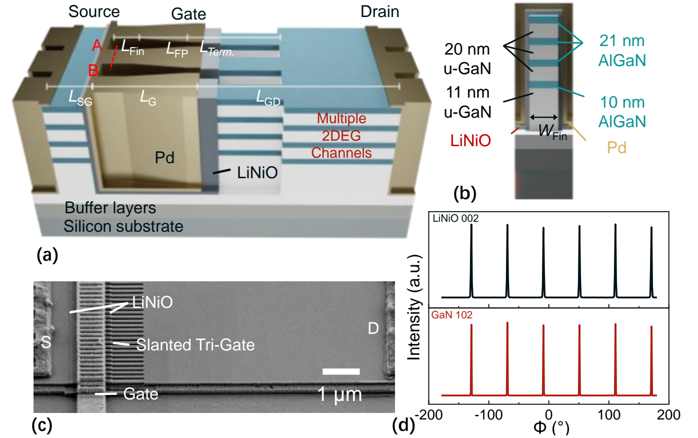

Fig. 1. (a) 3D schematic of multi-channel tri-gate HEMT with LiNiO junction gate, featuring four parallel channels. In slanted tri-gate field-plate region, the gate metal and LiNiO layer both are terminated in the nanowire region. (b) cross-section schematic of single tri-gate structure covered with LiNiO layer and Pd gate metal along the line AB in (a). (c) Tilted top-view SEM image of the fabricated device, a second mesa structure and precise pattern LiNiO are included. (d) XRD Φ scan on LiNiO on AlGaN/GaN planar sample, patterns take on LiNiO (002) and GaN ($10\bar{1}\bar{2}$) crystal planes, an epitaxial relationship of LiNiO (111)[$1\bar{1}0$]//GaN(0002)[$11\bar{2}0$] could be determined.

I. Introduction

GaN-based multi-channel tri-gate MOSHEMTs have been demonstrated as a very promising technology for future high-performance power transistors for low/medium voltage rating applications [1-5]. The multiple vertically stacked 2DEG channels offer a way to break the trade-off between N_S and mobility (μ). An excellent gate control and modulation of the multiple channels was demonstrated by tri-gate structures, resulting in a significant reduction of the device R_{ON}, without sacrificing V_{BR} [1, 2]. However, achieving e-mode operation with large V_{TH} is still very challenging in such high N_S structures. MOS tri-gate, which rely on sidewall depletion to pinch-off the multiple 2DEGs in the gate region, have achieved e-mode operation with V_{TH} of ~0.9 V (defined at 1 μA/mm) [1, 2]. However, the use of gate dielectrics, such as SiO_2 and Al_2O_3, poses serious drawbacks in terms of V_{TH} stability and reliability. This is due to their relatively low quality as these materials are typically deposited by low-temperature atomic layer deposition (ALD) and plasma-enhanced chemical vapor deposition (PECVD). On the other hand, the high deposition temperature required for high-quality dielectrics may degrade the etched GaN surface, which can be particularly damaging for tri-gate structures [3, 6, 7]. Today, the most reliable technology to achieve e-mode is based on the p-(Al)GaN gate, which lifts the conduction band of the GaN channel to locally deplete the 2DEG [8-10]. Nevertheless, applying this technology to multi-channel tri-gate structures is very challenging, due to the difficulty of p-(Al)GaN regrowth control over the nanoscale structure in tri-gates, and GaN surface degradation at the high growth temperature. Recently p-type NiO_x [11, 12] and LiNiO [11] have been demonstrated for e-mode operation in single-channel tri-gate structures. In particular, the LiNiO offers a significant advantage due to the small band offset to AlGaN, hole concentrations that can be tuned from 1×10^{16} cm^{-3} to 6×10^{21} cm^{-3}, and a low deposition temperature of 400 °C [13, 14]. In this work, we demonstrate the e-mode multi-channel junction tri-gate AlGaN/GaN HEMTs, by successfully integrating a high-quality low-temperature p-type LiNiO layer on a multi-channel tri-gate structure. The devices presented high performance with a positive and stable V_{TH} at high temperatures.

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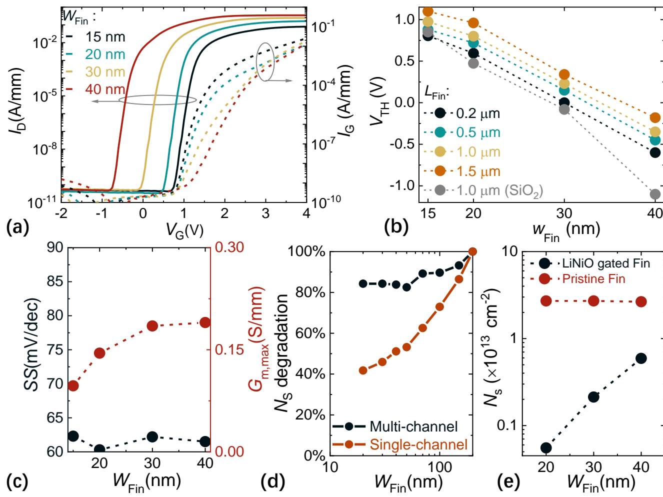

Fig. 2. (a) Transfer (V_D = 5 V) characteristics of multi-channel junction tri-gate HEMT with LiNiO. Different tri-gate fin width (W_{Fin}) devices are included, the length of fin (L_{Fin}) was set to 1 µm. (b) V_{TH} (defined at 1 µA/mm) versus W_{Fin} and L_{Fin}, compare to most positive V_{TH} ever achieved on the same epitaxy, with different gate oxide and metal. Using LiNiO/Pd gate stack result in a nearly 0.5 V V_{TH} shift towards positive in small $W_{Fin} \leq 30$ nm and shift nearly 1 V at W_{Fin} = 40 nm. (c) *SS* and maximum transconductance ($G_{m,\,max}$) versus W_{Fin}. (d) Carrier density (N_s) degradation of pristine fin (without oxide and gate metal) with multi-channel and single-channel epitaxy (relative to Ns for 200 nm wide fin). (e) N_s of pristine tri-gate fin and fins with LiNiO gate stack (normalized on total top surface areas of fins) versus W_{Fin}. Over 1 order of N_s was reduced by LiNiO junction gate. N_s in pristine fin was extracted by hall measurement, details can be found in [1]. And N_s in LiNiO junction gate were extracted by CV measurement on large gate length (L_G) device, details in [4] (L_G = 10 µm and V_G = 0 V).

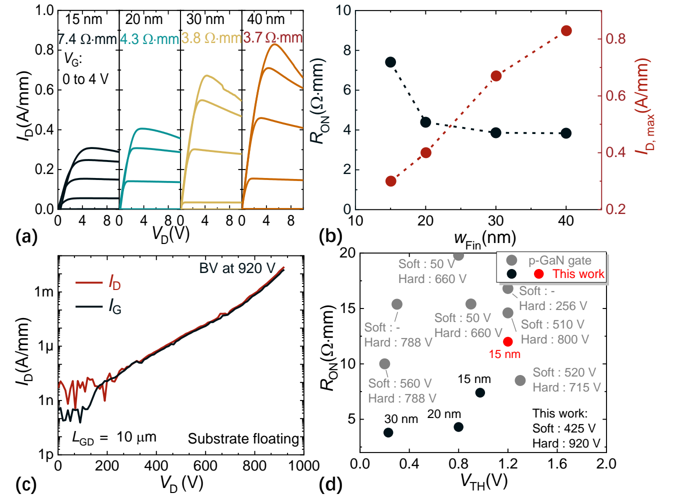

Fig. 3. (a) Output characteristic of different W_{Fin}, the L_{Fin} was set to 1 µm. (b) R_{ON} (extracted at V_G of 4 V) and $I_{D,\,max}$ versus W_{Fin}. (c) three terminal breakdown characteristics of the device (W_{Fin} = 20 nm, L_{Fin} = 1.0 µm) at V_G = 0 V (under floating substrate with fluorinert). (d) R_{ON} versus V_{TH} benchmark for presented device with state-of-the-art e-mode devices through p-GaN gate devices from the literature. Devices in this work present a much lower R_{ON} for the same V_{TH} with respect to the reported p-GaN gate e-mode devices, the reported hard and soft breakdown (at 1µA/mm) voltages are marked next to each point. Device with L_{Fin} of 1.5 µm and W_{Fin} = 15 nm is marked red.

II. Device Structure and Fabrication

The epitaxial structure consisting of four AlGaN/GaN channels is the same as that described in Ref. [1], which presents a large Ns of 3.9x10^{13} cm^{-2} and μ of 1,930 cm^{2}·V^{-1}·s^{-1}, resulting in a low sheet resistance (R_S) of 83 Ω·sq^{-1}. The device fabrication started with mesa isolation and the definition of the tri-gate fins by ebeam lithography (EBL). A 2 nm-thick Ti glue layer was used to enhance the Hydrogen silsesquioxane (HSQ) adhesion to the GaN surface [15]. The mesa and fin structures were etched by Ar/Cl_2 inductively coupled plasma etching (ICP) with a depth of 250 nm. Four cycles of digital etching were used to remove sidewall damages during dry etching [1, 16]. To better isolate the device, a second mesa was patterned by a thicker HSQ layer (300 nm) and etched with a depth of 200 nm. The ohmic metal stack composed of Ti/Al/Ti/Ni/Au was defined in the source and drain regions, followed by rapid thermal annealing. A 250-nm-thick SiO_2 was deposited by PECVD as an etching stop layer (ESL) of ion beam etching (IBE) for the LiNiO patterning. To precisely define the LiNiO oxide layer in the gate region, a 180 nm thick HSQ layer was directly patterned by EBL exposure to serve as a lift-off mask. The LiNiO deposition was done by pulsed-laser-deposition (PLD) [14, 17] using a $Li_{0.25}Ni_{0.75}O$ target at 400 °C with a thickness of 70 nm. The deposition was performed by laser ablation with a repetition rate of 5 Hz, and energy density of 400 mJ·cm^{-2} with a 248 nm KrF laser. It was followed by IBE and BHF etching to lift-off LiNiO layer. Finally, the gate electrode was defined by EBL followed by deposition of the ohmic gate consisting of Pd/Au. Device performance was normalized by total device width of 20µm.

III. Results and Discussion

Figure 1 (a) shows the schematic of the LiNiO junction tri-gate multi-channel HEMT [1]. The detailed multi-channel epitaxy and cross-section of the tri-gate fin structure are shown in Fig. 1(b). The device consisted of a source-gate distance (L_{SG}) of 1 µm, gate-drain distance (L_{GD}) of 10 µm, tri-gate slanted field plate length of 0.7 µm, LiNiO termination length (L_{Term}) of 100 nm. The gate length (L_G) is equal to the fin length (L_{Fin}) plus 0.4 µm. Fig. 1 (c) shows the scanning electron microscopy (SEM) image of the fabricated device, where a precisely patterned LiNiO over the tri-gate can be observed. X-ray diffractometer (XRD) Φ-scan taken on the (002) LiNiO and $(10\bar{1}2)$ GaN crystal planes (on planar LiNiO on AlGaN/GaN sample) confirms the epitaxial relation between the high-quality rock-salt LiNiO on wurtzite AlGaN/GaN (Fig. 1 (d)) [13, 17].

The transfer characteristics of devices with different tri-gate fin widths (W_{Fin}) and the same L_{Fin} of 1 µm are shown in Fig. 2 (a). The decrease of W_{Fin} results in fewer carriers in the channel, thus shifting V_{TH} towards positive values. E-mode operation (I_D = 1µA/mm) was possible for all devices with W_{Fin} below 30 nm. The devices presented near-ideal *SS* of 61-63 mV/dec and an on/off ratio of over 9 orders of magnitude, which reveals the high-quality LiNiO and the excellent gate control of the tri-gate structure. All measurements in this work were normalized by the entire width of the device (W_D). The I_G (for $V_G > V_{TH}$) of devices with small W_{Fin} was larger compared to those with large W_{Fin} due to two reasons: first, the over etching of top AlGaN barrier, which is more prominent in small fin widths, especially at 15 nm. Second, the larger carrier depletion in smaller fins results in smaller turn-on voltage of gate diode.

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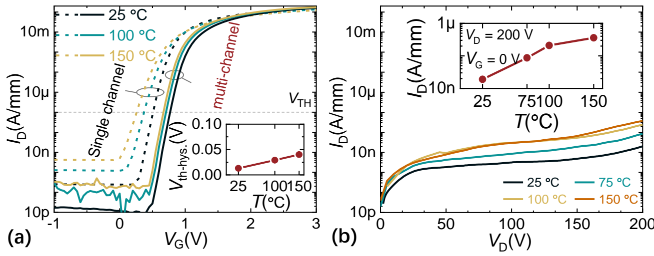

Fig. 4. (a) Temperature-dependent transfer characteristics of multi-channel (W_{Fin} = 20 nm) and reference single-channel device (W_{Fin} = 40 nm) with measurement temperature from 25 °C to 150 °C, inset presents the V_{TH} hysteresis (defined at 1 μA/mm) of multi-channel device from double sweep. (b) Temperature-dependent off-state leakage measurement with measurement temperature from 25 °C to 150 °C. V_G was set at 0 V with floating substrate, and fluorinert was used. Inset: I_D (V_D = 200 V) versus temperature.

Figure. 2 (b) shows the increase in V_{TH} for longer L_{Fin} and narrower W_{Fin}. P-type LiNiO junction gate resulted in an over 0.5 V shift in V_{TH} compared with the most positive V_{TH} achieved on MOS multi-channel tri-gate structures with the same W_{Fin}. The maximum V_{TH} achieved on LiNiO multi-channel devices was 1.2 V (for W_{Fin} of 15 nm and L_{Fin} of 1.5 μm), which is very close to the theoretical prediction for e-mode tri-gate device [18]. While long-fin devices were fabricated to explore the maximum possible V_{TH} of proposed structure, a better balance between the V_{TH} and on-state performance was achieved for a device with L_{Fin} of 1 μm, which was chosen for the further characterizations.

The near-ideal *SS* and large peak G_m ($G_{m,\,max}$) extracted from Fig. 2 (a) reveals excellent gate control and drive ability (Fig. 2 (c)). One advantage of multi-channel epitaxy over single-channel is the much smaller N_S degradation as W_{Fin} decreases [1], which however results in a more difficult pinch-off of the channel purely by W_{Fin} scaling (Fig. 2 (d)). To elucidate the origin of the observed larger V_{TH}, the Ns of fins covered with LiNiO junction gate structure was measured by capacitance-voltage (CV) method, and compared with that of a pristine fin (without metal/oxide) obtained from hall measurements (Fig. 2 (e)) [1]. A clear depletion of carriers is observed for smaller W_{Fin} with LiNiO/Pd, which is not the case in pristine fins. The reduced N_S at V_G = 0 V makes it easier to achieve e-mode.

Figure 3 (a) shows the dependence of the output characteristics on W_{Fin}. As summarized in Fig. 3 (b), devices with smaller W_{Fin} present a higher R_{ON} and lower maximum driving current ($I_{D,\,max}$), which is due to their increased resistance as well as the over-etching of the fin, especially for the narrower fins (W_{Fin} of 15 nm). In addition, to keep the slanted tri-gate portion constant for a fair study, the number of tri-gate fins was fixed in each device, which resulted in a reduction of $I_{D,\,max}$, and in an increase in R_{ON} with a decrease in W_{Fin}, as they are normalized by the entire W_D. This degradation could be mitigated by increasing the number of fins in the same W_D as well as by improving the etching process for the narrow fins.

Figure 3 (c) presents the breakdown voltage characteristics of the proposed devices (L_{Fin} of 1 μm and W_{Fin} of 20 nm). Due to the well-distributed electric field by slanted tri-gate structure [2, 19-21], the device presents V_{BR} (hard breakdown) of 920 V, and the majority of the off-state current was through the gate ($I_G \approx I_D$). The gate leakage current could be reduced by improving the step coverage and thickness of the LiNiO over the tri-gate, offering a large room for further improvement on V_{BR} [13]. An unprecedented low R_{ON} was achieved at similar V_{TH} when compared to state-of-the-art e-mode devices by p-GaN gate or p-oxide gate structures (Fig. 3 (d)), resulting in a $R_{ON,\,sp}$ of 0.62 mΩ·cm^2 (by considering a 1 μm transfer length at each source/drain sides).

In addition, these devices presented outstanding stability at high temperatures compared with single-channel devices using LiNiO junction gate (with a similar V_{TH} for fair comparison). A temperature rise from 25 ℃ to 150 ℃ (Fig. 4 (a)) resulted in a small V_{TH} shift of -0.11 V, and the leakage level was kept below 1 nA/mm at 150 ℃. Moreover, the proposed devices presented a very small V_{TH} hysteresis (from double sweep transfer measurement) of 0.05 V at 150 ℃. This small hysteresis reveals the great quality of the LiNiO layer, as evidenced by XRD measurements (Fig. 1 (d)), which results in a small negative shift of V_{TH}.

The leakage current in off-state during positive drain voltage (V_D) stress could be maintained below 1 μA/mm at 150 ℃ and V_D = 200 V (Fig. 4 (b)). This superior high-temperature voltage blocking capability is benefited from the depletion from three sides by the LiNiO layer, which results in deeper depletion inside of fin [11]. Finally, LiNiO junction gate structures have also presented excellent reliability performance on single-channel epitaxy [22].

Conclusion

In this work, we presented high-performance multi-channel transistors based on the LiNiO junction gate, presenting a large positive V_{TH} of 1.2 V, near-ideal *SS* of 61 mV/dec, high on/off ratio over 9 orders of magnitude. This work unveils a promising technology path for future high-performance lateral GaN HEMT through structure, epitaxy, and gate material engineering.

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