

A 1 μ W radiation-hard front-end in a 0.18 μ m CMOS process for the MALTA2 monolithic sensor

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Abstract—In this paper, a low-power, radiation-hard front-end circuit for monolithic pixel sensors, designed to meet the requirements of low noise and low pixel-to-pixel variability, the key features to achieve high detection efficiencies, is presented. The sensor features a small collection electrode to achieve a small capacitance (< 5 fF) and allows full CMOS in-pixel circuitry. The

circuit is implemented in the 180 nm CMOS imaging technology from the TowerJazz foundry and integrated in the MALTA2 chip, which is part of a development that targets the specifications of the outer pixel layer of the ATLAS Inner Tracker upgrade at the LHC. One of the main challenges for monolithic sensors is a radiation hardness up to 10^{15} 1 MeV n_{eq}/cm^2 Non-Ionizing Energy Loss (NIEL) and 80 Mrad Total Ionizing Dose (TID) required for this application. Tests up to $3 \cdot 10^{15}$ 1 MeV n_{eq}/cm^2 and 100 Mrad were performed on the MALTA2 sensor and front-end circuit, which still show good performance even after these levels of irradiation, promising for even more demanding applications such as the future experiments at the HL-LHC.

Index Terms—Front-end circuits, Monolithic Active Pixel Sensors, pixel detectors, radiation hardness.

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I. INTRODUCTION

MONOLITHIC Active Pixel Sensors (MAPS) constitute an attractive alternative to the more largely used hybrid pixel sensors for high-energy physics experiments. Their main advantage stems from the integration of the readout electronics and sensor in the same silicon die, avoiding the expensive fine-pitch bump bonding. MAPS therefore facilitate significantly the detector assembly and reduce the production cost. Without bump bonding, they also tend to offer a smaller pixel pitch and thus a better spatial resolution. Furthermore, the sensor capacitance can be made so small (< 5 fF) that it can offer a higher voltage signal even with a reduced sensor thickness, i.e. a lower generated charge. This leads to a better power-performance ratio, allowing a significant reduction of the material related to the powering and cooling of the detectors. A lower material budget reduces the probability for multiple scattering of the particles emerging from the interaction point, improving the impact parameter resolution and momentum resolution on the reconstructed tracks and the overall detection efficiency of a tracker. Encouraging results from CMOS sensor prototypes [1]–[3] prompted the development of large-scale CMOS sensors [4], [5] which would meet the requirements of the outer pixel layer of the ATLAS inner tracker (ITk) upgrade [6]. This entails a NIEL tolerance up to 10^{15} 1 MeV n_{eq}/cm^2 , a TID tolerance up to 80 Mrad and a timing response within 25 ns with a power density below 500 mW/cm². To this end, the 20.6 mm \times 20.2 mm MALTA sensor was designed in the TowerJazz 180 nm imaging technology. The MALTA pixel matrix features a sensor with a small collection electrode, an open-loop charge-sensitive front-end and a fast, low-power, asynchronous digital readout architecture [7]. Measurements

on the chip showed a timing response within the specifications [8], however, the efficiency was degraded in the pixel corners already after 10^{14} 1 MeV n_{eq}/cm^2 [9]. This was addressed in a subsequent small-scale prototype called Mini-MALTA [10] by modifying the sensor to enhance the lateral electric field and improve charge collection. The sensor modifications were then implemented in another large-scale prototype, MALTA2, along with improvements on the front-end circuit. This paper presents the design of the MALTA2 front-end, able to cope with the ATLAS ITk outer pixel layer requirements. For this circuit, the main challenge is to amplify the generated charge with high pixel-to-pixel uniformity and low noise, which are the key features to set low charge thresholds to determine particle hits and obtain good detection efficiencies. Extensive characterization of the prototype is currently in progress and the first measurements, performed on samples irradiated up to $3 \cdot 10^{15}$ 1 MeV n_{eq}/cm^2 and 100 Mrad, are shown here.

II. SENSOR

The cross section of the standard sensor in the TowerJazz 180 nm CMOS imaging technology is shown in Fig. 1a. It implements a small collection electrode, defined by an n-well implant, which is located inside the sensing volume, typically a high-resistivity p-type epitaxial layer. The in-pixel circuitry is placed outside the collection electrode and it is shielded from it by a deep p-well, which avoids collection of the signal charge by parts of the circuit other than the designated collection electrode. The key features of the technology are therefore the deep p-well, which allows full CMOS in-pixel circuitry, and the possibility to use different starting materials compatible with particle detection. The depletion volume within the sensor can be increased by increasing the reverse bias between the collection electrode and the surrounding p-well and p-type substrate. For visible light, the signal is generated within a depth of a few microns, whereas high energy particles generate charge over the full thickness of the silicon (~ 60 electron/hole pairs per micron traversed [11]) which needs to be collected within the time resolution of the event reconstruction. For the TowerJazz standard sensor of Fig. 1a, the epitaxial layer is only partially depleted and the signal charge generated outside the depletion area is collected by diffusion (with a collection time of ~ 100 ns). The ATLAS experiment has more stringent timing requirements, since the particle hits have to be associated to different bunch crossings, 25 ns apart from each other. To obtain a faster response, the depletion zone needs to be extended over the whole sensitive layer. The objective is to push the charge carriers towards the collection electrode by drift and thus reduce the collection time. Faster collection times also reduce the probability for charge carriers to get captured by the radiation-induced defects, improving the sensor tolerance to NIEL. To achieve full depletion of the sensor volume, the process has been modified [12] by adding a uniform ion-implanted low-dose n- layer under the deep p-well covering the entire matrix/pixel area, as shown in Fig. 1b. Due to its low doping, the n- layer is fully depleted in typical biasing conditions, and the electrode is effectively still defined by the the small n-well. This modification creates

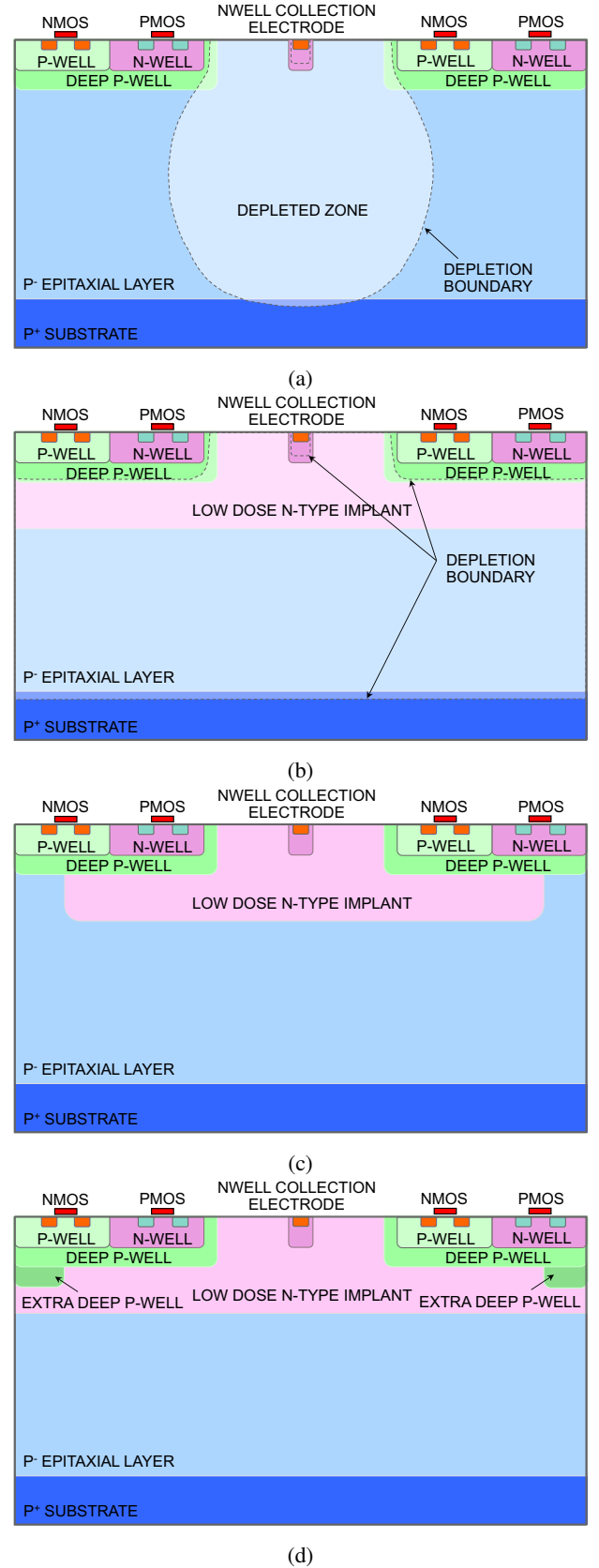


Fig. 1: Cross section of the TowerJazz 180 nm CMOS imaging sensor (a) standard process (b) modified process with low dose n- implant (c) with gap in the low dose n- implant (d) with extra deep p-well. Sensors in (c) and (d) also fully deplete with a sufficiently large reverse bias.

a planar junction deep in the epitaxial layer and the depletion extends immediately over the full pixel area. However, despite the full depletion of the epitaxial layer, the lateral electric field in the pixel corners and along the pixel edges is still quite low, resulting in a relatively long collection time and hence a high probability for the charge to get captured by the radiation-induced traps which leads to efficiency loss in these regions [9]. The strength of the lateral electric field in the corner regions can be increased by introducing a lateral gradient in the doping profile [13]. This can be achieved by patterning the n- layer, i.e. removing it at the pixel edges, as shown in Fig. 1c, or with the introduction of an extra deep p-well implant, as shown in Fig. 1d [10].

The advantage of the small collection electrode is its low sensor capacitance, which is key to achieve a lower analog power consumption for a given charge, bandwidth and signal-to-noise ratio (SNR) [14]. The SNR of the analog front-end can be calculated comparing the input signal created by the ionization of a high-energy particle to the input-referred RMS noise. The latter is typically dominated by the input transistor thermal noise, inversely proportional to the square root of its transconductance g_m , and can be expressed as an equivalent series voltage. The input signal can be calculated as the ratio of the generated charge divided by the sensor capacitance, i.e. the Q/C ratio. Therefore, assuming the front-end power consumption dominated by the input transistor current, one can write

$$\frac{S}{N} \propto \frac{Q}{C} \sqrt{g_m} \propto \frac{Q}{C} \sqrt[2]{P}, \quad (1)$$

with $m=2$ for the input transistor in weak inversion, where g_m is proportional to the biasing current, or $m=4$ in strong inversion, where the g_m is proportional to the square root of the biasing current. Rearranging, for a fixed SNR and bandwidth

$$P \propto \left(\frac{Q}{C}\right)^{-m}, \quad (2)$$

with $2 \leq m \leq 4$, depending on the operating point of the input transistor. The expression states that the required power consumption to reach a given SNR is heavily dependent on the Q/C ratio. It is therefore important to mention that the process modification does not introduce any penalty on the sensor capacitance thanks to the full depletion of the additional n- layer [12]. This paper shows results for pixels which implement the sensor from Fig. 1d. The epitaxial layer is 30 μm thick and has a resistivity larger than 1 $\text{k}\Omega\cdot\text{cm}$. The collection electrode is an octagonal shaped n-well with a diameter of 2 μm , distanced 4 μm in all the directions from the surrounding p-well containing the circuitry. This geometry is the result of a trade-off between a small sensor capacitance (< 5 fF) and a large lateral electric field [15], with collection times in the nanosecond range [13]. The sensor in this modified process was tested up to 10^{15} 1 MeV $n_{\text{eq}}/\text{cm}^2$ [3], still showing good tolerance to NIEL. The transistors also have a good tolerance to TID due to the thin oxide thickness provided by the technology [16].

III. FRONT-END

The front-end is a continuously active circuit which performs the reset of the collection electrode, the amplification

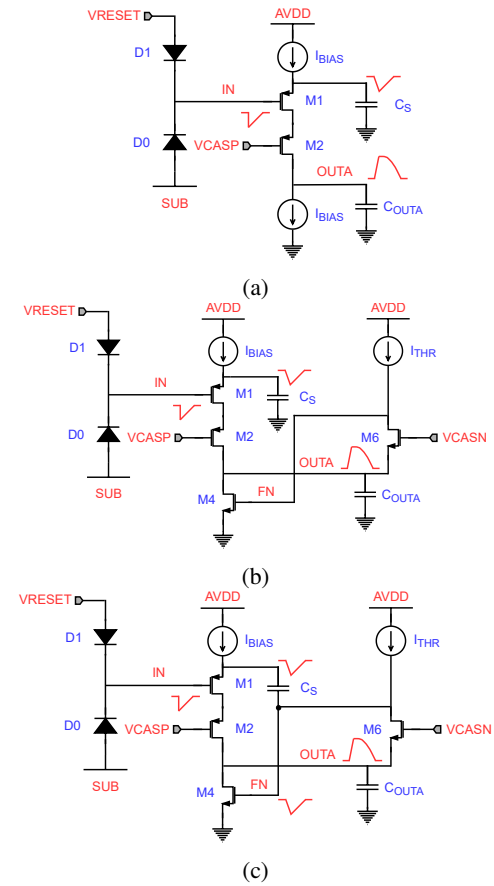


Fig. 2: Front-end principle: (a) simplified schematic (b) with feedback to adjust the operating point (c) with additional gain mechanism.

of the generated charge, the shaping of the analog signal and the digitization of this signal through a discrimination stage. The basic principle of the amplification stage is illustrated in Fig. 2a. The continuous reset mechanism uses the diode D1 to hold the collection electrode voltage. The latter is set to $\sim 1\text{V}$ for a proper front-end operation by tuning the V_{RESET} bias depending on the sensor leakage current. The p-type substrate and p-well containing the circuitry can be biased down to -6V , allowing to achieve a sensor reverse bias of $\sim -7\text{V}$. When no charge is collected by the collection electrode, D1 is biased by the leakage current of the sensor diode D0. Upon a particle crossing, the electrode collects the generated electrons and a negative voltage step with an amplitude of $\Delta V = Q/C$ is generated on it. This causes the reset diode to conduct more current and to slowly charge the input node back up to its original value, which can take several hundreds of μs . The reset diode is implemented with a small p+ implant in the n-well of the collection electrode, adding only a small capacitance to the sensor. A closed-loop charge-sensitive amplifier which integrates the charge on a feedback capacitor [17] is typically used in these applications. In such architecture, for a very small sensor capacitance, the feedback capacitance might be non-negligible with respect to the sensor capacitance and create a noise penalty for the same power consumption. Lowering the feedback capacitance to a small fraction of the

timing response, the main biasing current I_{BIAS} needs to be ~ 470 nA for a sufficiently large g_m of the amplifying devices. The I_{THR} current, typically a few nA, and the discriminator off current, typically a few tens of nA, need to be added to the I_{BIAS} current to obtain the total current consumption which is ~ 500 nA. With a supply voltage of 1.8 V, the total power consumption is less than 1 μ W per pixel, which is used efficiently thanks to the current reuse between the input follower M1 and the common-source device M4. A parasitic-extracted simulation of the transient waveforms at the input IN, analog output OUTA and discriminator output OUTD of the front-end with the charge threshold set to 100 e^- is shown in Fig. 4. The solid lines show the response for a collected charge of 250 e^- , the dashed lines for a charge of 1000 e^- . The simulation was performed using a current pulse at the input, i.e. by injecting the input charge uniformly in a collection time of 1 ns. The sensor is modelled as a capacitance of 2.5 fF, which is a value previously measured on prototype chips [18], in parallel with a leakage current source of 10 pA. The red curves represent the input signals and show that the voltage step on the electrode is proportional to the collected charge. The blue curves represent the amplified signals on OUTA. The front-end gain is non-linear since the transistor M6 dynamically turns off as the output voltage rises, offering a larger impedance on the output node. At threshold, the gain is ≈ 1.9 mV/ e^- , whereas for a charge of 250 e^- , as seen in Fig. 4, it is ≈ 2.5 mV/ e^- . For larger charges, the analog output signal on OUTA is sufficiently large to push the cascode transistor M2 out of saturation and the front-end gain drops. This makes the cascode ineffective, so the equivalent input capacitance increases due to the Miller effect. The input signal is therefore lower during this transition time, as shown from the dashed red curve of Fig. 4, and a saturation of the analog output signal is reached. However, its Time over Threshold (ToT), i.e. the duration of the discriminator output pulse shown in green in Fig. 4, has a linear dependence on the input charge. Indeed, the ToT depends on the time required for the feedback circuit to charge up the capacitor C_S through the current I_{THR} .

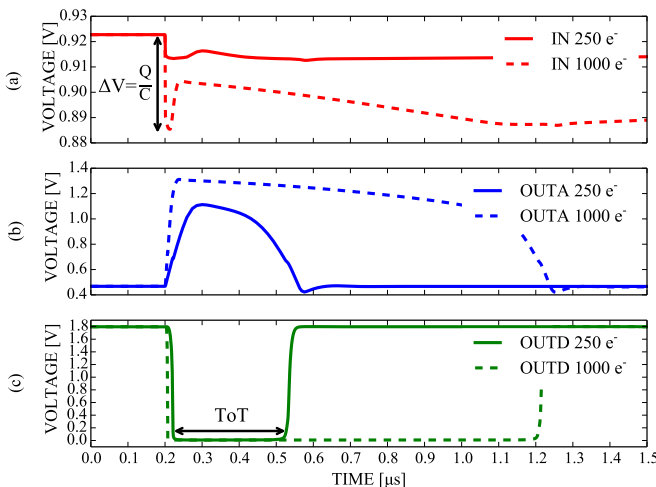


Fig. 4: Front-end simulated transient response with a 100 e^- threshold: signals at the (a) sensing node (b) output of the amplifier (c) output of the discriminator.

For a reliable operation of the sensor, the front-end ENC has to be considerably lower than the charge threshold. Even though the circuit is highly non-linear, a small-signal AC noise analysis helps to gain insights about the main noise sources. The results of this type of simulation are shown in the Table I which reports the highest contributions with the corresponding percentage of the output noise, integrated from 1 Hz to 10 GHz, i.e. in a frequency range much broader than the amplifier passband, which extends from ~ 15 kHz to ~ 10 MHz.

TABLE I: Output noise contributions

Device	Noise source	Percentage
M1	Thermal noise	53%
M4	Thermal noise	36%
D1	Shot noise	2.5%
M6	Thermal noise	2%
M5	Thermal noise	1.75%

The thermal noise of the amplifying devices M1 and M4 is the dominating noise contributor, as assumed in the previous section for the derivation of the power consumption as a function of the sensor capacitance. The next main contributor is the shot noise from the reset diode. The simulation was performed with a leakage current of 10 pA which is an overestimate for an unirradiated sensor. A small percentage of noise comes from the I_{THR} current source and the device M6 which define the baseline of the amplifier output. Other contributions to the output noise are much less significant. An important noise source not accounted for in the simulation is the Random Telegraph Signal (RTS) noise. Indeed, the simulation models do not include RTS noise which is therefore difficult to estimate during design. The most critical devices for RTS noise are again the transistors M1 and M4 whose sizing required an iterative process [10]. Increasing the gate area of the transistor M1 to combat RTS noise results in a larger effective sensor capacitance. A gate area of 0.18 μm^2 has been chosen since it is a good compromise between capacitance penalty and noise. A gate area of ~ 2.4 μm^2 has instead been chosen for the transistor M4 since it exhibits a larger noise transfer function to the output node and the RTS noise is typically larger in NMOS transistors. One of the main parameters for good noise performance is the size of the capacitance C_S : a larger capacitance provides dynamically more charge to the output node for the same input signal and improves the coupling between the input transistor source and the gate of the transistor M4. From a frequency standpoint, it widens the amplifier passband towards lower frequencies where the input signal has a large frequency content. The output signal therefore increases more than the noise level and a larger SNR is obtained. The PMOS transistor implementing this capacitor has a gate area of ~ 14.24 μm^2 , providing a capacitance of ~ 114 fF, and it is one of the largest components of the circuit.

Apart from the noise, another limit to the minimum operating threshold is the pixel-to-pixel variation of the transistor parameters which causes the threshold to vary over the matrix. It is well known that the transistors' mismatch scales down with the square root of their area [19]. The pixel size is

however limited and often dictated by the target sensor spatial resolution. To optimize the space, it is therefore necessary to identify the devices with the largest impact on the threshold dispersion and increase their area. In the amplification stage, the most critical devices are the transistors M5 and M6. As previously said, the current I_{THR} of the transistor M5 defines the speed of the feedback loop and significantly influences the amplifier gain. Regarding the transistor M6, its gate-source voltage directly defines the amplifier output baseline, setting the discriminator DC current and hence its switching threshold. The transistor M5 is biased with a current of only a few nA and therefore operates in weak inversion, which makes the impact of its mismatch even more prominent. For these reasons, it is designed with a low aspect ratio and a large area ($20 \mu\text{m}^2$). The size of the transistor M6, however, cannot be increased to the same extent because of the capacitance penalty on the output node. In the discriminator stage, the input transistor M9 is the main critical device: a variation of its threshold voltage directly shifts the switching point of the discriminator, appearing effectively as an offset. As for the transistor M6, it has to be kept small to prevent increasing the amplifier output capacitance and it represents the largest contribution (nearly 50%) to the overall threshold dispersion. Fig. 5 shows the front-end probability to generate a hit as a function of the input charge, obtained with transient-noise simulations (Fig. 5a) and Monte Carlo simulations for transistors' mismatch (Fig. 5b). The mean value of the Gaussian error function fit gives the nominal threshold, which is $\sim 100 \text{ e}^-$, whereas its standard deviation gives the ENC and the pixel-to-pixel threshold variation for the two simulations respectively, which are $\sim 6.4 \text{ e}^-$ and $\sim 2.5 \text{ e}^-$.

The radiation effects that influence the front-end operation and performance include the increase of the sensor leakage current due to NIEL and the TID effects that affect the transistor characteristics. For a good tolerance to NIEL, the front-end has been designed to cope with a wide range of sensor leakage currents. As for the tolerance to TID, minimum dimensions have been avoided for the critical devices to mitigate Radiation-Induced Narrow Channel (RINCE) and Short Channel (RISCE) effects [20]. Leakage currents in the order of a hundred pA have been measured for NMOS transistors in this technology after 20 Mrad of TID [21]. Since the I_{THR} current can be below 1 nA, the transistor M6 has been designed as an enclosed layout transistor (ELT [22]) and is surrounded by a p+ guard ring to prevent any leakage to neighboring devices. These precautions double its area but they are necessary to ensure radiation hardness. The layout of the pixel is shown in Fig. 6. The $2 \mu\text{m}$ octagonal collection electrode, distanced $4 \mu\text{m}$ from the surrounding p-well of the circuitry, is placed in the centre of the pixel. The front-end circuit occupies an area of $\sim 160 \mu\text{m}^2$ and is placed to the left of the collection electrode with other analog circuitry. The latter includes decoupling capacitors and a testing circuit which can capacitively inject a tuneable amount of charge to the collection electrode. The rest of the pixel is occupied by the digital readout circuitry for a total pixel area of $36.4 \mu\text{m} \times 36.4 \mu\text{m}$, leading to an analog power density of $75 \text{ mW}/\text{cm}^2$ over the matrix.

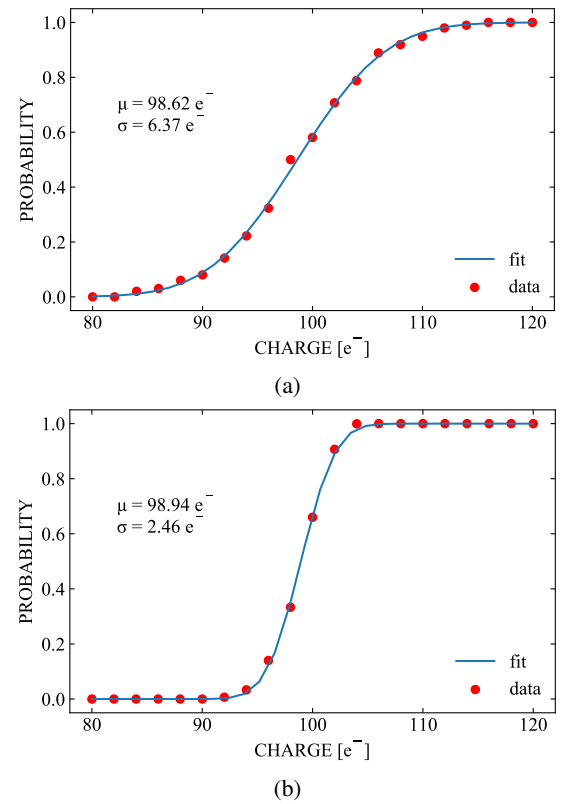


Fig. 5: Hit probability as a function of the input charge with simulated (a) transient noise and (b) transistors' mismatch.

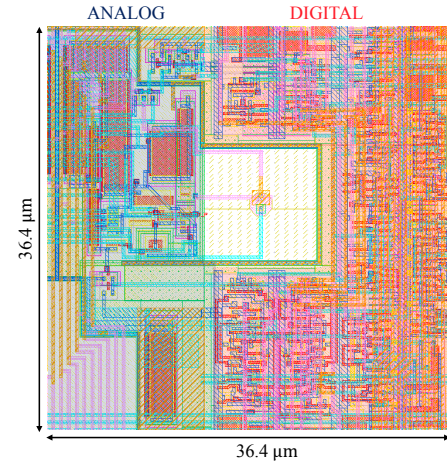


Fig. 6: Layout of the pixel.

The MALTA2 chip has a size of $10.12 \text{ mm} \times 20.2 \text{ mm}$ and integrates a matrix of 224×512 pixels. It features an asynchronous readout which avoids propagation of the clock in the matrix to reduce the digital power consumption. Upon a particle hit, the in-pixel digital circuitry sends a pattern of short pulses corresponding to the pixel address to the periphery on a digital data bus. The pixels are organized in double columns, where each double column has a dedicated bus for the transmission of the data down to the periphery. Here, a binary tree-like structure which merges the hits of the whole matrix onto a single bus is implemented. In case of simultaneous

events, this logic delays one of the two hits in time while keeping track of the delay for later reconstruction. The final word is 40 bits wide and is transmitted off chip via LVDS drivers, which are designed to operate at a maximum speed of 5 Gbps [23], sufficiently high for the pixel detector to cope with the ATLAS ITk outer layer hit rate of 100 MHz/cm². A micrograph of the MALTA2 chip is shown in Fig. 7.

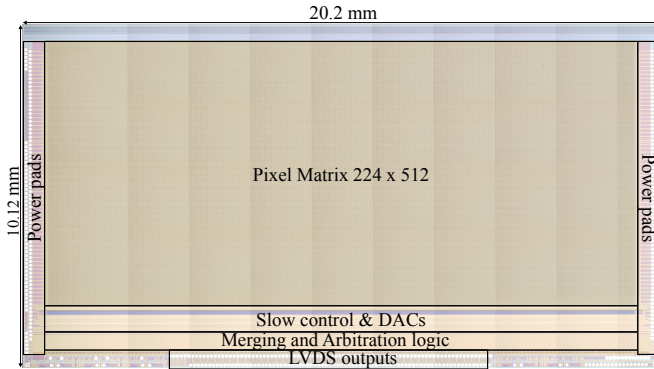


Fig. 7: Micrograph of the MALTA2 chip.

IV. FRONT-END CHARACTERIZATION

To test the performance of the front-end, a special set of pixels which allows the monitoring of its analog output has been included on the left and right side of the matrix. In these pixels, the front-end analog output is buffered to an output pad with a two-stage source follower with a gain close to 1. The first stage is optimized to match closely the discriminator input capacitance to have the same amplifier output load as in the other pixels of the matrix. An oscilloscope is used to monitor the output pad through a low-capacitance active probe and the full buffering system is designed not to degrade the signal timing. The front-end speed can be evaluated with the plot of Fig. 8 which shows the time walk curve, i.e. the time for the amplifier output to reach the discriminator threshold as a function of the charge. The conversion between charge and amplitude is derived through the charge injection circuitry. The injection capacitance was calibrated with ToT measurements of signals from test pulses and an ⁵⁵Fe source. For this measurement, the front-end operates with the nominal bias settings ($\sim 1 \mu\text{W}$ power consumption, as confirmed by measuring the total analog current consumption of the matrix) and the oscilloscope is set to trigger with a signal of $\sim 100 e^-$. The waveforms are collected while exposing the chip to a ⁹⁰Sr radioactive source which undergoes β^- decay emitting electrons that generate an ionization signal close to a Minimum Ionising Particle (MIP). The most probable value of charge deposition for a MIP in the 30 μm thick epitaxial layer is $\sim 1800 e^-$ [11]. The signal is collected by a cluster up to 4 pixels and the seed pixel, the one with the largest signal, has a charge $\geq 1/4$ of a MIP charge. Events with high charges ($\geq 1200 e^-$) have a threshold crossing time close to the minimum value of ~ 10 ns. With respect to the ATLAS application, an event is considered in time when it falls within 25 ns from this value. As can be noticed in Fig. 8, the in-time threshold corresponds to an input charge of $\sim 200 e^-$. Less than 10% of

the hits are below the in-time threshold. Statistically, these are mostly caused by non-seed pixels, with a neighboring seed pixel which is likely to collect a charge above the in-time threshold.

The front-end timing can also be studied through the matrix digital readout. An increasing amount of charge can be injected in a specific pixel with the aforementioned charge injection circuitry. The time of arrival of the generated hits can then be compared to a time reference. This procedure has been performed using as time reference the charge injection trigger pulse sent to the chip. In order to do so, this signal is also sent to an external 3 ps binning TDC [24] together with a fast-OR signal from the chip. The mean difference between these two signals' time of arrival provides a time walk curve compatible with the one in Fig. 8. This methodology, however, allows to better study the front-end jitter by evaluating instead the RMS difference of the two signals' time of arrival, which is plotted as a function of the charge in Fig. 9. For each injected charge, ten thousand events are acquired. The time jitter of the reference pulse has been estimated to be below 100 ps, therefore, the values in Fig. 9 are dominated by the front-end jitter which reduces from 4.7 ns at threshold, down to 0.16 ns for very high input charges.

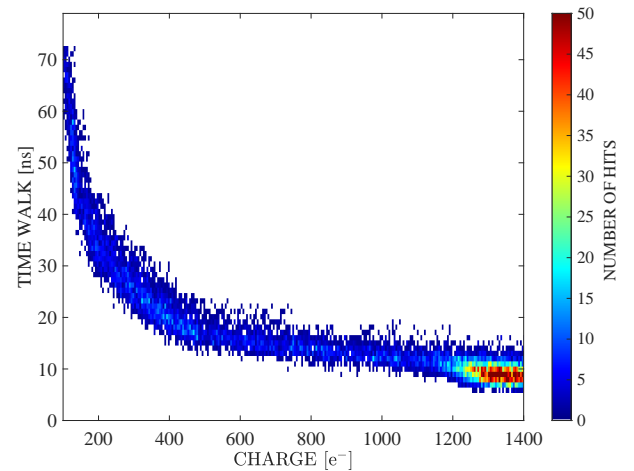


Fig. 8: Time walk curve obtained with a ⁹⁰Sr source.

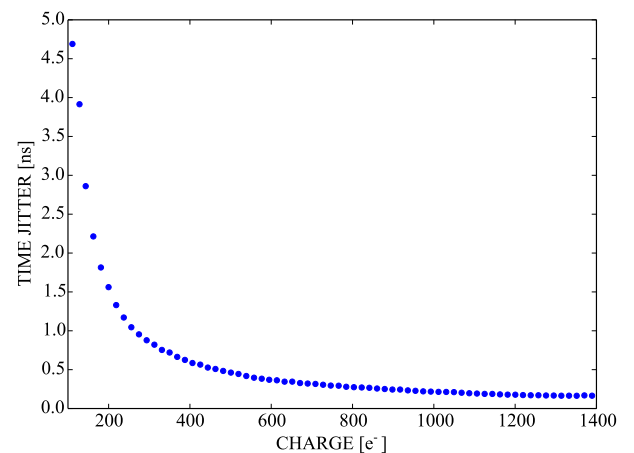


Fig. 9: Dependence of front-end time jitter on charge.

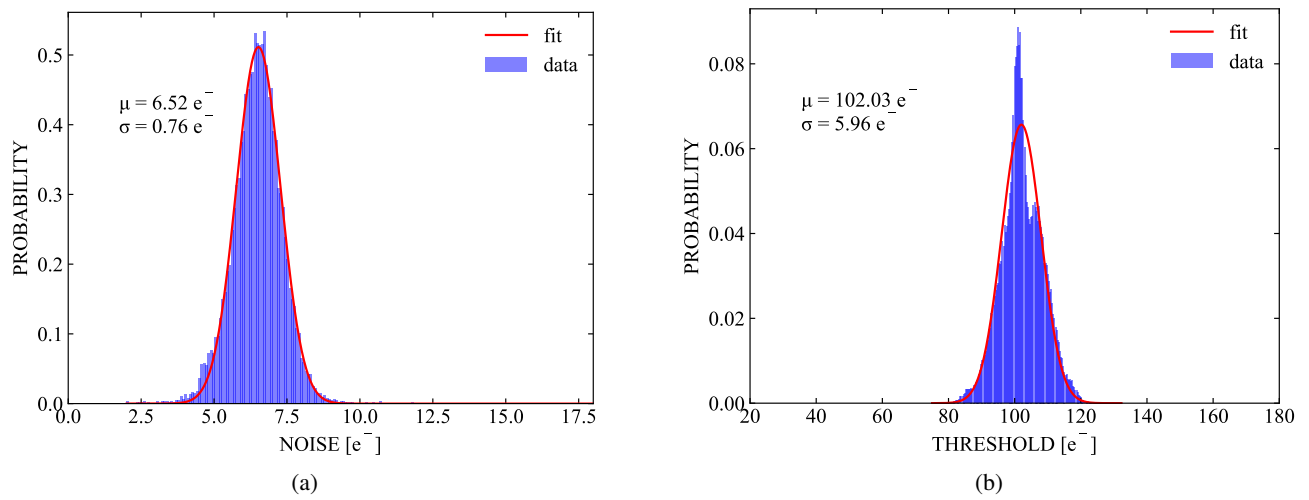


Fig. 10: Distribution of (a) ENC (b) threshold.

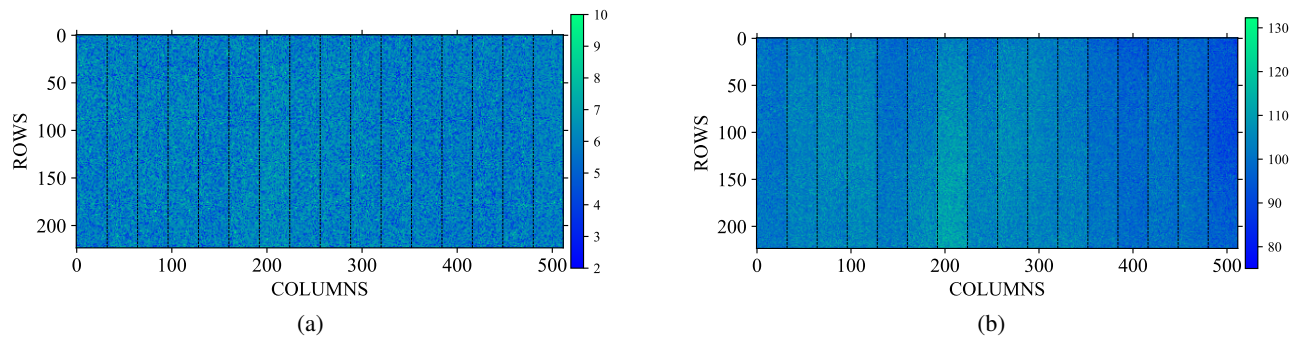


Fig. 11: 2D map for (a) ENC (b) threshold.

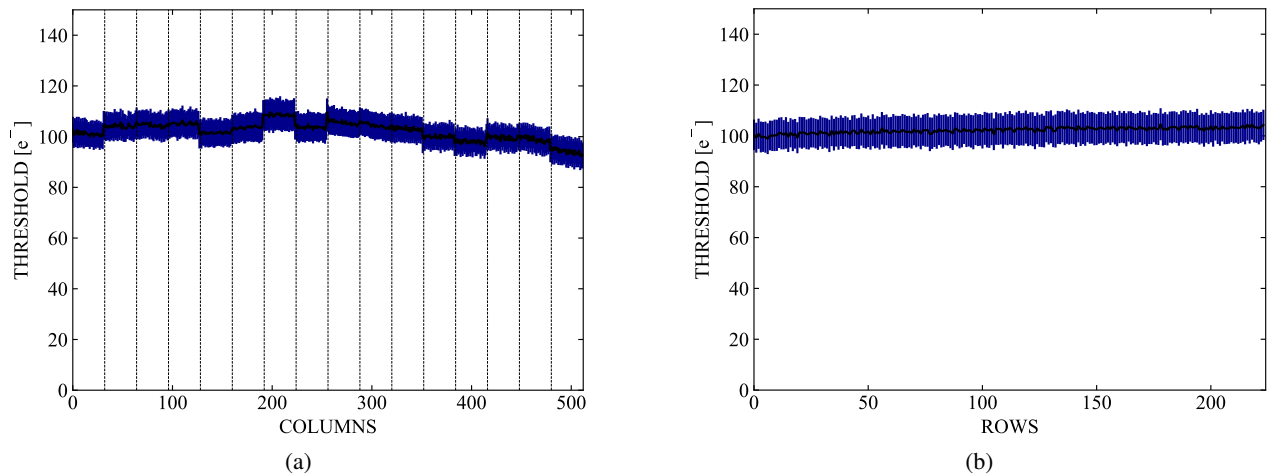


Fig. 12: Distribution of the threshold vs the (a) columns and (b) rows.

The charge injection circuitry also allows to extract information such as threshold and noise for all the pixels. Fig. 10 shows the threshold and noise distribution for an entire matrix with nominal front-end settings. The average threshold is $\sim 100 \text{ e}^-$ with a variation of $\sim 6 \text{ e}^-$, more than a factor of 2 higher than the simulated value shown in Fig. 5. The noise distribution has an average of 6.5 e^- with a low spread, matching fairly well the simulations. 2D maps of the pixels' threshold and noise are shown in Fig. 11. No systematic effects are observed for the noise. As for the

threshold, it is possible to notice a variation of its average over different vertical sections of the matrix. This effect strongly correlates with the scheme of the front-end biasing which is adjusted through DACs in the bottom periphery. The power pads are distributed only along the left and right side of the matrix. For this reason, a horizontal power voltage drop is inevitably present and is estimated to reach $\sim 12 \text{ mV}$ in the middle of the matrix. To compensate this effect and avoid a systematic threshold gradient, the biasing DACs have a dedicated mirroring stage for every 32 columns of the matrix

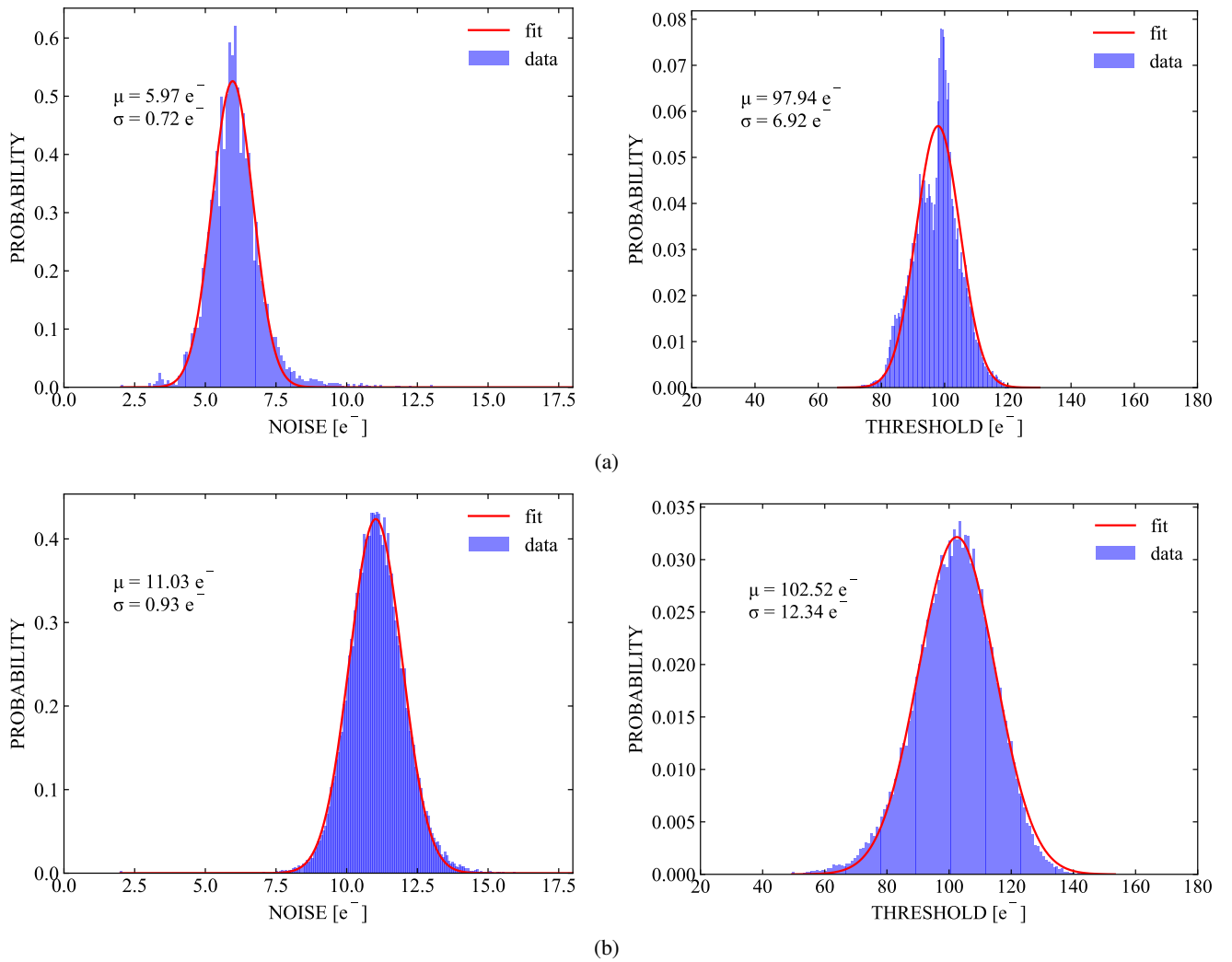


Fig. 13: Distribution of ENC and threshold with a threshold of ~ 100 e⁻ for (a) an unirradiated sample and (b) a sample irradiated at $3 \cdot 10^{15}$ 1 MeV n_{eq}/cm^2 and 3 Mrad.

which shares their local power supply. To better study the threshold behaviour, the distribution of the threshold along the columns with one RMS error bar is shown in Fig. 12a and here the threshold average variation at every biasing group is more clearly visible. A straightforward solution to increase the biasing transistors' area and mitigate this effect is to connect more mirroring stages together, trading-off with the power voltage drop compensation accuracy. This is envisaged for a future prototype. Fig. 12b illustrates the distribution of the threshold along the rows showing a slight vertical gradient which is caused by the mirroring stages at the matrix bottom which load the matrix power grid and introduce a vertical power voltage drop. Considering only pixels within the same biasing group and correcting the systematic vertical gradient, the threshold variation is ~ 5.1 e⁻. The variation of the NMOS transistors' output conductance with a high reverse bias to the bulk (beyond the normal supply voltage) is not fully covered by the simulation models and this is thought to be the cause of the discrepancy between the simulated and measured threshold variation. Even with a larger pixel-to-pixel mismatch, the chip can be operated reliably with thresholds of ~ 100 e⁻.

A number of chips have been irradiated with neutrons at the TRIGA reactor in Ljubljana [25] up to $3 \cdot 10^{15}$ 1 MeV n_{eq}/cm^2 of NIEL fluence. The chips also received a background TID of 1 Mrad for every 10^{15} 1 MeV n_{eq}/cm^2 . During irradiation, the chips were not powered. After irradiation, the chips are stored at a low temperature (below -20 °C) to avoid annealing of the radiation damage. For the same reason, all the measurements of irradiated samples are performed at -20 °C which also helps to contain the increase of the sensor leakage current. The chip still shows full functionality after these levels of irradiation.

Charge injection tests have been performed on these samples with a step of 10^{15} 1 MeV n_{eq}/cm^2 and 1 Mrad. For a fair comparison, the measurement of the unirradiated sample has been repeated at -20 °C and the I_{THR} current setting of the front-end has been adjusted to obtain similar thresholds in all the cases. An increasing level of ENC and threshold dispersion as a function of the irradiation level has been noticed. The distribution of ENC and threshold dispersion for an unirradiated sample and a sample irradiated to $3 \cdot 10^{15}$ 1 MeV n_{eq}/cm^2 and 3 Mrad are shown in Fig. 13 for reference. The noise average for the unirradiated sample is ~ 6 e⁻,

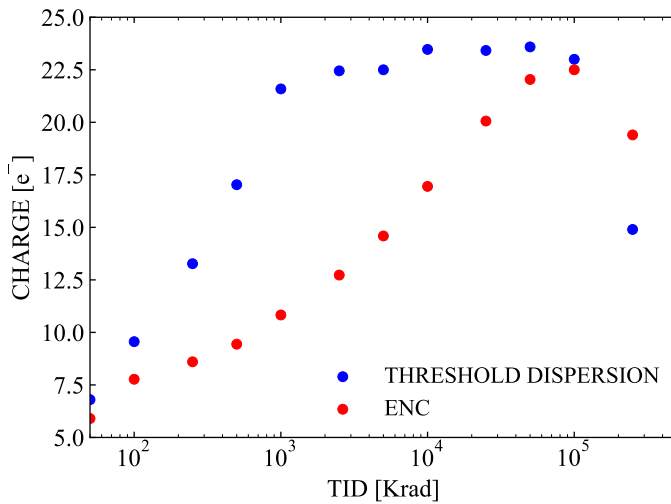


Fig. 14: Dependence of ENC and threshold dispersion on TID with a threshold of ~ 100 e^- . The points at 50 krad represent measurements before irradiation. The points at 250 Mrad and 500 Mrad correspond to measurements after 24 hours annealing at room temperature and additional 24 hours of annealing at 80 °C, respectively.

slightly lower than in the previous case due to the lower temperature, and increases to ~ 11 e^- for the sample irradiated at $3 \cdot 10^{15}$ 1 MeV n_{eq}/cm^2 and 3 Mrad. The lack of substantial non-Gaussian tails suggests a negligible contribution of RTS noise. The pixel-to-pixel variation increases from ~ 7 e^- in the unirradiated case to ~ 12.5 e^- for the sample irradiated at $3 \cdot 10^{15}$ 1 MeV n_{eq}/cm^2 and 3 Mrad.

To evaluate the front-end performance for higher TID levels, the chip has been irradiated with X-rays at a dose rate of 25 krad/min up to 100 Mrad. The chip still shows full functionality at this TID level. The irradiation was stopped at different doses to perform basic functionality tests and evaluate the front-end performance. In order to reproduce the typical operating conditions, the chip was powered and biased during irradiation. Additionally, to minimise annealing effects, the chip was kept at low temperature (-10 °C) during the whole process. The measured ENC and pixel-to-pixel threshold variation as a function of TID are shown in Fig. 14. The threshold was adjusted to ~ 100 e^- at each step of the measurement. The ENC grows monotonically from ~ 5.9 e^- before irradiation (first data point) to ~ 22.5 e^- at 100 Mrad. High levels of RTS noise are present in the ENC distributions for TID levels higher than 1 Mrad. However, already after 24 hours of annealing at room temperature, the RTS noise disappears and the mean ENC drops from ~ 22.5 e^- to ~ 19 e^- (data point at 250 Mrad). After other 24 hours of annealing at 80 °C, the mean ENC reduces to ~ 14 e^- (last data point). As for the pixel-to-pixel threshold variation, it increases from ~ 6.8 e^- before irradiation to ~ 23 e^- at 100 Mrad. The threshold dispersion more rapidly increases with TID compared to the noise, but it settles around ~ 23 e^- already at 1 Mrad. After 24 hours of annealing at room temperature, it drops to ~ 14.5 e^- and it further drops to ~ 9 e^- after other 24 hours of annealing at 80 °C.

V. CONCLUSION

This paper describes the design and characterization of a low-power, radiation-hard front-end circuit for monolithic pixel sensors. The circuit is implemented in the TowerJazz 180 nm CMOS imaging technology and integrated in the MALTA2 chip. The sensor features a small octagonal collection electrode with a diameter of 2 μm to achieve a low sensor capacitance (< 5 fF), which is key for low-power operation for a given ENC and bandwidth. Process modifications have been introduced to fully deplete the sensor and enhance the lateral electric field in the pixel corners for good tolerance to NIEL. The front-end is a continuously active open-loop amplifier followed by a high-gain common-source discriminator stage. It is designed for a gain of ~ 2 mV/ e^- and a peaking time in the order of tens of ns, requiring < 1 μW per pixel and a layout area of ~ 160 μm^2 . It is optimized for low noise and low pixel-to-pixel variation to achieve low charge thresholds. MALTA2 samples were extensively characterized to evaluate the front-end performance before and after irradiation. The main front-end metrics with a threshold of 100 e^- are summarized in Table II.

TABLE II: Front-end specifications with a 100 e^- threshold

Parameter		Value
Area		160 μm^2
Power consumption		1 μW
In-time threshold (for a 25 ns time window)		200 e^-
ENC	unirradiated	6.5 e^-
	$3 \cdot 10^{15}$ 1 MeV n_{eq}/cm^2 , 3 Mrad	11 e^-
	100 Mrad	22.5 e^-
Threshold dispersion	unirradiated	6 e^-
	$3 \cdot 10^{15}$ 1 MeV n_{eq}/cm^2 , 3 Mrad	12.5 e^-
	100 Mrad	23 e^-
Timing jitter	at threshold	4.7 ns
	for high charges (≥ 1200 e^-)	0.16 ns

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