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Energy Efficient Sensing using Steep Slope Devices

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par

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The problem is not the problem
The problem is your **attitude** towards the problem

— Captain Jack Sparrow —

Acknowledgements

As I am writing these words at the end of a 6 years-long journey navigating PhD life I realize none of it would have been possible without the help and motivation provided by countless other people, to whom I am forever grateful and indebted.

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In closing, I must acknowledge my old friends from the Polytechnic Institute in Bucharest - **Adrian** and **Suzana Gaspar**, **Bogdan Istrate**, **Ovidiu Alexandru** and **Mircea Zamfira** for feeding my hunger for awkwardly technical hobbies like building robots, and for the precious times we spent together in competitions - often in very exotic places (some long trips to Austria and Japan come to mind here) - over the past 8-9 years. A special place on the acknowledgements podium is reserved for **Cristina Teodorescu**, who over the course of many years supported and motivated me to keep going no matter what, and who also taught me a few life lessons that will surely serve me good going forward.

Last but not least, I must confess nothing would have been possible - quite literally - without the help of my dear parents - **Irina** and **Gabriel Rosca**. I want to thank them for imparting me with the desire to pursue this path towards achieving greater knowledge and wisdom, which is a journey that will probably continue forever. Never ceasing to believe in me, their invaluable advice, help and support throughout the years are the reason I am here, today, writing these words, and for that, I am truly grateful.

Thank you all, and enjoy the reading!

Lausanne, June 2022 Teodor Rosca.

Abstract

Today, we are witnessing the Internet of Things (IoT) revolution, which facilitates and improves our lives in many aspects, but comes with several challenges related to the technology deployment at large scales. Handling ever growing amounts of information that needs to be sensed, stored, transmitted and processed requires severe improvements in energy efficiency and smart distribution of computational power spanning from Cloud systems (handling Big Data in a massively parallel fashion) all the way to Edge devices (interfaces to the real world), where co-integration of sensing and computation plays a big role. Innovations in this field require the development of new device principles in existing technology platforms and/or new abundant and non-toxic materials that can enable electronic functions beyond the classical semiconductors, such as the field of oxide electronics that holds promise for both classical electronics functions and for future neuromorphic implementations. In this thesis, we explore both these aspects, having as a common denominator *steep slope devices*, which have the merit of offering a path for improved energy efficiency via voltage scaling. We particularly focus our work on their ability to serve energy efficient sensing functions that can be integrated with the computational platforms.

The first part of the thesis focuses on Tunnel Field Effect Transistors (TFETs) and how they can be used to perform similar tasks to Single Electron Transistors for qubit readout and also for serving as interfacing electronics. Such applications rely on cryogenic operation where conventional CMOS technology shows performance degradation due to low temperature effects such as dopant deactivation and carrier freeze-out. Our study shows that state-of-the-art heterostructure nanowire TFET arrays maintain excellent figures of merit over wide temperature ranges, down to the Kelvin regime, while simultaneously showing reduced temperature dependence once

Trap Assisted Tunnelling mechanisms are removed below 150K. Leveraging such properties, we suggest that TFETs are promising candidates as charge sensing devices for qubit readout architectures with high sensitivity to single or few elementary charges.

In the second part of the thesis we focus towards sensing architectures more suitable for Edge-of-Cloud (EoC) applications, by exploring phase-transition materials such as Vanadium Dioxide (VO_2). In this context, we explore the optimization of a Pulsed Laser Deposition (PLD) process in order to achieve high quality VO_2 thin films grown on CMOS compatible substrates, followed by electrical characterization of fabricated VO_2 two-terminal devices, which provides valuable data that aid us in developing compact SPICE-compatible device models. Built on top of the VO_2 resistor elements, we propose a novel Spiking Voltage-Controlled Oscillator (VCO) architecture that exhibits low device count (1 Transistor 1 Resistor - 1T1R) while at the same time providing frequency tuning capabilities in excess of 400% in the 10s of kHz range. We experimentally validate that the VCO cell can be used as a power-to-frequency transducer in a wide spectrum, ranging from near-UV, throughout the entirety of the visible domain, and as far as the Mid-Infrared and mmWave ranges, suggesting a new class of sensors capable of responding to a broad range of stimuli.

Key words: Steep-slope devices, tunnel field-effect transistor (TFET), band-to-band tunneling (BTBT), trap-assisted tunneling (TAT), low temperature electronics (LTE), cryogenic, charge sensing, metal-insulator transition (MIT), insulator-metal transition (IMT), vanadium dioxide (VO_2), pulsed laser deposition (PLD), Complementary metal-oxide-semiconductor (CMOS), voltage controlled oscillator (VCO), sensor, sensing platform, visible light sensing, infrared sensing.

Résumé

Nous assistons aujourd'hui à la Révolution de "l'Internet des Choses" (IoT en anglaise), qui facilite et améliore nos vies dans différents domaines, mais qui reste difficile, pour des raisons technologiques, à implémenter à large échelle. La gestion d'une quantité grandissante d'information qui doit être collectée, stockée, transféré et traitée requiert des améliorations significatives dans le domaine de l'efficacité énergétique et de la répartition "intelligente" de la puissance de calcul. Ces améliorations doivent s'étendre dans le domaine des systèmes "Cloud" (la gestion des Big Data de façon massivement parallèle) jusqu'aux dispositifs périphériques, qui font l'interface avec le monde physique et où la cointégration entre capteur et processeur joue un rôle majeur. Les innovations dans ce secteur nécessitent le développement de nouveaux principes dans les technologies existantes et/ou l'utilisation de nouveaux matériaux, si possible abondants et non-toxiques, qui permettraient de surclasser les matériaux semi-conducteurs classiques. A cet égard, un champ de recherche prometteur en électronique est celui des oxydes fonctionnels, qui peuvent servir à la fois dans les applications électroniques "classiques" ainsi que dans les futures implémentations neuromorphiques. Dans cette thèse, nous explorons ces différents aspects dont le dénominateur commun est le développement de dispositifs à pente raide ("Steep slope devices") qui montrent une meilleure efficacité énergétique en permettant le fonctionnement à des tensions plus basses. Nous concentrons particulièrement notre travail sur leur capacité à servir des fonctions de détection économes en énergie qui peuvent être intégrées aux plates-formes de calcul.

La première partie de la thèse se focalise sur les transistors à effet tunnel (TFETs), en particulier sur la manière dont ils peuvent être utilisés pour des taches similaires aux "transistors à un électron" (SET) pour la lecture des qubits ou pour servir d'interface électronique pour de tels systèmes. Ces différentes applications nécessitent

des opérations cryogéniques, où la technologie CMOS classique montre des performances suboptimales à basse température (à cause des effects comme le "dopant deactivation" et "carrier freeze-out"). Notre travail démontre que des “heterostructure nanowire TFET arrays” maintiennent d’excellentes propriétés pour une large plage de température aussi basse que <10K tout en montrant une dépendance à la température réduite une fois que les effets tunnel assistés par pièges (TAT) sont supprimés en dessous de 150K. Forts de ces propriétés, nous suggérons que les transistors à effet tunnel sont d’excellents candidats comme dispositifs de détection de charge pour la lecture des qubits (sensibilité à des charges élémentaires uniques).
Dans la seconde partie de la thèse, nous nous focalisons sur l’architecture des dispositifs permettant l’implémentation de technologies « Edge-of-Cloud » (EoC), particulièrement, en explorant des matériaux à transition de phase tel que le Dioxyde de Vanadium (VO2). Nous investiguons l’optimisation d’un processus de déposition de VO2, directement sur des substrats compatibles avec la technologie CMOS, via un procédé de dépôt par laser pulsé (PLD). Une fois les dispositifs produits, nous procédons à leur caractérisation électrique, avec pour objectif de développer des modèles de dispositifs compacts compatibles avec des plateformes SPICE. Construit directement au-dessus d’éléments de résistance VO2, nous proposons une nouvelle architecture de oscillateur commandé en tension (VCO) qui démontre un nombre reduit de dispositifs tout en fournissant des capacités de modulation de la fréquence en excès de 400% dans la gamme 10 kHz. Nous avons démontré expérimentalement que les cellules VCO peuvent être utilisées comme transducteurs de puissance à fréquence, dans une large gamme entre les UV, l’entièreté du spectre visible et jusqu’au infrarouge et la gamme des ondes millimétriques, démontrant ainsi une nouvelle classe de capteurs capable de répondre à un large éventail de stimuli.

Mots clefs : Dispositifs à pente raide, transistors à effet tunnel (TFET), effet tunnel bande à bande (BTBT), effet tunnel assisté par pièges (TAT), électronique à basse température (LTE), cryogénique, détection de charge, transition métal-isolant (MIT), transition isolant-métal (IMT), dioxyde de vanadium (VO_2), dépôt à laser pulsé (PLD), technologie complémentaire métal-oxyde-semiconducteur (CMOS), oscillateur controlé en tension (VCO), capteur, plate-forme de détection, détection de la lumière visible, détection de la lumière infrarouge.

Riassunto

Oggigiorno, siamo testimoni della rivoluzione riguardante l'Internet delle Cose (IdC, in inglese Internet of Things), che facilita e migliora le nostre vite in molti settori, la quale peró é accompagnata da diverse sfide relative alla produzione di nuove tecnologie su larga scala. Manipolare il crescente volume di informazioni che bisogna rilevare ('sensing'), conservare, trasmettere e processare richiede profondi miglioramenti in termini di efficienza energetica e distribuzione intelligente di potenza computazionale, che si estende dai servizi di Cloud (manipolazione di Big Data in operazioni parallele) fino ai dispositivi 'Edge' (le interfacce al mondo reale), dove l'integrazione tra il mondo del sensing e della computazione gioca un ruolo fondamentale. Le innovazioni in questo settore richiedono lo sviluppo di dispositivi basati su nuovi principi compatibili con le piattaforme tecnologiche esistenti e/o nuovi materiali abbondantemente presenti in natura e non tossici, che permettono nuove funzioni elettroniche che vanno oltre quelle date dai semiconduttori classici. Un esempio é l'elettronica basata su ossidi a effetto di campo, una tecnologia promettente sia in termini di classiche funzioni elettroniche sia per future implementazioni nel campo del calcolo neuromorfico. In questa tesi, esploriamo entrambi questi aspetti, avendo come comune denominatore i cosidetti dispositivi ad 'alta pendenza' (dispositivi a steep slope), i quali hanno la capacitá di offrire una migliore efficienza energetica attraverso la riduzione del potenziale elettrico necessario. Concentriamo il nostro lavoro sulla loro abilitá di fornire funzioni ad alta efficienza energetica, che possono essere integrate nelle piattaforme computazionali esistenti.
La prima parte della tesi si focalizza sui Tunnel FETs (TFETs) e su come possano essere utilizzati per implementare funzioni simili ai transistori a singolo elettrone (Single Electron Transistor – SET) per la lettura di qubit (bit per quantum computer) e anche come interfacce elettroniche. Tali applicazioni si basano sul funzionamento

a temperature criogeniche, temperature alle quali i dispositivi CMOS convenzionali sono caratterizzati da una degradazione delle prestazioni dovute a effetti esibiti a basse temperature, come la disattivazione dei dopanti e il congelamento dei portatori di carica. Lo studio che viene presentato in questa tesi mostra lo stato dell'arte dei nanowire TFET arrays, che mantengono un'eccellente figura di merito su un largo intervallo di temperature, fino a temperature minori di 10K mentre mostrano simultaneamente una minore dipendenza nel momento in cui meccanismi di Trap Assisted tunneling sono rimossi sotto i 150K. Sfruttando tali proprietá, consideriamo questi TFET promettenti candidati come sensori di carica per la lettura di architetture basate su qubit, con alta sensibilitá a singole o un ridotto numero di cariche elementari.
Nella seconda parte della tesi, focalizziamo la nostra attenzione su architetture sensoriali piú adatte per applicazioni relative all' Edge-of-Cloud, esplorando materiali a transizione di fase come il diossido di vanadio (VO_2). In questo constesto, esploriamo l'ottimizzazione di un sistema per deposizione a laser pulsato (Pulsed Laser Deposition – PLD), al fine di ottenere film sottili di VO_2 ad alta qualitá, depositati su substrati compatibili con tecnologie CMOS. Successivamente, presentiamo la caratterizzazione elettrica di dispositivi a due terminali basati su VO2, che forniscono dati preziosi che possono aiutarci nello sviluppo nuovi modelli SPICE compatti per questi dispositivi. Inoltre, proponiamo un nuovo Oscillatore controllato da voltaggio (VCO) basato su un elemento resistivo a VO_2, il quale esibisce un basso numero di dispositivi (1 Transtore 1 Resistenza – 1T1R), mentre contemporaneamente fornisce capacitá di regolabilitá della frequenza di oltre il 400% nell'intervallo di decine di kHz. Abbiamo sperimentalmente convalidato che una cella VCO possa essere utilizzata come trasduttore potenza-frequenza per un ampio spettro, che si estende dal quasi-UV, attraverso tutto lo spettro visibile, fino al semi-infrarosso e onde millimetriche, suggerendo una nuova classe di sensori capaci di rispondere a un largo spettro di stimoli.

Parole chiave: Dispositivi ad alta-pendenza, FET a effetto tunnel (TFET), tunnelling banda-a-banda (BTBT), tunnelling assistito da trappole (TAT), elettronica a bassa temperature (LTE), criogenia, sensori di carica, transizione metallo-isolante (MIT), transizione isolante-metallo (IMT), diossido di vanadio (VO_2), deposizione a laser pulsato (PLD), tecnologia complementare a metallo-ossido-semiconduttore (CMOS), oscillatore controllato da Voltaggio (VCO), sensore, piattaforma sensoriale, rilevazione di luce visibile, rilevazione di infrarossi.

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1 Introduction and rationale

The Internet-of-Things (IoT) represents an ecosystem of interconnected sensors and devices deployed at large scales that enables physical "things" such as computing devices, machines or objects to collect and transmit data continuously and communicate by leveraging network connectivity (internet or local networks). The IoT revolution is relevant today in a number of contexts, ranging from environment monitoring and agriculture, the automotive and manufacturing industry, all the way to personal healthcare and energy management in smart homes. As technology costs are lowering, increasing numbers of internet-capable devices and sensors such as smartphones or smart wearables are built and deployed, and contribute to the accelerated growth of the IoT ecosystem.

A direct consequence of the widespread nature of IoT "nodes" is the generation of vast amounts of data that is ever increasing [1] and that requires realtime, autonomous and secure information generation and processing, putting strain on the architecture of communication networks, standardization and, importantly, energy efficiency [2]. The emergence of IoT was accompanied by the development of Cloud and Edge-of-Cloud (EoC) technologies that enabled heavy computation and storage to be performed by networks of dedicated data centers while EoC devices handled data acquisition and interfacing with end-user devices (figure 1.1). Recently, however, focus is shifting towards performing smart computation at the EoC level, in order to circumvent possible limitations induced by the infrastructure or energy consumption and communication latency. For example, as the amounts of data that needs to be processed are growing, performing computation directly at the edge has a beneficial impact on energy efficiency and network throughput [3], saving energy and bandwidth associated with

uploading/downloading raw and processed data to and from the Cloud. In addition, certain critical functionalities such as those enabled by intelligent sensors used for healthcare require fast, realtime processing, in addition to ensuring data privacy and security [4]. As the growing amounts of data that need to be handled worldwide have pushed today's technologies into the "Zettabyte era" [1], the improvement in energy efficiency of both Cloud and EoC technologies is becoming challenging, with a new role being played by moving more "intelligence" to the Edge (such as the so-called "tiny machine learning" [5]). Energy efficiency, realtime processing and local intelligence opened new opportunities for the role of bio-inspired neuromorphic computing architectures and new devices and materials beyond the exclusive use of traditional silicon CMOS.

The rapid growth of Information and Communication Technologies (ICT) was enabled and accelerated in the latter half of the past century by breakthrough discoveries and inventions in the field of electronics such as the first transistor, developed at Bell Labs in 1947 [6], the first integrated circuit developed by Kilby and Noyce in 1959 [7], the invention and first production of the nowadays ubiquitous metal-oxide-semiconductor field effect transistor (MOSFET) in 1960 [8] and the evolution step represented by the Complementary Metal-oxide-Semiconductor (CMOS) platform that allowed to drastically reduce cost and improve performance of the fundamental digital building blocks for computing technology. In the years that followed, the microelectronics industry focused its resources on MOSFET miniaturization towards the nanoscale (with transistor dimensions smaller than 100nm). By decreasing transistor sizes, device capacitances decreased allowing for higher maximum operating frequencies which led to an increased overall performance of integrated circuits. In 1965 Gordon Moore (co-founder of Intel) observed based on the data available at that time that the number of devices comprised in integrated circuits increased steadily over time and predicted that such an increase would continue, doubling the number of components every two years [9].

The establishment of silicon-based CMOS technology, along with the development of precise semiconductor doping processes enabled the beginning of the "happy scaling" era, closely following Moore's prediction through the implementation of geometrical device scaling principles set forth by Robert Dennard in 1974 [10]. By following the constant field scaling laws proposed by Dennard, the industry was able to keep up with Moore's Law mainly by means of geometric scaling of transistor

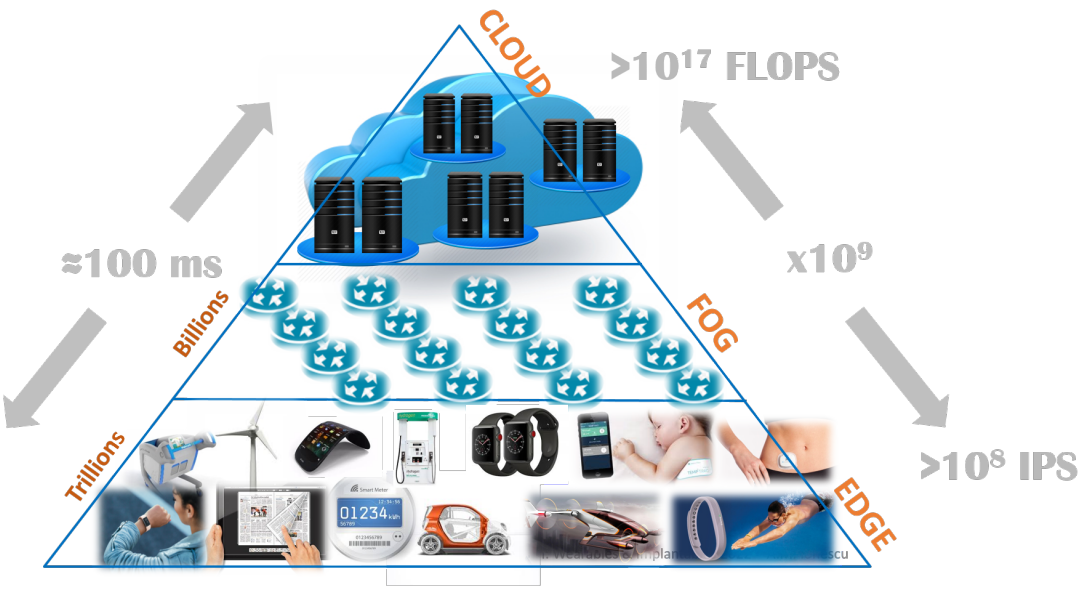


Figure 1.1: The Edge-to-Cloud information processing model for AI, suggesting unsustainable, inefficient and slow zettabyte data movement. Adapted from [1]

dimensions and the proportional increase in doping concentration and decrease in supply voltage necessary in order to satisfy the constant electric field guideline. As the trend continued, the introduction of technology boosters was necessary in order to overcome limitations that were not detectable in early, larger technology nodes. Notable examples include the adoption of high-κ dielectrics and metal gates [11] and strain-engineered Si and SiGe channels with increased carrier mobility [12].

Based on all technological innovations, Moore's Law has been respected and followed by the industry for decades to reach device densities of more than 100 million transistors per mm^2 but today it is facing a triple challenge: (i) limits of physics and principles, (ii) limits of energy efficiency, and (iii) limits of costs per transistor that started to slightly increase for technologies below 28nm.

In this complex context, the development of new materials and device concepts has an increasingly important role with two main trends that are recognized by the nanoelectronics community: (i) **scaling the operation voltage** (and consequently increase the energy efficiency) of digital and analog electronics, and (ii) **providing new functionalities** beyond the one of conventional MOSFET devices.

Within the first category, the classes of so-called steep slope switches emerged after

2010, among which Tunnel FETs [13–15], Negative Capacitance FETs [16–18] and Nano-Electro-Mechanical (NEM) switches [19–21]. Interestingly, in this quest, the phase change switches (based on the reversible metal-insulator transition in functional oxide materials) offer an interesting and promising combination of both steep-slope switching and new functionality, linked to their hysteretic behavior and to their high sensitivity to a large number of external stimuli like temperature, electromagnetic waves, light, strain, magnetic fields. [22].

Therefore, in this work we decided to focus on two classes of devices: (i) **Tunnel FETs for charge detection** (especially in the context of necessary alternative charge detectors to Single Electron Transistors (SETs) at deep cryogenic temperature) and (ii) **Phase-change switches to build new spiking sensors** architectures serving some of the challenges of IoT and Edge Artificial Intelligence (Edge AI) with innovations from materials to devices to circuit level. While for the first topic we established a cooperation with Lund University for providing some of the most advanced nanowire Tunnel FETs, on the second topic we have developed and optimized a technology based on Vanadium Dioxide (VO_2) that can be co-integrated with CMOS in order to build new classes of spiking oscillators serving to develop multiple classes of sensors capable of detecting different types of stimuli. We particularly focused on this direction, from technology, to analytical modeling and experimental validations.

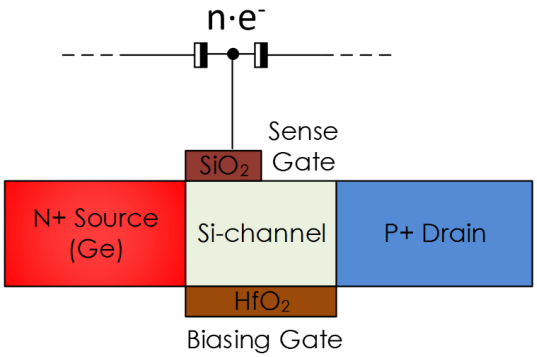
Therefore, the manuscript is organized in four chapters, dealing with the following topics: Chapter 2 - Charge sensing for Qubit readout using Tunnel FETs, Chapter 3 - Phase transition characteristics of VO_2 thin films, Chapter 4 - A 1T-1R Spiking Voltage Controlled Oscillator based on VO_2, and Chapter 5 - VO_2 Oscillators for sensing. Chapters 3, 4, and 5 are highly interconnected as they jointly deal with the field of VO_2-based spiking sensors, while Chapter 2 is a rather standalone work on the evaluation of an external technology.

This work has been carried out in the context of the Millitech ERC Advanced Grant, aiming at a novel technology platform that serves both computation and sensing using steep slope switches that exploit new device physics and concepts with the ultimate goal to achieve operation at voltages below 100 millivolts, which enabled collaborative work between a number of PhD students and post-doctoral fellows at EPFL.

1.1 Thesis Outline

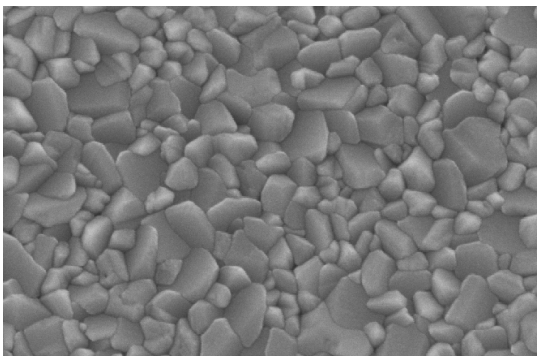
This thesis is structured as follows:

Chapter 2: Charge Sensing for Qubit Readout using Tunnel FETs



In this chapter we evaluate the functionality of Tunnel FETs at low temperatures with focus on liquid-helium temperatures as low as 10K. We perform an experimental study using state-of-the-art heterojunction nanowire TFET arrays and observe that their analog and digital figures of merit are quasi-insensitive to temperature variations when BTBT remains the dominant carrier transport mechanism. Continuing, we propose that double-gate TFETs could harness the temperature-insensitive steep subthreshold slope to provide enhanced sensitivity towards single or few elementary charges. To this end, we validate the sensing concept via TCAD simulations and propose an optimization strategy for increasing sensitivity to elementary charges. In closing, we perform an experimental proof-of-concept using Silicon-on Insulator SiGe/Si line tunneling TFETs.

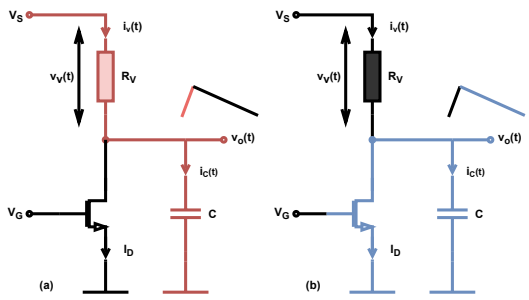
Chapter 3: Phase transition characteristics of VO_2 thin films



In chapter 3 we become familiar with Vanadium Dioxide (VO_2), a functional oxide which represents a promising candidate towards achieving new and interesting functionalities in electronics. We provide an overview on the multitude of stimuli that VO_2 is sensitive to, outlining its importance for novel sensing architectures. We continue by establishing an optimized set of growth parameters by Pulsed Laser Deposition focusing on CMOS

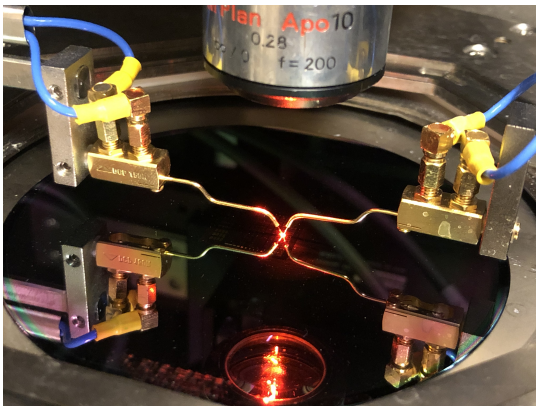
compatibility. We study the influence of Laser fluence and Oxygen partial pressure during deposition and establish an optimal "growth window" - a set of growth parameters that ensure reproducible, high quality CMOS-compatible VO_2 depositions.

Chapter 4: A 1T-1R Voltage Controlled Spiking Oscillator based on VO_2



In this chapter we explore the simple but interesting implementation of a 1Transistor-1Resistor (1T-1R) voltage controlled oscillator based on two-terminal VO_2 devices. We perform static and dynamic analyses of the circuit and find that key metrics of the oscillating output such as frequency and amplitude are closely correlated to the intrinsic properties of the VO_2 device, such as phase transition thresholds and electrical resistance, suggesting that the VCO can be used as a compact sensing unit that exploits the sensitivity of VO_2 towards a wide variety of stimuli.

Chapter 5: VO_2 Oscillators for optical sensing (and beyond)



In the final chapter of this work, we continue the journey set forth at the end of chapter 4 and experimentally validate the functionality of the VO_2 spiking oscillators as sensors. In the first study we investigate the sensitivity of VO_2 intrinsic device parameters and oscillator output towards visible light radiation ranging from near UV to near infrared light in eight distinct wavelength bands. We find that oscillation frequency is strongly dependent on incident power and wavelength, with higher sensitivities towards the short-wavelength end of the spectrum. We continue the exploration of sensing functionality by "illuminating" the VO_2 device with RF mmWave power via coplanar waveguides

and we find that the sensitivity of the VCO circuit is preserved also in this region of the spectrum. The final chapter ends with the proposal of a SPICE-compatible device model that aims to capture key behaviors of VO_2 such as its hysteretic resistance-temperature characteristic and effects of self heating and external power stimuli.

2 Charge Sensing for Qubit Readout using Tunnel FETs

2.1 Introduction

The aggressive geometric scaling of the feature size in the now ubiquitous CMOS technology has had an extraordinary impact on circuit performance, with considerable improvements being made in terms of switching speed, device density, functionality and cost [13]. A direct consequence of geometric scaling, however, is the proportional reduction of supply voltage required to maintain the constant electric field , as per Dennard's scaling laws [10]. However, supply voltage scaling needs to be accompanied by a corresponding decrease in threshold voltage V_T. Although not specifically required by Dennard rules, scaling of the V_T is necessary in order to ensure sufficient overdrive voltage $V_{OV} = V_{DD} - V_T$, as this directly influences the maximum achievable on-current $I_{ON} \propto (V_{DD} - V_T)^2$, which is required for high performance operation of digital circuits, particularly related to switching capacitive loads at high speeds thus ensuring high operating frequency.

In addition, the behavior of the MOSFET in the subthreshold regime (where the semiconductor channel is in weak inversion and the drain current is diffusion-dominated) is of fundamental importance for applications that require low-power operation, as it determines the MOSFET's behavior when switching between off- and on-state, indirectly affecting static power dissipation in logic circuits.

The steepness of the transition between off- and on- states in MOSFETs is dictated by the Subthreshold Slope (SS), a parameter that describes the relationship between gate voltage V_G and drain current I_D in weak inversion, and can be expressed as:

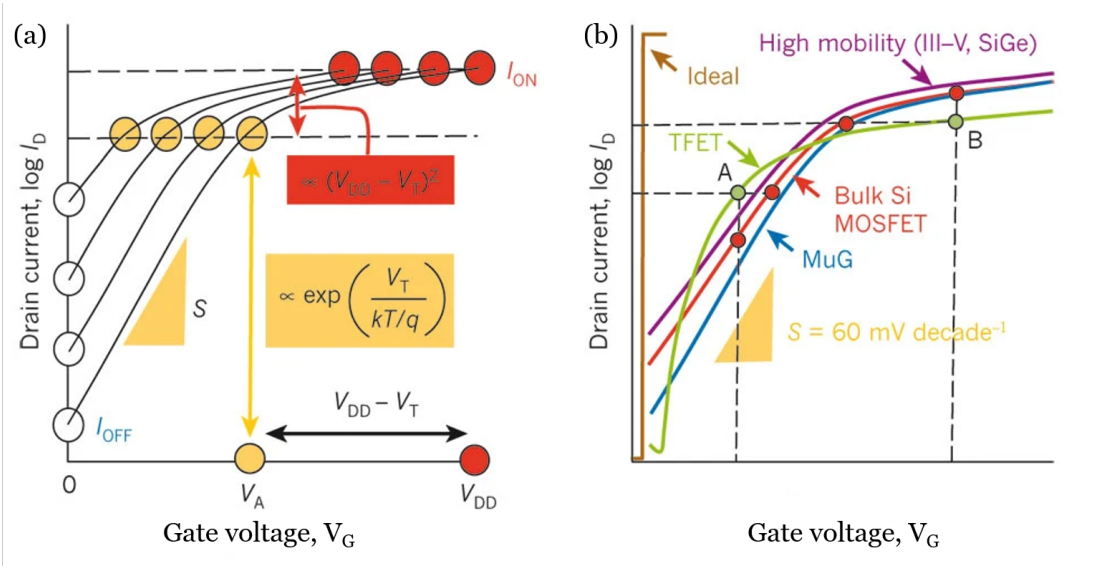


Figure 2.1: (a) - Qualitative representation of the exponential increase in I_{OFF} as a consequence of supply voltage reduction; (b) - A comparison of transfer characteristic for a bulk Si MOSFET alongside a Tunnel FET, a high-mobility channel MOSFET a multi-gate MOSFET and an ideal switch. The TFET can offer a steeper subthreshold slope at the cost of lower on-current. Adapted from [13]

$$S = \underbrace{\frac{\partial V_G}{\partial \Phi_S}}_{\text{m}} \underbrace{\frac{\partial \Phi_S}{\partial (log_{10} I_D)}}_{\text{n}} = \left(1 + \frac{C_d}{C_{ox}}\right) ln10 \frac{kT}{q}$$

where Φ_S represents the surface potential, and its relationship to gate voltage is given by the gate to channel coupling, also known as the "body factor" $m = 1 + C_d/C_{ox}$ and depends on the depletion layer capacitance C_d and the gate oxide capacitance C_{ox}. The second factor n represents the relationship between surface potential Φ_S and drain current, and is determined by the charge injection mechanism. In MOSFETs, the mechanism is represented by the thermionic emission of carriers [23] and the n term is described by $n = ln10(kT/q)$ where k represents the Boltzmann constant and q is the electron charge.

In a best-case scenario, where a body factor $m = 1$ can be achieved, the minimum SS remains limited by the charge injection mechanism, and the minimum subthreshold slope SS reduces to 60 mV/dec, assuming operation at room temperature $T = 300K$. The inferior limit of SS has strong consequences upon reducing the supply voltage V_{DD} and threshold voltage V_T accordingly. The transfer characteristic of a MOSFET with

subthreshold slope S is represented in figure 2.1(a) and describes that any decrease in supply voltage V_D is accompanied by a decrease of threshold voltage V_T and the increase in off-current I_{Off} at a rate that is determined by the subthreshold slope S. Consequently, if SS is limited to no less that 60mV/decade, this implies that a supply voltage decrease of only 60mV is sufficient to cause a ten-fold increase in off-current which results in a considerable impact on standby power consumption.

In order to circumvent this limitation, electronic switches that exhibit steeper turn-on characteristics are desirable, ideally preserving high on-current I_{ON} capability as well as exhibit off-currents I_{OFF} as low as possible, with a transfer characteristic close to that of an "ideal" switch, as depicted in figure 2.1(b).

2.1.1 The Tunnel FET

The Tunnel FET (TFET) represents a promising solution to circumvent the SS limitations imposed by the thermionic emission mechanism in MOSFETs. The most common TFET architecture is the gated p-i-n diode operated in reverse bias [24]. The

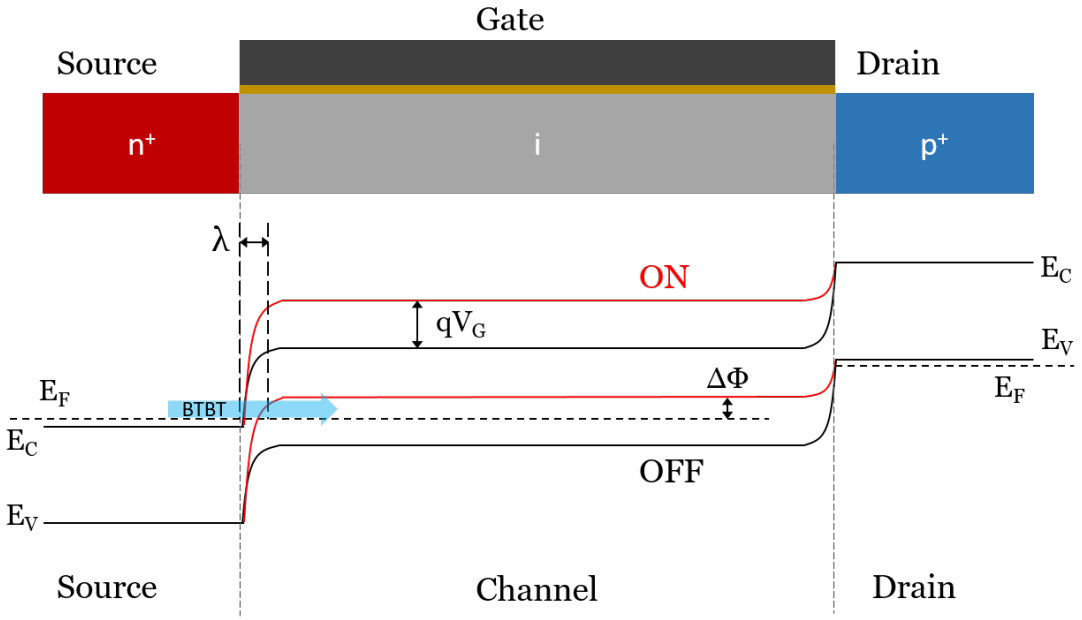


Figure 2.2: (top) - Schematic diagram of a planar p-Type TFET and (bottom) - Qualitative band diagram showing how the gate bias V_G can induce an overlap between the source conduction band and the channel valence band which enables band-to-band tunneling at the source-channel interface.

typical structure of a p-type TFET is shown in figure 2.2 highlighting the doping profile required to obtain TFET functionality: The source region is heavily n-doped, and the drain region is p-doped, while the semiconductor region between the source and drain remains undoped (intrinsic). Such a dopant distribution results in the band diagram represented qualitatively in figure 2.2(bottom), assuming a negative drain voltage is applied. In such a structure, the transistor effect is obtained by controlling the onset of a band-to-band tunneling (BTBT) current between the source and channel regions, utilizing the electrostatic control provided by the gate contact. In the p-type TFET illustrated in figure 2.2, a negative gate bias pulls the channel bands upward, introducing an overlap between the conduction band of the source region and the valence band of the channel region. As the negative gate bias pulls the valence band edge in the channel above the conduction band edge of the source region, electrons in the energy window highlighted by the blue arrow in figure 2.2 can tunnel across the source/channel interface, establishing a current flow from the source region to the drain region [13]. The current therefore depends on the source-channel band-to-band tunneling probability, which can be calculated using the Wentzel-Kramer-Brillouin (WKB) approximation [13, 24]:

$$T_{WKB} \approx exp\left(-\frac{4\lambda\sqrt{2m^*}\sqrt{E_g^3}}{3q\hbar(E_g+\Delta\Phi)}\right) \tag{2.1}$$

where λ represents the spatial extent of the source-channel tunneling region, m^* is the tunneling effective mass, E_g represents the bandgap, and $\Delta\Phi$ represents the energy difference between the source conduction band and the channel valence band. In the case of the p-TFET shown in figure 2.2, applying negative gate bias results in a reduction of λ and an increase of $\Delta\Phi$, which increases the tunneling probability T_{WKB} and enables the onset of tunneling current at the source-channel interface. Moreover, since only the carriers in the energy window defined by $\Delta\Phi$ can tunnel across the source-channel interface, the high-energy part of the source Fermi distribution is filtered, which makes it possible for TFETs to achieve SS values below 60mV/dec [13].

The TFET can, therefore, outperform the MOSFET in low power and low current applications where the steeper subthreshold slope of the TFET can be exploited. However, TFETs commonly exhibit lower on-current, as shown in figure 2.1(b), due to

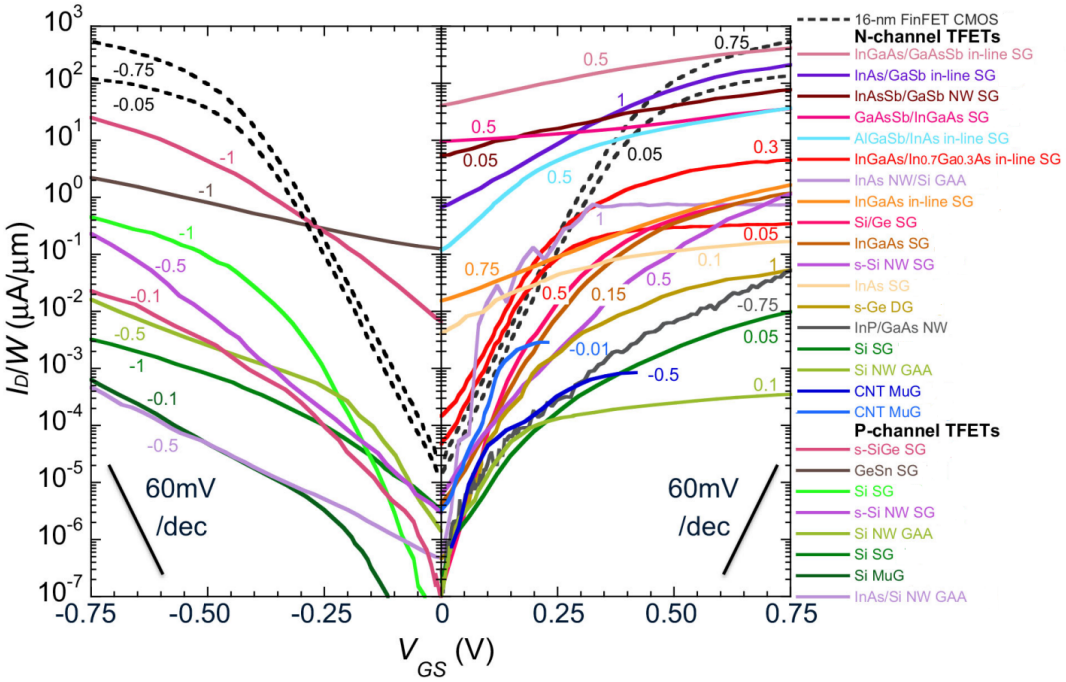


Figure 2.3: A comparison of several published TFET transfer characteristics compared to a commercial 16 nm low-power Fin-FET. Adapted from [14] with data from [25–49]

the limited "transparency" of the tunneling barrier [13] causing a lower probability of the tunneling mechanism when compared to the probability of thermionic emission in a MOSFET.

As a consequence, research efforts have been made into identifying performance boosters for the TFET technology, with the aim of obtaining devices that exhibit both a steep SS, while at the same time providing sufficiently high I_{ON}, desirable figures of merit for the implementation of logic circuits. A collection of TFET transfer characteristics obtained by several research groups is represented in figure 2.3, and are compared with the the transfer characteristic of a commercial 16nm Fin-FET (MOSFET) [14]. Considering the different material classes and architectures analyzed, it can be noticed that the TFETs analyzed all exhibit on-currents I_{ON} lower than the reference MOSFET. Particularly, although they exhibit lower off-current I_{OFF} and subthermal or close to subthermal SS, TFETs that are based on Si homojunctions generally register the lowest I_{ON}, which suggests that the Si platform may not be optimal for the development of high performance TFET technologies. This is caused by Silicon exhibiting a relatively high indirect bandgap that negatively impacts BTBT probability.

This effect may be alleviated by the use of strain engineering and integration with germanium (Ge). For example, Blaeser et al. [50] reported a SiGe/Si TFET that exploits line tunneling parallel with the electric field induced by the gate and obtained I_{ON} values as high as 6.7 $\mu A/\mu m$ at supply voltages of 500mV. Although not subthermal, the SS was reported at 80mV/dec over four decades of I_D.

The implementation of TFETs using III-V materials can also provide an interesting alternative, due to their lower effective mass and lower, direct bandgap and both effects influence tunneling probability beneficially. Of the III-V TFETs analyzed in figure 2.3, heterojunction III-V devices show the highest values of I_{ON}, however also reporting degraded SS, despite the fact that there doesn't seem to be any fundamental limitation towards achieving subthermal SS in heterojunction III-V TFETs [14] and performance is expected to improve with fabrication optimization and electrostatic control enhancements. Indeed, in 2016 Memisevic et al. [51] reported a highly scaled vertical nanowire InAs/GaAsSb/GaSb with a minimum SS of 48mV/dec at supply voltages ranging from 100 to 500mV and I_{ON} values as high as 10.6 $\mu A/\mu m$ followed in 2017 [52] by an InAs/InGaAsSb/GaSb nanowire TFET with a demonstrated minimum SS of 43 mV/dec and an I_{ON} = 10.4$\mu A/\mu m$, achieved through excellent electrostatic control enabled by the Gate-All-Around architecture, aggressive scaling down to nanowire diameters of 20nm and a graded tunneling junction design that helped reduce trap density at the tunneling junction interface.

The steep turn-on characteristic achievable by Tunnel FETs is an attractive feature for analog applications that exploit the subthreshold regime. Most notably, the steep subthreshold slope of TFETs is a feature that is highly beneficial for the development of biosensors, where label-free detection of biomolecules can be achieved with better sensitivity than by using conventional FETs [53–55]. In addition, Dubey et al.[56] recently investigated the impact of mechanical strain on monolayer $MoSe_2$-based TFETs and indicated that uniaxial tensile strain causes an increase in both I_{ON} and I_{OFF} and proposed the design of an ultrasensitive strain sensor, suggesting a sensitivity $\Delta I_D/I_D \approx 3.61$ for a strain of 2%.

These studies suggest that in addition to being worthy candidates for low-power low-current digital applications where low supply voltages are required, Tunnel FETs can also play a role in analog applications and the development of new sensing architectures that exploit the steep subthreshold in order to achieve higher sensitivities.

2.2 Cryogenic Tunnel FETs

Low temperature electronics (LTE) has proven to be a valuable and sometimes unique method of performing certain processing tasks. It has been shown that the impact of low temperature on carrier transport and key CMOS performance parameters such as current, conductance, drift velocity, and noise margin is extremely beneficial[57]. As a consequence, cryogenic electronics has relied on traditional CMOS technology, making use of performance improvements brought about by going down to liquid nitrogen temperatures (80K). LTE is also a domain that enables certain applications that are completely inaccessible at room temperatures, such as superconducting structures and Josephson devices[58, 59].

One particular application that falls in this category is Quantum Computing[1, 60, 61]. Recent advancements in this field have triggered new studies on the viability of using advanced CMOS platforms in the 1-10K temperature range[62]. Its purpose would be to support the implementation of readout and control electronics compatible with semiconductor qubits that would need to function in the sub-100mK range. As this technology develops further, constraints may become even more stringent in the future, with increasing number of physical qubits and associated logic qubits for error correction[63, 64], as this drastically impacts the number of interconnects that should be optimized. In this very low temperature range CMOS technology experiences significant degradation generally associated with carrier freeze-out, dopant deactivation, hysteretic effects, and kinks in the output characteristics. In addition, common CMOS analog parameters and subthreshold swing are highly dependent on temperature, which adds another degree of complexity to an already difficult problem[65].

Tunnel FETs hold tremendous potential for LTE, and especially deep cryogenic operation, as they rely on quantum mechanical BTBT as main carrier transport mechanism, as opposed to thermionic emission such as the case for CMOS. BTBT shows very low dependence on temperature, limited only by the quasi-linear temperature coefficient of the semiconductor bandgap[66]. However, BTBT is accompanied by Trap Assisted Tunneling in the vicinity of room temperature, and this comes as a detrimental effect that severely degrades the superior performance that would be attainable by BTBT alone. Such effects have been studied mostly in individual Tunnel FET devices with limited current capability [15] and the TAT in arrays of nanowire Tunnel FETs, nec-

essary to produce a useful high level of current, was scarcely reported. Additionally, some authors [67] have demonstrated that at low temperatures, the effect of TAT in Tunnel FETs is minimized and band-to-band-tunneling could prevail as the main carrier transport mechanism.

2.2.1 Experimental Methods

The low-temperature measurements presented in this chapter have been performed using a SUSS MicroTec PMC150 cryogenic probing station, shown in figure 2.4. The PMC150 uses a continuous-flow cryostat system designed for low liquid gas consumption compatible both with liquid nitrogen (LN_2) and liquid helium (LHe), allowing a Device-Under-Test (DUT) to be measured at temperatures ranging from room temperature down to 10K. To avoid freezing and formation of ice crystals, the chamber is kept under high vacuum using a combination between a backing diaphragm pump and a high-performance turbomolecular pump capable of achieving pressures lower than 10^{-5} mbar. All measurements taken between 300K and 80K have been performed using LN_2 refrigeration, while measurements below 80K and down to 10K were performed using LHe. The probing needles are mounted on micromanipulators that rest on a stainless steel shield actively cooled by the backflow of the main chuck cooling system. This allows the shield to protect the DUT from external thermal radiation while

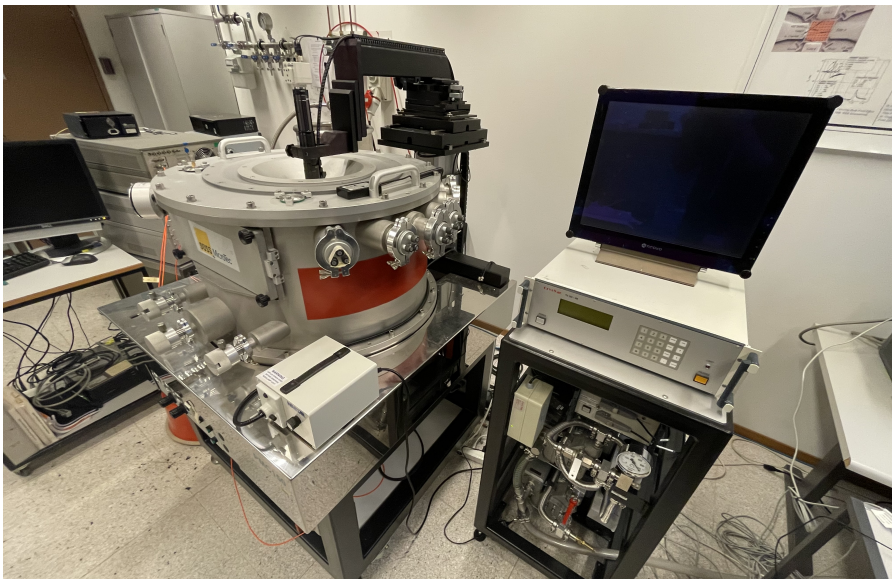


Figure 2.4: The SUSS MicroTec PMC150 Cryogenic probing station

also keeping the probing needles cool for minimum temperature gradients. Finally, transfer and output characteristics were acquired using a HP4155 Semiconductor Parameter Analyzer used in conjunction with the IC-CAP device characterization software.

2.2.2 Devices under test

The measurements presented in this section have been performed on devices kindly provided to us by the authors of [52, 68]. In addition, the results and measurements discussed here have been published and presented in [69].

For this study we have focused on two devices based upon relatively similar nanowire geometries, but with considerably different multiplicities, such that we can identify a Small Array (SA), with a multiplicity of 4 nanowires, and a Large Array (LA), nominally consisting of 184 nanowires connected in parallel. The purpose of this choice was to assess whether the inherent variability between devices that originates from the fabrication process can be averaged out. As shown in figure 2.5(b), each individual nanowire consists of three segments InAs, $In_xGa_{1-x}As_ySb_{1-y}$, and GaSb. The segments have lengths of 160/80/300nm and 190/90/330nm for the LA and the SA, respectively. Segment diameters are also slightly different between the two arrays, with nominal values of 20/22/53nm and 25/27/53nm for the LA and the SA, respectively.

The authors of [52, 68] engineered the nanowires such that they achieve superior electrostatic control over the channel by aggressively scaling the diameters down to $\approx 25nm$ and taking advantage of the Gate-All-Around geometry. In addition, the

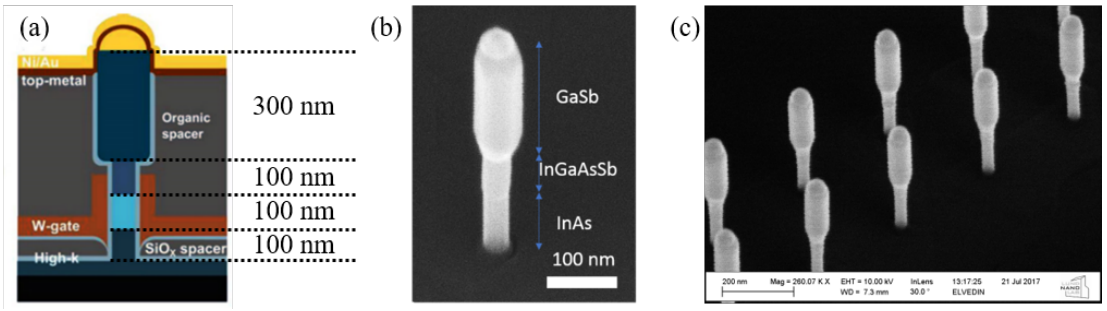


Figure 2.5: (a) - Cross sectional view of the InAs/$In_xGa_{1-x}As_ySb_{1-y}$/GaSb Nanowire Tunnel FET; (b) - SEM image of a single nanowire, indicating the individual segments; (c) - SEM image of a section of the 184 nanowire Large Array - Adapted from [69]

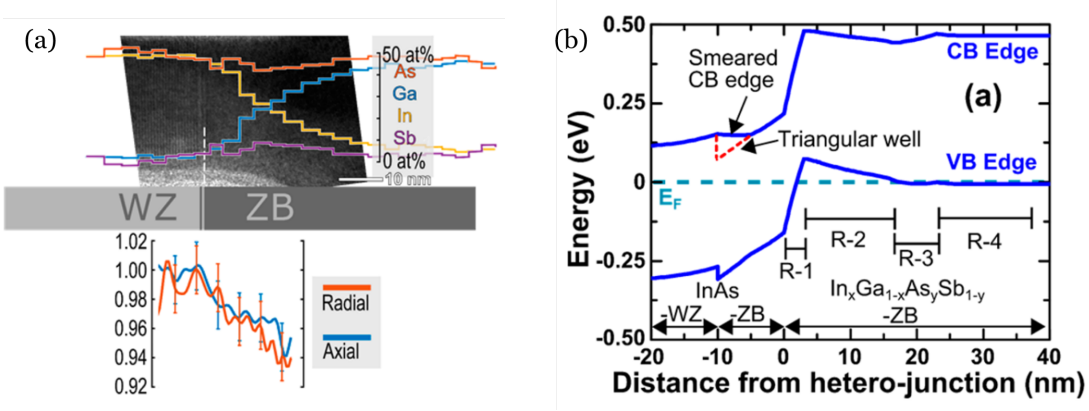


Figure 2.6: (a) Illustration of the composition and strain profile changes across the graded tunneling junction; (b) - Simulation of the band edge diagram along the axis of the nanowire - From [68]

tunneling junction is graded over a distance of 25nm in order to ensure a defect-free transition from the InAs (channel) segment to the InGaAsSb portion of the source region, obtaining a near-broken band alignment, shown in figure 2.6(b). The composition of the $In_xGa_{1-x}As_ySb_{1-y}$ segment changes, starting with values of x=0.7 and y=0.84 in the vicinity of the InAs/InGaAsSb junction, and ending with values of x=0.32 and y=0.72 at the InGaAsSb/GaSb interface. The composition change is shown in figure 2.6(a), along with the strain profile indicating the compression effect as a consequence of the structural transition. The bottom half of the InAs segment is doped N-type using Sn and the InGaAsSb portion is doped P-type using Zn, along with the GaSb segment. The undoped region of the PIN junction is the top half of the InAs segment (light blue segment in figure 2.5(a)). In case of the Large array, the nanowires are laid out in a zig-zag pattern at a pitch of 300nm as shown in figure 2.5(c), while the Small array consists of Nanowires laid out at a pitch of 1.5um.

Room temperature measurements performed on multiple distinct small arrays indicate a substantial amount of variability from device to device, mainly in terms of On-current, Off-current and threshold voltage, as shown in figure 2.7. This is due to multiple factors such as dimensional differences, trap densities and defect variability. Arraying a larger number of individual nanowires in a single device helps average out and eliminate the so-called *golden device* effect, such as a particular nanowire exhibiting deep subthermionic swing, enabling the real evaluation of this technology's potential. Although achieving control over dimensional stability can only be done at the fabrication level, device variability due to trap densities can be minimized by lim-

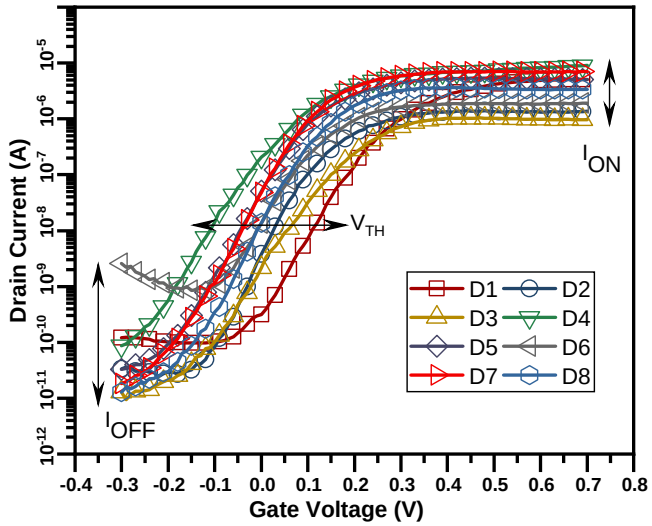


Figure 2.7: Room temperature transfer characteristic of multiple distinct devices, showing considerable variability in on-current I_{On}, off-current I_{Off} and threshold voltage V_T. Measurements were taken at $V_D = 0.4V$

iting the detrimental influence of the Trap-assisted-Tunneling transport mechanism [67] by operating the devices at lower temperature.

2.2.3 Transfer Characteristic and Subthreshold Slope

Indeed, the transfer characteristic measurements shown in figure 2.8 (a) and (b) indicate that as a consequence of lowering temperature, the transfer characteristics become steeper, suggesting an elimination of Trap-Assisted Tunneling, accompanied by a reduction in Subthreshold Slope (SS), and an increase in Threshold Voltage (V_T). The threshold voltage was measured at a constant current $I_T = 10^{-6}A$ in the case of the large array, and $I_T = 10^{-8}A$ for the small array. It is also observable that the temperature dependence of both SS and V_T reduces drastically, such that the curves almost completely overlap in the 150K-10K range.

The apparent mismatch between measured and expected values of on-current for the two devices is firstly a consequence of geometrical differences. As the two devices comprise of nanowires with slightly different dimensions, this will impact overall performance (SS, transconductance $g_m = \partial I_D / \partial V_{GS}$, and on-current I_{ON}). The small array is comprised of relatively thicker nanowires - 25nm - while the large array consists of thinner nanowires measuring only 20nm. The reduction of diameter has

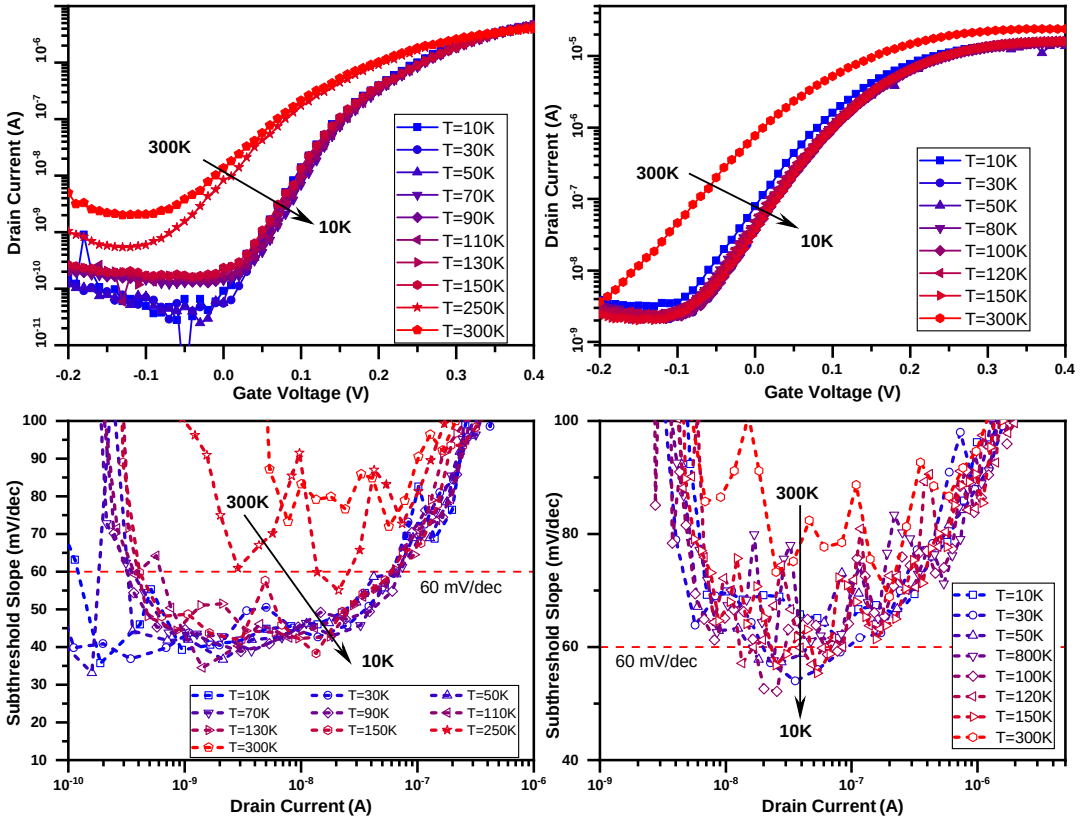
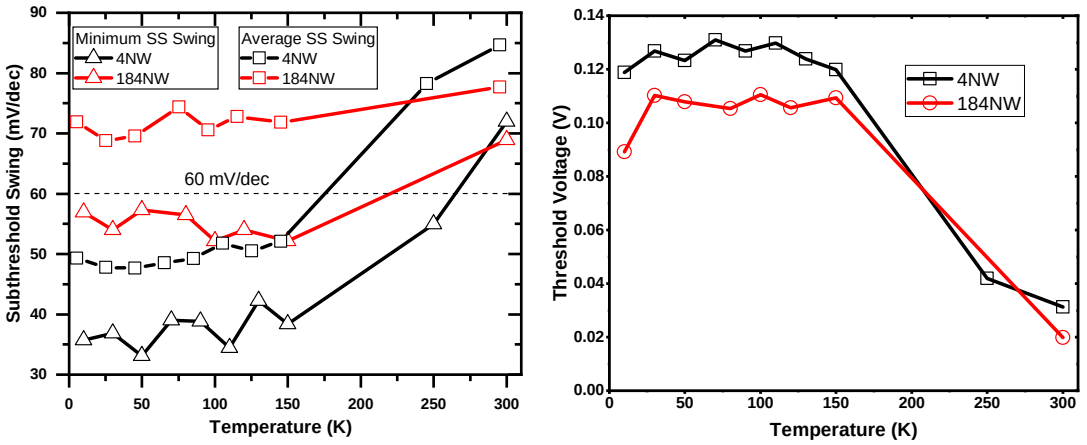


Figure 2.8: Top - Transfer characteristic of the 4NW (left) and 184NW (right) devices at multiple temperatures from 300K down to 10K at drain voltage $V_D = 0.4V$; Bottom - Subthreshold slope of the 4NW (left) and 184NW (right) devices

noticeable impact on on-current, such that thicker nanowires typically show higher current values, therefore the current per nanowire will be greater for the small array. Subthreshold slope is also affected by diameter changes but is also impacted by multiplicity. In this case, higher multiplicity determines a degradation of SS, which can be confirmed by the measured values of minimum and average subthreshold slope reported in table 2.1, and supported by figure 2.8 (c) and (d).

Technological variability also plays a role here - according to the authors of [52] who fabricated the devices, the GaSb segment on some nanowires can get damaged during manufacturing of the top contacts. This is a random, uncontrollable process that renders a number of nanowires poorly connected. Especially in large arrays, as is the case with our nominally-184-nanowire device, a nanowire loss of approximately 10% can be expected.

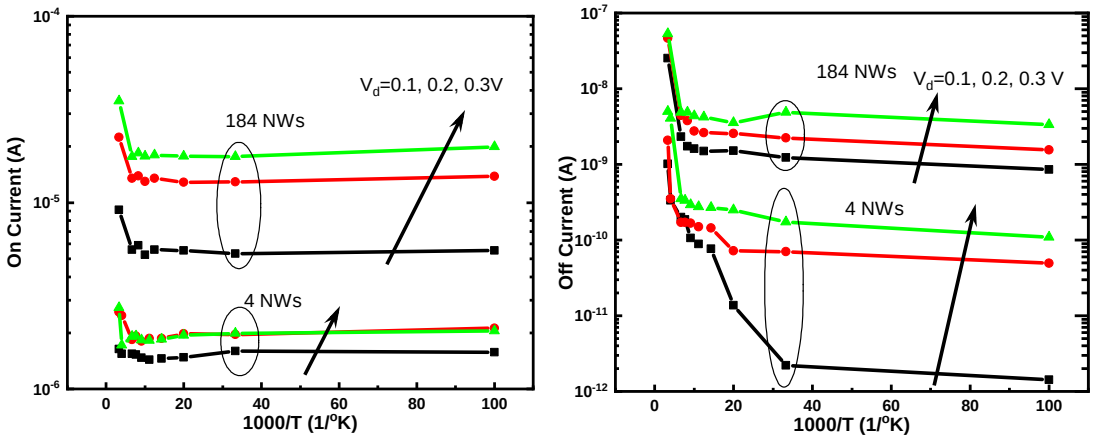


(a) (b)

Figure 2.9: (a) - Minimum and average subthreshold slope values for both devices at $V_D = 0.4V$; (b) - Effect of operating temperature on threshold voltage

2.2.4 Influence of temperature on device performance

Our experiments confirm that lowering the operation temperature of TFETs leads to increased abruptness of the subthreshold slope, and a substantial reduction in its temperature coefficient. In the deep- to mid-cryogenic range, this effect of insensitivity can be attributed to the fact that the only temperature-dependent parameter affecting BTBT current is the semiconductor bandgap, which in itself has a limited, quasi-linear temperature coefficient: $E_g(T) = E_0 - \alpha T^2/(T+\beta)$ [70]. We have investigated mini-



(a) (b)

Figure 2.10: Arrhenius plots of the On- and Off- current in both arrays

mum and average SS values (Figure 2.9a) and found that their values decrease down to $\approx 50mV/dec$ and $\approx 35mV/dec$ at sub-100K temperatures for large and small arrays, respectively. In large arrays, an averaging effect of SS could explain the larger value. By applying linear regression over SS values under 150K for the 4-Nanowire device, we can approximate that the first order temperature coefficient of the minimum and average SS lies in the vicinity of $+28\mu V/dec/K$. In the sub-ambient temperature range (150K-300K), the SS is higher, most probably due to the trap assisted tunneling, and reduces considerably upon cancellation of this effect at low temperatures. Moreover, a strong decreasing trend in the off-current I_{OFF} values can be noticed in figure 2.8a and b, in contrast with a limited variation of On-current. This is due to the Off-current being dominated by Shockley-Read-Hall (SRH) generation-recombination currents in the reverse biased junction, a phenomenon that is temperature dependent. Conversely, the On-current is dominated by Band-to-Band Tunneling which is temperature independent, and the slight current drop can be attributed to the elimination of Trap-Assisted Tunneling. The Arrhenius plots shown in figure 2.10 confirm the considerably larger temperature dependence of the Off- current with respect to the On-current. In addition, it is indicating TAT activation energies of 0.26 eV and 0.21eV for the small and large arrays, respectively.

2.2.5 Analog Figures of Merit

The potential applicability of Tunnel FETs in readout circuitry for quantum computing brings forth a need for high and stable performance in the analog domain. The transconductance curves for both arrays are depicted in figure 2.11(left), indicating that maximum values of g_m are reached below 150K, and tend to saturate at maximum values as temperature drops towards 10K. Another key analog figure of merit - the transconductance efficiency g_m/I_D is reported and shown in figure 2.11(right), demonstrating the capability of Tunnel FETs to reach values near $60V^{-1}$, which is breaking the CMOS limit of $40V^{-1}$ for g_m/I_D at 300K.

Measurements conducted on the output characteristic of the large array are shown in figure 2.12(top) and indicate that the devices can reach good saturation at cryogenic temperatures as low as 10K and supply voltages below 0.5V. In addition, the output characteristics show no noticeable kink effect or hysteresis at drain voltages lower than 0.5V, both effects that can appear at very low temperatures in older CMOS

process nodes[71]. Furthermore, we have evaluated the intrinsic gain of the large array across multiple bias conditions and operating temperature. Intrinsic gain (A_V) is an important metric for evaluating analog device performance. Defined as the

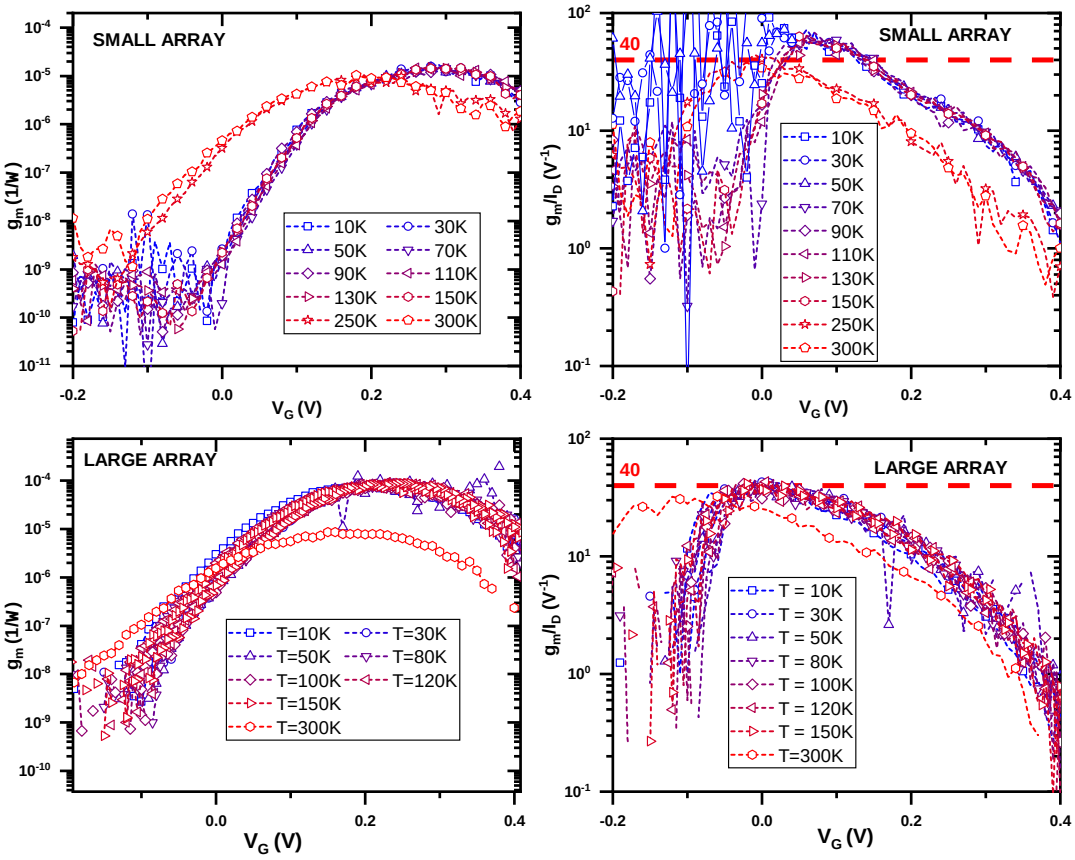


Figure 2.11: Transconductance g_m (left) and Transconductance efficiency g_m/I_D (right) for both arrays between 300K and 10K, and $V_D = 0.4V$

Table 2.1: TFET figures of merit at key temperatures: 300K, 150K and 10K

Temperature	300K		150K		10K	
	Small	Large	Small	Large	Small	Large
I_{Off} [nA], V_D=200mV	2.07	3.68	0.23	2.43	0.09	3.55
I_{On} [μA], V_D=200mV	3.98	23.89	4.51	15.93	4.68	15.79
I_{On}/I_{Off}	$1.92 \cdot 10^3$	$6.49 \cdot 10^3$	$1.96 \cdot 10^4$	$6.56 \cdot 10^3$	$5.2 \cdot 10^4$	$4.45 \cdot 10^3$
Threshold Voltage [V]	0.031	0.020	0.120	0.109	0.119	0.089
Minimum SS [mV/dec]	71.94	68.92	38.38	52.14	35.69	56.92
Average SS [mV/dec]	80.73	73.76	48.16	67.90	45.36	67.94
Maximum g_m [μS]	10.28	8.63	14.70	88.63	14.76	81.15
Maximum g_m/I_D [V^{-1}]	38.22	33.43	63.23	44.71	68.01	41.46

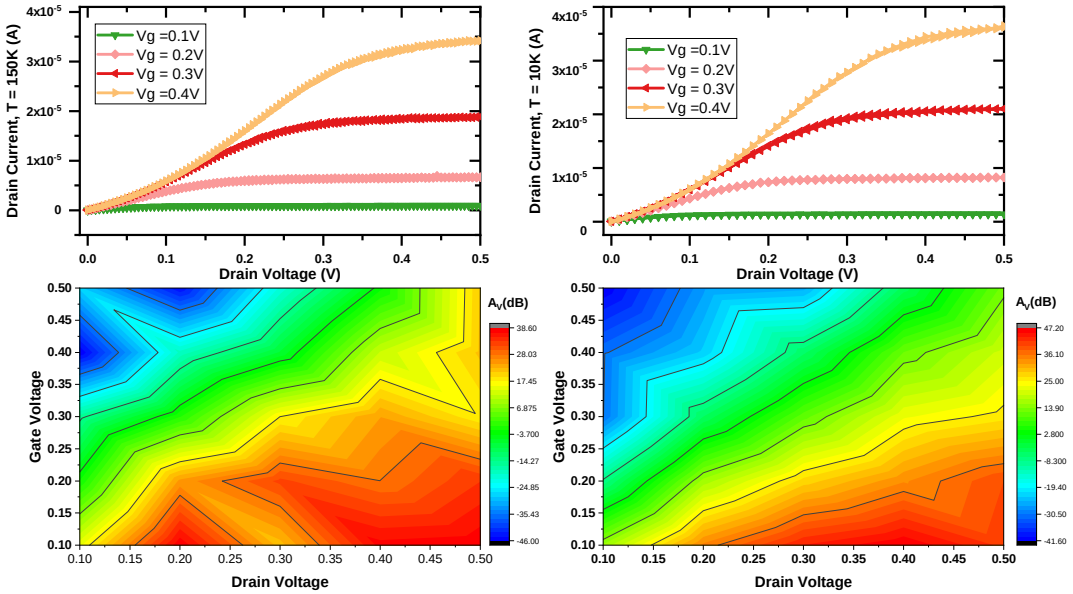


Figure 2.12: Top: Output characteristics of the large array at gate voltages between 0.1 and 0.4 V at 150K and 10K, Bottom - Color map distribution of intrinsic gain across the operating point space (V_G and V_D between 0.1V and 0.5V)

ratio between transconductance and output conductance ($A_V = g_m / g_{ds}$), the intrinsic device gain indicates the maximum possible gain the device can attain while working as a common-source amplifier, regardless of load. In figure 2.12(bottom) we represent the extracted intrinsic gain in the V_G-V_D space between 0.1V and 0.5V which corresponds to 25 distinct operating points both at 150K and 10K. Our results indicate that maximum values higher than 45dB are attained by the large array at 10K, while at higher temperatures (150K) the maximum achievable gain falls short of 40dB. In both cases, intrinsic gain maxima are reached in the low-V_G & high-V_D range of operating points.

Finally, all key analog figures of merit are condensed in Table 2.1, for both extremes and middle of the temperature range (300K, 150K, and 10K), including On- and Off-current values, I_{ON}/I_{OFF} values, threshold voltages, V_T, subthreshold slope, SS, and transconductance g_m.

Based on these results, a direct comparison with several commercial CMOS platforms reveals distinct differences in how operating temperature influences the device parameters, with respect to the TFET platform investigated in this work. Cryogenic characterization studies performed by other research groups on 160nm and 40nm bulk

Table 2.2: Temperature variation of device parameters in Bulk CMOS processes

Technology	Bulk CMOS [72]			
Node	160nm		40nm	
W/L	2.32um/0.16um		1.2um/0.04um	
Temperature	300K	4K	300K	4K
SS (mV/dec)	87	22.8	88.2	27.7
V_T (V)	0.4	0.55	0.38	0.5
I_{On} (A)	$1.5 \cdot 10^{-03}$	$2 \cdot 10^{-03}$	$5.3 \cdot 10^{-04}$	$6 \cdot 10^{-04}$
g_m/I_D (V^{-1})	27	70	27	92
Av_i (dB)	33.06	26.52	26.36	27.23

Table 2.3: Temperature variation of device parameters in an FD-SOI CMOS process

Technology	FD-SOI CMOS [73]		
Node	28nm		
W/L	1μm/28nm		
Temperature	300K	77K	4.2K
SS (mV/dec)	77	24	12
$V_T - V_{T@300K}$ (V)	0	0.11	0.13
$I_{On}/I_{On@300K}$ (A/A)	1	1.13	1.14
$g_m/g_{m@300K}$ (S/S)	1	1.67	2

CMOS technologies [72] (summarized in table 2.2), as well as 28nm Fully-Depleted Silicon-on-Insulator (FDSOI) [73] (summarized in table 2.3) showed that both subthreshold slope SS and threshold voltage V_T exhibit considerable dependence on operating temperature from room temperature ($\approx 300K$) all the way down to liquid Helium temperatures ($\approx 4.2K$). Subthreshold slope, in particular, show a steady decrease when reducing temperature, reaching values close to 12mV/dec at 4.2K in advanced nodes such as the 28nm FD-SOI platform. In addition, MOSFET On-current increases upon lowering temperature, in contrast to Tunnel FETs, where we observed the opposite effect - a decrease in I_{ON}. However, similarly to what we have observed in TFETs, MOSFETs also exhibit an increase in threshold voltage upon lowering the operation temperature, as well as improved analog performance metrics, particularly higher transconductance g_m and transconductance efficiency g_m/I_D, along with a slight improvement of the intrinsic voltage gain $A_{Vi} = g_m/g_{ds}$ upon lowering the temperature in devices with shorter gate length (in the Bulk 40 nm node), although not reaching values as high as those observed in the large TFET nanowire array (more than 45 dB).

In contrast with CMOS, where device characteristics scale continuously when decreasing temperature down to the sub-10K regime, the performance of TFETs does not exhibit the same drastic improvements upon lowering temperature, but instead reveals a different advantage: The temperature dependence characteristic of almost all TFET figures of merit saturates upon elimination of trap assisted tunneling revealing temperature-insensitive behavior below 150K. The reduced temperature dependence of TFET Figures of merit enabled by band-to-band tunneling would therefore enable room-temperature operation at the same level of performance as in cryogenic operation, provided that the detrimental influence of TAT is reduced or eliminated through smart material choices and careful engineering of Tunnel FET platforms in order to reduce defect density.

2.3 Elementary Charge sensing with Tunnel FETs

The discussion presented in this section forms the subject of US Patent 10,818,785, referenced in [74]. In addition, the TCAD simulations presented later in section 2.3.2 have been performed together with Dr. Cem Alper.

In addition to being a worthy alternative for logic devices, the unique subthreshold slope of Tunnel FETs can be exploited by other applications. As we have shown in the previous section, the superior subthreshold slope enables TFETs to achieve very high transconductance values at low voltages and low currents, which is a beneficial metric for analog applications, but most importantly, sensing, as proven in [75, 76]. We have also shown that band-to-band tunneling is a process with very limited temperature dependence, which predicts that such a device can be successfully relied upon across a vast range of operating temperatures. An already established method for the readout of spin or charge qubits confined in quantum dots (QDs) is represented by the Single-Electron Transistor (SET). Although exhibiting considerable charge sensitivity with the ability to detect sub-single-electron variations of its gate charge [77], SETs exhibit limitations in implementation such as the need for very carefully controlled nanoscale island shapes, which requires precise fabrication control of the nanometer-sized SET islands[78]. In addition, when operating in the region of Coulomb blockade, SETs operate at low voltages (10s of mV) and currents (nA range and lower) [79], which poses additional challenges for the integration with processing electronics.

2.3.1 Principle of DG-TFET as elementary charge sensor

A double-gate TFET where one of the control gates is floating can be used as a highly accurate charge detector, sensitive enough to detect elementary charges. The principle being exploited is that any free charge capacitively coupled to the tunneling junction will have an influence on the transistor's drain current. In such a configuration, as depicted in figure 2.13, we can express the sensitivity of drain current with respect to charge variation as:

$$S \stackrel{def}{=} \frac{dI_D}{dQ} = \frac{dI_D}{dV}\frac{dV}{dQ} \tag{2.2}$$

The sensitivity S depends on two factors. The first term depicts the coupling strength between detectable charges and the induced control voltage, a term that is inversely proportional to the coupling capacitance $dV/dQ \sim C^{-1}$ and is device independent. The second term, however, represents the change in drain current as a function of infinitesimal voltage changes caused by the detected charges. This term is highly dependent on device parameters such as gate oxide thickness and dielectric constant, channel material and overall device geometry. As Band-To-Band Tunneling current (drain current) is very strongly correlated to the voltage drop across the control gates in the tunneling junction region, this makes the architecture particularly suitable for the task of elementary charge detection. In order to better characterize the performance of such a sensor, we can refine the definition of sensitivity, in order to reveal its key dependence on one of TFET's most attractive characteristics: the steep subthreshold slope. Thus we introduce a new measure of sensitivity that we will subsequently elaborate upon: S_V. As the sensed charge accumulates on the sensing gate, this triggers a shift in the TFET's threshold voltage. Therefore, we can define S_V as the sensitivity of threshold voltage shift versus sensed charge, as follows:

$$S_V \stackrel{def}{=} \frac{dV_{th}}{dQ} \tag{2.3}$$

In order to evaluate the overall sensitivity, linking detected charges to effective drain current variation, we need a link between threshold voltage shift and output current variation. It becomes easily apparent, at this point, that if we operate the TFET in subthreshold regime, this link between S and S_V is nothing more than its subthreshold

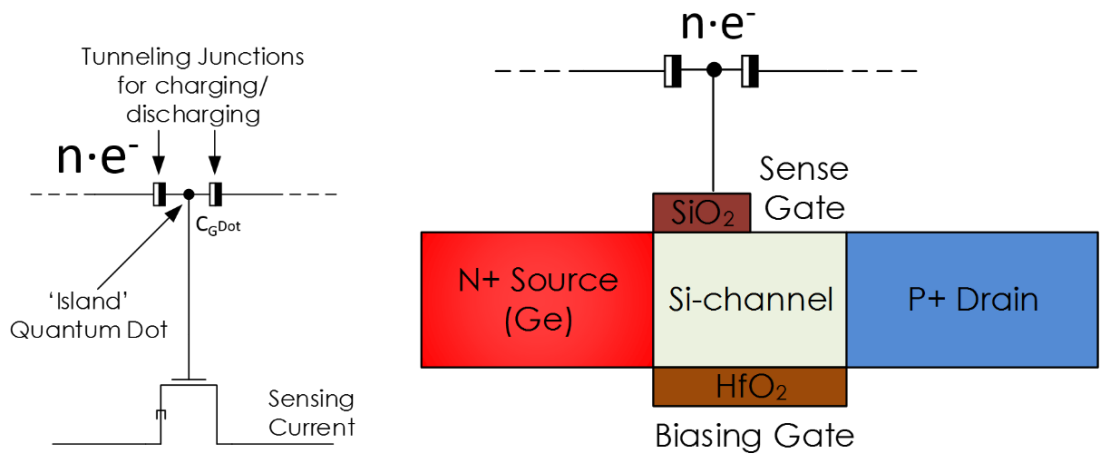


Figure 2.13: Left: Charge sensor schematic; Right - DG-TFET coupled with island (Quantum Dot)

slope (further represented by SS).

$$S = S_V \cdot \frac{1}{SS} \tag{2.4}$$

For a constant S_V, a steeper subthreshold slope will determine greater overall sensitivity of the charge sensor.

As detailed previously, the implementation of such a charge sensor would harness the steep-slope property of TFETs to sense changes in electrical charge. This can be achieved by capacitively coupling a quantum dot to the sensing gate of a DG-TFET. The sensor is essentially a hybrid device, where the writing (charging and discharging) of the quantum dot is done through a "Single Electron Transistor"-like structure. Similar to SETs, the conductive island is weakly coupled to two electrodes which source and sink the charge to be detected. Capacitive coupling between the island and the sensing gate alters the effective gate potential of the TFET, which can be sensed in high resolution as a consequence of the TFET's steep subthreshold slope. Compared to a similar implementation using MOSFETs, the TFET version is at a clear advantage. Firstly, because its switching slope does not obey the thermionic limit of 60 mV/dec, the TFET implementation allows for higher resolution at room temperature. Secondly, the switching slope of TFETs is much less dependent on temperature, as shown in the previous section, making it a robust charge detector across a wide range of temperature.

2.3.2 Validation by simulation

We demonstrate the sensing scheme through Technology Computer-Aided-Design (TCAD) simulations of a double gate Si TFET with a Ge source where the bottom gate is used as "biasing gate", which is meant to bias the device in a regime of maximum sensitivity. The top gate is being used as "sensing gate" which is capacitively coupled to the tunneling junction. In figure 2.14 and table 2.4 we show and summarize the

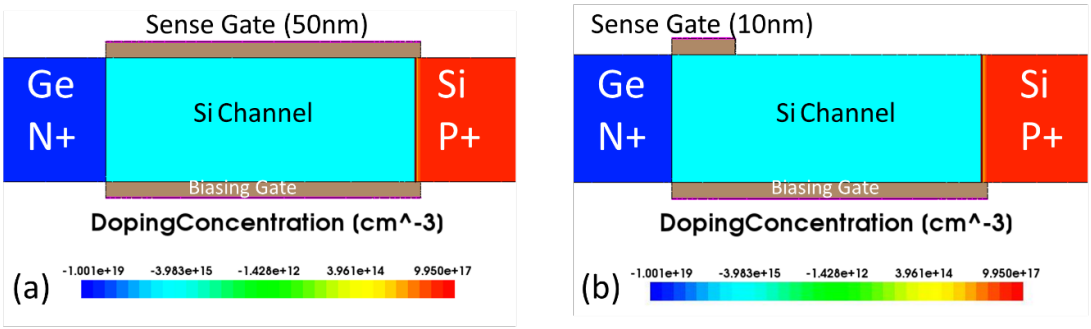


Figure 2.14: (a) - DG-TFET structure used in simulation; (b) - Optimized version for high sensitivity

simulated device structure and parameters for the standard device and a more optimized structure(figure 2.14b), for which the sensing gate insulator is present only around the tunneling junction (effectively making the gate length $L_{sense} = 10nm$) to further focus the electric field lines toward the tunneling junction.

Table 2.4: TCAD Simulation parameters

Parameter	Standard structure	Optimized structure
Channel Thickness	10 nm	10 nm
Bias gate insulator thickness	2.5 nm	2.5 nm
Sense gate insulator thickness	2.5 nm	2.5 nm
Device width	10 nm	10 nm
Source/Drain doping	10^{20} cm^{-3}	10^{20} cm^{-3}
Channel length	50nm	50 nm
Sense gate length	50nm	10nm

In figure 2.15(a) we present the transfer characteristic for different numbers of injected charges at the sensing gate. It is notable how the shift in threshold voltage is almost linearly dependent on the number of injected charges, and this effect is also visible

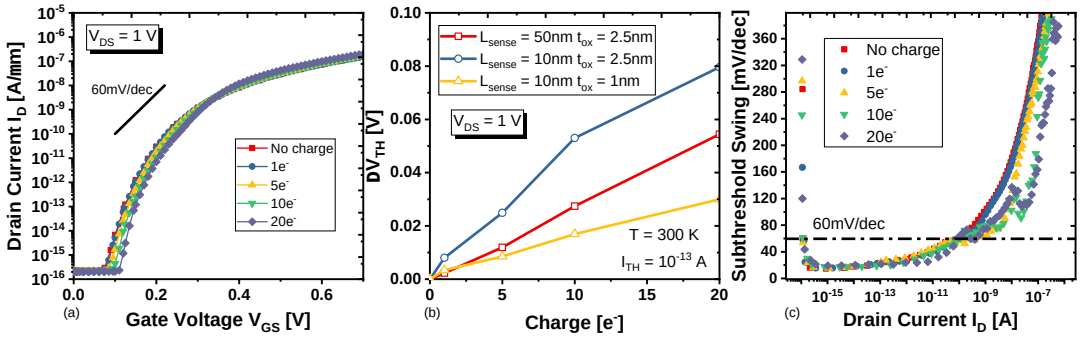


Figure 2.15: (a) - Transfer characteristic with respect to sensed charge; (b) - Threshold voltage shift for standard and optimized structures; (c) - Subthermal subthreshold slope values at room temperature, measured at 100fA

in figure 2.15(b), where we also show the beneficial effect of the smaller gate length that concentrates the electric field around the tunneling junction. In figure 2.15(c) we represent the point SS values as a function of drain current, and we can infer that the TFET under consideration can offer subthermal SS values at room temperature up to about $I_D = 10^{-11}\,A$ for up to 20 injected electrons.

In figure 2.16(b) we are presenting the induced voltage shift at temperatures between 300K and 200K, outlining that in this range, temperature shows no influence upon sensitivity. It can be noted, however, that for large values of injected charges, the induced gate voltage becomes large enough that the voltage drop across the tunneling junction becomes pinned as a consequence of inversion layer formation beneath the sensing gate, effectively screening the field effect on the tunneling junction. This translates into a dramatic reduction of sensitivity, through the term dI_D/dV. Decreased temperature, however, shows a beneficial influence on the overall transfer characteristic of the device, as lowering the temperature results in a decrease of the SRH recombination current, indicated in figure 2.16(a) as a decrease in Off-current (leakage). From the data shown in figure 2.15(b) we can extract a maximum value of 4 mV/e^- for threshold voltage sensitivity to sensed charge. This value was extracted after evaluating the slope of ΔV_{th} vs charge curve, and choosing the maximum value corresponding to the most optimal parameter set, a sense gate length of 10nm and 2.5 nm oxide thickness. The minimum subthreshold slope value obtained from simulation is approximately 10 mV/dec. Combining these results together, we conclude that a sensed charge of 5 electrons would trigger a drain current shift of two decades, i.e. a 100-fold increase in output current.

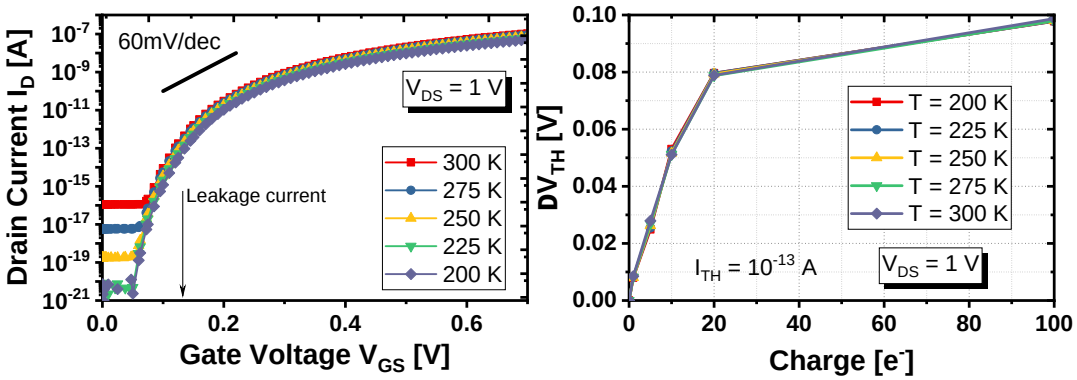


Figure 2.16: (a) - Transfer characteristic between 200K and 300K showing decrease of leakage at lower temperature; (b) - Threshold voltage shift independent on temperature between 200K and 300K

2.3.3 Experimental validation on a SiGe/Si Line Tunneling TFET

In order to perform proof of concept, we have carried out measurements using p-type TFETs as reported in [50], generously provided to us by the authors. As explained by the developers, the benefit of line tunneling (tunneling direction parallel to gate electric field) as opposed to point tunneling is that it allows for constant subthreshold slope values with respect to gate voltage, in a certain range of drain current.

Although this is not a truly double-gate device, the fact that it was built on an SOI platform enabled us to use the substrate as a back gate, albeit with a lower influence over the electrostatics of the tunneling junction, due to increased oxide thickness (buried oxide is acting as the back gate insulator, in this case). Transfer characteristics measurements at 80K, 180K and 300K, shown in figure 2.18a, confirm again that low

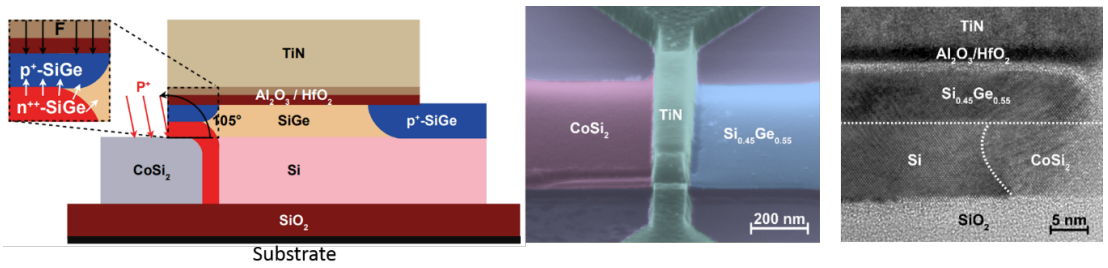


Figure 2.17: Left - TFET cross section outlining increased area for line tunneling; Center - SEM micrograph of the device; Right - TEM micrograph of the tunneling junction area. Adapted from [50]

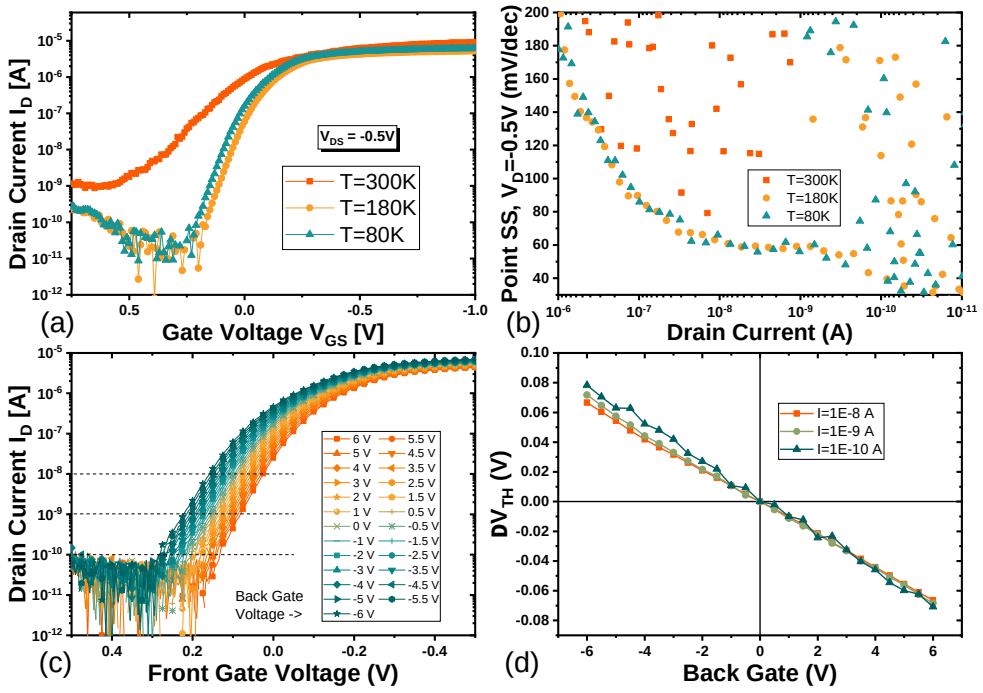


Figure 2.18: (a) - Transfer characteristics of line TFET measured at 300K, 180K and 80K; (b) - Subthreshold slope values associated to transfer characteristics in (a); (c) - Forward transfer characteristics measured at 180K with back gate bias ranging from -6 to 6V; (d) - Measured shift in threshold voltage as a consequence of back gate bias

temperature operation removes Trap Assisted Tunneling (which impacts subthreshold slope negatively, as explained earlier in section 2.2) and lowers the SRH recombination current, revealing a clean, steep subthreshold slope attributed to Band-To-Band Tunneling mechanism. Figure 2.18b shows the associated point subthreshold slope values for the curves in 2.18a. It can be noted how at low temperatures the subthreshold slopes are similar and show almost constant values across at least one decade of drain current. We will use the extracted value of 60 mV/dec in order to compute the sensitivity S, as described earlier in section 2.3.1. As opposed to the simulated devices, where TCAD software enabled us to simulate individual charges injected into the sensing gate, an experimental validation of such a mechanism was impossible due to technological limitations. We are not able to **directly** evaluate the sensitivity in terms of drain current variation as a function of charge, but rather as a function of applied voltage on the sensing gate. Therefore, we have performed a dense voltage sweep of the back gate (substrate) and evaluated the resulting threshold voltage shift of the TFET. Figures 2.18c and 2.18d summarize the result of this experiment, showing an

ample shift in threshold voltage maintaining integrity of the transfer characteristics, and not affecting subthreshold slope between individual bias points. In figure 2.18d we plotted threshold voltage as a function of back gate bias measured at three different current levels. The results show a consistent and linear shift of the threshold voltage at current levels varying between 10^{-10} and 10^{-8} A. Moreover, the dataset shown in figure 2.18d enables us to extract a sensitivity of 11.6 mV/V of threshold voltage shift with respect to back gate bias. In order to compute the sensitivity to accumulated charge in this case, we must estimate the capacitance of the back gate, and for that it is necessary to estimate the thickness of the buried oxide (BOX) of the SOI wafer that the TFETs were fabricated on. In [80] the authors indicate that the effective oxide thickness (EOT) of the high-κ gate dielectric is 1.2nm. Under a crude approximation, starting from the measured $\Delta V_{TH}/\Delta V_{BG}$, we can estimate that the BOX thickness is approximately 100nm. This results in an equivalent back gate capacitance per unit area $C_{BG} = 34.5 \cdot 10^{-9} F/cm^2$. Using the value of capacitance per unit area for the back gate (sense gate, in this case) and assuming that the sense gate voltage is modulated by an accumulated charge Q coupled to the tunneling junction through C_{BG}, we can then compute the charge sensitivity according to equation 2.4 as

$$S = \frac{\Delta V_{TH}}{\Delta V_{BG}} \cdot \frac{1}{C_{BG}} \cdot \frac{1}{SS} = \frac{1}{0.36} \frac{dec}{e^-/nm^2} \tag{2.5}$$

In other words, an accumulated charge of 0.36 e^- per unit area of 1 nm^2 would trigger a variation of 1 decade in the drain current of the TFET, in the nanoampere drain current range ($10^{-10} A \rightarrow 10^{-8} A$). Clearly, the sensitivity estimated from measurement is many times lower than that obtained from simulation. This is of course due to the weak coupling of the back gate (used as sense gate, in our experiment) and the considerable difference in simulated versus measured subthreshold slope of the TFET. It is difficult, though, to compare the simulated results with measurements, in terms of sensitivity, for multiple reasons. Firstly, it is difficult to physically recreate the effect of single charges injected in the sensing gate. Secondly, it is difficult to estimate the total capacitance of the back gate insulator due to unpredictable variations in substrate and buried oxide thickness. Thirdly, there is the possibility that with higher back gate capacitance (as would be the case with a true double-gate device) the effect of the back gate would not be limited to a threshold voltage shift only, but would also start to affect the tunneling mechanism in a way similar with what was shown in simulation, leading to non linearity in the $\Delta V_{TH}/\Delta Q$ characteristic.

Finally, it is worth to provide a brief comparison with respect to the charge sensing capabilities of the Single Electron Transistor (SET). To this end, we have performed a simulation of an SET using the MIB model [79, 81] with the aim of evaluating the threshold voltage shift in the presence of a background charge. In figure 2.19a, we show that the simulated SET exhibits a considerable threshold voltage shift with respect to background charge $\Delta V_{TH}/\Delta Q \approx 80mV/e^{-}$. In addition, at the lowest simulated temperature T=5K, the subthreshold slope of the SET is approximately $3mV/dec$, as indicated by the simulation results shown in figure 2.19b. Consequently, we can estimate the charge sensitivity following the approach presented earlier in equation 2.4 as $S = 26.6dec/e^{-}$. Clearly, this result is orders of magnitude higher than what was measured and simulated using TFETs, and is due to the very high sensitivity of the SET to background charge and its very steep subthreshold slope. However, in an SET, such sensitivity is only achievable at very low temperatures, as indicated in figure 2.19b - where we show that upon increasing operation temperature, the SET transfer characteristic quickly degrades, reaching subthreshold slope values close to 80mV/dec already at 50K, accompanied by a drastic reduction in on-off current ratio I_{ON}/I_{OFF}, limiting the device functionality. Moreover, the gate and drain voltages fall within the 10s of mV regime, and the achievable drain currents lie in the picoAmpere range, which increases the difficulty of interfacing with more traditional CMOS computation platforms.

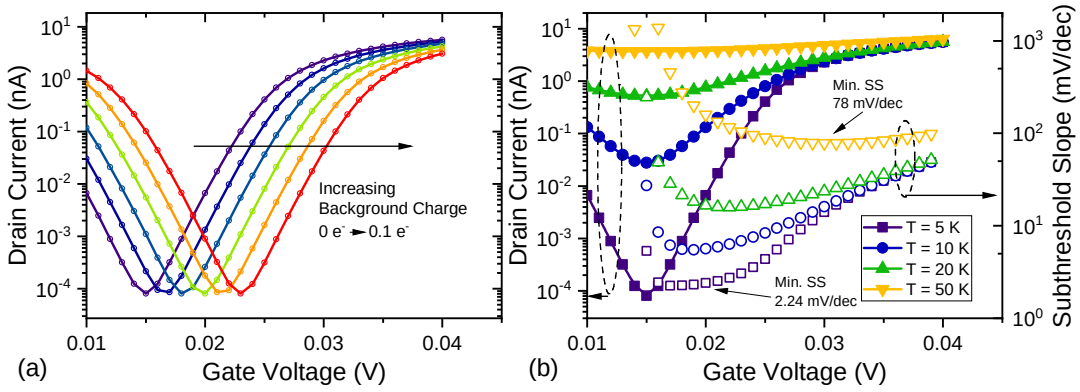


Figure 2.19: (a) - Simulated transfer characteristics of the SET at temperature T=5K and supply voltage $V_{DS} = 30mV$ indicating considerable shift of the threshold voltage with respect to background charge (model parameter ξ [81]); (b) - Simulated transfer characteristics and extracted subthreshold slope of the SET at temperatures between 5K and 50K; MIB model parameters [81] used in simulation: $R_{TD} = R_{TS} = 1M\Omega$, $C_G = 2aF$, $C_{TD} = C_{TS} = 1aF$

2.4 Summary

In this chapter we studied and discussed the potential use of Tunnel FETs as: (i) stable and energy efficient electronic digital and analog devices operating at cryogenic temperature, and (ii) elementary charge sensors, as a possible counter candidate to Single Electron Transistor (SET), with potential applications in the field of quantum computing.

The experimental test vehicles for the cryogenic study in section 2.1 concerning the behaviour, performance, and comparison to state-of-the-art, was represented by heterojunction nanowire TFETs fabricated at Lund University in Sweden. The study was conducted from room temperature down to liquid helium-temperatures in ranges as low as 10K and operation voltages below 500mV. The used test vehicles already showed a good behavior as band-to-band tunneling devices at room temperatures and data is reported in both small (4 nanowires) and large (184 nanowires) arrays of devices. When arraying the TFET devices, an averaging effect is observed on the values of the normalized characteristics indicating a slight reduction of performance in high-multiplicity devices, yet our study showed that the **variability and functional yield of tunnel FETs are sufficiently good to preserve the main device properties even in large arrays of hundreds of nanowires**.

Another main conclusion of our experimental study is that the key digital and analog figures of merit of TFETs such as subthreshold slope, SS, threshold voltage, V_t, on-current, I_{ON}, transconductance, g_m, transconductance efficiency, g_m/I_D and intrinsic analog gain exhibit **considerable stability without substantial variations with respect to temperature below 150K**, once the detrimental effects of Trap Assisted Tunneling (TAT) are removed by means of lowering operating temperature. In contrast, we have shown that state of the art CMOS platforms (both bulk and SOI) exhibit a considerable and continuous temperature dependence of analog and digital figures of merit from room temperature down to liquid helium temperatures, without any apparent saturation, as in the case of TFETs. This suggests that **Tunnel FETs can form an interesting electronic device candidate family for cryogenic electronics operation at voltages below 500mV, with less temperature dependence of digital and analog properties than the state of the art cyrogenic CMOS**.

In section 2.2 we have proposed **a new elementary charge sensor based on the**

concept of a double gate TFET (DG-TFET). We explained the sensing principle where one of the gates - called the biasing gate - is used to ensure an operating point of the device such that the front gate - called the sense gate - works in the steepest region of the subthreshold regime, thus ensuring maximum sensitivity. By means of TCAD simulations we validated the sensing principle and showed a clear dependence between drain current and just a few elementary charges injected into the sense gate. Moreover, simulations enabled us to optimize the geometry of the sense gate in order to better concentrate the electric field and increase its influence on the tunneling barrier, enabling us to **predict sensitivities as high as two decades of current change in the TFET per 5 injected electrons, in the fA range, corresponding to 4 mV/e^- of threshold voltage shift sensitivity**.

Although we indicated that the charge sensitivities achievable using the TFET charge sensor are not comparable with the much better sensitivities achieved by SETs, we believe that the **interest in such a DG-TFET charge detector as compared with Single Electron Transistors** is motivated by: (i) it may be **fabricated by a technology that is fully CMOS compatible**, without any additional requirements on the precise control as for the nanosizes of the central island of the SET to operate under Coulomb blockade at a given temperature, (ii) we expect that the **temperature sensitivity of DG-TFET implemented as silicon or SiGe sensor will be lower than in a MOSFET and SET**, (iii) this device can provide **higher analog gain (amplification) compared to an SET**, so it can operate with higher currents at low voltages, being more versatile to be interfaced with CMOS than SET, which usually is reported to operate in the range of few tens of mV as drain-to-source voltage (region of Coulomb blockade).

The last part of the chapter has been dedicated to an experimental validation of the sensing principle with measurements being performed on a SiGe/Si line tunneling TFET built on an SOI platform and using the substrate as the back gate (acting as the sense gate in this case). Even if not being optimized for our sensor principle, the measurements performed at room and low temperature overall confirmed our concept and simulations, and the front gate transfer characteristic measurement at a dense collection of back bias points suggests sensitivities of 11.6 mV/V of threshold voltage shift with respect to back gate bias. This corresponds to an induced drain current change of one decade when sensing charge per unit area values of 0.36 e^-/nm^2. Overall, this chapter **proposed and confirmed that steep-slope band-to-band tunneling devices such as TFETs can offer interesting solutions for cryogenic electronics**

and for charge sensing at such low temperature operation. Further optimizations and validations would be needed but the work presented here is among the first one advancing such new ideas based on both experimental results and TCAD simulations.

3 Phase transition characteristics of VO_2 thin films

3.1 Introduction

For the last half century, the progress of Silicon-based technologies has led modern society towards the so-called Silicon Age. Silicon (Si) is abundant in nature, can be synthesized and manufactured at reduced cost, is simple and is well understood. However, despite its success, the international technology roadmaps target qualitatively new concepts and functionalities ("Emerging Research Materials") that certainly cannot be supported by the present "simple" physics and chemistry of silicon [82]. Hence, for the past three decades, research on functional oxides has received great attention due to their stunningly rich physics and their potential as next-generation materials for electronics [83–85]. This research field represents one of the most pioneering research topics towards achieving the next generation of electronic materials and devices in conjunction with the *More than Moore* strategy. This class of materials includes many of the strongly correlated transition metal oxides (TMOs) that exhibit unusual but often very useful properties such as high temperature superconductivity, colossal magnetoresistance, high dielectric properties, ferroelectricity, high ionic conductivity and superior memristive effects (of particular interest to oxide Resistive RAM (ReRAM) applications[86]). Mastering the complexity of this material class can therefore offer unlimited degrees of freedom in controlling its states and engineering versatile functional properties for novel device concepts and applications.

Several TMOs have been proposed as promising resistive switching materials for electronic applications, i.e., the materials showing tunable resistance states induced

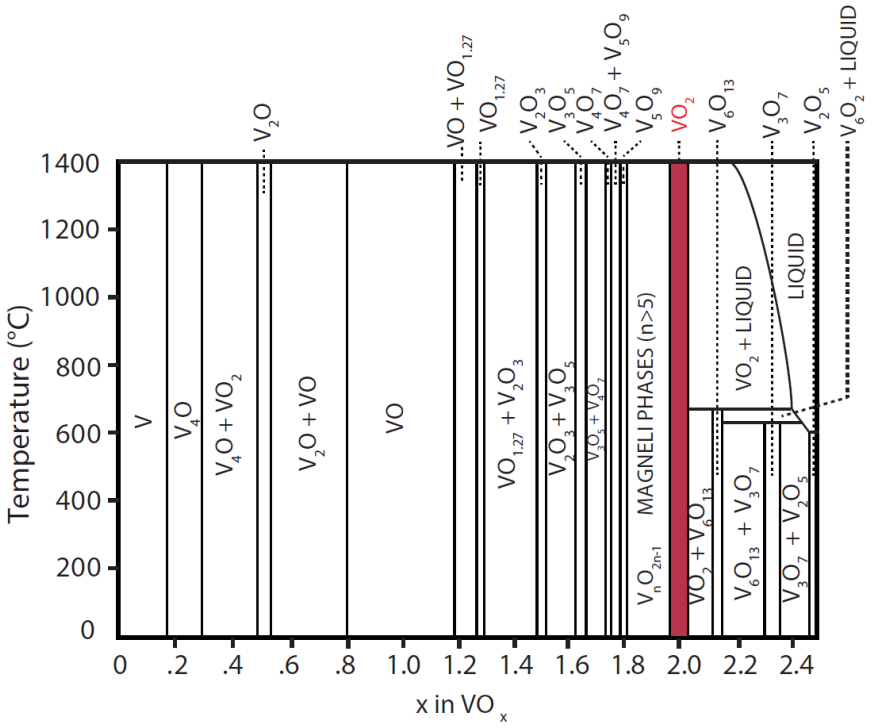


Figure 3.1: Phase diagram of the V-O system. Adapted from [23], originally from [91]

by an external electrical bias. Metal-to-insulator transitions (MIT) belong to the class of the aforementioned emergent phenomena and can be driven as a function of pressure, temperature, defects and doping [87, 88]. A representative group of TMOs are the vanadium oxides, that show intriguing strong correlation effects that are critically dependent on the oxidation state of vanadium (V). In 1959, F.J. Morin [89] reported a sharp thermally triggered increase in electrical resistivity of several orders of magnitude in vanadium and titanium oxides, particularly in vanadium monoxide (VO), vanadium dioxide (VO_2), vanadium sesquioxide (V_2O_3) and titanium sesquioxide (Ti_2O_3) and all the MIT behaviors were observed when temperature was decreased under a certain threshold temperature T_{MIT}. Several other oxides (e.g. Iron(II,III) oxide Fe_3O_4, praseodymium nickel oxide $PrNiO_3$, neodymium nickel oxide $NdNiO_3$, samarium nickel oxide $SmNiO_3$, lanthanum cobalt oxide $LaCoO_3$) exhibiting MIT have been reported showing transition temperatures ranging from liquid nitrogen temperatures (70K for V_8O_{15}) up to more than 1000K (1081K for niobium dioxide NbO_2)[90].

Among all the transition metal oxides, the vanadium oxide (V-O) system has received

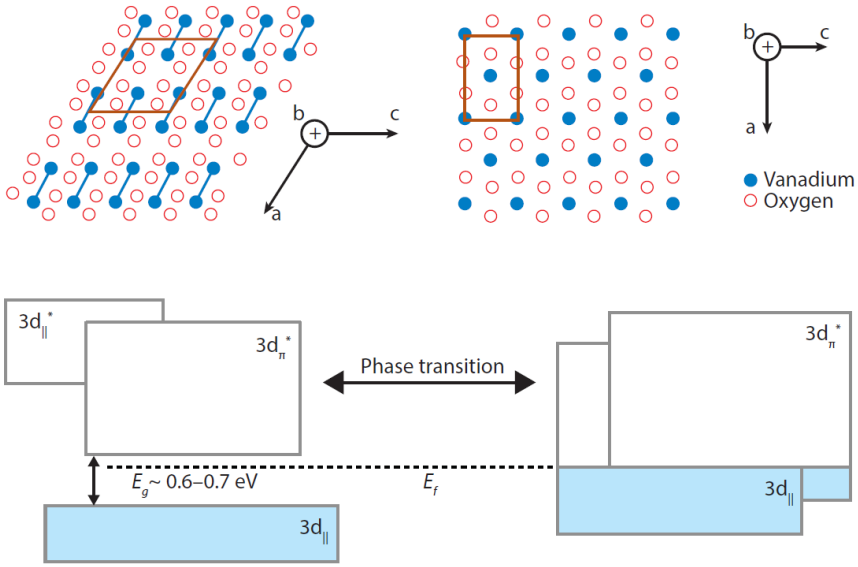


Figure 3.2: Top - the IMT structural change of VO_2 from the insulating phase (monoclinic) to the metallic phase (rutile); Bottom - Bandgap collapse due to the structural change; Adapted from [93], originally from [90]

a lot of attention due to the multivalent nature of vanadium and the stabilization of multiple oxide phases as illustrated by the phase diagram of the V-O system shown in figure 3.1. According to [87], three distinct stable phases such as VO_2, V_2O_3 and V_3O_5 all exhibit MIT behavior at different temperatures: (i) V_2O_3 ($3d^2, V^{+3}$) undergoes a first-order phase transition at $T_{MIT} \approx 150K$, (ii) VO_2 ($3d^1, V^{+4}$) shows an MIT at $T_{MIT} \approx 340K$ and (iii) V_3O_5 ($3d^1/3d^2$, a mixed valency of V^{+3} and V^{+4}) undergoes IMT at $T_{IMT} \approx 423-433K$[92]. Meanwhile, other phases such as VO, V_2O_5, or V_7O_{13} do not exhibit MIT characteristics. In addition, the MIT phases exhibit relative resistive changes from one order up to several orders of magnitude. For example, V_2O_3 can reach resistive reconfigurability of up to 10 orders of magnitude, which is interesting for switching applications. Its MIT transition temperature, however, falls in the 150K range, so its applicability remains fairly limited for developing practical electronic devices.

On the other hand, VO_2 exhibits a reversible MIT at a threshold close to room temperature ($T_{MIT} \approx 68$ °C, 340K). This opens the door towards applications that exploit its valuable properties at ambient conditions. Below the transition temperature, VO_2 is characterized by an insulating monoclinic phase with a bandgap $E_g \approx 0.6-0.7eV$

in the 3d orbital bands. As shown in figure 3.2, the crystal structure changes to a tetragonal rutile upon increasing the temperatures above the insulator-to-metal (IMT) threshold (T_{IMT}).

This phase transition is associated with a collapse of the bandgap which results in increased electron density in the conduction band. The direct result is a steep and large change in the electrical conductivity of VO_2 up to 5 orders of magnitude observed in VO_2 single crystals [94]. The IMT exhibits hysteretic behavior upon reducing temperature below the T_{MIT} threshold, with a hysteresis between 10 and 20K [95, 96], dependent on growth techniques, microstructural properties (e.g. grain size and shape), annealing, strain and doping [88, 97].

The origin of the MIT in VO_2, however, remains under considerable debate [98, 99], with competing theories which attribute the transition to either a Peierls instability due to electron-phonon interactions [100–102] or to a Mott transition due to electron-electron interactions [103, 104]. Regardless of the origin of the transition, the conductivity change exhibited by VO_2 can be achieved by employing different stimuli, e.g. electro-thermal excitation[105–108], optical stimulation[109, 110] and mechanical strain[111, 112], to name a few, enabling VO_2 to be considered as a good candidate towards developing smart and versatile sensors.

As a consequence, several attempts have been made to harness the sensitivity of vanadium dioxide towards external stimuli and the approaches generally rely on the modulation of electrical resistance or optical reflectance of the insulating states and the IMT threshold values by means of external stimuli. For example, Kim et al. [113] proposed the implementation of a programmable critical temperature sensor. The authors have identified that the threshold voltage for the IMT of VO_2 strongly depends on ambient temperature and thus the applied voltage can be used as a means to pre-set the temperature threshold of the IMT. Similarly, Darwish et al. [114] suggested that a pair of identical VO_2 resistors could be used as adjacent legs of a Wheatstone bridge, and they proposed that such a device array would be capable of measuring temperature gradients and rapid heat spikes with durations in the 100s of μs range. Temperature, however, is not the only commonly investigated stimulus.

Another strategy is to induce photoexcitation of the electronic energy band gap (insulating/semiconducting) state of VO_2. Li et al. [115] demonstrated a near-infrared

(NIR) uncooled photoconductive detector with a high responsivity of more than 2800 A/W at ambient conditions using a VO_2/V_2O_5 core/shell nanobeam heterostructure (CSNH). The authors reported highly tunable performance with fast and efficient photogeneration of electron-hole pairs at the staggered interfaces between VO_2 and V_2O_5.

Similarly, Lu et al. [116] demonstrated that single tungsten-doped VO_2 nanowires can be used for high sensitivity phototransistors that exhibit high responsivity upwards of 2×10^4 A/W and ultrafast photoresponse at visible wavelengths (405nm, 532nm, and 660nm). In addition, Wu et al. [117] demonstrated microwire VO_2 photodetectors reaching responsivities higher than 7000 A/W in the ultraviolet spectrum (between 360nm 400nm) at incident light intensities of $1\mu W/cm^2$. The authors attribute the achieved high responsivity to a significant increase in the photocurrent of the VO_2 microwire under UV illumination. This is driven by a hole-trapping effect on the surface of the microwire due to adsorbed atmospheric oxygen species, which significantly prevent the recombination of the photogenerated electron-hole pairs.

Finally, a number of studies have focused on investigating the sensitivity of VO_2 with external strain (mechanical excitation). Cao et al. [118] showed that VO_2 microbeams exhibit IMT at different temperatures as a function of applied strain. By monitoring the light reflectivity of the microbeam, it was confirmed that the IMT temperature of VO_2 becomes lower than a conventional IMT temperature when external tensile strain is applied to the in-plane direction of VO_2[119]. Moreover, Hu et al. [120, 121] were able to lower the IMT temperatures by means of compressive strain applied along the in-plane direction and the results indicated a change in the electrical properties of VO_2, in particular a change of the IMT threshold voltage. Moreover, in [121] the authors claim that compressive strain can trigger the phase transition of VO_2 only at high levels of applied voltage (8V), and that IMT cannot be triggered only by applying strain at lower voltage levels (3V), revealing that the transition trigger mechanism requires a combination of externally applied strain *and* sufficient self-heating.

From the examples above, we can distinguish two approaches towards sensing with VO_2 structures and devices: (i) the first approach is to exploit the MIT characteristics of VO_2 via light induced band excitation (the photogeneration of electron-hole pairs) to produce detectable photocurrents with a high sensitivity (e.g. incident radiation energy dependence demonstrated from NIR to UV), and (ii) the second approach

is to exploit the effects of external stimuli on the IMT of VO_2 to verify whether it is governed by induced thermal energy. If a heating effect occurs from an outside source during electrical operation, then the devices can undergo phase transition at lower temperatures. Moreover, biasing the devices in the "corner" region of the R(T) or I(V) curves close to the IMT threshold (either by controlling ambient temperature or applied voltages or currents) enables triggering the phase transition of VO_2 by external stimuli.

3.2 Experimental Methods

3.2.1 Pulsed Laser Deposition

For the last two decades, the rapid advancement of thin film deposition technologies has allowed to fabricate high-quality film materials and to design and synthesize novel thin films and artificial structures. These have offered not only wide-range tunability of material properties, but it has triggered rich physics phenomena and emerging functionalities for the next generation of electronic applications. Thus, thin film materials have been widely used as key active elements in the fields of electronic, optoelectronic, photonic and magnetic devices to date.

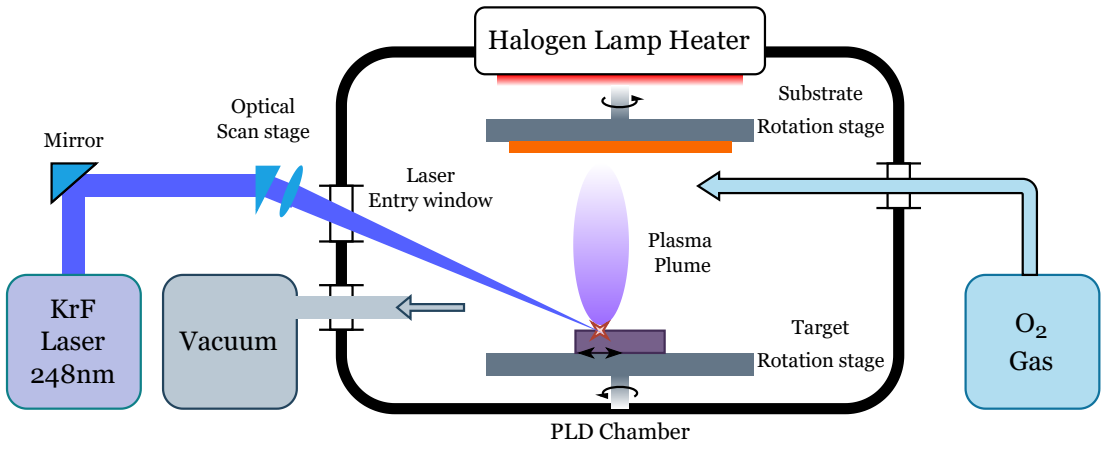


Figure 3.3: Schematics for a pulsed laser deposition system including a vacuum chamber (a base pressure: $\approx 5 \times 10^{-8}$ mbar), KrF excimer laser ($\lambda = 248$ nm), halogen lamp heater, target and substrate stages, optics for the alignment of incident laser to the surface of targets, and gas inlets (O_2, Ar, and N_2).

Thin film deposition techniques from the vapor phase can be classified mainly in two parts; physical vapor deposition (PVD) and chemical vapor deposition (CVD). The former represents the cases of sputtering (e.g. DC, RF, magnetron, and ion beam sputtering), evaporation (e.g. thermal and electron beam evaporation), and pulsed laser deposition (PLD). The latter is thermal, radiative, plasma, and metal-organic CVD (MOCVD). In this thesis, all the films, i.e., VO2-based thin films, were prepared using PLD.

PLD is a well-established PVD technique and has become one of the most popular thin film growth techniques for wide areas of thin film and multi-layer research. In a vacuum chamber an incident high-power pulsed laser beam is focused on and strikes the surface of a target material to be deposited. In PLD systems, the incident laser is usually focused onto the surface of target materials by a set of optics including mirrors, aperture, lenses, and attenuators as schematically illustrated in figure 3.3. The target is typically oriented at an angle of $\approx 45°$ with respect to the incident laser. The incident laser pulse induces extremely rapid heating of target material as the so-called pulsed laser ablation. This leads to the excitation and ionization of material species (e.g. atoms, molecules, electrons, positive and negative ions, clusters, particulates, and molten globules) in the target, resulting in the formation of a plasma plume and subsequent optical emission. Thus, the ejected energetic species transport through the plasma plume and can be deposited on a substrate as a film. This laser ablation process on target materials can be carried out in a background gas such as oxygen, which is commonly used as oxygen partial pressure (P_{O_2}) for PLD oxide film growth. Especially, for oxide film growth, different oxygen-reactive growth environment in the chamber significantly determines the stoichiometry of grown films, thus a careful control of P_{O_2} is always required depending on the purpose of study. In the vacuum chamber, substrate temperatures are controlled by a heater (halogen lamp for the case of Solmates PLD, as seen in figure 3.3). Controlling various deposition parameters such as temperature, pressure and type of background gas, laser fluence, laser repetition rate, and target-to-substrate distance determines microstructural properties, surface/interface morphology, defect density, and chemical composition of the PLD-deposited films:

1. **Temperature:** Crystal structure, orientation, surface morphology, and stoichiometric composition of the as-deposited films are strongly influenced by

substrate temperature [122]. For example, high temperatures can lead to an increase in the mobility of the absorbed atoms that arrive at the surface of substrate during deposition process and promote the development of grain structures. However, if temperature is too high, atomic desorption, interdiffusion at film/substrate interfaces, and substrate reconstruction can occur, significantly causing the deterioration of film crystallinity. In vacuum, the substrate temperature might show no direct influence on how the energetic species arrive at the surface of substrate during the PLD process. However, by employing a certain gas pressure, high substrate temperatures heat the background gas and this can significantly vary the expansion dynamics of laser plumes. This heat-and-gas interaction is more obvious with higher temperatures and can create a gas density gradient from the target to the substrate. The reduced gas density is encountered by a decrease in the background gas resistance to plume propagation [123]. This results in a reduction of the confining effect of the background gas and a consequent rise of the impact velocity of the ablated species. Hence, finding optimal/appropriate substrate temperatures is crucial to achieve high-quality and/or desired films.

2. **Background gas pressure:** In the PLD vacuum chamber, high-energy species are substantially attenuated by collisional events in a given background gas. Introducing a background gas (especially oxygen for oxide film growth) leads to a shift in the entire kinetic energy of the species to a lower one. The background gas pressure classifies different transport modes for the ablated species [124]. In a vacuum-like regime, there are no or negligible interactions with the background gas and thus highly energetic species (> 1000 eV) can transport to the substrate with different arrival times of the species as a ballistic mode. Second, a "transition-like" regime (when the mean free path of the species is smaller than a tenth of the target-to-substrate distance, 5×10^{-3} mbar to 5×10^{-2} mbar) allows chemical reactions between the background gas and the plasma plume. In this regime, relatively high kinetic energies of the arriving species can be still kept at the substrate. Lastly, in a high oxygen background pressure (e.g. P_{O_2} = 0.1 mbar), the plume expansion is very slow and thus the background gas confines all species together as the diffusion-like regime. However, this regime can cause ≈50 % loss for the deposited materials and often causes porous film structure. Therefore, the selection of the background pressure is a very im-

portant growth parameter which significantly determines the stoichiometry of films, especially for the growth of complex oxides and light-element-containing oxide compounds [122, 125].

3. **Laser fluence:** Laser fluence has a strong effect on the ablation rates and film thickness. To obtain sufficient removal of materials for the formation of films, an appropriate laser fluence (above a threshold ablation fluence) needs to be employed, dependent on materials. When laser fluence increases above the threshold value, the ablation rate logarithmically increases and thus deposition rate increases. Moreover, the laser fluence varies the kinetic energy of the ablated species. This directly affects the film crystallinity due to different adatom mobility at the substrate. However, highly energetic ablated species can give a considerable detrimental effect on the quality of the deposited films as a source of defects due to a preferential re-sputtering. This causes significant compositional deviations. Such a detrimental effect can be prevented by introducing a background gas (e.g. oxygen) that can simultaneously incorporate with and moderate the kinetic energy of arriving atoms. This is one of the most important interdependences between PLD growth parameters. Therefore, a suitable balance between laser fluence and background gas is essential to obtain the desired plume interaction with the background gas and ensure an optimal kinetic energy of arriving atoms to the substrate. Another important aspect on manipulating the laser fluence is to control the stoichiometry of materials from the ablated target. Especially for complex compound materials, a dissimilar ablation with an inadequate fluence that can preferentially ablate particular elements causes the formation of non-stoichiometric films. For example, in the case of $SrTiO_3$, a preferential ablation of Ti can be induced by increasing laser fluence, leading to the formation of Ti-rich (Sr-deficient) STO film growth. In other words, a delicate tuning of laser fluence is an effective method to induce and control desired atomic defects in PLD films for the creation of defect-mediated physical and chemical properties [126, 127].

4. **Repetition rate and target-to-substrate distance:** Repetition rate can also influence the growth mode and composition of materials. This effect can become significant when the materials are comprised of light-elements and elements for the formation of volatile phases (with their high vapor pressure). For example, laser repetition rates significantly affect the growth mode and composition of

$SrRuO_3$ films. Ru deficiency was found in the $SrRuO_3$ films when the films were deposited with high frequency (≥ 10 Hz) due to the increased amount of arriving species and following enhanced random island nucleation. Subsequently, the islands can be engulfed with newly incoming species and thus increased random adatom interactions which can enhance the probability of volatile $RuO_{3/}RuO_4$ forming [128] Thus, the increased random adatom interactions in the film's nucleation and growth process need to be avoided for homogeneous and stoichiometric film growth. The target-to-substrate distance shows a strong influence on film deposition rate (thickness), composition, and film crystallinity. Larger distance causes a reduction of deposition rate, while shorter distance causes an increase in the deposition rate. A set of closer depositions can give a strong rebound of ablated species and damage of deposited films due to very high kinetic energies (> 1000 eV). Thus, in a given pressure with a background gas, it is important to set a longer distance which is larger than the mean free path of ablated species. This leads to the interactions between the plume species and the background gas. For oxygen-stoichiometric oxide film growth, these interactions are mostly desired using reactive oxygen background gas to enhance the incorporation of oxygen species in the films. Furthermore, the composition of multicomponent films can be strongly influenced by the distance. When the target-and-substrate distance increases at a given background gas, a deficit of lighter elements occurs due to relatively higher scattering events, compared to those for heavier elements. Also, such a long distance significantly lowers the kinetic energies of arriving species to the substrate, resulting in lower adatom mobility and a subsequent poor film crystallinity.

In this work, we carefully considered all the above deposition parameters to achieve high-quality functional VO2 films using a PLD system in EPFL-CMi (Solmates SMP 800). Firstly, all other PLD deposition conditions, reported by other research groups, were compared to obtain insights how general deposition parameters (i.e. laser fluence and P_{O_2}) influence the resistive switching characteristics of VO2 films as illustrated in figure 3.4[129–148]. Although specific PLD deposition parameters for film growth usually depend on laboratory environment and equipment setup, this comparison clearly indicates that the interdependence between PLD parameters, e.g., a certain laser fluence ($\approx 2\ J/cm^2$) and relatively sufficient oxygen background pressure ($\approx P_{O_2} < 10^{-2}$ mbar), is important to obtain high-quality VO2 films with high resistive switching

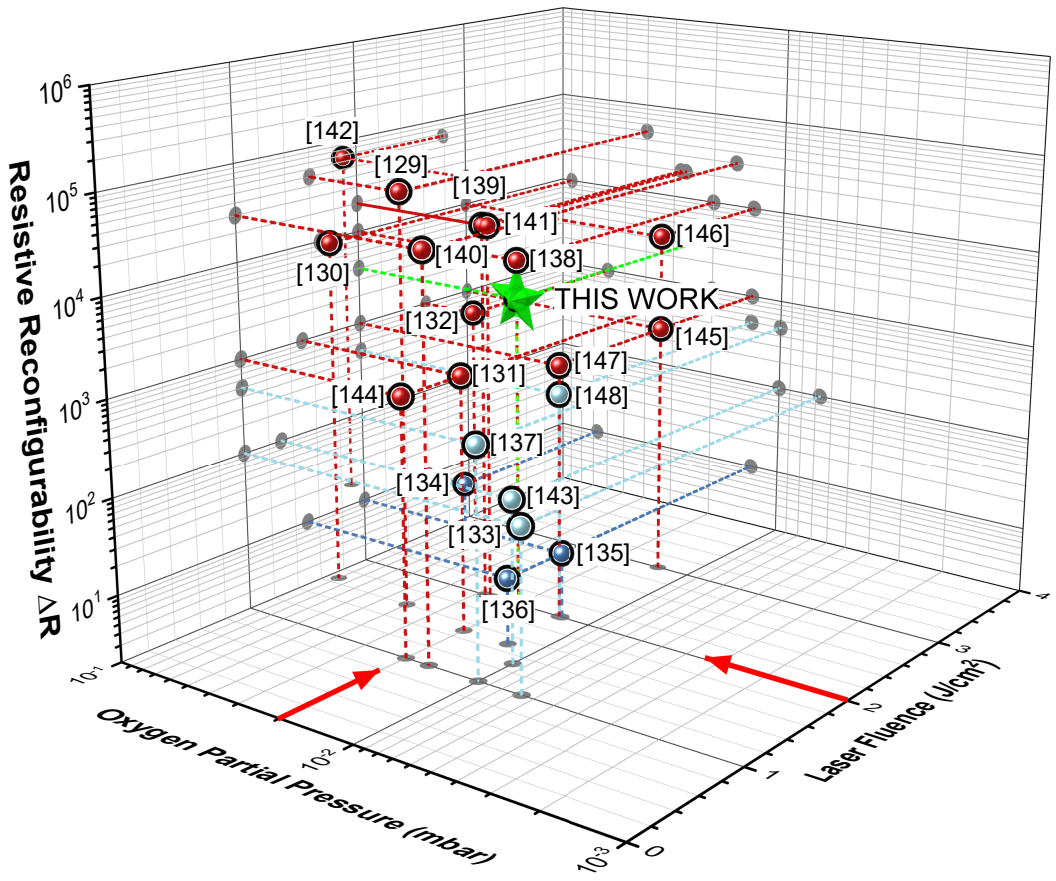


Figure 3.4: A comparison of resistance switching ratios (ΔR of various VO_2 films grown by different PLD deposition parameters (P_O and laser fluence) using data from [129–148]; Blue data points represent reported films that show resistive switching ratios lower than 10^3 while deep blue data points correspond to switching ratios lower than 10^2

ratios (ΔR > 10^3). Otherwise, electrically leaky VO2 films are formed with poor switching characteristics (ΔR < 10^2). Based on this, we carried out an optimization study for high-quality VO2 film deposition by controlling PLD deposition parameters, laser fluence and P_{O_2}. Details of this work will be discussed in the following section 3.3. All of the films presented in this thesis were deposited on SiO_2/Si substrates and thus there is no epitaxial relationship between the films and the underlying layers/substrates. Hence, all of the PLD depositions yield the formation of polycrystalline films with columnar grain structures in 3D-island growth mode (Volmer-Weber mode): when the stable clusters nucleate on the substrate and grow in 3D to form islands [149].

3.2.2 Device fabrication Process Flow

Two-terminal VO_2 devices were fabricated at EPFL's Center of MicroNanoTechnology (CMi) starting from 4 inch 525 μm thick p-type silicon wafers passivated with 200 nm of wet thermally grown silicon dioxide (SiO_2). The wafers were subsequently coated with a VO_2 thin film by means of the Pulsed Laser Deposition process described in the previous section.

Following VO_2 deposition, we performed a standard bi-layer lift-off photolithography process in order to define electrical contacts. The wafers were spin-coated with a double layer photoresist (PR) consisting of 400nm of sacrificial LOR5A resist followed by a 1.1 μm layer of the commercial positive photoresist AZ-1512 HS. The photoresist-coated wafers were then exposed using a Heidelberg MLA150 mask-less aligner tool in order to define the contact geometry. The MLA150 allows for pixel-by-pixel exposure of the entire wafer surface using a 405 nm diode laser focused and scanned across the entire design area. Following the exposure, carried out with a dose of 100 mJ/cm^2, the wafers were developed using AZ 726 MIF developer, which is an organic solution based on tetramethylammonium hydroxide (TMAH). The TMAH solution develops the exposed areas of the AZ1512 positive photoresist but in addition also dissolves part of the LOR5A sacrificial layer underneath the non-exposed PR areas. This creates an undercut beneath the remaining PR, facilitating the subsequent lift-off process. The amount of undercut is controlled by the thicknesses of the PR layers and the development sequence and duration. Spin coating and development as well as control of their respective parameters were performed on an EVG150 automated coater/developer processing station using standard recipes developed by the CMi staff.

The developed wafers were then transferred to an Alliance Concept EVA760 metallic layer evaporation equipment. The EVA760 employs an electron beam to heat up a crucible containing the target metal causing it to evaporate on the sample surface. Using this method, we coated the wafers with a 100 nm thick platinum (Pt) layer using an intermediate 5 nm thick titanium (Ti) layer in order to promote adhesion between the Pt metal and the underlying VO_2 film. In order to minimize heating of the substrates during metal evaporation, the wafers were backed using thick copper discs to increase thermal mass and the process was run at a working distance of 450mm between the crucible and the substrates (the highest available on EVA760).

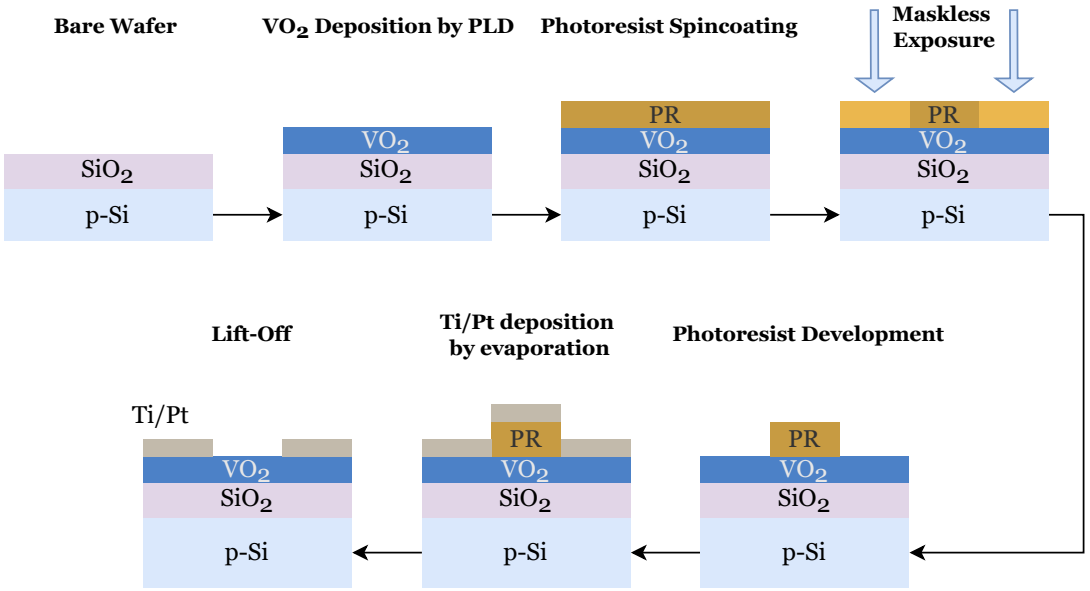
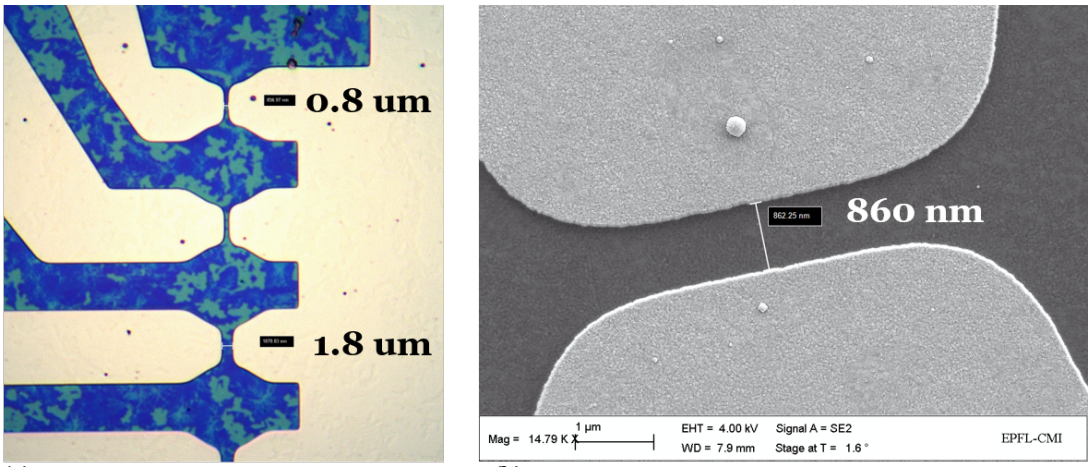


Figure 3.5: An established process flow for the fabrication of two-terminal VO_2 devices

Finally, after Ti/Pt metal deposition was carried out, the wafers were put in a bath of MICROPOSIT™Remover 1165 photoresist stripping agent and were left for 24 hours at room temperature on a chemical wetbench, ensuring complete dissolution of the remaining (unexposed) photoresist along with the Ti/Pt layer above it, revealing the device definition laser-written in the exposure stage. AZ-1512 HS is not a particularly high-resolution photoresist (critical dimensions are listed as minimum 2 μm) so in order to obtain sub-micron gaps between the metal electrodes, an overestimation of the device length (electrode gap size) was necessary in the layout design. According to the Scanning Electron Microscope (SEM) micrograph shown in figure 3.6(b), the shortest achieved gap size was $\approx 0.8\ \mu m$, starting from a layout definition of 3 μm. This suggest a PR overdevelopment of 2.2 μm in total corresponding to 1.1 μm removal on each side of the device gap, also confirmed by the optical micrograph shown in figure 3.6(a), The overdevelopment was identical when a 4 μm gap design was employed, resulting in an effective device length of $\approx 1.8 \mu m$.



(a) (b)

Figure 3.6: Optical microscopy (a) and SEM (b) images for the fabricated two-terminal VO_2 lateral devices

3.2.3 VO_2 thin film characterization

Electrical resistivity

The resistivity vs. temperature curves of the PLD VO_2 thin films were measured by means of a 4-point probing setup as shown in figure 3.7. Once deposited by PLD, the wafers under test were cleaved into rectangular chips and copper contact wires were attached to the pristine VO_2 film surface in a collinear arrangement at an equal spacing "s" much greater than the film thickness. Wire bonding was carried out using indium (In) balls to promote adhesion, and the bonded samples were placed in a temperature-controlled environment (Delta Design 9023 Chamber). The 4 contacts (indicated in numbers in figure 3.7) were connected to a pair of Source-Measurement Units (SMUs). Temperatures, input currents and output voltages are controlled and monitored via an in-house designed LabView program. The SMUs are used to force a probing current I_P through the outer contacts (1,4) and measure the resulting voltage V_{23} between the inner contact points (2,3). The same bus is shared with a multimeter that helps measure the thermocouple TC attached to the sample chuck inside the chamber as well as with the temperature controller of the chamber itself. This arrangement allows for automatic programming of temperature-controlled electrical measurement cycles. At each temperature setpoint (verified by the TC reading at sample level) a sequence of probing currents is applied to the measured samples, and the resulting voltages are recorded after temperature stabilization. Using the I_P and V_{23} values recorded at

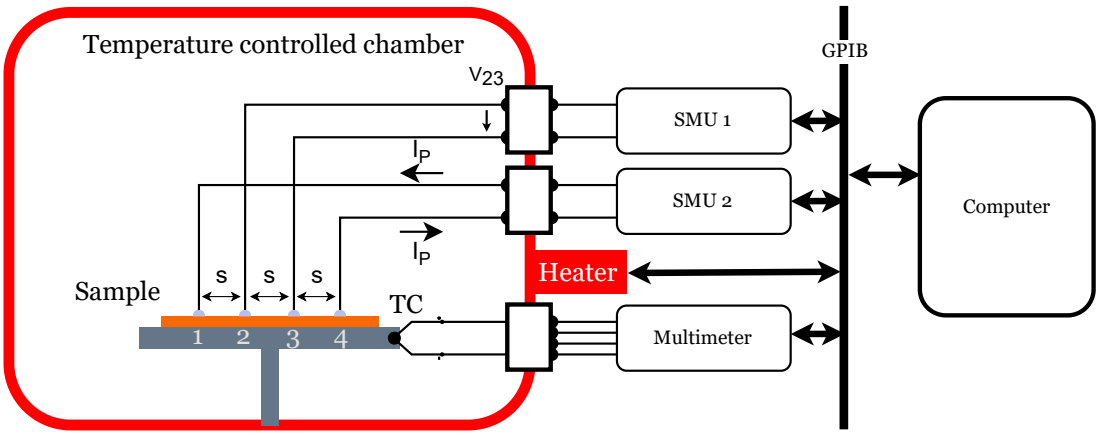


Figure 3.7: Four-point probing setup used for resistivity measurement of the VO_2 thin films in a temperature-controlled environment

every programmed temperature value, the thin film resistivity can be calculated by [150] :

$$\rho = \frac{\pi}{ln(2)} \cdot \frac{V_{23}}{I_P} \cdot t \tag{3.1}$$

where V_{23} represents the voltage drop across the inner contacts, I_P represents the current applied to the outer contacts, and t represents the film thickness.

Scanning Electron Microscopy

The Scanning Electron Microscope (SEM) typically consists of an electron gun, a focusing column, a sample stage, and various different electron detectors. The electron energy is adjusted in a range of 1 – 30 keV to achieve different depths of interaction between electrons and sample surface followed by the inelastic mean free path of electrons. This is because the electron scattering event at the surface is dependent on the energy of the incident electrons, the incident angle with respect to the surface of the sample, and the atomic number and density of the elements in the sample. Secondary electrons (SEs) arise from the emission of the valence electrons in the sample excited by the incident electron beam. Since, only the SEs generated at the surface of the sample are emitted, such SE emission allows for a surface sensitive measurement. Moreover, SE emission is larger in an oblique incidence of the electron beam, and by measuring the difference in the incident angle of the electron beam, the

distinct brightness of the sample surface can be obtained. Therefore, the SEs collected by several detectors are used for detailed imaging of the topography of the sample surface. This microscopy technique was applied to study the surface morphologies and thicknesses of the oxide samples presented in this chapter. The SEM images were acquired using a Zeiss LEO 1550 SEM, in EPFL-CMi.

3.2.4 Electrical characterization of VO_2 two-terminal devices

In order to analyze the electrical switching dynamics and extract IMT and MIT switching parameters of the two-terminal VO_2 devices that were fabricated, we performed electrical characterization using a Keithley 4200A-SCS semiconductor parameter analyzer (SPA). The two-terminal VO_2 devices were connected to the SPA using needle probes in a Cascade Summit 2000 semiconductor probing station, and electrical biasing of the device terminals was achieved using two source-measurement units (SMUs) integral to the SPA. The devices were subjected to both voltage and current sweeps in order to obtain the current-voltage (I-V) and the voltage-current (V-I) characteristics, as shown in figure 3.8. The voltage sweeps were carried out under a current

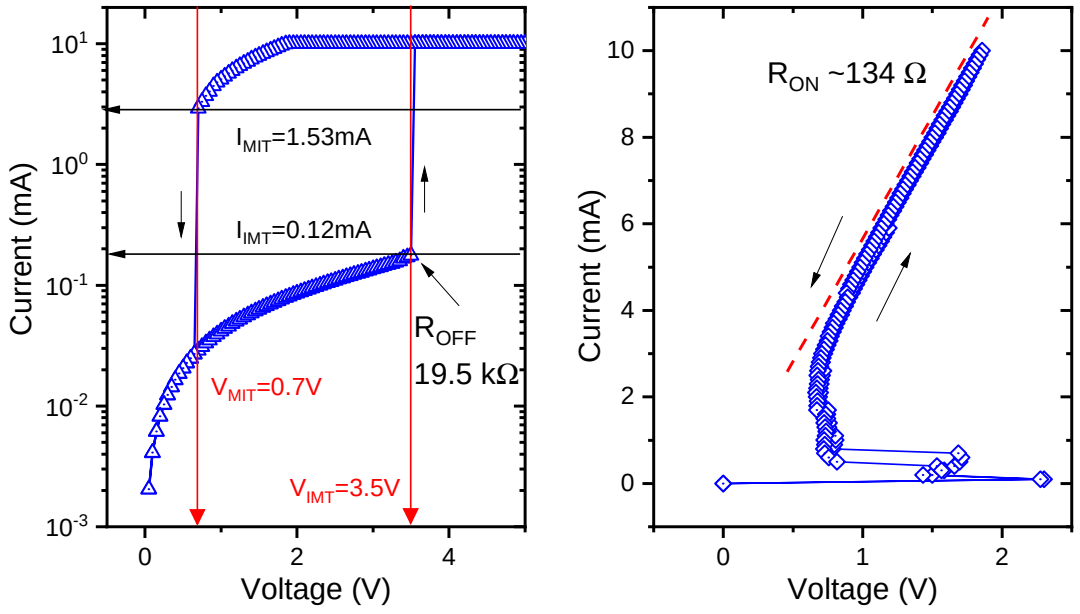


Figure 3.8: Semiconductor parameter analyzer measurements: (a) - Current-Voltage characteristic allowing extraction of IMT and MIT threshold voltages along with IMT and MIT currents and off-state resistance, and (b) - Voltage-Current characteristic allowing extraction of on-state resistance R_{ON}

compliance limit of $I_C = 10mA$ in order to protect the devices from excessive power dissipation once the IMT threshold is reached and the devices transition to the low-resistance state. The I-V characteristic curve obtained from the voltage sweep (figure 3.8(a)) allows for the extraction of the turn-on and turn-off voltages (associated to the IMT and MIT, respectively) as well as the turn-on and turn-off currents (I_{IMT} and I_{MIT}, respectively). In addition, the I-V characteristic allows for the extraction of the off-state (insulating) resistance of the VO_2 device at the IMT transition. Finally, the V-I characteristic obtained by performing the current sweep (figure 3.8(b)) allows for the extraction of on-state electrical resistance. This can be done by measuring the slope of the characteristic once the VO_2 IMT has been triggered. In this case, the reciprocal of the measured slope indicates the value of R_{ON}. The set of measurements presented in figure 3.8 correspond to a device with a length of L=0.8 μm and a width of W=5 μm that was fabricated using the process described in section 3.2.2 on a thin film of VO_2 deposited with a laser fluency of 2 J/cm^2, and at an oxygen partial pressure $P_O = 0.02mbar$.

3.3 Optimization of the PLD process for VO_2 thin films

3.3.1 Laser Fluence

In this work, various PLD deposition parameters (i.e. the interdependent parameters between laser fluence and P_{O_2}) were tuned to obtain a growth window of functional VO_2 films. We first investigated the effect of laser fluence (1 - 2 J/cm^2) in a given oxygen partial pressure (P_{O_2} = 0.01 mbar) while fixing the substrate temperature at T = 450 °C, which is the maximum temperature allowed in CMOS processing. Figure 3.9 illustrates the variation in the resistive switching ratios of VO_2 films as a function of laser fluence, deposited on SiO2 (200 nm)/Si. To get a consistent thickness for the deposited VO_2 films, the deposition time of each film was adjusted in an exponential relation of laser fluence and deposition time [151]. As a result, the thickness of the deposited films is ≈220 –250 nm. Using the $VO_2/SiO_2/Si$ wafers, two-terminal VO_2 lateral switching devices with an effective channel length of ≈ 0.8 μm were fabricated and the I-V curves of each VO_2 switch were measured by 100 switching cycles at room temperature: (i) current measurement at each voltage step while performing DC voltage sweeps (0 V → 5 V → 0 V) with a current compliance of 10 mA, which was set

in order to limit the metallic state current and prevent permanent device breakdown, and (ii) voltage measurement at each current step during current sweeps (0 A $\rightarrow$ 10 mA $\rightarrow$ 0 A).

In figure 3.9 we present the electrically driven I-V curves for the VO_2 film devices as a function of laser fluence. All the switches show visible electrically induced MIT for both activation modes as abrupt changes in the current (voltage) during voltage (current) sweeps, marked by a sudden increase (drop) of current (voltage) in each circuit with a threshold voltage (current) of the IMT, V_{IMT}, or by a sudden drop (increase) of current (voltage) with a threshold voltage (current) of the MIT, V_{MIT}. However, it was found that large variations occur in the abruptness of electrically-induced IMT (/MIT), the on-and-off switching ratio, and threshold voltages when the laser fluence is increased up to $\approx 2\ J/cm^2$. The VO_2 film grown using the lowest laser fluence of $\approx 1\ J/cm^2$ shows a very low R_{OFF}/R_{ON} ratio of 2.27 with a large leakage current (> 3 mA) before the occurrence of an abrupt electrical IMT. Such a poor electrical switching performance becomes more obvious with the current sweeps. In principle, when the IMT is triggered by a critical current injection, a negative differential resistance (NDR) appears as a consequence of a sudden rise in conductivity and a simultaneous reduction in the voltage across the VO_2 device. If the phase transition dynamics is homogeneous, a non-hysteretic MIT of the device on the load should appear when the injected current reaches values below the critical one. However, multiple and irreversible NDR states were found in both of the IMT and MIT, resulting from a largely disordered crystallinity, a multiple electrical network across the channel and subsequent inhomogeneous (non-abrupt) phase transition dynamics. In contrast, a significant increase in the on-and-off resistance ratio (R_{OFF}/R_{ON}) of the VO2 film devices, grown by the highest laser fluence of $\approx 2\ J/cm^2$, was found to be $R_{OFF}/R_{ON} \approx 42.77$ with a largely reduced leakage current of $\approx 500\ \mu A$. A well-defined reversible NDR in the VO_2 switch was found with a larger voltage drop ($\Delta V \approx 2.45V$) during the current-driven transition process.

Furthermore, the threshold voltage, which is a critical voltage to switch an off-state (insulating/semiconducting state) to an on-state (metallic state) and vice versa, gradually increased with higher laser fluence. Effective threshold electric fields for the insulating-to-metal transition of the VO_2 lateral device were found in the range of $\approx 34kV/cm$. Variations in the resistance switching ratios and threshold voltages of all the VO_2 switches with different laser fluence are presented in figure 3.10.

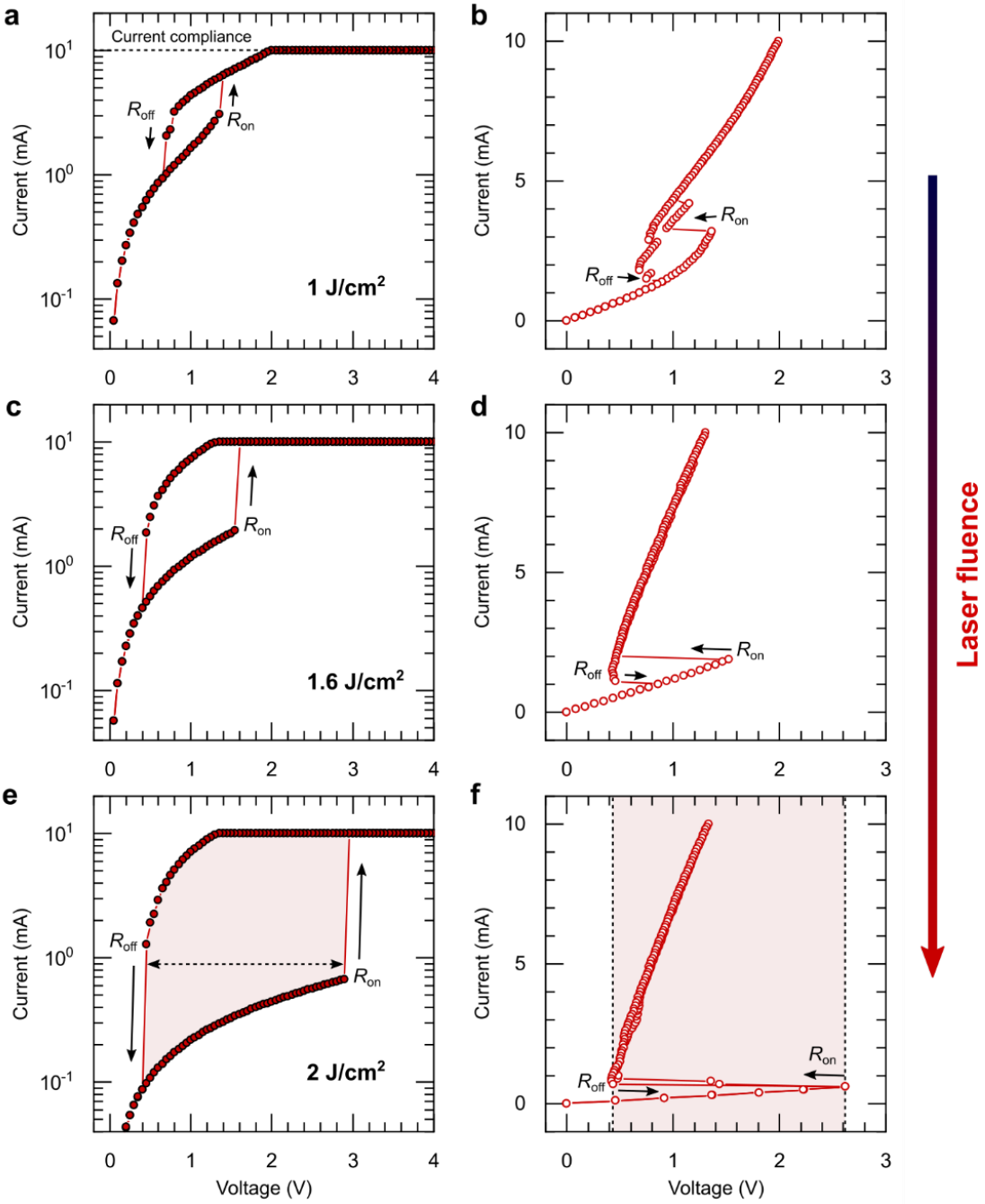


Figure 3.9: The I-V characteristic in both V- and I-modes of two-terminal VO_2 film devices with the same channel length of 800nm. The VO_2 films were grown at different laser fluence (1-2 J/cm^2). The left panels (a,c,e) show the current variations of the devices measured by double voltage sweeping (0V-5V-0V). The right panels (b,d,f) show the voltage changes of the devices measured by current injection (0A-10mA-0A)

The results presented above clearly show a strong effect of laser fluence on the electrical switching characteristics of the deposited VO_2 films. As mentioned in section 3.2.1, PLD laser fluence strongly influences the film growth dynamics, crystallization, and microstructural properties (the size and orientation of grains) as it modulates the kinetic energy of the arriving species during the PLD growth process. The lower arrival energies by lower laser fluence translate to lower adatom mobility, thus the formation of smaller grain structure (greater ratios of surface-area-to-volume) and poor crystallinity at a given temperature are expected when lower laser fluence is employed. The electronic properties of VO_2 are strongly determined to a great extent by grain boundary defects which largely depend on the size, shape, and crystallographic orientation of the grains [152, 153]. It was found that oxygen vacancies, which is one of the typical defects in VO_2, is preferentially accumulated at grain boundaries, resulting in lower resistance and work function at the grain boundaries [154]. This significantly inhibits the MIT characteristics (e.g. R_{OFF}/R_{ON} ratio, abruptness, and leakage current) of VO_2. In fact, a much smaller grain size (an average size of $\approx 35nm$) in the VO_2 film grown by the lowest laser fluence of 1 J/cm^2 was found as shown in figure 3.11. This directly reflects a relatively non-abrupt IMT (/MIT) switching and a small switching ratio (<10) with a large leakage current in the R_{OFF} state (figure 3.9). On the other hand, such detrimental effects on the IMT/MIT of the VO_2 film devices are significantly reduced with larger grain size distribution (reduced grain bound-

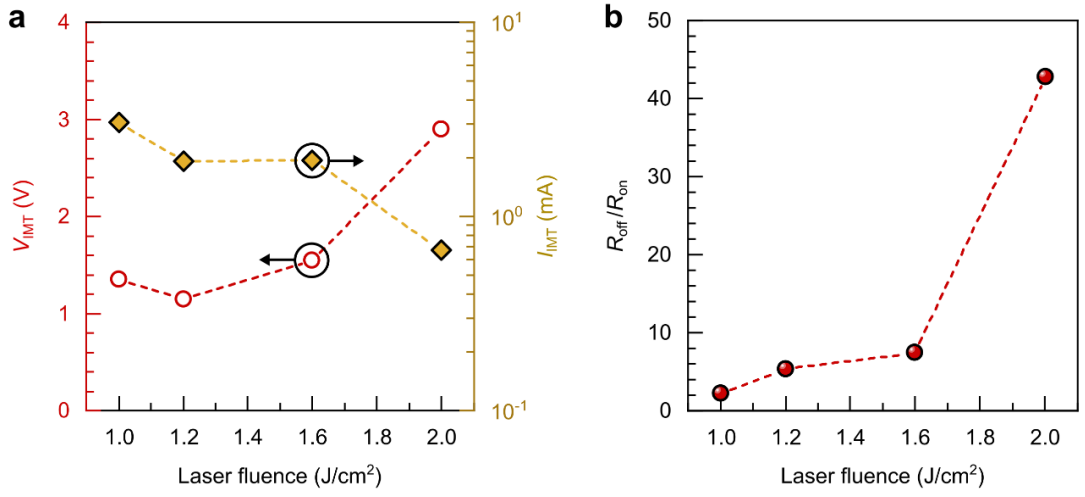


Figure 3.10: (a) - The threshold voltage and current for the insulator-metal transition of the VO_2 devices as a function of laser fluence; (b) - The resistance switching ratios (R_{OFF}/R_{ON}) of the devices as a function of laser fluence

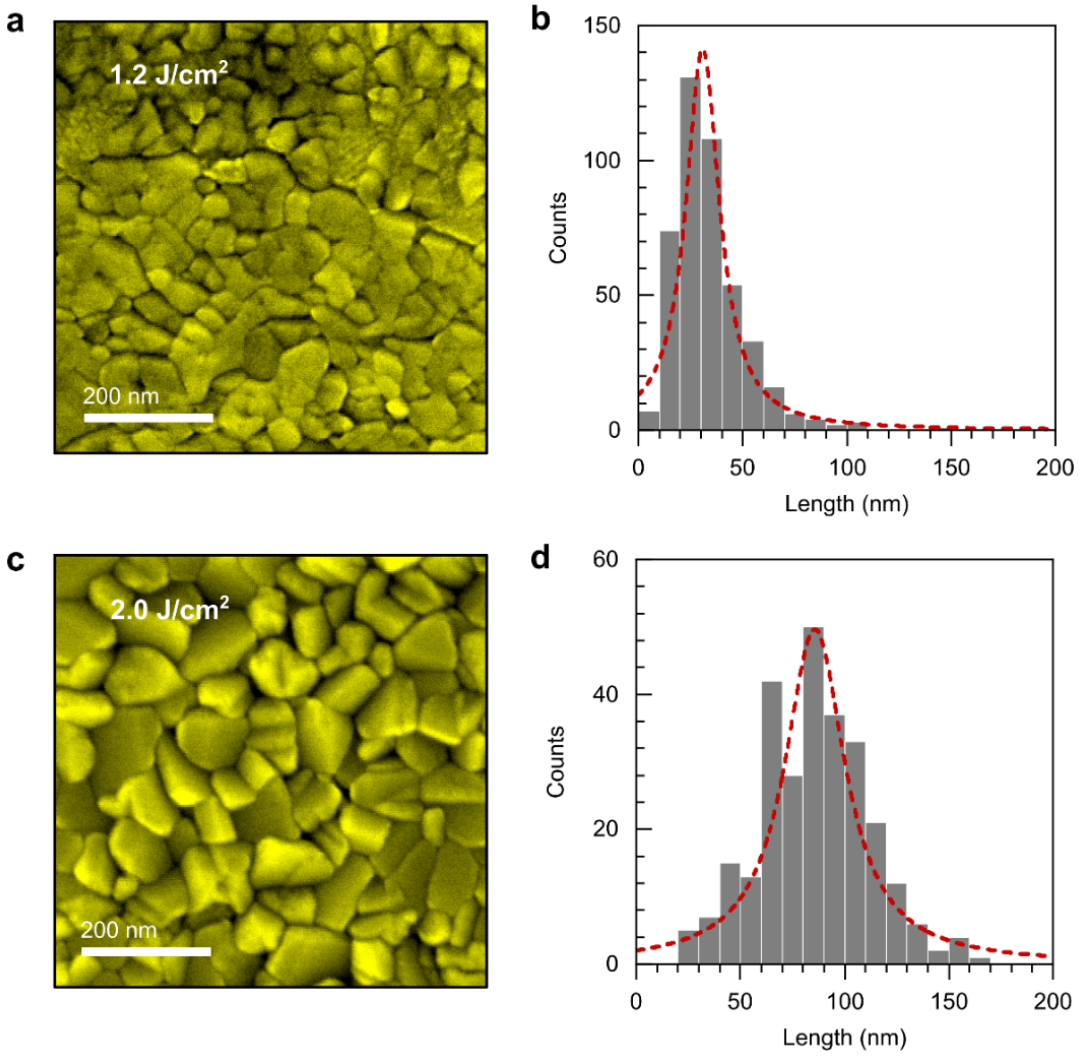


Figure 3.11: (a) - A planar view SEM image of a VO_2 film grown on SiO_2(200nm)/Si in $P_O = 0.01 mbar$ with a relatively low laser fluence of 1.2 J/cm^2; (b) - The corresponding grain size distribution. The averaged grain size is 35 nm; (c) - An SEM image of a VO_2 film grown using a higher laser fluence of 2 J/cm^2, while all other parameters were kept the same; (d) - The corresponding grain size distribution, with an average grain size of 86nm

ary density and oxygen defects), resulting in the enhanced switching characteristics (switching abruptness, ratio, and leakage current) in the film grown by the highest laser fluence of 2 J/cm^2.

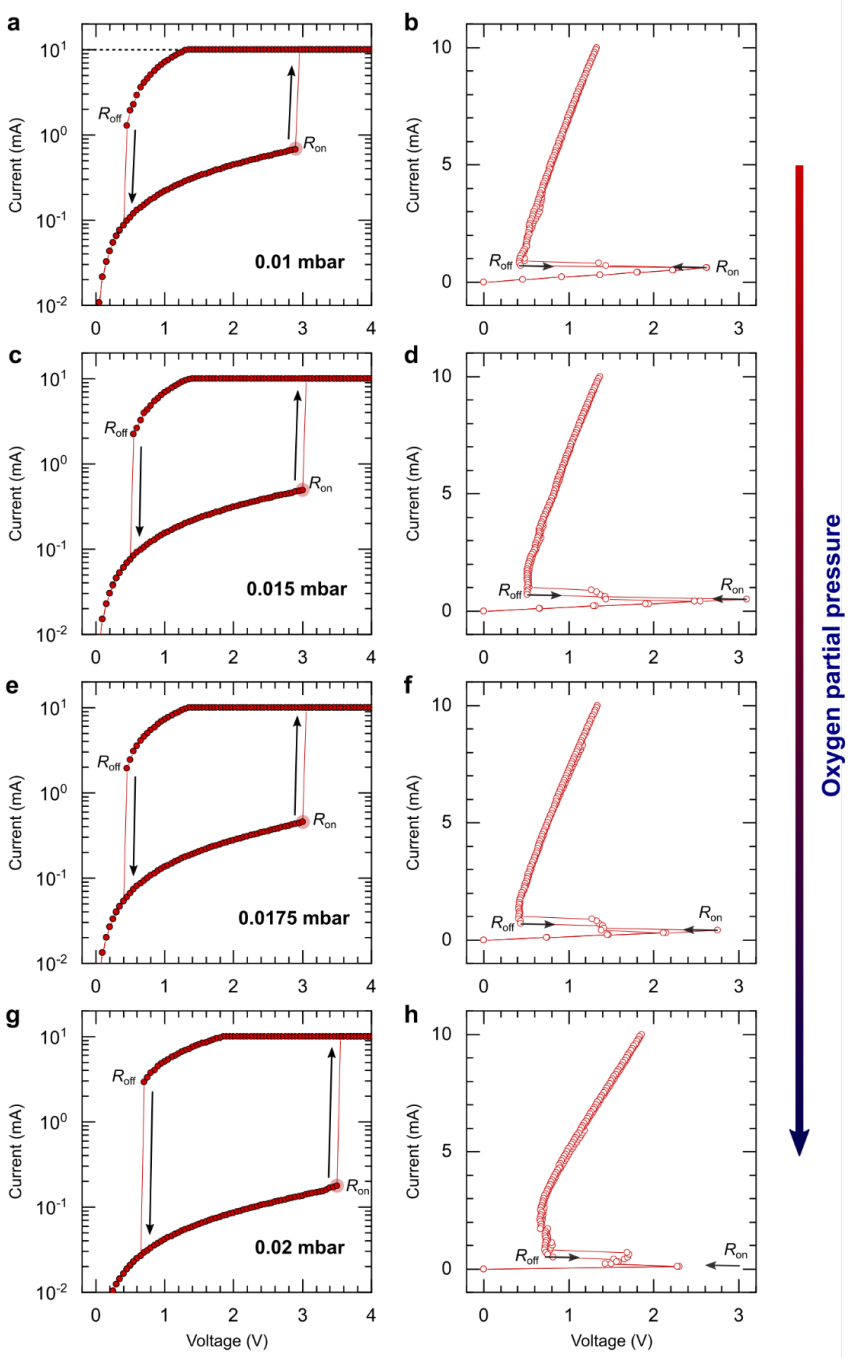


Figure 3.12: The I-V characteristics in both V- and I-modes of two-terminal VO_2 film devices as a function of PO. The left panels (a,c,e,g) show the current variations of the devices, measured by double voltage sweeping (0V - 5V - 0V). The right panels (b,d,f,h) show the voltage changes of the devices, measured by current injection (0A - 10mA - 0A)

3.3.2 Oxygen partial pressure

Based on the results presented above, it is clear that the elimination of oxygen defects in VO_2 films is essential in order to achieve the MIT functionality, consistent with recent reports [155, 156]. However, the VO_2 film grown by the laser fluence of 2 J/cm^2 at P_{O_2} = 0.01 mbar still shows poor switching ratio with a large off-state current ($R_{OFF} \approx 4.30k\Omega$). Thus, our next attempt was to find an optimal P_{O_2} condition for VO_2 film growth by comparing various P_{O_2} (0.01 mbar to 0.03 mbar) to improve the electrical switching performance of the VO_2 devices. Figure 3.12 exhibits the electrically-driven IMT (MIT) of the two-terminal VO2 switches (with the same channel length, $\approx 0.8\ \mu m$) with different P_{O_2}. The results reveal a continuous decrease in the current of the insulating/semiconducting states of the switch from ≈670 μA to ≈170 μA when P_{O_2} increased up to 0.02 mbar. The VO_2 switch grown at 0.02 mbar shows the largest R_{OFF}/R_{ON} ratio (145.75) with sharp IMT and MIT characteristics during voltage sweeps. The V_{IMT} slightly increased to 3.5 V ($E_{Th} = 40kV/cm$) with P_{O_2} = 0.02 mbar, while the V_{MIT} remained almost the same (0.5 – 0.7 V). This V_{IMT} increase could be due to the minimized effect of oxygen vacancies (a reduced grain boundary conductivity in the current channel). The P_{O_2}-dependent threshold voltage/current and R_{OFF}/R_{ON} ratios for the VO_2 switches are shown in figure 3.13.

To further understand the phase transition characteristics of the VO_2 films grown

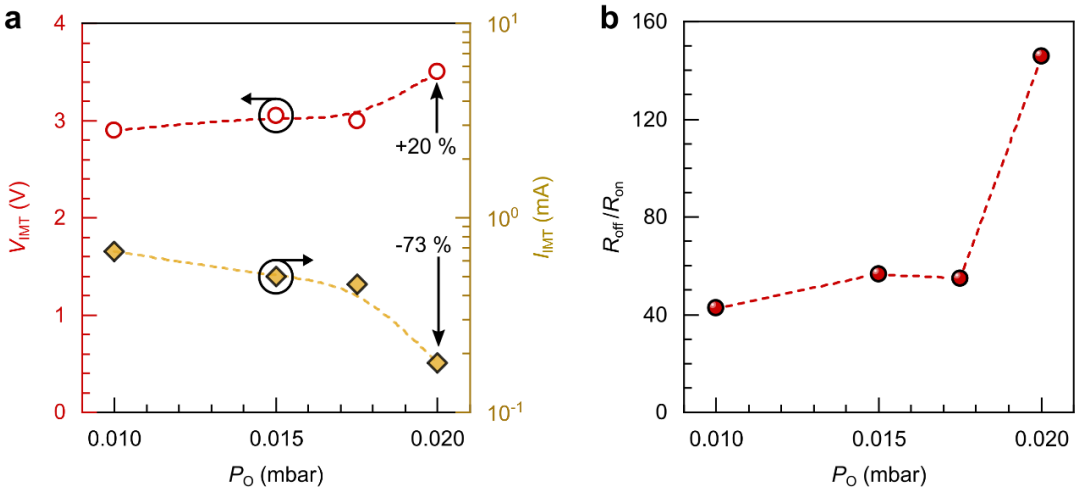


Figure 3.13: (a) - The threshold voltage and current for the insulator-metal transition of the VO_2 devices as a function of P_{O_2}; (b) - The resistance switching ratios (R_{OFF}/R_{ON}) of the devices as a function of P_{O_2}

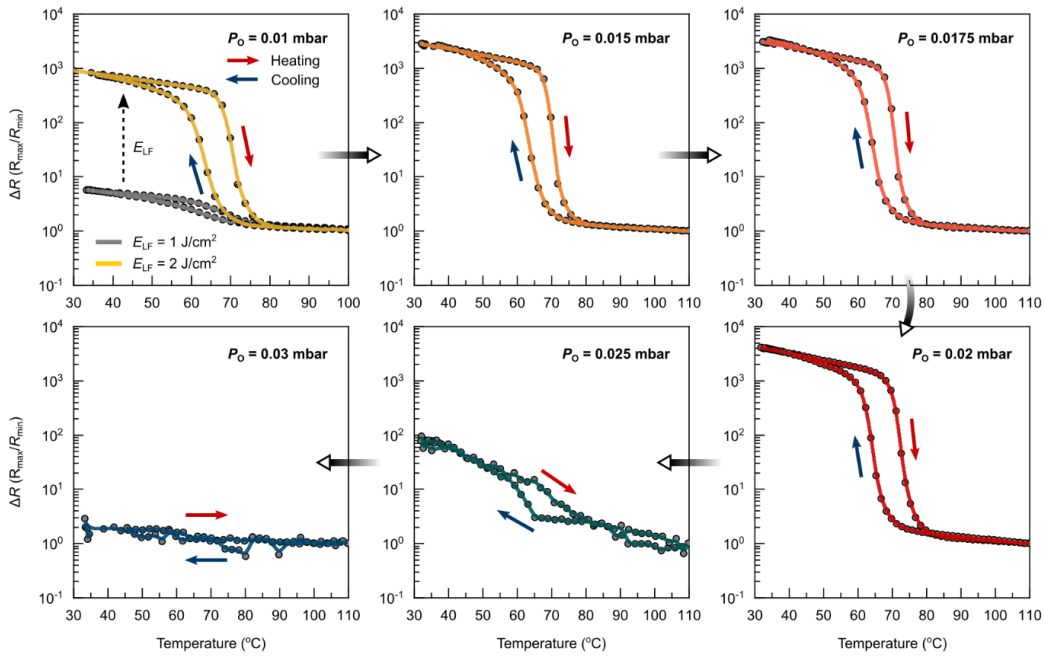


Figure 3.14: Temperature-dependent resistance variations of the VO_2 films as a function of P_{O_2}, grown by laser fluence E_{LF} of 2 J/cm^2. The resistance variation of each sample was recorded by temperature sweeps (heating to cooling 30 °C $\rightarrow$ 110 °C $\rightarrow$ 30 °C). For comparison, the resistance variations of the films are determined by R_{MAX}/R_{MIN}. Only the upper left panel compares the thermally induced resistance changes of the films, grown at different laser fluence (1 J/cm^2 and 2 J/cm^2) in P_{O_2} (0.01 mbar).

by different P_{O_2}, the temperature-dependent electrical resistance of the VO_2 films was measured by temperature cycling (30 °C $\rightarrow$ 110 °C $\rightarrow$ 30 °C), with a temperature interval of 2 °C and temperature stabilization time of 10 minutes at each temperature setpoint). In figure 3.14 we illustrate the normalized temperature-dependent resistance for the films as a function of P_{O_2}, obtained using the four-point probe measurements. A strong P_{O_2} dependence on the temperature-induced electrical resistance change ($\Delta R = R_{OFF}/R_{ON}$) of the samples was found. The VO_2 film grown at P_{O_2} = 0.01 mbar shows a relatively small ΔR (50) in temperature. By increasing P_{O_2} up to 0.02 mbar, the thermally-driven ΔR of the films greatly increased to $\approx 4 \times 10^3$. Note that the achieved large thermally-induced resistance switching ratios are comparable with ratios (> 10^3) usually observed in well-grown epitaxial VO_2 films on Al_2O_3/TiO_2 and single VO_2 crystals [88, 130, 156, 157]. However, when higher P_{O_2} (0.025 and 0.03 mbar) was employed for the film growth, the films significantly became just resistive (R = 10 -100 Ω at RT) without notable hysteretic transition characteristics. Such metallic

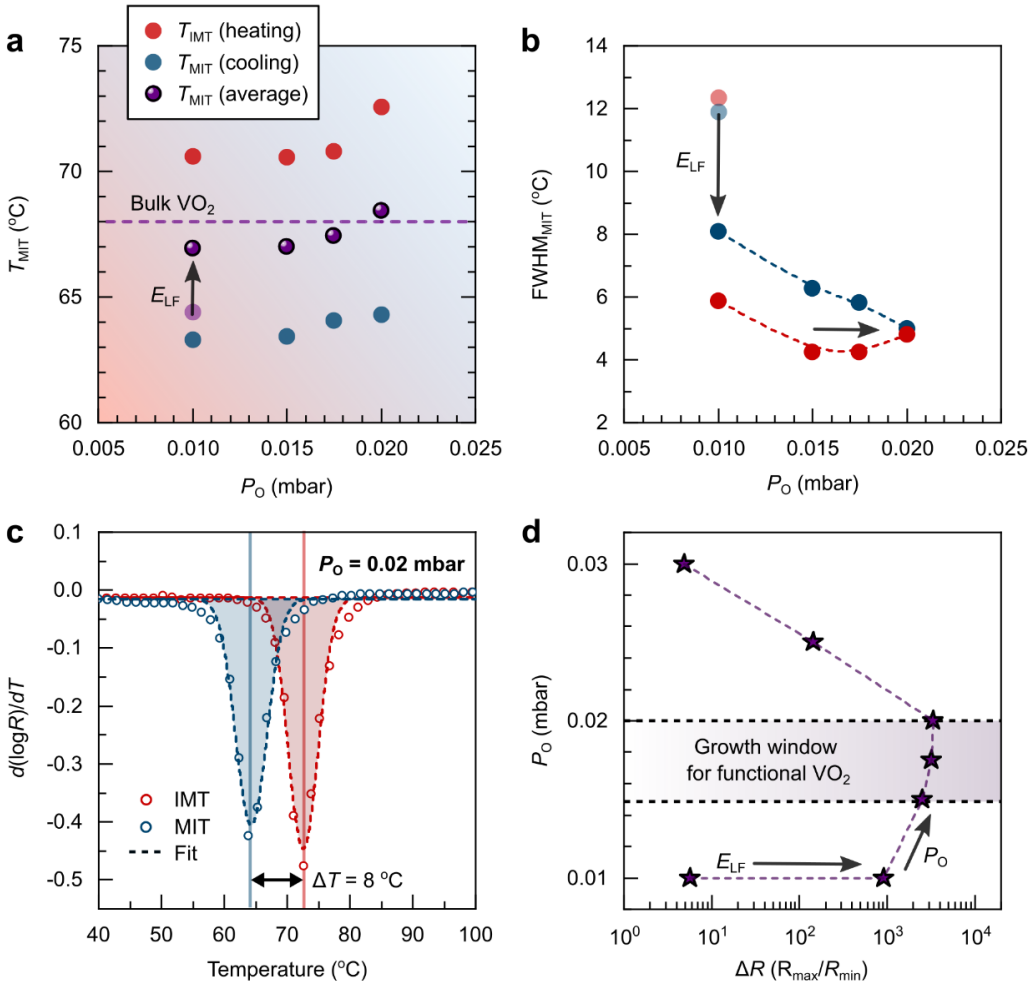


Figure 3.15: (a) - Variations in the IMT, MIT, and averaged transition $[(T_{IMT}+T_{MIT})/2]$ temperatures of the VO_2 films grown by different P_{O_2}. When P_{O_2} increases up to P_{O_2} = 0.02 mbar, the averaged phase transition temperatures reaches a typical MIT temperature (68 °C) of bulk VO_2. (b) The FWHM values for $d(logR)/dT$ versus T plots of the IMT and MIT, which reflect the abruptness of the phase transitions. (c) A $d(logR)/dT$ versus T plot for a VO_2 film grown in P_{O_2} = 0.02 mbar which shows symmetrical IMT and MIT with a hysteresis width of $\Delta T = 8°C$. (d) The optimized growth window (0.015 mbar ≥ P_{O_2} ≥ 0.02 mbar, 2 J/cm^2) for the deposition of high-quality functional VO_2 films with high resistance variations (>10^3).

behaviors in the VO_2 films grown in higher P_{O_2} are unexpected, rather than forming other insulating vanadium oxide phases (e.g. V_2O_5) with excess oxygen.

A reasonable explanation could be the formation of intrinsic defects (i.e. oxygen interstitials) in oxygen-rich VO_2 or mixed valency compounds [158, 159]. The most

abundant intrinsic defects in VO_2 are oxygen vacancies and oxygen interstitials, which can be formed under oxygen-deficient and -rich conditions during film growth. Both point defects can contribute electrons or holes as free carriers, which can be correlated with the charge localization within the electronic band gap (between the filled a1g band and empty e_g^{π} band) of VO_2. For example, two oxygen interstitials can create acceptor-like energy states near the valence bands (O $2p$ and V^{+4} $3d$) of VO_2. This could provide four-hole carriers near the V^{+4} sites, leading to a reduction in the bandgap of VO_2 by band tailing [158, 160, 161]. Thus, the effect of such oxygen defects in oxygen-rich VO_2 may largely degrade the fundamental MIT characteristic of VO_2, as seen here.

Importantly, when P_{O_2} is increased up to 0.02 mbar, the thermal hysteresis loops (the IMT in heating and the MIT in cooling) tend to be symmetric with an identical full width half maximum (FWHM ≈ 5 °C) of the IMT and MIT transitions and the averaged transition temperature, [$T_{av} = (T_{IMT} + T_{MIT})/2$], eventually reaches the conventional MIT temperature (T_{av} = 68 °C) of VO_2, as illustrated in figure 3.15. However, it should be pointed out that there is a large discrepancy between electrically-driven (≈ 10^2) and thermally-driven resistance (≈ 10^3) variations of all the developed VO_2 films. This could be caused by external contact resistance between the VO_2 and the Ti adhesion layer (e.g. formation of highly resistive other vanadium oxide phases and $TiO_{2/2\text{-x}}$ through oxygen exchange) during device fabrication. This can largely vary the R_{ON} state of the excited VO_2 switches during device operation. Thus, further development on the VO_2-based device fabrication process is required (e.g by employing oxygen-inert metals) in the future.

3.4 Summary

The work presented in this chapter was performed in order to study and gain insight into the phase transition characteristics of VO_2 thin films and their close correlation with the Pulsed Laser Deposition (PLD) process.

After a thorough description of the PLD process, we established that thin films deposited by PLD are particularly sensitive to deposition temperature, laser repetition rate and target-to-substrate distance, background gas pressure and laser fluence. We found that higher deposition temperatures are beneficial and promote the development of grain structures, however, the purpose of this work was to obtain CMOS-compatible processing methods and as such the temperature employed was limited at 450 °C. Similarly, we found that lower laser repetition rates are preferred, and thus we carried out the study using a laser repetition rate of 5Hz, the slowest available on the Solmates SMP 800 installed in EPFL-CMi.

Following a review of several PLD deposition conditions reported by other research groups, we were able to identify that the interdependece of laser fluence and sufficient oxygen background pressure was important in order to obtain high resistive switching ratios ΔR in VO_2 thin films. Based on this, **we carried out an optimization study by controlling laser fluence (1, 1.6 and 2 J/cm^2) and oxygen partial pressure P_{O_2} (0.01, 0.015, 0.0175 and 0.02 mbar)**.

We observed that when deposited at low laser fluence (1 J/cm^2), the VO_2 films exhibit poor resistive switching ratio ΔR = 2.27 and considerably high leakage current (>3mA) in the off state. In contrast, we found that by employing a high laser fluence (2 J/cm^2), ΔR improves considerably (ΔR = 42.77) with reduced off-state leakage current of $\approx$ 500 μA. This result correlates with a measurable difference in grain size of the deposited thin film, with smaller grain size (35 nm on average) being measured at 1.2 J/cm^2 and larger grain sizes averaging 86 nm when high laser fluence was used (2 J/cm^2).

Upon choosing the optimal laser fluence at 2 J/cm^2, we continued the study by investigating the effect of oxygen partial pressure P_{O_2} on film quality. By increasing P_{O_2} from 0.01 mbar up to 0.02 mbar we observed a steady improvement in resistive switching ratio ΔR up to 145.75 at 0.02 mbar, accompanied by a considerable reduction in

off-state from $\approx 670\mu A$ down to $\approx 170\mu A$ for the sample deposited at P_{O_2}=0.02mbar.

Consequently, the results presented in this chapter clearly reveal that the control of P_{O_2} is essential for VO_2 film growth to obtain stoichiometric VO_2 films together with high resistance switching ratios, homogeneous phase transition dynamics under external stimulus (electrical and thermal excitation) and high endurance. The results also show significant detrimental effect of defects that are created under non-optimal PLD deposition processes and govern the entire microstructural and electronic properties of VO_2 films/devices. Thus, finding the optimal growth conditions is absolutely required to achieve highly functional VO_2 films. It is further emphasized that the established optimal growth conditions (e.g. temperature, laser fluence, and P_{O_2}) for VO_2 film growth **are CMOS-compatible, and thus can be integrated with standard CMOS circuits in a Back-End-Of-Line process flow**, an aspect which is greatly beneficial for the applications that we will discuss in the next chapters.

4 A 1T-1R Voltage Controlled Spiking Oscillator based on VO_2

4.1 Introduction

Oscillations in circuits containing devices that exhibit Negative Differential Resistance (NDR) have been observed as early as 1921 when Pearson and Anson conducted experiments using Neon gas lamps in conjunction with RC (resistor-capacitor) pairs [162, 163]. The two found that under certain conditions involving the operating point of the circuit and the characteristics of the neon lamp, the circuit could produce self sustaining oscillation of the current passing through the lamp, thus producing intermittent flashing.

Similarly, in devices based on VO_2, the reversible and hysteretic Metal-to Insulator Transition (MIT) determines a regime of negative differential resistance in the device I-V characteristic between the Metal-Insulator threshold and the Insulator-Metal threshold on the return path, enabling oscillatory behavior. Although oscillations in VO_2-based devices have been identified as early as 1975 [164], recently these properties of VO_2 attracted more attention due to its potential use in emerging fields such as neuromorphic computing. For example, Datta et al. [165] showed that such oscillators can be coupled in large numbers and exploit frequency locking either passively by capacitive coupling between oscillator cells or by employing active frequency control by means of variable load resistors to perform tasks associated to pattern recognition. Moreover, oscillator-like structures based on VO_2 can be tailored for single-shot operation, producing single, well defined spiking events - akin to neuron firing - that may open the door for applications using spiking neural networks [166].

4.2 Circuit analysis and Modeling

4.2.1 DC Operating point

In order to produce oscillations, VO_2 devices are commonly connected with parallel RC circuits, where the series resistor is chosen such that the VO_2 element is *properly biased*, while the capacitor acts as a storage element that filters out the abrupt changes in voltage and current induced by the VO_2 element during transition events. In this section, however, we are treating the biasing aspects of the VO_2 relaxation oscillator from a static perspective, so the circuit will be regarded as a simple series connection between a passive resistor and a VO_2 element, not taking the capacitor into account.

Properly biasing the VO_2 element is done by choosing the load resistance value such that its associated load line intersects the I-V characteristic of the VO_2 element in the negative differential resistance regime, highlighted in red in figure 4.1. Because the characteristic of the VO_2 element is hysteretic, showing two distinct switching thresholds, this gives rise to two possible operating points for the simple series connection

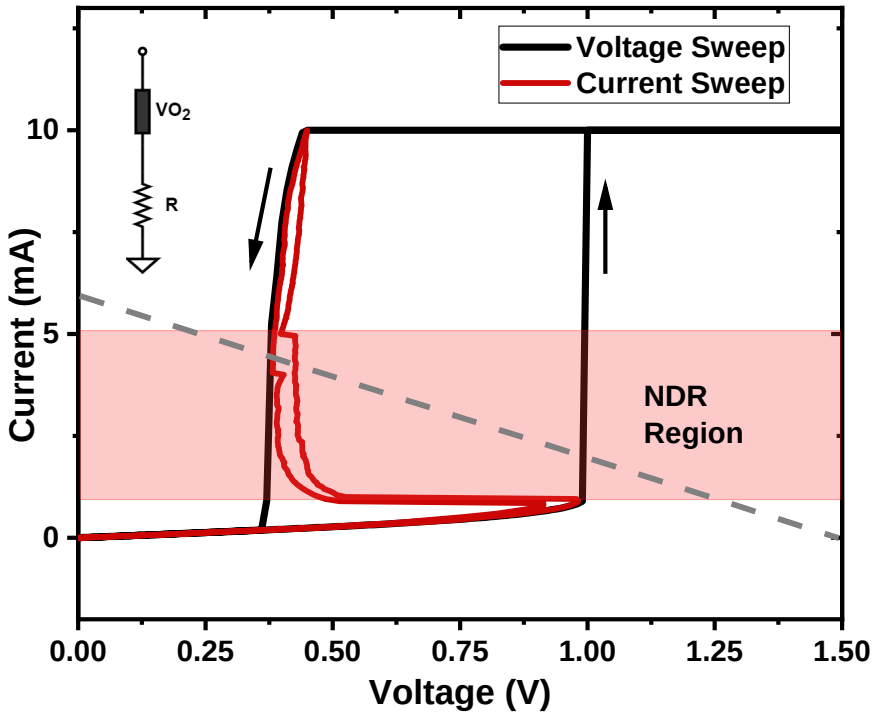


Figure 4.1: VO_2 switching characteristic in the I-V space showing the region of negative differential resistance, along with the load line of an arbitrarily-valued resistor in series.

between a VO_2 element and a resistor, defined by the two intersection points marked A and B on the figure. In order to access the oscillatory behavior, **both** operating points need to be found within the NDR region. This essentially means that the load line needs to intersect the VO_2 characteristic in its transition regions, where there is no stable operating point. If this condition is met, the circuit behaves like an astable multivibrator as it is constantly switching from one unstable operating point to the other.

As we will see in the next section, the characteristics of the loading element contribute to determining the running frequency of such an oscillator. As such, it is important to mention that the slope of the load line (the electrical resistance of the load element) is constrained in two places. First, the intersection with the X axis (in this case, the horizontal line denoting zero current) happens at exactly $V = V_S$ - the supply voltage of the series circuit. Second, the intersection with the Y axis (vertical line at zero voltage) takes place at $I = V_S/R$. It becomes apparent that at a given supply voltage, there is a limited range of resistance values that satisfy the condition set forth earlier with respect to operating point, and this impacts the frequency tuning

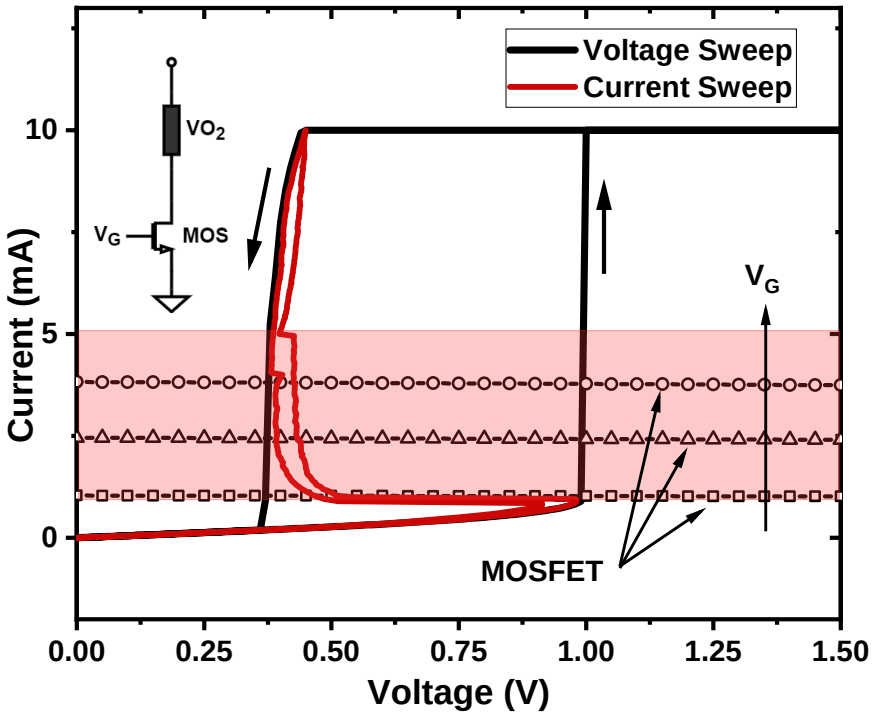


Figure 4.2: VO_2 switching characteristic in the I-V space showing the region of negative differential resistance, along with the load line of a series connected n-type MOSFET

range detrimentally. The ideal case that would theoretically ensure maximum range of intersection excursion within the NDR region would be an infinitely large resistor, and the circuit to be biased at an infinitely large supply voltage, essentially producing a perfectly horizontal load line at an arbitrarily high current level. This is of course impractical.

Luckily, by replacing the passive load resistor with an active element, such as an n-type MOSFET, we can optimize the crossing points such that they are distributed on an as close to a horizontal line as possible, while also having opened the way towards controlling and tuning precisely the intersection level by means of operating its gate voltage V_G. In figure 4.2 we present the superimposed MOSFET characteristic as a load line, on top of the VO_2 element curves to highlight this fact. It should be mentioned, however, that the slope of the MOSFET load line, although appearing relatively flat, is actually limited by the transistor's output conductance, which cannot be perfectly zero. Moreover, the operating regime of the MOSFET that enables such an operation is the saturation regime, where the transistor's drain voltage V_{DS} is substantially higher than $V_{GS} - V_T$. This means that a combination between the switching threshold values of the VO_2 element and the full characteristic of the MOSFET and its "start of saturation" point will dictate the minimum supply voltage of such a circuit. The full picture can be seen in figure 4.3, and it shows a VO_2 element with an IMT threshold of approximately

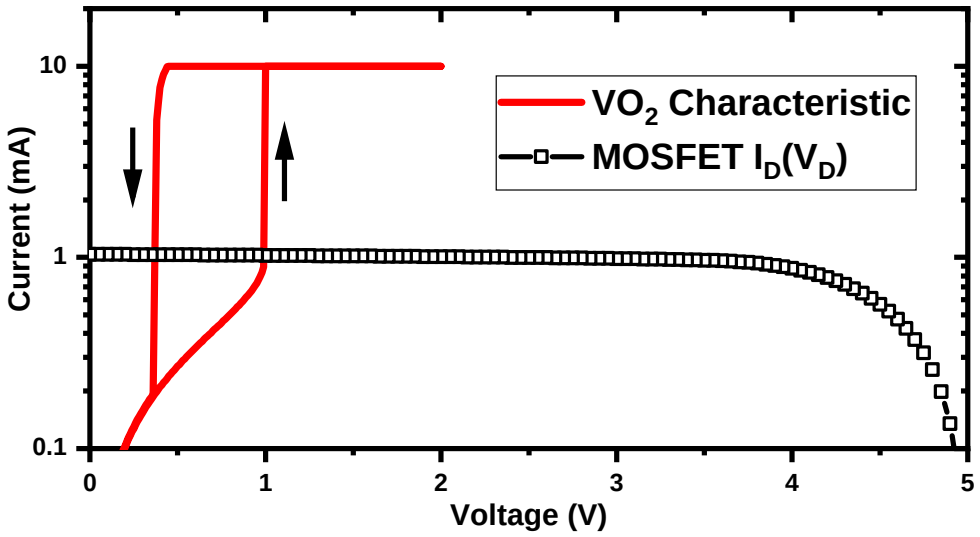


Figure 4.3: VO_2 switching characteristic in the I-V space and the complete MOSFET load line, at a supply voltage of $V_S = 5V$ and gate voltage $V_G = 2.5V$

1V, and the circuit is supplied at 5V. The MOSFET is working deep in saturation where it exhibits minimum - but not zero - output conductance.

4.2.2 Dynamic analysis

The complete circuit of the spiking oscillator can be seen in figure 4.4(a). It shows that the VO_2 element R is loaded to a parallel connection between a MOSFET channel and a load capacitance C. The circuit is supplied with a DC voltage V_S and the MOS transistor is biased by an external DC voltage V_G. Finally, the time dependent output voltage of the oscillator is read at the series connection node and is depicted here by the potential $v_O(t)$ along with a qualitative depiction of the time evolution of the output signal which, as we will demonstrate further, can be approximated by a sawtooth waveform shape.

In order to describe the time evolution of the output voltage - oscillating between the two possible operating points mentioned earlier, we need to perform the circuit analysis taking into account the parallel load capacitance C. Moreover, it is useful to represent the MOSFET using a variation of its small signal model. We previously mentioned that the transistor is biased such that it operates in saturation and so in this case it can be regarded as a constant DC current source. Granted, the traditional small signal model of the MOSFET contains a *Voltage Controlled Current Source* described

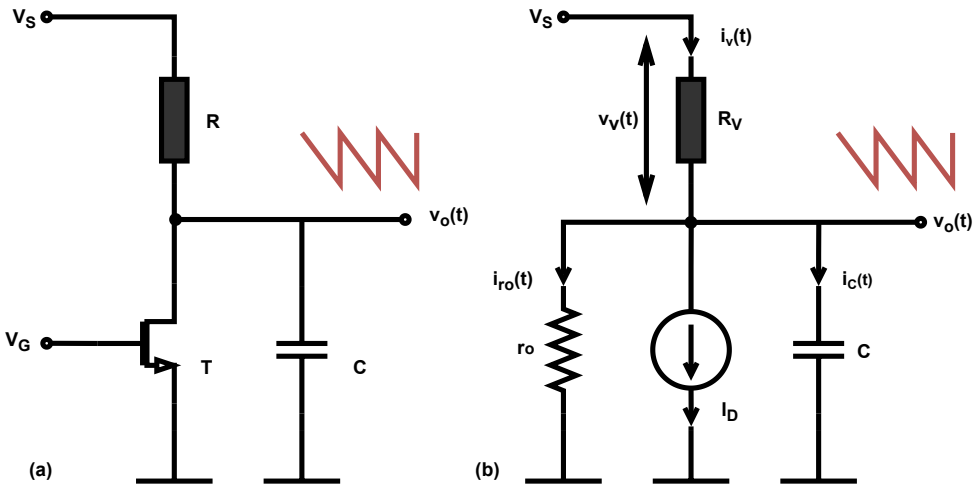


Figure 4.4: (a) - Schematic of the VO_2 voltage controlled spiking oscillator alongside (b) - its small signal equivalent circuit

as $i_D = g_m v_{GS}$ but since in this case V_{GS} is treated as a constant, so can the drain current be approximated as being constant. In order to complete the picture, the finite output resistance of the MOSFET is modeled using a resistor r_o placed in parallel with the ideal constant current source I_D. Finally, the schematic shown in figure 4.4(b) contains all the linear elements along with all their parameters required to describe the dynamics of the output voltage.

A general equation that governs the behavior of the circuit shown in figure 4.4(b) can be written as follows:

$$V_S = R_V \cdot \left(i_{r_o}(t) + I_D + i_C(t)\right) + v_o(t) \tag{4.1}$$

Where V_S is the supply voltage, R_V is the electrical resistance of the VO_2 element (assumed constant, for now), and $v_O(t)$ is the time-dependent output voltage. The currents flowing through all the elements are time-dependent, in this case, with the exception of the MOSFET drain current I_D which is constant due to biasing at a fixed gate voltage V_G. From equation 4.1 we can further expand the term $v_O(t)$, since it represents the voltage drop across capacitor C, therefore $v_o(t) = \frac{1}{C}\int_{t_0}^{t_1} i_C(t)dt$. We can rewrite equation 4.1 as follows:

$$V_S - I_D R_V = R_V i_C(t) + \alpha \cdot \frac{1}{C}\int_{t_0}^{t_1} i_C(t)dt \tag{4.2}$$

The term α in the above equation is defined as $\alpha = 1 + \frac{R_V}{r_o}$ and represents the contribution of the MOSFET output resistance to the circuit's time constant. In addition, the integration limits t_0 and t_1 define an arbitrary time interval over which the equation holds. In order to solve the equation, we need to put it in differential form. By taking the derivative of both sides we can eliminate the time-invariant terms V_S and $I_D R_V$. This also eliminates the integral term along with the unknown integration limits, putting the equation in a much simpler form, as follows:

$$\frac{R_V C}{\alpha}\frac{di_C(t)}{i_C(t)} = -dt \tag{4.3}$$

The formulation above is a simple 1st order Ordinary Differential Equation (ODE) that can be solved by integration on both sides. If we furthermore condense the term containing α, R_V and C into a single term $\tau = \frac{R_V C}{\alpha}$, we obtain the general solution for variable $i_C(t)$:

$$i_C(t) = e^{-\frac{t}{\tau}} \cdot i_C(t=0) \tag{4.4}$$

Finally, by rewriting $i_C(t)$ and $i_C(t=0)$ in terms of $v_o(t)$ and $v_o(t=0)$ respectively using equation 4.1, we obtain the general solution for the time evolution of the output voltage as a function of all the circuit parameters, as follows:

$$v_o(t)\left(1+\frac{R_V}{r_o}\right) = V_S - R_V \cdot \left[I_D + e^{-\frac{t}{\tau}} \cdot \left(\frac{V_S}{R_V} - I_D - v_o(t=0)\left(\frac{1}{R_V}+\frac{1}{r_o}\right)\right)\right] \tag{4.5}$$

In order to arrive at the expression for frequency of oscillation, we must isolate the time variable t and express it as a function of $v_o(t)$ and $v_o(t=0)$. This can be done by rearranging 4.5 and isolating the term $e^{-\frac{t}{\tau}}$, followed by applying the natural logarithm of both sides, yielding:

$$t = -\frac{R_V C}{\alpha} ln\left[\frac{V_S - I_D R_V - v_o(t)\alpha}{V_S - I_D R_V - v_o(t=0)\alpha}\right] \tag{4.6}$$

Equation 4.6 essentially gives the time needed for the output voltage v_o to evolve from an arbitrary value $v_o(t=0)$ to another value $v_o(t)$. It is now important to impose appropriate boundary conditions in order to obtain an exact solution. First, we must focus towards the electrical resistance of the VO_2 element. As the voltage across its terminals rises to the IMT threshold, its electrical resistance changes from a high value (R_{OFF}, in the insulating state) to a lower value (R_{ON}, in the metallic state). Conversely, as the voltage across its terminal decreases, the transition takes place in reverse (from R_{ON} to R_{OFF}) at the lower, MIT voltage threshold. The evolution of the circuit under the two different values of VO_2 resistance gives rise to two distinct relaxation cycles in the oscillator waveform, as depicted in figure 4.5, for which equation 4.6 holds

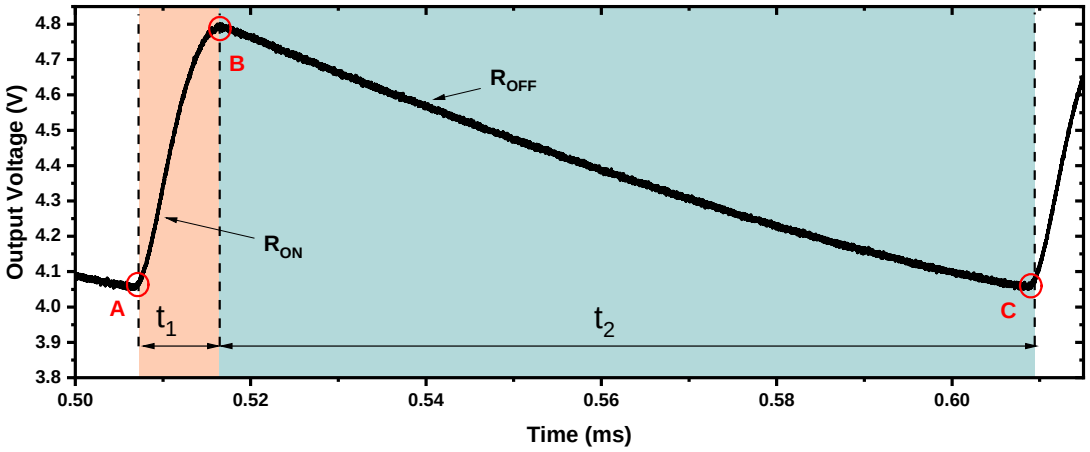


Figure 4.5: One oscillation period, revealing the exponential transitions between points A, B and C that define the limits of the linear charge and discharge regimes, and the associated charging and discharging times t_1 and t_2

respectively, albeit with different sets of parameters. In addition, since parameter α depends on the value of R_V, we will deal with the corresponding terms $\alpha_{ON} = 1 + \frac{R_{ON}}{r_o}$ and $\alpha_{OFF} = 1 + \frac{R_{OFF}}{r_o}$ for the two distinct regimes, respectively.

Firstly, we can consider the case when the output capacitor is charging, accompanied by a rise in the output voltage. In this regime, highlighted in red in figure 4.5, the VO_2 element is found in its low-resistance state, therefore we can consider that $R_V = R_{ON}$. In addition, we can observe that point A marks an IMT event, which tells us that the voltage drop across the VO_2 element equals its IMT threshold voltage. For the charging regime, we can therefore consider that $v_o(t=0) = V_S - V_{IMT}$. Similarly, in point B we expect an MIT event, that happens at $v_o(t) = V_S - V_{MIT}$ after a time t_1. Using this parameter set we can write the expression for t_1, as follows:

$$t_1 = -\frac{R_{ON}C}{\alpha_{ON}} ln\left[\frac{V_S - I_D R_{ON} - (V_S - V_{MIT})\alpha_{ON}}{V_S - I_D R_{ON} - (V_S - V_{IMT})\alpha_{ON}}\right] \tag{4.7}$$

Similarly, when the VO_2 element is found in its high-resistance state, this corresponds to the blue regime highlighted in figure 4.5, and $R_V = R_{OFF}$. In the discharge regime, time $t = 0$ corresponds to point B, therefore we can write $v_o(t=0) = V_S - V_{MIT}$ since we expect an MIT event, and finally $v_o(t) = V_S - V_{IMT}$ corresponding to point C on the evolution of the output voltage. The equation for the time spent in the discharge

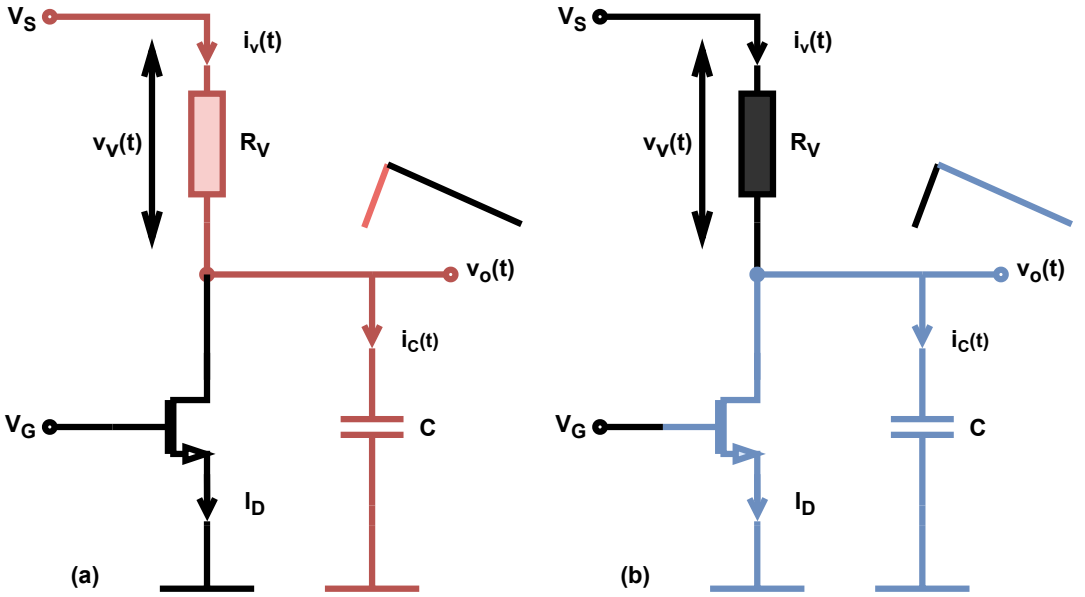


Figure 4.6: Description of the "least resistance path" when (a) the VO_2 element is found in metallic state ($R_V = R_{ON}$) and (b) when it is showing insulating behavior ($R_V = R_{OFF}$)

regime t_2 can be written as:

$$t_2 = -\frac{R_{OFF}C}{\alpha_{OFF}} ln\left[\frac{V_S - I_D R_{OFF} - (V_S - V_{IMT})\alpha_{OFF}}{V_S - I_D R_{OFF} - (V_S - V_{MIT})\alpha_{OFF}}\right] \tag{4.8}$$

In figure 4.6 we present a qualitative description of the two regimes, and highlight the "least resistance path" in both cases. In the charging regime, the VO_2 element is in a low-resistance state, therefore causing charging of the load capacitance (a). Conversely, after the MIT event at point B, the VO_2 element becomes highly resistive, and the least resistance path provided by the current source I_D determines the discharge of the load capacitor. Earlier in section 4.2.1 we mentioned that one of the advantages of using a MOSFET operated in saturation was that it exhibited relatively large output conductance ensuring its operation as a constant current source. Working under the assumption that the MOSFET's r_o is significantly larger than the resistance of the VO_2 element, which is a sensible approximation, as we will later notice, the formulation of the oscillator frequency can be simplified. The term $\alpha = 1 + \frac{R_V}{r_o}$ can be approximated as close to unity, since it is inversely proportional to the large value of r_o, and therefore can be eliminated from the formulations of t_1 and t_2, respectively. Finally, for

completeness, we can express the free-running frequency of the spiking oscillator in closed form by computing the reciprocal of the oscillation period, represented by $T = t_1 + t_2$, as

$$F = \frac{1}{T} = \frac{1}{-R_{ON}Cln\left[\frac{V_{MIT}-R_{ON}I_D}{V_{IMT}-R_{ON}I_D}\right] - R_{OFF}Cln\left[\frac{V_{IMT}-R_{OFF}I_D}{V_{MIT}-R_{OFF}I_D}\right]} \tag{4.9}$$

From 4.9 it can be observed that the oscillator frequency can be tuned by adjusting the biasing current I_D between the bounds set by the NDR region. As a consequence, the proposed oscillator is a current-controlled oscillator. Furthermore, by exploiting the fact that the drain current of the MOSFET is directly dependent on the gate voltage V_G, the circuit's tunability is extended to the voltage domain, ultimately making this circuit a voltage-controlled oscillator (VCO). Typical waveforms produced by our VO_2 VCOs approach a sawtooth shape with variable frequency an minimal changes in amplitude, as we show in figure 4.7. The red curve in the figure corresponds to a tuning voltage $V_G = 3V$ while the red curve represents the case when $V_G = 5V$, yielding waveforms with a frequency of 8.45 kHz and 25.7 kHz, respectively.

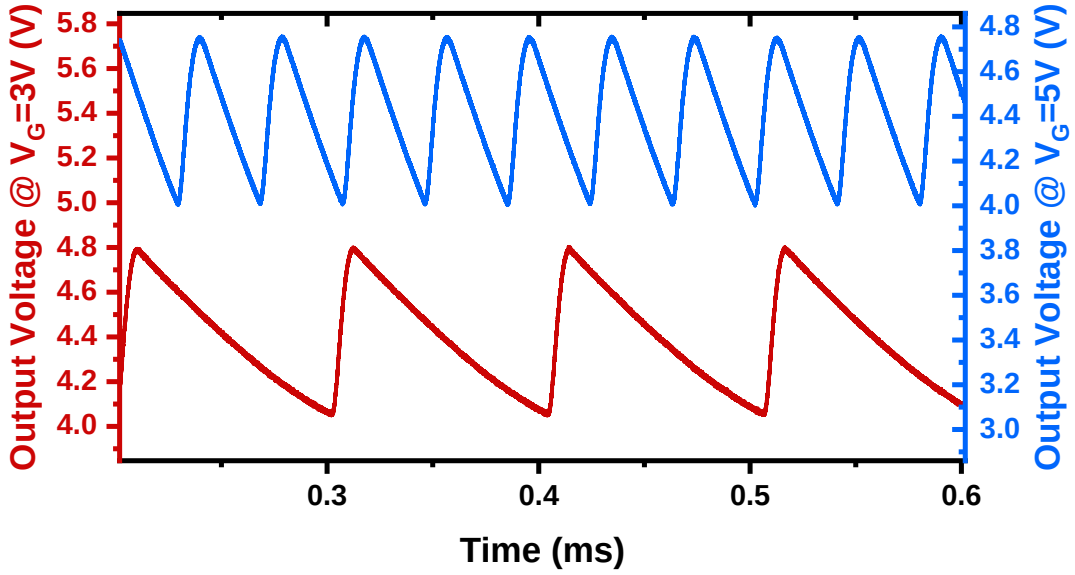


Figure 4.7: Oscilloscope capture of the VCO output voltage under two distinct control voltages: $V_G = 3V$ and $V_G = 5V$

4.2.3 Oscillation condition and tuning range

It can be noticed that the formulations for the charge and discharge time t_1 and t_2 depend on the value of the logarithm being negative, in order to produce realistic, positive time values. In other words, the argument of the natural logarithm in equations 4.7 and 4.8 must be smaller than 1, but positive, otherwise the logarithm would produce complex valued results. Solving the implied inequalities will produce the following constraints:

$$\frac{V_{IMT}}{R_{OFF}} < I_D < \frac{V_{MIT}}{R_{ON}} \tag{4.10}$$

The inequality 4.10 is synonymous to the biasing conditions presented earlier in section 4.2.1 and it defines the range of MOSFET current I_D that intersects the VO_2 characteristic within the negative differential resistance region, allowing for sustained oscillations.

Intuitively, one could say that the lower bound of the permissible current range

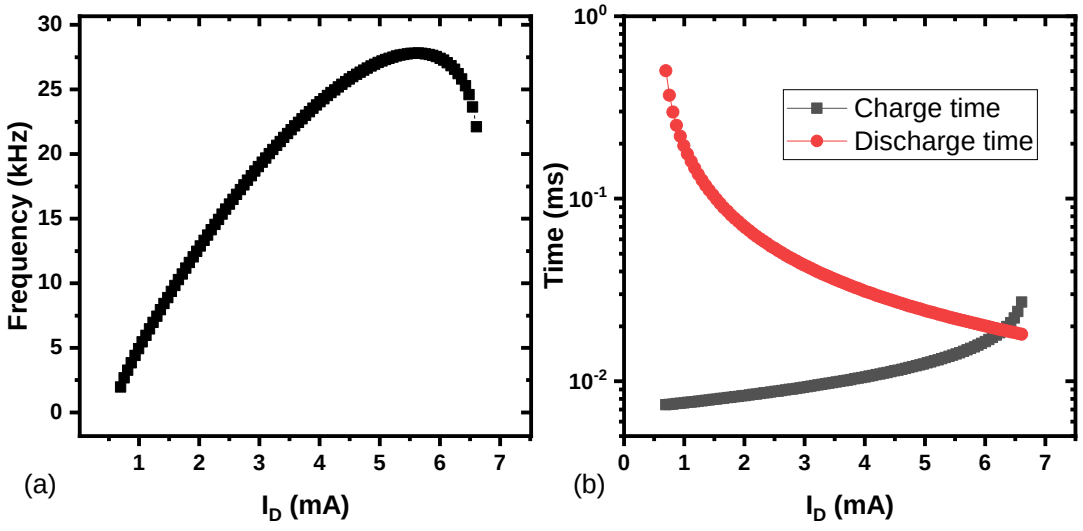


Figure 4.8: (a) - The frequency range of the spiking oscillator, within the bounds set by equation 4.10 showing a sudden decrease at high bias currents; (b) - Simulation of the relaxation periods across the tuning range, crossing at maximum frequency and causing decrease of frequency at high current levels

corresponds to the lowest achievable oscillation frequency and that the highest current produces the highest frequency. That is, however, not correct. As we show in figure 4.8(left), the frequency/current characteristic is nonlinear and non-monotonic, as it reaches maximum value at a current lower than the upper bound of V_{MIT}/R_{ON}. This is due to the fact that at high values of I_D, the charging time becomes comparable and even exceeds the discharge time of the capacitor, causing a decrease in frequency as the current is increased. This phenomenon and the crossing point can be observed in figure 4.8(right) occurring at values close to the upper bound of the interval described in equation 4.10.

In order to identify the exact value of I_D where maximum frequency is reached, we need to find the minimum period T as a function of I_D by taking its derivative and equating it to 0, and then extracting the corresponding value for I_D, as follows:

$$I_{D,Fmax} = \frac{V_{IMT} \cdot V_{MIT} \cdot \left(\frac{R_{OFF}}{R_{ON}} - \frac{R_{ON}}{R_{OFF}}\right)}{(V_{IMT} + V_{MIT}) \cdot (R_{OFF} - R_{ON})} \tag{4.11}$$

The set of circuit parameters used to produce the data shown in figure 4.8 corresponds to the measured characteristics of the VO_2 element discussed in the static analysis at the beginning of this chapter, and was published in [167]. According to the model presented above, the maximum frequency corresponding to the peak of the curve shown in 4.8 is 27.8 kHz, while the minimum value, corresponding to the lower bound of the current range, is 1.96 kHz. This corresponds to a theoretical maximum tuning range of more than 1400% if measured from the lowest frequency, or more than ±200% if measured from the center frequency at 12.92 kHz.

4.3 Experimental validation of the analytical model

In order to measure the VCO circuit and validate the model presented above, we have built the measurement setup shown in fig 4.9. The VO_2 two-terminal device was contacted via probing needles using a Cascade Summit 2000 wafer probing station, while the MOSFET and the load capacitance have been implemented on a printed circuit board equipped with Triax/BNC connections towards the probing station and the biasing/readout equipment. Biasing the circuit is done using two laboratory DC power

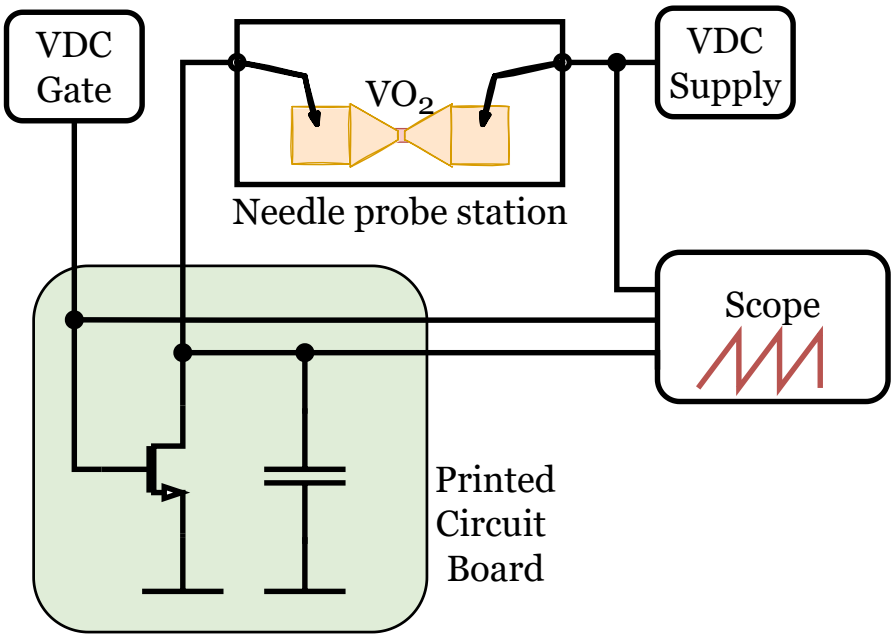


Figure 4.9: Oscillator measurement setup, outlining the connections between the biasing supplies, the oscilloscope, the printed circuit board and the needle probing station used for contacting VO_2 devices

supplies to provide the supply V_S and MOSFET gate V_G voltages, respectively. Finally, the oscillator output voltage is interpreted and recorded using a Rohde&Schwarz RTB2004 Oscilloscope that is simultaneously monitoring the supply and gate voltages applied to the oscillator. Although not shown here explicitly, the measurement setup permits connection to a Keithley 4200A-SCS Semiconductor Parameter Analyzer which is used to measure the I-V and V-I characteristics of the VO_2 element using Source-Measurement Units (SMUs).

The VO_2 devices used for the oscillator experiment were fabricated using standard lithography techniques and originate from two different fabrication batches that

Table 4.1: PLD recipes used for samples A and B

Recipe parameter	Sample A	Sample B
Laser repetition rate [Hz]	20	5
Laser energy [mJ]	400	500
Oxygen partial pressure [mbar]	0.01	0.02
Oxygen flow [sccm]	2	20
Temperature [C]	400	450

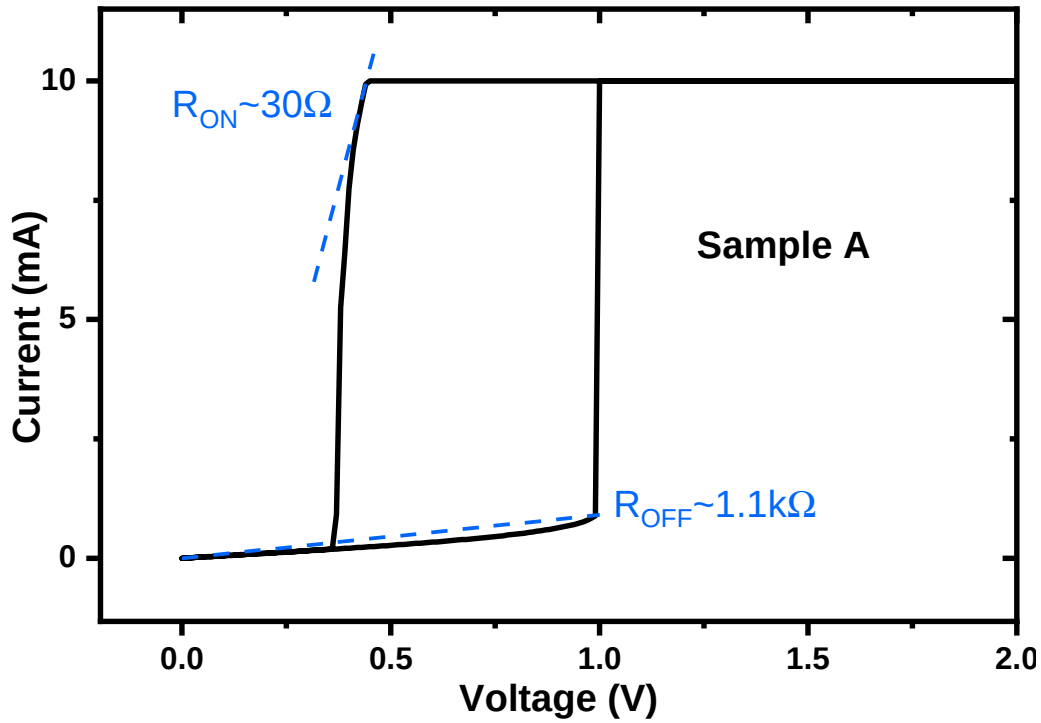


Figure 4.10: I-V Measurement used to extract the device parameters of Sample A

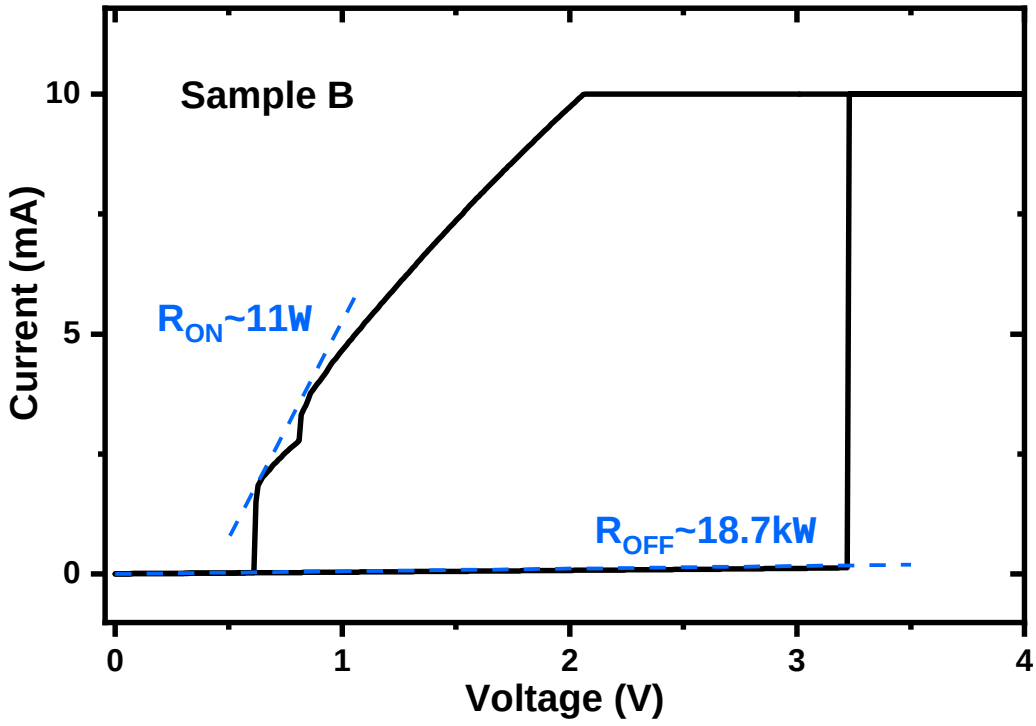


Figure 4.11: I-V Measurement used to extract the device parameters of Sample B

exhibit distinct particularities. The VO_2 thin films employed were deposited using Pulsed Laser Deposition (PLD) in both batches but using different deposition recipes, as outlined in table 4.1. As a consequence, the resulting devices, which we will call from now on "Sample A" and "Sample B" show very different properties in terms of on- and off-state resistance and phase transition thresholds. In order to asses the properties of Samples A and B we performed I-V characteristic measurements using the semiconductor parameter analyzer and were able to extract the following device parameters:

Sample A: This device exhibits an insulator-to-metal transition at approximately 0.95V while the metal-to-insulator transition takes place at close to 0.4V, according to figure 4.10. In addition, we measured the on-state resistance at approximately $R_{ON} = 30\Omega$ by estimating the slope of the I-V curve right before the MIT region. It is important to note that, even though the measurements have been carried out using a current compliance limit of 10mA (in order to protect the device), we are still able to capture the end of the high resistance regime and estimate R_{ON}. Static off-state resistance at the border of the NDR regime can be estimated by the ratio between V_{IMT} and I_{IMT} and in the case of Sample A is found as $R_{OFF} = 1.1k\Omega$.

Sample B: Similarly, in the case of Sample B we find the IMT threshold at $V_{IMT} = 3.15V$ while the MIT threshold is $V_{MIT} = 0.62V$ (figure 4.11), giving rise to a much larger voltage hysteresis window, which translates into a higher oscillation amplitude. The on-state resistance is estimated similarly to sample A and has a value $R_{ON} = 11k\Omega$, while the off-state resistance was measured at $R_{OFF} = 18.7k\Omega$.

In both experiments the supply voltage was kept at 5V in order to ensure saturation of

Table 4.2: Model parameters for samples A and B

Parameter	Sample A	Sample B
V_{IMT} [V]	0.95	3.15
V_{MIT} [V]	0.4 / 0.2	0.62
R_{ON} [Ω]	30	11
R_{OFF} [$k\Omega$]	1.1	18.7
Load Capacitance C [nF]	150	47

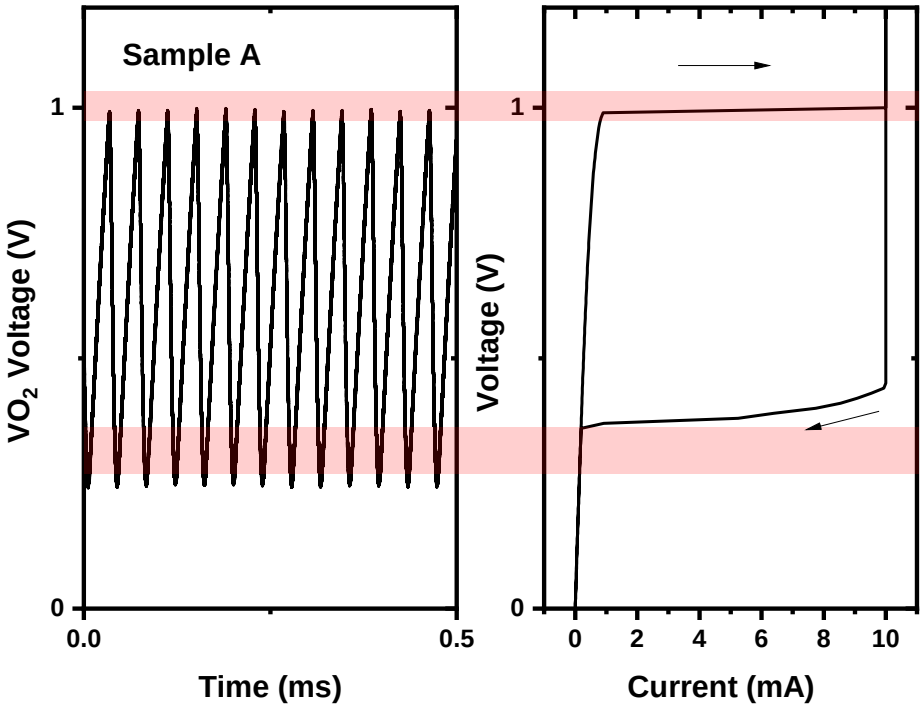


Figure 4.12: Right - The I-V characteristic of Sample A rotated such that the voltage axis is aligned with Left - the voltage drop across Sample A during oscillation

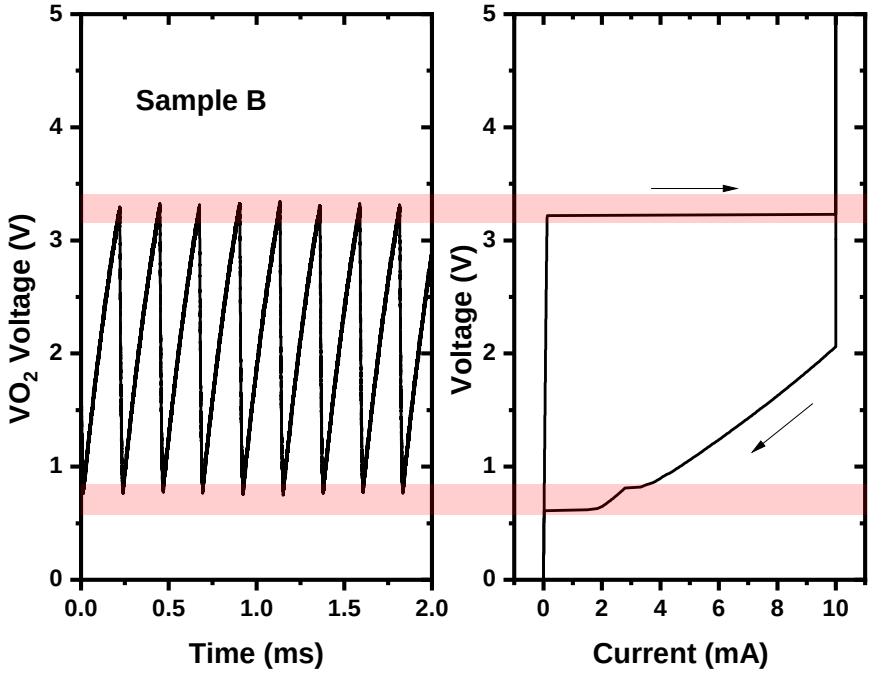


Figure 4.13: Right - The I-V characteristic of Sample B rotated such that the voltage axis is aligned with Left - the voltage drop across Sample B during oscillation

the MOSFET output characteristic. We should mention that, even though the V_{IMT} of sample B is much higher than that of sample A - bringing the drain voltage of the MOSFET lower during operation, the transistor is still safe from being driven in the triode region. Finally, we summarize the measured device parameters in table 4.2 and will use them further on for evaluating the analytical model, with the exception of Sample A's V_{MIT}, which we will amend in the next paragraph.

In figure 4.12 we represent the relationship between the oscillation amplitude and the IMT/MIT switching thresholds of Sample A. According to the analytical model, the oscillation amplitude is directly dictated by the switching thresholds, as the evolution of the operating point is confined within the NDR region. While the IMT threshold of Sample A is in good agreement with the peak level of the output waveform, the same cannot be said about the MIT threshold. The difference may arise from measurement errors but is most probably a consequence of material properties that have been impacted differently by single measurement versus multiple rapid switching cycles as is the case of the oscillator running for prolonged times. For subsequent calculations involving Sample A, we will use the V_{MIT} value associated to the lower peaks of the oscillation waveforms, which corresponds to $V_{MIT} = 0.2V$. On the other hand, sample B performs much better in this regard, as shown in figure 4.13. We notice that both top and bottom peaks align to a greater extent to the voltage levels given by V_{IMT} and V_{MIT}, confirming their interdependence implied by the analytical model.

In figures 4.14 and 4.15 we present a direct comparison between the analytical prediction of oscillator frequency with respect to the control voltage V_G for Sample A and B, respectively. The model shows good agreement with experimental data for both devices using the device parameters estimated from the I-V characteristics. It is worth to point out, however, that Sample B shows a more pronounced deviation from the theoretical prediction and can be attributed to higher variability of the MIT and IMT thresholds when the device changes state from cycle to cycle, which impacts the frequency stability in a negative way. In addition, fitting the model curve to experimental data can be iterated and performed in conjunction with device parameter extraction, in order to yield a more accurate set of parameters that better reflects the circuit behavior. Such an iteration has been performed for Sample A, which results in a set of parameters that agree better with experimental observations both in terms of static device characteristics (figure 4.10), frequency estimation (4.14) and waveform matching (4.16).

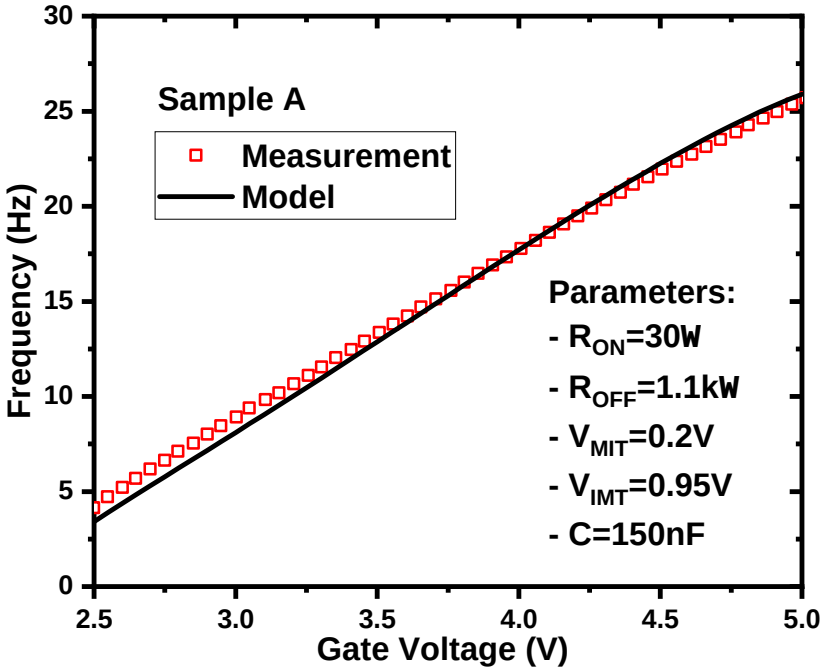


Figure 4.14: Comparison of the analytical prediction of oscillator frequency with respect to experimental data gathered using Sample A. Model parameters in inset

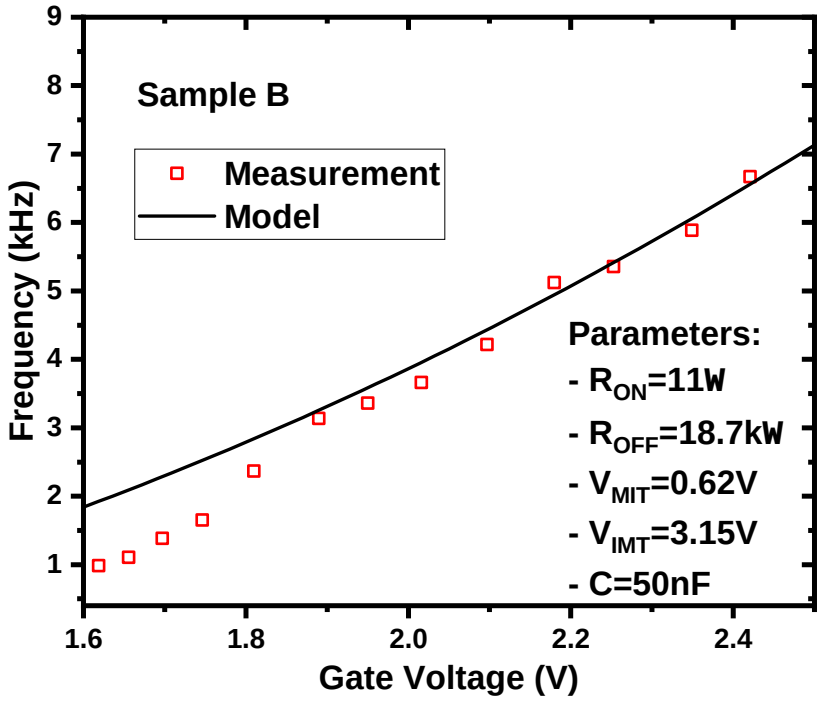


Figure 4.15: Comparison of the analytical prediction of oscillator frequency with respect to experimental data gathered using Sample B. Model parameters in inset

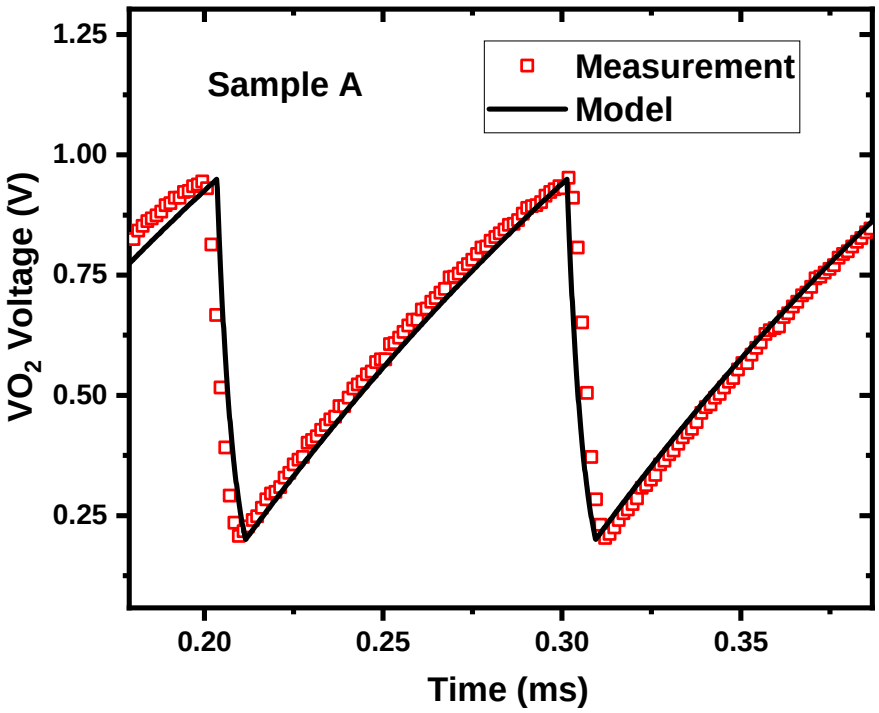


Figure 4.16: Time-domain representation of the modeled oscillator output superimposed over the experimental waveform capture - Sample A

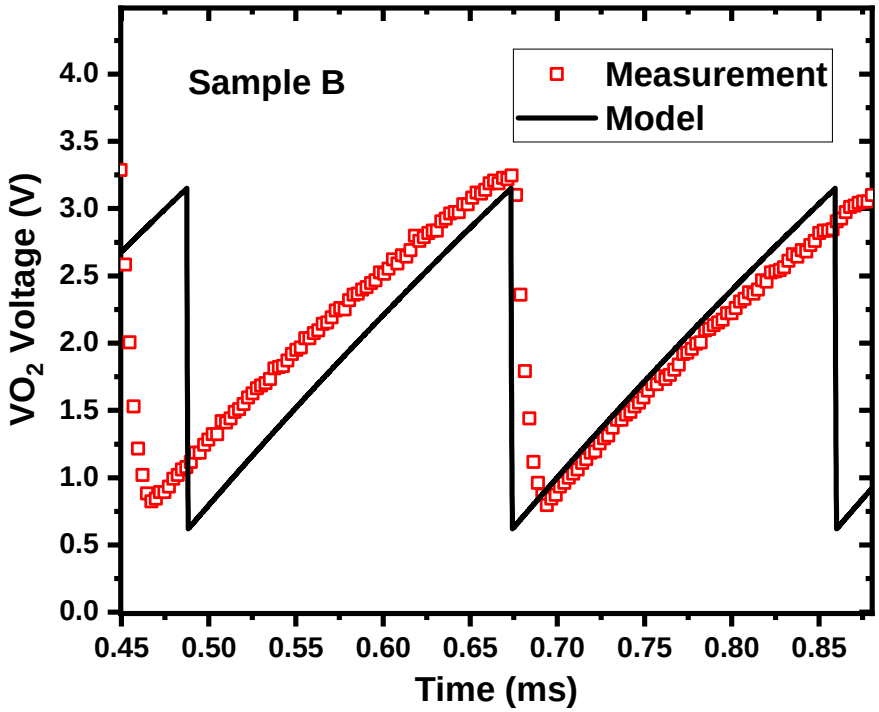


Figure 4.17: Time-domain representation of the modeled oscillator output superimposed over the experimental waveform capture - Sample B

The analytical model can also be used to simulate the time-domain evolution of the spiking oscillator signal based on extracted device parameters, as depicted in figures 4.16 and 4.17, which show a direct comparison between calculated and measured waveforms for both samples. As mentioned above, the parameter set associated to Sample A allows for more accurate tracking of the output waveform when compared to Sample B due to multiple iterations having been performed in order to adjust the parameters for better agreement with all measurements simultaneously.

4.3.1 Frequency dependence on device and circuit parameters

In order to assess the impact of device and circuit parameters on oscillator frequency we used the analytical model to calculate the individual contribution of each parameter. To start, we used the parameter set of sample A and then varied each parameter individually in order to estimate the sensitivity. The results we have obtained are presented in figure 4.18, for a fixed control voltage $V_G = 3V$. The parameters are varied in ranges that contain the nominal values of one or both of the samples we studied, and have been chosen as follows:

- R_{ON}: from 10Ω to 100Ω
- R_{OFF}: from 1kΩ to 20kΩ
- Load capacitance C: from 10nF to 200nF
- Hysteresis window width $V_{IMT} - V_{MIT}$: from 0.55V to 0.8V

Our result shows that the impact of R_{ON} is limited, with an extracted frequency sensitivity of -3.6Hz/Ω. This is attributed to the fact that the on-resistance of the VO_2 element contributes only to the charging time of the output capacitor which is comparatively small with respect to discharge time at $V_G = 3V$ due to the high ratio between R_{ON} and R_{OFF}.

Off state resistance, on the other hand, exhibits a more considerable impact on frequency, since its contribution to the oscillation period dominates the discharge regime of the load capacitance. Combined with the fact that R_{OFF} has values in the $k\Omega$ range, this results in a highly nonlinear frequency shift of almost 2 kHZ over the range of R_{OFF} that we investigated.

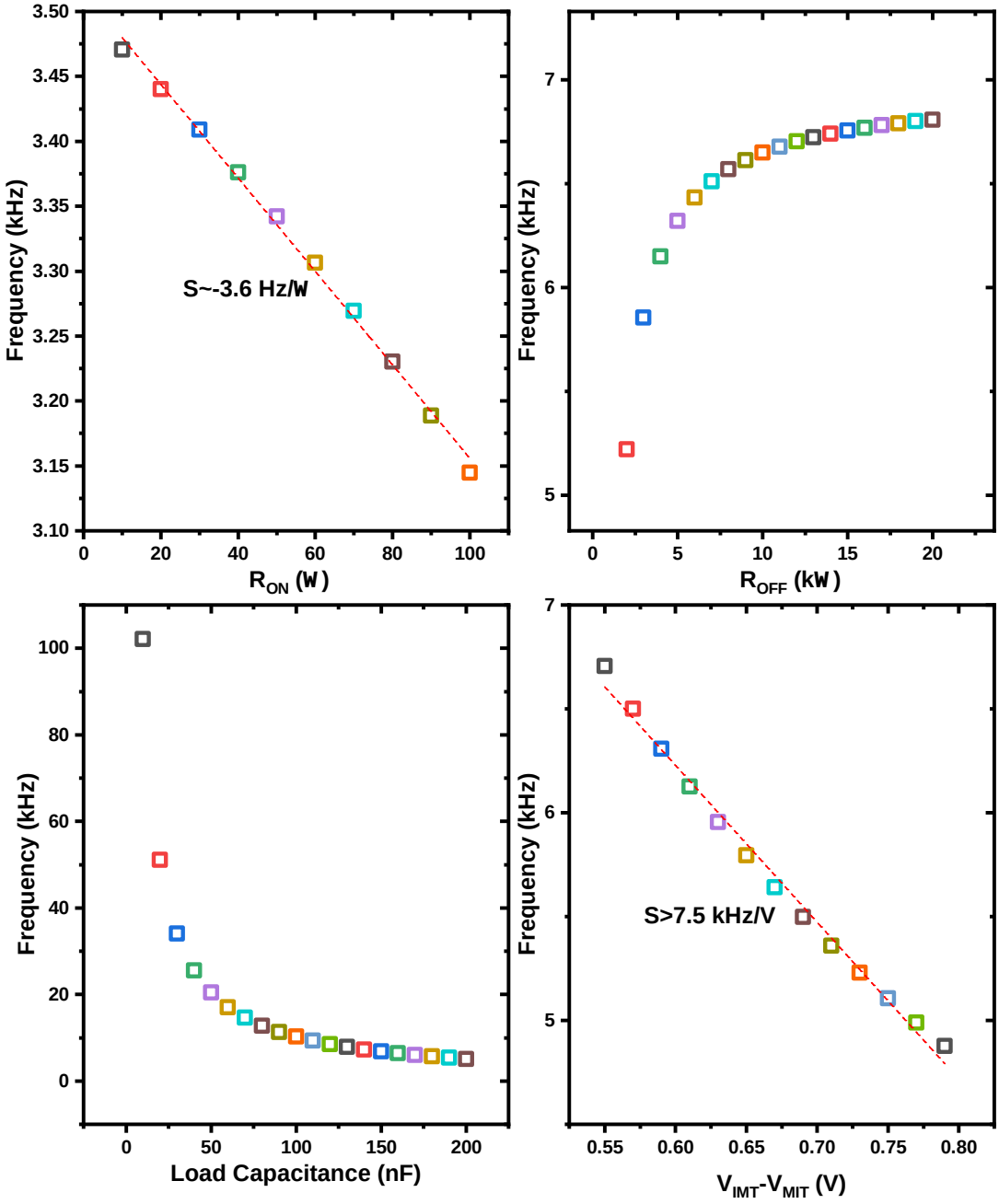


Figure 4.18: Sensitivity of oscillator frequency with respect to device and circuit parameters, in particular R_{ON}, R_{OFF}, load capacitance and VO_2 hysteresis window $V_{IMT} - V_{MIT}$

Load capacitance shows an even more pronounced impact on oscillator frequency, as depicted in figure 4.18(c), because the output capacitance is directly proportional to the oscillation period. The frequency sensitivity follows a $1/x$ relationship with respect to capacitance yielding frequencies approaching the 100 kHz range at very small load capacitance conditions. Indeed, we have experimented with running the VCO without adding the external capacitor, and relying only on the parasitic capacitance of the output node. In such configuration, we measured frequencies exceeding 230kHz using Sample B at $V_G = 2.15V$, suggesting that such spiking oscillators can work at high frequencies using only the input capacitance of subsequent devices (used for signal processing) as load. For example, the circuit could oscillate using only the gate capacitance of another transistor to provide the required load. An oscilloscope capture taken during this experiment is shown in figure 4.19.

Finally, the influence of hysteresis window width is highly correlated to frequency, as illustrated in figure 4.18(d), showing frequency sensitivity greater than 7.5 kHz/V. This is due to the direct impact of V_{IMT} and V_{MIT} thresholds on the oscillation amplitude. Decreasing the amplitude by narrowing the hysteresis window translates into higher

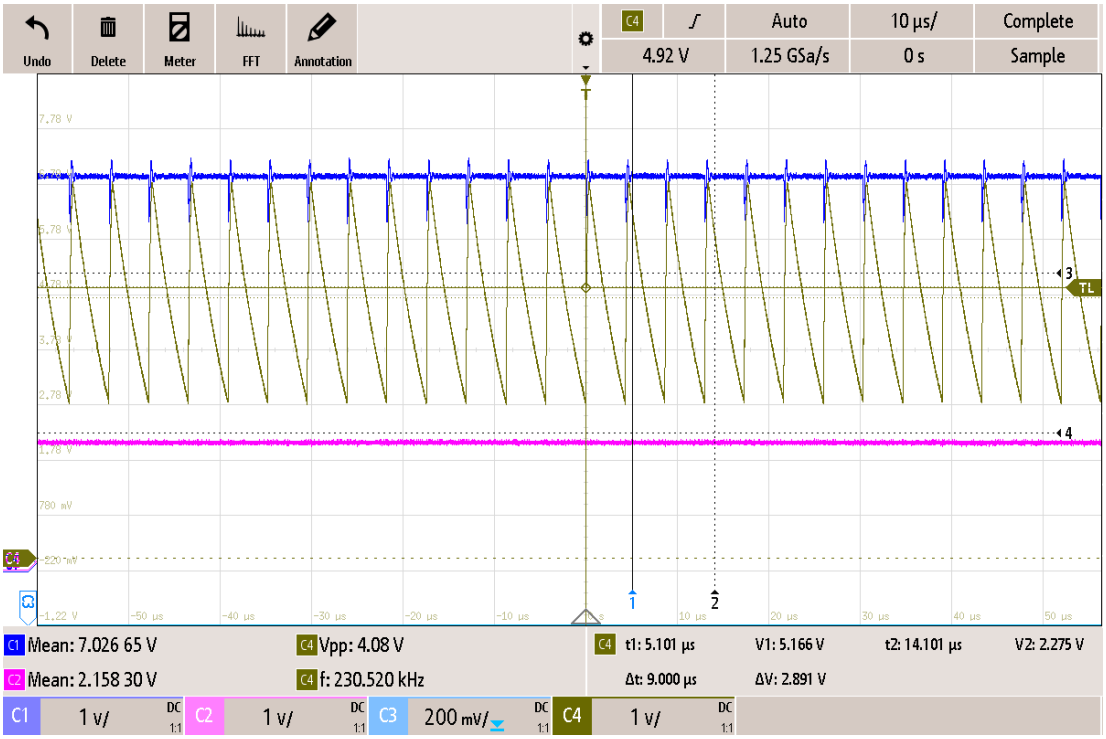


Figure 4.19: Waveform capture of the VCO loaded only by the parasitic capacitance of the output node, showing oscillation frequencies higher than 200 kHz

frequency due to the shortening of the charging and discharging intervals dictated by start- and end- voltage levels. The sensitivity of frequency towards parameters specific to the VO_2 element and the circuit components opens the door towards using such simple spiking oscillators as a sensing platform compatible with several types of sensors and sensitive to a variety of stimuli. For example, the load capacitance can be replaced with any capacitive sensor providing a readout method via the dependence of $F(C)$. Similarly, sensors that output analog voltage levels can be used as biasing elements connected to the MOSFET gate and exploit the sensitivity of frequency with respect to V_G. Finally, the intrinsic properties of VO_2 and their sensitivity to many types of external stimuli [22] can be harnessed and the sensitivity of frequency to hysteresis window width or on/off state resistance can be exploited. Such an application where the VCO is used as a Power-to-Frequency transducer for several bands of electromagnetic radiation - including visible light - is based upon the $F(V_{IMT} - V_{MIT})$ sensitivity and is discussed in more detail in the next chapter.

Observation of stochastic behavior

Static I-V measurements performed over 50 switching cycles in Sample A reveal the presence of random variations in the insulator-to-metal threshold voltage V_{IMT}, as shown in figure 4.20. We have investigated the distributions of V_{IMT}, V_{MIT} and the hysteresis width $V_{IMT} - V_{MIT}$, along with the distribution of the spiking oscillator output frequency deviation from the average f_0 depending on bias. The frequency distribution was measured using the cycle-to-cycle oscillation periods over a time-frame of 12 seconds in biasing conditions $V_G = 3V$ and $V_G = 5V$. Interestingly, V_{IMT}, V_{MIT}, and the hysteresis window do not appear to follow the normal distribution, but rather a bimodal distribution, as depicted in figure 4.21(a, b, c), which correspond to V_{IMT}, V_{MIT}, and $V_{IMT} - V_{MIT}$, respectively. This may suggest the influence of two (or more) distinct noise sources that influence the distribution of VO_2 threshold voltages. In addition, although the oscillation frequency is theoretically closely linked to the value of the hysteresis window, the bimodal distributions do not propagate to the output - this is highlighted in figure 4.21(d), which shows that the oscillation frequency is characterized by a single-mode distribution. Although not studied in detail in this work, understanding and modeling the stochastic and noise behavior of the VO_2 spiking oscillators certainly requires further investigation.

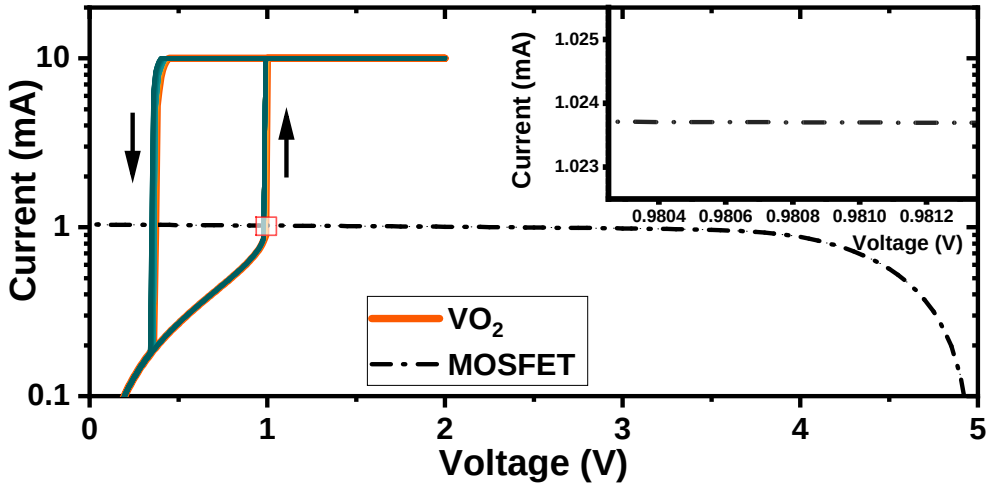


Figure 4.20: VO_2 static characteristic superimposed with the MOSFET loadline (V_G=2.5V) at supply bias of 5V. Inset shows random variation of the switching threshold across 50 switching cycles.

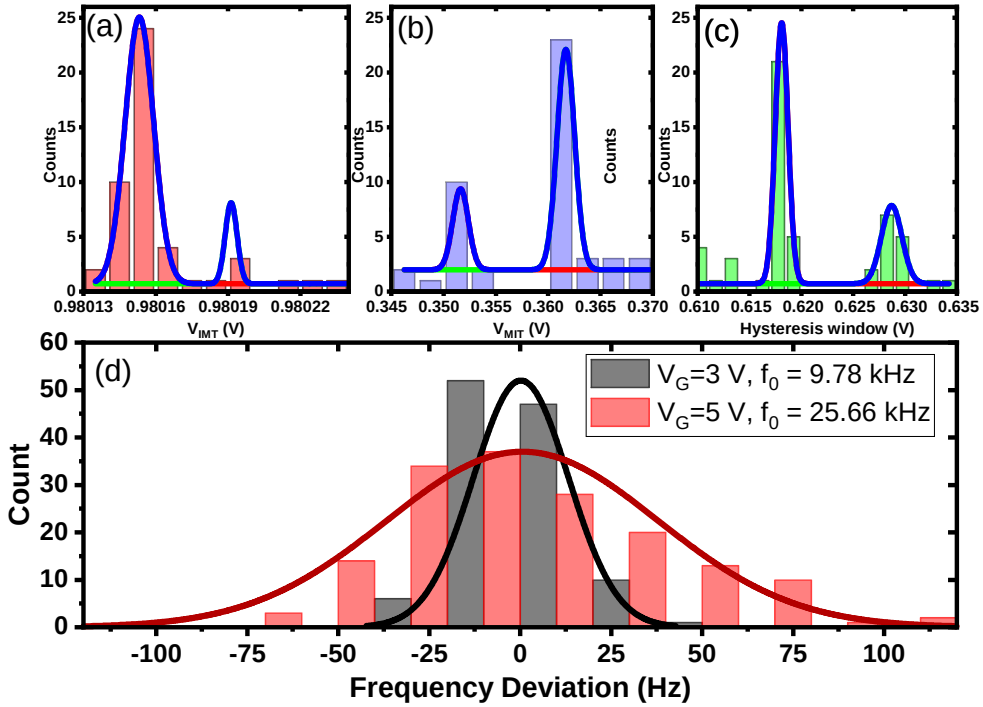


Figure 4.21: Threshold voltage histograms for a - V_{IMT}, b - V_{MIT}, c - hysteresis window; d - histogram showing the distribution of the frequency deviation from the average value at $V_G = 3V$ and $V_G = 5V$.

4.4 Summary

In this chapter we have proposed **the design, implementation and study of a compact 1T-1R Voltage Controlled Spiking Oscillator that exploits the Negative Differential Resistance induced by the reversible metal-to-insulator transition in two-terminal Vanadium Dioxide (VO_2) devices**. The devices used here are based on the VO_2 material fabrication and processes presented in Chapter 3.

The development of such spiking oscillating circuits can help advance the field of VO_2 sensors and neuromorphic applications, in which the majority of such oscillators were originally implemented using fixed resistors in series with 2 terminal VO_2 switches. The use of a MOSFET transistor as a loading element to the VO_2 switches provides promising paths for oscillator output signal tunability (frequency range and amplitude) as well as for fully CMOS integrable schemes of such circuits using functional oxide devices.

Firstly, in section 4.2 we have presented **a circuit analysis of the VCO starting with the importance of DC operating point for the characteristics of the resulting spiking signal**. We showed that the intersection points between the static I-V characteristics of the VO_2 element and the MOSFET define the oscillation amplitude and that the MOSFET characteristic is required to fall within the NDR region of the VO_2 in order to achieve sustained oscillation. The presented dynamic analysis of the VCO includes the derived formulation of oscillator frequency as a function of MOSFET drain current ID as well as the evolution of the output voltage in time $v_O(t)$ based on intrinsic VO_2 device properties and circuit elements. We also provided a more in depth look at the oscillation condition and how it impacts the tuning range, showing that the relationship between frequency and current is highly nonlinear and non-monotonic, exhibiting a frequency peak at current levels close to the upper bound of the NDR region. Using the minimum and maximum frequency values from this study we were able to compute a theoretical tuning range higher than 1400% or more than ±200% if measured from the center frequency range. Moreover, such tuning ranges may be achieved with low voltages that could be scaled below 1V, offering full compatibility with low power CMOS.

Secondly, **we have validated the accuracy of the proposed original analytical model**, based on measurements of the VCO circuit using two case studies based on two VO_2

samples that exhibit considerably different material properties due to different VO_2 deposition parameters and device fabrication process flows, and presented the results in section 4.3. We extracted VO_2 parameters from I-V measurements of the 2-terminal devices and used them as inputs for the analytical model. We then compared the prediction of the model against experimental data and showed good agreement between the two in terms of frequency dependence on applied control voltage and time-domain waveforms of the output signal. This study highlights the importance of the model proposed that includes physical electrical parameters intrinsically connected to material properties and I-V switching characteristics. Therefore, **our model has the capability to further support material-circuit co-optimization studies** that are very useful for both sensor and neuromorphic future applications.

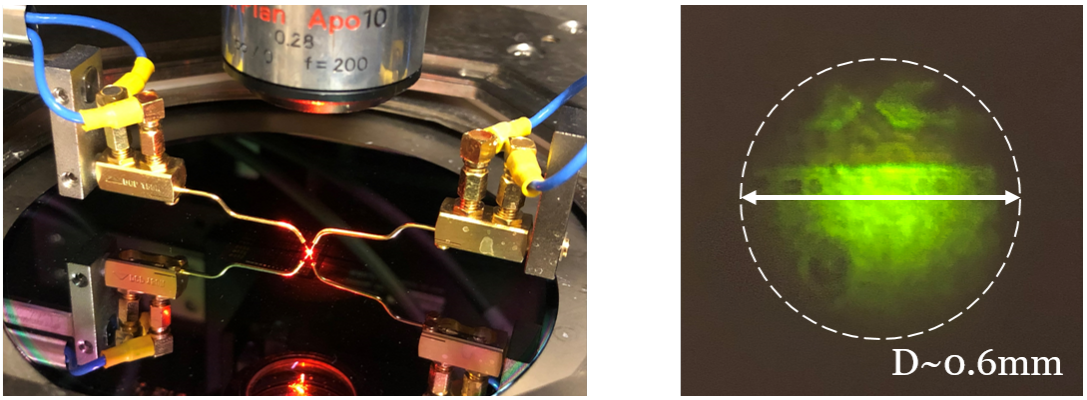
Finally, we investigated the sensitivity of VCO frequency towards individual model parameters, such as on- and off- state resistance, load capacitance and the hysteresis window in the VO_2 static characteristic. We found that **the proposed spiking VCO can be used as a compact sensing platform with integrated readout by exploiting the frequency sensitivity towards control voltage and load capacitance** (thus providing readout options for capacitive or other types of analog sensors) and **hysteresis window width - harnessing the sensitivity of VO2 static switching characteristics towards a wide variety of external stimuli**. Such spiking oscillator vehicles have been used in the work that is reported in chapter 5 and are expected to **form a base for future all-analog spiking information processing in biologically inspired electronic circuits**.

5 VO_2 Oscillators for optical sensing (and beyond)

5.1 Visible light sensing

5.1.1 Methods

The experimental study presented in this section was carried out in order to investigate the effect of visible light radiation on VO_2 electrical switching characteristics and subsequently its impact on the output frequency of the VO_2-based oscillator cell presented in the previous chapter. To this goal, we illuminated the active VO_2 device (integral to the oscillator circuit) by means of a wideband laser source. The laser employed in this study was an NKT Photonics SuperK Extreme supercontinuum white laser that delivers a wide spectral output covering the 400nm - 2400nm range. However, in order to properly assess the effect of visible radiation on switching dynamics and oscillator output frequency in specific wavelength bands, the laser output was fed through an adjustable bandpass optical filter (NKT Photonics SuperK Varia) that was capable of producing 100 nm wide bands centered at visible spectrum wavelengths ranging from 450 nm up to 800 nm in increments of 50nm. Since the filter passband was 100nm wide and distributed at ± 50nm with respect to the selected center frequency, our experiment covered the range between 400nm and 850nm using 8 wavelength bands that overlapped by 50nm. The filtered laser beam was subsequently connected and aligned to the collimating optics of a patch optical fiber. The optical fiber was guided and connected to the sample illumination path of the microscope integral to a Cascade Summit 200 semiconductor probing station, that was used to provide electrical contact to the VO_2 devices (a depiction of the setup is shown in



(a) (b)

Figure 5.1: (a) - The laser focusing setup on the wafer probing station, showing the needle probes used to contact the VO_2 devices and the laser spot focused by the microscope optics on the wafer surface; (b) - Low-resolution photograph of the illuminated device showing a beam diameter of approximately 0.6 mm. The dimension was estimated starting from the known dimensions of the contact pads visible in the picture.

figure 5.1(a)), similar to the measurement setup presented earlier in section 4.3. This optical arrangement was employed in order to obtain optimal focusing of the filtered laser beam in the plane of the VO_2 devices under test.

Using this method, we were able to obtain a focused spot diameter of approximately 0.6mm at the device/wafer level, as shown in figure 5.1(b), and in addition, the X/Y motion stage of the microscope enabled us to precisely focus the spot over the active VO_2 device under test.

It is also important to mention that the optical path starting at the white laser output and ending at device level induces a severe attenuation of the optical power. This is due to unavoidable losses in the bandpass filter, imperfect alignment between the filter output and the optical fiber used for guiding the beam to the probing station, losses due to the optical fiber itself and finally, the attenuation caused by the optical elements (mirrors, lenses) that are used in the optical column of the microscope itself, and so a set of calibration measurements were necessary. In order to evaluate the optical power delivered at the wafer plane we carried out measurements using a Thorlabs S120-VC Si Photodiode power sensor connected to a Thorlabs PM100D Powermeter console. In order to measure the optical power delivered at each wavelength of interest we carried out multiple power readings in Wavelength-power setpoint pairs and obtained

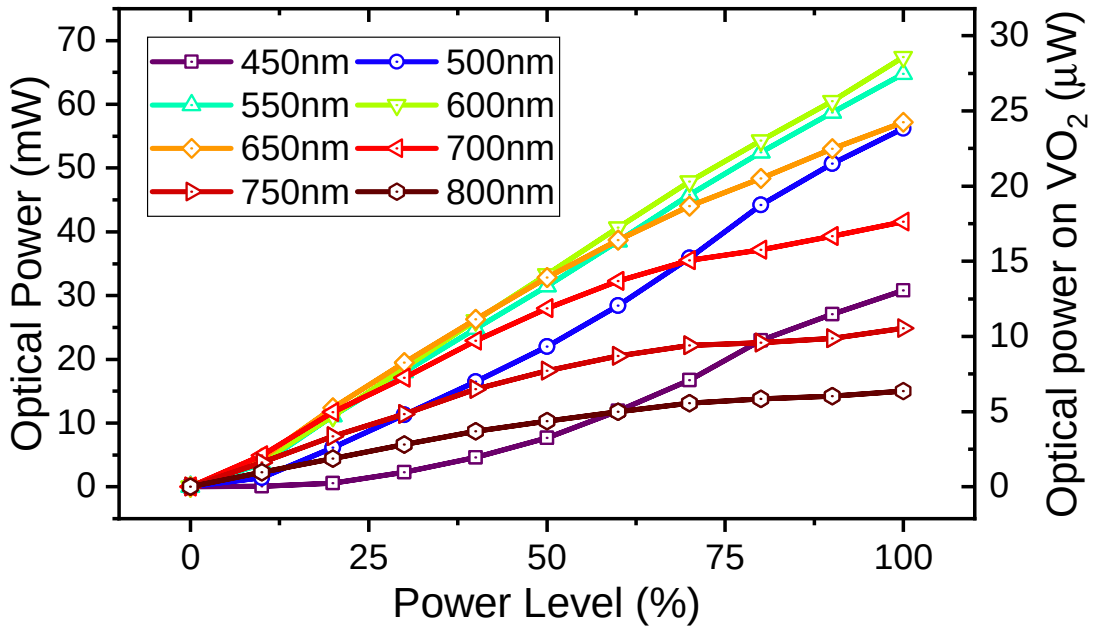


Figure 5.2: Optical power measurement at the end of the optical chain at setpoints between 0 and 100% and wavelengths between 450nm and 800nm. On the left Y axis we represent the power levels recorded with the powermeter at the wafer level while on the right Y axis we represent the calculated optical power incident on the active VO_2 device area. The X-axis corresponds to the user-set percentage of the maximum laser power.

the curves shown in figure 5.2. The calibration measurement results indicate that the attenuation caused by the optical path is heavily dependent on the wavelength and power setpoint level, showing considerable losses towards the longer and shorter ends of the wavelength spectrum, with comparably higher losses in the 450nm-500nm and the 700nm-800nm ranges as opposed to the 550nm-650nm wavelength range. As a consequence, all subsequent measurements will be reported with respect to the true optical power measured at the wafer plane, irrespective of the power setpoint of the laser source itself.

One important aspect to consider is that the beam power is distributed across the entire area of the focused spot. According to figure 5.1(b), the spot diameter in the plane of the wafer measures approximately 0.6mm across. This dimension was estimated by comparison with the dimensions of the VO_2 device contact pads that can be seen illuminated by the laser, which were designed to be 100 μm wide and 250 μm long. The active VO_2 device dimensions, however, are defined by the layout drawing

mask at $6\mu m \times 10\ \mu m$. This implies that only a fraction of the available optical power can be absorbed by the VO_2 device due to the large discrepancy between illumination spot area ($\approx 0.28 mm^2$) and the active VO_2 area (only $60\mu m^2$). Moreover, the intensity of the beam is not constant along the radius of the spot so the ratio between the beam power and the power incident on the active device area cannot be defined simply in terms of area ratios. Under the assumption that the laser beam is a gaussian beam, the power delivered to an aperture of a diameter smaller than the beam diameter can be found by [168]:

$$P_a = P_0 \cdot \left[1 - e^{\frac{-2r^2}{w^2}}\right] \tag{5.1}$$

Where P_a and P_0 represent the optical power delivered to an aperture with radius r, and the total beam power, respectively, and w represents the radius of the incident beam. In our case, P_0 corresponds to the powermeter reading at each wavelength and setpoint, w corresponds to half of the spot diameter shown in figure 5.1(b) $w = 0.3mm$, and r represents the radius of a circular aperture of area equal to the VO_2 area $P_a = 60\mu m^2$, resulting in $r = 4.37\mu m$. The right Y axis of the plot in figure 5.2 illustrates this effect, and indicates that an incident laser power of $70mW$ corresponds to approximately $30\mu W$ of power delivered to the VO_2 device under test.

5.1.2 Results and discussion

The first experimental step consisted in the DC characterization of the VO_2 device, in order to asses the impact of visible light radiation on the switching dynamics and device parameters. Under laser illumination, we observed a significant modulation of the IMT transition, particularly (i) - we measured a strong, repeatable decrease in the IMT threshold voltage V_{IMT} while increasing illumination intensity across all wavelengths we investigated, and (ii) - we also observed a slight impact of the incident light on the off-state resistance R_{OFF} of the VO_2 devices.

In figure 5.3 we illustrate these effects in the case of illumination at $\lambda = 450nm$. The two effects indicate that under external illumination, the dissipated power required to trigger the IMT decreases, since $P_{IMT} = V_{IMT}^2 / R_{OFF}$, which suggests that the incident optical power is absorbed and the resulting generated heat contributes to bringing

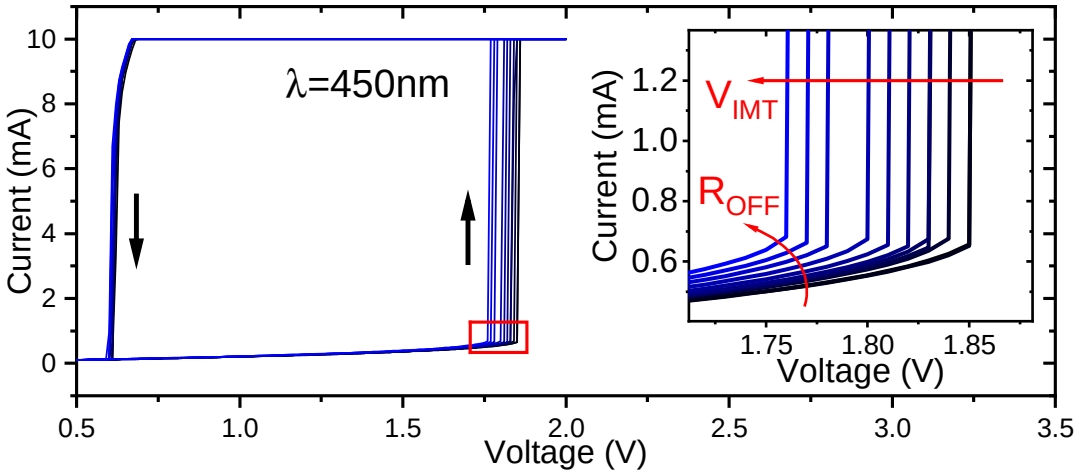


Figure 5.3: Current-Voltage characteristic of the VO_2 device subjected to increasing optical power levels at $\lambda = 450nm$. Inset illustrates that as the incident power is increased, the IMT transition threshold V_{IMT} decreases, accompanied by a slight increase in the off-state resistance R_{OFF}

the device temperature above its IMT transition temperature T_{IMT}. This effect is noticeable across all wavelengths we investigated and the I-V curves of the device under test illuminated across the visible spectrum are depicted in figure 5.4. It is important to notice, however, that the magnitude of the effects described here are heavily dependent on incident wavelength - for example, towards the shorter-wavelength end of the spectrum the decrease in V_{IMT} and increase in R_{OFF} are considerably more pronounced than in the region that corresponds to longer wavelengths. We attribute this effect to the wavelength-dependent absorption coefficient of VO_2 and will be discussed shortly.

It can also be observed that the effect of incident light on the reverse MIT transition, however, remains limited, and as such, the opening of the hysteresis window $V_{IMT} - V_{MIT}$ is dominated by the considerably larger shift induced upon V_{IMT}. In the previous chapter (4) we revealed that the opening of the hysteresis window is strongly correlated to the frequency of the oscillator circuit due to the direct influence of V_{IMT} and V_{MIT} on the oscillation amplitude. A decrease in the value of $V_{IMT} - V_{MIT}$ translates into an increase in operating frequency due to shorter charge- and discharge-intervals that the load capacitance undergoes.

This effect is clearly demonstrated in figure 5.5, where we illustrate the correlation be-

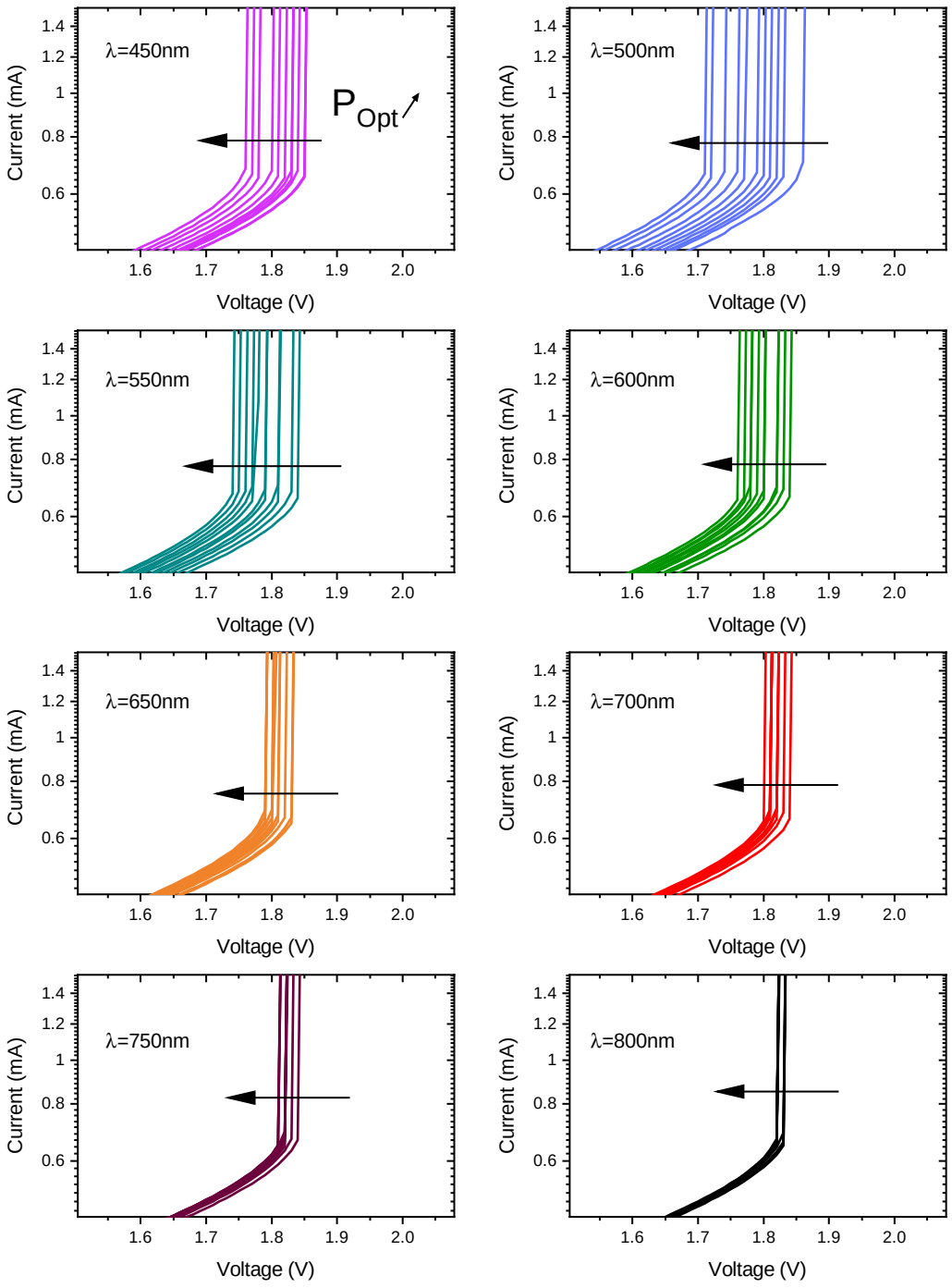


Figure 5.4: Current-Voltage characteristic of the VO_2 device subjected to increasing optical power levels at eight key wavelengths across the visible spectrum. Arrows indicate a downward shift in the IMT threshold V_{IMT} and the magnitude of the shift depends considerably on wavelength.

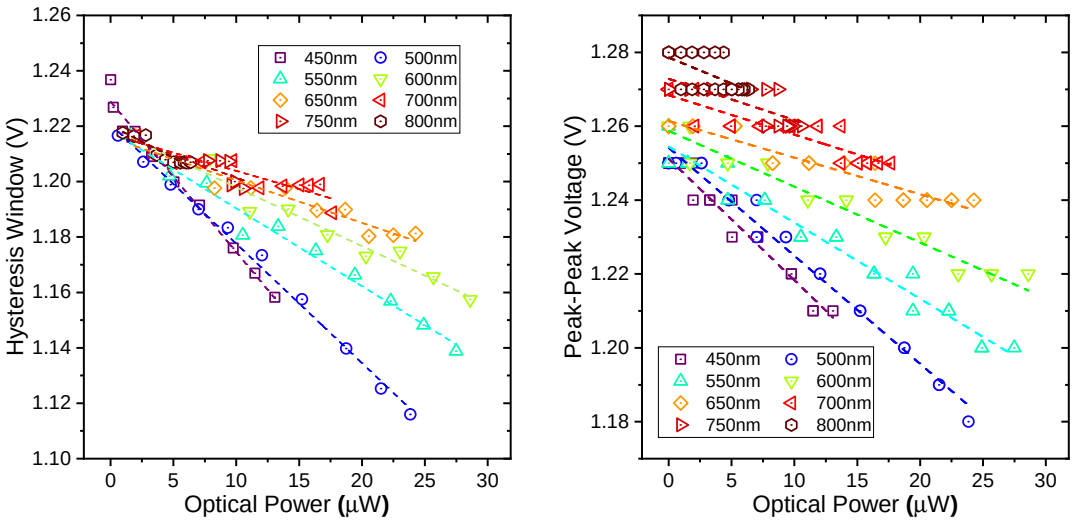


Figure 5.5: Left: The VO_2 hysteresis window width, extracted from static I-V characteristics under optical stimulation across the visible spectrum; Right: Measurement of the peak-to-peak voltage of the oscillator output under optical stimulation across the visible spectrum

tween the hysteresis window width (left) and the peak-to-peak voltage measurement of the oscillator output signal (right) at all wavelengths and incident power levels. There is, however a certain lack of similarity between the hysteresis window width and the peak to peak voltage. First, the measurement of the peak to peak voltage was performed using an automated algorithm running in realtime on the Rohde&Schwarz RTB2004 oscilloscope, with a resolution of only 10 mV. This effect is easily noticeable, especially towards the longer-wavelength end of the visible spectrum, where the total variation of $V_{IMT} - V_{MIT}$ is comparatively small with respect to the region of shorter wavelengths. Second, the mismatch between the measurements can be attributed to slight variations in VO_2 switching dynamics when measured in a static fashion (single I-V characteristics, as performed in order to obtain the hysteresis window width values) as opposed to the true switching behavior of the VO_2 while continuously being subjected to repeated on-off cycles. The third and most obvious effect is the misalignment of the wavelength V_{PP} curves at no illumination (zero incident power).

The cause of the measured misalignment can be attributed to a slight amount of drift that can be caused by a progressively higher background thermal contribution due to continuous prolonged oscillation. This long term heating phenomenon has the same effect on VO_2 switching dynamics as the incident optical power does, causing an

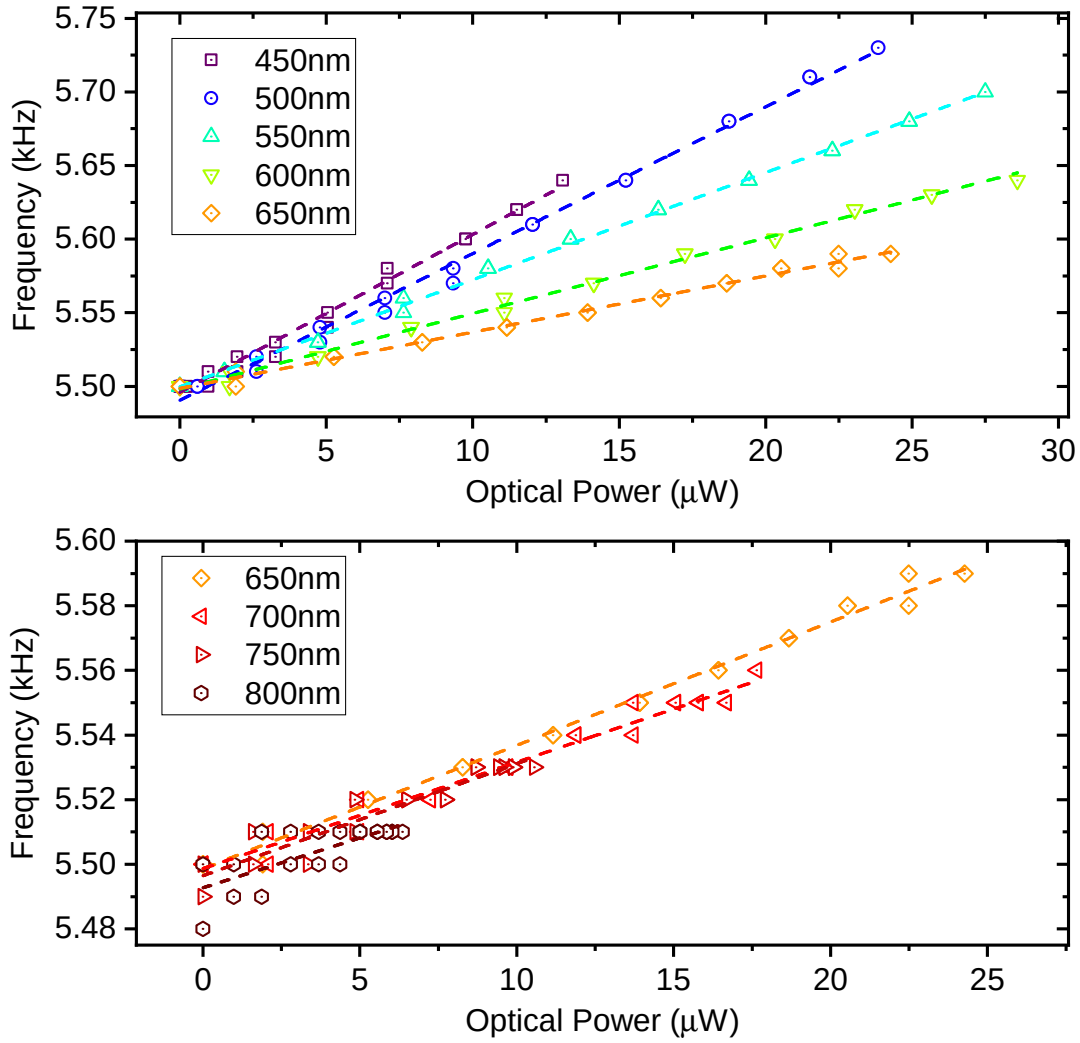


Figure 5.6: Frequency shift of the oscillator output as a function of incident power at different wavelength of the visible spectrum, with a drift correction of -80 Hz/h applied. The curves were separated in order to improve clarity of the long-wavelength plots.

increase in oscillator frequency over longer time periods by the exact same mechanism that is exploited for incident power sensing - the thermal stimulation of the VO_2 device induces variations in V_{IMT} and R_{OFF} that translate into variable voltage levels available for the load capacitance to charge to and discharge from, thus modulating the free running frequency of the VO_2 oscillator. The drift amount has been estimated at approximately -80Hz/h by monitoring the frequency measured at no illumination (before every wavelength measurement series) across the entire experiment duration.

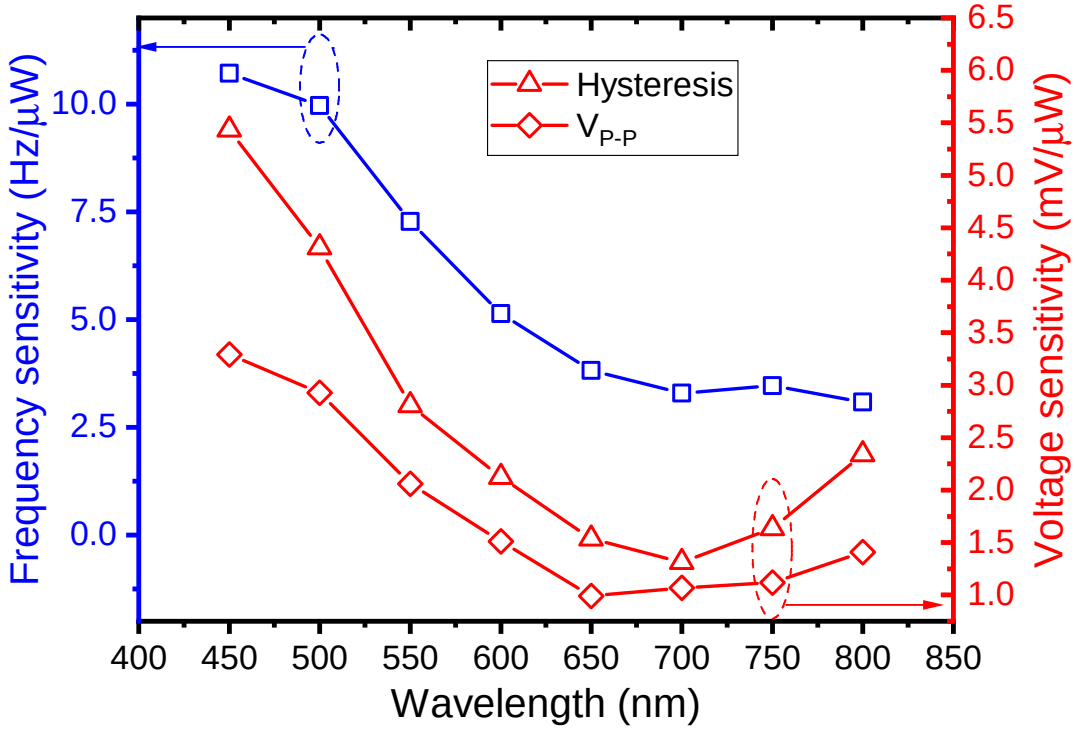


Figure 5.7: Experimentally extracted sensitivities of oscillator output frequency, hysteresis window width and peak-to-peak voltage to incident optical power as a function of wavelength

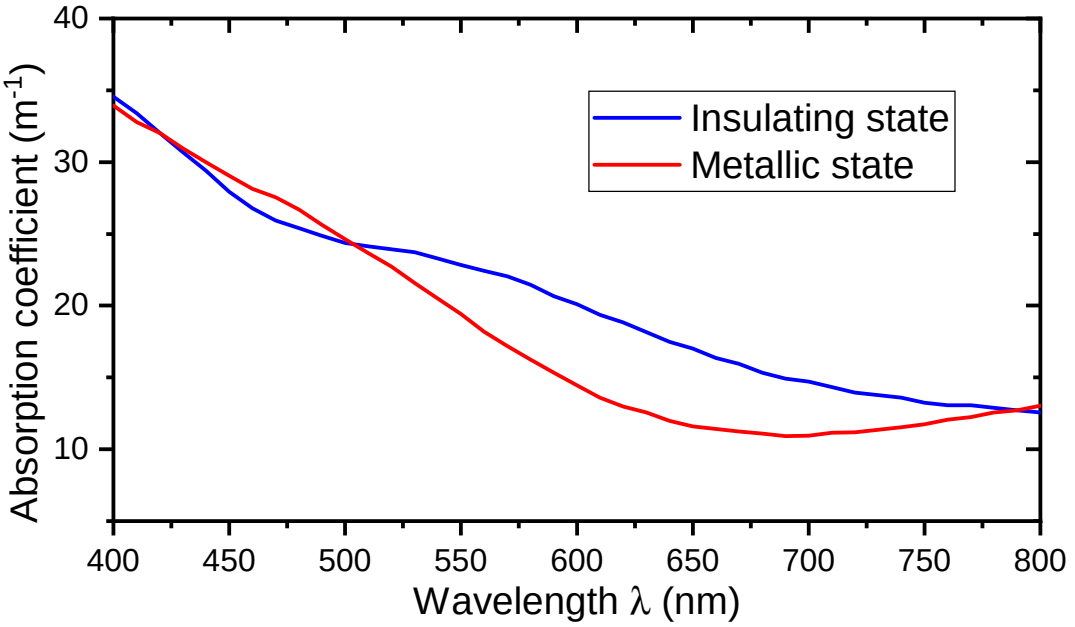


Figure 5.8: The absorption coefficient of VO_2 in the insulating and metallic states as a function of wavelength. Data from [169]

In figure 5.6 we illustrate the oscillator frequency measurements performed under laser illumination from 450nm to 800nm with an applied drift correction. It can be noticed that the Frequency-to-Power (F-P) characteristics exhibit outstanding linearity across the wavelengths of the visible spectrum. This is mainly due to the fact that both the incident power and the subsequent shift in V_{IMT} are relatively small quantities (in the order of μW and mV).

In the previous chapter we explored the sensitivity of output frequency to the hysteresis window width and observed that even at $V_{IMT} - V_{MIT}$ shifts in the 100s mV range, the frequency-hysteresis width curve still deviates very little from its associated linear regression. In contrast, the power levels employed in this experimental study induced V_{IMT} shifts almost one order of magnitude lower (maximum 10mV at 500nm, according to figure 5.5), so the linearity improved even more. The sensitivity of output frequency with respect to incident power, as well as the sensitivities of hysteresis window width and peak-to-peak output voltage with respect to incident power are depicted in figure 5.7, indicating sensitivities up to more than 10 Hz/μW for frequency and more than 5 mV/μW for VO_2 hysteresis width under optical stimulation in the visible spectrum.

Finally, we again observe a decreasing trend in the slope of the F-P characteristic confirmed also by the frequency sensitivity curve shown in figure 5.7, indicating lower sensitivities towards the long-wavelength region of the visible spectrum. This effect can be explained by the considerably lower absorption coefficient that VO_2 exhibits both in insulating and metallic state[169] at longer wavelengths. By comparing figures 5.7 and 5.8, a clear correlation can be observed between all sensitivity curves and both metallic- and insulating-state absorption coefficients of VO_2. This suggests that higher absorption coefficients determine a more efficient conversion from incident radiation power to VO_2 intrinsic temperature increase, translating into higher responsivity and better frequency control via the electrothermal sensing mechanism presented in this study.

5.2 Ghz/mmWave sensing

The surprisingly good linearity and high responsivities obtained under optical stimulation in the visible light range reported in the previous section have determined

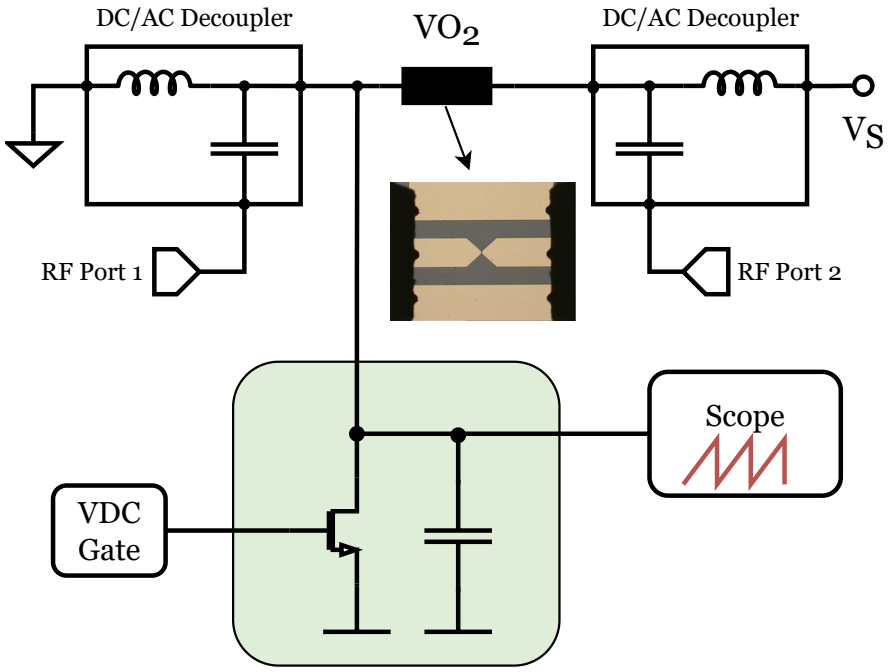


Figure 5.9: Measurement setup used to carry out experiments investigating the effect of incident mmWave radiation on the switching dynamics of VO_2 and output frequency of the VO_2 oscillator. Inset shows the microscope capture of the interrupted co-planar waveguide (CPW) that contains the VO_2 device.

us to continue investigating the feasibility of the VO_2 relaxation oscillator sensing circuit in other bands of the electromagnetic spectrum. Particularly, in this study we focused on the response of the proposed oscillator towards excitation via low-energy millimeter-Wave (mmWave) photons. Specifically, we have investigated the impact of incident mmWave radiation on VO_2 switching dynamics and oscillator free running frequency under broadband (60GHz - 110GHz) RF power injection at incident power levels ranging from -30 dBm up to 0 dBm.

5.2.1 Methods

The experiment was carried out using the experimental setup presented in figure 5.9, and is broadly similar to the measurement setups employed for oscillator measurements presented in the previous chapters, with differences arising only from the method of power delivery to the active VO_2 device integral to the oscillator circuit. It can be noticed from the inset in figure 5.9 that the VO_2 device is constructed in a Ground-Signal-Ground (GSG) configuration, and thus acts as a co-planar waveguide

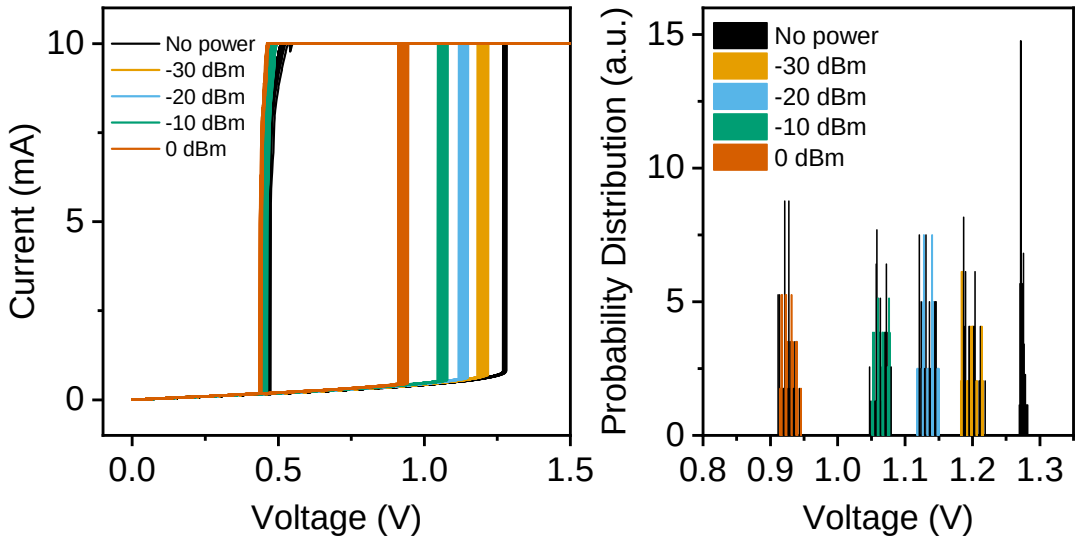


Figure 5.10: (a) The effect of external RF excitation at multiple power levels on the static I-V characteristics of the VO_2 device, indicating a strong influence of incident radiation on the IMT threshold voltage V_{IMT}; (b) The probability distribution of the V_{IMT} threshold voltages at different power levels confirming a considerable downwards shift as a consequence of increasing incident power levels.

(CPW) that is interrupted along the signal line by the impedance of the VO_2 patch. This enabled connecting the VO_2 device to the DC and RF external circuits and instruments using a pair of GSG 220Ghz Infinity Probes. The mmWave power was applied to the VO_2 using an ANRITSU Vector Star Vector Network Analyzer (VNA) routed to a pair of DC/AC decouplers, as shown in figure 5.9. This allowed the application of mmWave power to the VO_2 while also permitting DC (and low frequency) connectivity to the rest of the oscillator circuit (the MOSFET and the load capacitance).

5.2.2 Results and discussion

Upon applying RF power levels ranging from -30 dBm up to 0 dBm in the 60Ghz-110Ghz range, we observed again a considerable shift in the IMT voltage threshold V_{IMT} towards lower voltages, similar to the results we reported on the optical study presented in the previous section. As we performed the static I-V characterization, we subjected the VO_2 device to 100 switching cycles (double sweeps of the DC applied voltage) and recorded the results, illustrated here in figure 5.10(a).

The individual I-V curve measurements reveal that although the V_{IMT} exhibits vari-

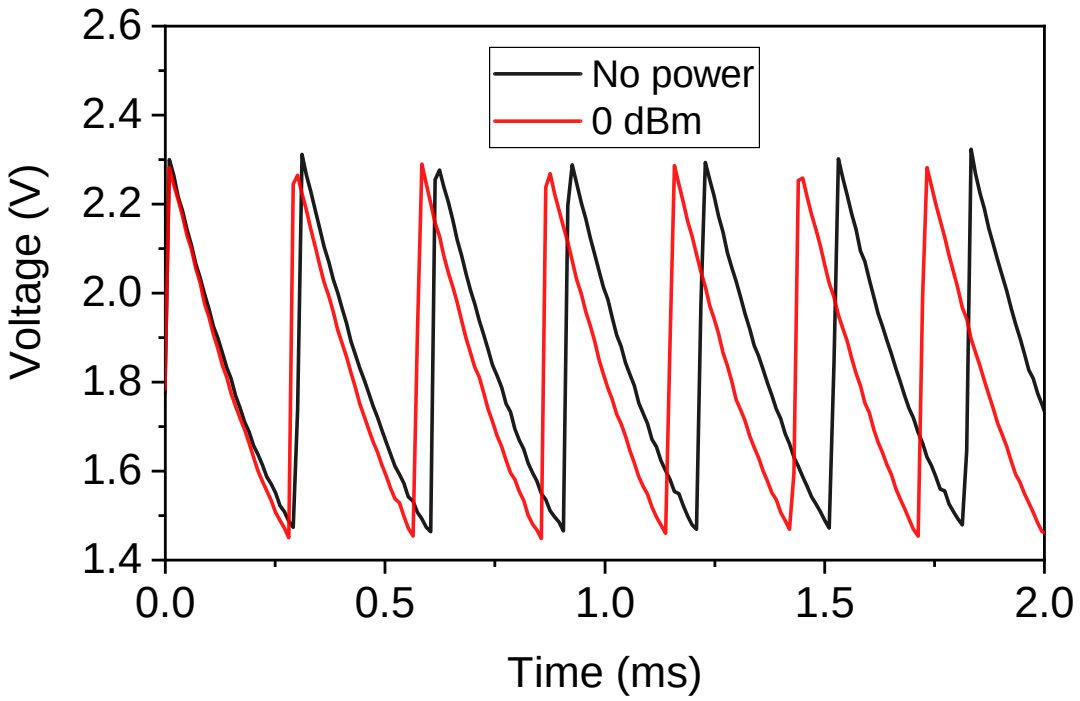


Figure 5.11: Oscilloscope capture of the oscillator output waveform under no applied power and at 0 dBm of applied RF power, outlining a clear increase in oscillation frequency as a consequence of external stimulation of the VO_2 device

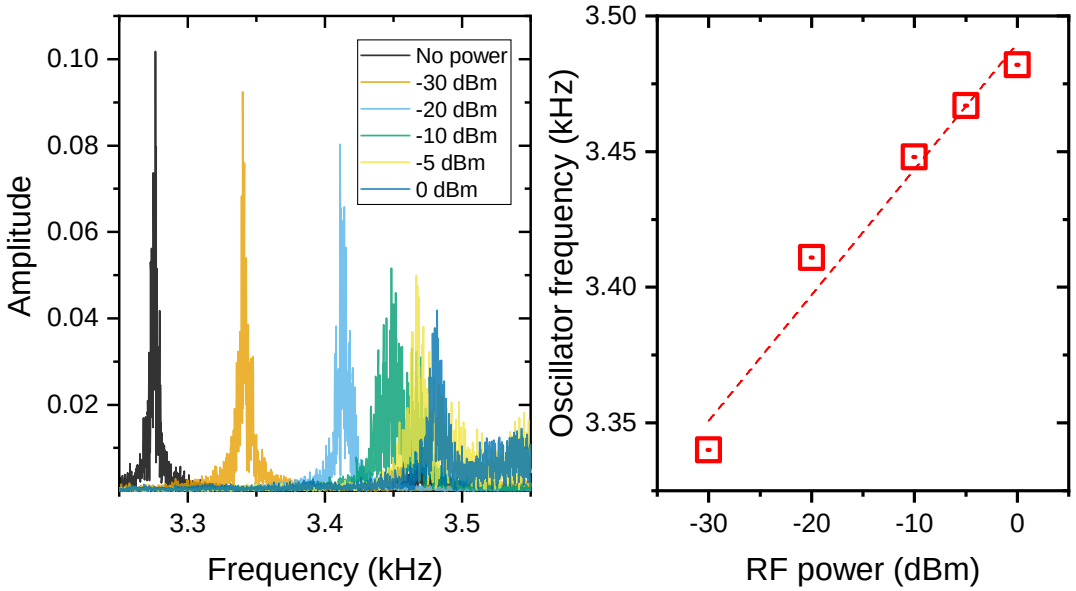


Figure 5.12: (a) - FFT spectra of the oscillator output voltage at RF power levels ranging from -30 dBm up to 0 dBm, including the case where no power was applied; (b) - Oscillator output frequency represented as a function of incident RF power

ability from cycle to cycle, the sets of characteristics are well separated and clearly defined under the incident power levels we applied, and in figure 5.10(b) we present the probability distributions of the V_{IMT} threshold voltage at each applied power level. It can be noticed that, similar to what we found when performing the optical illumination experiment, the influence of incident power on the switching characteristics of VO_2 remains limited to V_{IMT} only, while the reverse transition threshold V_{MIT} remains largely unaffected. The immediate effect is a downwards shift of the hysteresis window width $V_{IMT} - V_{MIT}$ that has a direct influence on oscillation frequency. Indeed, this effect is noticeable in figure 5.11 where we illustrate the oscilloscope captures of the oscillator output voltage when no power is applied and when 0 dBm of 60-110 GHz RF power is applied. In order to assess the frequency shift caused by incident power, we calculated the frequency spectra by means of FFT and subsequently measured the frequency corresponding to the first harmonic for each power. The results are shown here in figure 5.12(a), along with the representation of frequency shift with respect to applied RF power, in figure 5.12(b), indicating a frequency sensitivity of approximately 4.6 Hz/dBm with respect to applied wideband (60GHz-110Ghz) RF power.

5.3 SPICE-Compatible modeling of vanadium dioxide steep slope switches

Modeling the electrical switching behavior of VO_2 switches is an important aspect to consider, as it enables the evaluation of more complex and potentially interesting circuit configurations that implement one (or more) VO_2-based devices as active elements. There have been several proposals towards compact modeling of the VO_2 behavior with the aim of integration with standard circuit simulation frameworks, and the approaches generally focus on reproducing the hysteretic current-voltage characteristics commonly exhibited by two-terminal VO_2 switches. For example, Maffezzoni et al. [170] proposed a driving point model of the VO_2 device that is able to reproduce the hysteretic I-V behavior with high accuracy. In this approach, the electrical resistance of the VO_2 is modeled as a voltage-dependent resistor that is being controlled by the output of a voltage comparator which monitors the voltage drop across the device terminals and compares it to preset V_{IMT} and V_{MIT} voltage thresholds. The advantages of this model lie in its simplicity and ease of implementation in commercial CAD platforms and simulators. On the other hand, this model does not capture

the electrothermal behavior characteristic to VO_2 devices and cannot reproduce the change in VO_2 electrical resistance as a function of temperature.

An alternative modeling approach has been proposed by Dasgupta et al. [171], where a physics-based compact model that can capture the interesting behavior of phase-transition materials has been developed and implemented in VerilogA. The model formulates the insulator-metal phase transition in terms of a first-order Landau phase transition in order to model the resistivity-temperature relationship. In addition, the authors capture the self-heating effect that occurs when the VO_2 element dissipates power, a contribution that is evaluated and added to the "local" device temperature at every simulator iteration. Moreover, the authors also capture the dynamics of multiple domain switching by treating the VO_2 resistor as a 1-D device consisting of multiple identical smaller resistors that undergo phase transition independently and are thermally coupled to one another.

The model we have developed is based on a driving point equivalent approach similar to that presented in [170], while also capturing the temperature-dependent electrical resistance of the VO_2 driven by the local temperature increase caused by electrical power dissipation (Joule heating). Our model makes use of behavioral sources that can implement mathematical functions and calculations of arbitrary complexity using circuit voltages and currents. In addition, behavioral sources are a feature common to most SPICE-based simulators so the model implementation is not constrained to a single development platform and simulator choice. The simulations presented in this section have been carried out using SPECTRE, the standard SPICE simulator available in the Cadence Virtuoso suite.

5.3.1 Thermal hysteresis modeling

The first step towards modeling the VO_2 device consisted of capturing the dependence of electrical resistance on ambient temperature, ideally also implementing the hysteretic nature of the transition. This was done using a pair of equations that implement a comparator with variable threshold, and can be expressed as follows:

$$COMP = \frac{1}{2}\left[1 + tanh\left(GAIN \cdot (TLOCAL - TREF)\right)\right] \tag{5.2}$$

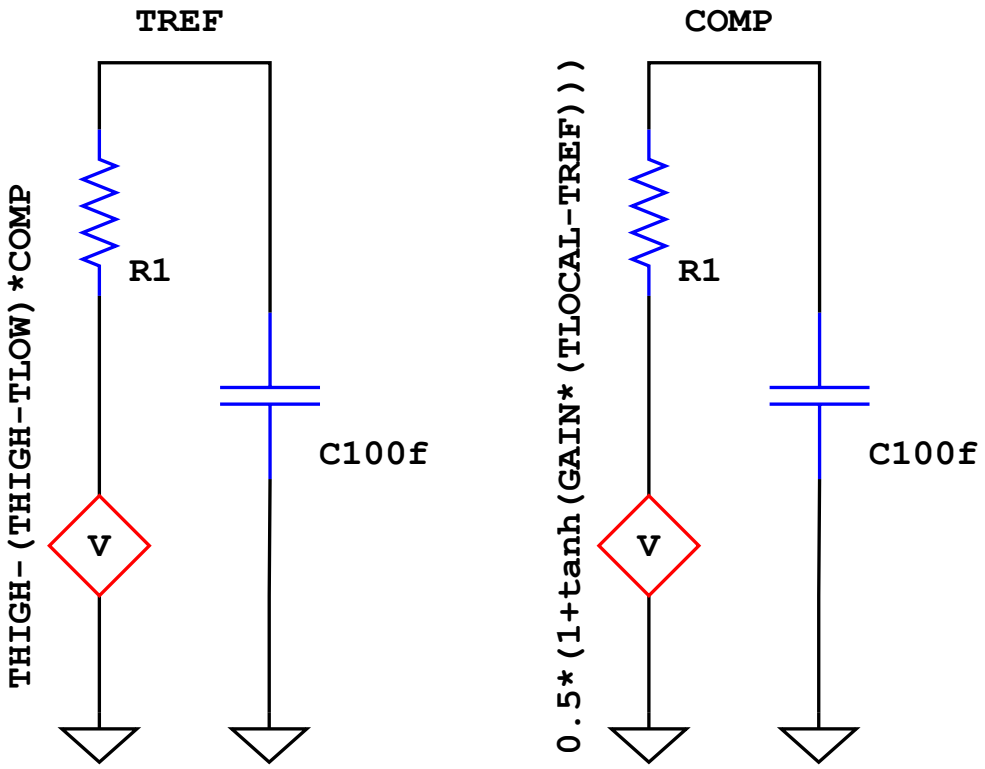


Figure 5.13: Schematic implementation of the Hysteretic comparator using two behavioral sources that implement the comparator equations. Resistors R1 and capacitors C100f are used as convergence aids.

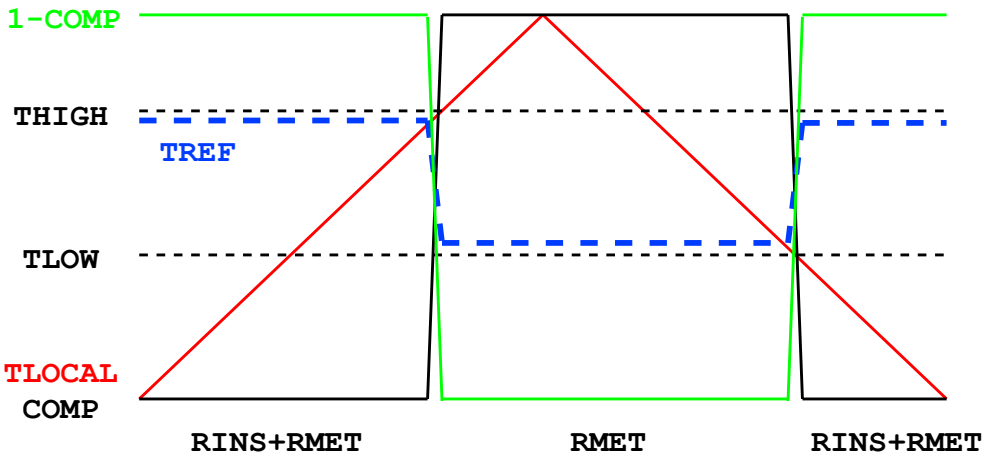


Figure 5.14: Qualitative depiction of the mechanism that enables hysteretic operation of the comparator, outlining the evolution of internal variables as a function of local device temperature $TLOCAL$

$$TREF = THIGH - (THIGH - TLOW) \cdot COMP \tag{5.3}$$

Where $COMP$ represents the output of the comparator, ranging from 0 to 1, $GAIN$ represents a parameter that is used to tune the steepness of the transition at the output of the comparator, $TLOCAL$ represents the effective device temperature (and is not necessarily equal to the ambient/simulator temperature), and $TREF$ represents the comparator threshold with respect to which the comparison of $TLOCAL$ is being computed. Equation 5.3 shows that the reference temperature threshold $TREF$ is directly influenced by the comparator output $COMP$ and is constrained by the parameters $THIGH$ and $TLOW$ that represent the IMT and MIT threshold temperatures, respectively. The schematic representation of the two behavioral sources that implement the equations described above is shown in figure 5.13. In order to facilitate simulation convergence, the sources were not left floating, but instead were connected to ground via very small resistors and capacitors (1 Ohm and 100 femtofarads, respectively). Similarly, a qualitative depiction of the comparator functionality can be seen in figure 5.14, showing the switching of both $COMP$ and $TREF$ when the local device temperature $TLOCAL$ exceeds or falls below $THIGH$ or $TLOW$, respectively.

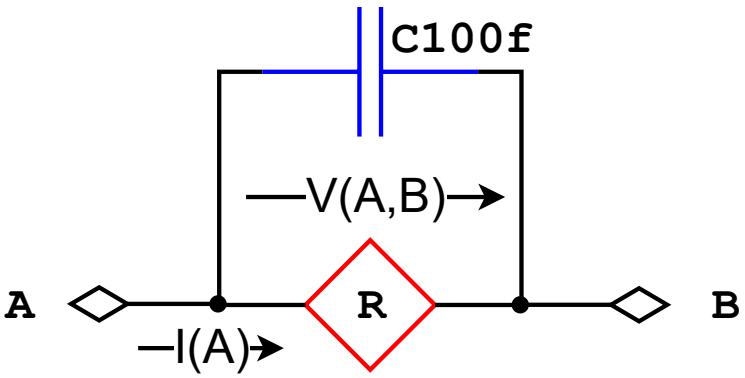


Figure 5.15: Schematic implementation of the behavioral resistor that models the electrical resistance of the VO_2 device controlled by the comparator output. The capacitor C100f is used as convergence aid. Arrows indicate the voltage drop across the VO_2 V(A,B) and the current flowing through the device, measured at terminal A, I(A).

The electrical resistance of the VO_2 device is modeled using a behavioral source as well. The behavioral resistor implements equation 5.4 and its circuit representation is depicted in figure 5.15.

$$RDEV = RMET + RINS \cdot (1 - COMP) \tag{5.4}$$

In other words, when $COMP$ has a value of 0, i.e. the local temperature $TLOCAL$ has not triggered a transition because it is still below the threshold set by $TREF$, the device resistance $RDEV$ is computed as the sum of the VO_2 resistance in metallic and insulating states $RDEV = RMET + RINS$. Once the transition is triggered and $COMP$ becomes 1, the term $1 - COMP$ becomes 0 and thus removes the contribution of the insulating resistance and results in $RDEV = RMET$. In addition, the temperature comparison threshold $TREF$ is updated to the value set by $TLOW$. It is important to mention that the influence of $GAIN$ on the steepness of the transition modeled by the hyperbolic tangent function in equation 5.2 causes a deviation in threshold temperature from the nominal values set by $TLOW$ and $THIGH$.

As shown in figure 5.14, using a $GAIN$=0.07 to ensure smoothness of the transition, it is necessary to overcompensate the $THIGH$ and $TLOW$ values in order to produce the hysteretic behavior. On the contrary, if $TLOW = 58°C$ and $THIGH = 68°C$, the resistance follows the curve indicated in blue, with no noticeable hysteresis. It should be noted, however, that the hysteresis exhibited by the VO_2 resistance versus temperature is not sufficient (and not even necessary) to explain and capture the hysteretic behavior exhibited during electrical measurements. To demonstrate this, all following simulations have been carried out with the parameter set that does **not** produce a

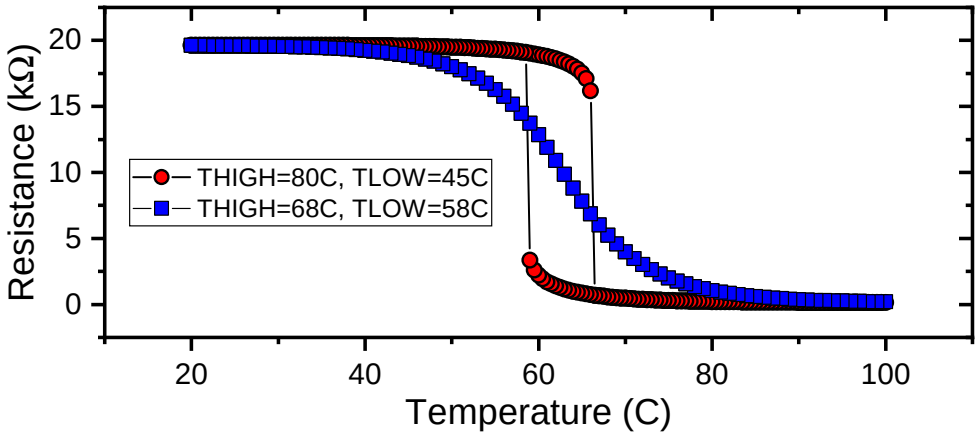


Figure 5.16: Simulation result of the temperature-dependent resistance of the VO_2 device with $THIGH$ and $TLOW$ values that allow (red) or inhibit (blue) the formation of a hysteresis loop in the $R(T)$ characteristic.

hysteretic $R(T)$ characteristic, using $GAIN = 0.07$, $THIGH = 68°C$ and $TLOW = 58°C$. Although this configuration is not entirely realistic and physical, we carried out the simulations without R-T hysteresis in order to achieve faster convergence with minimal loss of accuracy.

5.3.2 Joule heating thermal network

The origin of the hysteretic nature of I-V characteristics of VO_2 devices lies in the self heating mechanism caused by the power dissipated by the device. The effect can be compared to a positive feedback loop, as follows: Upon increasing applied voltage at the VO_2 terminals, the power dissipated by the device follows $P = V/R_{OFF}$. The dissipated power causes a temperature increase that triggers the transition in device resistance according to figure 5.14. Once the transition occurs, the VO_2 resistance becomes considerably smaller, dropping to R_{ON}. This causes an increase in dissipated power that increases the local temperature of the device even more. Upon decreasing applied voltage on the return path of the double sweep, the dissipated power starts to decrease (causing a corresponding decrease in the local device temperature) but the device does not transition back into the insulating state until the temperature falls below the MIT transition threshold. On the return path, though, (temperature decreasing, VO_2 metallic) the power dissipated by the VO_2 is given by $P = V/R_{ON}$. Under the assumption that there exists a direct proportionality relationship between dissipated power and local temperature, and that the critical temperature for the IMT is equal to the critical temperature for MIT (equivalent to a non-hysteretic R-T characteristic), The dissipated power required to satisfy the critical temperature both in the forward and reverse sweep would also be equal. However, since the power dissipated at the IMT event is given by $P_{IMT} = V_{IMT}/R_{OFF}$ and the power dissipated at the MIT event is $P_{MIT} = V_{MIT}/R_{ON}$ and $P_{IMT} = P_{MIT}$, then the critical voltages required to trigger the IMT and the MIT are different, giving rise to a hysteresis in the I-V characteristic, the cause of which is solely the difference between R_{OFF} and R_{ON}, regardless of whether the R-T characteristic is hysteretic or not. In reality, the small hysteresis of the R-T characteristic will, indeed, have an impact on the final hysteresis of the I-V curves, because it directly influences the critical power levels required to induce IMT and MIT, causing the critical power level required for MIT to be smaller than that required for IMT, resulting in a slight widening of the hysteresis loop in the

voltage-sweep I-V characteristic.

The self heating effect has been modeled using a parallel RC circuit supplied by a behavioral current source that models the electrical power dissipated by the VO_2 device:

$$ITH = V(A,B) \cdot I(A) \tag{5.5}$$

Where $V(A,B)$ represents the voltage drop across the terminals of the VO_2 device, and $I(A)$ represents the current flowing through the device measured at one of the terminals (as indicated in figure 5.15). Using the thermal-electrical analogy, the current ITH can be regarded as a power quantity, while the R and the C that are part of the RC network represent the thermal conductivity from device to substrate $RTHSUB$ and heat capacity of the VO_2 element CTH, respectively. Finally, the RC thermal network is referenced to an electrical potential that follows the ambient (simulator) temperature in a 1:1 relationship. The voltage drop across the RC network, therefore, represents the temperature rise over ambient temperature caused by dissipated power, leading to a higher local temperature $TLOCAL$. A simulated voltage sweep is represented in figure 5.18 and indicates that upon IMT, the current through the VO_2 device increases, leading to increased power dissipation, and is hence accompanied by a sharp increase in the device temperature. It should be noted that this simulation has been performed using a 1.2 $k\Omega$ resistor placed in series with the VO_2 device in order to simulate the effect of current limiting, as the implementation of a voltage source with arbitrary compliance current was difficult to implement in the simulation framework. The result of the simulation indicates that the VO_2 device reaches temperatures above 100°C once IMT is triggered, corresponding to a 70-80 deg$C$ temperature rise over ambient, which is comparable to what was reported in [172] upon performing Scanning Thermal Microscopy on two terminal VO_2 devices.

The simulation illustrated in figure 5.19 has been performed using a set of model parameters that match one of the devices we obtained during the PLD optimization study presented earlier in chapter 3, deposited at a laser fluence of 2 J/cm^2 and oxygen partial pressure $P_O = 0.02mbar$. The parameters are summarized in table 5.1 and result in a device with off-state resistance of 19.5$k\Omega$ and on-state resistance of 135Ω switching at $V_{IMT} \approx 3.5V$ and $V_{IMT} \approx 0.5V$. The values of the thermal resistance and capacitance were estimated taking into account the dimensions of the VO_2 device and

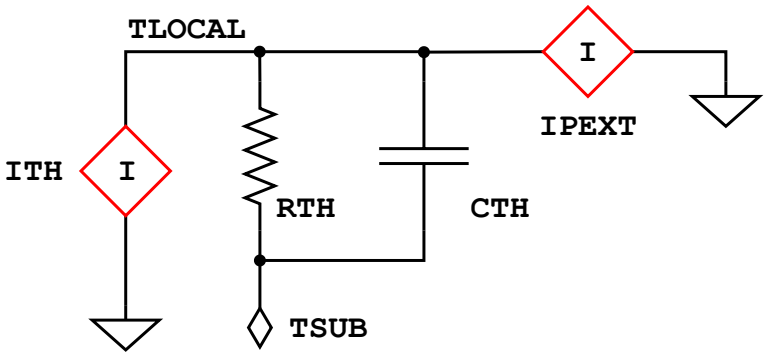


Figure 5.17: Schematic implementation of the Joule heating thermal network, where the thermal resistance and capacitance of the VO_2 device RTH and CTH are used to calculate the local temperature rise over ambient as a consequence of dissipated power - modeled by the behavioral current source ITH and external incident power - modeled by the behavioral current source IPEXT.

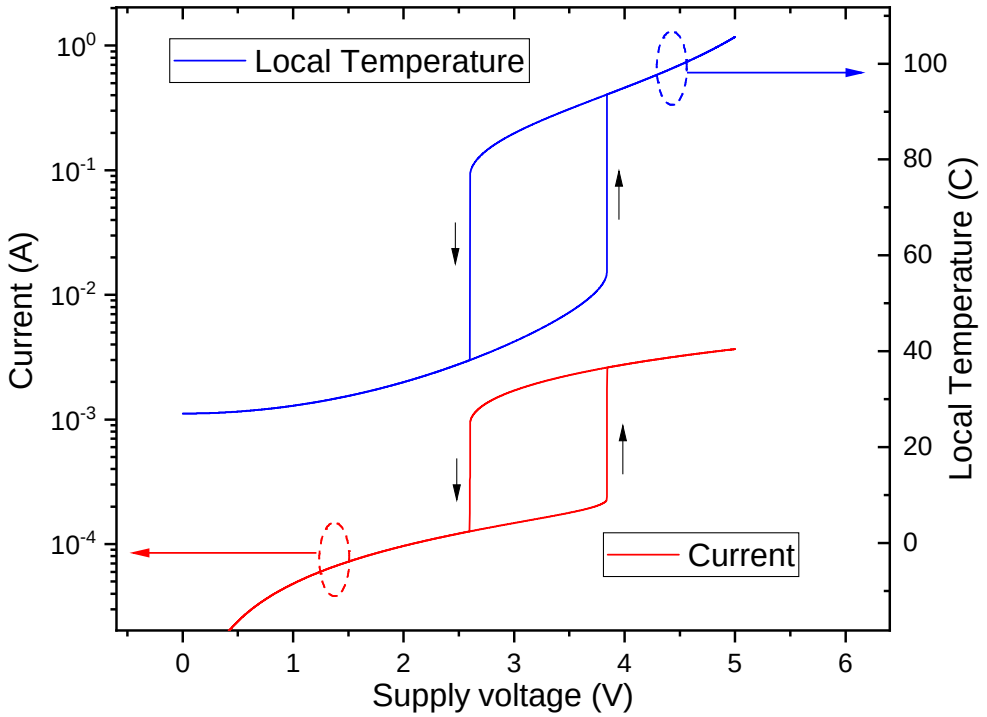


Figure 5.18: Simulated voltage sweep of the modeled VO_2 device using a series resistor of $1.2k\Omega$ implemented for current limiting. With current levels limited to ≈5mA, the modeled local device temperature rises to just above 100C, comparable with reported values measured using Scanning Thermal Microscopy [172]. Device current is represented on the left axis, while device temperature is represented on the right axis.

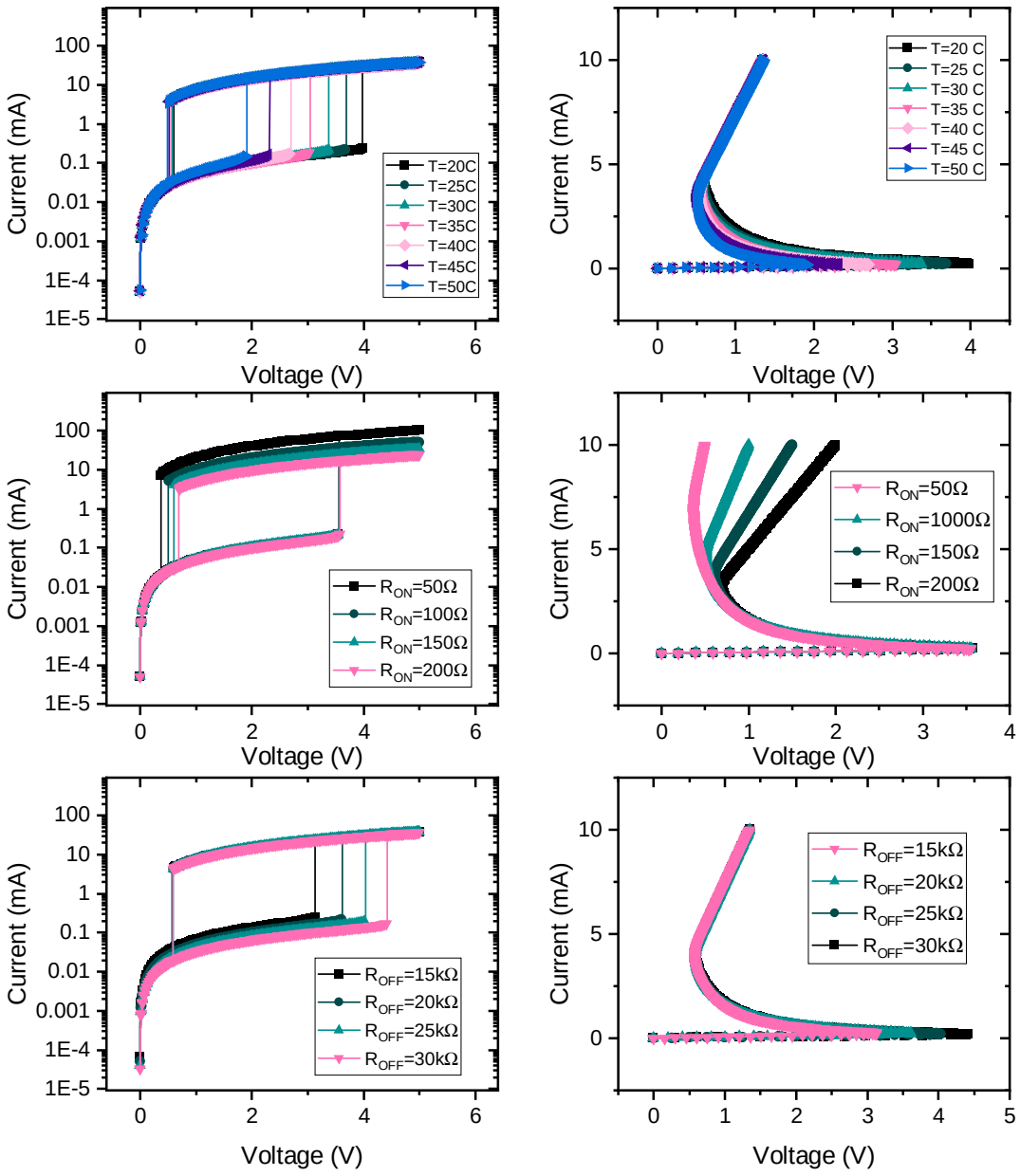


Figure 5.19: Simulation of the current-voltage and voltage-current characteristics of the VO_2 model indicating the influence of model parameters on switching dynamics: (a, c, e) - I-V curves at different temperatures, R_{On} and R_{Off}, respectively; (b, d, f) - V-I curves at different temperatures, R_{On} and R_{Off}, respectively

using a volumetric heat capacity $s = 1.5 \cdot 10^6 J/(m^3 K)$ and a thermal conductivity to the substrate $k = 10^8 W/(m^2 K)$[172]. The dimensions of the device were measured as length $L = 0.8 \mu m$, width $W = 5 \mu m$ and the thickness of the VO_2 film was $t = 200 nm$. We

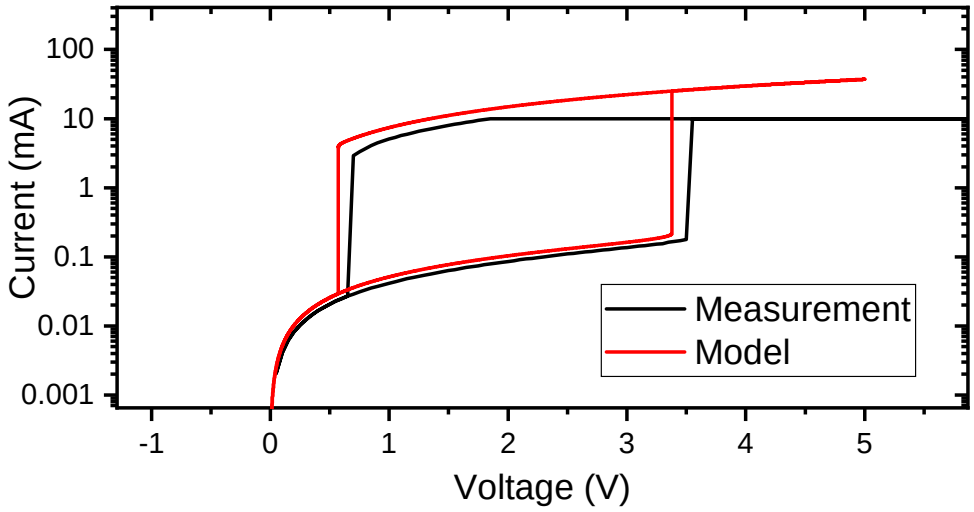


Figure 5.20: Direct comparison between the measured device and the simulated device model, using the parameters from table 5.1. The flattening of the measured curve is due to the current compliance limit set at 10mA.

thus obtained the thermal capacitance parameter $CTH = 1.2 \cdot 10^{-12}$ and the thermal resistance parameter $RTH = 2.5 \cdot 10^{2}$. In order to obtain agreement between the device measurement and the simulated device, it was necessary to amend the thermal resistance RTH by a great amount, which suggest that the model does not yet fully capture the entire physical behavior of VO_2. The large discrepancy between the calculated value of $2.5 \cdot 10^{2}$ and the value used in simulation to produce a close match with the measurement $RTH = 45 \cdot 10^{3}$ may be an indication of a secondary switching mechanism or a thermal distribution that is considerably different from the ideal case, which is entirely possible, given that polycrystalline VO_2 exhibits granular structure and the interaction between single grains can have a considerable influence. This aspect certainly requires further investigation. The comparison between a simulated current-voltage characteristic of the device and the corresponding measurement is presented in figure 5.20.

Using this parameter set we were able to carry out simulations of the I-V as well as V-I characteristics of the device and investigate the impact of ambient temperature, as

Table 5.1: Simulation parameters

THIGH	TLOW	RINS	RMET	RTHSUB	CTH	GAIN
68	58	$19.5 \cdot 10^{3}$	135	$45 \cdot 10^{3}$	$1.2 \cdot 10^{-12}$	0.07

well as on- and off-state resistance R_{ON} and R_{OFF} on the model behavior. The results are illustrated in figure 5.19. First, the effect of temperature is assessed, and appears consistent with previously reported [173] temperature-dependent current-voltage characteristics of two-terminal VO_2 devices. The temperature increase induces a considerable shift in actuation voltage V_{IMT} while at the same time showing limited influence over the reverse transition threshold V_{MIT}. The simulations performed at different values of R_{ON}, however, reveal that the MIT threshold V_{MIT} is considerably influenced by the on-state resistance. This effect was also apparent in our devices measured during the PLD optimization study, exhibiting considerable correlation between the on-state resistance and the MIT threshold. The influence of R_{ON} on the switching characteristics is even more pronounced when performing Voltage-Current characteristic measurements, as shown in figure 5.19(d). Finally, we have assessed the influence of the off-state resistance on the switching behavior and the result indicates that R_{OFF} has a notable influence over the V_{IMT} switching threshold, consistent with our findings from the optical illumination study presented in the first section of this chapter.

5.3.3 Oscillator simulation

Once the SPICE-compatible model of the VO_2 devices was developed, we were able to carry out simulations of the VCO circuit presented in chapter 4. Moreover, the availability of the SPICE model enabled us to simulate the VCO including the sensing functionality offered by the sensitivity of VO_2 switching characteristics with respect to external stimuli. We modeled the external contribution from incident power to the local temperature of VO_2 through a secondary current source as part of the thermal network, adding its contribution to the current source that models the dissipated electrical power.

We were able to observe a frequency shift of 70 Hz in the oscillator output frequency using an incident power level ranging from 0 to 30 μW, comparable to the optical power delivered to the VO_2 device in the visible light study conducted earlier. As it can be seen in figure 5.22(b), the SPICE-based model achieves a sensitivity of 2.35 $Hz/\mu W$ with respect to incident power, which is comparable with the values we obtained in the visible light illumination experiment. Moreover, we have assessed the VCO functionality by evaluating the frequency to control voltage characteristic,

and obtained results that show good linearity and tuning capability, with a simulated sensitivity of 1.87 kHz/V. The transistor model used in the simulation was based on the TSMC 180nm High Voltage BCD process - this was necessary in order to cope with the relatively high supply voltage (5V) needed to ensure oscillation, given the relatively high threshold voltages of the VO_2 device model.

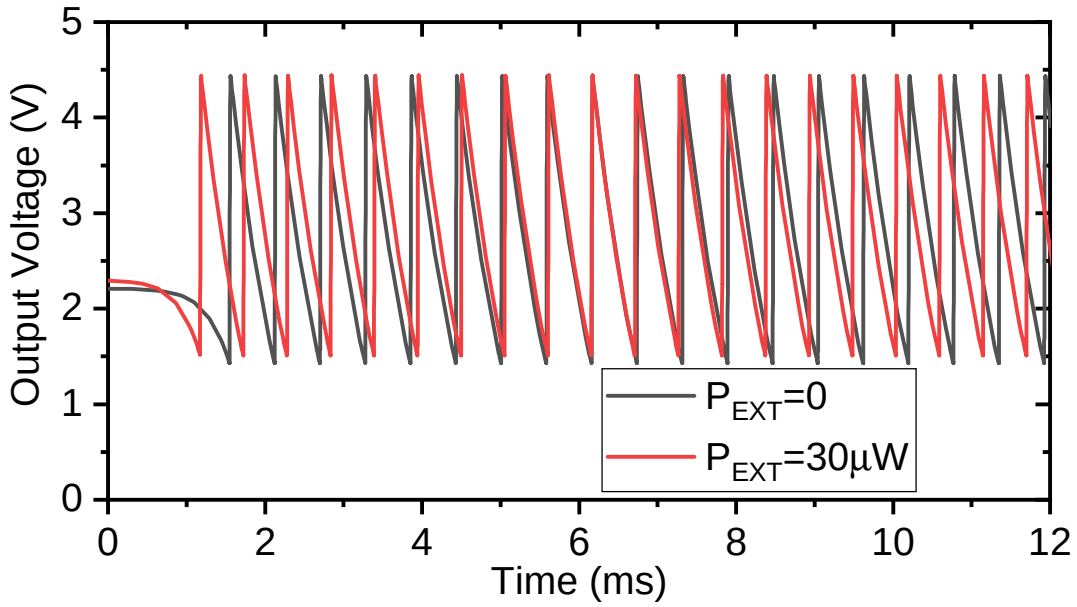


Figure 5.21: Simulated oscillator waveforms with no applied power (black) and with 30μW of external power applied (red)

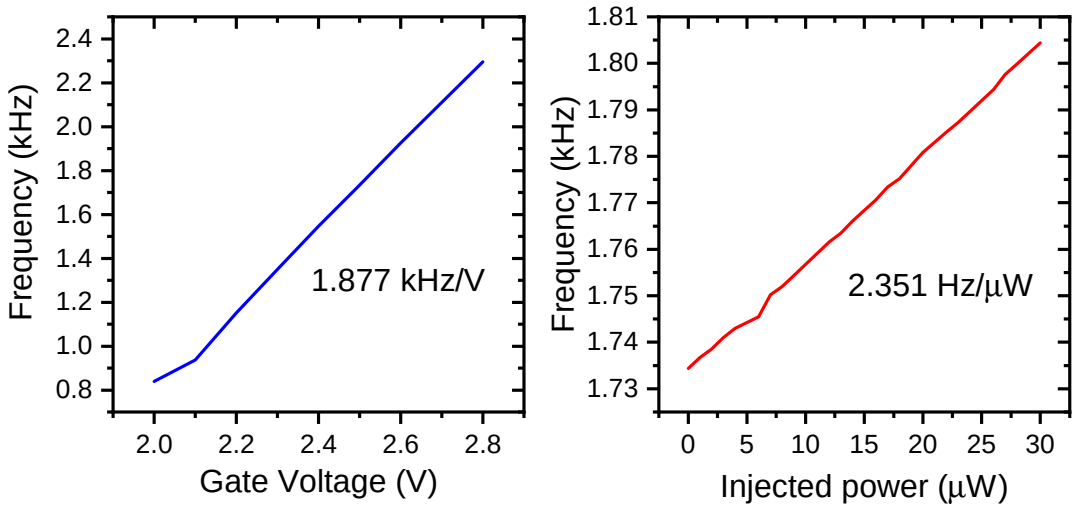


Figure 5.22: (a) - Simulated frequency-voltage characteristic indicating a sensitivity of 1.877 kHz/W; (b) - Simulated frequency-injected power characteristic with a sensitivity of 2.351 Hz/μW

5.4 Summary

The work presented in this chapter was aiming to experimentally validate the spiking sensing functionality enabled by the abrupt transitions and highly sensitive Insulator-to-Metal transitions inherent to VO_2 devices in both static experiments and oscillator readouts. At the same time, we have demonstrated that the compact 1T-1R voltage-controlled spiking oscillator circuit is capable of generating frequencies that experience significant changes depending on the influence of externally applied stimuli on the intrinsic electrical properties of 2-terminal VO2 structures such as phase transition thresholds and the electrical resistance in the metallic and insulating phases.

In the first part of this chapter we have reported results on the experimental investigations of the VO_2 oscillator used as a light intensity transducer, in the visible range of the electromagnetic spectrum. In the wavelength range from 400nm to 850nm, we have observed a strong modulation of the insulator-to-metal switching thresholds of the VO_2 device that translated into significant changes in oscillation amplitude and frequency. This enables **our proposed circuit to function as a power-to-frequency transducer across the entirety of the visible spectrum** exhibiting excellent transducing linearity and moderate sensitivities as high as 10 $Hz/\mu W$ in the short-wavelength region of the visible spectrum, indicating increased sensitivity to ultraviolet radiation. As reported in the previous chapter, we have observed an associated stochasticity of the behavior of these VO2 spiking circuits and a resulting noise but here we have not investigated how this could affect the sensor performance (such as the signal-to-noise ratio).

On the other hand, we conducted another exploratory study on a spiking VO_2 oscillator functionality as a read-out circuit for GHz/mmWave sensitive VO_2 structures and demonstrated RF power-to-frequency sensitivity figures of 4.64 Hz/dBm, when exposed to incident wideband RF power in the 60Ghz to 110GHz range. This study was conducted in collaboration with another PhD of Nanolab-EPFL who designed the high frequency setup and made measurements in both co-planar waveguide and antenna concentrator configurations. In the work reported here, my contribution was to setup and tune the spiking oscillations conditions for this high frequency study and collaborate in the joint interpretation of the data and sensitivity extractions.

In the final part of this chapter, we have **proposed and validated a SPICE-compatible**

model for 2-terminal VO_2 devices that captures one key behavior of VO_2 concerning the hysteretic dependence between electrical resistance and ambient temperature, as well as the self-heating effect caused by electrical power dissipation internal to the device. The temperature dependence (or temperature drift) is a very important parameter of every sensor and, for the case of **VO2**, this forms a mandatory requirement for a good calibrated sensor to model and predict the intrinsic temperature dependence of the optical and/or electromagnetic spiking sensors.

The **proposed model includes the effect of the thermal resistance and thermal capacitance of the device and is semi-empirical**; overall, it shows very good capability to capture the main temperature effects on the static device characteristics (and associated hysteresis) that dictate the dynamic oscillator behavior. Therefore, using this original model we were able to simulate the experimental behavior of the voltage controlled spiking oscillator based on VO_2 as well as the sensing functionality enabled when external stimulation is applied. The model was proposed with an extraction procedure based on experimental data (on- and off- resistance, temperature switching thresholds) and calculated data (thermal resistance and thermal capacitance). While the model exhibits great flexibility for refinement and calibration through 7 independently controllable parameters, and accuracy in reproducing the oscillation phenomena in agreement with measurements, it certainly exhibits some limitations at this stage in terms of modeling the entirety of the physical mechanisms and effects characteristic to VO_2, which can be addressed in conjunction with further studies of the VO_2 switching mechanisms involved.

It is important to mention, however, that the sensing architecture we have proposed and implemented so far provides fairly limited advantages in terms of energy efficiency, which remains dictated by the DC power consumption of our circuit. More precisely, the switching characteristics of the VO_2 devices employed dictate circuit operating points that place the overall power consumption in the milliWatt - 10s of milliWatts range (at a supply voltage of $\approx 5V$ and MOSFET drain currents of a few mA). With the help of the device and circuit models we developed, however, we were able to identify several "tuning knobs" that we could potentially explore towards maximizing the energy efficiency of the sensors. Particularly, the supply voltage could be reduced without affecting circuit functionality if (i) VO_2 switches can be developed that exhibit lower turn-on threshold voltage (V_{IMT}) by optimizing the switch geometry and heat dissipation characteristics in order to enhance the electrothermal switching effect

and (ii) advanced MOSFET or other platforms are used that enable high-performance analog operation at lower drain/supply voltages and currents. In summary, we believe that further optimization is required both in terms of device development (further engineering and optimizing material properties and device geometry) and the integration of VO_2 devices with CMOS circuitry at the wafer level (Back-End-Of-Line integration).

Overall, the ability of our spiking oscillator to convert power delivered by external stimulation into a measurable modulation of output frequency makes our proposed circuit a very compact sensor responsive to a wide variety of stimuli integrated with its own readout scheme, and represents one of the first steps towards energy efficient co-integration of sensing and computation.

6 Perspectives

In this PhD thesis, we developed some technological and device building blocks for energy efficient sensing beyond the classical CMOS established technologies. This domain remains relatively new and challenging and has a rather long-term horizon. Therefore, many challenges remain open, many shortcomings need to be addressed, and future research in Nanolab-EPFL and elsewhere is necessary and should be continued on the most promising, highlighted options. In this short final chapter, we build on the conclusions laid out at the end of each chapter of this thesis and we enumerate some of the remaining research priorities that could follow-up after this work, as per the opinion of the author of this manuscript.

Firstly, concerning the topic of Tunnel FETs for cryogenic applications and for charge sensing applied to scalable qubits on CMOS-compatible platforms:

1. The current work demonstrated stable operation of Tunnel FETs down to around 10K, and the removal of the detrimental effect of trap-assisted tunneling below 150K. This is very useful for interfacing electronics for qubits as compared to CMOS and would require the development of complementary tunnel FET technology (high performance complementary devices on same technology has not yet been achieved). However, **qubit integrated readout would require demonstration of the charge sensing with TFETs down to 10-100mK**, which remains an open challenge following this work. To our best knowledge, good TFETs operating at sub-100mK have not yet been demonstrated, and this remains an experiment that should be performed.

2. Applying the charge sensing principle with TFETs may also require more innova-

tion in the design and implementation of the circuitry scheme and measurement techniques, beyond what was initially reported in this work. For example, stimulating the sense gates during measurement using carefully timed current pulses could allow for better estimation of injected/sensed elementary charges. In addition, a complete benchmark is required, comparing Tunnel FETs to Single Electron Transistors (SET) in terms of **sensitivity and charge noise reduction**, a big challenge for future qubits concerning error reduction.

Secondly, concerning the spiking VO_2 sensing architectures, we believe that this is a highly promising domain where functional oxides could really revolutionize the IoT and Edge AI applications, offering a path for the implementation of bio-inspired signal processing in the analog domain. We foresee the following perspectives after this work:

1. The **understanding and the modeling of the stochastic behavior and resulting signal-to-noise ratio in VO_2 spiking oscillators and sensors** – this is a big challenge from a fundamental point of view and for understanding the real limits and advantages of these types of sensors. This will only be achieved by conducting further studies on the switching dynamics - and particularly the filamentary nature of switching in polycrystalline VO_2 thin films in both lateral and vertical switches, as well as using considerably longer sampling times when performing data acquisition of oscillator waveforms, allowing for the identification of stochastic noise sources and phenomena that occur at multiple different time scales.

2. **Optimization of VO_2 material by doping and/or strain to achieve near-100°C IMT/MIT transition temperatures** – in Nanolab-EPFL there is already significant work concerning Ge-doping of VO_2 to achieve transition temperatures larger than 80°C. These types of doped- VO_2 materials should be further developed and their temperature sensitivity studied. Alternatively, it is known that the application of local strain, in structures that can be used as Micro-Electro-Mechanical devices, could also affect and control the transition temperature. This is another avenue for studies, branching from the work presented here.

3. **Development of MHz spiking oscillators operating at sub 0.5V supply voltage** – Improving the energy efficiency of the oscillators can be achieved through the scaling of the supply voltage and active device size. We have shown that the heat transfer

dynamics play an important role in determining switching thresholds in VO_2 and the optimization of heat conduction through scaled geometry of lateral switches, the implementation of thin film vertical switches, and/or using thermally-insulating substrates can help reduce the power thresholds required for switching, thus opening the door towards low-voltage low-current operation of the spiking oscillators. We consider that a MHZ oscillator with sub-0.5V operation is the next feasible step in this domain.

4. **Optimized design of dedicated spiking sensors depending of the external stimuli to sense** – while the VO_2 material itself is sensitive to a large variety of stimuli, dedicated sensor design should better address the reduction of crosstalk and improve the sensitivity to the desired signal (visible spectrum of light, infrared, UV, THz, etc.) This can be achieved by using dedicated design of spiking sensors (for instance, suspended VO_2 spiking bolometers for IR, using specific materials for local filtering for UV sensing, using antenna concentrators for THz sensing). In addition, dedicated spiking oscillator sensors could be specifically designed for sensing mechanical strain, which would require more complex geometries (integration of VO_2 on suspended membranes or cantilevers) and micromachining. For THz sensing, the VO_2 sensors should be co-designed with specific antennas aiming at concentrating the high frequency signals into the regions where the VO_2 material is deposited and connected to monitor the induced changes in the phase transition characteristics.

5. **Fully compact modeling, including scalability, accurate dynamic response and noise** – while in this work we developed first order models for 2-terminal VO_2 switches and oscillators, an accurate compact model capturing scalability and the full DC and AC behavior of VO_2 devices would be necessary in order to support circuit design not limited to just few VO_2 elements. This will require further investigations on the mechanisms involved in the phase transition dynamics of VO_2 in order to expand the modeling approach from the simple electro-thermal formulation used in this work. In addition, an aspect that should be treated in conjunction with the first perspective listed here, would be the development and addition of accurate noise models opening the way towards the design of large-scale Stochastic Neural Networks.

6. **Back-End-Of-Line integration of VO_2 switches on commercial CMOS platforms** - Finally, we believe this is an important aspect that will reinforce implementation paths of many of the perspectives laid out in this chapter. Successful CMOS inte-

gration of VO_2-based devices and optimized sensing structures will unlock the full potential of spiking oscillator-based sensing through the availability of analog signal processing and versatile oscillator biasing techniques that will improve noise behavior and frequency stability. Several challenges lie ahead, however, potentially requiring re-optimization of the VO_2 deposition process flows in order to accommodate for different substrates (for example, if VO_2 is deposited on top of a passivation layer). Another advantage of integrating spiking oscillator structures on CMOS will be the reduction of parasitic elements that negatively impact switching and oscillator dynamics, opening the way towards large-scale integration of high-speed and energy-efficient spiking oscillators for sensing and bio-inspired computing.

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