

# A Cryo-CMOS Wideband Quadrature Receiver With Frequency Synthesizer for Scalable Multiplexed Readout of Silicon Spin Qubits

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**Abstract**—In this article, a cryo-CMOS receiver integrated with a frequency synthesizer for scalable multiplexed readout of qubits is presented, focusing on radio frequency (RF) reflectometry readout of silicon-based semiconductor spin qubits/quantum dots. The proposed spin qubit readout chip consists of a wide-band low noise amplifier (LNA), a quadrature mixer, a complex filter, a pair of in-phase/quadrature (I/Q) intermediate frequency (IF) amplifier chains, and a type-II charge-pump phase-locked loop (PLL) with a programmable frequency divider providing local oscillator (LO) signals. Noise optimizations are applied to the LNA design and the quadrature active mixer design to obtain the required performance. A mode-switching complementary voltage-controlled oscillator (VCO) is proposed to achieve low-power and low-phase noise in a wide-frequency tuning range (46.5%). Circuit modifications and design considerations for robust cryogenic temperature operation are presented and discussed. Measurements show that the receiver provides an average gain of 65 dB, a minimum noise figure of 0.5 dB, an IF bandwidth of 0.1–1.5 GHz, and an image rejection ratio of 23 dB at 3.5 K with a power consumption of 108 mW. This cryo-CMOS receiver with frequency synthesizer for spin qubit readout is a first step toward fully-integrated qubit readout and control.

**Index Terms**—Cryo-CMOS, frequency multiplexing, frequency synthesizer, low noise amplifier (LNA), mode-switching voltage-controlled oscillator (VCO), push-pull VCO, quantum computing, qubit readout, receiver, spin qubit.

## I. INTRODUCTION

QUANTUM computers are expected to address specific sets of computational problems more efficiently than any

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existing classical computer. Their realization is being pursued in a number of technologies, among which solid-state implementations, such as spin or superconducting qubits, are very promising. These qubits require deep cryogenic temperatures (<1 K) to exhibit quantum properties. Therefore, in order to read out and control the qubit state, it was proposed to use integrated CMOS circuits operating at cryogenic temperatures, to be near the qubits [1]–[4].

At the qubit layer, recently, silicon spin qubits have demonstrated relatively long coherence times  $T_2 = 28$  ms [5], fault-tolerant readout and control fidelities exceeding 99.9% [6], and operation at higher temperatures (1.1 K) [7], [8], thus laying the foundations for the realization of compact silicon quantum computers. So far, such achievements were obtained with custom fabrication processes and the simultaneous implementation of all of these properties has not yet been achieved. Nonetheless, thanks to their small size and potential for co-integration with the required classical readout and control electronics, silicon spin qubits realized in quantum dots show great prospects for the creation of cryogenic CMOS quantum-classical platforms for fully-integrated quantum computers.

Together with advances at the qubit layer, significant progress has been made at the electronics layer, with the demonstration of integrated control of spin qubits [9] and superconducting qubits [10] with cryogenic CMOS controllers operating at  $\sim 3$  K. Alternatively, works showing integration at 4 K of charge qubits with classical readout/control electronics have been shown [11], advocating faster readout and control to mitigate the limited coherence time of charge qubits. Such works have shown good prospects for the co-integration of charge qubits and classical electronics at higher cryogenic temperatures (>1 K). On the other hand, less progress and complexity have been shown in the literature on the spin qubit readout side, thus resulting in a cryogenic CMOS chip integrating quantum dots and electronic circuits at 100 mK [12], but without advanced multiplexing and scaling features. Recently, however, receivers for qubit readout have been concurrently reported [13]–[15]. In order to address this gap with the realization of a fully-integrated scalable readout system, this article describes in detail the first fully-integrated cryo-CMOS system-on-chip (SoC) with in-phase/quadrature (I/Q) receiver and frequency synthesizer [13] for scalable, multiplexed radio frequency (RF) dispersive readout of silicon qubits in quantum dots. The cryo-CMOS blocks designed for the cryogenic receiver include a low noise amplifier (LNA), an I/Q

quadrature mixer, intermediate frequency (IF) amplifiers, and a type-II charge-pump (CP) phase-locked loop (PLL) with a proposed mode-switching complementary  $LC$ -tank voltage-controlled oscillator (VCO). For the critical blocks, modified models following previous works [16]–[19] were used to guide the design.

This article is organized as follows. Section I outlines the topic of quantum computing, with the most recent advances in the field of silicon qubits and corresponding readout/control electronics. Section II describes the envisioned fully-integrated cryogenic CMOS platform, focusing on the quantum devices and their dispersive multiplexed readout. Section III derives the specifications for readout and describes the overall SoC architecture. Section IV describes the circuit details and implementation of the proposed  $I/Q$  receiver and frequency synthesizer. Section V details the measurement and characterization of the designed SoC at 296 and 3.5 K. Finally, Section VI concludes this article with a perspective for the future.

## II. MULTIPLEXED RF REFLECTOMETRY READOUT

The implementation of fully-integrated quantum-classical platforms in cryogenic CMOS technology requires the realization of a scalable architecture for the readout and control of silicon qubits. Traditionally, silicon qubits have been implemented in custom fabrication processes [20], thus allowing reaching state-of-the-art performance, but preventing large-scale fabrication and co-integration with electronics in standard processes. Recently, it was shown that reproducible quantum dots can be realized in CMOS technology [21], thus moving in the direction of such co-integration.

In this approach, minimum size transistors in deep sub-micrometer technology nodes can realize few electron quantum dots when cooled down to very low temperatures (50 mK), as depicted in Fig. 1(a). This behavior manifests itself at low drain-to-source bias and in the subthreshold region, as Coulomb oscillations in the current [21], as shown in Fig. 1(b). In order to read out the state of such quantum devices, a typical technique is based on the readout and amplification of the dc transport current with a transimpedance amplifier, as in [12]. This technique is usually limited in bandwidth and does not provide scalability through parallel readout. In addition, direct current measurements do not allow for single-shot readout.

Consequently, RF techniques have become more popular for the readout of quantum devices, in particular, RF reflectometry gate-based readout [22], [23]. In this technique, a weak RF signal is sent to the gate of the quantum device through an  $LC$  resonator, which is tuned to match the gate impedance to  $50\ \Omega$  at the readout frequency, as shown in Fig. 1(c). The cyclic tunneling of electrons in the quantum device creates an additional tunneling capacitance  $C_q$ , thus causing a phase shift in the reflected signal, which carries information about the quantum device state. In the case of few electron quantum dots realized by minimum size transistors at low temperature, similar to dc transport current measurements, the Coulomb peaks can also be resolved in reflectometry. The reflected signal shows a linear dependence with respect to

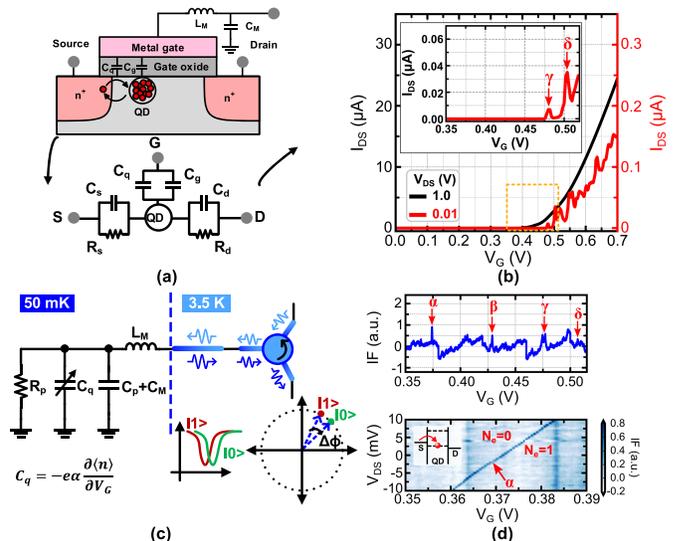


Fig. 1. (a) Few-electron quantum dots realized in minimum size transistors and (b) their corresponding Coulomb oscillations in dc at 50 mK [21]; (c) Gate-based reflectometry readout technique and (d) corresponding Coulomb peaks of few electron quantum dots detected in RF reflectometry [24].

the drain-to-source bias, thus showing that it comes from the charge transition between source and quantum dot [24], as shown in Fig. 1(d). The advantage of this technique, besides not using any additional electrometer in front of the quantum device, is that the frequency-encoded readout allows performing frequency multiplexing, thus allowing parallel readout of quantum devices.

So far, gate-based RF reflectometry has been typically performed at frequencies below 1 GHz using bulky (discrete) surface mount inductors for the implementation of the lumped  $LC$  matching network. This is a disadvantage both in terms of area and available bandwidth. Higher readout frequencies (5–6.5 GHz) allow realizing integrated ( $L \sim 1$  nH) inductors and  $LC$  resonators, with larger readout bandwidths. This solution is more suitable for a scalable, frequency-multiplexed approach, thus enabling co-integration in CMOS technology.

For this reason, the overall cryogenic CMOS platform envisioned in this work, shown in Fig. 2, operates at frequencies around 6 GHz. It comprises a quantum-classical matrix with co-integrated quantum devices and a (time-) frequency-multiplexed readout interface using compact  $LC$  resonators to perform gate-based dispersive readout [24]. It uses a row–column architecture with transistors controlled by shared word line voltages ( $V_{WLi}$ ) for sequential time-multiplexed readout and multiple  $LC$  resonators connected to independent data lines ( $V_{DLj}$ ), resonant at different frequencies ( $f_1, f_2, \dots, f_N$ ), for parallel frequency-multiplexed readout [24]. A multicarrier signal generator creates the required multitone probing signals, using a cryogenic frequency synthesizer generating the local oscillator (LO). The signals flow across the cryogenic circulator [25], which acts as an integrated non-reciprocal device decoupling incident and reflected waves, followed by an integrated phase-sensitive receiver to read out and discern the state of the quantum devices. In this work, the focus is on the receiver and frequency synthesizer.

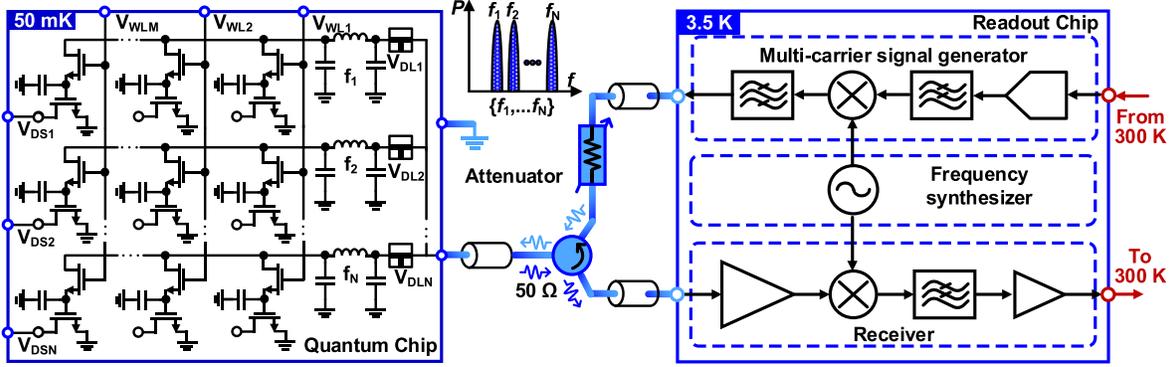


Fig. 2. Envisioned cryogenic-CMOS platform with quantum-classical matrix including quantum dots and (time-) frequency-multiplexed interface using lumped  $LC$  resonators for dispersive gate-based readout, cryogenic circulator, and phase-sensitive receiver with frequency synthesizer.

### III. CHIP ARCHITECTURE AND SPECIFICATIONS

RF reflectometry uses a weak signal to probe a quantum device. The reflected portion carries information about the state of the quantum device. As mentioned in Section II, the change of the tunneling (quantum) capacitance  $C_q$  causes a phase shift ( $\Delta\phi$ ) in the reflected signal. At the same time, the additional  $C_q$  also results in the impedance mismatch ( $\Delta\Gamma$ ) between the quantum device and the  $50\ \Omega$  impedance of the readout cables. This impedance mismatch leads to an amplitude change of the received reflected signal ( $\Delta V = V_{in}\Delta\Gamma$ ) accordingly [26]. Therefore, the quantum information signal can be modeled as an amplitude-modulated (AM) and phase-modulated (PM) version of the input carrier

$$S(t) = A_R \cos(\omega_R t + \phi_R) \quad (1)$$

where  $\omega_R$  is the probing frequency, while  $A_R$  and  $\phi_R$  are the qubit-state-dependent amplitude and phase to be observed, respectively. The modulation values are analog, determined by the Sisyphus resistance  $R$  and tunneling capacitance  $C_q$  of the quantum device. However, the modulation is quantized in the values given by the quantum device states, which reduce to the two states  $|0\rangle$  and  $|1\rangle$  in a qubit. Consequently, the resulting signal can be described as a binary polar amplitude and phase shift-keying (APSK) signal, whose data values are not restricted to 0/1, but determined by the qubit physics. Typically, the amplitude change between the two states is in the order of 1 dB, while the phase shift can vary between  $1^\circ$  and  $12^\circ$  [26]. In order to demodulate such signal, allowing frequency multiplexing at  $\sim 6$  GHz, a wideband  $I/Q$  receiver, as shown in Fig. 3(a), is designed to extract the amplitude and phase information from the  $I/Q$  components according to  $A_R = (I^2 + Q^2)^{1/2}$  and  $\phi_R = \tan^{-1}(Q/I)$ , as shown in Fig. 3(b). For our test sample, the probing signal power is set to  $-100$  dBm, as such value is typical since it should not be too high, thus affecting the state of the quantum device while probing it (kick-back), and should not be too small, so to achieve high charge sensitivity and make the requirements for readout feasible.

#### A. Chip Architecture

As mentioned above, the signal at the input of the receiver is weak, so cryogenic amplification is required. A wideband LNA is chosen for this goal, and it is expected to have the most power consumption among all receiver blocks, in order to satisfy the strict noise figure (NF) requirements for qubit readout. However, a wideband is used to enable multiple qubit channels in frequency multiplexing, thus minimizing power consumption per qubit.

After the LNA, since phase sensitivity is required, an  $I/Q$  down-converter is required. An  $I/Q$  LO signal is generated and used for single-sideband (SSB) down-conversion with an  $I/Q$  mixer on high-side injection, which generates sum and difference frequencies. In order to suppress the sum frequencies (symmetrically at both positive and negative frequencies) and to preserve only the difference frequency, a low-pass filter (LPF) is used. In order to suppress the unwanted image at  $-f_{IF}$ , resulting from the unwanted down-conversion of the signal at  $-f_{IM}$ , a non-symmetrical-in-frequency polyphase filter (PPF) [27] is applied [28]. The residual image signal is determined by the image-rejection ratio (IRR) of the PPF. The use of the PPF allows eliminating the noise that would fall into the gain band from the image band, once the IF signal band is further downconverted to baseband in the digital domain.

Finally,  $I$  and  $Q$  signals are amplified coherently, so as to further increase the signal strength. The IF amplifiers can be followed directly by an external high-speed analog-to-digital converter (ADC) and a digital signal processor (DSP) to perform digitization and baseband down-conversion. Several further filtering operations may be performed in the digital domain. This architecture with a wideband LNA at the input is planned to extend the overall receiver bandwidth in a future implementation by creating an additional IF path with swapped gain and image bands (using the same LO) and using low-side injection. This would not require the use of another LNA, thus making the approach more power-efficient. Moreover, the PPF filter is implemented immediately after down-conversion in the analog domain, because otherwise the image signal would also be amplified by the IF amplifier, thus adding additional noise on a still weak signal and making it harder to address image rejection later in the digital domain.

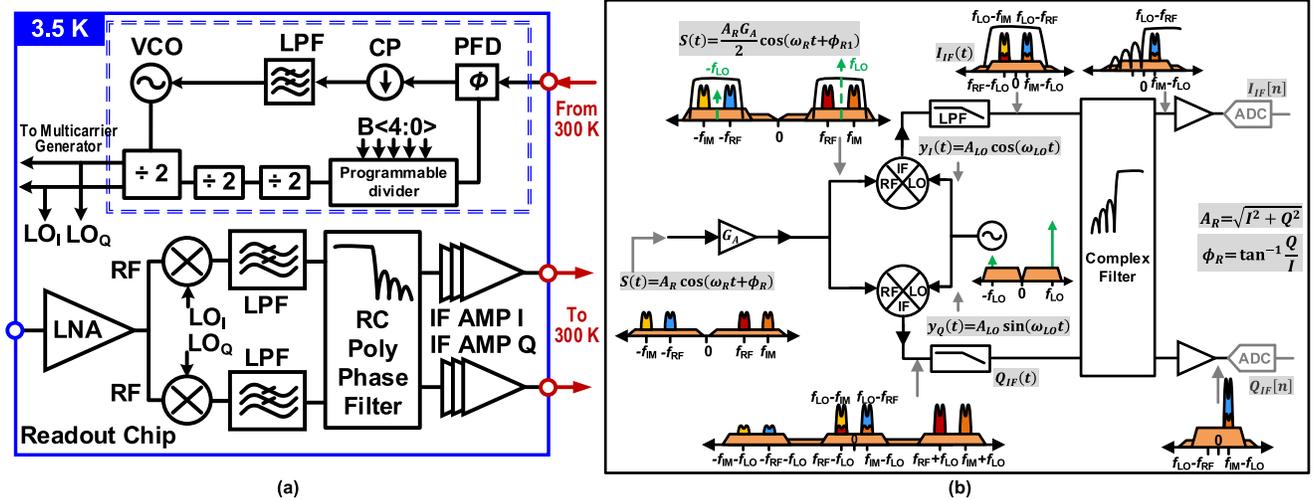


Fig. 3. (a) Structure of the cryogenic receiver for qubit readout proposed in this work; (b) Signal flow and Fourier analysis for the demodulation of the reflected quantum signals.

Additionally, a digital implementation would also result in higher power consumption. In this prototype, ADC and DSP are implemented off-chip at room temperature, but in the future, they could be included on chip.

### B. Specifications

1) *Frequency*: In our architecture, we plan to have a combined time- and frequency-multiplexed readout, thus allowing us to read  $N^2$  qubits by combining parallel readout of  $N$  qubits via frequency-multiplexing with a sequential readout of  $N$  columns via time-multiplexing. The receiver is designed to operate at a frequency around 6 GHz. Assuming a qubit bandwidth  $B = 10$  MHz, which corresponds to a resonator quality factor  $Q = f_0/B = 6 \text{ GHz}/10 \text{ MHz} = 600$  that can be obtained with superconducting resonators co-located with the qubits at 50 mK, the channel spacing can be set to  $10 \times$  the resonator linewidth, so a spacing  $S = 100$  MHz is chosen. To simultaneously read out the qubits at  $f_1 - f_N$ , the IF bandwidth ( $B_{IF}$ ) should be higher than  $f_N - f_1$ . The wider  $B_{IF}$ , the more qubits can be read out in frequency multiplexing. On the other hand, a large  $B_{IF}$  increases the complexity and power consumption for the ADC, which must operate at cryogenic temperature as well [3], thus making it closer to a direct RF sampling ADC [29]. A signal band around 5–6.5 GHz with  $B_{IF} \sim 1.5\text{--}0.1 \text{ GHz} = 1.4 \text{ GHz}$  is chosen, so as to accommodate frequency multiplexing. With this choice, a number of qubits  $N = B_{IF}/(B+S) = 1.4 \text{ GHz}/110 \text{ MHz} \sim 12$  can be read out in parallel in a single qubit measurement time  $\tau$ . Assuming then a square matrix, this would allow to read  $N^2 = 144$  qubits in an  $N \cdot \tau$  time window with time multiplexing.

2) *Noise*: The NF specification of the receiver is linked to the required readout fidelity, which is connected to the bit error rate (BER) of the demodulation of M-ary amplitude-phase shift keying (M-APSK) signals for a given signal-to-noise ratio (SNR) and measurement time  $\tau$  [30].

In dispersive readout, we can assume a phase shift difference to be read out  $\Delta\phi = 12^\circ$  (this can vary depending on the

quantum device and  $Q$ -factor of the  $LC$  matching network between the quantum device and the readout chain). The corresponding multiple phase shift keying (M-PSK) equivalent electrical signal is a 32-PSK signal, given that  $M = 360^\circ/12^\circ = 30$ , so 32 is chosen to have some margin. For a required readout fidelity  $F = 99.9\%$ , the corresponding BER =  $1 - F = 0.1\%$ , and in order to obtain such BER for a 32-PSK signal, the required SNR of the receiver is approximately 100. In dispersive readout of superconducting qubits, quantum efficiency typically also affects SNR, but in spin qubits, the minimum integration time metric  $t_{\text{int,min}}$  is typically used [31], in particular when the readout noise dominates. Assuming a minimum integration time  $t_{\text{int,min}} = 500 \text{ ns}$  (to achieve SNR = 1) for silicon spin qubits, the total required measurement time is linked to SNR by  $\tau = \text{SNR} \cdot t_{\text{int,min}}$ . Consequently, the total measurement time to reach the SNR target becomes  $\tau = 100 \cdot 500 \text{ ns} = 50 \mu\text{s}$ . Considering typical decoherence times  $T_2 = 28 \text{ ms}$  and relaxation times  $T_1 = 1 \text{ s}$ , this readout can be achieved in a fraction of the overall decoherence time and faster than the error rates that occur due to  $T_1$ , which are about  $e^{-N \cdot \tau / 2 \cdot T_1}$  in the proposed time-multiplexing scheme. The resulting error induced by relaxation and decoherence would be smaller than 0.1%, and also better than current state-of-the-art readout fidelity for spin qubit dispersive sensing at microwave frequencies.

One can then assume that the reflected power received at the input of the receiver  $P_r$  is  $-118 \text{ dBm}$ , that is,  $1.58 \text{ fW}$  for  $50 \Omega$  impedance. In order to achieve the previously derived value of  $\text{SNR}_{\text{out}} = P_r/P_N = 100$ , the noise power  $P_N = k_B (T_{\text{sys}} + T_N) B_N$  should then be  $15.8 \text{ aW}$ , where  $k_B$  is the Boltzmann constant,  $B_N$  is the noise bandwidth, and  $T_{\text{sys}}$ ,  $T_N$  are the noise temperatures of the quantum device and the receiver, respectively. If the readout probing signal is gated, and the measurement time is  $\tau = 50 \mu\text{s}$ , then a noise bandwidth  $B_N = 1/(2\pi \cdot 50 \mu\text{s}) = 3.5 \text{ kHz}$  can be assumed. With such values, the overall noise temperature  $T_{\text{sys}} + T_N$  is found to be  $327 \text{ K}$ . Assuming an electron temperature  $T_{\text{sys}} = 100 \text{ mK}$  and small losses between quantum device, resonator,

and receiver, the target receiver noise temperature must be better than or equal to  $T_N = 326$  K. This corresponds to a noise factor  $F = 1 + T_N/T = 2.1$  with a reference temperature  $T = 290$  K, according to the IEEE definition, and to an NF of 3.3 dB. Finally, the LNA determines the overall receiver NF if it has sufficient gain.

3) *Gain and Linearity*: The system is supposed to operate with  $\sim -100$ -dBm input signals, so an overall gain in excess of 70 dB is required to amplify the signal to a level suitable for room temperature readout. In order to suppress the noise from all the stages following the input amplifier, the gain is distributed to 40-dB RF gain in the LNA and  $>30$  dB in the mixer and IF amplification chain. A limited IF gain also helps to avoid oscillations.

Considering the linearity, since the probing signal is  $\sim -100$  dBm, assuming the worst input return loss is  $\sim -6$  dB, the average input signal power is  $\sim -106$  dBm. If then a multi-tone received signal is taken into account, with a peak-to-average power ratio (PAPR) of  $\sim 11$  dB [32], then an input-referred 1-dB compression point ( $P_{1dB_{in}}$ ) for strong signals of  $-85$  dBm is desired, allowing enough margin. Considering a frequency-multiplexed readout of the qubits, multi-tone reflected signals are seen at the input concurrently, so the third-order intermodulation distortion signal power at the output of the receiver should be lower than the noise floor. For the input-referred third-order intercept point (IIP3), which indicates the weakly nonlinear behavior of the receiver, it is set to  $\sim -70$  dBm to satisfy the requirements.

4) *LO Specifications*: The frequency tuning range (FTR) of the oscillator is planned to be around 10–16 GHz, thus, after a divider by 2, 5–8-GHz quadrature signals can be obtained. This is necessary to perform high-side down-conversion. A wideband LO can be used to tune the LO in a sliding-IF scheme to read out sequentially more qubit matrices tuned at different frequency bands and with the same frequency separation  $B_{IF}$ . In addition, to generate wideband multi-carrier qubit probing signals, a large FTR for the LO signal is also required. To distinguish the  $\phi_R$  variation ( $\Delta\phi$ ) of the reflected signals under different quantum states, the phase noise (PN)  $L(\Delta f)$  of the LO signal should satisfy [3]

$$\beta_\phi(^{\circ}) \approx \frac{180^{\circ}}{\pi} \sqrt{2 \int_{f_a}^{f_b} L(\Delta f) d\Delta f} < \Delta\phi \cdot \lambda \quad (2)$$

where  $\lambda < 0.2$  to prevent the phase demodulation error from influencing the demodulation of the APSK signal. The lower integration bound  $f_a$  is set by the total readout time ( $f_a = 1/(2\pi \cdot N \cdot \tau) = 260$  Hz here), and the higher limit  $f_b$  is determined by the channel bandwidth (5 MHz, since the PN integral is single-sided). The in-band PN close to the carrier of a locked PLL is dominated by the CP, phase-frequency detector (PFD), and the reference. For a well-designed PLL under locked status, it can be considered almost constant with small ripples versus offset frequency [3]. The out-of-band noise is determined by the VCO, and it has a dependence  $\propto 1/\Delta f^2$ . By considering a PLL bandwidth of 0.2 MHz and  $\Delta\phi = 5^{\circ}$ , the in-band PN should be  $< -93.5$  dBc/Hz, and the 1-MHz offset PN should be  $-113.9$  dBc/Hz. So, the PN target

for the VCO is set as  $-115$  dBc/Hz at 1-MHz offset frequency, with enough margin. Note that, if the receiver and the multi-carrier signal generator share the same LO, the PN should be improved  $\sim 6$  dB with respect to the above specifications.

5) *Power*: The circuit is designed to operate at cryogenic temperatures,  $\sim 4$  K, where cooling budgets are limited (e.g., a typical dilution refrigerator  $\sim 4$  K stage has a 1.5-W power budget). Consequently, the overall power consumption for the receiver is set to a target of  $\sim 100$  mW ( $<10\%$  of total power budget), in which the LNA will dissipate about 50 mW alone due to the low NF requirement. This is considered as a reasonable requirement for a proof-of-concept design, but for larger highly-scaled systems, a stricter constraint should be required.

#### IV. CRYOGENIC CMOS CIRCUIT DESIGN

The receiver needs to satisfy the described functionality and specifications at cryogenic temperature. Standard process design kits (PDKs) do not provide device models at 4 K, so parameters need to be adapted for cryogenic operation. Before proceeding with the design, we performed a first rough characterization of the behavior of transistors [16] and passives [17] at cryogenic temperature and we created simple modified PDK models to guide the design. Such models can capture the basic transistor behavior but are not yet complete as they do not cover RF or noise performance.

As shown in Fig. 3(a), the reflected signals from the quantum devices are amplified by an LNA and converted to differential signals with a transformer-based balun to drive  $I/Q$  differential Gilbert cell mixers. Differential signaling is used since the signal is very small and can, therefore, be easily corrupted by interference and noise, even within the same chip. With the help of an LPF and a three-stage  $RC$  poly-phase filter ( $RC$ -PPF), the noise of the image signal is suppressed. Then, five-stage IF amplifiers are used to boost the amplitude further. The differential and quadrature LO signals are provided by a current-mode logic frequency divider (CML-FD) following the VCO. As discussed in Section II, the readout frequency of the system is proposed to be around 6 GHz. Therefore, the LNA is designed to operate in the 4.5–8.5-GHz band, and also the LO frequencies ( $f_{LOI}$ ,  $f_{LOQ}$ ) are tunable between 5 and 8 GHz, since the VCO FTR is 10–16 GHz ( $\sim 46\%$ ). The IF is planned to be between 0.1 and 1.5 GHz to avoid the effect of increased flicker noise at cryogenic temperatures. The cutoff frequency of the LPF and  $RC$ -PPF in this design is set to  $\sim 1.8$  GHz, which could be extended by adding more stages or using a tunable  $g_m$ -C PPF [33].

##### A. Low Noise Amplifier

The structure of the LNA, which has been discussed in detail in [30], is shown in Fig. 4. Here, we adopted the inductively degenerated common-source architecture with transformer-based  $LC$ -tank as the input low noise stage, instead of the resistive feedback or load structures, to achieve sub-1-dB NF at room temperature such that a  $<0.5$ -dB NF at cryogenic temperature (4 K) can be expected. The gain of the receiver has been carefully distributed. The LNA needs to provide

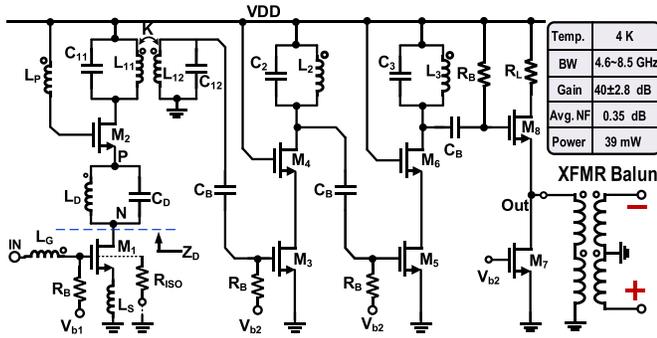


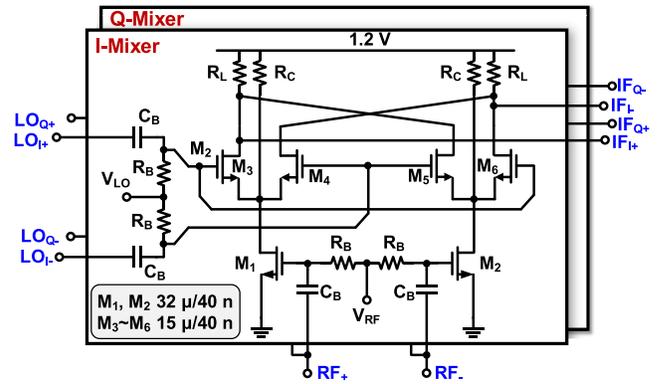
Fig. 4. Cryogenic CMOS LNA schematic and performance summary.

enough gain, which is set to  $\sim 40$  dB, to lower the gain requirement of the IF amplifiers since a too large gain of IF stages can easily cause instability at low frequency (tens of MHz) due to their low-pass property. Hence, in addition to the first low-noise stage (1st stage) with  $\sim 10$ -dB gain, two additional gain stages implemented by LC-tank loaded cascode structures are included to provide an extra  $\sim 30$ -dB gain. To achieve both input noise matching and impedance matching, the capacitive load technique is applied to the design of the 1st stage. The capacitive load is implemented by adding an LC-tank ( $L_D$  and  $C_D$  are resonant at  $\omega_d$ ) at the drain of  $M_1$ . The optimum noise impedance  $Z_{opt}$  is first matched by adjusting  $L_G$ ,  $L_S$ , and the transistor parameters. Then,  $S_{11}$  is optimized by tuning  $C_D$  and  $L_D$ . The gate inductance of the cascode stage is then added to decrease the noise contribution of  $M_2$  caused by the parasitic capacitance at the source of  $M_2$ . The LNA has been designed using the PDK room temperature models first; then, the parameters of the circuit were adjusted according to the cryogenic models of the key devices extracted by measurements, to make sure the LNA can operate well at cryogenic temperatures. In general, the frequency will be shifted up about 8% from room temperature to 4 K due to the decrease of the transistor parasitic capacitance and the decrease in the inductance of the LC-tanks. The measurement results of the standalone LNA at 4.2 K show 40-dB gain between 4.6 and 8.5 GHz and an NF as low as 0.3 dB with 39-mW power consumption, under a voltage supply of 1.4 V (70% of the power is consumed by the 1st stage).

To convert the single-ended LNA output to differential, to drive the differential inputs of the transconductance stage in the Gilbert cell mixers, a transformer-based balun is designed and an output source follower is used to match the low input impedance of the balun. The measured S-parameters of the balun at 4.2 K show  $\sim 1.3$ -dB insertion loss.

### B. Quadrature Gilbert Cell Mixer

An active Gilbert cell mixer is used in this design to downconvert the RF to IF. An active mixer is chosen to have additional gain in the RF-to-IF down-conversion (at least 6–7 dB to cancel the loss of the subsequent PPF) and improved LO-RF isolation (to mitigate LO kickback to the input) with respect to a passive switching mixer, while providing enough gain and RF-LO isolation. At cryogenic temperatures, the

Fig. 5.  $I/Q$  Gilbert cell active mixer.

threshold voltage of MOS transistors increases by a difference  $\Delta V_{TH}$  of about 0.15 V [16]. Hence, the voltage headroom at cryogenic temperature is reduced by  $N \cdot \Delta V_{TH}$  for structures with  $N$  gate-source stacks and the employed biasing scheme. As shown in Fig. 5, pseudo-differential input transconductance ( $G_m$ ) cells are used in this design to save voltage headroom by a  $V_{dssat}$  compared to the fully-differential counterpart, so the mixer power supply can be set to 1.2 V while still achieving  $\sim 0.4$ -V peak-to-peak headroom at room temperature to avoid compression. Static current bleeding resistors ( $R_C$ ) are applied to reduce the current flowing into the switching quad ( $M_3$ – $M_6$ ), so as to decrease their flicker noise contribution [34] while increasing the output voltage headroom further. The current division and the mixer conversion gain can be, respectively, expressed as

$$X_1 = \frac{i_{R_L}(t)}{i_{R_C}(t)} \cong \frac{R_C}{R_C + \frac{1}{g_{M_3}(t)} + \frac{1}{g_{M_4}(t)}} \quad (3)$$

$$A_{MIX} \cong \frac{C_B}{C_{GS,M_1} + C_B} g_{M_1} X_1 R_L. \quad (4)$$

The mixer gain is designed as 6 dB with  $X_1 \sim 0.5$  under a bias current of 1.5 mA in this design. The output LPF is designed without using additional components or blocks by co-designing the output stage of the mixer (with its load resistance) and the frequency-dependent input impedance of the subsequent PPF (set by the  $R_i$  and  $C_i$  component values chosen by design) to create a loaded output RC LPF with a 3-dB cutoff frequency of 1.8 GHz.

### C. PPF and If Amplifiers

The  $I/Q$  mixer is followed by a complex passive RC-PPF, whose goal is to suppress the noise of the image band falling into the gain band after down-conversion. Here, the complex filter was designed in the analog domain (by PPF) instead of the digital domain to save power. This also helps to reduce the overall system noise when the IF band is further downconverted in the digital domain. The PPF is designed to achieve at the same time  $\sim 2$ -GHz bandwidth and at least 20-dB IRR.

The filter is designed as a type-I three-stage RC filter for maximum bandwidth, as shown in Fig. 6, and following

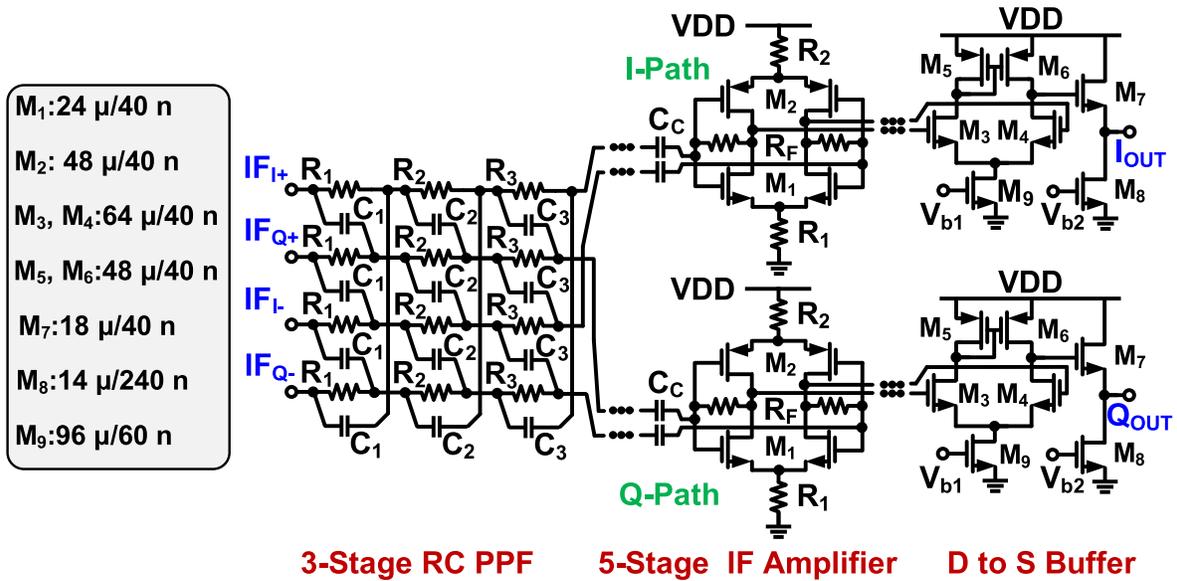


Fig. 6. IF signal chain of the receiver, showing the three-stage RC-PPF, the  $I/Q$  IF amplifiers, and the output buffers.

the design strategy in [27], the poles are chosen to be at  $f_{p1} = -1.607$  GHz,  $f_{p2} = -803$  MHz, and  $f_{p3} = -268$  MHz. By considering the filter input and output impedances, respectively, the output impedance of the mixer output buffer (150  $\Omega$ ) and the input impedance of the IF amplification chain (3 k $\Omega$ ), the component values are determined to be  $C_1 = C_2 = C_3 = 110$  fF for capacitors, while  $R_1 = 900$   $\Omega$ ,  $R_2 = 1800$   $\Omega$ , and  $R_3 = 5400$   $\Omega$  for resistors. The components are chosen to have the same capacitor value, while resistors are designed to achieve increasing impedance levels along the chain and balance wide relative bandwidth with sufficient image rejection. In this design, polysilicon resistors and metal-oxide-metal (MoM) capacitors are used to realize the PPF. It has been verified by measurements that the polysilicon resistors show good temperature stability ( $<10\%$  for 160- and 40-nm CMOS processes) when temperature decreases from 300 to 4.2 K [3], [35], while MoM capacitors increase their value  $\sim 5\%$  at 4.2 K [17], consequently the variation of the three poles of the three-stage PPF at cryogenic temperature will be small.

After the PPF, a chain of separate  $I$  and  $Q$  amplifiers is used to magnify the IF signal. This is designed as a five-stage chain to achieve  $\sim 30$ -dB gain with 1.5-GHz  $-3$ -dB bandwidth. The stages, shown in Fig. 6, are pseudo-differential inverter-based amplifiers with resistive feedback ( $\sim 5$  k $\Omega$ ), including common mode resistors ( $\sim 100$   $\Omega$ ) to supply and ground to improve the common-mode rejection ratio ( $>30$  dB), thus helping to reject the common-mode LO leakage from the mixer. This structure is used to achieve a tradeoff between bandwidth and gain, exploiting the feedback resistor to create a distributed gain-bandwidth product, by choosing a scaled-up gain in the subsequent stages, while the inter-stage bandwidth is determined by a controlled output RC time-constant. Since the transistor capacitances ( $C_{gs}$  and  $C_{gd}$ ) are expected to decrease by  $\sim 35\%$  at cryogenic temperatures [18], the RC time constant is decreased. Therefore,

the bandwidth of the IF chain is expected to be improved accordingly.

Finally, a buffer is included at the  $I/Q$  output, to achieve both the function of differential to single-ended (D-to-S) signal conversion and 50- $\Omega$ -impedance matching for testing. The D-to-S conversion is achieved by a five-transistor operational transconductance amplifier (OTA), which is used to take the difference of the  $+$  and  $-$  signal in current at the output node (to avoid signal loss), while 50- $\Omega$  output impedance is achieved by means of a properly sized and biased source follower (Fig. 6). Considering the  $-100$ -dBm input signals and the average 65-dB gain in the receiver, the  $-35$ -dBm output signal level is considered to be small enough for the common drain to maintain its small-signal 50- $\Omega$  output impedance. Moreover, at cryogenic temperature, the designed output impedance is ensured to be kept around the 50- $\Omega$  design value by controlling the bias of the current source transistor  $M_8$  through the external bias voltage  $V_{b2}$ , thus regulating the transconductance of the common-drain transistor  $M_7$ .

#### D. Push-Pull Mode-Switching VCO

The proposed LC-tank VCO in the PLL is shown in Fig. 7. The flicker noise of a transistor increases  $\sim 10\times$  when temperature decreases from room temperature (RT) to cryogenic temperature (CT), i.e., 4.2 K [36], which may cause considerable degradation of PN in the  $1/f$  noise region of the VCO. Thus, the PMOS-NMOS-complementary architecture is adopted to lower the flicker noise thanks to the use of the PMOS transistors [37], whose flicker noise is one or two orders of magnitude lower than the NMOS counterpart [38]. To achieve a wideband tuning range (10–16 GHz), the mode-switching technique is applied to this design [39]. In general, a mode-switching VCO requires two independent oscillating cores, which means the power consumption will be doubled. To circumvent this issue, a dual-mode LC-tank based on a switchable-inductor is inserted between the

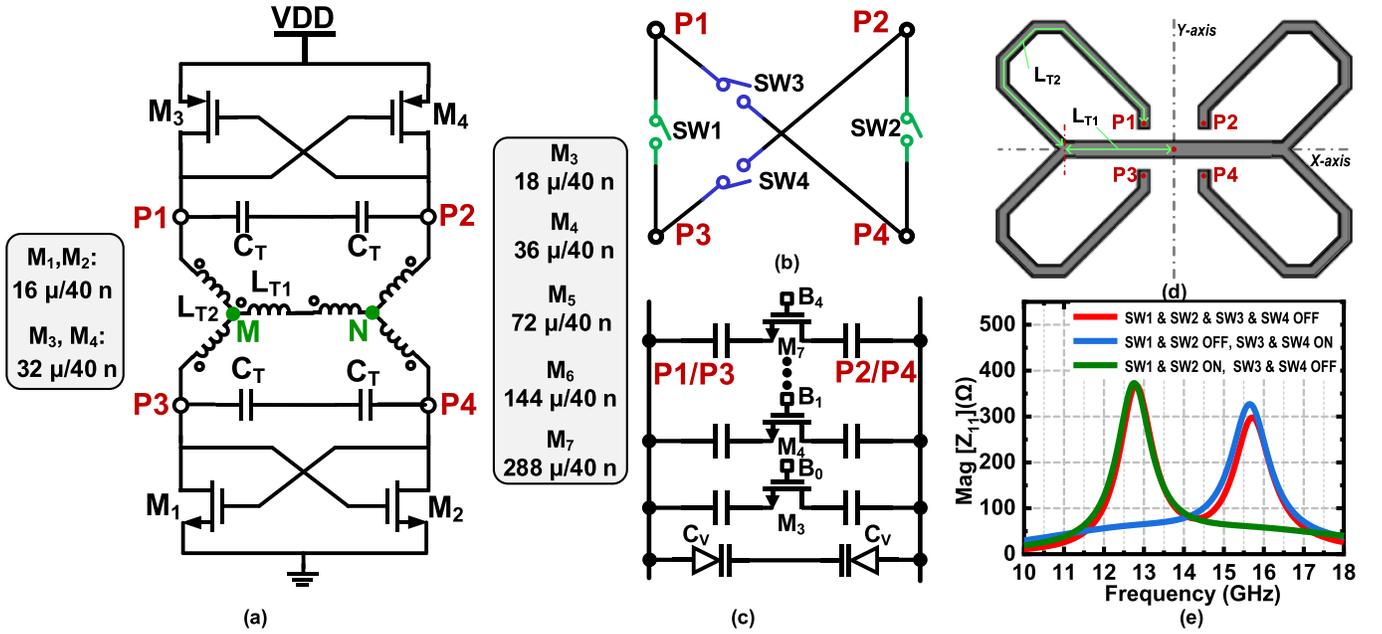


Fig. 7. Proposed mode-switching push-pull VCO: (a) circuit schematic and topology of the VCO; (b) configuration of common-mode switches; (c) switched-capacitor bank and varactors for frequency tuning under different oscillation modes; (d) layout and footprint of the multiarm switchable inductor; and (e) input impedance of the dual-mode LC-tank under different configurations of the common-mode switches.

NMOS cross-coupled transistors ( $M_1/M_2$ ) and the PMOS cross-coupled transistors ( $M_3/M_4$ ), as illustrated in Fig. 7(a), so to reuse the static current. Each of the two cross-coupled pairs is loaded by one of the two ports of the dual-mode resonator, respectively. Four switches  $SW_1$ – $SW_4$ , implemented by PMOS transistors, are used for mode-selection between Mode L and Mode H, to realize band switching of the VCO [Fig. 7(b)]. This will not deteriorate the PN since the voltage at the nodes connected by the switches in the ON-state will always be in-phase. When  $SW_1/SW_2$  are ON and  $SW_3/SW_4$  are OFF, the common-mode inductor  $L_{T1}$  is involved in the resonance, with a resonant frequency

$$f_L = \frac{1}{2\pi\sqrt{2C_T(L_{T1} + 0.5 \cdot L_{T2})}}. \quad (5)$$

When  $SW_3/SW_4$  are ON and  $SW_1/SW_2$  are OFF,  $L_{N/T1}$  is located in the common-mode plane and will only serve as the dc voltage supply line ( $M/N$  are virtual ground nodes). Then, the resonant frequency increases to

$$f_H = \frac{1}{2\pi\sqrt{C_T L_{T2}}}. \quad (6)$$

$L_{T1}$  is set as 0.13 nH, while  $L_{T2}$  is set as 0.285 nH to obtain  $f_H - f_L = 2.75$  GHz. The coarse frequency tuning is fulfilled by a symmetrical 5 bit ( $B(4:0)$ ) switched capacitor bank, as illustrated in Fig. 7(c), whose minimum capacitor  $C_0$  is 18 fF. In our design, we set the large NMOS transistor sizes (18–288 μm) of the switches in the capacitor banks to achieve a higher  $Q$ -factor while relying on the mode-switching operation of the VCO to widen the FTR ( $\sim 48\%$  with 25% for each mode), which is necessary due to the low PN demands of the quantum application. Small MOS varactors are used for fine frequency tuning, with a control sensitivity of 175 MHz/V.

The layout of the switchable inductor is shown in Fig. 7(d) (modified from [40]), where the two adjacent  $L_{T2}$  inductor arms are designed to be orthogonal to each other to decrease the coupling between them, which will enhance the equivalent  $Q$ -factors [41]. The simulation of the input impedance of the dual-mode resonator under different switch configurations is illustrated in Fig. 7(e), where the slight frequency discrepancy is caused by the different  $SW_1$ – $SW_4$  configurations.

Ideally, a 3-dB PN enhancement can be gained for the dual-core mode-switching VCOs compared with the free-running single core oscillators since the synchronous behavior between the two cores makes the oscillation phase more stable [42]. The PN enhancement will decrease by a factor  $30 \cdot \log(X)$  in the presence of frequency mismatch  $\Delta f$  of the two oscillating cores [43], where

$$X = \left[ 1 + \frac{1}{r} - \frac{\sqrt{1 - (Q \cdot K \cdot r)^2}}{r} \right]^{-1} \quad (7)$$

$r$  is the ratio of the switch ON resistance ( $R_{ON}$ ) of  $SW_1$ – $SW_4$  and the tank equivalent resistance  $R_P$  ( $r = R_{ON}/R_P$ ), and  $K$  is the ratio of the frequency mismatch  $\Delta f$  and the central oscillation frequency  $f_0$  ( $K = \Delta f/f_0$ ), while  $Q$  is the tank  $Q$ -factor. In this design,  $R_{ON} = 100 \Omega$  with  $r = 0.25$ , so using  $Q = 16$  and a maximum  $\Delta f = 120$  MHz (obtained by Monte Carlo analysis),  $30 \cdot \log(X) = 0.65$  dB. At 4.2 K, the  $Q$ -factor of the LC-tank increases by  $2.5\times$  and the mismatch of the frequency increases by  $\sim 1.2\times$  [19]; thus, the PN improvement becomes  $30 \cdot \log(X) \approx 0.5$  dB.

The PN measurement results of the proposed standalone VCO at a typical frequency ( $\sim 12.7$  GHz) are illustrated in Fig. 8(a) at 295 and 3.5 K. As can be seen, the PN close to the carrier is deteriorated by 3.5 dB at 3.5 K against 300 K due to the increase of  $1/f$  noise. This degradation is about

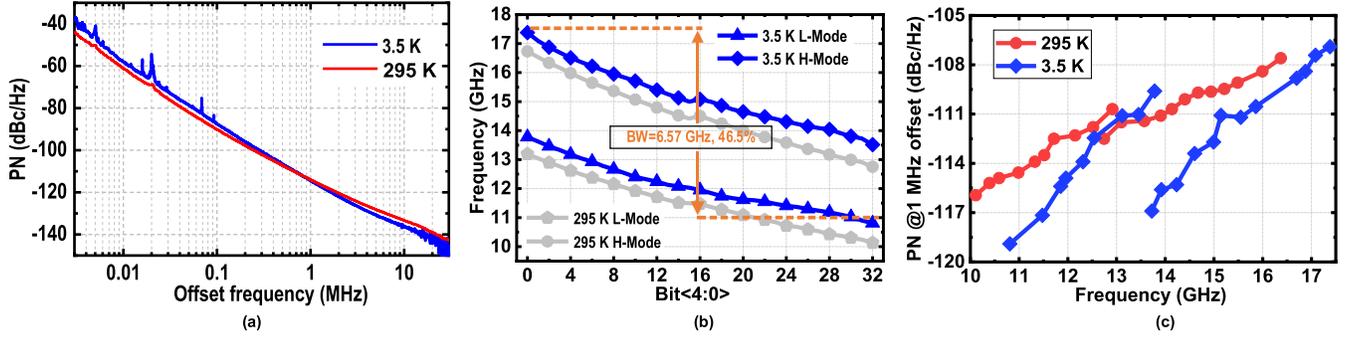


Fig. 8. Measurement results of the VCO: (a) PN at 12.7 GHz; (b) FTR at 295 and 3.5 K; and (c) PN at 1-MHz offset frequency in the FTR.

5 dB smaller compared with the NMOS-based *LC*-tank VCO in [3] thanks to the use of PMOS transistors. The FTR is also measured at 295 and 3.5 K [Fig. 8(b)], and the VCO achieves a 46.5% FTR from 10.8 to 17.3 GHz at 3.5 K. The measured PN at 1-MHz offset in the FTR is plotted in Fig. 8(c). We can also observe that deterioration of PN at CT ( $\sim 10$  dB) with frequency is more severe. This is because the flicker noise corner is larger than 1 MHz, which means flicker noise up-conversion contributes more PN at CT. The figure-of-merit (FoM) of the designed VCO is better than the cryo-CMOS VCO in [3]. When compared to the state-of-the-art room temperature VCOs [39], [44], [45], our VCO also has competitive performance in terms of power consumption, FTR, and PN.

### E. Charge Pump Phase-Locked Loop

The frequency synthesizer provides the LO signals ( $\sim 6$  GHz) to drive the two Gilbert cell mixers of the quadrature demodulator. The output differential signals of the VCO ( $\sim 12$  GHz) are first divided by a CML-FD [Fig. 9(a)]. The minimum peak-to-peak voltage swing in the FTR of the VCO is around 0.6 V, and when accounting for the insertion loss of the routing connections, the minimum input amplitude ( $A_{IN}$ ) for the CML-FD can be as low as 0.4 V. The CML-FD locking-range is sensitive to the impedance of the output nodes ( $R_{DL}$  and  $C_{DL}$ ), the transconductance of  $M_1$  and  $M_4$  in the VCO, and  $A_{in}$ . Enough margin ( $\sim 25\%$ ) for the locking range needs to be considered for cryogenic operation due to the increase of  $V_{th}$  and mismatch at low temperature [19], which inevitably increases power dissipation. Therefore, inductive peaking ( $L_{DL}$ ) is adopted as a technique to make the locking range of the divider robust at cryogenic temperature at the cost of increased area, but without current increase ( $I_D$ ). The locking range of the CML-FD is determined by [46]

$$G_N(1 + X \cdot e^{j\phi} - X^2)(j\alpha + 1) = \left( j\omega C_{DL} + \frac{1}{R_{DL} + j\omega L_{DL}} \right) \quad (8)$$

where  $X = G_C A_{IN} / 4I_D$ ,  $\alpha = G_D / G_N$ , and  $G_C$ ,  $G_D$ , and  $G_N$  are the transconductances of  $M_C$ ,  $M_D$ , and  $M_N$ , respectively.  $\phi$  is the phase shift between the input and output signals (it can be any value). The simulated sensitivity curve of the 1st CML-FD is shown in Fig. 9(b), thus showing that the

self-oscillation frequency is  $\sim 14$  GHz, while the locking range under  $A_{IN} = 0.4$  V is 6.2–20 GHz and the power consumption is  $\sim 6$  mW.

The pre-scaled signals are further divided by another two CML-dividers obtaining  $\sim 1.5$ -GHz signals, which can be readily handled by the digitally programmable frequency divider (DPFD). As illustrated in Fig. 9(c), the DPFD is designed with five stages of dual-modulus cell divider cells ( $2/3$  cells) [47]. The DPFD can realize an integer division from 32 ( $P_0-P_4$  are “0”) to 63 ( $P_0-P_4$  are “1”). At cryogenic temperatures, the transistor capacitances ( $C_{gs}$  and  $C_{gd}$ ) decrease, so the frequency handling of the DPFD increases.

The PFD is implemented by resettable D flip-flops with their  $D$  inputs set to logical high [Fig. 10(a)]. Proper delay cells ( $\sim 110$  ps) have been designed for the PFD to reset the path to mitigate the dead-zone problem. The output of the PFD drives a differential CP, as shown in Fig. 10(b). The output spurs of the PLL increase with the phase offset of the CP, which is expressed by

$$\Phi_E = 2\pi \frac{\Delta T_{ON} |I_{UP} - I_{DN}|}{T_{REF} I_{CP}} \quad (9)$$

where  $\Delta T_{ON}$  is the dead-zone time of the PFD,  $T_{REF}$  is the period of the reference clock,  $I_{CP}$  is the bias current of the CP, and  $|I_{UP} - I_{DN}|$  is the mismatch of the “UP” and “DOWN” currents. The current mismatch becomes worse at cryogenic temperature. To mitigate the mismatch, first, a relatively high  $I_{CP}$  ( $\sim 0.1$  mA) is set. Second, double replica current mirrors ( $M_3/M_7$  and  $M_4/M_6$ ) are adopted to reduce the mismatch caused by the PMOS and NMOS [48]. Third, to eliminate the mismatch caused by charge-sharing, a differential CP structure is employed and a unity-gain buffer is connected between the differential outputs of the CP (nodes A and B) to synchronize their common-mode voltages [49]. However, the time delay of the voltage follower reduces the effect of synchronization. Moreover, the behavior of the self-biased operational amplifier is hard to predict at cryogenic temperature, due to the threshold voltage variation. To make the minimization of the charge sharing effect at cryogenic temperature more robust, a dummy LPF is proposed at node A, similar to node B, at the cost of increased area.

As discussed previously, the close-in carrier PN increases at cryogenic temperature, thus raising the flicker noise corner of the VCO to a worst case  $f_{corner} \sim 1.2$  MHz. Therefore,

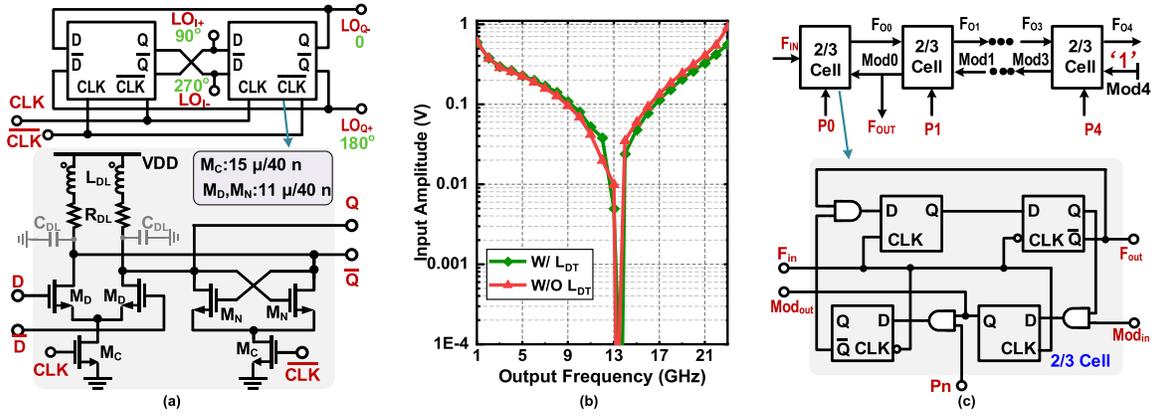


Fig. 9. Frequency dividers in the PLL: (a) CML-FD; (b) simulated sensitivity curve of the CML-FD; and (c) digitally programmable FD.

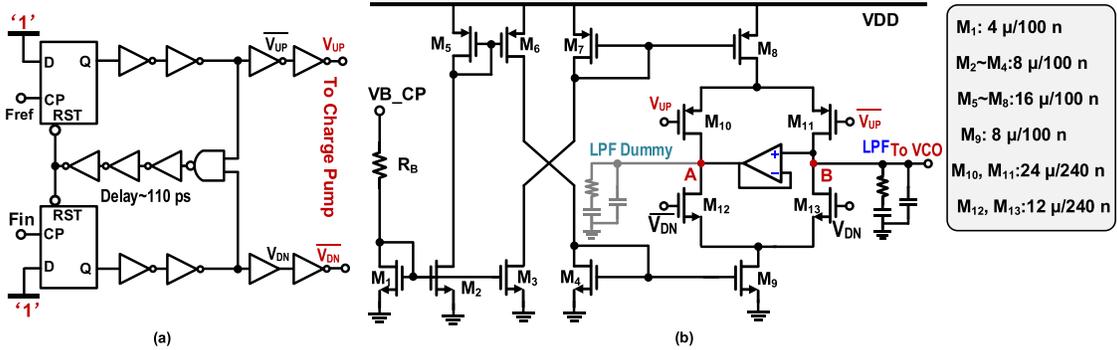


Fig. 10. (a) PFD and (b) proposed low mismatch CP.

the selection of the bandwidth of the loop filter ( $\omega_c$ ) is critical for cryogenic operation. In general, the loop bandwidth of a type-II PLL is restricted by Gardner's limitation ( $f_{REF}/10$ ) [50], to guarantee the loop stability. The natural frequency  $\omega_n$  and the damping factor  $\zeta$  for a type-II PLL are

$$\zeta = \frac{R_1 C_1}{2} \sqrt{\frac{I_{CP} K_{VCO}}{2\pi N(C_1 + C_2)}} \quad (10)$$

$$\omega_n = \sqrt{\frac{I_{CP} K_{VCO}}{2\pi N(C_1 + C_2)}} \quad (11)$$

The measured  $K_{VCO}$  at 3.5 K is  $\sim 175$  MHz/V at 12 GHz. A  $f_{REF}$  of  $\sim 50$  MHz is selected to lower the frequency division ratio ( $N$ ) and increase the CP feedback gain ( $\beta_n = I_{CP}/2\pi N$ ), so that the in-band noise contribution of the CP can be reduced [51]. Using  $\zeta \approx 0.86$  (to make the stability of the loop robust at cryogenic temperature),  $\omega_n \approx 1.88$  Mrad/s, the average  $N = (256 \cdot 464)^{1/2} \approx 345$ , one obtains  $R_1 \sim 45$  k $\Omega$ ,  $C_1 \sim 20$  pF, and  $C_2 = 0.1 \cdot C_1 = 2$  pF.

## V. MEASUREMENTS AND DISCUSSION

The proposed SoC is implemented in a standard 40-nm CMOS process, and its micrograph is shown in Fig. 11. The chip area is 2.8 mm<sup>2</sup>, including pads and decoupling capacitors, which occupy large portions of the die, since this is a pad-limited design, given the choice to have multiple external voltages for testing purposes. The chip is mounted on a printed

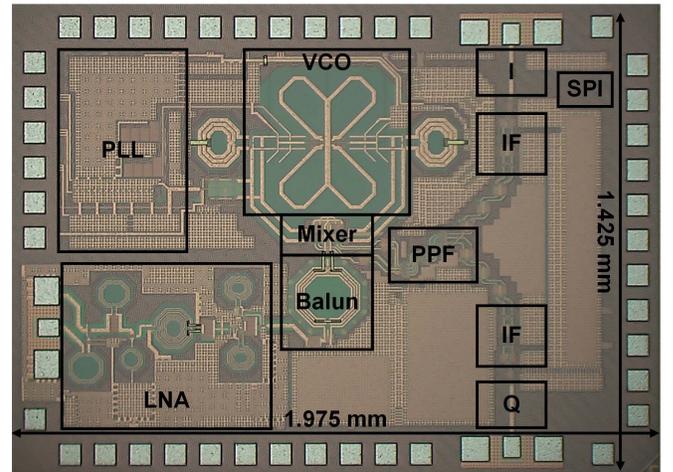


Fig. 11. Micrograph of the cryogenic CMOS receiver with PLL.

circuit board (PCB) for performance evaluation. As shown in Fig. 12, the bias voltages are provided via wire-bonding, and the input-output RF signals are measured through ground-signal-ground (GSG) probes, with preceding calibration. The chip is measured at 296 and 3.5 K in a Lakeshore CRX-4K cryogenic probe station.

First, the PLL is configured properly and tested. The serial peripheral interface (SPI) block is used to set the SW<sub>1</sub>-SW<sub>4</sub>,  $B <4:0>$ , and P<sub>0</sub>-P<sub>4</sub> bits to tune the output frequency at  $\sim 12.8$  and  $\sim 12.7$  GHz at 296 and 3.5 K, respectively.

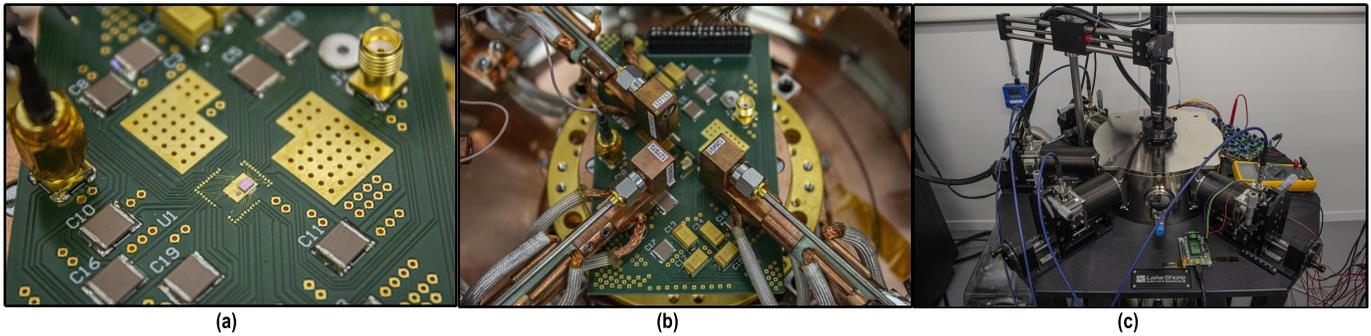


Fig. 12. Photographs of: (a) chip-on-board; (b) on-wafer testing with GSG probes; and (c) cryogenic probe station measurement setup.

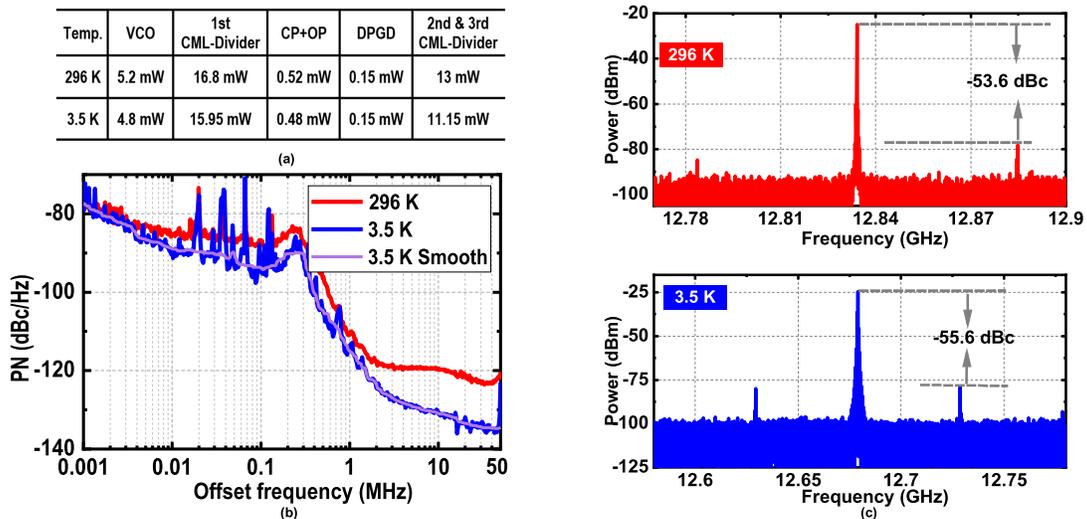


Fig. 13. (a) Power consumption; (b) PN; and (c) reference spurs measurements of the PLL at 296 and 3.5 K.

So, after the CML-FD, the quadrature output frequency  $\sim 6$ -GHz LO signals can be obtained. The bias conditions are slightly adjusted from room temperature to ensure that the PLL works properly at cryogenic temperature [Fig. 13(a)]. Fig. 13(b) and (c) shows the measured output PN and reference spur of the PLL using the Keysight signal analyzer N9030A, where the reference signal is  $\sim 50.4$  MHz provided by the signal generator Keysight E8267D. At 296 K, the measured in-band PN is  $-86$  dBc/Hz at 10-kHz offset and the out-of-band PN is  $-112$  dBc/Hz at 1-MHz offset [Fig. 13(b)]. The reference spurs are  $\sim -54$  dBc with respect to the carrier. At 3.5 K, the in-band PN is  $-90$  dBc/Hz at 10-kHz offset (5-dB enhancement from 296 K) and the out-of-band PN is  $\sim -114$  dBc/Hz at 1-MHz offset. The reference spurs are around  $-55.6$  dBc.

Then, the small-signal transmission and port matching performance are measured. At room temperature, the receiver shows  $\sim 60$ -dB gain. At 3.5 K, the circuit exhibits a 68-dB maximum conversion gain and a better than  $-10$ -dB input and output match, as shown in Figs. 14 and 15. The bandwidth is 1.4 GHz, between 100 MHz and 1.5 GHz of IF due to the chosen non-zero IF architecture.

To characterize the receiver linearity, the  $P1dB_{in}$  and IIP3 are tested. At a typical 670-MHz output frequency,  $P1dB_{in}$

is  $-76.5$  dBm at 3.5 K [Fig. 16(a)].  $P1dB_{in}$  is in the range  $-77.5$  to  $-72.5$  dBm in the operating frequency band at 3.5 K [Fig. 16(b)], which is much higher than the typical  $\sim -100$ -dBm input signal reflected by the qubits. IIP3 measurement results at 670-MHz output frequency are shown in Fig. 17(a), obtaining  $-68$  dBm at 3.5 K. The measured IIP3 is between  $-72$  and  $-63$  dBm in the operating band at 3.5 K [Fig. 17(b)]. The degradation of the linearity at cryogenic temperature is caused by the reduction of the bias current of the IF gain stages and the output buffer at 3.5 K.

The SSB NF is measured with a cold attenuator wire-bonded to the receiver input at 3.5 K, and Y-factor NF measurements are performed using the Keysight noise source N4002A and the Keysight signal analyzer N9030A. As shown in Fig. 18, the minimum NF is 0.55 dB, with degradation at low and high frequency, where the limited bandwidth of the PPF achieves less efficient image noise rejection. If compared to the NF of the LNA alone (0.3–0.7 dB in its bandwidth), the receiver shows a degradation that can be explained by a weaker than expected sideband rejection. Additional noise sources, external or coming from the co-operation with other blocks such as the PLL, could also result in additional noise. Given the stringent noise requirements for the readout of spin qubits, an additional cryogenic low noise preamplifier might still be

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON TABLE WITH STATE-OF-THE-ART

	This work	ISSCC 21 [14]	ISSCC 21 [15]	ISSCC 20 [12]	MWCL 20 [52]	RSI 14 [53]
Operating temperature	3.5 K	4.2 K	4 K	0.11 K	300 K	100 K
Qubit platform	Spin qubits, transmons	Spin qubits	Spin qubits	Silicon quantum dots	Si/SiGe spin qubits	N.A. (Radio astronomy)
Architecture	Intermediate IF I/Q receiver	Intermediate IF I/Q receiver	I/Q receiver	DC TIA readout	Intermediate IF I/Q down-converter	Discrete receiver
RF Frequency	5-6.5 GHz	6~8 GHz	DC-600 MHz	DC	240 GHz	0.4-3 GHz
Bandwidth	1.4 GHz	2 GHz	400 MHz	1.1 kHz	59 GHz	2.6 GHz
Gain	70 dB	58 dB	40-90 dB	<sup>a</sup> 11.3 M $\Omega$	23 dB	34 dB
S <sub>11</sub>	< -10 dB	N.R.	N.R.	N.A.	< -5 dB	N. R.
NF	0.55 dB	0.6 dB	0.61 dB	<sup>b</sup> 300 fA/ $\sqrt{Hz}$	24.5 dB	0.5 dB
IIP3	> -72 dBm ( $\Delta f=1$ MHz)	-50.8 dBm ( $\Delta f=50$ MHz)	N.R.	N.R.	N.R.	N. R.
P1dB <sub>in</sub>	> -77.5 dBm	-58.4 dBm	N.R.	N.R.	-27.3 dBm	N. R.
PN at 1 MHz $\Delta f$	-115 dBc/Hz	N.A.	N.A.	N.R.	-82 dBc/Hz	N.A.
On Chip I/Q LO	Yes, PLL	No	No	Yes, VCO	Yes, VCO	No
LO FTR	6.6 GHz (46.5%)	N.A.	N.A.	4 GHz	27 GHz	N.A.
Technology	40-nm CMOS	40-nm CMOS	22-nm FFL FinFET	28-nm FDSOI	55-nm SiGe	GaAs HEMT, discrete
Area	2.8 mm <sup>2</sup>	0.68 mm <sup>2</sup>	<sup>c</sup> 0.48 mm <sup>2</sup>	<sup>c</sup> 1.4 mm <sup>2</sup>	1.8 mm <sup>2</sup>	> 1 m <sup>2</sup>
Power	108 mW	66 mW	<sup>d</sup> 72 mW	295 $\mu$ W	859 mW	N. R.

<sup>a</sup> Transimpedance amplifier gain, <sup>b</sup> Input referred noise, <sup>c</sup> Estimated from chip micrograph, <sup>d</sup> Includes the probing signal generator.

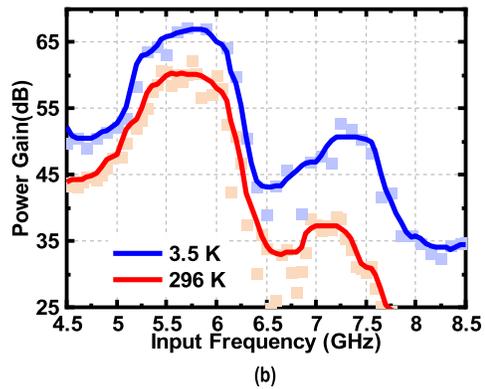
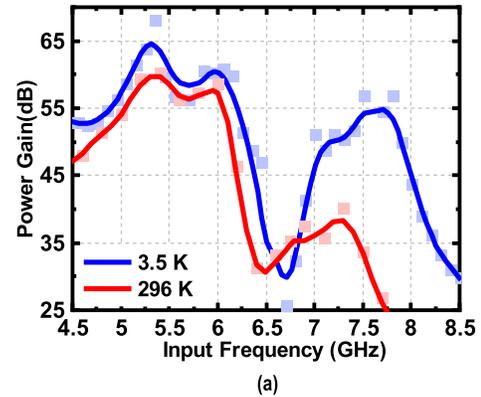
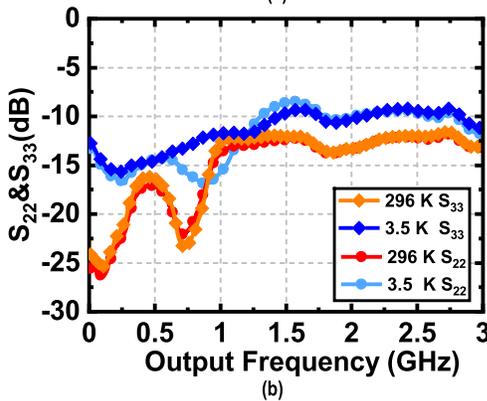
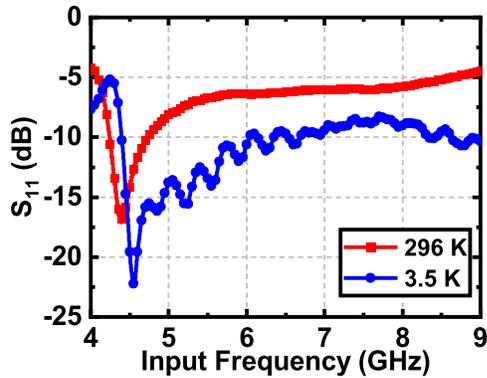


Fig. 14. Measured results for: (a)  $S_{11}$  and (b)  $S_{22}$  and  $S_{33}$  at 296 and 3.5 K.

Fig. 15. Measured conversion gain of: (a)  $I$  and (b)  $Q$  path.

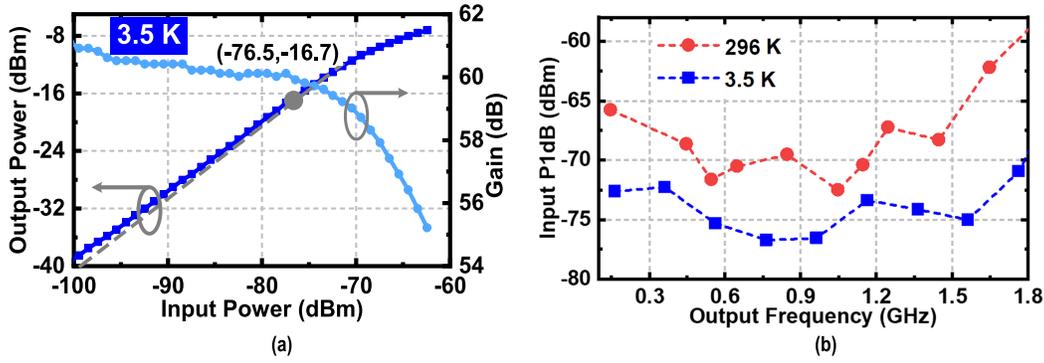
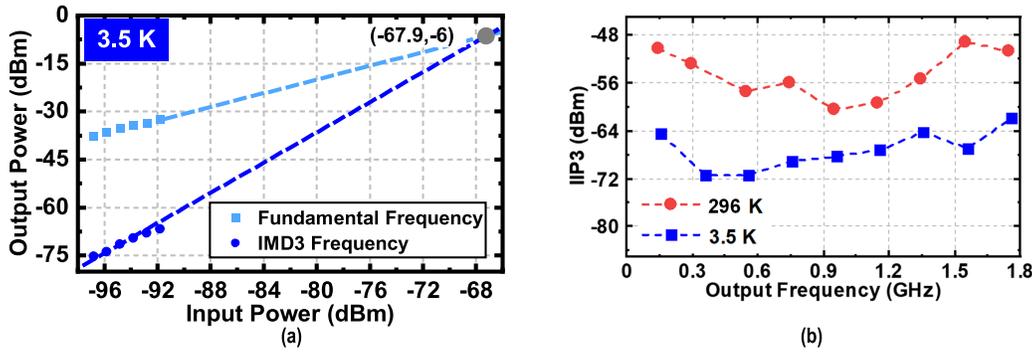
Fig. 16. P1dB measurement results with IF = 670 MHz: (a) at 3.5 K and (b) P1dB<sub>in</sub> versus output frequency IF.

Fig. 17. IIP3 measurement results with IF = 670 MHz: (a) at 3.5 K and (b) IIP3 versus output frequency IF.

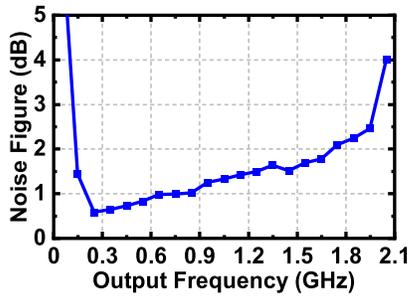
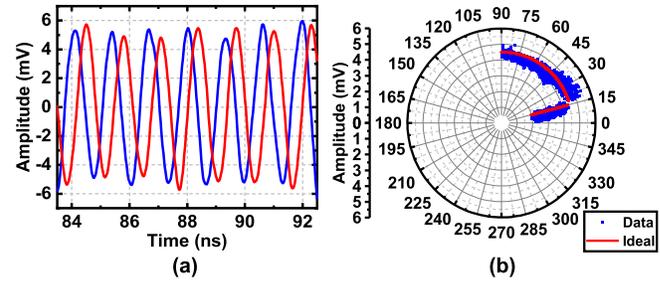


Fig. 18. Measured NF at 3.5 K.

Fig. 19. (a) Time-domain  $I/Q$  signals at 3.5 K and (b)  $I/Q$  output constellation plot for linear AM and PM input signals at 3.5 K.

required for direct readout. In this case, the use of an additional amplifier would increase the gain in front of the receiver, thus providing a larger input signal. In order for our receiver to keep meeting the linearity specifications, its gain would have to be reduced. This could be accomplished by reducing the gain of the on-chip LNA thanks to the external voltages  $V_{b1}$  and  $V_{b2}$  and the gain of the IF amplifiers by reducing the  $V_{DD_{IF}}$ . This would also result in degraded noise performance but with large power savings and assuming a high-gain external LNA in front, this would not pose a problem.

Finally, the time-domain performance is evaluated by acquiring the real-time  $I/Q$  output signals at 3.5 K, obtaining a phase imbalance of  $6^\circ$  [Fig. 19(a)]. The phase sensitivity is measured directly by sending a linear AM and PM signals at the input at 3.5 K, sampling the output  $I/Q$  waveforms and reconstructing the baseband signals off-chip at 296 K. As shown in Fig. 19(b), the receiver is capable of

downconverting the input signal, while the demodulated waveforms track amplitude and phase of the input signal in the  $I/Q$  plane at 3.5 K.

The overall circuit dissipates 108 mW with a 1.4-GHz bandwidth, and the power consumption of different blocks at 3.5 K is illustrated in Fig. 20. Considering the planned hybrid time- and frequency-multiplexed readout, with a 10-MHz resonator bandwidth, which allows qubit readout in the time domain faster than typical decoherence times, and 100-MHz spacing for each qubit, the proposed system should allow to read out up to  $N = 12$  qubits in frequency-multiplexing in a measurement time  $\tau = 50 \mu\text{s}$  and  $N^2 = 144$  qubits in a time  $N \cdot \tau = 600 \mu\text{s}$ , thanks to time-multiplexing, thus improving scalability. Table I summarizes the performance of the designed receiver and compares it with state-of-the-art.

As an application for the described receiver, the frequency multiplexed gate-based RF reflectometry readout of quantum

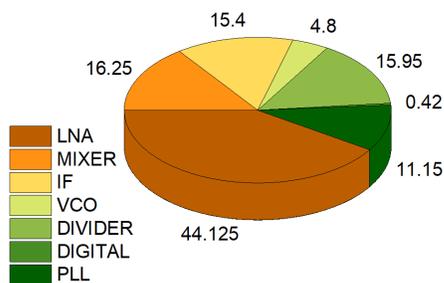


Fig. 20. Power consumption breakdown of the receiver at 3.5 K.

dots in the same 40-nm standard CMOS technology through fully-integrated high-frequency lumped-element  $LC$  resonators in the receiver band [24] is proposed. The combination of such platforms, thanks to its scalability, integration, and compactness, could form the basis for future silicon quantum computing systems. Moreover, since the operation frequency and the receiver analog/RF front-end for quadrature demodulation proposed for semiconductor qubits is similar to the architecture used for superconducting qubits, the chip proposed in this work is compatible with the readout of both spin and transmons. In the case of superconducting qubits, the frequency range is typically similar ( $\sim 6$  GHz), but quantum-limited amplifiers are used in front of the readout chain, thus lowering the noise temperature considerably. Moreover, considering that high-quality superconducting microwave resonators are typically used for dispersive readout of transmons, this would allow smaller qubit channel bandwidths, thus resulting potentially in a larger number of qubits addressed in frequency-multiplexing from the mere frequency spectrum perspective. In practice, however, the number of qubit channels is limited by the non-linearity of the parametric amplifiers in the front end.

## VI. CONCLUSION

A qubit RF-reflectometry readout chip including a cryo-CMOS  $I/Q$  receiver and frequency synthesizer is proposed in this work. The quantum information signals were modeled as APSK signals. Accordingly, the receiver architecture was presented and specifications were discussed. The receiver was designed to operate at deep-cryogenic temperatures. A sub-1-dB NF LNA, a current-bleeding quadrature mixer, and a type-II PLL with a proposed dual-mode VCO were designed with strict noise, power, and bandwidth constraints. The circuit parameters were set carefully for cryogenic application. The receiver was characterized at 3.5 K, and it showed wideband operation, thus allowing the multiplexed readout of tens of qubits with 108-mW power consumption in total. Therefore, this work represents a step toward a fully-integrated cryo-CMOS SoC for qubit readout and control.

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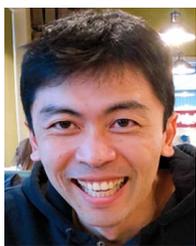
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