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Virtual Capacitor Concept for Partitioning of Large Converter Systems for RT-HIL Simulations

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Abstract—In this paper, the real-time simulation model of the modular multilevel matrix converter was split into three independent instances using the concept of virtual capacitance. In doing so, the number of state space matrices that define the system has been reduced significantly making it suitable for a small-scale real-time simulator, such as the RT Box. The verification of the proposed concept is done on a hardware-inthe-loop system compromising ten RT Boxes, where the physical model of the matrix modular multilevel converter is deployed, and control algorithms are implemented on the ABB PEC800 industrial controllers.

Keywords—Hardware-in-the-Loop, Real-Time Simulation, Matrix Modular Multilevel Converter, Pumped Hydro Storage Power Plants

I. INTRODUCTION

Real-Time Hardware-In-The-Loop (RT-HIL) simulations are widely recognized as a reliable method for verification of the control structures and algorithms. Generally, they include the tested controller interfaced to an RT computer aiming to provide results as close as possible to the real physical system. Especially for expensive and large power converters, such as the Matrix Modular Multilevel Converter (M3C), this verification process is crucial.

As seen in Fig. 1, the M3C comprises a series connection of cells each with its own capacitance, which connected together form a branch. The M3C requires Full Bridge (FB) cells as both positive and negative branch voltages are needed. The modularity of the M3C is achieved through the ability to connect an arbitrary number of cells to form a branch, thus resulting in the required voltage rating of a given application. In applications such as Pumped Hydro Storage Power Plant (PHSP), with a high power and voltage rating, the high number of cells connected per branch leads to a high number of voltage levels at the terminals of the converter, reducing the filtering requirements on the converter terminals and the low dv/dt reduces the stress on the machine winding insulation.

Before the deployment in the field, a thorough verification process of the expected converter operation is required to avoid damaging high value equipment. For application such as PHSP with custom designed equipment and high converter power ratings, this is especially important. Additionally, the Modular Multilevel Converter (MMC) topology, due to its series connection of cells, requires a complex control structure to maintain constant energy within the branches. An RT-HIL testing platform, simulating the power part of the converter while having the real control structure, ensures high fidelity results and is a common verification tool. While RT-HIL systems for the Indirect Modular Multilevel Converter (IMMC) have been described and used in several papers [1]–[8], the work on RT-HIL modeling of M3C is rather scarce.

Some RT-HIL systems, like the RT Box [9] or Typhoon HIL [10], use the state-space matrix representation to run converter and application real-time models. The number of matrices used for that matter depends, as will be explained shortly, upon the complexity of the employed model. Therefore, the converter model must be simplified to the highest possible extent without compromising its correctness.

For the converter comprising N switches, the number of possible states generated through different combination of switching states equals 2^N . For a converter consisting of N_{cell} FB cells (each one of the comprising 4 switches), the total number of switching states might result in overloading the employed real-time simulator. Therefore, the first model simplification lies in the use of sub-cycle averaged modeling of an M3C branch, which is thoroughly explained in [8], [11]. More details on this approach can be found in the next section.

However, even with the reduction of the number of switching states to $2^{(2 \times 9)}$, the simulator chosen for this work struggles to run the desired real-time model and this paper focuses on the way of circumventing this weakness. To reduce the dependency of the nine branches, and allow the deployment



Fig. 1. The matrix modular multilevel converter with the three subclusters, highlighted in gray, each containing three branches, highlighted in green, and N cells per branch. The two AC systems connected to the terminals are represented by a grid on the input side and a 3 phase machine on the output side connected to a pump/turbine as is the case in a PHSP.

on small-scale simulators, the concept of Virtual Capacitor (VC) and Virtual Resistor (VR), which is presented in this paper, is used and allows to split the M3C into 3 independent instances. Together with simplifications of the branch model, this split model reduces the number of state space matrices to a total of 3×2^6 irrespective of the number of cells per branch.

The paper is structured in the following way, section II presents the equivalent branch model as well as the splitting strategy of the M3C. Section III presents the tuning procedure of the VC and VR, and includes a mathematical verification of the operational principles of the simplified model. Section IV includes a description of the RT-HIL platform and the simulation results of the split M3C model, and section V concludes the paper.

II. REAL-TIME MODELING OF THE M3C

A. Branch equivalent model

The first step in the simplification process of the M3C aiming to reduce the number of state space matrices, is to reduce the number of switches. The simplifications should not alter or limit the operating modes of the converter. Additionally, the simplification should not be time-varying, as some real-time platforms do not support this (such as the RT-Box).

Conventionally, the MMC branch can be replaced by a single controlled voltage source, as is the case in [12] and [13]. While this model reduces the number of state space matrices significantly by eliminating all switches and allows an accurate simulation of the steady state operation, it fails to model the blocked state which is used during charging and faulty operation of the converter. An extension was proposed in [14], but the number of required switches not considered acceptable for real-time simulations. Due to their time-varying characteristic, the models used in [15] and [16] are not considered for this application.

With two diodes and two controlled voltage sources, the model as proposed in [17] and [18] ensures correct simulation of both blocked and active states of the converter. Figure 2(b) shows the equivalent time-invariant branch model comprising two diodes and two voltage sources. The voltage sources v_1 and v_2 represent a combination of both, the instantaneous cell capacitor voltage and the cell switching signal. The equivalent model of the converter using this branch simplification is shown in Fig. 3.

This simplification reduces the number of switches to two diodes per branch independently from the number of cells, thus



Fig. 2. Equivalent branch model for (a) the real converter using a cascaded connection of full bridge cells (b) the real time model using two controlled voltage sources and two diodes



Fig. 3. M3C model using a branch equivalent representation reducing the number of switches and making them independent from the number of cells per branch.

the number of state space matrices is significantly reduced from $2^{4 \times 8 \times 9} = 2^{288}$ to $2^{2 \times 9} = 2^{18}$. Nevertheless, the complexity of this model due to the high number of state space matrices, makes it unsuitable for the implementation on small scale simulators such as the RT Box, to the point of not even being able to load this configuration onto the RT Box (something observed in our initial modeling attempts). Further reducing the number of switches in the branch model results in a loss of various operation modes. To achieve a reduced number of state space matrices and making the model compatible with small scale simulators, the model of the M3C has to be decoupled. Consequently, the already simplified model requires additional splitting to further reduce the number of state matrices, which is achieved through the use of VCs and VRs.



Fig. 4. Example of circuit splitting, with (a) showing the initial circuit an arbitrary switching state and (b) the equivalent split circuit in the same switching state

III. VIRTUAL CAPACITANCE CONCEPT

Splitting a circuit in multiple independent systems while keeping the same functionalities, achieves a reduction in the simulation time step, through reducing the number of state space matrices defining the system. To illustrate the benefits, the concept of splitting a circuit into smaller independent circuits is demonstrated on the circuit shown in Fig. 4 using two FB cells with a common capacitance in an arbitrary switching stage. With eight switches, the initial system shown in Fig. 4(a) counts a total of 2^8 state space matrices, and the one defining the given switching state is expressed as:

$$\underbrace{\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{g1}} \\ v_{\mathrm{c}} \\ i_{\mathrm{g2}} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{L_{\mathrm{g1}}} & 0 \\ \frac{1}{C} & 0 & \frac{1}{C} \\ 0 & \frac{1}{L_{\mathrm{g2}}} & 0 \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_{\mathrm{g1}} \\ v_{\mathrm{c}} \\ i_{\mathrm{g2}} \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} \frac{1}{L_{\mathrm{g1}}} & 0 \\ 0 & 0 \\ 0 & -\frac{1}{L_{\mathrm{g2}}} \end{bmatrix}}_{B} \underbrace{\begin{bmatrix} v_{\mathrm{g1}} \\ v_{\mathrm{g2}} \end{bmatrix}}_{u}$$
(1)

An intuitive way of splitting this circuit is at the common capacitance, resulting in two individual circuits with each four switches, thus resulting in $N_{ss} = 2 * 2^4$ state space matrices. This corresponds to an 8-fold reduction in the number of state space matrices and results in a equivalent reduction ratio to the initially feasible simulation time step. The resulting state-space matrices of the split circuit in the same switching state is shown in Fig. 4 is:

$$\frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{g1}} \\ v_{\mathrm{c}} \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & -\frac{1}{L_{\mathrm{g1}}} \\ \frac{1}{C} & 0 \end{bmatrix}}_{A_{1}} \begin{bmatrix} i_{\mathrm{g1}} \\ v_{\mathrm{c}} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_{\mathrm{g1}}} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix}}_{B_{1}} \begin{bmatrix} v_{\mathrm{g1}} \\ i_{\mathrm{s}} \end{bmatrix}$$
(2)
$$\frac{\mathrm{d}i_{\mathrm{g2}}}{\mathrm{d}t} = \underbrace{\begin{bmatrix} 0 \\ A_{2} \end{bmatrix}}_{A_{2}} \begin{bmatrix} i_{\mathrm{g2}} \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_{\mathrm{g2}}} & -\frac{1}{L_{\mathrm{g2}}} \end{bmatrix}}_{B_{2}} \begin{bmatrix} v_{\mathrm{s}} \\ v_{\mathrm{g2}} \end{bmatrix}$$
(3)

Due to the introduced delay at the controlled current source, a small time step must be assured in order for the following approximation to hold: $i_s = i_{g2}[k-1] \approx i_{g2}[k]$. Fulfilling this condition, i_s in the first system can be replaced by the current flowing in the second system $i_{g2}[k]$. From the circuit shown in Fig. 4(b), it is straightforward that $v_s = v_c$, and with these equations fulfilled, it is obvious that the resulting state space matrix from the split circuit corresponds to the initial one.

A. Real-time modeling of the M3C

The splitting as illustrated in the example can not be applied to the M3C directly due to the lack of centralized capacitance. However, the RT-HIL platform is processing only virtual power, meaning that additional components can be added to the simulated model as long as this addition does not to alter the models behavior from a controller perspective. This means that the circuit shown on Fig. 3 can be extended with a set of VC and VR, and the result is shown in Fig. 5. With this addition, the subcluster 1 and 2 into can be separated into two structures separated from the main system. The branches that



Fig. 5. Final real-time suitable model of the M3C divided into five independent circuits. System 1 incorporates the virtual circuit as well as all nine branches where the first six are replaced with ideal current sources. System 2 and 3 are the separated circuit of the branches 1 to 3 and 4 to 6 respectively. System 4 is the three phase as grid input and system 5 while shown as three phase output grid can also be replaced with a three phase machine as would be the case for a PHSP.

constitute the separated subclusters can be replaced by current sources in the main system due to the series connection of a voltage source and an inductor.

The addition of the VCs and VRs connected as shown in Fig. 5 allows for an additional simplification, namely the separation of both the load and the grid from the branches of the M3C. Even if this additional separation does not reduce the number of state space matrices, it allows due to the separation of the ac grid and electrical machine, to reduce the size of the state space matrix, which allows a further reduction in simulation time step.

To prove the validity of this separation, the Kirchhoff voltage and current laws can be analyzed and compared to the initial equations resulting from Fig. 3. The following analysis holds for any of the nine branches, where x denotes the input phase, $x \in [A, B, C]$ and y the output phase $y \in [1, 2, 3]$.

$$u_{\rm xy} = u_{\rm x} + u_{\rm x0} - u_{\rm y} - u_{\rm y0} \tag{4}$$

From (4), combining u_{y0} and u_{x0} , the common mode voltage can be defined by $u_0 = u_{y0} - u_{x0}$.

The AC terminal currents from both the input and output terminals of Fig. 1 can be defined by:

$$i_{\mathbf{x}} = \sum_{\mathbf{y}} i_{\mathbf{x}\mathbf{y}} \quad \text{for } \mathbf{x} \in [A, B, C]$$
 (5)

$$i_{y} = \sum_{x} i_{xy}$$
 for $y \in [1, 2, 3]$ (6)

While it is obvious that (4) remains the same for the model with the virtual circuit shown in Fig. 5, (5) and (6) will be influenced by the addition of the virtual circuit.

$$i_{\mathbf{x}} = \sum_{\mathbf{y}} i_{\mathbf{x}\mathbf{y}} + i_{\mathbf{v}\mathbf{x}} \qquad \text{for } \mathbf{x} \in [A, B, C] \tag{7}$$

$$i_{y} = \sum_{x} i_{xy} + i_{vy}$$
 for $y \in [1, 2, 3]$ (8)

As previously mentioned, the RT-HIL system verifies control structure and algorithm, thus for the split model to be valid, it must be proven that from a controller point of view, the functionality of the converter remains unchanged, thus the following equations are verified (5) = (7) and (6) = (8). The high frequency components being filtered out in the control loop, the range of interest for analyzing the influence from a controller point of view lies in the nominal operating frequencies of the M3C. A small tolerance of 2% of the nominal current in the frequency range of interest is considered for the validation of the model.

The Kirchhoff voltage laws between subcluster 1 from Fig. 1 and system 2 Fig. 5 as well as subcluster 2 and system 3 must be equal, which leads to the equations:

$$u_{\rm vc_{1,2,3}} = u_{\rm A,B,C} - 0.5u_0 \tag{9}$$

$$u_{\rm vc_{4,5,6}} = u_{1,2,3} + 0.5u_0 \tag{10}$$

And using these equations in system 1, the analysis from the grid and the load side terminals can be done to prove equal terminal dynamics between the real and the split model:

$$u_{\rm g_{A,B,C}} - L_{\rm x} \frac{\mathrm{d}i_{\rm A,B,C}}{\mathrm{d}t} = \underbrace{\frac{u_{\rm eq_{A,B,C}}}{u_{\rm b_{1,2,3}} + u_{\rm b_{4,5,6}} + u_{\rm b_{7,8,9}}}_{3} + u_{0}}_{+ \frac{L_{\rm br}}{3} \frac{\mathrm{d}i_{\rm A,B,C}}{\mathrm{d}t}} (11)$$

With the same procedure, the expression of the ac output voltage can be developed:

$$u_{\mathrm{g}_{1,2,3}} + L_{\mathrm{y}} \frac{\mathrm{d}i_{1,2,3}}{\mathrm{d}t} = -\left(\underbrace{\frac{u_{\mathrm{b}_{1,4,7}} + u_{\mathrm{b}_{2,5,8}} + u_{\mathrm{b}_{3,6,9}}}{3} + u_{0}}_{-\frac{L_{\mathrm{br}}}{3}} \frac{\mathrm{d}i_{1,2,3}}{\mathrm{d}t} - \frac{1}{2} \right)$$

With both (11) and (12), an equivalent model of the analyzed M3C as seen from the input and output ac terminals can be developed. Thereafter, the dynamics of the M3C input and output ac currents can be described and compared to the dynamics of the initial model shown in Fig. 3 to validate the usage of the model shown in Fig. 5.

$$L_{\Sigma_x} \frac{di_{A,B,C}}{dt} = \frac{2u_{g_{A,B,C}} - u_{g_{B,C,A}} - u_{g_{C,A,B}}}{3} - \frac{2u_{eq_{A,B,C}} - u_{eq_{B,C,A}} - u_{eq_{C,A,B}}}{3}$$
(13)



Fig. 6. Illustration of the algorithm used to find the values of VC and VR

$$L_{\Sigma_y} \frac{\mathrm{d}i_1}{\mathrm{d}t} = \frac{2u_{\mathrm{g}_{1,2,3}} - u_{\mathrm{g}_{2,3,1}} - u_{\mathrm{g}_{3,1,2}}}{-\frac{3}{2u_{\mathrm{eq}_{1,2,3}} - u_{\mathrm{eq}_{2,3,1}} - u_{\mathrm{eq}_{3,1,2}}}{3}}$$
(14)

Where $L_{\Sigma_x} = L_x + \frac{L_{br}}{3}$ for the equivalent circuit seen from the input ac side, and $L_{\Sigma_y} = L_y + \frac{L_{br}}{3}$ for the equivalent circuit seen from the output ac side. Equations (13) to (14) are equivalent as the equations from the initial model seen in Fig. 3, thus this initial model can be interchanged with the one from Fig. 5, effectively reducing the number of state space matrices to 3×2^6 , as to enable the implementation on small scale RT Boxes. The final time step achieved on the RT Box using the split model is 10µs.

To fulfill the condition of negligible influence on the converter terminal currents, proper tuning of the VC and VR has to be done. Additionally, the virtual circuit might trigger resonances in the circuit, which can also be eliminated by correct tuning. The system being of 12th order and having two degrees of freedom, namely the value of the VR and the VC, makes solving it analytically quite challenging. For this reason an algorithm shown in Fig. 6 was developed and solution obtained and used is this work is:

$$C_v = 850 \text{ nF}$$
 (15)

$$R_v = 35 \ \Omega \tag{16}$$

IV. MODEL VERIFICATION

A. RT-HIL description

Figure 7 shows the RT-HIL platform developed at the Power Electronics Laboratory at EPFL, initially used for the IMMC presented in [8] and [19], was modified to simulate the M3C



Fig. 7. RT-HIL system configured for the M3C using one application RT Box (number 1) and nine branch RT Boxes (number 2).



Fig. 8. Picture of the branch RT Box, with an illustration of the sub-cycled average model running on it

configuration. To validate the split model described in the previous section, it is implemented on the RT-HIL system described above, using a connection of multiple small scale simulators (RT Box). Figure 7 shows one application RT Box, marked by the number one, and nine branch RT Boxes, simulating the nine branches of the M3C and marked by number two. The back of the cabinet which is not shown in the picture hosts the ABB PEC800 controller on which the control of the M3C is implemented.

The model running on the application RT Box corresponds to the model seen in Fig. 5, including the ac grid, electrical machine and the split model of the M3C. The application RT Box is receiving voltage references for each branch from the given branch RT Box. The interface board connected to the Application RT Box allows for scaling of the analog and digital input/output to meet the requirements of the ABB PEC800 controller.

The power stage of the series connection of FB cells representing a branch of the M3C runs on the respective branch RT Box. The limitations of digital input ports available in the RT Box, namely 32, together with the requirements of four switching signals per cell that are generated by DSP on the cell card, limits the number of cells per RT Box to eight. In this paper, the maximum of eight cells per branch is used, thus requiring the connection of eight cell cards to the branch RT box. Each cell cards hosts the logical implementation of the FB cell [20], and communicating the four switching signals to the branch RT Box. As seen on Fig. 8, the model of the FB cells running on the RT Box is the sub-cycle average model, using a controlled current source and a voltage measurement. Based on the switching signals received by the cell card and the branch current measurements received from the application RT Box, the branch RT Box calculated the resulting branch voltage.

B. Simulation Results

The parameters of the model from Fig. 1, which is running on the application RT Box are given in table I.

A start up procedure of the M3C is shown in Fig. 9, where initially the converter is disconnected from the grid, highlighted in yellow (a). After the connection to the grid, the

TABLE I: Details of the ac grid, Synchronous Machine (SM) and M3C model running on RT-HIL

	Value	Unit
Grid Voltage	6.6	kV
Grid Inductance	27.7	mH
Grid Resistance	0.1	mΩ
SM Voltage	6.3	kV
SM Power	500	kVA
SM Torque	6088	Nm
SM Speed	750	rpm
Shaft inertia	152	$\rm kgm^2$
M3C cell capacitance	1	mF
M3C cell voltage	1500	V
M3C cells per branch	8	
M3C branch inductance	2.5	mH
M3C branch resistance	66.4	mΩ

cells are charged through passive charging using a charging resistor to limit the inrush current. This stage is marked by a red background color (b) on the branch cells voltage plot and allows the branches to be charged at the amplitude of the ac grid voltage. After passive charging and before starting active charging, a timeout is introduced during which the charging

M3C grid voltage (V) 4000 -4000 Grid current (A) 500 -5(M3C machine voltage (V) 4000 \cap -4000 Machine current (A) 50 0 -50 M3C branch voltage (kV) 12 (b) (d) (a) (c)Virtual capacitor currents (A) 50 0 -50 0 2 3 4 5

Fig. 9. Results of the RT-HIL simulation showing the start up process of the M3C. The divisions on the branch voltage plot highlight the different steps throughout the process. Currents through the virtual network are shown on the bottom plot.

resistors are bypassed, highlighted in orange (c). After passive charging, the M3C is able to control the ac currents from the grid, thus enabling the active charging process which is highlighted in blue (d) on the same plot. During this stage, the ac grid currents are controlled to increase the branch voltages to their nominal setpoint. When the cells are charged close to their nominal voltage of $1.5 \,\mathrm{kV}$, the branch energy balancing control is activated enabling energy exchange between the branches to guarantee the equal distribution of energy to all branches. Throughout the passive charging, negligible currents are flowing through the virtual network, and once active charging starts, they remain negligible due to their high frequency nature as will be shown in the following simulation result.

Full load operation of the electrical machine in pumping mode is shown in Fig. 10. The currents flowing though the virtual network are shown in the last plot. To prove that these currents have a negligible influence on the control algorithm, a spectral analysis of the currents flowing through the VC at this



Fig. 10. Results of the RT-HIL simulation showing input grid voltages and currents, machine voltages, currents, torque and speed, branch voltages as well as the currents through the virtual network during nominal load and speed operation of the machine in pumping mode.



Fig. 11. Spectral analysis of the current passing through the virtual capacitances in full load mode, including a zoom on the amplitude for the frequency range from 0 Hz to 200 Hz.



Fig. 12. Results of the RT-HIL simulation showing input grid voltages and currents, machine voltages, currents, torque and speed, branch voltages as well as the currents through the virtual network during the speed reversal transient of the electrical machine.

operating mode is shown in Fig. 11. As the high frequencies are filtered out in the control loop, an additional zoom on the frequency components below 200 Hz, which are of interest, is included. The two peaks revealed in the zoomed part of Fig. 11 occur at the nominal input and output frequency of the current operating condition of the M3C. As previously mentioned, to validate the control structure and algorithm, the virtual network should not influence the currents within the frequency range of the ac terminals, as these frequencies are not filtered out in the control loop. As can be seen in Fig. 11, neither of the peaks of the VC currents at operating frequencies is exceeding the previously defined threshold of 2% of the nominal ac terminal currents.

To validate the use of the M3C model implemented on the RT-HIL to serve the purpose of simulating PHSP scenarios, Fig. 12 shows the speed reversal from pumping to generating of the electrical unit. The transition from full pumping power to full generating power takes less than 2 seconds as both the load torque and machine torque contribute to this transition. Throughout the whole process, the currents through the virtual network remain of high frequency nature, and the current amplitude within the frequency band of the ac terminals through the VC remain negligible. Additionally, balancing of the energy of the branches is provided through a proper implementation of an energy control algorithm.

V. CONCLUSION

The time step constitutes a major factor in the determination of the quality of real time simulations. For an RT-HIL system with the main purpose of validating the control structure and algorithm, the smallest possible time step is required as to guarantee fidelity of the simulation results. This paper presents the possibility of a simulation time step reduction through the use of VC and VR allowing the splitting of a converter into multiple independent subsystems. In this paper, this splitting process using VC and VR was demonstrated using the M3C topology, allowing a reduction in simulation time step through a division into three independent subsystems. Proper tuning of the virtual network ensures negligible influence of the addition of the virtual network to the basic operational principle of the original model. This paper includes a mathematical proof as well as simulation results demonstrating the validity of the split M3C model for the implementation on a RT-HIL system to validate the control structure and algorithm.

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REFERENCES

 W. Li and J. Bélanger, "An equivalent circuit method for modelling and simulation of modular multilevel converters in real-time hil test bench," *IEEE Transactions on Power Delivery*, vol. 31, no. 5, pp. 2401–2409, 2016.

- [2] G. Li, D. Zhang, Y. Xin, S. Jiang, W. Wang, and J. Du, "Design of mmc hardware-in-the-loop platform and controller test scheme," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 2, pp. 143–151, 2019.
- [3] S. Dennetière, H. Saad, B. Clerc, E. Ghahremani, W. Li, and J. Bélanger, "Validation of a mmc model in a real-time simulation platform for industrial hil tests," in 2015 IEEE Power Energy Society General Meeting, 2015, pp. 1–5.
- [4] Y. Wang, C. Liu, H. Liu, B. Ling, and G. Li, "Real-time simulation model and experimental test bench for modular multilevel converter," in 2018 2nd IEEE Conference on Energy Internet and Energy System Integration (EI2), 2018, pp. 1–6.
- [5] M. R. Lotz, M. Kohn, T. Öznur, and M. Könemund, "Hardware-inthe-loop setup for low voltage modular multilevel converter control development," in 2020 IEEE 29th International Symposium on Industrial Electronics (ISIE), 2020, pp. 126–133.
- [6] C. Lin, D. Liu, X. Wu, Z. He, W. Wang, and W. Li, "Setup and performance of a combined hardware-in-loop and software-in-loop test for mmc-hvdc control and protection system," in 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015, pp. 1333–1338.
- [7] W. Wu, X. Wu, L. Jing, and J. Li, "Design of modular multilevel converter hardware-in-loop platform based on rt-lab," in 2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia), 2016, pp. 2350–2355.
- [8] S. Milovanovic, I. Polanco, M. Utvic, and D. Dujic, "Flexible and efficient mmc digital twin realized with small-scale real-time simulators," *IEEE Power Electronics Magazine*, vol. 8, no. 2, pp. 24–33, 2021.
- [9] The simulation platform for power electronics systems, https://www. plexim.com/sites/default/files/rtboxmanual.pdf, [Accessed on 02.08.2021].
- [10] T. HIL, Typhoon hil402. [Online]. Available: https://www.typhoonhil.com/doc/products/Typhoon-HIL402-brochure.pdf.
- [11] PLEXIM, *The simulation platform for power electronics systems*, English, version Version 4.5, 830 pp.

- [12] "Modeling and simulation," in Design, Control and Application of Modular Multilevel Converters for HVDC Transmission Systems. John Wiley and Sons, Ltd, 2016, ch. 6, pp. 272–282.
- [13] H. Saad, J. Peralta, S. Dennetière, J. Mahseredjian, J. Jatskevich, J. A. Martinez, A. Davoudi, M. Saeedifard, V. Sood, X. Wang, J. Cano, and A. Mehrizi-Sani, "Dynamic averaged and simplified models for mmc-based hvdc transmission systems," *IEEE Transactions on Power Delivery*, vol. 28, no. 3, pp. 1723–1730, 2013.
- [14] J. Xu, A. M. Gole, and C. Zhao, "The use of averaged-value model of modular multilevel converter in dc grid," *IEEE Transactions on Power Delivery*, vol. 30, no. 2, pp. 519–528, 2015.
- [15] P. Le-Huy, P. Giroux, and J. Soumagne, "Real-time simulation of modular multilevel converters for network integration studies," in *International Conference on Power Systems Transients*, 2011, pp. 14–17.
- [16] T. Maguire, B. Warkentin, Y. Chen, and J. Hasler, "Efficient techniques for real time simulation of mmc systems," in *Proc. Int. Conf. Power Syst. Transients (IPST)*, 2013, pp. 1–7.
- [17] W. Li and J. Bélanger, "An equivalent circuit method for modelling and simulation of modular multilevel converters in real-time hil test bench," *IEEE Transactions on Power Delivery*, vol. 31, no. 5, pp. 2401–2409, 2016.
- [18] J. Allmeling and N. Felderer, "Sub-cycle average models with integrated diodes for real-time simulation of power converters," in 2017 IEEE Southern Power Electronics Conference (SPEC), 2017, pp. 1–6.
- [19] S. Milovanovic, M. Luo, and D. Dujic, "Virtual capacitor concept for effective real-time mmc simulations," in *PCIM Europe digital days* 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2021, pp. 1–8.
- [20] M. Utvic, I. P. Lobos, and D. Dujic, "Low voltage modular multilevel converter submodule for medium voltage applications," in *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2019, pp. 1–8.