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Abstract

Condition health monitoring strategies applied to different power electronics applications are gaining popularity as early component degradation detection can trigger preventive maintenance actions before a significant fault occurs. In highly modular converter structures, such as the modular multilevel converters, made out of many submodules, the development and implementation of condition health monitoring strategies are significant and challenging. This paper analyzes and demonstrates the use of the auxiliary submodule power supply consumption to recognize submodule sub-circuits abnormal operation. Thus, a new strategy to monitor submodules components is provided, enabling new prospective condition health monitoring methods locally or at the converter level. Experimental results show the effectiveness of the proposed idea.

1 Introduction

Higher reliability requirements combined with new and advanced computational and measurement techniques have made the condition health monitoring (CHM) concept an increasingly popular research topic in power electronics-based applications. Among various power converter solutions, it is commonly accepted that power semiconductors and power capacitors are the most sensitive components presenting high failure rates [1]. In the case of medium voltage (MV) high-power MMC, formed by several low-power SMs, a large number of power semiconductors and power capacitors are employed among several other integrated-circuits, logic gates, passive components, processors, low-power semiconductors, magnetics and connectors. Thus, there is a reasonable interest in developing strategies to reduce the likelihood of SM failures and/or to overcome fault situations so that the converter reliability and availability can be further increased. Commonly, MMC reliability is addressed at the production level by considering proper electric circuit design and quality control procedures performed before and after the unit is placed in the field [2]. On the other hand, at the operational level, reliability is improved using active fault-tolerant control systems [3], [4] in which a fault is detected so that the defective SM is isolated to reduce consecutive failure and extra damage to the converter [5], [6]. It is important to point out that production level approaches have a limited ability to handle unexpected situations not considered during the design phase. Moreover, fault-tolerant methods react after the fault occurs, managing the unexpected situation up to some extent to keep the converter operating. Therefore, other promising concepts, such as CHM, are gaining attention to improve MMC reliability further. The main idea behind CHM is to periodically observe selected components by moni-

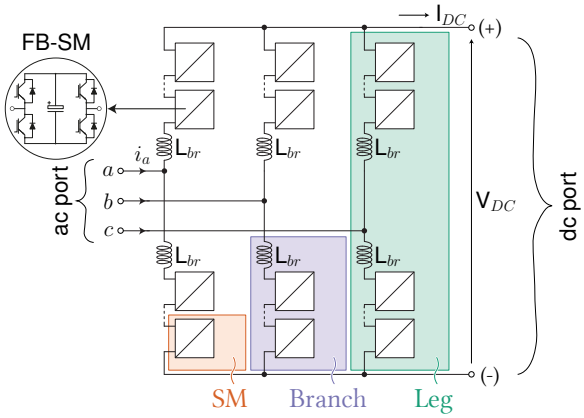

Fig. 1: A classical configuration of the modular multilevel Converter (MMC) for the ac-dc conversion, formed by 48 full-bridge submodules (SMs).

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toring failure precursor parameters so that changes and trends of the monitored characteristic can be used to estimate the component health condition (or deterioration state). This information is used to trigger preventive maintenance alarms before severe deterioration, or a significant fault occurs [7], [8]. Different condition monitoring algorithms have been developed around the MMC; however most of them have focused on estimating the ageing state of the SM insulated gate bipolar transistors (IGBTs) [9] and power capacitors [10], [11]. Less sensitive but equally important components for the proper operation of the SM, such as the IGBT gate drivers, logic gates, processor, and passive components are not taken into account. This might be explained as monitoring such components requires additional hardware to sense and process new information, representing extra cost, volume, complexity, and reliability reduction counter effect. Consequently, new observation or measurement techniques should be considered to gather additional information about the SM to improve or develop new CHM strategies.

For the first time, this work presents monitoring the power consumption of the flyback-based auxiliary submodule power supply (ASPS) as a plausible approach to acquire new and valuable information about the MMC SM condition. It is explored the idea that ASPS consumption behaves as a measurable signature that reflects SM operation under normal conditions, i.e., hardware behaves as expected, and abnormal conditions, i.e., SM sub-circuits operation has changed due to, for instance, components failure or degradation. An estimation of the ASPS consumption is mathematically derived and validated through experimental tests. It has been found that the proposed method successfully tracks the ASPS consumption trend under different SM operating conditions. Results from this work suggest that new MMC CHM strategies might be enabled.

2 System overview

The proposed idea is developed considering a 250 kV A MMC whose topology is depicted in Fig. 1, and the already existing SM presented in Fig. 2. Each branch is composed of eight 650 V 70 A SMs series connected with a 2.5 mH inductor, enabling 3.3 kV and $\pm$ 5 kV in the ac and dc side, respectively. During regular MMC operation, the SM can find itself in several states, however only passively charged (no pulse-width modulation (PWM)) and operating states (PWM operation) are considered relevant. At the start-up, the MMC is connected to the grid through precharge resistors, allowing the passive charging of the SMs using their freewheeling diodes. Once a minimum of 290 V is reached, the SMs enter into the passively charged state. At this point, the ASPS is on and supplies the different SM sub-circuits, particularly the digital signal processor (DSP)-based controller and communication. Then, the MMC main controller sends the command so that each SM uses its power switches to actively charge its dc-link capacitors up to the nominal value (650 V), reaching the operating state where the SMs are ready to operate and follow the control set points.

2.1 Submodule and sub-circuits

Depicted in Fig. 2 scheme, three main sections can be recognized in the considered SM: **(a)** protec-

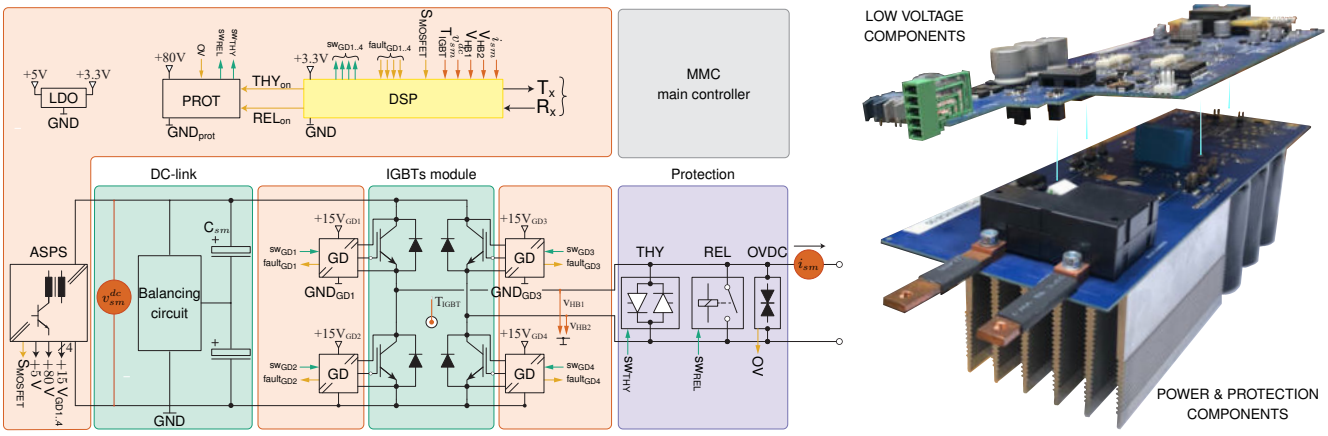


Fig. 2: Considered SM scheme (left) and prototype (right). Power capacitors, IGBT module and protection components (THY and REL) are placed in the bottom PCB, while the low-power components are in the top PCB.

tion, which comprises an antiparallel thyristor (THY) and a bi-stable electromechanical relay (REL) used to provide non-permanent and permanent SM bypass, respectively, and an overvoltage detection circuit (OVDC) to detect SM terminals overvoltage and trigger signal to activate protection devices simultaneously (THY+REL). During normal operation (no fault detected), the consumption of the circuitry associated with protections is neglected; **(b)** power components, highlighted in green, comprising a 1.2 kV 72 A full-bridge IGBT module, a 2.25 mF 650 V to 800 $V_{nom/max}$ capacitor bank, and an active balancing circuit to balance voltage between series-connected capacitors; and **(c)** low-voltage components, highlighted in red, comprising the four IGBT gate drivers which consumption is considered while the SM is switching, a DSP-based local controller performing sensor and digital signal acquisition, monitoring, and additional protection actions (that might result in triggering either THY or THY+REL), PWM generation, SM capacitor balancing control, and communication with the MMC main controller, and the flyback-based ASPS, supplying with isolated low-voltage the components mentioned above.

The protection and power components are placed in the bottom PCB (right side of Fig. 2), while the low-voltage components are in the top PCB. Finally, it is important to point out that the two red circles labeled v_{sm}^{dc} and i_{sm} are the dc-link voltage and terminal current measurement, respectively, considered the main sensed variables for the proper operation of the SM. Additional information about presented SM components and operation can be found in [12], [13].

3 Auxiliary SM power supply

The ASPS is based on an isolated single-switch multiple-outputs flyback converter powered from the SM dc-link capacitors. The ASPS is governed by the UCC 28C44 low-power current mode PWM controller, self-supplied from $V_{out,15V}$, the 15 V secondary with split windings. The PWM controller regulates only the 5 V output to assure the DSP-based local controller is supplied with a stable voltage, while the remaining secondaries are cross-regulated. Four 15 V outputs with floating grounds supply the four IGBT gate drivers, and an additional 80 V floating ground output supplies the protection circuitry [14]. A scheme of the ASPS is depicted in Fig. 3 and its main parameters are presented in Table 1.

As shown in Fig. 4, during passive charging none of the sub-circuits can operate as the ASPS has not reached the minimum input voltage. Once $v_{sm}^{dc} \geq v_{sm_{\text{min}}}^{dc}$, the SM is in passively charged state, allowing the ASPS to supply the DSP-based local controller and the communication circuitry. Afterward, SM modulation, and basic control actions are enabled permitting the active charging of its dc-link until $v_{sm_{\text{nom}}}^{dc}$ is reached. Then, the SM is in operating state, ready to receive a voltage reference and operates exchanging power within the converter. It is important to mention that protection circuitry is considered as it can be triggered any time during the SM operation.

3.1 Power consumption estimation

The principles of flyback converter operation are well known, and it is not difficult to establish a link between control duty cycle, supply voltage and input power. When the flyback power switch is conducting, the ASPS input voltage v_{sm}^{dc} produces a

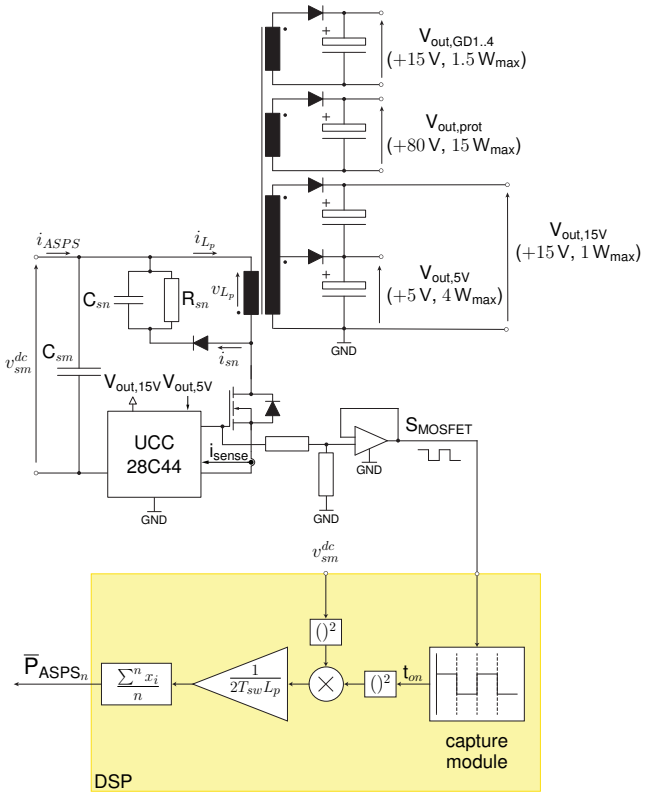


Fig. 3: Considered flyback-based ASPS and proposed idea scheme. DSP calculations and used measurement are highlighted in yellow.

Tab. 1: ASPS main parameters

Parameter	Value	Unit
Primary winding voltage	$200 - 900$	V
Primary winding turns	120	-
Primary magnetizing ind.	12.5	mH
MOSFET switching freq.	20	kHz
Snubber C_{sn}	2.7	nF
Snubber R_{sn}	196	kΩ
Sec. wind. turns $V_{out,15V}$	9	-
Sec. wind. turns $V_{out,5V}$	3	-
Sec. wind. turns $V_{out,GD1..4}$	9	-
Sec. wind. turns $V_{out,prot}$	48	-

voltage v_{L_p} in the primary inductor (cf. Fig. 3). As a consequence, a current i_{L_p} flows through the primary coil, which is limited by its magnetizing inductance L_p and increases linearly with $\frac{v_{L_p}(t)}{L_p}$ slope (cf. Fig. 5). Assuming that flyback primary side power losses and voltage drop due to input filters and MOSFET are negligible, v_{L_p} and i_{L_p} can be approximated by v_{sm}^{dc} and the ASPS input current i_{ASPS}, respectively. Then, i_{ASPS} can be written as (1).

$$i_{\text{ASPS}} \approx \frac{v_{sm}^{dc}}{L_p} t, \quad t \in [0, t_{on}] \tag{1}$$

Where t_{on} is the total time the MOSFET is on. Due to SM dc-link large capacitance C_{sm}, $v_{sm}^{dc}(t)$ can be considered constant during the whole MOSFET switching period T_{sw}. Until $t = t_{on}$, the output diodes are reverse polarized, preventing the current to flow from the secondary windings to the output capacitors, thus an input energy $E_p = 0.5 L_p i_p^2$ is delivered to the magnetic circuit and stored, mainly, in the core air gap, where i_p is i_{ASPS} at $t = t_{on}$. Considering discontinous conduction mode, when the MOSFET is off, the secondary windings reverse their polarity and a big portion of the energy stored in the magnetic circuit is transferred to the secondaries before the MOSFET switching period is reached, charging the output capacitors and supplying the load. Then, the ASPS stored energy can be approximated by

$$E_p = \frac{1}{2} L_p i_p^2 \approx \frac{1}{2} L_p \left(\frac{v_{sm}^{dc}}{L_p} t_{on} \right)^2 \approx \overline{P}_{\text{ASPS}} T_{sw} \tag{2}$$

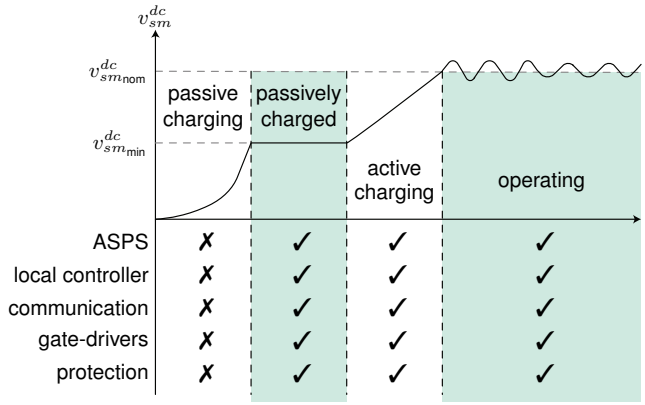


Fig. 4: SM sub-circuits use with respect to its state. The check mark means the associate sub-circuit is or might be operating.

where $\overline{P}_{\text{ASPS}}$ is the ASPS mean input power over the switching period T_{sw}. Finally, rewriting (2) yields

$$\overline{P}_{\text{ASPS}} \approx \frac{1}{2} \frac{(v_{sm}^{dc} t_{on})^2}{T_{sw} L p}. \tag{3}$$

Due to the imperfect magnetic coupling between the primary and secondary coils, a small portion of the energy transferred to the magnetic core during t_{on} is not captured by the output windings, but it is still present in the magnetic circuit. This is represented through a leakage inductor in series with the primary coil. Then, right after the MOSFET stops conducting, this leakage magnetic energy is returned to the primary side, reflected as a negative v_{L_p} and the current i_{sn}, and dissipated by the R_{sn}-C_{sn} snubber circuit. Thus, expression (3) already considers this effect and no extra energy has to be taken into account.

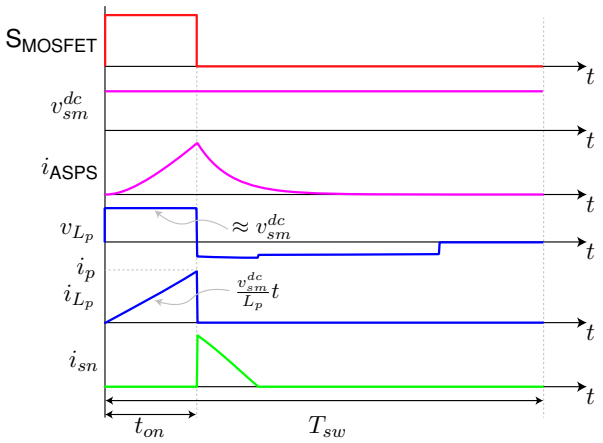


Fig. 5: Main ASPS primary waveforms. Secondary side waveforms are not shown as they are not used for power consumption calculation.

It is important to mention that despite the signal i_{sense} is measured through a shunt resistor and might help estimating the ASPS consumption, it is only used as a feedback by the PWM controller and the DSP does not acquire it. Instead, v_{sm}^{dc}, available in the SM local controller for specific control and protection actions, and t_{on}, are used to estimate the ASPS consumption according to (3). t_{on} is estimated measuring the active time of the MOSFET firing pulse (S_{MOSFET}) using the DSP capture module (ECAP) (cf. Fig. 3). Please note that the MOSFET pulse measurement circuit is not commonly available in the SM designs, however can be easily implemented with few low-cost components.

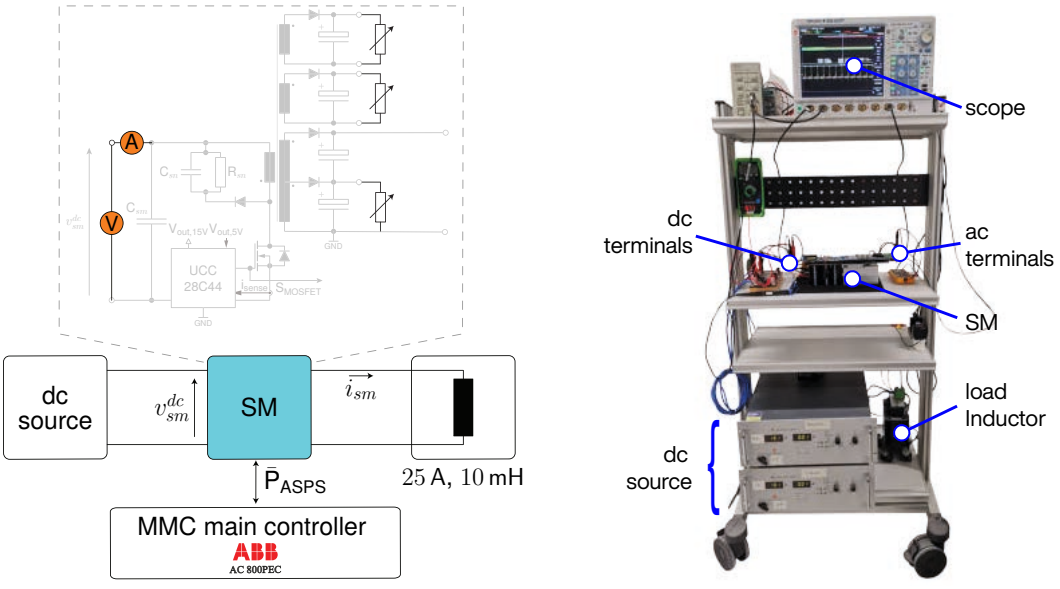
4 Experimental setup

The experimental setup considers a single SM whose dc-link is connected to two series connected Delta Elektronika SM600-10 dc power supplies through auxiliary dc terminals, and a 10 mH inductor, connected to its ac terminals, as it is presented in Fig. 6. The SM synthesizes terminal its voltage using unipolar modulation at 1 kHz switching frequency, and the output current is not controlled, but simply circulates through the inductor. From the classical MMC theory, (4) is deduced, the current flowing through the SMs terminal within a branch of any leg, e.g. a of the upper branch (similar result can be derived for the other branches). It was considered that the converter operates at nominal values, balanced and without distortion ac port currents, input/output steady-state power balance and zero circulating currents.

$$i_{sm} = \frac{I_{DC}}{3} + \frac{\hat{i}_a \cos(\omega t - \varphi)}{2} \tag{4}$$

I_{DC} is the converter dc port current, $\hat{i}_a$ is the magnitude of the ac port line current, ω is the system angular frequency and φ is the phase-shift between ac port voltage and current. It is important to note that due to the pure inductive load in the experimental setup, no active power can be delivered, thus (4) contains only the ac component and φ is close to $\frac{\pi}{2}$.

The MOSFET firing pulses are acquired every 50 µs (20 kHz) by the DSP-based local controller using its ECAP and used to estimate t_{on}, while the SM dc-link voltage is sensed by means of a voltage divider in cascade with a voltage follower and digitalized by a DSP ADC port at 40 kHz. Despite the DSP ADC and ECAP sampling time are not the same and results are not necessarily synchronized, the difference between the voltage value during T_{sw} and the one stored in the memory is negligible as v_{sm}^{dc} vari-



(a) (b)

Fig. 6: Experimental setup. (a) electrical diagram: a single SM supplied through auxiliary dc terminals and loaded with an inductor at the ac terminals. Highlighted in orange, the scope voltage (V) and current (A) probes. (b) laboratory experimental setup: two series connected Delta Elektronika SM600-10 as dc power supply, SM, a 10 mH inductive load and an ABB PEC800AC controller (not visible in the picture).

ation is much slower compared to S_{MOSFET} duty cycle changes. Once t_{on} is available, $n = 10$ $\overline{P}_{ASPS}$ estimations are performed, averaged and sent to the main controller through the communication system. On the other hand, a scope monitoring the ASPS input voltage (v_{sm}^{dc}) and current is used to compare actual and estimated consumption.
It is important to mention that this experimental setup does not mimic precisely the conditions of the SM operating in the MMC; however, for what is sought to be demonstrated, any difference can be neglected.

5 Experimental results

In order to assess the ASPS power consumption variation when electrical changes occur in its secondary windings, and taking into consideration the presented experimental setup, the following conditions are investigated:

① $\bar{P}_{ASPS}$ at baseline condition. DSP-based local controller and communication are active,

② $\bar{P}_{ASPS}$ when a small resistive load is added to the $V_{out,5V}$ circuit,

③ $\bar{P}_{ASPS}$ when the PWM is activated and i_{sm} =10 A, and

④ $\bar{P}_{ASPS}$ when protection is triggered (THY and both THY + REL).

Each one of these conditions is explored in passively charged and operating states. In passively charged, $v_{sm_{min}}^{dc}$ is set to 300 V, while in the operating state, $v_{sm_{nom}}^{dc}$ is set to 650 V. Fig. 7 and Fig. 8 present the results for both operating conditions. The cases from ① to ③ are concatenated to show the difference between them, while case ④ is presented in a different plot for clarity. Due to the characteristics of SM protection devices, case ④ shows results for THY and THY + REL activation. In addition, results are presented together with their moving average.
In the passively charged state (cf. Fig. 7), on average, the power measured by the scope is approximately 1 W larger than the estimated by the method, representing a relative error between 22% and 28% (cf. Table 2). Notably, the relative error in case ④ decreases considerably to less than 6% during THY or THY+REL activation. Another important observation is the sensitivity of the proposed idea in case ②, where a resistive load of 48 mW was added to the $V_{out,5V}$, and case ③, where the $V_{out,GD1..4}$ outputs supply the IGBT gate driver circuits while the IGBTs are switching and supplying the inductive load with 10 A. According to Table 2, the power difference between cases ② and ① matches the connected load in the $V_{out,5V}$.

Concerning case ③, interestingly, when PWM is activated, DSP measures slight power reduction, which is consistent with scope measurements. The gate driver consumption is generally very low at 1 kHz switching, and noise appears to impact calculations performed in the DSP. While this is undergoing investigation, no conclusive results were gathered to be included in this paper.

For operating state results, similar observations are

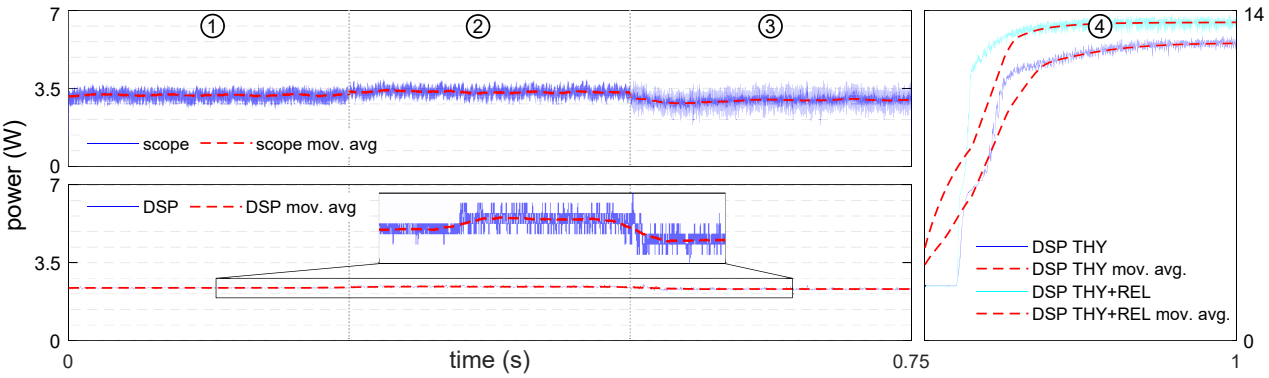


Fig. 7: Experimental results at passively charged state (300 V) for each studied case. Top left plot shows the ASPS average input power measured with the scope. Bottom left and right plots show the DSP ASPS average input power estimated using the explained method. The results are presented as a raw data (blue) and moving average (dash red line).

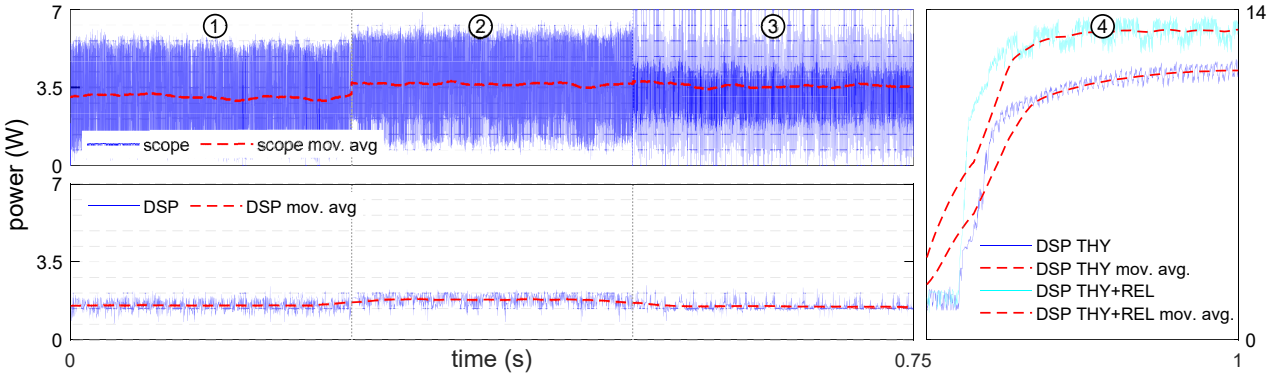


Fig. 8: Experimental results at operating state (650 V) for each studied case. Top left plot shows the ASPS average input power measured with the scope. Bottom left and right plots show the DSP ASPS average input power estimated using the explained method. The results are presented as a raw data (blue) and moving average (dash red line).

found (power estimation trend with the proposed idea for each case); however, a particular situation is highlighted. The proposed method results for the operating state, cases ①, ②, and ③, are up to 58% lower than scope results, which combined with up to 28% difference found in the previous state, make the authors consider two leading causes. The first one is that the proposed method is not sensitive to primary side losses, especially those dependent on the voltage, such as capacitor ESR, primary coil and snubber network. This is particularly advantageous as the method is proposed to observe ASPS secondary side power variations. The second cause is the S_{MOSFET} duty cycle reduction due to primary inductor current reduction when ASPS input voltage increases. According to (2), t_{on} has to be half when v_{sm}^{dc} is double to transfer the same power. Then, shorter pulses are more challenging to acquire by the DSP, especially when the duty cycle is lower than 5% and switching noise, coming from MOSFET (higher dv/dt) and IGBT operation, distort the S_{MOSFET} signal. Once ASPS load increases, as when protection devices are triggered (③), power estimation improves considerably, showing that the method is, in fact, sensitive to duty-cycle.

Tab. 2: Results summary. Average value per case.

State	Case	①	②	③	④	
Pas. charged	$\bar{P}_{ASPS}$ scope (W)	3.20	3.34	2.95	THY	13.05
					THY+REL	14.30
	$\bar{P}_{ASPS}$ DSP (W)	2.37	2.42	2.31	THY	12.59
					THY+REL	13.49
	Abs. error (W)	0.83	0.92	1.04	THY	0.46
					THY+REL	0.81
	Rel. error (%)	25.94	27.54	21.69	THY	3.52
					THY+REL	5.66
Operating	$\bar{P}_{ASPS}$ scope (W)	3.07	3.64	3.58	THY	13.39
					THY+REL	14.38
	$\bar{P}_{ASPS}$ DSP (W)	1.54	1.80	1.50	THY	11.40
					THY+REL	13.08
	Abs. error (W)	1.53	1.84	2.08	THY	1.99
					THY+REL	1.30
	Rel. Error (%)	49.84	50.55	58.10	THY	14.86
					THY+REL	9.04

Despite the considerable difference between the scope and method results, it can be claimed that $\bar{P}_{ASPS}$ estimation tracks the actual ASPS consumption trend reasonably well, recognizing a specific power signature for each observed SM operating state. In the light of this outcome, more elaborated SM monitoring strategies performed locally in the SM or at the MMC-level fed by the SMs information might be explored. Local strategies based on detecting abnormal ASPS consumption during passively charged or operating state, for instance, can help to detect incipient SM deterioration before any power is actively exchanged within the converter or during regular operation, respectively. Moreover, considerable power consumption drift seen from the ASPS primary side might indicate faulty components such as gate drivers or protection devices. Advanced approaches based on machine learning techniques might recognize and provide specific information for each secondary winding load change, focusing on and facilitating maintenance and repairing of SM particular circuits or components.

Nevertheless, complex algorithms implemented in devices with limited processing power, such as the DSPs, become a bottleneck for developing this kind of strategies. Instead, MMC-level approaches, where simple information collected by the SMs is sent to the converter controller, or a specialized processing unit to perform complex algorithms, might

be more appropriated. For instance, 48 SMs are monitored in the MMC of Fig. 1, each one sending back the ASPSs estimated consumption. Then, for a given converter state, one might expect that the ASPSs present a similar consumption signature, making it not difficult to recognize, employing an appropriate mathematical tool, the SM or a set of them operating differently.

6 Conclusions

Commonly found in literature and industry, the MMC is a promising power converter solution for future high and medium-voltage high power applications. However, because of its large number of SMs, composed of several electronic, magnetic and mechanical components, reliability might be of concern, and further investigation must be done to improve it. CHM techniques applied to converter SMs are gaining attention as monitoring failure precursor parameters can help estimate some selected components' deterioration state. Nevertheless, monitoring components usually require additional hardware and processing power, thus increasing the SM's cost, volume, and complexity, unless existing hardware and measurement capabilities are used differently.
This work presented a new approach to monitor MMC SM condition, based on observing the power consumption of the ASPS. A simple methodology was implemented in the SM DSP-based local controller and tested under different SM operating conditions. It was found that the proposed idea can recognize ASPS secondary power change satisfactorily. The method takes full advantage of observing the flyback regulator control pulses directly to recognize even small ASPS output power variations.

Compared with more classical alternatives such as adding a current sensor at the ASPS input or in series with the primary coil, this idea might represent a lower cost option and less processing power requirement as no digital filter to remove commutation noise or no extra calculations have to be done to remove ASPS primary side losses effect. The main drawback is that the method does not work correctly under small S_{MOSFET} duty cycles; however, this is a circumstantial condition of the designed SM as flyback duty cycle range is a parameter choice during the design process.

The main findings suggest that ASPS power consumption estimation to detect changes in the circuits loading its secondary side might enable new MMC SM CHM methods.

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