

# Scalable fabrication of functional nanostructures on stretchable substrates by capillary-assisted particle assembly and adhesion lithography

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*To my nephew, Mr. Chen-Hsi Yu...*





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*Lausanne, February 22, 2022*

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# Abstract

The fabrication of metallic nanostructures on stretchable substrates enables specific applications that exploit the combination of the nano-scale phenomena and the mechanical tunability of the physical dimensions of the nanostructures. Due to the large difference in the thermal expansion coefficient between metals and polymer-based soft materials, patterning metallic nanostructures directly on a stretchable substrate is a known challenging task. In this thesis, scalable fabrications of metallic nanostructures on stretchable substrates by top-down and bottom-up methods are studied. Metallic nanostructures are first fabricated on Si substrates and subsequently transferred to stretchable substrates.

In the first part of this thesis, fabrication of nanogap electrodes (NGEs) on a polydimethylsiloxane (PDMS) substrate using adhesion lithography is reported. With wafer-level processes, the nanogap is created on an Al sacrificial layer by separating two Au electrodes with an Al<sub>2</sub>O<sub>3</sub> nanolayer. By etching the Al sacrificial layer, the NGEs are transferred to the PDMS substrate. Tunneling currents across the nanogap on PDMS are measured under various mechanical deformation statuses of the PDMS substrate. The electrical measurement results show that the nanogap distance is mechanically tunable in the quantum tunneling regime. The NGEs on PDMS might be eventually integrated with micro piezo-electric actuators to become miniaturized tunable NGEs, which could pave the way towards the application of an on-chip single-molecule detector. Apart from developing the fabrication process of the NGEs on PDMS, a yield study of the essential step of the adhesion lithography, e.g., the tape peeling process, is also conducted to understand the design principles of the NGEs. The yield of the wafer-level tape peeling process is larger than 80%.

In the second part of this thesis, chip-level ( $\sim 2 \times 2 \text{ cm}^2$ ) fabrication of ordered gold nanoparticles (AuNPs) on a PDMS substrate using capillary-assisted particle assembly (CAPA) technique is reported. AuNPs are first assembled on reusable Si templates with pre-defined topographical traps, and then transferred to the PDMS substrate by etching the Al sacrificial layer. The reusable assembly trap has the shape of the funnel which is designed for high assembly yield ( $> 90\%$ ) and precise particle placement (offset  $\sim 10 \text{ nm}$ ). The assembly yield, the particle position offset, the yield of the transfer process, and the reusability of the assembly template are systematically studied. Two functional AuNP structures are demonstrated using the reported fabrication process. The first structure is the plasmonic surface lattice resonance (SLR) arrays of 150 and 200 nm AuNP. The optical spectra of the AuNP arrays on PDMS are measured showing pitch-related SLR peaks that agree with the finite element method (FEM) simulation results. The second structure is the dimer of 200 nm AuNPs which has a nanogap between two AuNPs. By

assembling two AuNPs in the same funnel-shaped trap, a nanogap is formed between two AuNPs. Combining Au electrodes fabricated using electron beam lithography and the lift-off process, NGEs are fabricated and successfully transferred to a PDMS substrate.

**Keywords**

Nanogap electrodes, Adhesion lithography, Capillary-assisted particle assembly, CAPA, Surface lattice resonance, Stretchable substrate, Wet etching transfer, Tape peeling

# Résumé

La fabrication de nanostructures métalliques sur des substrats étirables permet des applications spécifiques qui exploitent la combinaison des phénomènes à l'échelle nanométrique et la possibilité de réglage mécanique des dimensions physiques des nanostructures. En raison de la grande différence de coefficient d'expansion thermique entre les métaux et les matériaux souples à base de polymères, la fabrication de nanostructures métalliques directement sur un substrat étirable est une tâche difficile. Dans cette thèse, les fabrications évolutives de nanostructures métalliques sur des substrats étirables par des méthodes descendants et ascendants sont étudiées. Des nanostructures métalliques sont d'abord fabriquées sur des substrats de Si et ensuite transférées sur des substrats étirables.

Dans la première partie de cette thèse, la fabrication d'électrodes à nano-espace (NGE) sur un substrat de polydiméthylsiloxane (PDMS) à l'aide de la lithographie par adhérence est rapportée. Le nano-espace est créé sur une couche sacrificielle d'Al en séparant deux électrodes d'Au avec une nano-couche d' $\text{Al}_2\text{O}_3$ . En gravant la couche sacrificielle d'Al, les NGE sont transférées sur le substrat en PDMS. Les courants tunnels à travers le nano-espace sur le PDMS sont mesurés sous différents états de déformation mécanique du substrat PDMS. Les résultats des mesures électriques montrent que la distance du nanogap est mécaniquement réglable dans le régime de l'effet tunnel quantique. Les NGE sur PDMS pourraient éventuellement être intégrés à des micro-actionneurs piézoélectriques pour devenir des NGE miniaturisés et réglables, ce qui pourrait ouvrir la voie à l'application d'un détecteur de molécules uniques sur puce. Outre le développement du processus de fabrication des NGE sur PDMS, une étude de rendement de l'étape essentielle de la lithographie par adhésion, c'est-à-dire le processus de décollement du ruban, est également menée pour comprendre les principes de conception des NGE. Le rendement du processus de transfert par décollement de film adhésif effectué sur des plaquettes est supérieur à 80%.

Dans la deuxième partie de cette thèse, la fabrication au niveau des puces ( $\sim 2 \times 2 \text{ cm}^2$ ) de nanoparticules d'or ordonnées (AuNPs) sur un substrat en PDMS en utilisant la technique d'assemblage de particules assistée par capillarité (CAPA) est rapportée. Les AuNPs sont d'abord assemblées sur des moules Si réutilisables avec des pièges topographiques prédéfinis, puis transférées sur le substrat PDMS en gravant la couche sacrificielle d'Al. Le piège d'assemblage réutilisable a une forme d'entonnoir qui est conçue pour un rendement d'assemblage élevé ( $> 90\%$ ) et un placement précis des particules (le décalage  $\sim 10 \text{ nm}$ ). Le rendement de l'assemblage, le décalage de la position des particules, le rendement du processus de transfert et la réutilisabilité du moule d'assemblage sont systématiquement étudiés. Deux structures d'AuNP fonctionnelles

sont démontrées en utilisant le procédé de fabrication rapporté. La première structure est un réseau de AuNPs (150 et 200 nm) plasmoniques à résonance de réseau (SLR). Les spectres optiques des réseaux d'AuNP sur PDMS sont mesurés et montrent des pics de SLR liés au pas et qui correspondent aux résultats de la simulation FEM. La deuxième structure est le dimère d'AuNPs (200 nm) qui présente un nano-espace entre deux AuNPs. En assemblant deux AuNPs dans le même piège en forme d'entonnoir, un nano-espace est formé entre deux AuNPs. En combinant des électrodes en Au fabriquées par lithographie par faisceau d'électrons et le processus de lift-off, les NGEs sont fabriquées et transférées avec succès sur un substrat en PDMS.

### **Mots-clés**

Électrodes à nano-espace, lithographie par adhérence, assemblage de particules assisté par capillarité (CAPA), résonance de réseau, substrat extensible, transfert par gravure humide, décollement de bande.

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# Chapter 1 Introduction

## 1.1 Nanostructures on stretchable substrates

Micro/Nanofabrication techniques have been developed since the mid of 20<sup>th</sup> century<sup>[1]</sup> to fabricate micro/nanoscale structures or devices on mechanically rigid substrates (Young's modulus,  $E > 10$  GPa), e.g., Si and glass substrates. Miniaturized structures or devices such as electronic devices<sup>[1]</sup>, sensors,<sup>[2]</sup> actuators,<sup>[3]</sup> fluidic,<sup>[4]</sup> and optical<sup>[5]</sup> devices were fabricated monolithically to build various integrated systems on a single chip. These systems including integrated circuits (IC),<sup>[1]</sup> micro/nano-electromechanical systems (MEMS/NEMS),<sup>[3,6]</sup> lap-on-a-chip (LOC),<sup>[7,8]</sup> and micro/nano-optoelectromechanical systems (MOEMS/NOEMS)<sup>[9,10]</sup> are essential elements to the boost of cutting-edge technologies.

In the early 1990s, researches regarding the fabrication of polymer transistors on flexible plastic substrates were reported,<sup>[11,12]</sup> which are pioneers among others to explore the feasibility of fabricating micro-devices on mechanically unconventional substrates.<sup>[13]</sup> The primary motivations of fabricating micro-devices on non-rigid substrates can be summarized into the following two categories. On one hand, by fabricating well-developed micro-devices on flexible or stretchable substrates ( $E < 10$  MPa), novel applications that are not feasible with the conventional rigid substrates can be achieved due to the flexibility or stretchability of the substrates. For example, the research field "stretchable electronics"<sup>[13–15]</sup> has been extensively developed to enable applications such as e-skin,<sup>[16,17]</sup> flexible/stretchable displays,<sup>[18–20]</sup> and wearable/implantable devices.<sup>[21–23]</sup> On the other hand, novel functional micro/nano structures or devices with working principles that are not compatible with rigid substrates can be realized on flexible/stretchable substrates. Strain sensors with high stretchability,<sup>[24,25]</sup> mechanically tunable plasmonic structures<sup>[26,27]</sup>/photonic crystals<sup>[28]</sup>, and mechanically assembled 3D nanostructures<sup>[29,30]</sup> are remarkable examples in this category.

Among the above-mentioned research works, the optics-related applications particularly motivate the fabrication of nanostructures on stretchable substrates. Firstly, the working principle of plasmonics and photonics depends on physical features that are similar to or smaller than the wavelengths of interest, for example, from dozens to hundreds of



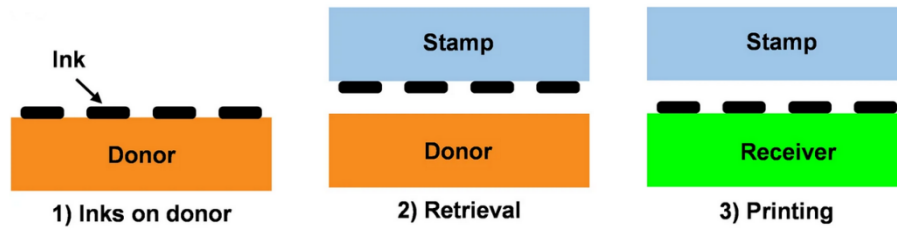
nanometers for visible light. Secondly, the tunability of the optical response of the nanostructures, such as reflectance or transmittance spectrum, is enabled by mechanical tuning of the physical dimensions of the nanostructures, e.g., the inter-structural gap size, thanks to the stretchability of the substrate. In particular, the integration of metallic nanostructures and stretchable substrates is by far the most promising methodology to realize such applications.

## 1.2 Fabrication strategies

In practice, to pattern metallic nanostructures directly on a stretchable substrate is a known challenging task, which is mainly due to the large difference in the thermal expansion coefficient between metals and polymer-based soft materials.<sup>[31,32]</sup> As an alternative, a strategy to first deposit and pattern metallic thin film nanostructures on a silicon substrate using the conventional nanofabrication processes and subsequently transfer the metallic nanostructures onto a stretchable substrate is developed. Depending on the mechanism of structure transfer, three different methodologies are categorized and briefly described here: (1) Transfer printing,<sup>[33–35]</sup> (2) dry peel-off transfer,<sup>[29,36]</sup> and (3) wet etching transfer.<sup>[37,38]</sup>

“Transfer printing is a materials assembly technique that uses elastomeric stamps for heterogeneous integration of various classes of micro- and nanostructured materials into two- and three-dimensionally organized layouts on virtually any type of substrate.”<sup>[34]</sup> As shown in Figure 1.1, nanostructures are transferred from a donor substrate onto a receiver substrate via an elastic stamp by manipulating the adhesion strength between the stamp/ink and the ink/substrate interfaces. The major advantage of the transfer printing technique is the variety of the receiver substrate.

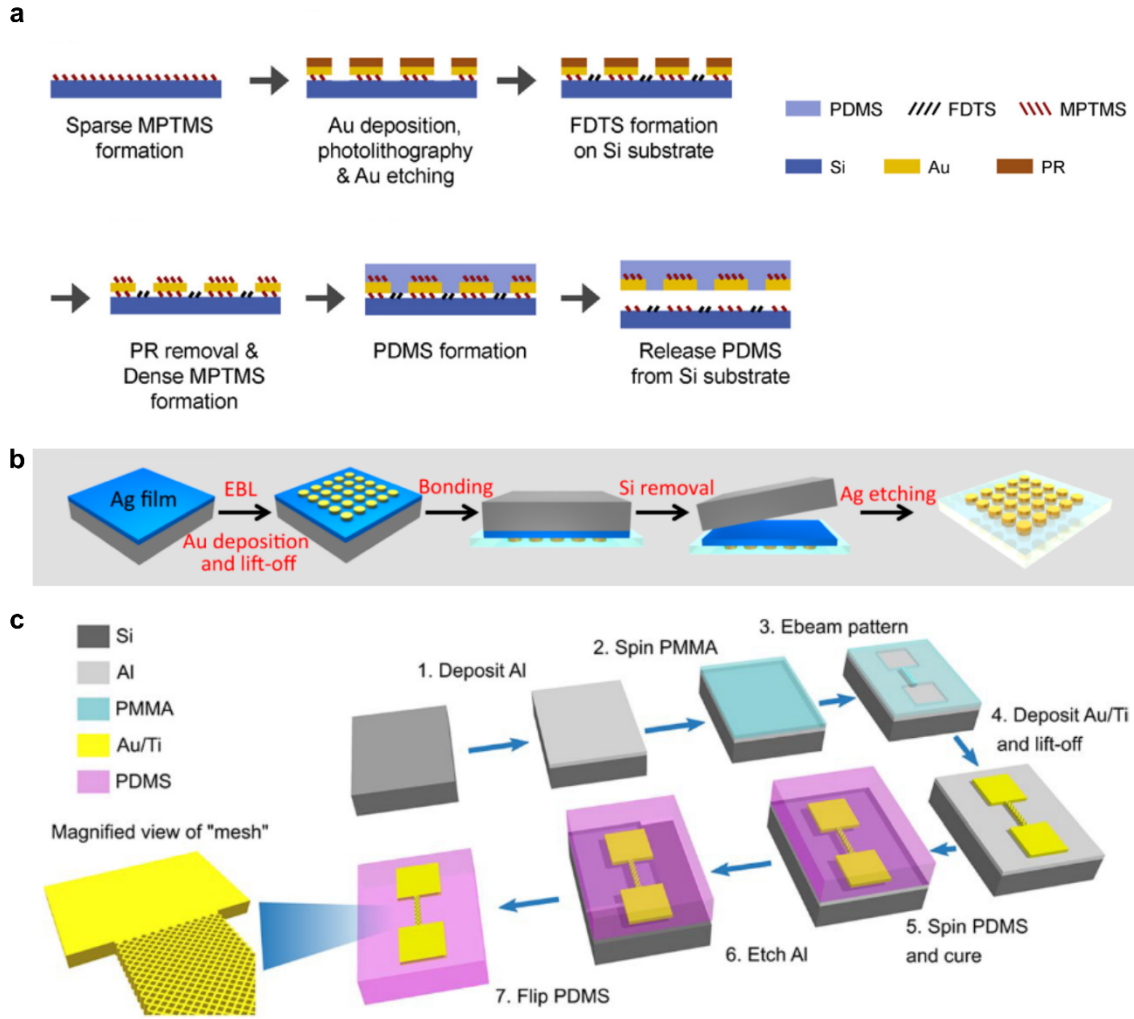
Similar to the transfer printing technique, the dry peel-off transfer is accomplished by creating an adhesion of the stretchable substrate/structures interface that is larger than the adhesion of the donor substrate/structures interface (see Figure 1.2a). Apart from using a solid-phase stretchable substrate to receive the transferred structures on top of the surface, embedded transferred structures can also be obtained using dry peel-off transfer. By pouring/coating uncured liquid-phase polymer materials such as polydimethylsiloxane (PDMS) on the donor substrate, the structures to be transferred are embedded in the stretchable substrate after the curing process, which is not straightforward to the transfer printing technique. The dry peel-off process is a simple method to transfer microstructures to stretchable substrates, however, this method does not work well to transfer the structures with the lateral dimension smaller than 10  $\mu\text{m}$ .<sup>[29]</sup> To increase the transfer yield of nanostructures, a sacrificial metal film is introduced under the nanostructures, as shown in Figure 1.2b, to replace the interface between the stretchable substrate and the top surface of the donor substrate. The weak adhesion between the



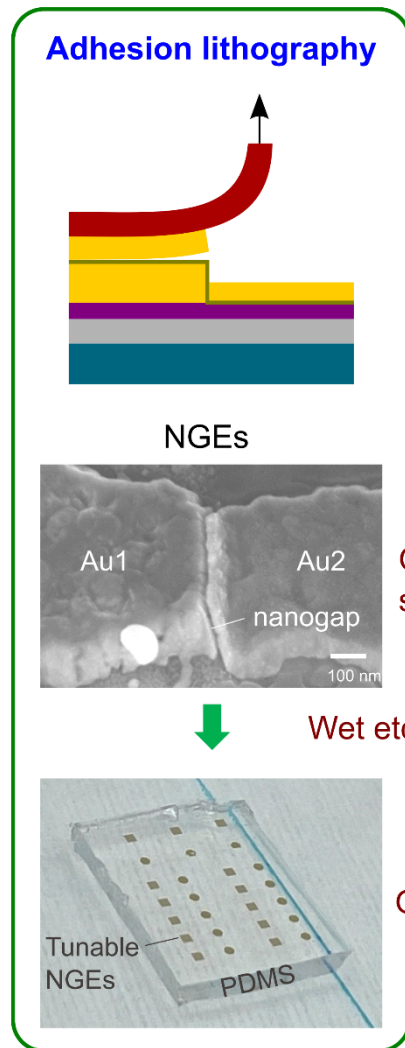
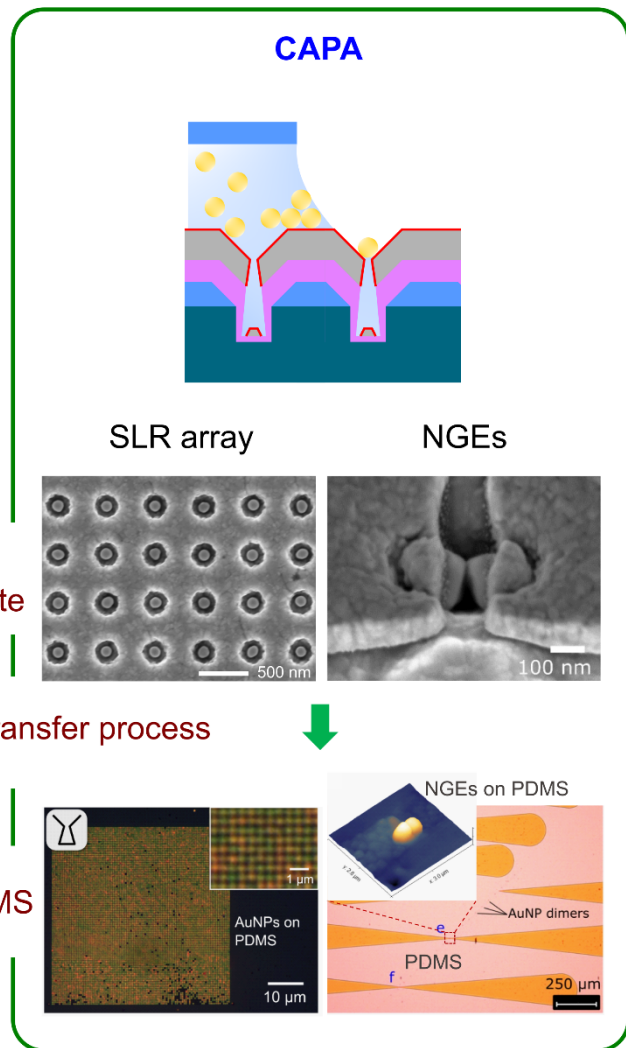
**Figure 1.1.** Schematic working principle of transfer printing technique. (adapted from Figure 2 in ref. <sup>[35]</sup>). Micro/nanostructures are transferred from a donor substrate onto a receiver substrate via an elastic stamp by manipulating the adhesion strength between the stamp/ink and the ink/substrate interfaces.

sacrificial metal film and the donor substrate allows a high transfer yield of the nanostructures using the dry peel-off process.

A sacrificial layer is also introduced under the nanostructures when conducting the wet etching transfer as shown in Figure 1.2c. Instead of peeling off the sacrificial layer along with the nanostructures from the donor substrate, the sacrificial layer is etched in a chemical bath to eliminate the attachment of the nanostructures to the donor substrate. Compared to the transfer printing technique and the dry peel-off process, the mechanical stress induced by deforming the stretchable substrate during the process is avoided, and thereby the stress applied on the transferred nanostructures is reduced. To exploit this advantage, the research works reported in this thesis focus on using the wet etching transfer process to fabricate nanostructures on a stretchable substrate such as PDMS.



**Figure 1.2.** Schematic fabrication processes of dry peel-off and wet etching transfer. (a) Dry peel-off transfer process with transferred microstructures embedded in the PDMS substrate (adapted from Figure 1 in ref. <sup>[36]</sup>). (b) Metal-assisted dry peel-off transfer (adapted from Figure 1 in ref. <sup>[29]</sup>). By introducing a sacrificial layer (Ag film), Au nanostructures are transferred onto a PDMS substrate via the direct dry peeling process. (c) Wet etching transfer (Figure 1 in ref. <sup>[37]</sup>). By introducing a sacrificial layer (Al film), Au nanostructures are transferred and embedded in the PDMS after the Al wet etching process, avoiding the mechanical stress induced by deforming the PDMS substrate during the peel-off process.

**Top-down fabrication****Bottom-up fabrication**

**Figure 1.3.** Scheme of the research works in this thesis. This thesis is composed of two parts regarding using adhesion lithography and capillary-assisted nanoparticle assembly (CAPA) technique, respectively, to fabricate functional nanostructures on PDMS. The nanostructures are first fabricated on Si substrates and subsequently transferred to PDMS substrates by the wet etching transfer process.

### 1.3 Thesis outline

As shown in Figure 1.3, this thesis is composed of two parts regarding using adhesion lithography and capillary-assisted nanoparticle assembly (CAPA) technique, respectively, to fabricate functional nanostructures on PDMS. The nanostructures are first fabricated on Si substrates and subsequently transferred to PDMS substrates by the wet etching transfer process. Chapter 2 reports the work regarding the tunable nanogap electrodes (NGEs) on PDMS fabricated by adhesion lithography. Chapter 3 and chapter

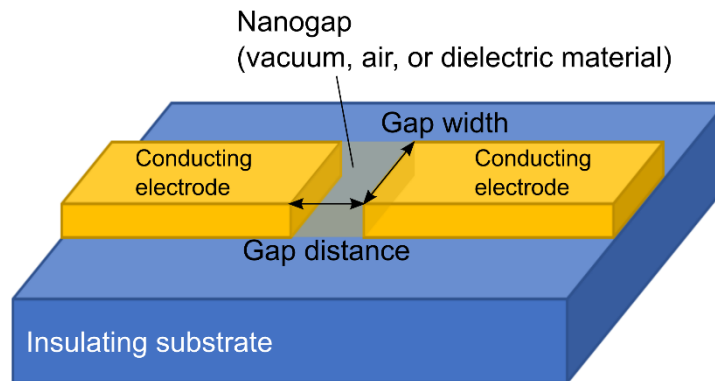
4 report the works regarding the fabrication of plasmonic surface lattice resonance (SLR) nanoparticle arrays and NGEs, respectively, on PDMS by the CAPA technique. The introductions, motivations, conclusions, and outlooks of each work are given in the corresponding chapters. Finally, chapter 5 concludes the thesis and summarizes the outlooks for future works in scalable fabrications of NGEs towards the sensor and optical applications.

# Chapter 2 Tunable nanogap electrodes on PDMS fabricated by adhesion lithography

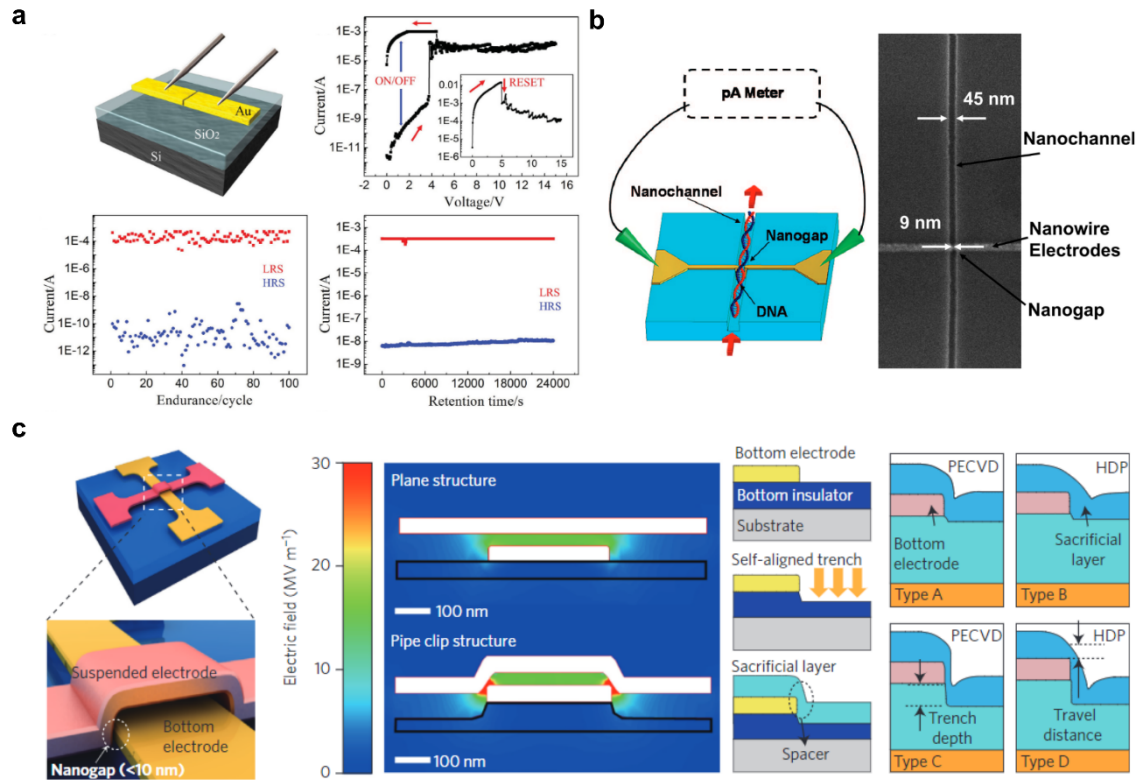
## 2.1 Introduction

### 2.1.1 Nanogap electrodes

Nanogap electrodes (NGEs) comprise a pair (or more) of conducting electrodes on an insulating substrate.<sup>[39]</sup> The electrodes are separated by a gap distance ranging from several nm to dozens of nm. As shown in Figure 2.1, the gap can be in vacuum, air, or filled by dielectric materials depending on the desired application. In the past decades, NGEs have been proposed as a unique nano-device in terms of interaction with electrons, photons, and molecules. Various applications have been studied and developed accordingly, such as resistive random access memory (RRAM),<sup>[40–42]</sup> nano-electromechanical (NEM) switch,<sup>[43,44]</sup> and biosensing.<sup>[45–47]</sup> These applications are briefly described in Figure 2.2.



**Figure 2.1.** Illustration of nanogap electrodes.



**Figure 2.2.** NGEs applications on rigid substrates. (a) Nonvolatile RRAM (adapted from Figure 3 in ref. [41]). The electrical conductance across the nanogap ( $\sim 5$  nm) can be “SET” to a low resistive state (LRS) and “RESET” to a high resistive state (HRS) by sweeping the applied voltage due to the formation and the dissolution of conducting filaments around the nanogap. (b) Label-free DNA detector (Figure 1, 3 in ref. [45]). A change in transverse current can be measured from the NGEs when a DNA molecule passes through the NGEs in the nanochannel. (c) Sub-1-V NEM switch (adapted from Figure 1 in ref. [43]). The “ON” and “OFF” statuses can be switched by relative mechanical motion between the NGEs which is induced by electrostatic force and mechanical restoring force.

When the nanogap distance is smaller than 2 nm, more distinctive applications can be achieved as shown in Figure 2.3, including single-molecule discrimination,<sup>[48–50]</sup> electrical-driven nano-antenna,<sup>[51–54]</sup> molecular electronics.<sup>[55–57]</sup> These applications are enabled thanks to the enhanced phenomena in sub-2 nm nanogaps, i.e., significant quantum tunneling, highly concentrated electric field, and single-molecule bridging, respectively.

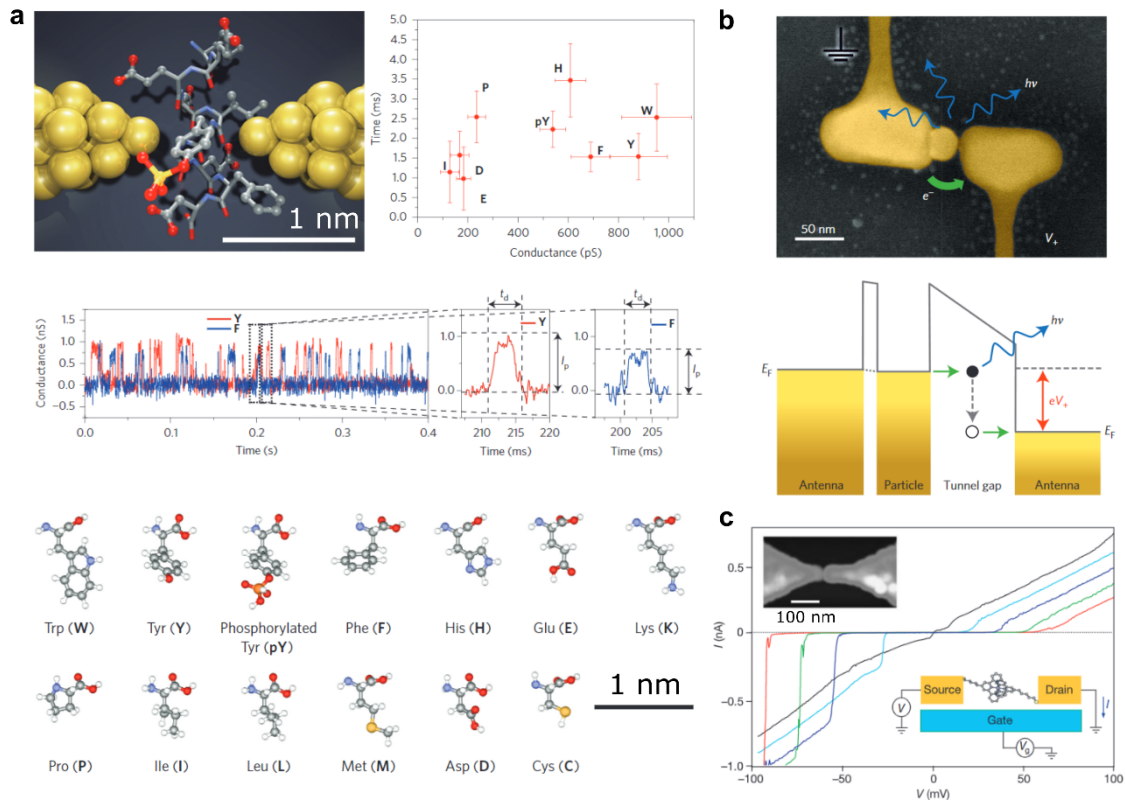
### 2.1.2 Fabrication of nanogap electrodes

Apart from the applications of NGEs, various fabrication methods of NGEs have also been reported. In 2019, Y. Yang et al. summarized the fabrication methods for sub-5 nm metal nanogaps (with or without electrodes) in their review article.<sup>[58]</sup> Here, based on their summary table, the methods reported for the fabrication of NGEs are the following:

- Electrochemical deposition<sup>[59,60]</sup>
- Electromigration breakdown<sup>[61]</sup>
- Focus ion/electron beam lithography<sup>[62,63]</sup>
- Crack junction<sup>[64,65]</sup>
- Shadow deposition<sup>[66,67]</sup>
- Self-terminating electroless gold plating<sup>[68]</sup>
- Nano-imprinting lithography (NIL)<sup>[69]</sup>
- Adhesion lithography<sup>[70,71]</sup>
- Laser direct writing lithography<sup>[72]</sup>
- On-wire lithography<sup>[73]</sup>

Among the above-listed techniques, crack junction, shadow deposition, self-terminating gold plating, NIL, and adhesion lithography are parallel fabrication techniques, i.e., multiple NGEs in a large-area scale are fabricated simultaneously. The rest of the techniques in the list are often considered as not scalable. Although all of them are able to fabricate sub-5 nm NGEs effectively, the reliable fabrication of sub-2 nm NGEs remains a challenging task even with these approaches. Therefore, instead of fabricating a sub-2 nm nanogap directly, some groups proposed the fabrication of tunable NGEs. In this case, NGEs are first fabricated without any materials filling the nanogap, and then the gap distance is adjusted (e.g., mechanically) to the sub-2 nm range for the aforementioned specific applications. Up to now, the most promising technique to fabricate such tunable NGEs is the use of mechanically controllable break junctions (MCBJ).<sup>[74–76]</sup> To do so, first, a sub- $\mu\text{m}$ , free-standing metallic wire is defined. Then, the substrate is bent inducing a tensile strain to the metallic wire until the break junction is formed. The process is accompanied by real-time monitoring of the electrical conductance, enabling a precise bending deflection control and a configurable attenuation factor of the bent device. This in turn results in a tunable gap distance at the sub-nm scale. The only drawback of the MCBJ technique is that the bending device is typically a few centimeters large to achieve small attenuation factor for sub-nm gap distance control, which disallows monolithic integration with other devices.





**Figure 2.3.** Sub-2 nm NGEs applications on rigid substrates. (a) Amino acid molecules discrimination (adapted from Figure 1, 2 in ref. [49]). The amplitude and the width of the tunneling current spikes induced when different amino acid molecules pass by the NGEs are statistically analyzed to discriminate the molecules. (b) Electrically-driven optical antennas (adapted from Figure 1 in ref. [54]). Photons are generated by inelastic tunneling across the NGEs and are resonating in the nano-antennas to radiate into the far field. (c) Molecular junctions (adapted from Figure 1 in ref. [57]). Single molecule bridges the NGEs with a back gate expressing the electronics properties as a single-electron transistor.

### 2.1.3 Aims and motivation

In the past decade, Masateru Taniguchi and his group reported a series of research works regarding the use of tunable NGEs fabricated by the MCBJ technique in single-molecule detection/sequencing of DNA/RNA and peptides.<sup>[49,50,77–80]</sup> The results present a promising potential of such technology to realize a fast and low-cost de novo DNA/RNA/protein sequencing and quantitative analysis. Inspired by these results, **the aim of this work is to develop a scalable fabrication process of tunable NGEs on a stretchable substrate such as PDMS.** The motivation to fabricate NGEs on a soft substrate is twofold. On the one hand, a soft substrate could allow the integration of deformable nanofluidic channels and tunable NGEs. A deformable nanochannel is reported as one of the effective methods to reduce the molecule speed in a fluidic channel,

which is critical to the feasibility of single-molecule sequencing/analysis using NGEs.<sup>[81–83]</sup> On the other hand, similar to the on-chip MCBJ reported in 2020,<sup>[84]</sup> micromechanical actuators, e.g., piezoelectric actuators might be also integrated on a soft substrate<sup>[85,86]</sup> to tune the gap distance. **An integrated system on a PDMS substrate could pave the way towards a miniaturized single-molecule analysis platform.**

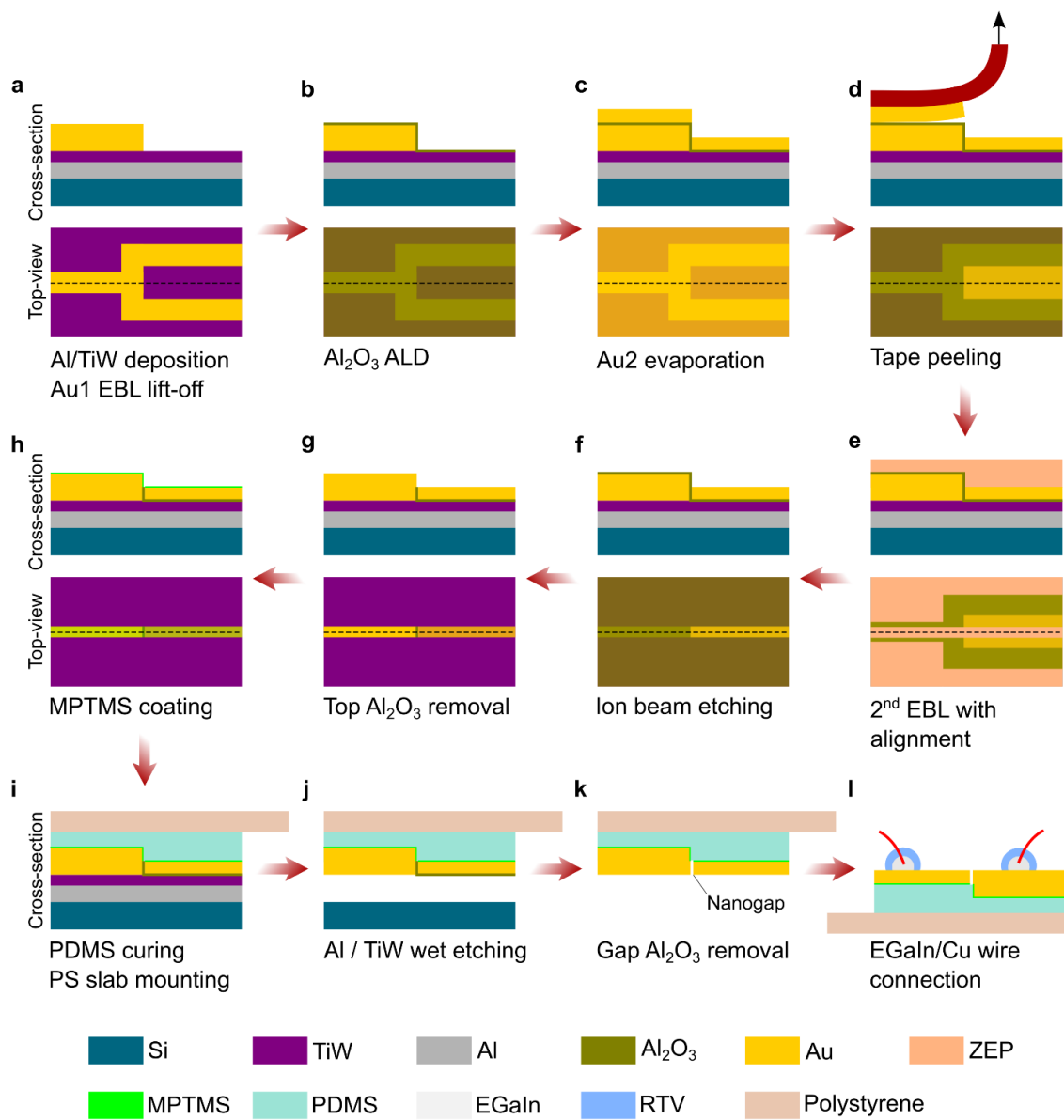
Here, we present the fabrication of tunable NGEs based on electron beam lithography (EBL) in combination with adhesion lithography. Atomic layer deposition (ALD) is used to deposit a sacrificial layer in the nanogap<sup>[70]</sup> for the ease and the accuracy of the initial gap distance configuration. A yield study of the essential step of the adhesion lithography, i.e. the tape peeling process, is also conducted in this work to understand the design principles of the NGEs. Finally, the electrical characterization of the NGEs is conducted in order to confirm whether the fabricated NGEs on PDMS are tunable in the tunneling regime.

## 2.2 Fabrication process and design

Figure 2.4 shows the fabrication process of the tunable nanogap electrodes on stretchable substrates demonstrated in this work, which is compatible with standard cleanroom processes. The first step is to pattern alignment marks for the EBL processes by typical direct laser writing photolithography and Si RIE etching. About 2  $\mu\text{m}$  deep Si etching into the Si wafer creates square holes for the electron beam to detect the topographical height difference and then align the wafer before the EBL process.

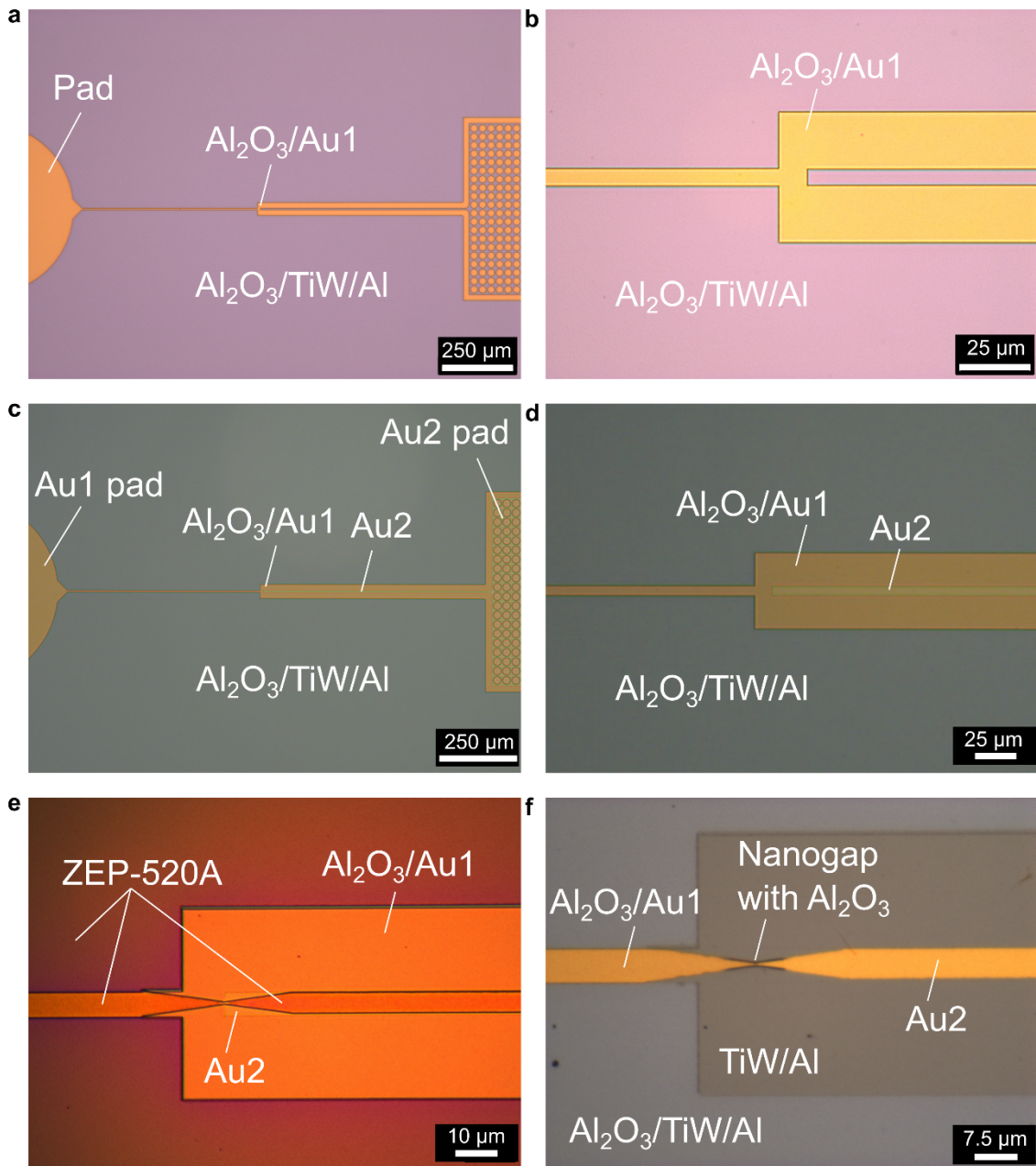
Following the alignment mark patterning, a 150 nm thick Al thin film serving as a sacrificial layer for the wet etching transfer process is deposited by e-beam evaporation. A 100 nm thick titanium tungsten (TiW) thin film is then deposited by DC sputtering on the Al layer. The TiW layer acts a diffusion barrier layer to prevent the inter-diffusion between the gold structures and the Al layer during the annealing process to be carried out afterward.<sup>[87]</sup> A MMA/PMMA positive resist bilayer is spin-coated on the TiW layer and then exposed to the electron beam writing with alignment control. The exposed bilayer is then developed. A metal thin film stack of Ti/Au/Ti (5/100/3 nm) is deposited for the lift-off process (Figure 2.4a). The patterned Ti/Au/Ti stack is hereafter referred to as the “Au1 layer”.

After patterning the Au1 layer, a 4 nm thick  $\text{Al}_2\text{O}_3$  thin film is deposited by ALD (Figure 2.4b), serving as a sacrificial layer to separate the Au1 electrode and the following second Au electrode. OM images of the wafer after Au1 layer patterning and  $\text{Al}_2\text{O}_3$  deposition are shown in Figure 2.5a, b. A thin film stack of Au/Ti (50/3 nm) is deposited by e-beam evaporation (Figure 2.4c), which is hereafter referred to as the “Au2 layer”.



**Figure 2.4.** Schematic illustration of the fabrication process of the tunable NGEs. The dimensions are not to scale to highlight the nano-scale structures.

The subsequent tape peeling process removes only the Au2 deposited on top of the Au1/ $\text{Al}_2\text{O}_3$ , thanks to the weak adhesion between Au and  $\text{Al}_2\text{O}_3$ . The Au2 layer deposited on TiW/ $\text{Al}_2\text{O}_3$  stays due to the height difference of the top surfaces (Figure 2.4d).<sup>[41]</sup> An experiment regarding the tape peeling process and the Au1 design is conducted and discussed in the following section. An OM image of the wafer after Au2 layer patterning is shown in Figure 2.5c, d.



**Figure 2.5.** OM images of the NGEs design after various process steps. (a) After the Au1 layer patterning and Al<sub>2</sub>O<sub>3</sub> deposition. (b) A magnified image of (a). (c) After using the tape peeling process to pattern the Au2 layer. (d) A magnified image of (c). (e) After the 2<sup>nd</sup> EBL to pattern ZEP-520A resist. (f) After the IBE process and resist removal, the NGEs are formed.

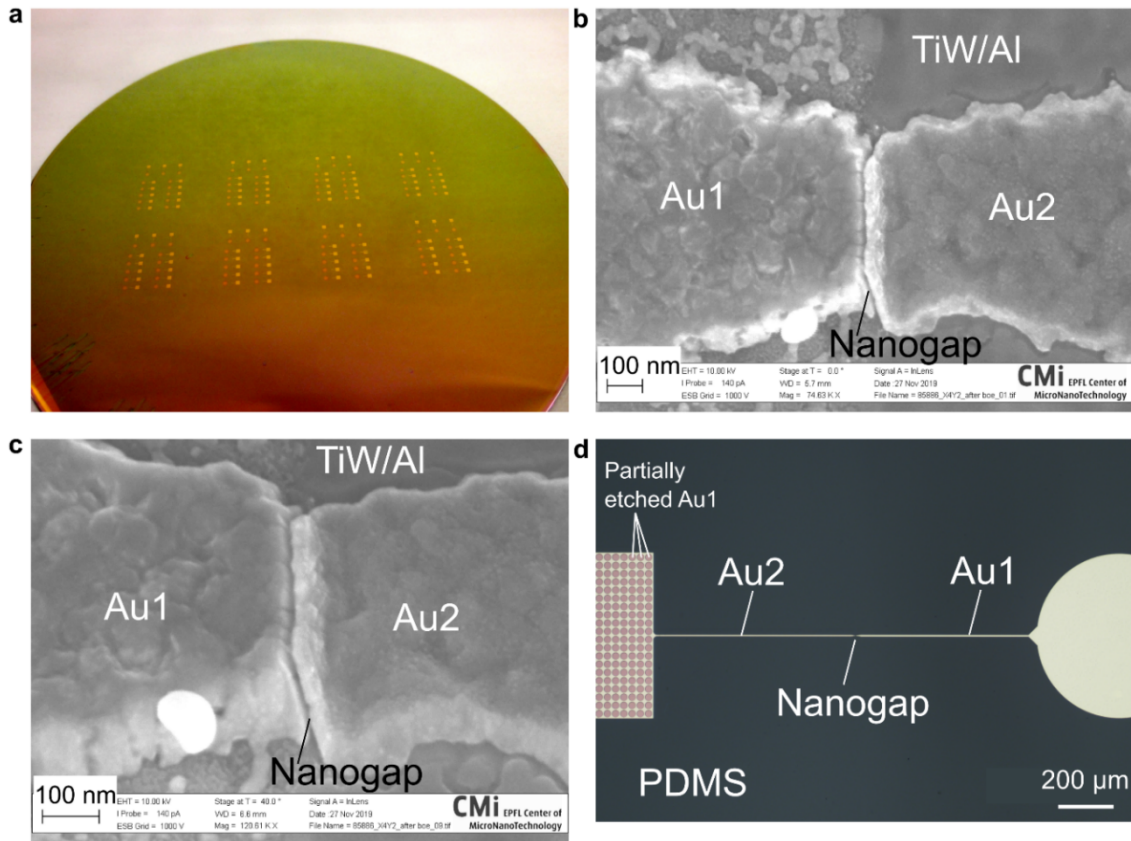
After the tape peeling process to pattern the Au2 layer, positive resist ZEP-520A is spin-coated on the wafer and the 2<sup>nd</sup> EBL is done (Figure 2.4e). The top Ti thin films on both Au1 and Au2 play the role of adhesion promoters to avoid poor coating of ZEP-520A at

this step. The patterned ZEP-520A is then subjected to a thermal reflow process to avoid the fence effect (re-sputtering deposition on the resist sidewall) during the later ion beam etching process (IBE). The IBE process etches unwanted  $\text{Al}_2\text{O}_3$ , Au1, and Au2 to form the NGEs structure (Figure 2.4f), and stops at the TiW layer by etching time control. OM images of the wafer after ZEP-520A patterning and IBE/resist removal processes are shown in Figure 2.5e, f, respectively.

After the IBE process, the NGEs are annealed at 400 °C in  $\text{N}_2$  ambient for 5 min to smooth the edges and surfaces of the Au electrodes. The  $\text{Al}_2\text{O}_3$  on top of the Au1 layer is removed in a photoresist developer bath (AZ 726 MIF/MF CD 26) to reveal the Au1 top surface (Figure 2.4g) for the following (3-Mercaptopropyl)trimethoxysilane (MPTMS, Sigma Aldrich) coating process. MPTMS serves as an adhesion promoter to increase the adhesion between Au electrodes and the PDMS substrate that comes in the following process step (Figure 2.4h).<sup>[88]</sup> An OM image of the Si wafer and SEM images of the NGEs before the MPTMS coating process are shown in Figure 2.6.

Before pouring the PDMS, the processed Si wafer is manually cleaved into chips of  $\sim 17 \times 17 \text{ mm}^2$ . PDMS (10:1) is then poured on the Si chip, degassed for 1 h, and cured at room temperature for a total time of 48 h in order to avoid thermal stress. After the curing, the PDMS is cut and trimmed to a substrate size of  $\sim 15 \times 15 \text{ mm}^2$  to increase the area of TiW/Al exposed to the chemical during the wet etching transfer process. Subsequently, a polystyrene (PS) slab ( $100 \times 40 \times 12 \text{ mm}^3$ ) is manually aligned and brought into contact with the PDMS substrate. Thanks to the Van der Waals force, the PDMS sticks to the PS slab (Figure 2.4i), which serves not only as a handling substrate but also as a bending cantilever to apply strain to the PDMS and the NGEs to tune the nanogap distance during the electrical measurements.





**Figure 2.6.** Images of NGEs before and after the wet etching transfer process. (a) OM image of a 100-mm Si wafer with 8 NGEs chips on it before the top  $\text{Al}_2\text{O}_3$  removal process. (b) Top-view and (c) 40° tilted-view SEM images of NGEs before the wet etching transfer process. (d) OM image of NGEs on a PDMS substrate after the wet etching transfer process.

After the PS slab mounting, the Si chip, along with the PDMS/PS slab, are soaked in a diluted HCl bath for 6 to 12 h to etch the sacrificial Al layer. The NGEs structures are transferred onto the PDMS that is separated from the Si chip after this wet etching transfer process. TiW is etched in a  $\text{H}_2\text{O}_2$  bath (Figure 2.4j), followed by a deionized (DI) water rinse and a BHF wet etching to remove the  $\text{Al}_2\text{O}_3$  both on the Au2 layer and in the nanogap (Figure 2.4k). Thanks to the use of the PS slab as handling substrate, the mechanical stress applied on the soft PDMS and the NGEs on it is minimized after the wet etching transfer process. An OM image of the PDMS and the NGEs after the wet etching transfer process is shown in Figure 2.6d.

Since the typical wire bonding processes are not compatible with soft PDMS substrates, an alternative metal wire connection method is adopted here.<sup>[89]</sup> In order to connect the metal pads on the PDMS and the electrical measurement setups while minimizing the applied mechanical stress, copper wires are not in physical contact with the metal pads.

Instead, droplets of liquid metal (eutectic GaIn, EGaIn, Sigma-Aldrich) are used to bridge the copper wire and pads as shown in Figure 2.4i. The copper wires and the EGaIn droplets are fixed on the PDMS by a room-temperature-vulcanizing (RTV) silicone sealant (DC 732, Dow Corning) which is a rubber-like, soft material to reduce the mechanical stress applied to the PDMS and NGEs structures whenever the copper wires are moved.

The parameters and details of each process step are summarized in Table 2.1.

**Table 2.1.** Fabrication details of the tunable nanogap electrodes.

Step	Process	Equipment	Parameters
1	PR coating for alignment mark patterning	Süss ACS200 GEN3	CMi tool recipe: 0123 Photoresist: AZ ECI 3007 HMDS priming/edge cleaning 2050 rpm, soft baking 90 s at 100 °C, thickness: 1 µm
2	Exposure	Heidelberg Instruments VPG200	i-line (355-365 nm), Dose: 120 mJ/cm <sup>2</sup>
3	Development	Süss ACS200 GEN3	CMi tool recipe: 0823 37s in AZ 726 MIF (or MF CD 26) at room temperature and DI water rinse Post-exposure baking: 1 min at 110 °C
4	Si RIE etching for alignment mark patterning	Alcatel AMS 200 SE	CMi tool recipe: Si_Opto RF 1500 W, DC 30 W, 40 / 55 sccm of SF <sub>6</sub> / C <sub>4</sub> F <sub>8</sub> for 3 min
5	PR ashing	TePla GiGAbatch	600 W, 400 sccm O <sub>2</sub> , 5 min
6	150 or 200 nm thick sacrificial Al e-beam evaporation	Leybold Optics LAB 600H	CMi tool recipe: 163 Room temperature, 1010 mm working distance, 1.8 x 10 <sup>-6</sup> mbar chamber pressure, 1 Å/s deposition rate
7	100 nm thick diffusion barrier layer TiW deposition	Alliance-Concept DP 650	CMi tool recipe: RTU_WTi10% Room temperature, 80 mm working distance, 5 x 10 <sup>-3</sup> mbar chamber pressure, 30 sccm Ar, DC power: 250 W, 3.4 Å/s deposition rate
8	MMA/PMMA spin coating	ATMsse OPTIspin SB20	5 min dehydration baking at 180 °C

			220 nm thick MMA EL6 coating: 500 rpm for 5 s and then 2000 rpm for 1 min 5 min soft baking at 180 °C 220 nm thick PMMA 495K A4 coating: 500 rpm for 5 s and then 2000 rpm for 1 min 5 min soft baking at 180 °C
9	E-beam exposure	VISTEC EBPG5000+	100 kV, 950 $\mu\text{C}/\text{cm}^2$
10	Development	Wet bench	1 min in methyl isobutyl ketone (MIBK) / IPA (1:3) at room temperature, IPA rinse and N <sub>2</sub> drying
11	Au1 e-beam evaporation	Leybold Optics LAB 600H	CMi tool recipe: 222 Room temperature, 1010 mm working distance, $1.5 \times 10^{-6}$ mbar chamber pressure, 4 Å/s deposition rate, Ti/Au/Ti thickness: 5/100/3 nm
12	Au1 lift-off	Wet bench	4 h in acetone and 10 s sonication
13	Al <sub>2</sub> O <sub>3</sub> atomic layer deposition	BENEQ TFS200	CMi tool recipe: 01_Al2O3_50nm Precursor: TMAI, H <sub>2</sub> O 50 cycles at 200 °C
14	Au2 e-beam evaporation	Leybold Optics LAB 600H	CMi tool recipe: 732 Room temperature, 1010 mm working distance, $1.5 \times 10^{-6}$ mbar chamber pressure, 0.5 Å/s deposition rate, Au/Ti thickness: 50/3 nm
15	Tape bonding and peeling	POWATEC P-200	Tape bonding: Use a 1.65 kg weight roller rolling over the wafer (Adwill E series polyolefin UV-curable tape, LINTEC) Tape peeling: Manual peeling with the force in the normal direction of the wafer, the overall peeling-off time ~ 10 s for a 100-mm wafer.
16	ZEP-520A spin coating	ATMsse OPTIspin SB20	500 rpm for 5 s and then 4000 rpm for 1 min, thickness: 400 nm
17	E-beam exposure	VISTEC EBPG5000+	100 kV, 260 $\mu\text{C}/\text{cm}^2$
18	Development	Wet bench	1 min in n-amyl acetate, and 1 min rinsing in methyl isobutyl ketone (MIBK) / IPA (9:1) at room temperature, IPA rinse and N <sub>2</sub> drying
19	ZEP-520A reflow	Hotplate	10 min at 145 °C

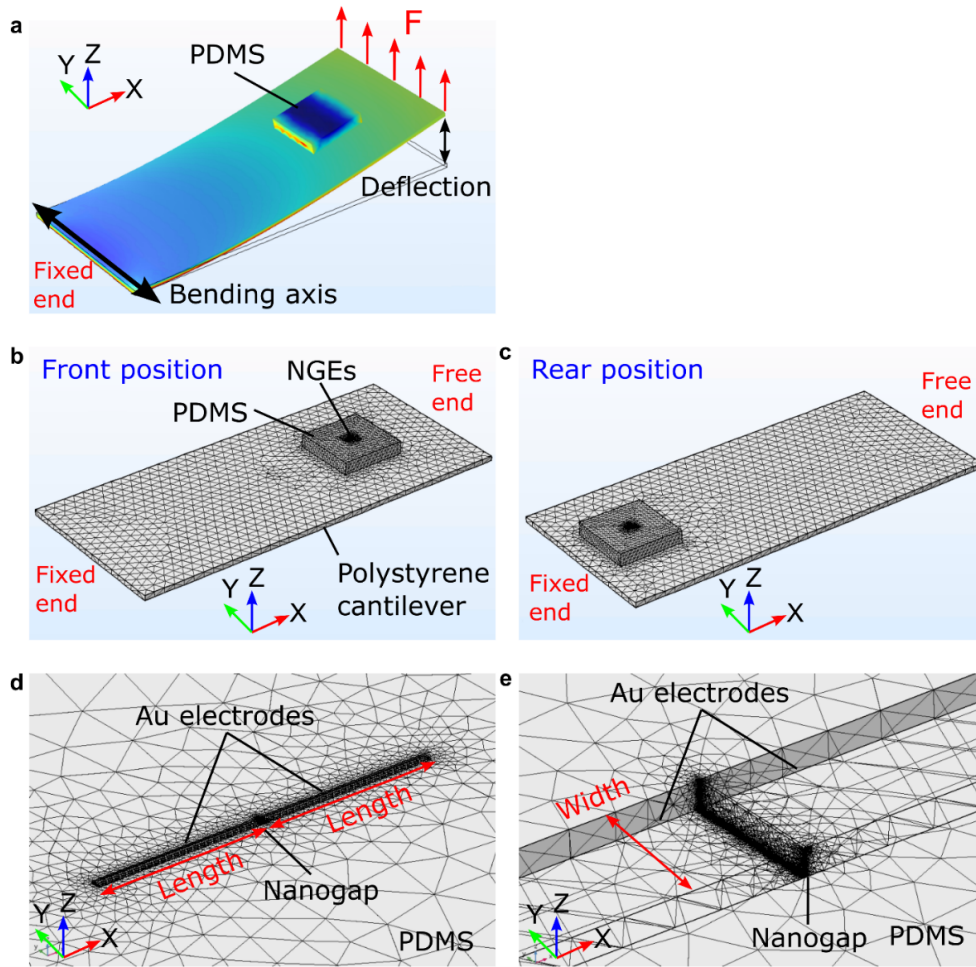


20	Ion beam etching	Veeco Nexus IBE350	CMi tool recipe: med_five_step 500 V, 800 mA, Ar ion beam at 10° to the normal direction of the wafer (12 s etching + 60 s cooling) x 4 + 12 s etching
21	ZEP-520A removal	TePla GiGAbatch Wet bench	600 W, 400 sccm O <sub>2</sub> , 1 min 10 min in NMP (Remover 1165), DI water rinse and N <sub>2</sub> drying 600 W, 400 sccm O <sub>2</sub> , 5 min
22	Rapid thermal annealing (RTA)	Jipelec JetFirst 200	400 °C for 5 min in N <sub>2</sub> ambient, ramping time: 20 s
23	Top Al <sub>2</sub> O <sub>3</sub> removal	Wet bench	3 min in AZ 726 MIF (or MF CD 26) at room temperature, 1 min in DI water, N <sub>2</sub> drying
24	MPTMS priming	Wet bench	2 h in 60 mM MPTMS ethanol solution 2 min in IPA, N <sub>2</sub> drying
25	Wafer cutting		Manual mechanical cleaving into chips
26	PDMS curing		Dow Corning Sylgard 184, Base : curing agent = 10 : 1, mixed and degassed PDMS pouring into a Petri dish with chips 1 h degassing Cured at room temperature for 48 h
27	Polystyrene slab mounting		PDMS manual cutting Manually bring polystyrene slab in contact with PDMS top surface with orientation alignment
28	Wet etching transfer	Wet bench	6 to 12 h in diluted hydrochloric acid bath (37% HCl : DI water = 1:6, volume ratio)
29	TiW removal	Wet bench	10 min in 30% H <sub>2</sub> O <sub>2</sub> at room temperature 2 min in DI water, N <sub>2</sub> drying
30	Nanogap Al <sub>2</sub> O <sub>3</sub> removal	Wet bench	1 min in 7:1 BHF at room temperature 2 min in DI water*2, N <sub>2</sub> drying

### 2.3 Gap distance tunability simulation

In order to understand how precisely the fabricated nanogap can be tuned by the PS cantilever bending, a finite element method (FEM) simulation is conducted to study the gap distance tunability. As shown in Figure 2.7, a COMSOL model which comprises a PS cantilever, a PDMS substrate, and a pair of Au NGEs on the PDMS substrate is created for the simulation study. By fixing the PS cantilever at one end and uniformly applying a force in Z-direction at the other end (free end), the cantilever is bent with a deflection in Z-direction at the free end (see Figure 2.7a). Thus strain is applied to the PDMS substrate and the NGEs to change the nanogap distance. Depending on the distance of the PDMS substrate to the cantilever free end, there are two configurations: front position (Figure 2.7b) and rear position (Figure 2.7c), corresponding to lower and higher applied strain, respectively. During the electrical measurements, these two configurations can be switched by physically clamping the PS cantilever at the different sides. The Au NGEs in Figure 2.7d are modeled in an orientation that is orthogonal to the bending axis as shown in Figure 2.7a. With this orientation, the cantilever should be bent upwards to apply a compressive strain to the PDMS substrate in X-direction to reduce the nanogap distance. On the other hand, by rotating the NGEs by  $90^\circ$  with respect to the normal direction of the PDMS top surface, NGEs are also modeled in an orientation in parallel to the bending axis (Y-axis). In such a case, the cantilever should be bent downwards to apply a tensile strain to the PDMS substrate in X-direction, the nanogap distance is then reduced by a compressive strain in Y-direction due to the Poisson effect. The magnified nanogap model in Figure 2.7e shows that no PDMS is filling the nanogap and the PDMS around the nanogap is densely meshed for ease of convergence and correctness of the simulation results. The top surfaces of the Au electrodes and the PDMS substrate are in the same plane.

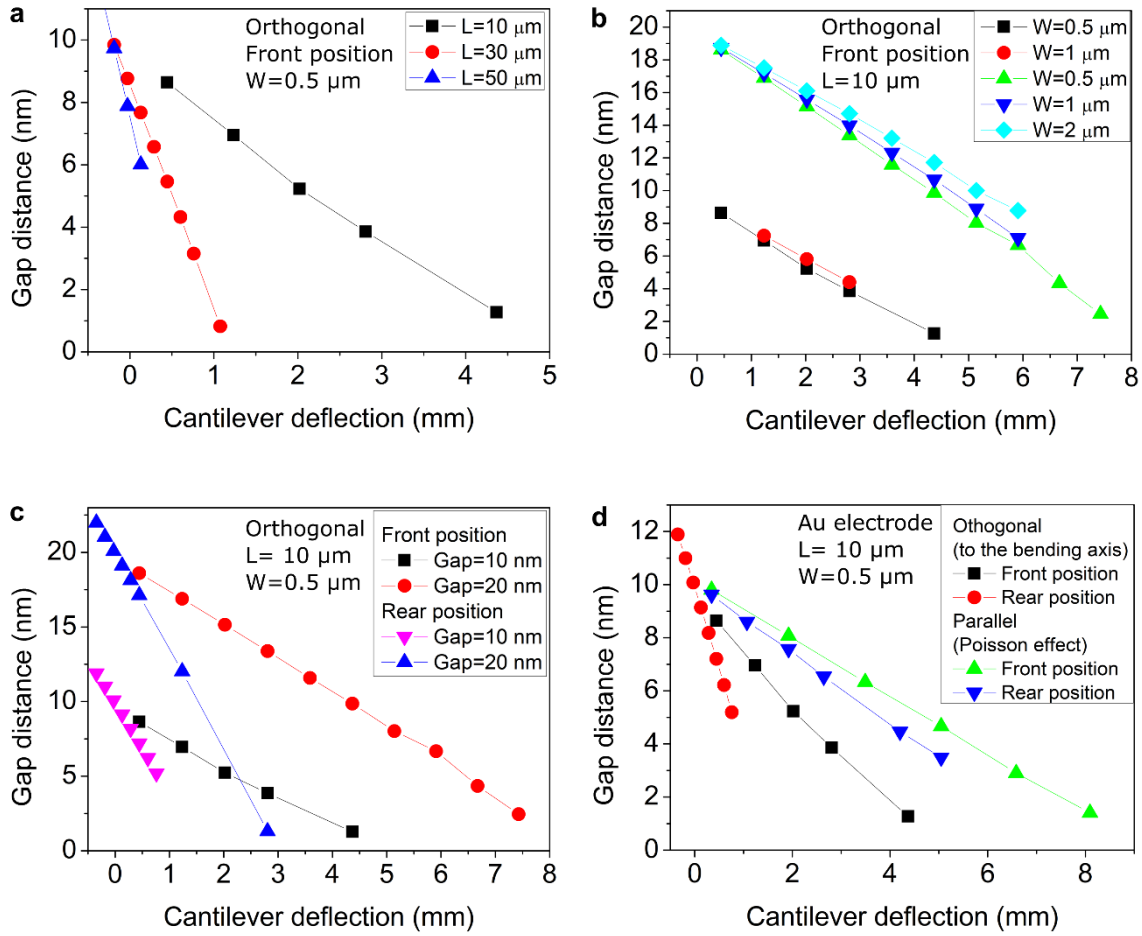
Due to difficulties in having convergence within a reasonable computation time, the NGEs in this simulation study are not modeled following the exact dimensions and shapes reported in the previous section of fabrication. Instead, both Au1 and Au2 electrodes are modeled as two cuboids with identical dimensions. By changing the length/width of the electrodes, as well as the PDMS position and the NGEs orientation, correlations between these factors and the nanogap tunability are studied. The nanogap tunability in this study is represented by the attenuation factor, which is defined as the ratio of the gap distance change,  $\Delta d$ , and the cantilever deflection,  $\delta$ . For example, if the attenuation factor is  $-10^{-6}$ , this means the gap distance can be reduced by 1 nm when the cantilever is deflected by 1 mm. Table 2.2 lists COMSOL parameters and values that are used in this study, and the simulation results are shown in Figure 2.8.



**Figure 2.7.** Nanogap tunability study by COMSOL simulation. (a) Illustration of the bending simulation. (b) The meshed model with the PDMS at the front and (c) the rear position. (d) The magnified meshed model of the NGEs in the X-axis orthogonal to the bending axis (Y-axis). (e) The magnified meshed model of the tunable nanogap. No PDMS is filling the nanogap and the PDMS substrate around the nanogap is densely meshed.

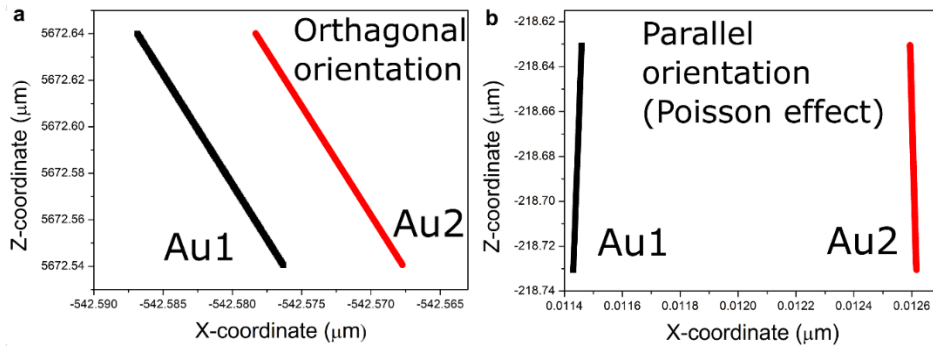
**Table 2.2.** COMSOL parameters of the gap distance tunability simulation.

Parameter		Value
PS cantilever	Length	90 mm
	Width	40 mm
	Thickness	1.18 mm
	Density	1157 kg/m <sup>3</sup>
	Young's modulus	2.6 GPa
	Poisson's ratio	0.4
PDMS	Length	15 mm
	Width	15 mm
	Thickness	3 mm
	Density	970 kg/m <sup>3</sup>
	Young's modulus	1.2 MPa
	Poisson's ratio	0.49
Au electrode	Length	10-50 $\mu$ m
	Width	0.5-2 $\mu$ m
	Thickness	100 nm
	Density	19300 kg/m <sup>3</sup>
	Young's modulus	83 GPa
	Poisson's ratio	0.44
Nanogap distance		10-20 nm
Free end to PDMS distance (Front position)		15 mm
Free end to PDMS distance (Rear position)		70 mm
COMSOL version		5.3
COMSOL Physics		Solid mechanics (solid)
Include geometric nonlinearity		Yes
Solver		Direct solver (MUMPS)
Nonlinear method		Automatic (Newton)
Gravity		On



**Figure 2.8.** COMSOL simulation results of the nanogap tunability. The study of (a) the electrode length, (b) the electrode width, (c) the PDMS position, and (d) the NGEs orientation with respect to the nanogap tunability, respectively. The slope of each curve is defined as the attenuation factor to represent the nanogap tunability.

Figure 2.8a to c shows various curves of NGEs in the orthogonal orientation with different electrode lengths, widths, and PDMS positions, respectively. The significant difference in slopes in Figure 2.8a indicates that the electrode length plays an important role in the attenuation factor. Here, the electrode length is only modeled up to 50  $\mu\text{m}$  to avoid a large amount of mesh and a long computation time. Within this length range, the absolute value of the attenuation factor increases with electrode length. On the other hand, from Figure 2.8b, the electrode width seems to be less relevant to the attenuation factor, regardless of the initial gap distance. Figure 2.8c shows that the attenuation factor with the PDMS at the rear position is higher compared to the case at the front position. As expected, this is due to the difference in the applied strain in both cases as shown in Figure 2.10e. Under the application of the same bending force, the strain applied to the PDMS at the rear position is almost 3 times higher than the strain applied to the PDMS at the front position.



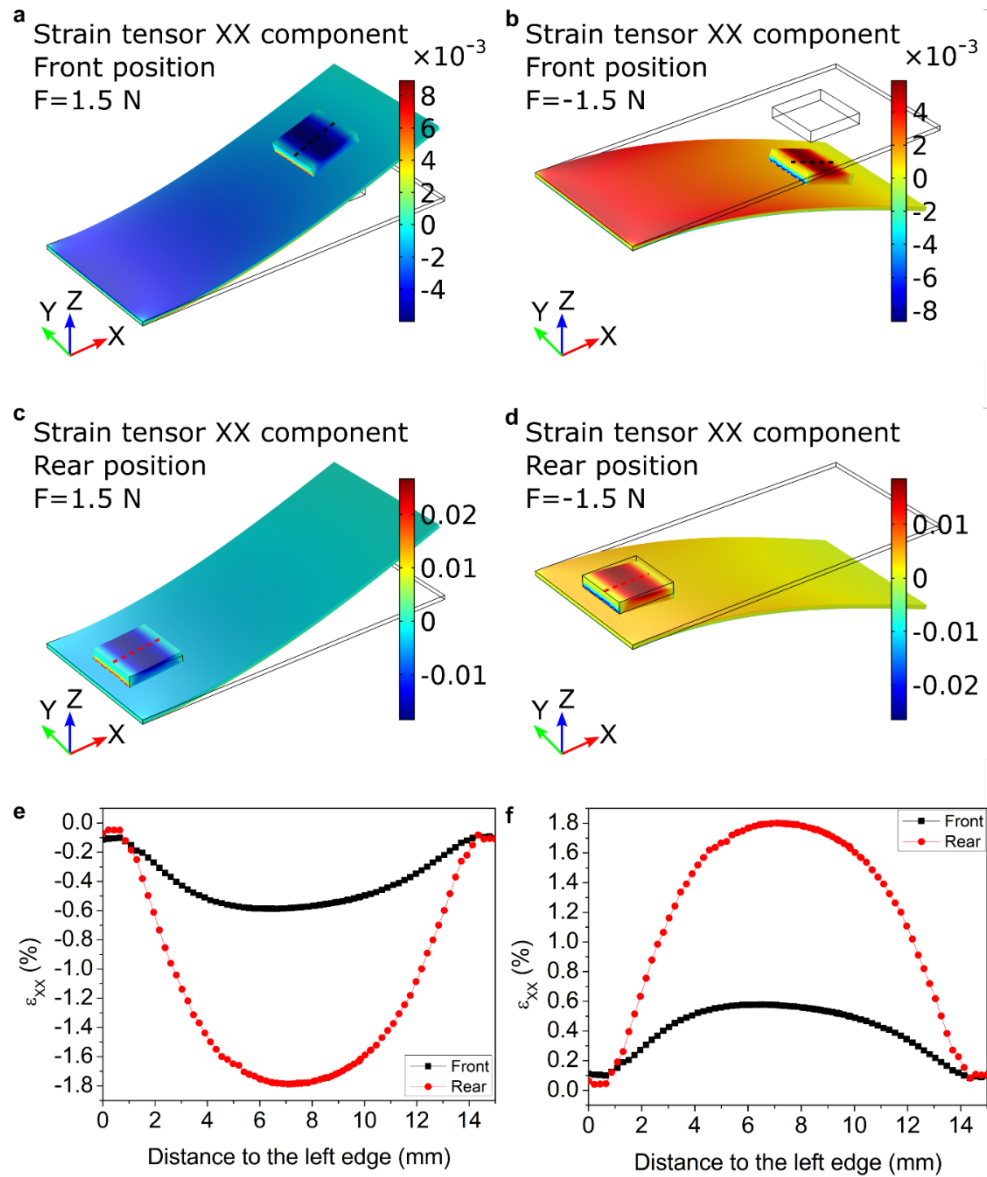
**Figure 2.9.** COMSOL simulation results of the sidewall profiles of the Au electrodes when the PDMS is strained. (a) NGEs are in the orthogonal orientation to the bending axis, the sidewalls of Au1 and Au2 remain parallel to each other. (b) NGEs are in parallel to the bending axis, the top ends of Au1 and Au2 are closer than the bottom ends.

Figure 2.8d shows curves of NGEs in different orientations. In general, the attenuation factor of NGEs in parallel to the PDMS normal is smaller than that of NGEs in the orthogonal orientation. This is because the gap distance is reduced via the Poisson effect with a downward bending in the former case, and the Poisson's ratios of the materials involved here are all smaller than 0.5. The difference in NGEs orientation also results in differences in deformed sidewall profiles of the Au electrodes under strain. As shown in Figure 2.9, the sidewalls of the Au electrodes remain parallel to each other as the NGEs are orthogonal to the bending axis, whereas the Au electrodes become closer to each other at the top ends as the NGEs are parallel to the bending axis. This difference could lead to different effective tunneling areas when the nanogap is in the quantum tunneling regime ( $< 3$  nm) and is subjected to a voltage bias across the nanogap.

Since all the curves in Figure 2.8 show good linearity, the attenuation factors are extracted from the linear regression curves, which are summarized in Table 2.3 for quantitative comparisons. In this study, attenuation factors range from about  $-1 \times 10^{-6}$  to  $-1.2 \times 10^{-5}$ , meaning the nanogap distance can be tuned at 1 nm or even sub-nm step sizes provided the deflection can be controlled at sub-mm step sizes.

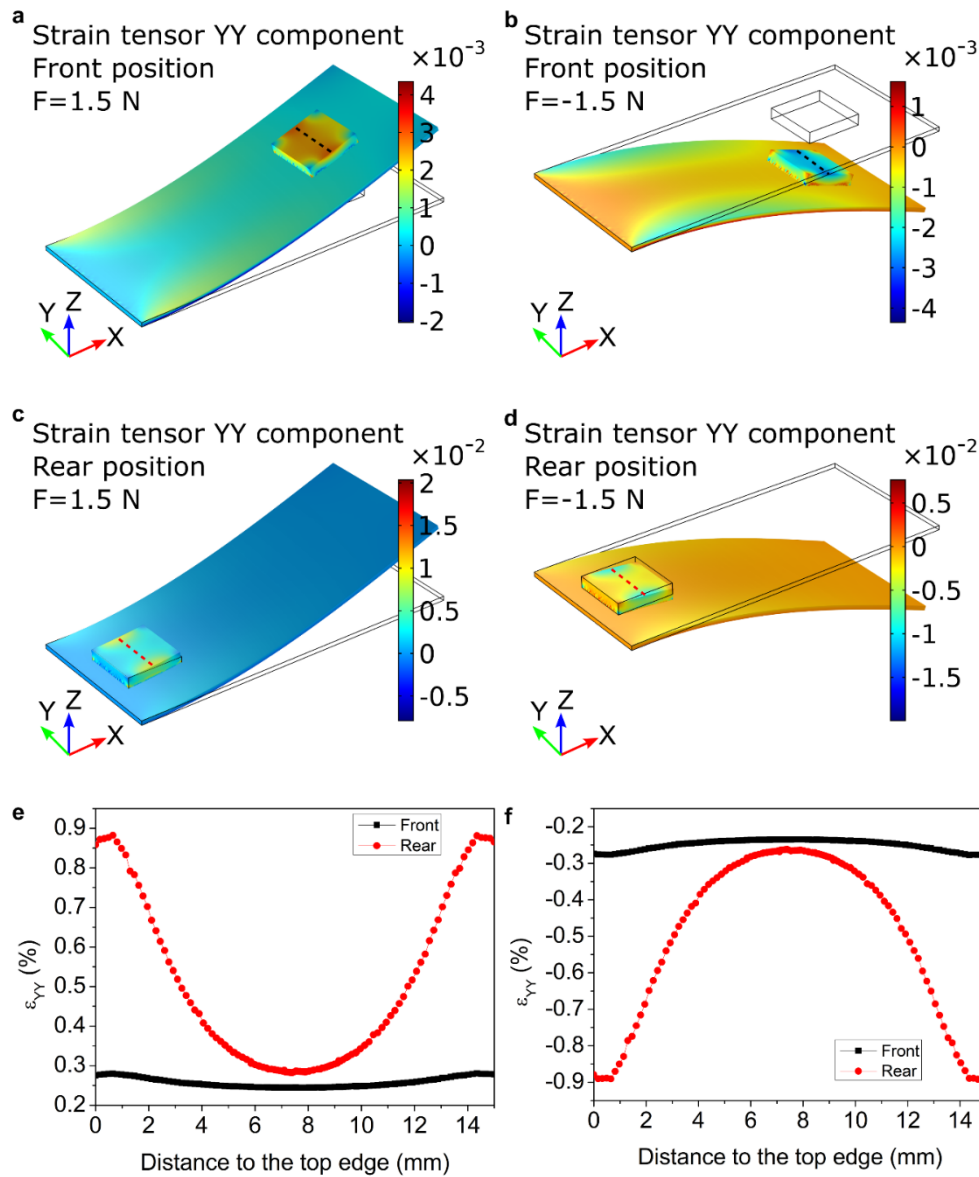
**Table 2.3.** Summary of attenuation factor.

NGEs orientation	PDMS position	Initial gap distance (nm)	Electrode length ( $\mu\text{m}$ )	Electrode width ( $\mu\text{m}$ )	Attenuation factor = $\Delta d/\delta$ ( $10^{-6}$ )
Orthogonal (to the bending axis)	Front	10	10	0.5	-1.9
		10	10	1.0	-1.8
		10	30	0.5	-7.1
		10	50	0.5	-11.7
		20	10	0.5	-2.3
		20	10	1.0	-2.1
		20	10	2.0	-1.9
Orthogonal	Rear	10	10	0.5	-6.1
		20	10	0.5	-6.6
Parallel	Front	10	10	0.5	-1.1
		10	30	0.5	-3.5
Parallel	Rear	10	10	0.5	-1.3
		10	30	0.5	-5.3

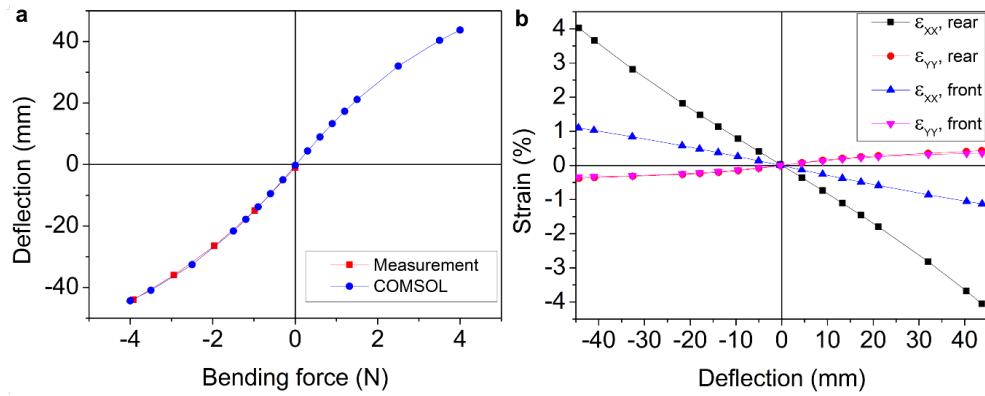


**Figure 2.10.** COMSOL 3D surface plots of the strain tensor XX component of the bent PS cantilever. (a), (b) PDMS at the front position (15 mm from the free end to the PDMS edge) with (a) an upward and (b) a downward bending. (c), (d) PDMS at the rear position (70 mm from the free end to the PDMS edge) with (c) an upward and (d) a downward bending. A force of 1.5 N is uniformly applied to the free end to bend the cantilever. (e), (f) Profiles of strain tensor XX components across the PDMS top surface for the upper bending displayed in (a), (c) and the downward bending in (b) and (d), respectively.





**Figure 2.11.** COMSOL 3D surface plots of the strain tensor YY component of the bent PS cantilever. (a), (b) PDMS at the front position with (a) an upward and (b) a downward bending. (c), (d) PDMS at the rear position with (a) an upward and (d) a downward bending. A force of 1.5 N is uniformly applied to the free end to bend the cantilever. (e), (f) Profiles of strain tensor YY components across the PDMS top surface for the upper bending displayed in (a), (c) and the downward bending in (b) and (d), respectively.



**Figure 2.12.** COMSOL calculation results of the PDMS/cantilever bending. (a) Deflection as a function of applied bending force, simulated (in blue) and experimentally measured (in red) using a linear ruler to measure the deflection in the z-direction with a weight of 0 to 500 g attached to the free end of the PS cantilever. (b) Strain tensor components,  $\epsilon_{XX}$  and  $\epsilon_{YY}$ , at the center point of the PDMS top surface under various bending conditions and PDMS positions. The positive deflection corresponds to upward bending which causes compressive strain in X-direction, and tensile strain in Y-direction due to the Poisson effect.

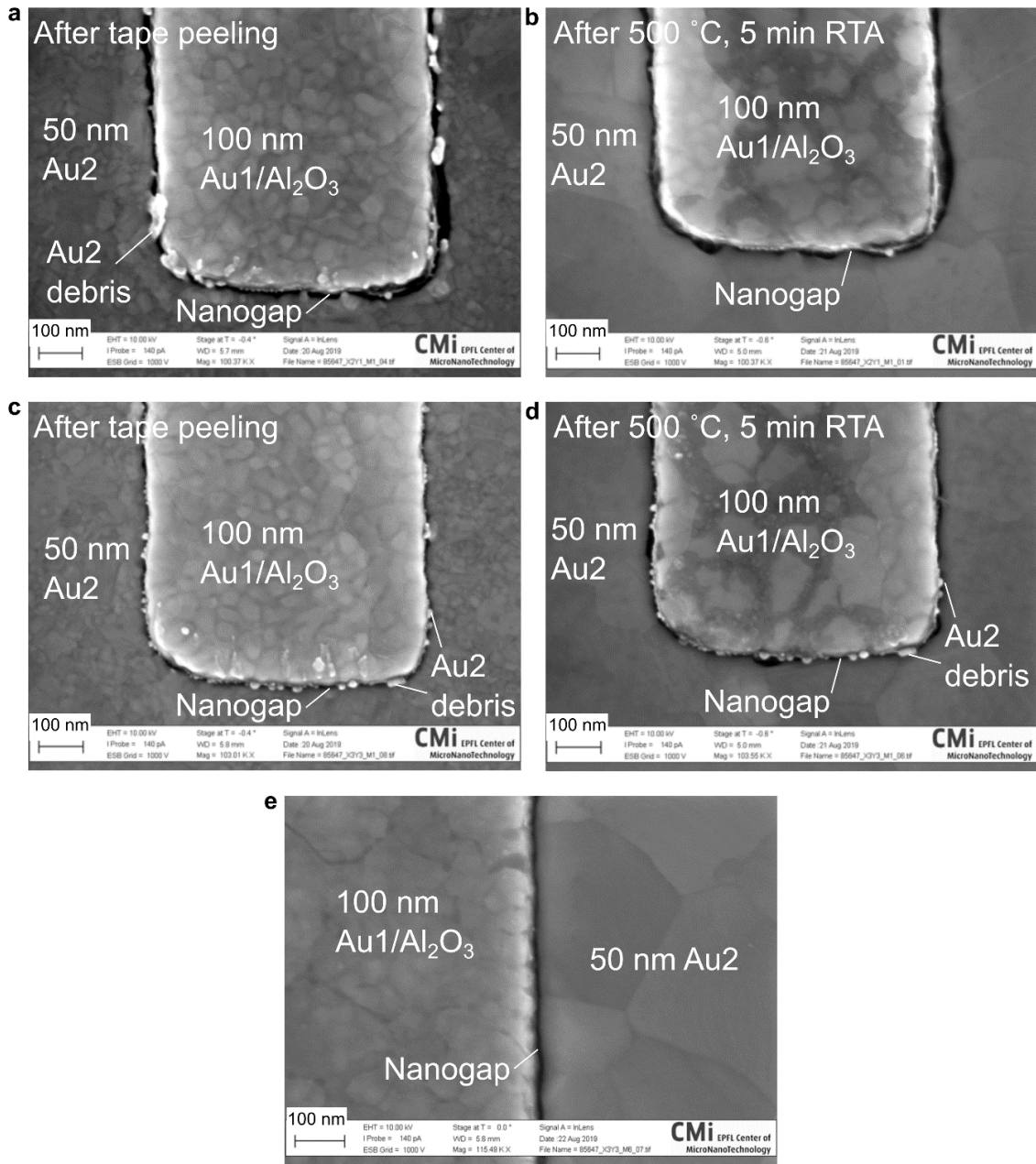
Figure 2.10 and Figure 2.11 show COMSOL simulation results of the strain tensor XX ( $\epsilon_{XX}$ ), and YY ( $\epsilon_{YY}$ ) components of the studied model, respectively. The strain applied on the PDMS substrate by the cantilever bending is not uniform on the PDMS top surface, regardless of the strain direction. As shown in Figure 2.10e and f,  $\epsilon_{XX}$  has a maximum absolute value close to the center of the PDMS substrate, regardless of the PDMS position or bending direction. On the contrary,  $\epsilon_{YY}$  has a minimum absolute value close to the center of the PDMS substrate, regardless of the PDMS position or bending direction (see Figure 2.11e, f). Therefore, the difference in  $\epsilon_{YY}$  at the PDMS center between the front and the rear position is relatively small compared to the other sites on the PDMS substrate. This is the reason why the difference in slope (attenuation factor) between the two curves with parallel orientation is small (-1.1 and -1.3) in Figure 2.8d. These simulation results show the importance of the position of the NGEs on the PDMS in the attenuation factor.

Figure 2.12a shows a non-linear relationship between the bending force and the caused deflection with the given parameters listed in Table 2.2. Figure 2.12b displays the relationships between the deflection and the strain applied at the center point of the PDMS top surface. The linearity of each curve remains good up to 20 mm deflection, which corresponds to 1.7%  $\epsilon_{XX}$  and 0.3%  $\epsilon_{YY}$  for the PDMS at the rear position, and 0.6%  $\epsilon_{XX}$  and 0.3%  $\epsilon_{YY}$  for the PDMS at the front position.

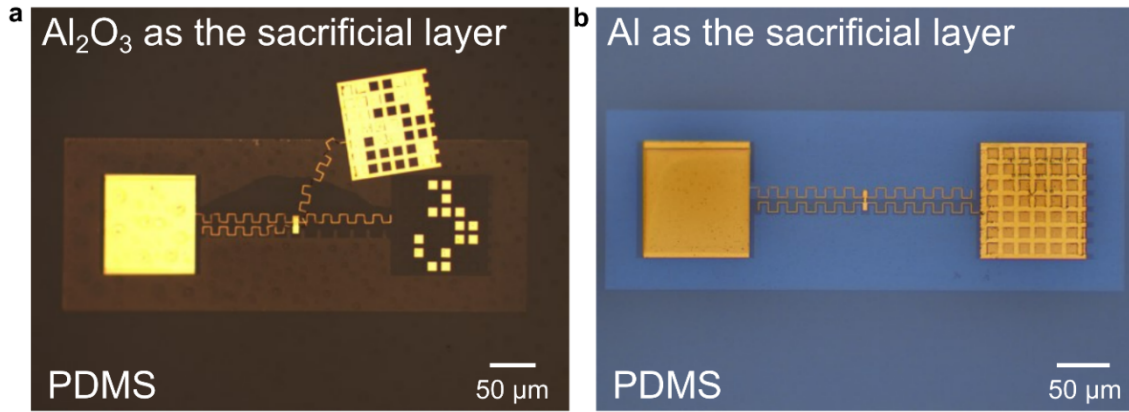
## 2.4 Study of diffusion barrier layer

### 2.4.1 The effect of rapid thermal annealing to NGEs

In previous research, the rapid thermal annealing (RTA) process is reported as a crucial step in obtaining NGEs, and 500 °C in N<sub>2</sub> ambient for 5 min is reported as a proper RTA condition to smooth the edge of the Au2 left over after the tape peeling process.<sup>[41]</sup> Figure 2.13 shows the results of NGEs with a test design in this work after 500 °C, 5 min RTA in N<sub>2</sub> (Jipelec JetFirst 200). The NGEs are fabricated on a 200 nm thick Al<sub>2</sub>O<sub>3</sub> thin film (evaporation, LAB 600H, Leybold Optics) on a Si substrate. In Figure 2.13a, a noticeable amount of Au2 debris around the nanogap is observed after the tape peeling process. The Au2 on this sample is deposited with a deposition rate (4 Å/s) which leads to a fewer amount of Au atom and less continuous film deposited on the sidewall. Hence, more Au2 debris is left around the nanogap after the tape peeling process. After 500 °C, 5 min RTA, the edge of Au2 is smoothed and most of the Au2 debris disappears as shown in Figure 2.13b. However, for some NGEs, a significant amount of Au2 debris is still observed after the RTA process (Figure 2.13c, d), which is presumably an isolated Au2 island on the sidewall. A linear I-V curve with a resistance of a few MOhm and a sudden current drop is measured from such a device after finishing the entire fabrication process, indicating that the remaining Au2 debris might bridge the nanogap and be burned out by the electrical current. The Au2 deposition recipe with a slower deposition rate (0.5 Å/s) is found to deposit thicker Au2 on the sidewall, thus fewer Au2 debris is left around the nanogap after the tape peeling process. As a result, the Au2 debris issue is mitigated by using the Au2 deposition recipe with a slower deposition rate. Further discussion is presented in 2.4.4.



**Figure 2.13.** Effect of 500 °C, 5 min RTA process to NGEs. (a) and (c): SEM images of nanogap electrodes after the tape peeling process and before the RTA process, (b) and (d): after 500 °C, 5 min RTA in N<sub>2</sub> ambient. Most of the Au<sub>2</sub> debris on the Au<sub>1</sub> sidewall is smoothed in (a), however, Au<sub>2</sub> debris on another NGEs in (c) remains after the RTA process. (e) Defect-free nanogap electrodes after 500 °C, 5 min RTA, which can be found on the Si substrates by chance.

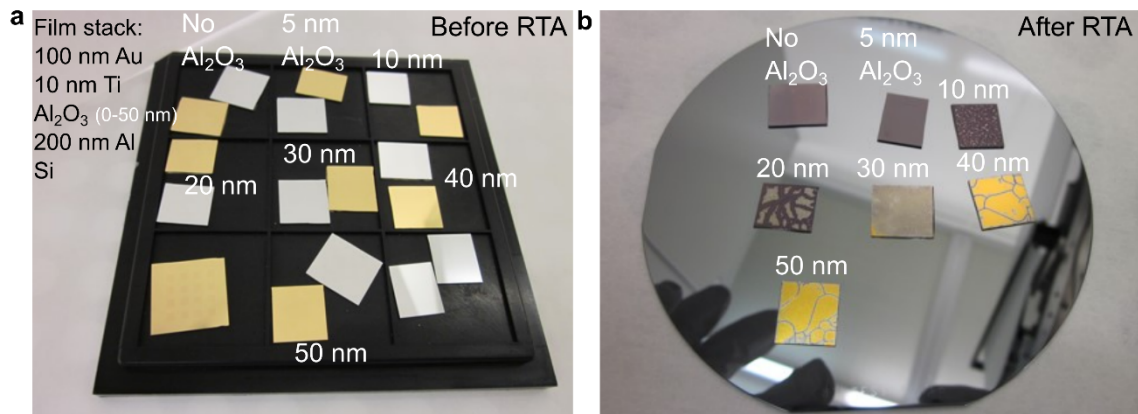


**Figure 2.14.** OM images of wet etching transfer results using different sacrificial layers. (a) Using 200 nm thick  $\text{Al}_2\text{O}_3$  deposited by e-beam evaporation as the sacrificial layer, the wet etching transfer is done in a 60%  $\text{H}_3\text{PO}_4$  bath at 30 °C for 72 h. All devices transferred onto the PDMS substrate are defective presumably due to  $\text{Al}_2\text{O}_3$  thin-film stress. (b) Using 200 nm thick Al deposited by e-beam evaporation as the sacrificial layer, the wet etching transfer is done in a diluted HCl bath (37% HCl : DI water = 1:6, volume ratio) at room temperature for 6 h. Most devices are successfully transferred onto the PDMS substrate. The difference in PDMS color between (a) and (b) is due to the different OM luminance conditions.

### 2.4.2 Sacrificial layer for the wet etching transfer process

In order to minimize the mechanical stress applied on NGEs during the transfer process, wet etching transfer is adopted in this work instead of the dry peeling transfer processes used in literature.<sup>[29,88]</sup> By etching a sacrificial layer between NGEs and the Si substrate in a chemical bath, NGEs are separated from the Si substrate and transferred onto the PDMS substrates. In selecting a proper sacrificial layer, the compatibility of the sacrificial layer with the NGEs fabrication processes (e.g., RTA), as well as the compatibility of the PDMS with the etchant of the sacrificial layer are the primary considerations. A wet etching transfer experiment using  $\text{Al}_2\text{O}_3$  as the sacrificial layer is firstly conducted on account of its compatibility with the RTA process (see Figure 2.13b). 200 nm thick  $\text{Al}_2\text{O}_3$  is deposited by e-beam evaporation (LAB 600H, Leybold Optics) prior to the NGEs fabrication processes (see Table 2.1) and is etched in a 60%  $\text{H}_3\text{PO}_4$  bath at 30 °C for 72 h to transfer NGEs onto the cured PDMS substrate. As the result, partial or entire Au structure dislocation on the PDMS substrate is observed (see Figure 2.14a) in all NGEs devices, which is presumably due to the mechanical stress applied by the  $\text{Al}_2\text{O}_3$  thin film during the transfer process.

On the other hand, previous research reported that the wet etching transfer process using Al as the sacrificial layer and diluted HCl as the etchant enable a promising transfer of Au structures from a Si substrate onto a PDMS substrate.<sup>[37]</sup> Our experiment with 200 nm



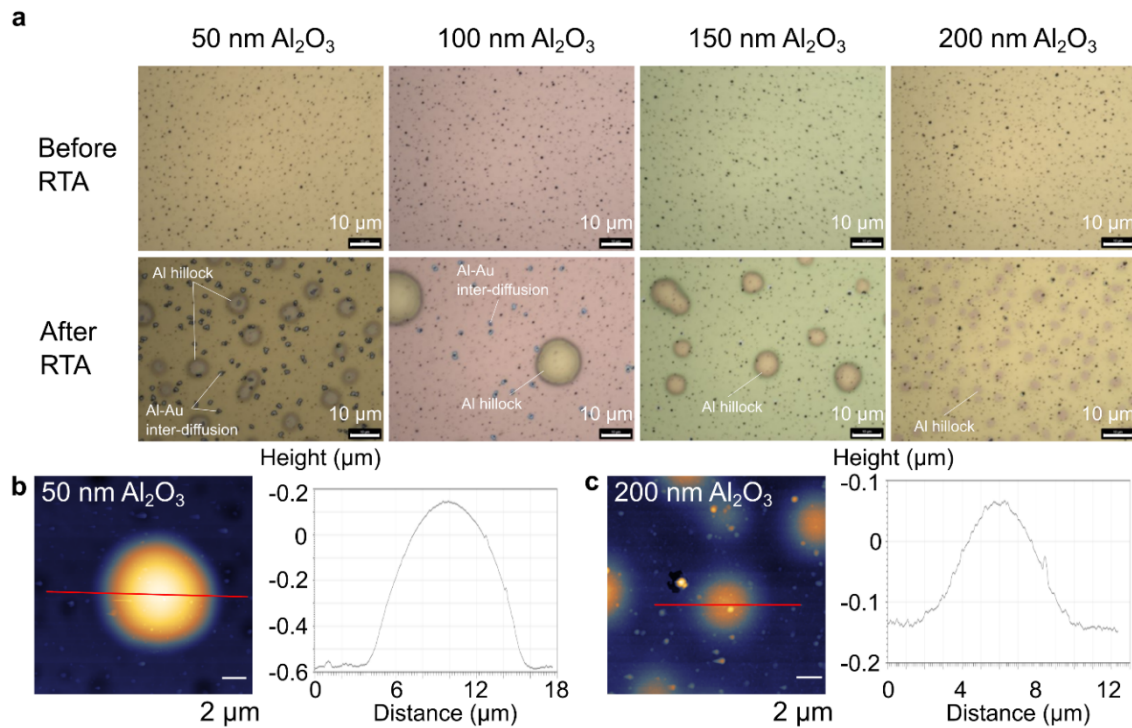
**Figure 2.15.** Result of RTA experiment using Al<sub>2</sub>O<sub>3</sub> as the diffusion barrier layer up to 50 nm. (a) Samples with various Al<sub>2</sub>O<sub>3</sub> thicknesses before the RTA process. Samples of silver color have only 200 nm thick Al/ALD Al<sub>2</sub>O<sub>3</sub> deposition whereas the golden ones have the thin film stack of Al (200 nm) / Al<sub>2</sub>O<sub>3</sub> (0-50 nm ALD) / Ti (10 nm) / Au (100 nm). (b) The golden samples with various Al<sub>2</sub>O<sub>3</sub> thicknesses in (a) after 500 °C, 5 min RTA process in N<sub>2</sub> ambient, showing the different levels of the inter-metallic diffusion between Al and Au across the Al<sub>2</sub>O<sub>3</sub> thin film. The wafer in (b) is a 100-mm wafer.

thick Al (LAB 600H, Leybold Optics) also shows a similar result that almost all of NGEs devices are transferred onto a PDMS substrate without a noticeable dislocation as shown in Figure 2.14b. However, it is known that Au and Al thin films tend to inter-diffuse and form various Au<sub>x</sub>Al<sub>y</sub> phases at elevated temperatures.<sup>[90]</sup> Therefore, using Al as the sacrificial layer is not compatible with the 500 °C, 5 min RTA process, unless a diffusion barrier layer (DBL) is introduced between the Au NGEs and the Al sacrificial layer. Marc-Aurele Nicolet listed the requirements for thin film diffusion barrier in 1978.<sup>[91]</sup> These requirements include limited transportation of the diffusing species across the barrier, low reaction rates with the diffusing species, good adhesion, and mechanical stability.

### 2.4.3 Using ALD Al<sub>2</sub>O<sub>3</sub> as the diffusion barrier layer

Al<sub>2</sub>O<sub>3</sub> thin film deposited by the ALD technique is known as an excellent diffusion barrier layer<sup>[92,93]</sup> thanks to its good conformity and low density of pinholes.<sup>[94,95]</sup> RTA experiments using ALD Al<sub>2</sub>O<sub>3</sub> (BENEQ TFS200) with various thicknesses as the diffusion barrier layer are conducted to find out a minimum thickness to prevent Au and Al thin films from diffusing across the Al<sub>2</sub>O<sub>3</sub> layer. As shown in Figure 2.15a, 0 to 50 nm of ALD Al<sub>2</sub>O<sub>3</sub> are deposited on chips with a 200 nm thick Al thin film, and then 10 nm/100 nm thick Ti/Au is deposited on the Al<sub>2</sub>O<sub>3</sub> layer. After 500 °C, 5 min RTA process in N<sub>2</sub> ambient, Figure 2.15b shows the different levels of the inter-metallic diffusion between Al and Au across the Al<sub>2</sub>O<sub>3</sub> layer with a thickness of 0 to 30 nm. The color of

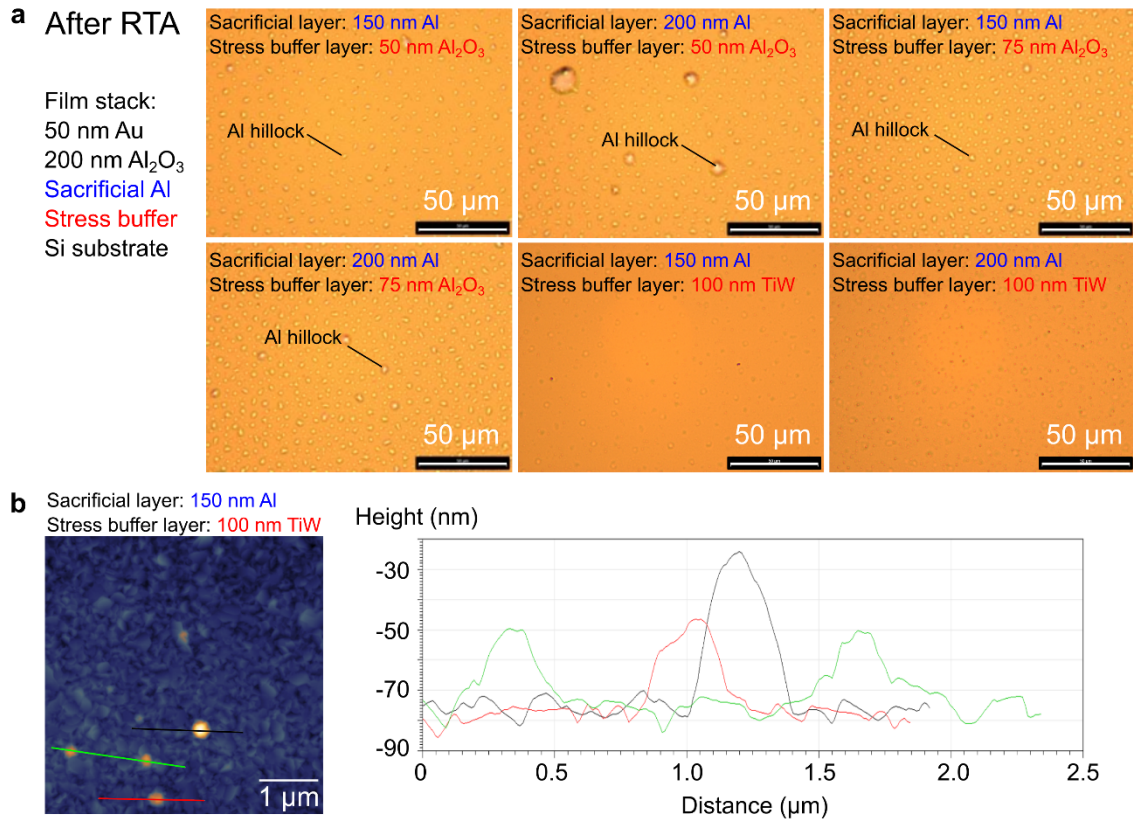




**Figure 2.16.** Result of RTA experiment using  $\text{Al}_2\text{O}_3$  as the diffusion barrier layer up to 200 nm (a) OM images of samples with various thicknesses before and after 500 °C, 5 min RTA process in  $\text{N}_2$  ambient. The thin film stack is 50 nm thick Au/ $\text{Al}_2\text{O}_3$ /200 nm thick Al/Si substrate. Different levels of inter-metallic diffusion and Al hillock are observed after RTA. The black dots in OM images before RTA are the small Al hillock after  $\text{Al}_2\text{O}_3$  ALD process at 300 °C. (b) AFM image and topographical profile of an Al hillock on the sample with 50 nm and (c) 200 nm thick  $\text{Al}_2\text{O}_3$  as the diffusion barrier layer. The heights of Al hillocks in (b) and (c) are about 700 nm and 200 nm, respectively.

Au remains on the test chips with 40 and 50 nm thick  $\text{Al}_2\text{O}_3$ , however, cracks in Au layer are also observed.

Further RTA experiment results using 50 to 200 nm ALD  $\text{Al}_2\text{O}_3$  as the diffusion barrier layer are shown in Figure 2.16. The thin film stack in this experiment is 50 nm thick Au/ $\text{Al}_2\text{O}_3$ /200 nm thick Al on Si substrates. The OM images in Figure 2.16a show that Al-Au inter-diffusion, as well as Al hillocks, are observed on both test chips with 50 and 100 nm thick  $\text{Al}_2\text{O}_3$ , whereas only Al hillocks are seen on the test chips with 150 and 200 nm thick  $\text{Al}_2\text{O}_3$ . Al hillock is an extrusion of film material extracted out of grains or grain boundaries in a process of relieving the compressive stress resulting from a mismatch in the coefficient of thermal expansion (CTE) between Al and the substrate.<sup>[96]</sup> The heights of the Al hillocks on the test chips with 50 and 200 nm thick  $\text{Al}_2\text{O}_3$  are about 700 and 200 nm, respectively, as determined by AFM surface profiles shown in Figure 2.16b, c.



**Figure 2.17.** Result of RTA experiment with various stress buffer layers. (a) OM images of samples with various stress buffer layers after 500 °C, 5 min RTA process in N<sub>2</sub> ambient. The thin film stack is 50 nm thick Au/200 nm thick Al<sub>2</sub>O<sub>3</sub>/sacrificial Al/stress buffer layer/Si substrate. Inter-metal diffusion is not observed in all samples but different levels of Al hillock are still observed after RTA. (b) AFM image and topographical profile of Al hillocks on the sample with 150 nm thick Al sacrificial layer and 100 nm thick TiW stress buffer layer, which shows the mildest Al hillocks in (a). The height of Al hillocks in the AFM image ranges from 30 to 60 nm.

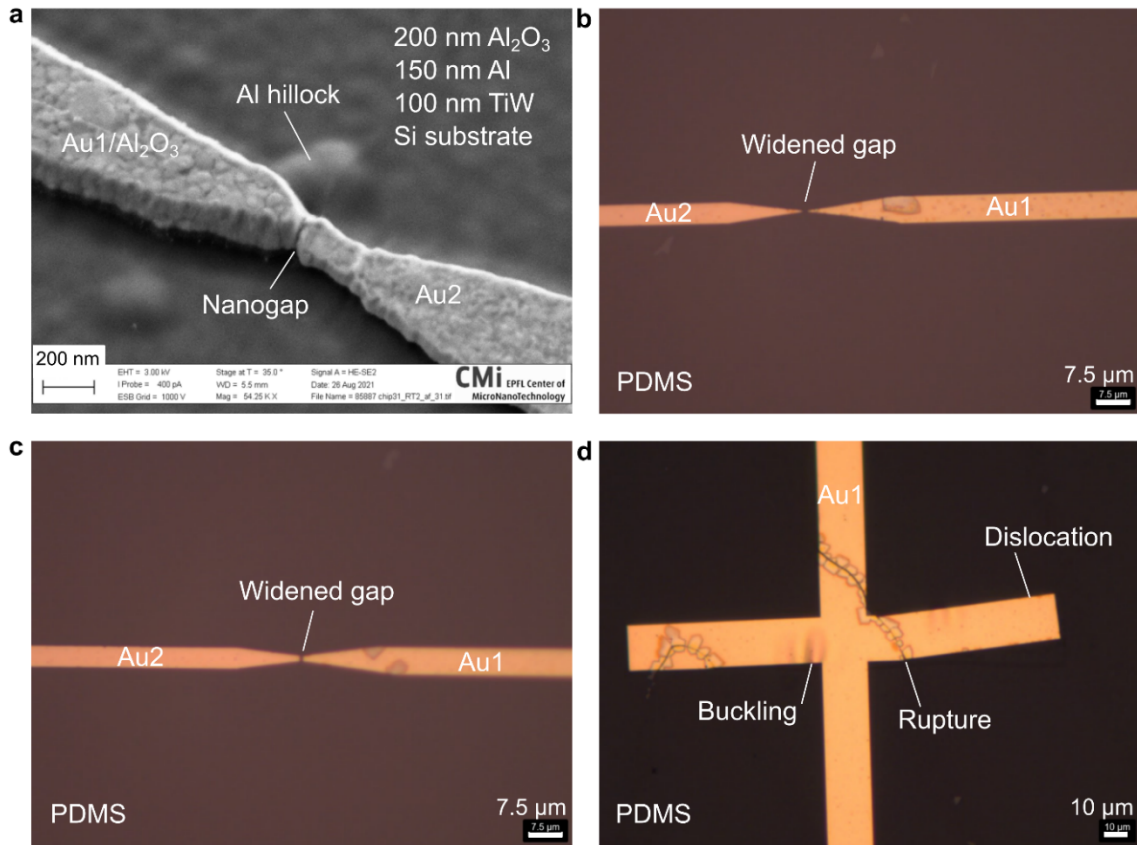
Al hillocks with such heights, densities, and diameters are critical defects to the NGEs fabrication in this work.

A countermeasure is to introduce a stress buffer layer between the Al sacrificial layer and the Si substrate. This stress buffer layer should have an intermediate CTE between Al (~ 18 ppm/k)<sup>[97]</sup> and Si (~ 2.5 ppm/k).<sup>[98]</sup> Figure 2.17 shows the results of the RTA experiment using ALD Al<sub>2</sub>O<sub>3</sub> (CTE= 4.2 ppm/k),<sup>[99]</sup> and TiW (wt. 10% Ti, CTE ~ 5 ppm/k)<sup>[100,101]</sup> with various thicknesses as the stress buffer layer. The thin film stack in this experiment is 50 nm thick Au/200 nm thick Al<sub>2</sub>O<sub>3</sub> DBL/sacrificial Al/stress buffer layer/Si substrate. The sacrificial Al is either 150 or 200 nm thick, whereas the stress buffer layer is one of 50 or 75 nm thick ALD Al<sub>2</sub>O<sub>3</sub> or 100 nm thick TiW (wt. 10% Ti, Alliance-Concept DP 650 sputter). From OM images of each sample after 500 °C, 5 min



RTA process in  $N_2$  ambient, mitigated Al hillocks are observed in all samples. In particular, the sample with 150 nm thick sacrificial Al layer and 100 nm thick TiW allows the smallest Al hillocks among all samples. The height of Al hillocks ranges from 30 to 60 nm, and the diameters are smaller than 500 nm as determined by the AFM scanning result of this sample shown in Figure 2.17b. These findings confirm that the density and size of Al hillocks can be significantly reduced by the introduction of a TiW stress buffer layer under the Al layer. Therefore, a full fabrication process of NGEs using 100 nm thick TiW as the stress buffer layer, 150 nm thick Al as the sacrificial layer, and 200 nm thick ALD  $Al_2O_3$  as the diffusion barrier layer is conducted.

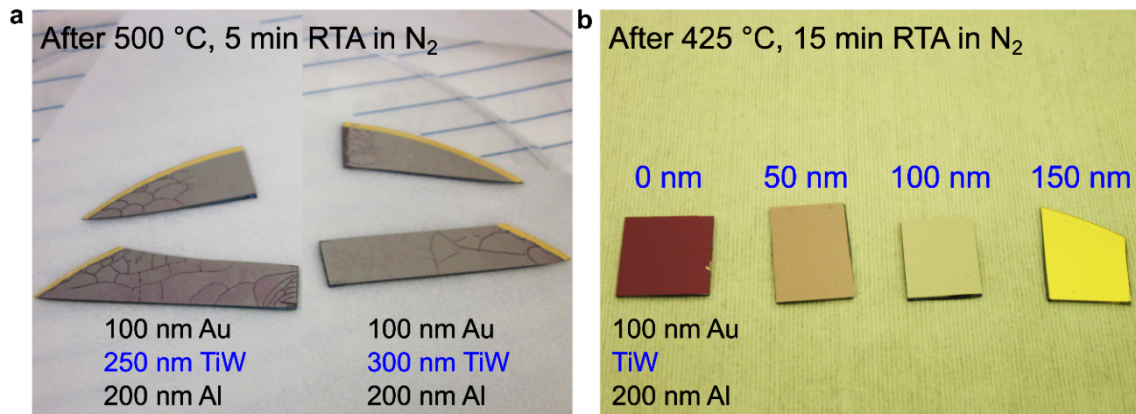
Figure 2.18a shows a tilted-view SEM image of the NGEs using the film stack mentioned above after 500 °C, 5 min RTA and before the wet etching transfer process. Both nanogap (filled with  $\sim 4$  nm ALD  $Al_2O_3$ ) and Au electrodes are well-defined. After PDMS processes (step 23 to 27 in Table 2.1), a sequential wet etching transfer process is done by first removing the Al sacrificial layer (diluted HCl) and then removing the  $Al_2O_3$  DBL (7:1 BOE). As the result, all NGEs devices are transferred onto the PDMS substrate, however, the nanogaps become significantly larger ( $> 500$  nm) as shown in Figure 2.18b, c. Moreover, buckling, ruptures, and dislocation are observed on other patterns such as a cross alignment mark shown in Figure 2.18c. These defects, as well as the enlarged nanogaps, can likely be attributed to the residual thin film stress from the film stack and the insufficient PDMS-NGEs adhesion force.



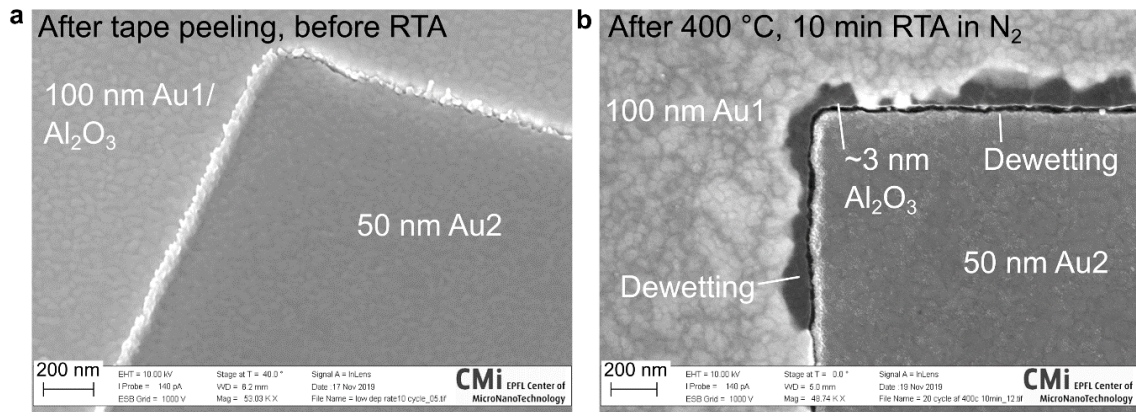
**Figure 2.18.** Fabrication result of NGEs with 200 nm thick Al<sub>2</sub>O<sub>3</sub> as the diffusion barrier layer, 150 nm thick Al as the sacrificial layer, and 100 nm thick TiW as the stress buffer layer. (a) A 35° tilted-view SEM image of NGEs after 500 °C, 5 min RTA process in N<sub>2</sub> ambient and before the wet etching transfer process. (b) and (c) OM images of PDMS substrates with NGEs after the wet etching transfer process. The gaps become larger due to the release of the residual stress of the thin film stack during the wet etching transfer process. Ruptures, buckling, and dislocation of Au1 structure are observed at an Au1 alignment mark in (d).

#### 2.4.4 Using TiW as the diffusion barrier layer

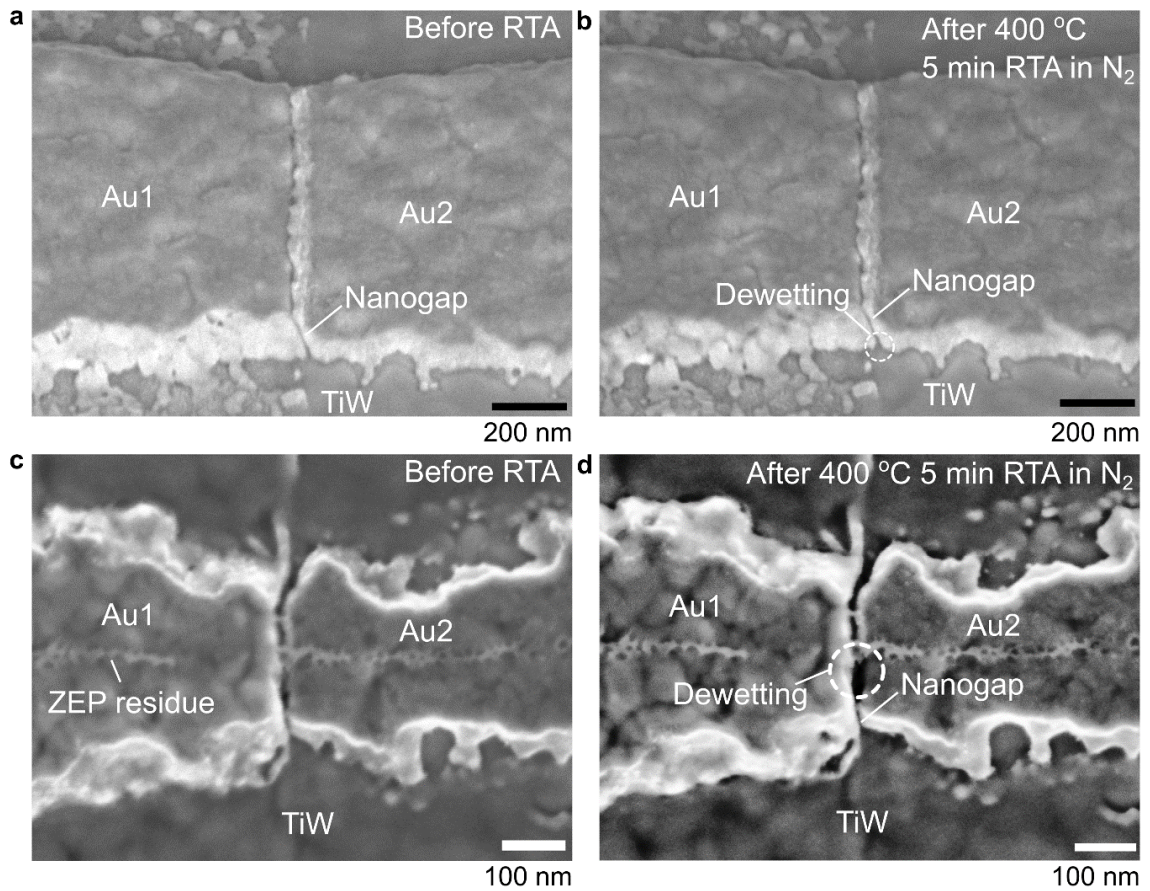
Researches regarding using TiW as a diffusion barrier layer in CMOS technologies can be traced back to 1980s.<sup>[102–104]</sup> In 1987, J. M. Oparowski et al. reported experimental results using TiW (wt. 10% Ti) as the diffusion barrier layer between Au and Al layers.<sup>[87]</sup> Optimization of the sputtering gas mixture of Ar, N<sub>2</sub>, and O<sub>2</sub> during the TiW deposition enables the TiW layer to withstand an annealing process at 450 °C for 1 h. Therefore, a RTA experiment using TiW (wt. 10% Ti, Alliance-Concept DP 650 sputter) as the diffusion barrier layer is also conducted in this work, and the result is shown in Figure 2.19. It is found that 250 nm and 300 nm thick TiW layers both did not significantly



**Figure 2.19.** Results of RTA experiments with TiW as the diffusion barrier layer. (a) OM image of samples with 250 nm thick TiW (left) and 300 nm thick TiW (right) after 500 °C, 5 min RTA process in  $N_2$  ambient. Inter-diffusion between Au and Al is observed on both samples except at the sample edge with golden color where Al is not deposited due to masking by the wafer holder of the evaporator (LAB 600H, Leybold Optics). (b) OM image of samples with 0 to 150 nm thick TiW after 425 °C, 15 min RTA process in  $N_2$  ambient. The Al-Au inter-diffusion is not observed on the sample with 150 nm thick TiW.



**Figure 2.20.** Effect of 400 °C, 10 min RTA process to NGEs on test samples without Al/TiW layers. (a) A 40° tilted-view SEM image of NGEs after the tape peeling process, before the RTA process. (b) A top-view SEM image of NGEs after 400 °C, 10 min RTA process in  $N_2$  ambient. The smoothing of Au2 at the sidewall is observed, and the dewetting effect in both 100 nm thick Au1 and 50 nm thick Au2 is observed as well. The sample in (b) is not the same one as (a) but from the same batch of tape peeling and RTA processes.



**Figure 2.21.** Effect of 400 °C, 5 min RTA process to NGEs. (a) A 40° tilted-view SEM image of NGEs before and (b) after the RTA process. Only slight dewetting of Au1 is observed and no noticeable smoothing of Au2 at sidewall is observed. (c) A top-view SEM image of NGEs from the other chip before and (d) after the RTA process. No Au2 is left at the sidewall on this device and significant dewetting is observed.

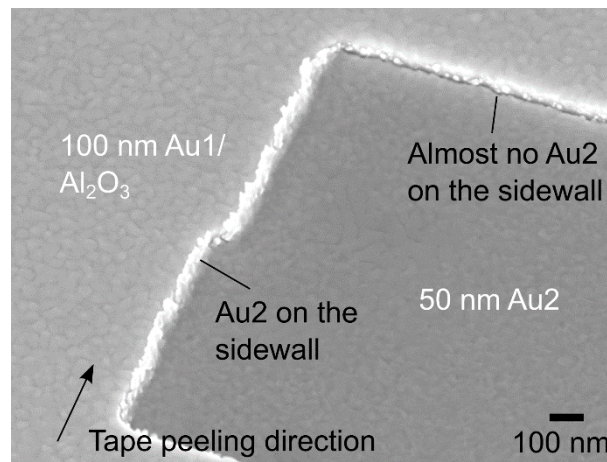
reduce inter-diffusion of Al and Au after 500 °C, 5 min RTA process in N<sub>2</sub> ambient as shown in Figure 2.19a, whereas 150 nm thick TiW is able to retard the Al-Au inter-diffusion up to 425 °C, 15 min RTA in N<sub>2</sub> (Figure 2.19b). Further experiment shows that 100 nm thick TiW is also able to retard the Al-Au inter-diffusion after 400 °C, 10 min RTA in N<sub>2</sub>. However, as shown in Figure 2.20, noticeable Au dewetting effect at the Au-Al<sub>2</sub>O<sub>3</sub> interface<sup>[41,105]</sup> after 400 °C, 10 min RTA in N<sub>2</sub> is observed on NGEs test chips where 100 nm thick Au1 and 50 nm thick Au2 are deposited on 200 nm thick Al<sub>2</sub>O<sub>3</sub> (evaporation, LAB 600H, Leybold Optics). This Au dewetting effect enlarges the gap distance between Au electrodes and hence jeopardizes the intention of the entire NGEs fabrication process.

To reduce the dewetting effect, 400 °C, 5 min RTA in N<sub>2</sub> is eventually adopted with a thin film stack of 150 or 200 nm thick Al as the sacrificial layer and 100 nm thick TiW

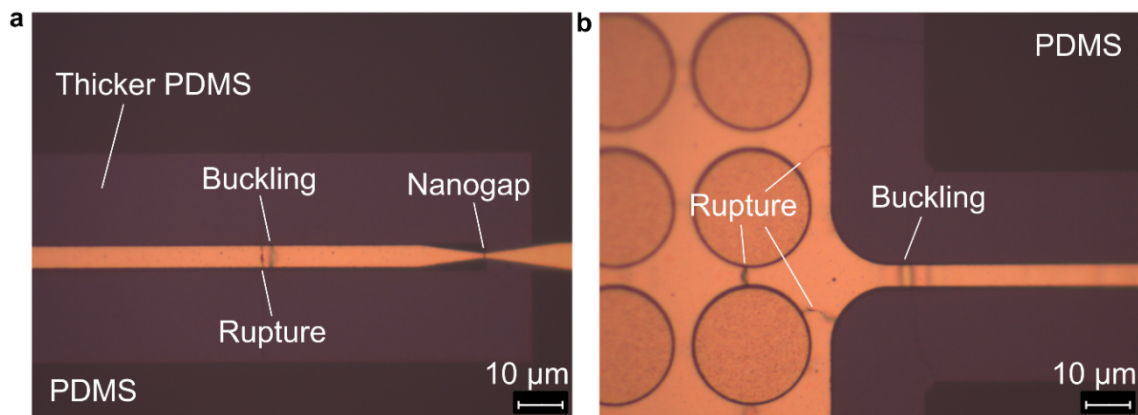


as the diffusion barrier layer (see Table 2.1). NGEs devices are fabricated following the full processes listed in Table 2.1, and Figure 2.21 shows the NGEs before and after the RTA process. As a consequence of slower Au2 deposition ( $0.5 \text{ \AA/s}$ , evaporation), a continuous Au2 at the sidewall without noticeable debris is observed in Figure 2.21a, and only slight dewetting of Au1 is observed in Figure 2.21b. However, on another chip fabricated by the identical but different batch of processes, NGEs devices without Au2 at the sidewall are observed (Figure 2.21c), and the dewetting effect is more obvious as shown in Figure 2.21d. The level of Au2 dewetting is presumably related to the remaining amount of Au2 on the sidewall after the tape peeling process. The remaining amount of Au2 on the sidewall not only depends on the Au2 deposition recipe, but also depends on the orientation of the sidewall with respect to the direction of the tape peeling. As shown in Figure 2.22, a significant difference in the remaining amount of Au2 on the sidewall is observed between two adjacent orthogonal sidewalls. A similar result is also observed in Figure 2.20a.

After the wet etching transfer and the TiW removal processes, NGEs devices discussed above are successfully transferred onto the PDMS substrates. As shown in Figure 2.23, ruptures and buckling on NGEs on the PDMS substrate could be further reduced compared to the samples using  $\text{Al}_2\text{O}_3$  as the diffusion barrier layer (Figure 2.18). Moreover, none of the dislocation defects and the significantly widened gaps as shown in Figure 2.18 are observed. The NGEs devices on the PDMS substrate attached to a PS slab are then subjected to electrical measurement.

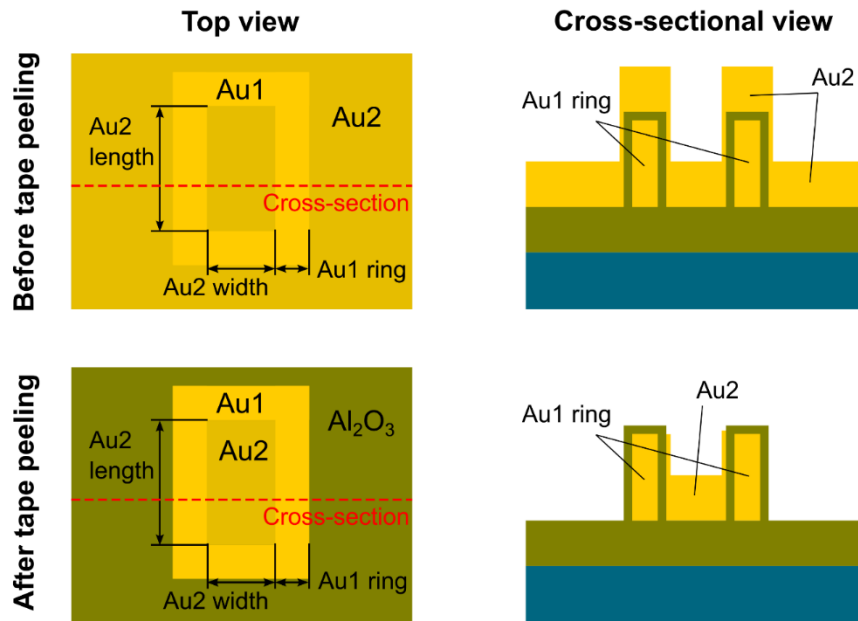


**Figure 2.22.** 40° tilted-view SEM image of NGEs after the tape peeling process. A significant difference in the remaining amount of the Au2 is observed between two adjacent orthogonal sidewalls after the tape peeling process. This result indicates that the remaining amount of the Au2 on the sidewall depends on the orientation of the sidewall with respect to the tape peeling direction.

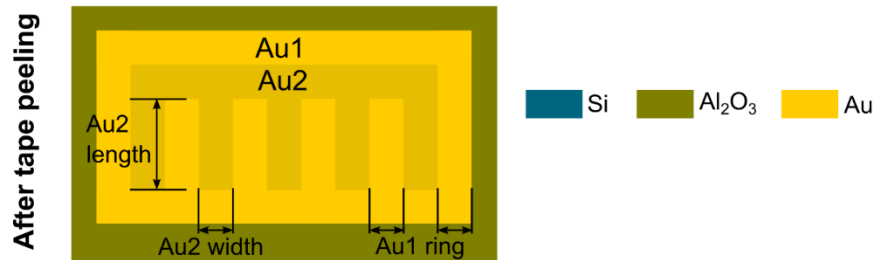


**Figure 2.23.** OM images of NGEs on a PDMS substrate after the wet etching transfer process. The sample has 100 nm thick TiW as the diffusion barrier layer and receives 400 °C, 5 min RTA process in N<sub>2</sub> ambient before the transfer process. The buckling and ruptures of Au thin films due to the release of the residual stress of the thin film stack are still observed, however, the significantly widened gaps as shown in Figure 2.18 are not observed on the PDMS substrate. The color difference in the PDMS substrate is due to the difference in the thickness as a consequence of the topographical replication.

**a Box-in-box test structure**



**b IDE test structure**



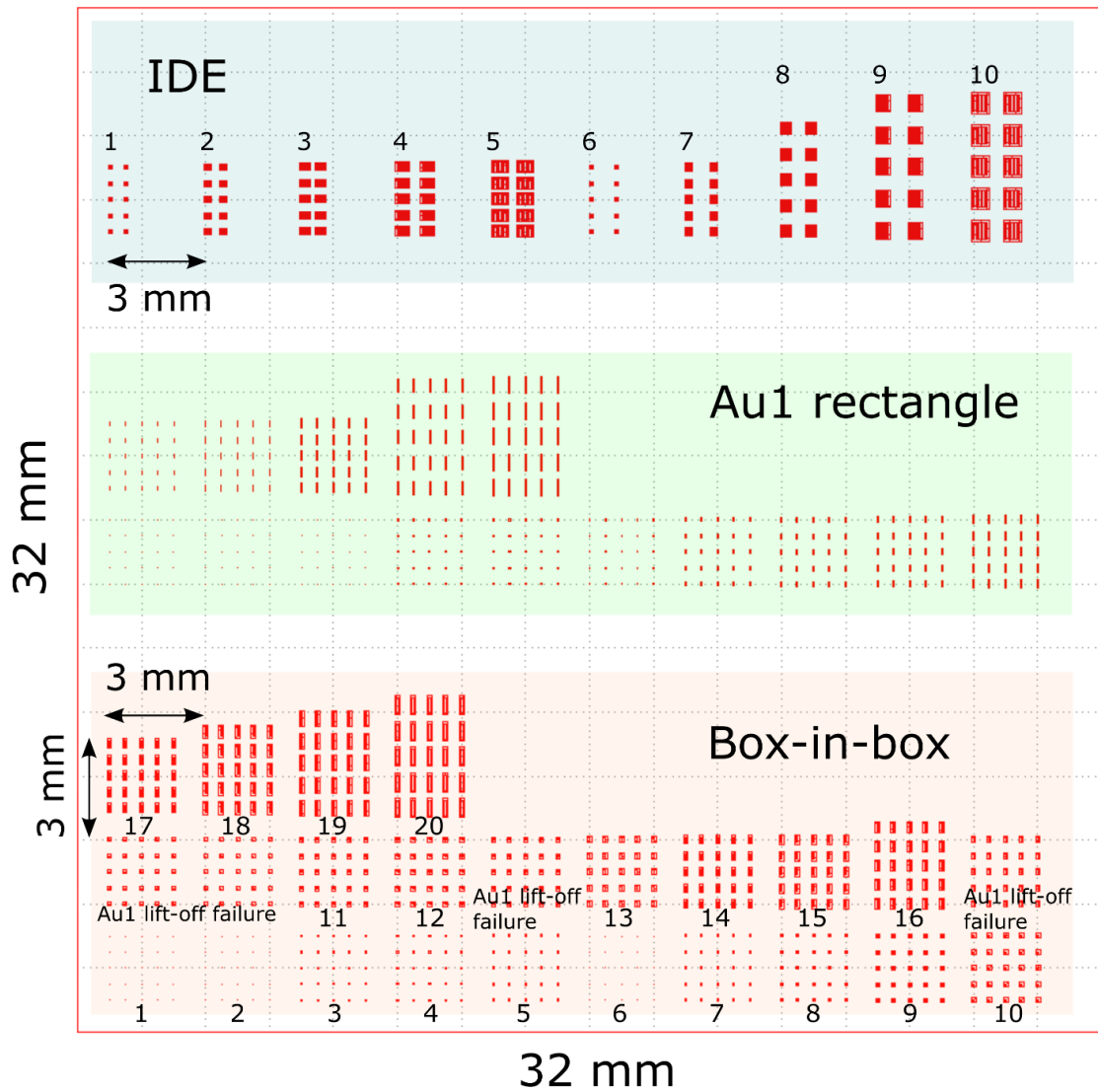
**Figure 2.24.** Illustrations of top and cross-sectional views of the tape peeling test structures. (a) box-in-box, and (b) interdigitated electrode (IDE), 5 Au2 fingers in this experiment.

## 2.5 Yield study of the tape peeling process

The tape peeling process is the essential step of adhesion lithography. From preliminary experiments in this work, it is found that the tape peeling yield is highly related to the NGEs design. Therefore, a systematic yield study is conducted here to understand the design principles of the NGEs.

### 2.5.1 Designs of test structures for yield study

Figure 2.24 shows the cross-sectional and the top views of the test structures fabricated in this experiment. Similar to the copper Damascene process utilized in CMOS technology,<sup>[106]</sup> a successful tape peeling process means specific Au2 areas on the



**Figure 2.25.** Chip layout of test structures for the tape peeling experiment. The detailed information of each test structure is listed in Table 2.4.

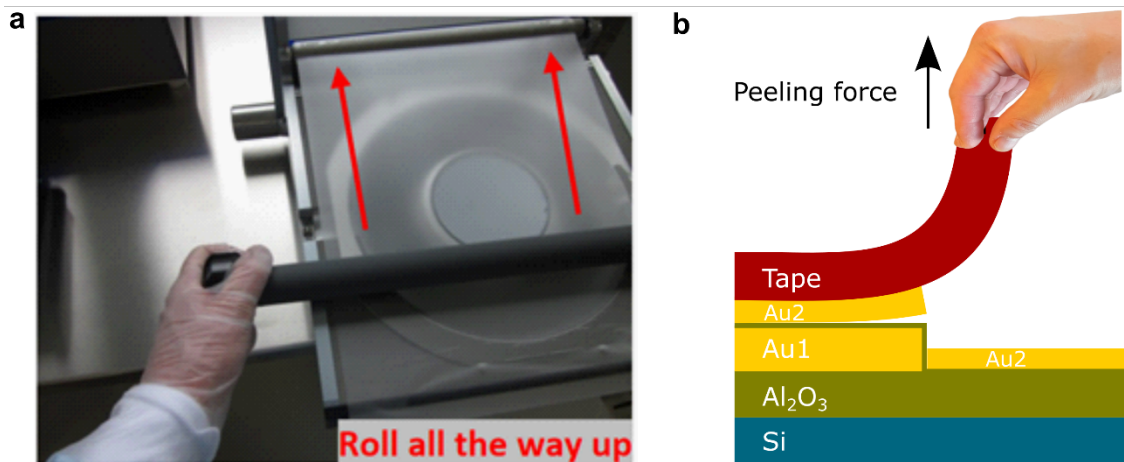
substrate that are surrounded by Au1 structures are kept while the rest of Au2 are removed from the substrate with the tape after the tape peeling process. Therefore, a design referred to as “box-in-box” (Figure 2.24a) which consists of an Au1 ring with uniform width and a surrounded Au2 rectangle is studied in this experiment. 20 box-in-box designs with various Au1 ring widths, as well as various Au2 lengths/widths with different aspect ratios (AR), are included in the chip layout as shown in Figure 2.25. Each of the box-in-box designs is repeated 25 times (in an array of 5 x 5) for the process yield estimation. The structure-to-structure pitches are 0.5 mm and 0.5-0.8 mm in X- and Y-directions, respectively. The array-to-array pitch is 3 mm in both X- and Y-directions.



Apart from the basic box-in-box designs, 10 designs of interdigitated electrodes (IDE, Figure 2.24b) with various dimensions are also included in the chip layout (Figure 2.25) to study the possibility of fabricating dense nanogap electrode arrays using the tape peeling process. Each of the IDE designs is repeated 10 times (in an array of 2 x 5) to estimate the process yield. The array-to-array pitch is 3 mm. The dimensions of each box-in-box and IDE design are listed in Table 2.4.

**Table 2.4.** List of tape peeling test structures with various dimensions.

Test structure	Au1 ring ( $\mu\text{m}$ )	Au2 width ( $\mu\text{m}$ )	Au2 length ( $\mu\text{m}$ )	Au2 AR	Number per run	Pitch X,Y (mm)
Box-in-box 1	5	10	10	1		(0.5, 0.5)
2	5	20	20	1		(0.5, 0.5)
3	5	30	30	1		(0.5, 0.5)
4	5	40	40	1		(0.5, 0.5)
5	5	50	50	1		(0.5, 0.5)
6	10	10	10	1		(0.5, 0.5)
7	20	20	20	1		(0.5, 0.5)
8	30	30	30	1		(0.5, 0.5)
9	40	40	40	1		(0.5, 0.5)
10	50	50	50	1	An array of 5 x 5=25	(0.5, 0.5)
11	50	30	30	1		(0.5, 0.5)
12	50	40	40	1		(0.5, 0.5)
13	50	20	100	5		(0.5, 0.5)
14	50	30	150	5		(0.5, 0.5)
15	50	40	200	5		(0.5, 0.5)
16	50	50	250	5		(0.5, 0.6)
17	50	20	200	10		(0.5, 0.5)
18	50	30	300	10		(0.5, 0.6)
19	50	40	400	10		(0.5, 0.7)
20	50	50	500	10		(0.5, 0.8)
IDE 1	10	10	50	5		(0.5, 0.5)
2	20	20	100	5		(0.5, 0.5)
3	30	30	150	5		(0.5, 0.5)
4	40	40	200	5	An array of 2 x 5=10	(0.8, 0.5)
5	50	50	250	5		(0.8, 0.5)
6	10	10	100	10		(0.8, 0.5)
7	20	20	200	10		(0.8, 0.5)
8	30	30	300	10		(0.8, 0.5)
9	40	40	400	10		(1.0, 1.0)
10	50	50	500	10		(1.0, 1.0)



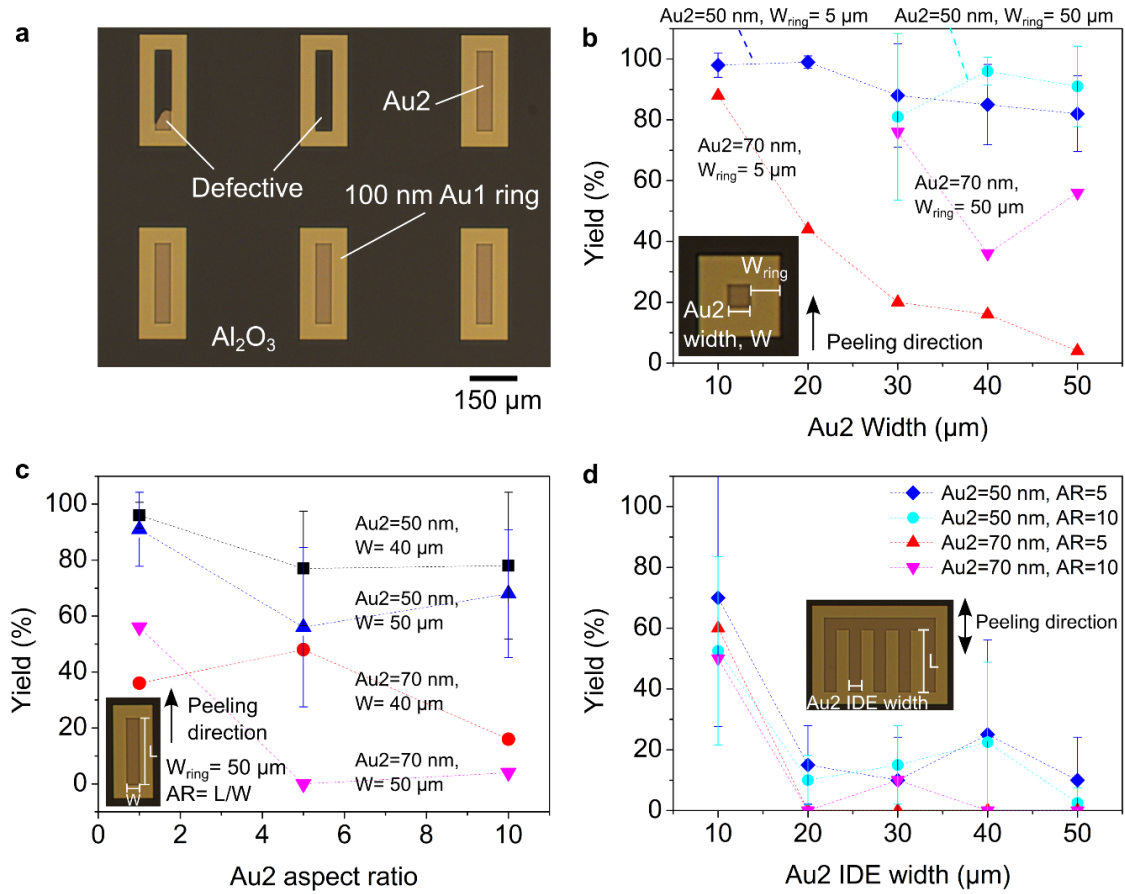
**Figure 2.26.** Illustration of the wafer-level manual tape peeling process. (a) The tape bonding process, a 1.65 kg weight roller is rolled over the substrate to attach the tape on the substrate. (Courtesy of Center of MicroNano Technology, EPFL), and (b) the peeling process, the tape is peeled off the substrate by hand with an upward force.

### 2.5.2 Tape bonding and peeling

As shown in Figure 2.26a, the tape bonding process is done with commercial equipment (POWATEC P-200) which is originally designed for wafer/frame mounting before the wafer grinding process. During the tape bonding process, a commercial polyolefin tape (Adwill E series, LINTEC) is brought in contact with the substrate by rolling manually a 1.65 kg weight roller over the substrate. In this work, the downward vertical force applied by the operator's hands is minimized to keep the applied force on the tape consistent between samples, i.e., only from the weight of the roller. The time span of the rolling procedure is about 3 s to roll over a 100-mm wafer.

After the tape bonding process, the tape is cut and trimmed to be slightly larger than the substrate and separated from the handling metal frame for ease of the subsequent tape peeling process. The tape is then peeled off the substrate by hand with the applied peeling force in parallel to the normal direction of the substrate during the entire peeling process (Figure 2.26b). The time span of the peeling procedure is about 10 s for a 100-mm wafer.

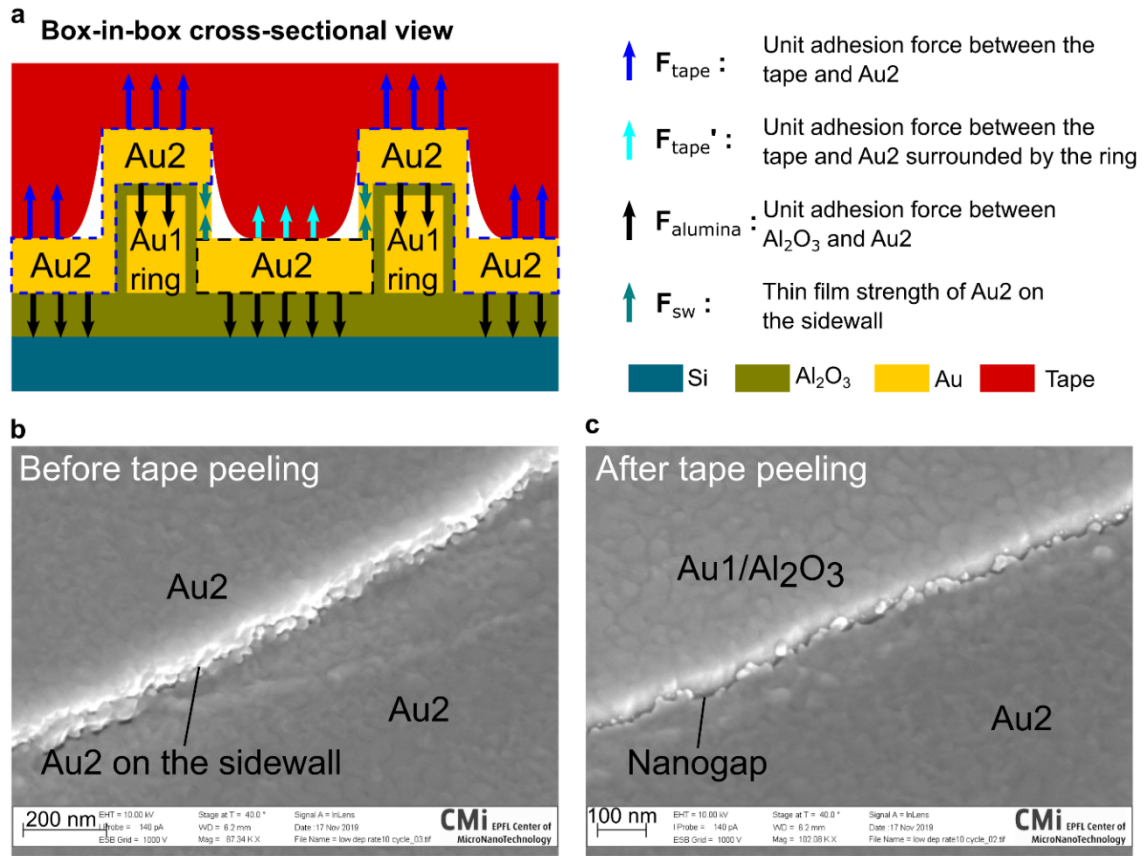
In this experiment, 2 Si wafers are fabricated for different Au2 thicknesses, 50 and 70 nm. There are 4 chips and 1 chip on the wafers of 50 nm and 70 nm thick Au2, respectively. After the deposition of the Au2 layer, the 50 nm Au2 wafer is mechanically cleaved into 4 wafer quarters for 4 tape peeling runs to collect statistical results, whereas the 70 nm Au2 wafer is not cleaved.



**Figure 2.27.** The statistical results of the tape peeling yield study. (a) An OM image of tape peeling test structures after the peeling process for yield calculation. Both partial and total removal of the Au2 inside the Au1 ring is considered defective. (b) The yields of the box-in-box test structure with various Au2 widths,  $W$ . 4 curves corresponding to Au1 ring widths,  $W_{ring}$  of 5 and 50 μm, and Au2 thickness of 50 and 70 nm are shown, respectively. (c) The yields of the box-in-box test structure with Au2 aspect ratios of 1, 5, and 10. The  $W_{ring}$  is 50 μm for all data points. (d) The yields of the IDE test structure with various Au2 IDE widths. 4 curves corresponding to the aspect ratio of 5 and 10, and the Au2 thickness of 50 and 70 nm are shown, respectively. The data points of 50 nm thick Au2 are the mean values of 4 tape peeling runs, and the error bars are  $\pm 1 \sigma$ . The data points of 70 nm thick Au2 are the yields of the single tape peeling run.

### 2.5.3 Result and discussion

The experimental results of the tape peeling yield study are shown in Figure 2.27. Figure 2.27a is an example of OM images of the test structures that are taken after the tape peeling processes. The number of non-defective test structures is counted from the OM images, both partial and total removal of the Au2 inside the Au1 ring are considered defective. The yield is defined as the ratio of the number of non-defective test structures



**Figure 2.28.** (a) Illustration of the cross-sectional view of the box-in-box tape peeling test structure with the force diagram. (b) 40° tilted-view SEM image of an edge of Au1 ring before the tape peeling process. The Au2 deposited on the sidewall is visible. (c) 40° tilted-view SEM image of an edge of Au1 ring after the tape peeling process. Au2 is torn and broken on the sidewall. The top surface of Au1/ $\text{Al}_2\text{O}_3$  and the nanogap are revealed.

to the total number of test structures (see Table 2.4). Figure 2.27b shows the yield results of the box-in-box test structures with various Au2 widths ( $\text{AR} = 1$ ). The blue and red curves are the results of 50 nm and 70 nm thick Au2, respectively. Both curves show that the yield is lower as the Au2 width is larger. The trend is particularly obvious in the case of 70 nm thick Au2.

In order to gain more insights from the experimental results, a schematic diagram of force analysis of the tape peeling process is shown in Figure 2.28a. 4 forces that are relevant to the tape peeling process are identified: (1)  $F_{\text{tape}}$  ( $\text{N/m}^2$ ), the unit Van der Waals adhesion force between the tape and the Au2 top surface. (2)  $F_{\text{tape}'}$  ( $\text{N/m}^2$ ), the unit Van der Waals adhesion force between the tape the Au2 inside the Au1 ring. (3)  $F_{\text{alumina}}$  ( $\text{N/m}^2$ ), the unit Van der Waals adhesion force between the  $\text{Al}_2\text{O}_3$  top surface and the Au2 bottom surface. (4)  $F_{\text{sw}}$  ( $\text{N/m}^2$ ), thin film strength of the Au2 on the sidewall. To have a successful tape peeling process, two hypothetical criteria must be fulfilled:

$$(1) F_{tape} * A_{ring} > F_{alumina} * A_{ring} + F_{sw} * t_{sw} * P_{Au2}$$

$$(2) F_{alumina} * A_{Au2} > F_{tape}' * A_{Au2} + F_{sw} * t_{sw} * P_{Au2}$$

, where

$A_{ring} \text{ (m}^2\text{)} = 2 * W_{ring} * (L + W + 2 * W_{ring})$ , is the area of the Au1 ring.

$t_{sw} \text{ (m)}$  is the thickness of Au2 on the sidewall.

$P_{Au2} \text{ (m)} = 2 * (L + W)$ , is the perimeter of the Au2 inside the Au1 ring.

$A_{Au2} \text{ (m}^2\text{)} = L * W$ , is the area of the Au2 in the ring.

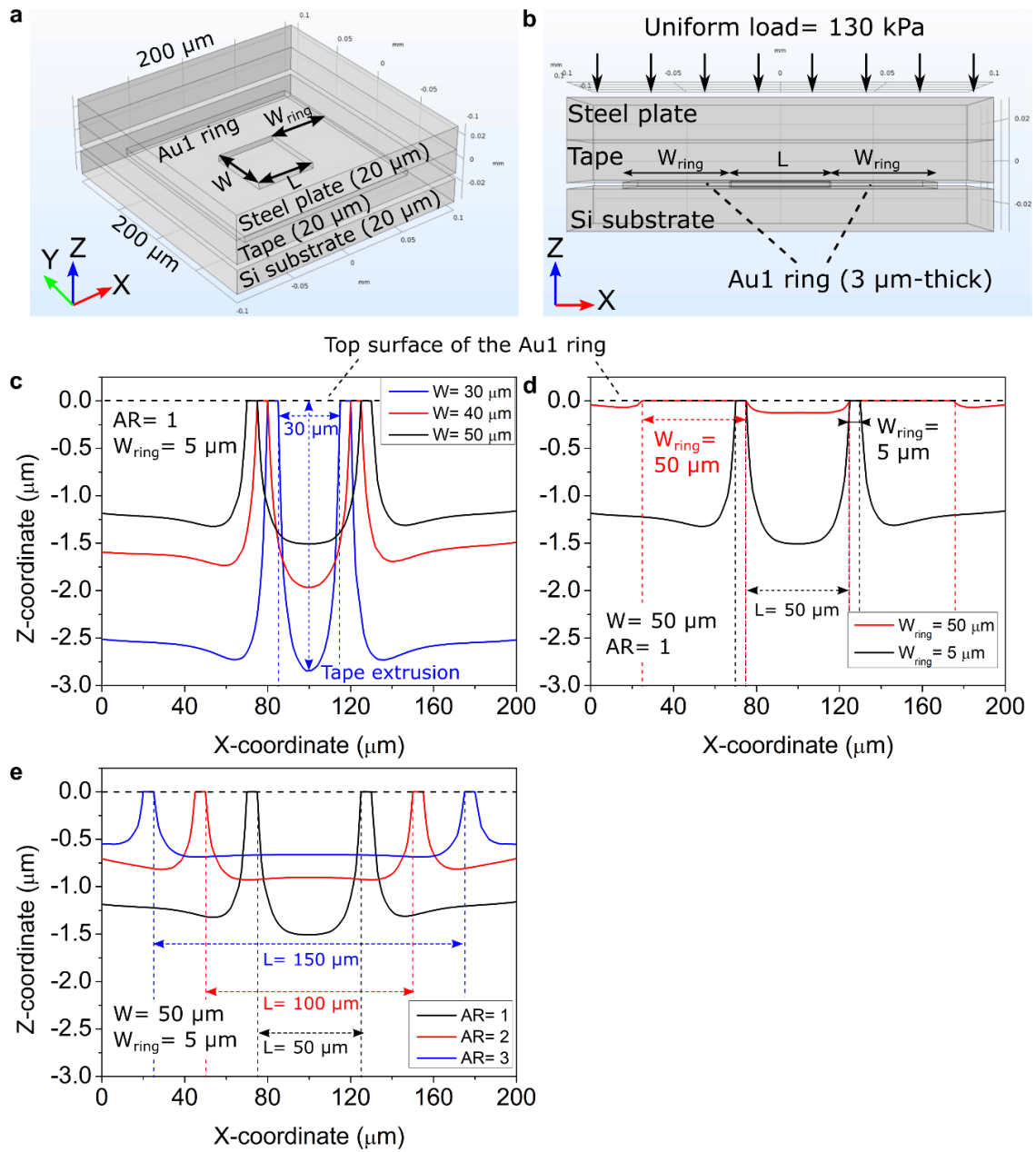
$W_{ring} \text{ (m)}$  is the width of the Au1 ring.

$L \text{ (m)}$  and  $W \text{ (m)}$  are the length and the width of the Au2 in the ring, respectively.

The fulfillment of the first criteria suggests  $F_{tape} > F_{alumina}$ , hence the Au2 on top of the Au1 ring, as well as the Au2 outside of the Au1 ring, are removed, whereas the fulfillment of the second criteria means the Au2 in the ring is adhered by  $F_{alumina}$  and is not peeled off during the tape peeling process.

With these forces and the criteria identified, a COMSOL simulation study is then conducted to show how the different dimensions of the test structures affect  $F_{tape}'$ , which is an important factor in the criteria (2). As shown in Figure 2.29a, b, a simplified model using a plain steel plate, instead of a circular roller, to apply a uniform load to deform a soft tape that is in contact with an Au1 ring structure on a Si substrate. Since the meshing and the convergence are challenging and time-consuming with a large area, 100 nm thick thin film of Au1 ring, the Au1 ring is set to be 3  $\mu\text{m}$  thick instead, so that the tape deformation inside the Au1 ring is calculated as an indicator of  $F_{tape}'$ . A larger tape deformation suggests a larger  $F_{tape}'$  applied on the Au2 inside the Au1 ring in the experimental cases. The elastic modulus of the tape is set as a typical value of a polyolefin tape, 20 MPa. For ease of convergence, the tape thickness is set to be 20  $\mu\text{m}$  instead of 140  $\mu\text{m}$  as the real case since the tape thickness in the model only affects the tape deformation outside the Au1 ring but not inside. The uniform loading is set to be 130 kPa since in the real case a roller of 1.65 kg weight is rolling over a quarter wafer with an assumed roller-tape contact area of 2.5 x 50  $\text{mm}^2$ .

Figure 2.29c shows 3 profiles of the bottom surface of the deformed tape with  $W$  of 30, 40, and 50  $\mu\text{m}$ . The extrusion, i.e., the tape deformation inside the Au1 ring, is smaller as  $W$  is larger, which means  $F_{tape}'$  is smaller with a larger  $W$ . However,  $P_{Au2}$  is proportional to  $W$ , which leads to a larger total force  $F_{sw} * t_{sw} * P_{Au2}$  at the right-hand side of the criteria (2) as  $W$  is larger. This explains the correlation between the yield and  $W$  shown in Figure 2.27b. Moreover, with the same  $W$ , yields of 70 nm thick Au2 (red curve) are in general significantly lower than those of 50 nm thick Au2 (blue curve). The difference in Au2 thickness does not result in a difference in the height nor in the lateral dimensions of the ring structure, which means  $F_{tape}'$  and  $P_{Au2}$  are the same for both cases of 50 nm and 70 nm thick Au2. However, the thicker Au2 deposition leads to larger  $t_{sw}$  (see Figure 2.28b) and results in a larger total force  $F_{sw} * t_{sw} * P_{Au2}$  at the right-hand side of the criteria (2).



**Figure 2.29.** COMSOL simulation study for the tape peeling experiments. (a) Isometric view and (b) cross-sectional view of the COMSOL model. (c) to (e) are the deformed profiles of the tape bottom surface under the same uniform load (130 kPa): (c) with different  $W$ , (d) with different  $W_{ring}$ , and (e) with different aspect ratios. The elastic modulus of the tape is set to be 20 MPa. The larger tape extrusion here indicates the larger  $F_{tape}'$ .

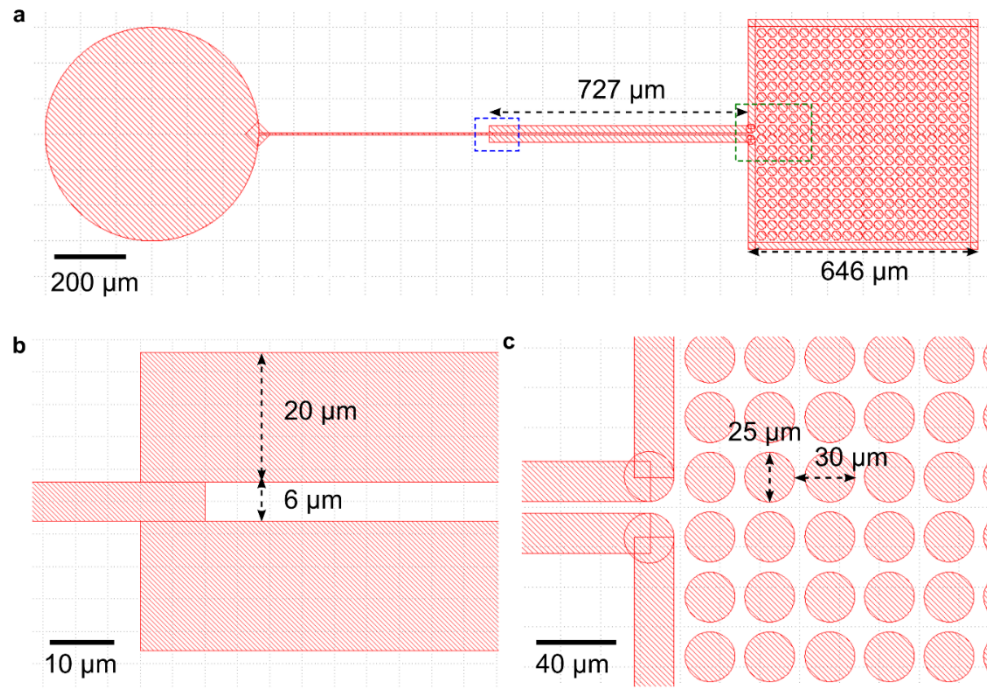
A larger  $t_{sw}$  is also observed as the Au2 layer is deposited with a slower deposition rate. As a consequence, the probability of accidentally removing the Au2 inside the ring during the peeling process increases with  $t_{sw}$  and reduces the overall tape peeling yield.

For  $W \geq 30 \mu\text{m}$  in Figure 2.27b, the yields of  $W_{ring} = 50 \mu\text{m}$  (cyan and pink curves) are significantly higher than the yields of  $W_{ring} = 5 \mu\text{m}$  (blue and red curves). This can be explained by the COMSOL study results shown in Figure 2.29d where two cases of  $W_{ring} = 5$  and  $50 \mu\text{m}$  are studied for comparison. Under the same load, the tape extrusion of  $W_{ring} = 50 \mu\text{m}$  (red profile) is much smaller than that of  $W_{ring} = 5 \mu\text{m}$  (black profile). This result suggests a smaller  $F_{tape}'$  is produced with a larger  $W_{ring}$ , which reduces the total force at the right-hand side of the criteria (2). Therefore, the yield of tape peeling is higher with a larger  $W_{ring}$  than with a smaller one.

Figure 2.27c shows the tape peeling yield results of various Au2 aspect ratios. The larger Au2 aspect ratio generally results in a lower yield. Similar to the results and the explanation regarding different  $W$  (Figure 2.29c), the COMSOL study results of various Au2 aspect ratios in Figure 2.29e also show that the larger aspect ratio leads to a smaller tape extrusion, i.e., a smaller  $F_{tape}'$ . As  $P_{Au2}$  increases with the aspect ratio, the yield drops. Therefore, higher yields are observed with  $W = 40 \mu\text{m}$  (black and red curves) than with  $W = 50 \mu\text{m}$  (blue and pink curves) due to the smaller  $P_{Au2}$ . The same observation is obtained in the case of IDE test structures as shown in Figure 2.29d, where the yields of Au2 IDE width  $\geq 20 \mu\text{m}$  are low due to the large  $P_{Au2}$  in these cases.

In summary, a combination of a thinner Au2 layer and a design of Au1 with larger Au1 ring width and a smaller perimeter of the Au2 inside the Au1 ring results in a higher tape peeling yield. Table 2.5 summarizes the factors that decide the magnitude of the 4 forces aforementioned that are relevant to the tape peeling process. For the design in this work as shown in Figure 2.30, the electrode area (Figure 2.30b) has an Au2 width of  $6 \mu\text{m}$  and a length of  $725 \mu\text{m}$ , and an Au1 ring width of  $20 \mu\text{m}$ , and the pad area (Figure 2.30c) has a pad width of  $646 \mu\text{m}$  and a pillar array with a pillar diameter of  $25 \mu\text{m}$  and a pitch of  $30 \mu\text{m}$ . The pillar array added in the pad area serves the role of the Au1 ring. With  $50 \text{ nm}$  thick Au2 deposited, 3 tape peeling runs are done with full  $100\text{-mm}$  wafers, the yields of each run are 94.4% of 72 devices, 95.7% of 208 devices, and 82.7% of 104 devices. More extensive investigations are required to comprehend the mechanics of the tape peeling process with such a complex design.





**Figure 2.30.** The Au1 design of the NGEs in this work. (a) The full view. (b) The magnified view of the blue rectangle in (a) showing the NGEs area. (c) The magnified view of the green rectangle in (a) showing the pad area.

**Table 2.5.** Deciding factors of the relevant parameters of the tape peeling process.

Parameter	Description	Deciding factors (+): positive correlation (-): negative correlation
$F_{tape}$ (N/m <sup>2</sup> )	The unit Van der Waals adhesion force between the tape and the Au2 top surface	Tape material (+ or -) Au2 deposition recipe (+ or -) Tape bonding force (+)
$F_{tape}'$ (N/m <sup>2</sup> )	The unit Van der Waals adhesion force between the tape the Au2 inside the Au1 ring	Tape material (+ or -) Au2 deposition recipe (+ or -) Tape bonding force (+) Au2 width, $W$ (-) Au2 length, $L$ (-) Au1 ring width, $W_{ring}$ (-)
$F_{alumina}$ (N/m <sup>2</sup> )	The unit Van der Waals adhesion force between the Al <sub>2</sub> O <sub>3</sub> top surface and the Au2 bottom surface	ALD recipe (+ or -) Au2 deposition recipe (+ or -)
$t_{sw}$ (m)	The thickness of the Au2 on the sidewall	Au2 deposition rate (-) Au2 thickness (+)



## 2.6 Electrical characterization of the NGEs

Since it is challenging to reliably observe the nanogap on PDMS by direct imaging methods, electrical characterization of the NGEs is conducted in order to confirm whether the fabricated NGEs on PDMS are tunable in the tunneling regime.

### 2.6.1 Theory of metal-insulator-metal tunneling

In 1963, John G. Simmons reported a generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film.<sup>[107]</sup> In particular, the tunneling current across a metal-insulator-metal (MIM) with the same electrode material can be also described by this formula. When the applied voltage is small, the Simmons model of a symmetrical MIM junction is simplified to the following equation:

$$J = \frac{3e^2\sqrt{2m\Phi}}{2dh^2} V * \exp\left(\frac{-4\pi d}{h}\sqrt{2m\Phi}\right) \quad \text{Eq. 2.1}$$

, where

$J$  : the current density,

$V$  : the voltage across the insulating film,

$h$  : the Planck constant,

$d$  : the gap distance (i.e. insulating film thickness),

$e$  : the electron charge,

$m$  : the electron mass,

$\Phi$  : the height of the rectangular energy barrier.

In this regime, the quantum phenomenon is called “direct tunneling” which is first described by Sommerfeld and Bethe.<sup>[108]</sup> With a fixed gap distance, the current density is proportional to the applied voltage.

When the applied voltage is high ( $V > (\Phi + E_F)/e$ ,  $E_F$  is Fermi level), the Simmons model of a symmetric MIM junction is simplified to the following equation which describes the phenomenon of Fowler-Nordheim (F-N) field emission tunneling:<sup>[109]</sup>

$$J = \frac{2.2e^3}{8\pi h\Phi d^2} V^2 * \exp\left(\frac{-8\pi d\Phi}{2.96heV}\sqrt{2m\Phi}\right) \quad \text{Eq. 2.2}$$

, where a linear correlation between  $\ln(J/V^2)$  and  $1/V$  is found. Therefore, the F-N field emission tunneling is often presented in the plot with  $1/V$  as the X-axis and  $\ln(I/V^2)$  as the Y-axis (i.e., F-N representation) to show a straight line in a high-voltage (i.e. low  $1/V$ ) range.

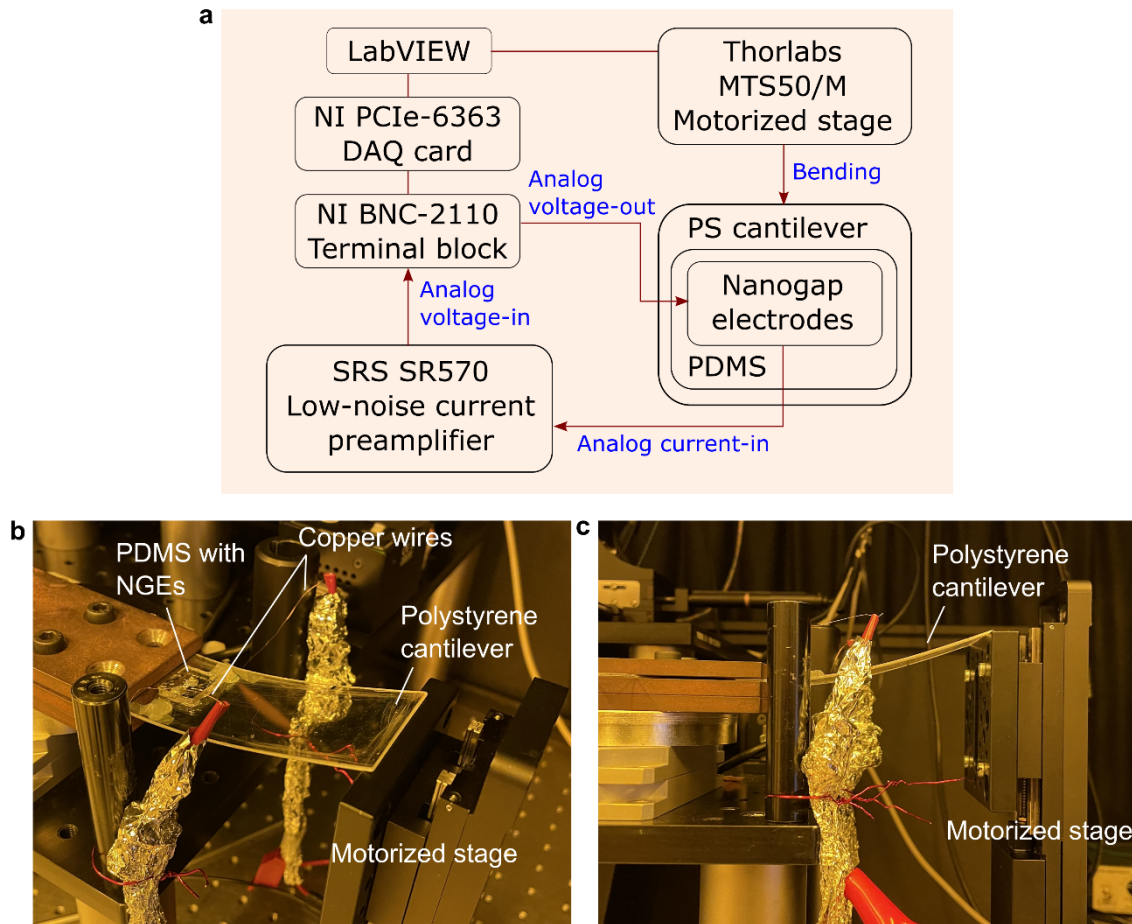
### 2.6.2 Mechanisms to change the nanogap distance

Apart from changing the nanogap distance by applying a mechanical strain to the PDMS substrate, the nanogap distance can also be changed by the current running in the electrodes and the electric field established at the nanogap. As an electric potential difference is created across the electrodes, metal atoms are affected by two forces, the electrostatic force and the force from the exchange of the momentum with electrons which are driven by the potential difference. On one hand, metal ions move along the direction of the electric field due to the electrostatic force and form metallic conducting filaments in the nanogap, which reduce the nanogap distance. This is known as field-induced surface migration.<sup>[40,110–112]</sup> On the other hand, metal atoms also move along the flow of electrons due to the exchange of momentum, which is in the opposite direction of the electric field. This is known as electromigration<sup>[113]</sup> which destructs the conducting filaments formed in the nanogap and thereby enlarges the nanogap distance.

### 2.6.3 Electrical measurement setup

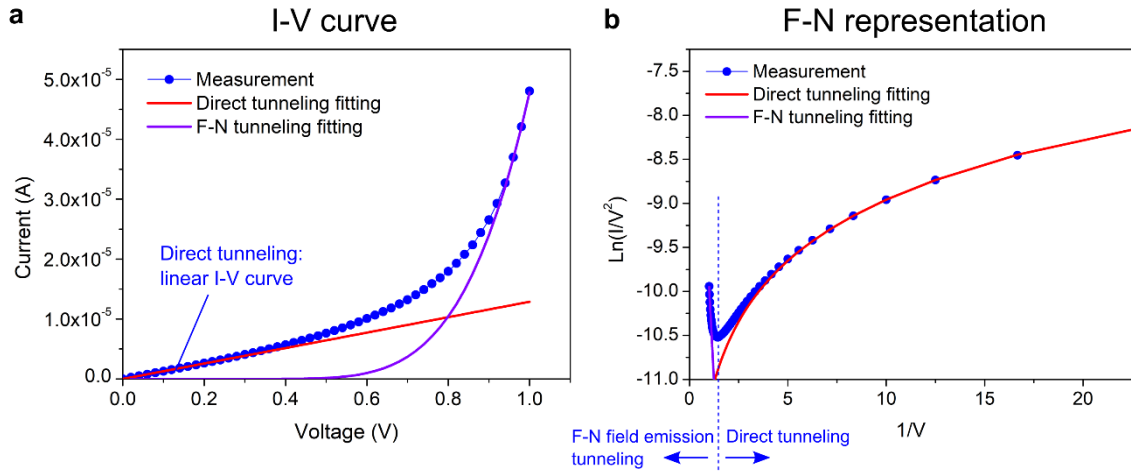
As shown in Figure 2.31a, the electrical measurement setup in this work can be categorized into two parts: mechanical bending and electrical measurement. The entire setup is installed on an optical table with pneumatic vibration isolators (Newport). Starting with the mechanical part, the PS cantilever is clamped and fixed at a stage with a certain elevation (see Figure 2.31b), and a motorized stage (MTS50/M, Thorlabs) is mounted on a XY-axis stage in such a manner that the initial/home position of the motorized stage is adjusted to be almost in contact with the PS cantilever's free end. The MTS50/M motorized stage has a maximal vertical load capacity of  $\sim 40$  N, a minimal moving step of  $1\text{ }\mu\text{m}$ , and a 50 mm maximal travel distance. This enables not only a large range of deformation but also a small increment of the strain applied on the PDMS substrate for an ideal nanogap distance tunability as studied in the previous section. The motorized stage is connected to a personal computer and it is controlled by LabVIEW (National Instruments).

The electrical measurement part comprises a data acquisition (DAQ) card (PCIe-6363, National Instruments) that is installed in the personal computer and a low-noise current preamplifier (SR570, Stanford Research Systems). The DAQ card is also controlled by LabVIEW and sends out an analog voltage signal through a BNC cable terminal block (BNC-2110, National Instruments) to apply a voltage bias on one of the NGE. From the other NGE, the analog current signal is first amplified and converted to an analog voltage signal by the current preamplifier, and then collected by the DAQ card with analog-to-digital signal conversion. In order to reduce the noise from the ground loop, the current preamplifier is powered using the embedded batteries during the measurement. For ease of change of the device under test (DUT), BNC adaptors (T3788, Thorlabs) are used to physically and electrically connect the copper wires that are fixed on the PDMS substrate,



**Figure 2.31.** Electrical measurement setup. (a) Schematic illustration. (b) The isometric view and (c) the side view.

as shown in Figure 2.31b. Copper wires with smaller stiffness are chosen to minimize the mechanical stress applied on the PDMS substrate during the electrical measurement with the cantilever bending. These wires have a diameter of 100  $\mu\text{m}$ .



**Figure 2.32.** Tunneling I-V curve measured from NGEs with ALD  $\text{Al}_2\text{O}_3$  filling in the gap. (a) I-V curve on a double linear scale. A linear correlation between  $I$  and  $V$  shows that the direct tunneling is dominating when the applied voltage is low. (b) The F-N representation of the I-V curve in (a) on a double linear scale. A linear correlation between  $I/V$  and  $\ln(I/V^2)$  shows that the F-N field emission tunneling is dominating when the applied voltage is high. The data is measured from test Au NGEs fabricated by the tape peeling process on a 200 nm thick  $\text{Al}_2\text{O}_3$  layer with the nanogap filled with  $\sim 2.5$  nm thick ALD  $\text{Al}_2\text{O}_3$ . The measured tunneling current ranges from several to dozens of  $\mu\text{A}$  due to the large nanogap width, i.e., the large conducting area. The red and purple lines are the Simmons model fitting of the linear regimes in (a) and (b), representing the direct tunneling and the F-N field emission tunneling, respectively. A tunneling area of  $602 \text{ nm}^2$ , a gap distance of  $0.84 \text{ nm}$ , and an energy barrier height of  $0.819 \text{ eV}$  are extracted from the fitting curves.

#### 2.6.4 Electrical measurement results of NGEs

##### Tunneling current measurement from NGEs on Si substrate

Figure 2.32 shows an example of a tunneling current measured from a test NGEs device fabricated in this work. The test NGEs are fabricated by the tape peeling process on a 200 nm thick  $\text{Al}_2\text{O}_3$  layer with the nanogap filled with  $\sim 2.5$  nm thick ALD  $\text{Al}_2\text{O}_3$  on a silicon substrate. Since the nanogap is filled with the ALD thin film, the gap distance is fixed during the measurement without being changed by the mechanisms mentioned in the previous section. Therefore, a smooth I-V curve without any drastic current jumps or drops is measured as shown in Figure 2.32a. An explicit linear regime is identified in this I-V curve representing the phenomenon of direct tunneling (Eq. 2.1). By plotting the measured I-V data with  $1/V$  as the X-axis and  $\ln(I/V^2)$  as the Y-axis (i.e., F-N representation), a linear regime is identified in a high-voltage range indicating the conduction mechanism of F-N field emission tunneling (see Figure 2.32b and Eq. 2.2).

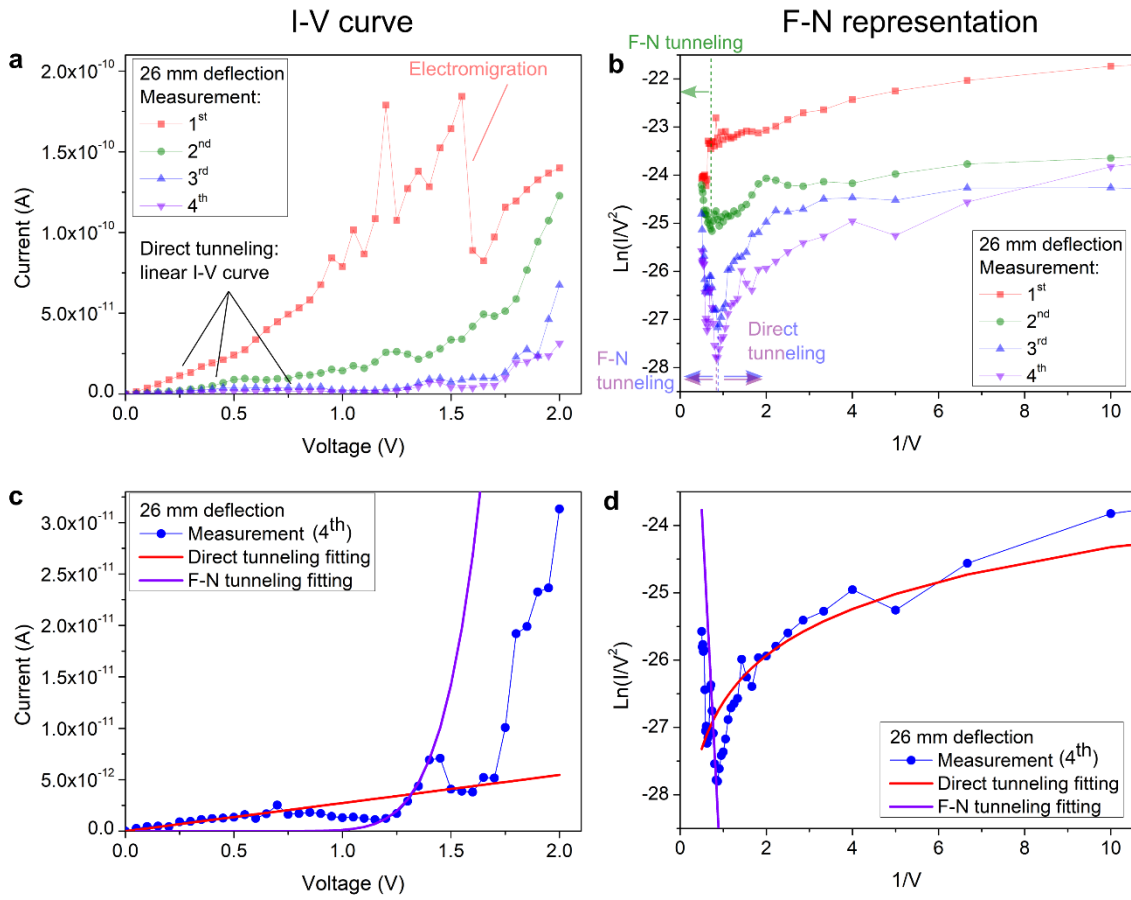
To extract the magnitude of the tunneling area,  $A$ , the gap distance,  $d$ , and the energy barrier height,  $\Phi$  of the NGEs, the Simmons model fitting without considering the image charges are conducted. The red and purple lines in Figure 2.32 are the fitting results of the linear regimes in the I-V curve and the F-N representation, representing the direct tunneling and the F-N field emission tunneling, respectively. As a result,  $A = 602 \text{ nm}^2$ ,  $d = 0.84 \text{ nm}$ , and  $\Phi = 0.819 \text{ eV}$  are extracted from the fitting curves. Compared to the nominal gap distance (i.e.  $\sim 2.5 \text{ nm}$  thick ALD  $\text{Al}_2\text{O}_3$ ) and electrode area ( $\sim 1.5 \text{ }\mu\text{m} \times 50 \text{ nm}$ ), extracted  $d$  and  $A$  are both much smaller than the nominal ones. The result indicates that the thickness of the ALD  $\text{Al}_2\text{O}_3$  film is not uniform on the electrode sidewall, and the tunneling current is mainly contributed by partial areas where the  $\text{Al}_2\text{O}_3$  film is thinnest. The non-uniformity of the ALD film thickness on the electrode sidewall might be due to the grainy surface of the sidewall and the ALD process configuration.

This result confirms that the nanogap defined by the ALD film and the tape peeling process is in the tunneling regime, and the tunneling current can be successfully measured from the NGEs fabricated on the Si substrate. The measured tunneling current ranges from several to dozens of  $\mu\text{A}$  due to the large nanogap width, i.e., the large conducting area.

### **Tunneling current measurements from NGEs on PDMS**

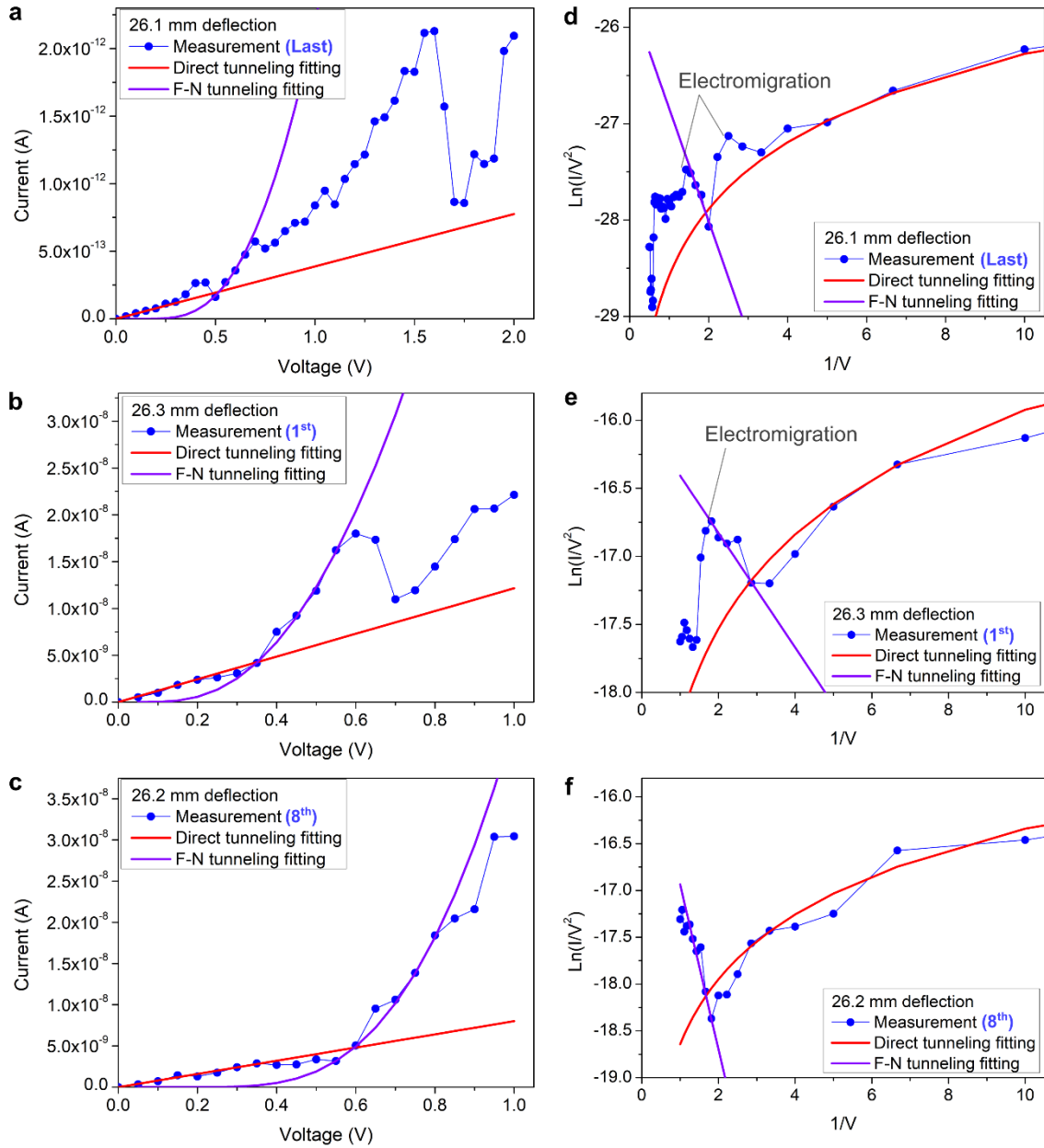
A NGEs device on PDMS mounted on a PS cantilever at the rear position is subjected to electrical measurements. The NGEs device is designed as shown in Figure 2.5 with a nanogap width of about  $700 \text{ nm}$ , and is fabricated by the processes listed in Table 2.1. The PS cantilever is mounted on the electrical measurement setup as shown in Figure 2.31. The current across the NGEs is measured as the PS cantilever is bent upwards to apply compressive mechanical strain to the NGEs on the PDMS substrate.

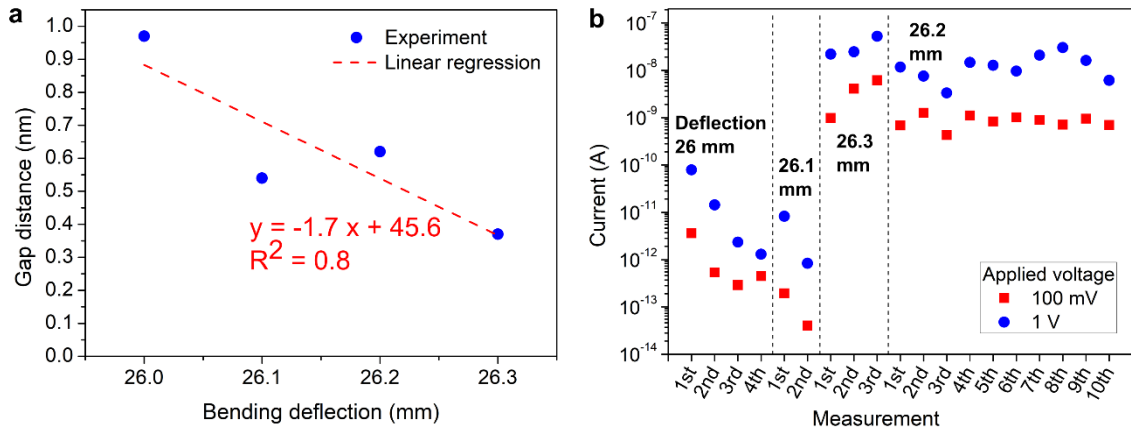
During the measurement, the magnitude of current remains about  $5 \times 10^{-13} \text{ A}$  in the voltage range of  $0$  to  $2 \text{ V}$  as the upward bending deflection increases from  $0 \text{ mm}$  to  $26 \text{ mm}$ . Under the deflection of  $26 \text{ mm}$ , i.e., about  $-2.25\%$  strain applied to the PDMS substrate, tunneling currents are measured as shown in Figure 2.33a, and the corresponding F-N representation curves are shown in Figure 2.33b. Linear regimes in I-V and F-N representation curves are identified which signify the direct tunneling and the F-N field emission tunneling, respectively. Significant current jumps and drops are observed in the I-V curve of the 1<sup>st</sup> measurement (red curve), indicating that the gap distance might be changed by both field-induced surface migration<sup>[112]</sup> and electromigration.<sup>[113]</sup> The drastic current drop at  $1.6 \text{ V}$  implies that the gap is enlarged by electromigration and causes significantly lower currents in the subsequent measurements under the same bending deflection. Figure 2.33c, d show the result of the Simmons model fitting of the last measurement (purple curve) in Figure 2.33a, b, where  $A = 0.008 \text{ nm}^2$ ,  $d = 0.97 \text{ nm}$ , and  $\Phi = 1.48 \text{ eV}$ .



**Figure 2.33.** Electrical measurement results of the mechanically tunable NGEs on PDMS under 26 mm bending deflections of the PS cantilever. (a) I-V curves measured under 26 mm upward bending deflections. Linear regimes at low voltage representing the direct tunneling are identified. (b) Corresponding F-N representations of the I-V curves in (a). Linear regimes at high voltage (i.e. low  $1/V$ ) representing the F-N field emission tunneling are identified. (c) and (d) The result of the Simmons model fitting of the 4<sup>th</sup> measurement in (a) and (b), where  $A = 0.008 \text{ nm}^2$ ,  $d = 0.97 \text{ nm}$ , and  $\Phi = 1.48 \text{ eV}$ .

After measurements under the deflection of 26 mm, the PS cantilever is then bent to 26.1 mm, 26.3 mm, and 26.2 mm sequentially, corresponding to the applied strain of -2.26%, -2.28%, and -2.27%, respectively. Multiple I-V curves are measured under each of the bending deflections and the curves with linear regimes in the F-N representation are selected for the Simmons model fitting. The fitting results are shown in Figure 2.34 and summarized in Table 2.6. Each data point in Figure 2.33 and Figure 2.34 is the average of multiple electrical samplings at a specific sampling rate which are summarized in Table 2.7.





**Figure 2.35.** Summary of the tunneling current measurement of the NGEs on PDMS. (a) Gap distance tunability. The attenuation factor is  $-1.7 \times 10^{-6}$  which is 2 orders of magnitude smaller than the estimation, presumably due to the electrode buckling. (b) Comparison of the magnitude of tunneling current under various bending deflections. A significant increment is observed between the data points of 26.1 mm deflection and those of 26.3 mm deflection, indicating that the nanogap distance is reduced with the increased deflection (i.e. the applied strain). As the deflection is decreased from 26.3 mm to 26.2 mm, a noticeable decrement in tunneling current is also observed, indicating that the nanogap is enlarged with the decreased deflection.

**Table 2.6.** Results of the Simmons model fitting

Deflection (mm)	Strain (%)	$\Phi$ (eV)	$d$ (nm)	$A$ (nm <sup>2</sup> )	Measurement
< 26.0			Noise floor		
26.0	-2.25	1.48	0.97	0.008	Last
26.1	-2.26	0.46	0.54	$2.8 \times 10^{-7}$	Last
26.3	-2.28	0.30	0.37	0.001	First
26.2	-2.27	0.55	0.62	0.016	8 <sup>th</sup>

By plotting the bending deflection versus the extracted gap distances in Table 2.6, the attenuation factor can be calculated as the slope of the linear regression line as shown in Figure 2.35a. The calculated attenuation factor is  $-1.7 \times 10^{-6}$ , which is 2 orders of magnitude smaller than the estimation from Table 2.3, provided that the electrode length is larger than 500  $\mu\text{m}$  (see Figure 2.30). This difference might be due to the Au electrode buckling observed right after the transfer process (see Figure 2.23), which becomes a stress buffer in the Au electrodes and reduces the attenuation factor. Figure 2.35b shows the comparison of the magnitude of tunneling current at 100 mV and 1 V under various

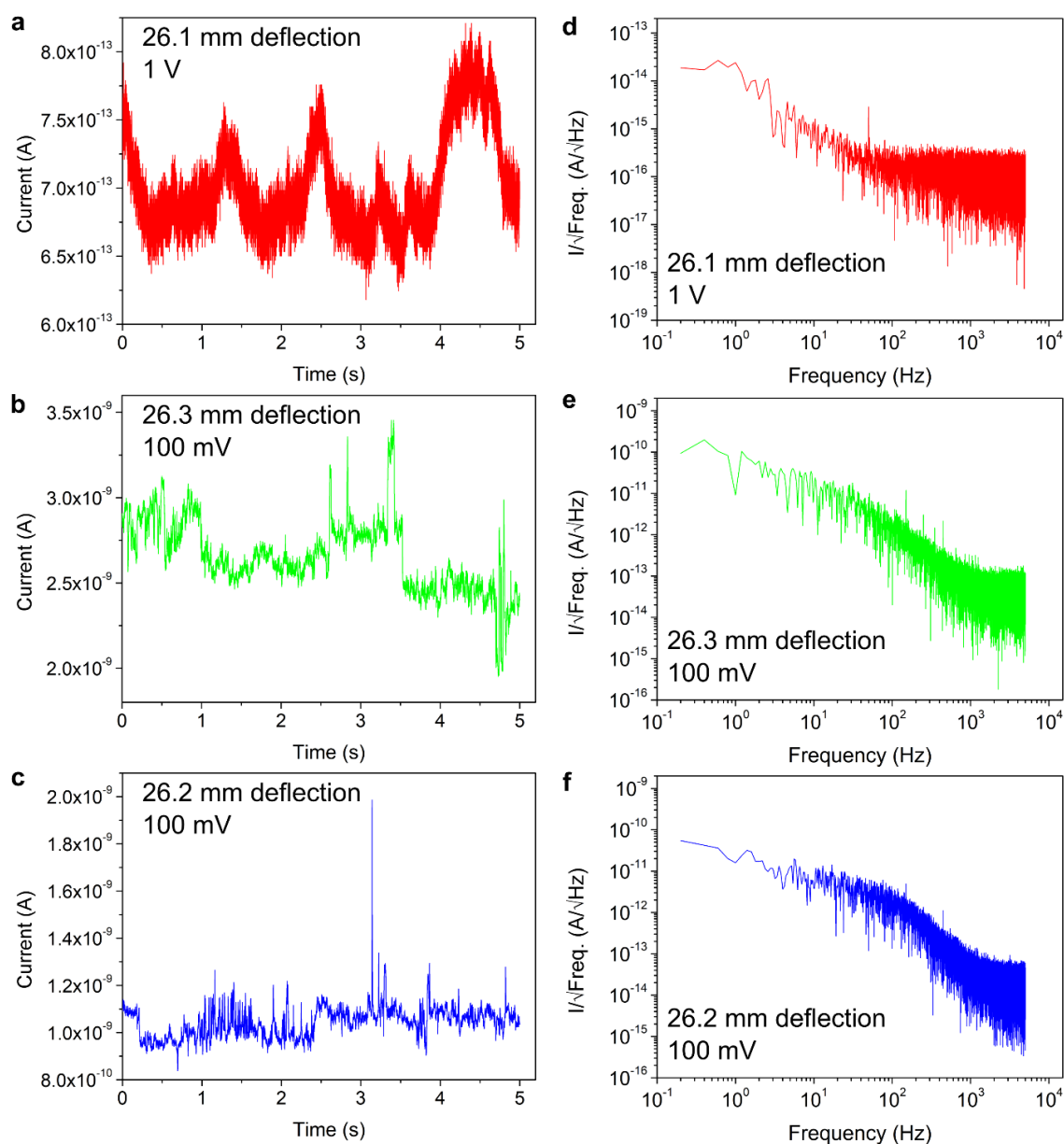


**Table 2.7.** Summary of the sampling rate of the current measurements

Bending deflection (mm)	Measurement	Sampling rate (kHz)	The number of samples averaged	Time duration of voltage application (s)
26.0	All	1	1000	1
26.1	All	1	500	0.5
26.3	All	1	1000	1
26.2	1 <sup>st</sup> and 2 <sup>nd</sup>	1	500	0.5
	3 <sup>rd</sup>	1	10000	10
	4 <sup>th</sup> to 10 <sup>th</sup>	10	1000	0.1

bending deflections. A significant increment is observed between the data points of 26.1 mm deflection and those of 26.3 mm deflection, indicating that the nanogap distance is reduced with the increased deflection (i.e. the applied strain). As the deflection is decreased from 26.3 mm to 26.2 mm, a noticeable decrement in tunneling current is also observed, indicating that the nanogap is enlarged with the decreased deflection. The measurement results shown in Figure 2.35 confirm that the gap distance of the NGEs on PDMS fabricated in this work is mechanically tunable in the tunneling regime.

Apart from the I-V curve measurements, temporal measurements of tunneling current are also conducted after the I-V measurements and then the bending deflection is changed. With a fixed applied voltage, current signals are measured at a sampling rate of 10 kHz for 5 s under 26.1 mm, 26.3 mm, and 26.2 mm bending deflections respectively. The measurement results of current signals in time and frequency domains are shown in Figure 2.36a to c and d to f, respectively. In Figure 2.36a (26.1 mm deflection), multiple current peaks in the range of  $6.5 \times 10^{-13}$  A to  $8 \times 10^{-13}$  A are observed. From the corresponding power spectral density function in Figure 2.36d, only a minor peak at 50 Hz is identified which is assigned to the electrical ground loop. The current fluctuations in Figure 2.36a are from sources with a low frequency which remain unknown in this work. The fluctuations are less likely due to the mechanical instability originating from the weak adhesion between PDMS and the NGEs since such instability should result in a monotonic drift in the signal. On the other hand, in Figure 2.36b (26.3 mm deflection), gradual increases and sudden drops in current are observed which are presumably due to field-induced surface migration<sup>[112]</sup> and electromigration,<sup>[113]</sup> respectively. Compared to Figure 2.36b, gradual increases and sudden drops in current are less obvious in Figure 2.36c (26.2 mm deflection), however, more current spikes without specific frequencies are observed. The reason behind these spikes is still unclear, perhaps they are related to contamination molecules that are possibly left in the nanogap after the wet etching processes.



**Figure 2.36.** Tunneling currents in time and frequency domains under various bending deflections. (a) Under 26.1 mm upward bending and 1 V bias. (b) Under 26.3 mm and (c) 26.2 mm upward bending, the bias is 100 mV. The sampling rates are all 10 kHz. (d) to (f) The power spectral density of currents in (a) to (c), respectively.

### **Au buckling after the mechanical stress application**

After the electrical measurement, more defects of Au buckling at the NGEs are observed. The Au buckling originates from insufficient adhesion between PDMS and the Au NGEs to resist the applied compressive stress during the electrical measurement. The weak PDMS-NGEs adhesion not only allows the enlargement of the initial gap distance after the NGEs transfer process, but also results in an unrepeatability of the gap distance under various bending deflections of the PS cantilever. One major takeaway point from these experiments is that the PDMS-NGEs adhesion is an essential factor to be further improved for a reliable tunability of the gap distance. With a reliable nanogap tunability, it might be eventually possible to generate sharper and refreshed NGEs in this work by re-connecting and re-breaking the electrodes, similar to what is achieved by MCBJ technique.<sup>[77]</sup>

### **How to improve the PDMS-NGEs adhesion**

In order to avoid poor spin coating of ZEP-520 resist on Au surfaces (Figure 2.4e), a 3 nm thick Ti layer is added on top of the Au electrodes. After the RTA process, however, the Ti layer diffuses into the Au layer to form Ti-Au inter-metallic compound.<sup>[114]</sup> The formation of Ti-Au compound might prevent the absorption of MPTMS molecules on the Au surfaces and thereby results in a weaker PDMS-NGEs adhesion. From this point of view, there are 3 possible countermeasures to improve the PDMS-NGEs adhesion:

- (1) Instead of adding a thin Ti layer on top of the Au electrodes, use MPTMS as the adhesion layer between the Au electrodes and ZEP-520 resist.
- (2) Remove the top Ti layer by H<sub>2</sub>O<sub>2</sub> wet etching before the RTA process. There is a risk of NGEs delamination since H<sub>2</sub>O<sub>2</sub> attacks also the bottom Ti layer of the Au1 electrode and the TiW diffusion barrier layer.
- (3) Skip the RTA process. The RTA process is adopted to smooth the NGEs after the tape peeling process (see Figure 2.13b). Since no noticeable Au<sub>2</sub> debris on the sidewall is observed by using the slow Au deposition recipe, the RTA process might be able to be skipped and thereby the diffusion barrier layer can be skipped as well.

## **2.7 Conclusion and outlook**

In this work, we have demonstrated a scalable process to fabricate mechanically tunable tunneling nanogap electrodes on PDMS substrates. The demonstrated process includes adhesion lithography and the use of TiW and Al as the diffusion barrier layer and the sacrificial layer for the wet etching transfer process, respectively. A COMSOL simulation regarding the gap distance tunability is studied. The simulation results show that the gap distance tunability, i.e. the attenuation factor, is configurable by changing the electrode dimensions, and the gap distance can be tuned at the sub-nanometer scale by controlling the PS cantilever bending at the sub-millimeter scale. A study regarding the diffusion

barrier layer is also conducted. A 200 nm thick  $\text{Al}_2\text{O}_3$  layer prevents Au-Al inter-diffusion during the 500 °C, 5 min RTA process, however, the nanogap is significantly enlarged on PDMS after the transfer process due to the residual stress of the thin film stack. The correlation between the Au1 design and the yield of the tape peeling process is systematically studied as well. A combination of a thinner Au2 and a design of Au1 with larger Au1 ring width and a smaller perimeter of the Au2 inside the Au1 ring in general results in a higher yield of the tape peeling process. Finally, the electrical measurement results from the NGEs device on PDMS show that the nanogap distance is mechanically tunable in the tunneling regime. The defects of Au electrodes buckling after mechanically stressing the NGEs indicates that the PDMS-NGEs adhesion is an essential factor to be further improved for a reliable tunability of the gap distance.

To improve the PDMS-NGEs adhesion for a reliable gap distance tunability, 3 possible methods are conceived and discussed. With a reliable nanogap tunability, the NGEs on PDMS fabricated by the process demonstrated in this work might be eventually integrated with micro piezo-electric actuators to become an on-chip, miniaturized mechanically tunable NGEs. The potential to fabricate such a miniaturized device with a scalable method might facilitate the application of a single-molecule detector, or ultimately, next-generation DNA sequencing.



## **Chapter 3    SLR arrays on PDMS fabricated by precise CAPA on reusable templates**

Most materials reported in this chapter have been published as a journal paper entitled “Precise Capillary-Assisted Nanoparticle Assembly in Reusable Templates” on “Particle & Particle Systems Characterization”<sup>[115]</sup>

Author contribution:

- Henry Shao-Chi Yu: topic development, experiment, data collection and analysis, manuscript writing.
- Ana Conde-Rubio: scientific discussion, OM images collection, optical simulation, manuscript revision.
- Hsiang-Chu Wang: scientific discussion, optical spectra measurement, optical simulation
- Olivier J. F. Martin, Giovanni Boero, Jürgen Brugger: advisor, manuscript revision.

### 3.1 Introduction

Nanoparticles have become one of the essential elements in nanotechnology due to their high surface-to-volume ratio, nanoscale size, and accompanying unique physicochemical properties.<sup>[116–118]</sup> Investigations regarding nanoparticles in research areas such as biosensing,<sup>[119]</sup> drug delivery,<sup>[120]</sup> catalysis,<sup>[121]</sup> electronics,<sup>[122]</sup> and plasmonics<sup>[123,124]</sup> have enabled a variety of novel or improved applications. To open up more opportunities in nanotechnology, manipulating swarms of nanoparticles with precise spatial arrangement by bottom-up assembly has been identified as an important process where tailored nanoparticles become the building blocks of ordered systems.<sup>[125,126]</sup> Among nanoparticle surface assembly techniques, capillary-assisted particle assembly (CAPA) with pre-defined topographical templates has shown to be a promising method for the assembly of micro- or nano-scale objects on various surfaces.<sup>[127–129]</sup> For example, by utilizing funnel-shaped topographical assembly traps, deterministic position and orientation of assembled nanorods can be achieved.<sup>[130]</sup> Such trap engineering techniques make CAPA particularly advantageous for applications that rely on the precise positioning of hundreds or thousands of synthesized, highly crystalline nanoparticles,<sup>[131–133]</sup> to be used collectively as an array of nanoantennas<sup>[134,135]</sup> or to exploit plasmonic surface lattice resonances (SLR).<sup>[136–138]</sup> Furthermore, the integration with well-aligned micro- and nano-scale structures fabricated with top-down techniques is enabled by the accurate positioning of the assembled nanoparticles. As a result of this combination of top-down and bottom-up approaches, scalable production of advanced nano-devices such as electrically-driven optical antennas<sup>[51,54]</sup> and tunneling nanogap electrodes<sup>[139,140]</sup> could be achieved. CAPA is a scalable process,<sup>[125,127,141,142]</sup> where a large batch of nanoparticles is assembled in parallel by a single step of a well-controlled capillary process. However, the fabrication of the topographical templates involves time-consuming processes such as electron beam lithography (EBL) or other costly high-resolution photolithography processes. In most cases reported to date, the fabricated template can be used only a single time for the assembly. A strategy to improve the scalability and reduce costs is to reuse the templates. Various ideas to recycle CAPA templates have been reported, such as by transferring gold nanoparticles (AuNPs) from a silicon template onto a polydimethylsiloxane (PDMS) substrate via a dry peeling process,<sup>[143]</sup> or by replicating first the silicon template into PDMS or PMMA, and performing CAPA on the PDMS or PMMA substrate for a subsequent transfer printing process.<sup>[144,145]</sup> By utilizing the dry peeling process, the transfer yield of the assembled 60 nm AuNPs is reported to be 58%, however, the assembly position accuracy is not discussed.<sup>[143]</sup> By utilizing the transfer printing technique, the printing yield is reported to be 98.1%, however, the mean value of the printing accuracy for the 100 nm AuNPs is reported to be 60.8 nm.<sup>[145]</sup> A reusable assembly template that provides high accuracy of particle positioning as well as high particle transfer yield has not been reported yet.

Here, we demonstrate a fabrication process for reusable CAPA templates with funnel-shaped traps, which are designed for precise nanoparticle placement and high assembly

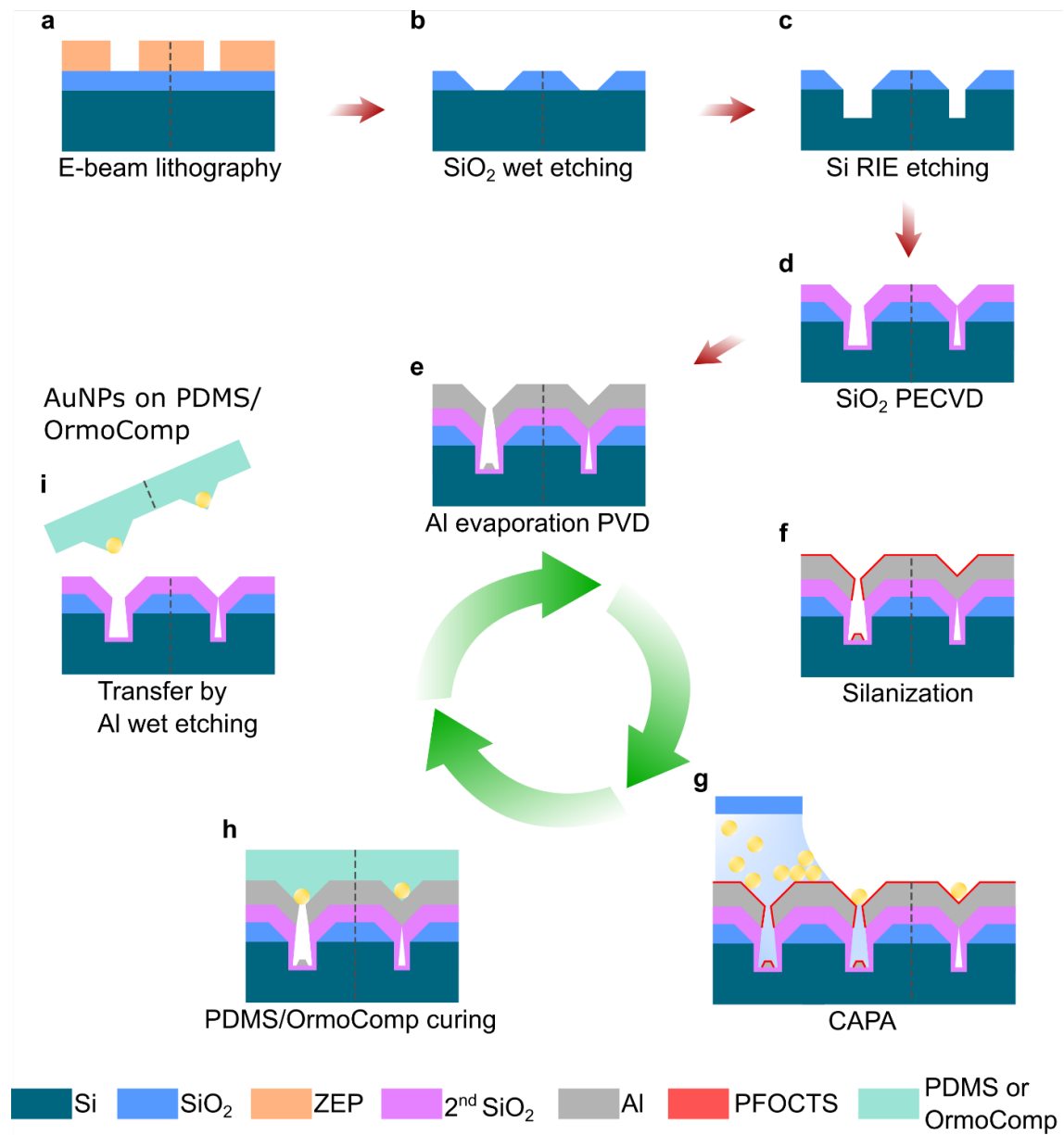
yield. After chip-level CAPA processes with templates diced from the full wafer, the assembled AuNPs are transferred reliably from the reusable silicon assembly templates onto polymer substrates that are either stretchable PDMS (Sylgard 184, Dow Corning) or rigid OrmoComp (micro resist technology GmbH), respectively. The SLR response of the transferred AuNP arrays is also characterized to show the functionality of the AuNP arrays on the PDMS substrate.

## 3.2 Materials and methods

### 3.2.1 Assembly template fabrication

The wafer-level fabrication process of assembly templates is compatible with standard cleanroom processes and is shown in Figure 3.1. A 130 nm thick  $\text{SiO}_2$  thin film is deposited on a silicon wafer (100 mm diameter, P-doped) by plasma-enhanced chemical vapor deposition (PECVD). Vapor hexamethyldisilazane (HMDS) is primed on the  $\text{SiO}_2$  surface before the spin coating of ZEP-520A resist to increase the adhesion at the interface of  $\text{SiO}_2$  and the resist, which determines the funnel sidewall angle. Circular openings with a diameter of about 100 nm in a 150 nm thick ZEP-520A resist are created by means of e-beam exposure and development. The subsequent  $\text{O}_2$  plasma descumming process and buffered hydrofluoric acid (BHF) wet etching create a vertically tapered funnel with sidewall angles of about  $45^\circ$ . After removing ZEP-520A resist by  $\text{O}_2$  plasma ashing, anisotropic reactive ion etching (RIE) with  $\text{SF}_6/\text{C}_4\text{F}_8$  plasma using the patterned  $\text{SiO}_2$  layer as the hard mask is conducted to etch the silicon substrate, thereby creating the bottom part of the funnel as shown in Figure 3.1c. The second  $\text{SiO}_2$  thin film with a thickness of 130 nm is then deposited by PECVD to narrow down the opening of the funnel neck, with a controllable sidewall deposition rate,<sup>[146]</sup> in order to prevent in the subsequent assembly that AuNPs are inserted into the funnel bottom. By reducing the diameter of the circular openings or increasing the thickness of the second  $\text{SiO}_2$ , the cone-shaped traps can be created with the trap neck that is clogged by the second  $\text{SiO}_2$  thin film as shown in Figure 3.1d. A 150 nm thick Al thin film is then deposited by means of e-beam evaporation to serve as a sacrificial layer for the final wet etching transfer process (Figure 3.1e). The as-deposited Al surface becomes hydrophobic by exposure to  $\text{O}_2$  plasma and vapor-phase absorption of trichloro(1H,1H,2H,2H-perfluorooctyl)silane (PFOCTS, Sigma-Aldrich) under vacuum for 1.5 h (Figure 3.1f). The wettability of the Al surface is characterized through static contact angle measurements, obtaining values of about  $110^\circ$  with 3  $\mu\text{l}$  deionized (DI) water droplets at room temperature. Prior to the CAPA process, the wafer is mechanically diced into chips (about  $17 \times 17 \text{ mm}^2$ ). Detailed process parameters are listed in Table 3.1.

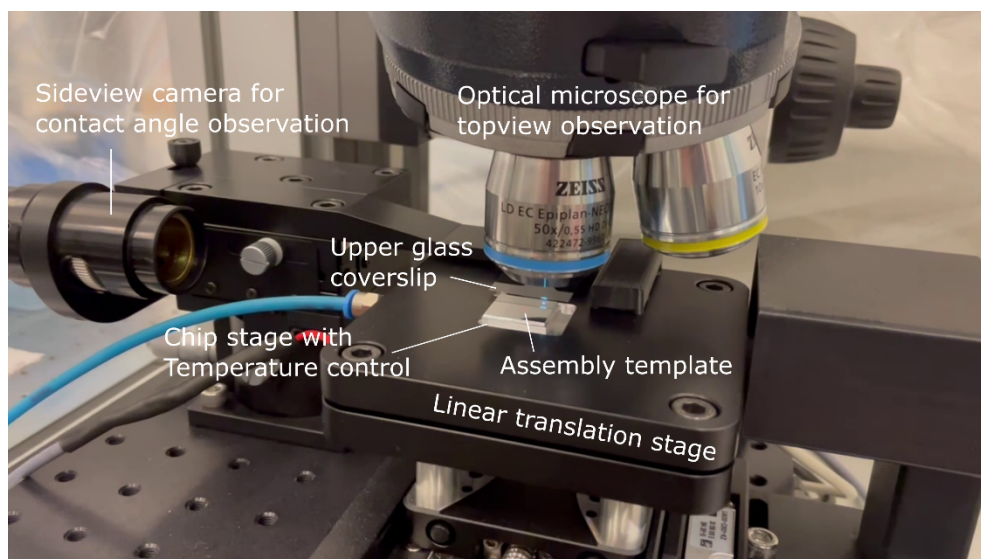




**Figure 3.1.** Scheme of the fabrication process flow of the reusable CAPA template with funnel- (left-half) and cone- (right-half) shaped traps. (a) to (d): One-time-only processes. (e) to (i): Cyclic processes to reuse the assembly template.

**Table 3.1.** Fabrication details of assembly templates

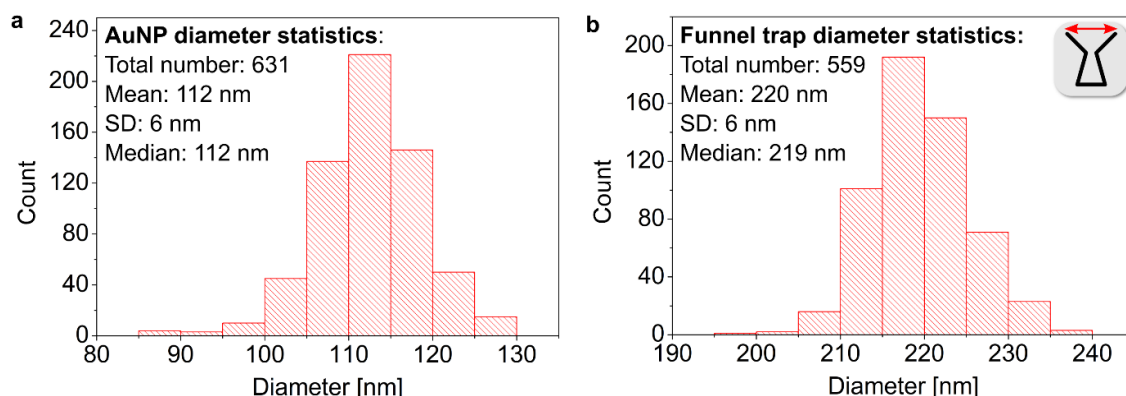
Step	Process	Equipment	Parameters
1	130 nm thick SiO <sub>2</sub> PECVD	Oxford plasmalab system 100	300 °C, RF 20 W, 400 sccm 2% SiH <sub>4</sub> /N <sub>2</sub> , 710 sccm N <sub>2</sub> O, 2 min
2	HMDS priming	ATMsse VB20	135 °C, 160 mbar HMDS, 1 min IPA and DI water rinse, N <sub>2</sub> drying 135 °C baking for 5 min
3	ZEP-520A spin coating	ATMsse OPTIspin SB20	50% in anisole, 500 rpm for 5 s and then 2500 rpm for 1 min
4	E-beam exposure	VISTEC EBP5000+	100 kV, 220 $\mu\text{C cm}^{-2}$
5	Developing	Wet bench	1 min in n-amyl acetate, and 1 min rinsing in methyl isobutyl ketone (MIBK)/IPA (9:1) at room temperature, N <sub>2</sub> drying
6	Descum	Tepla GiGAbatch	200 W, 200 sccm O <sub>2</sub> , 10 s
7	SiO <sub>2</sub> wet etching	Wet bench	7:1 BHF for 22 s, DI water for 5 min, and N <sub>2</sub> drying
8	ZEP-520A removal	TePla GiGAbatch	600 W, 400 sccm O <sub>2</sub> , 3 min
9	Si etching	Alcatel AMS 200 SE	RF 1500 W, DC 30 W, 40/55 sccm of SF <sub>6</sub> /C <sub>4</sub> F <sub>8</sub> for 20 s
10	130 nm thick SiO <sub>2</sub> PECVD	Oxford plasmalab system 100	300 °C, RF 20 W, 400 sccm 2% SiH <sub>4</sub> /N <sub>2</sub> , 710 sccm N <sub>2</sub> O, 2 min
11	150 nm Al e-beam evaporation	Alliance-Concept EVA760	450 mm working distance, 10 <sup>-6</sup> mbar chamber pressure, 5 Å s <sup>-1</sup> deposition rate
12	Al surface activation	TePla 300	1000 W, 500 ml min <sup>-1</sup> O <sub>2</sub> , 10 min
13	Silanization	Vacuum desiccator	PFOCTS under vacuum for 1.5 h IPA and DI water rinse, N <sub>2</sub> drying



**Figure 3.2.** The custom-made setup for capillary-assisted particle assembly (CAPA).

### 3.2.2 Nanoparticle assembly

The procedures for nanoparticle preparation and assembly follow a method that is detailed elsewhere.<sup>[130]</sup> An image of the custom-made setup for CAPA processes is shown in Figure 3.2. Spherical AuNPs with a nominal diameter of 100 nm stabilized with an adsorbed monolayer of CTAB (Nanopartz, USA) are suspended in 0.3 mM CTAB solution (in DI water). 120  $\mu\text{l}$  of AuNP solution is dispensed into a 1.8 mm separation between the template and the upper glass coverslip. The template temperature is typically set to 45 to 48  $^{\circ}\text{C}$  to accelerate the accumulation zone formation and the template is moved by a motorized linear translation stage (PI Micos, PLS-85) at a speed of  $1.2 \mu\text{m s}^{-1}$ . The initial position of the meniscus is set to be 1.5 mm away from the edge of the trap area to have  $\sim 20$  min pre-conditioning time and to achieve stable AuNP accumulation prior to crossing over the trap arrays. Figure 3.3 shows the statistical analysis of the diameter of the AuNPs and the funnel traps, respectively. The AuNPs have a mean diameter of 112 nm and a standard deviation of 6 nm, whereas the funnel traps have a mean diameter of 220 nm and a standard deviation of 6 nm.



**Figure 3.3.** The statistical analysis of the AuNPs and the funnel traps. (a) The diameter histogram of the AuNPs with the nominal diameter of 100 nm, and (b) the diameter histogram of the funnel traps after the Al deposition and the silanization processes.

### 3.2.3 AuNP wet etching transfer and template recycle

After the assembly of the 100 nm AuNPs, as shown in Figure 3.1g, the assembly templates with the AuNPs are treated with O<sub>2</sub> plasma (TePla 300) to remove the exposed CTAB layer covering the AuNPs. The templates with the AuNPs are subsequently immersed in (3-mercaptopropyl) trimethoxysilane solution (MPTMS, Sigma-Aldrich) for 2 h and rinsed with isopropyl alcohol (IPA) to assemble MPTMS on the surfaces of the AuNPs as an adhesive layer.<sup>[37]</sup> The template with the assembled AuNPs is then covered by a liquid polymer that is poured over the surface followed by curing. We study two polymer variations: first, partially cured 10:1 PDMS (~22 g, 80 °C, 7 min pre-baking) is poured, degassed for 1 h, and cured at room temperature for a total time of 48 h in order to avoid thermal stress. Second, UV-curable OrmoComp is poured, degassed for 1 h, and cured at room temperature by exposure to UV radiation (375 nm, 2.5 mW cm<sup>-2</sup>) for 30 s. The thickness of the cured films of PDMS and OrmoComp are about 3 and 1 mm, respectively. The sample is immersed in a diluted hydrochloric acid bath to etch the Al thin sacrificial film for a time ranging from 12 to 72 hours, until the cured PDMS or OrmoComp substrates are separated from the SiO<sub>2</sub> surface together with the assembled AuNPs. After the wet etching transfer process of the AuNPs, the assembly templates are ready to be reused by repeating the cyclic processes as shown in Figure 3.1e to i. Detailed process parameters are listed in Table 3.2.

**Table 3.2.** Fabrication details of AuNPs wet etching transfer

Step	Process	Equipment	Parameters
1	CTAB removal	TePla 300	500 W, 400 ml min <sup>-1</sup> O <sub>2</sub> , 4 min
2	MPTMS priming	Wet bench	2 h in MPTMS solution (60 mM in ethanol) IPA rinse and N <sub>2</sub> drying
3	PDMS preparation		Dow Corning Sylgard 184, Base/curing agent = 20 g/2 g, mixed and degassed 80 °C pre-baking for 7 min Cooled at room temperature for 15 min before pouring on the assembly template
4	PDMS or OrmoComp curing		PDMS: 1 h degassing Cured at room temperature for 48 h OrmoComp: 1 h degassing Cured at room temperature by exposure to UV radiation (375 nm, 2.5 mW cm <sup>-2</sup> ) for 30 s
5	Wet etching transfer	Wet bench	12 to 72 h in diluted hydrochloric acid bath (37% HCl : DI water = 1:6, volume ratio)

### 3.2.4 Assembly yield and position offset analysis

The assembly yield is defined as the ratio of the number of traps filled with a single AuNP versus the total number of traps of the given array, as imaged in the SEM (Zeiss Merlin). Assembly yield images are recorded with a resolution of 21.7 nm per pixel from corners of arrays, containing about 1200 traps in each image. The position offset is defined as the distance between the centroids of an assembled AuNP and the corresponding trap. The coordinates of centroids are extracted from post-processed SEM images by ImageJ software (v1.53e). A total number of 8 SEM images for a position offset analysis are recorded with a resolution of 10.9 nm per pixel and post-processed by Matlab software (R2017b) to correct the unavoidable sample tilting due to manual sample mounting on the SEM stage. SEM images for both assembly yield and position offset analysis are acquired at 3 kV and 400 pA probe current using either InLens or HE-SE2 secondary electron detectors to provide material contrast sufficient to distinguish the AuNPs from the Al surface and trap topography. To evaluate the reusability of the assembly template, two templates are prepared, one with funnel-shaped traps and one with cone-shaped traps.

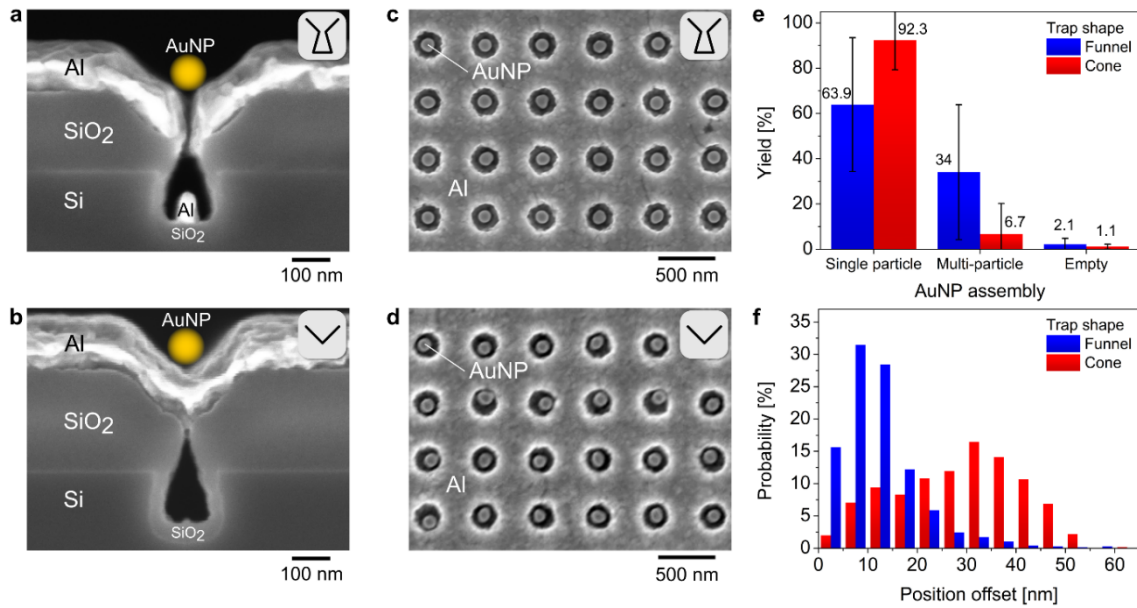
### 3.2.5 Analysis of PDMS / OrmoComp substrates with transferred AuNPs

The topographic study is done by scanning the PDMS and the OrmoComp substrate surfaces with an AFM (Bruker Dimension FastScan, ScanAsyst mode) after the wet etching transfer process. The topographic data are post-processed by Gwyddion software (64 bit v2.49) for the leveling. The SEM (Zeiss Merlin) images of the OrmoComp substrate (with 3 nm Cr coating) are acquired at 10 kV and 400 pA probe current using InLens secondary electron detectors to provide material contrast sufficient to distinguish the AuNPs from the OrmoComp surface. SEM imaging of AuNPs assembled on PDMS didn't result in high-quality micrographs because the energetic electrons which provide material contrast tend to damage the PDMS substrate. Therefore, only OM and AFM images are shown.

## 3.3 Result and discussion

### 3.3.1 AuNP assembly yield and position offset

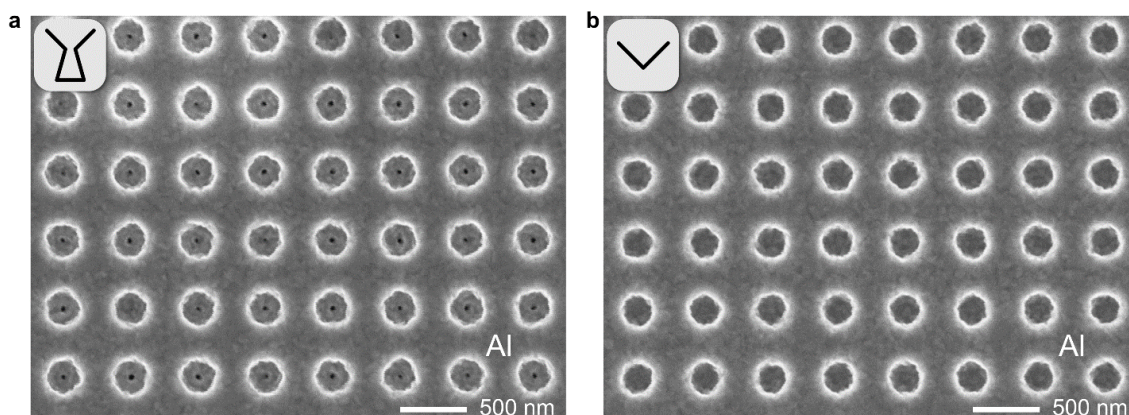
AuNPs with a diameter of 100 nm are assembled in arrays of cone-shaped and funnel-shaped traps with a pitch of 500 nm. To inspect the geometry of the traps, long trenches with analog dimensions to those of the traps are fabricated following the identical process and keeping the equal geometrical parameters. A diamond tip is used to cleave the sample and the cross-section is observed, shown in the scanning electron microscope (SEM) images in Figure 3.4a and b. The neck of the funnel-shaped trap has a width of 20-40 nm as measured by SEM prior to the assembly process (Figure 3.5). After CAPA, Figure 3.4c and 2d show assembled AuNPs in two templates with funnel- and cone-shaped traps, respectively. The assembly yield, presented in Figure 3.4e, is obtained by sampling multiple arrays of 100 by 100 traps (10000 traps) from the SEM images, for both funnel and cone templates. The comparably low percentage of empty traps (2.1% and 1.1%) suggests that the dynamics of particle insertion into the traps and resilience against the receding suspension front during the CAPA process are similar for both, funnel- and cone-shaped traps.<sup>[130]</sup> The difference in multiple particle assembly yields between the funnel and the cone template, as well as the large standard deviation of the multiple particle assembly yield, are presumably due to the variation of the meniscus contact angle during the CAPA process, which is in the range of 40°-55°. In order to study the AuNP positioning accuracy in different trap shapes, a large trap diameter is adopted to allow significant position offsets. The large trap diameter also allows multiple particles to be inserted by higher downward capillary force when the meniscus contact angle becomes smaller as the AuNP accumulation zone grows over time during the CAPA process. This results in the relatively large variations of the multiple particle assembly yields among the studied arrays and templates.



**Figure 3.4.** CAPA assembly results with traps of different shapes. (a) SEM cross-sectional image of long rectangular trenches, serving as the structural references for the investigated circular funnel-shaped traps, and (b) the circular cone-shaped traps (meaningful cross-sections of the circular traps cannot be effectively produced). The yellow dot is a sketch of a 100 nm AuNP, added to the SEM image as a dimensional reference in addition to the scale bar. The long rectangular trenches are fabricated using the identical process as the circular traps. (c) SEM top-view image of an array of 100 nm diameter AuNPs assembled on the Al layer on a funnel template and (d) on a cone template. (e) Assembly yield statistics from multiple arrays of 10000 traps sampled from the funnel and the cone templates, the error bars represent  $\pm 1\sigma$  among arrays (8 arrays for the funnel type and 10 arrays for the cone type). (f) Probability distribution of the position offset of the assembled 100 nm AuNPs. 696 and 553 traps are sampled from the arrays with the highest single-particle yield (94% and 97%) from the funnel and the cone templates, respectively.

For the AuNP position offset analysis, an array from the funnel template with an assembly yield of 94% (approximately 2% are empty and 4% contain more than one AuNP) is selected, and arrays from the cone template with an assembly yield of 97% (approximately 1% are empty and 2% contain more than one AuNP) are selected. In particular, about 700 and 550 traps are sampled from the selected funnel and cone arrays, respectively. As shown in Figure 3.4f, the probability distribution of the position offset for AuNPs that are assembled in funnel traps is significantly different from that for AuNPs that are assembled in cone traps. The funnel template has a median position offset of 10 nm and a standard deviation of 8 nm, whereas the cone template has a median position offset of 30 nm and a standard deviation of 12 nm, respectively.



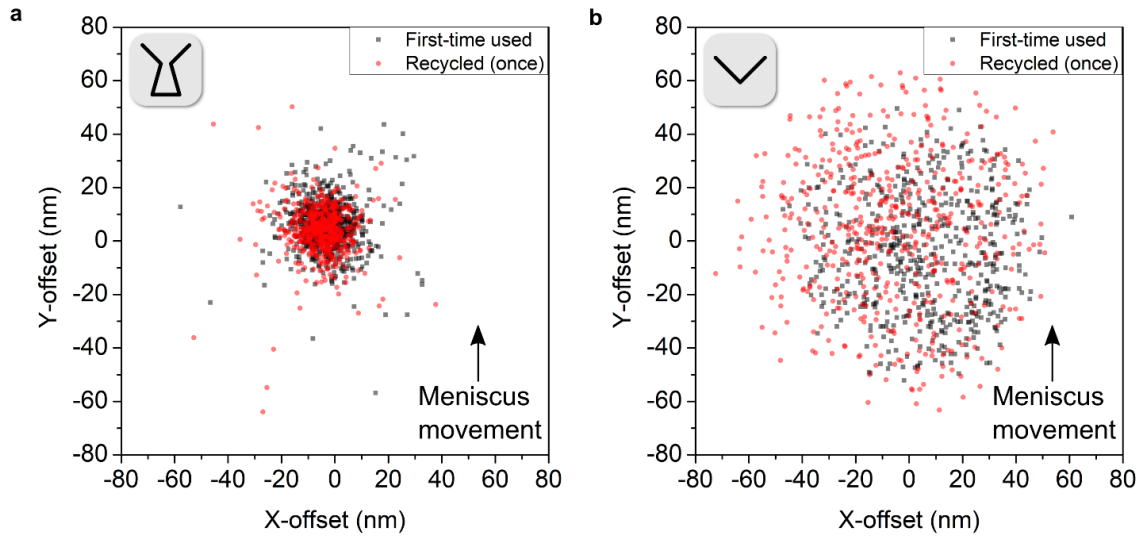


**Figure 3.5.** SEM top-view images of assembly traps before CAPA processes. (a) The funnel-shape traps, and (b) the cone-shape traps. The pitch of traps in both images is 500 nm. Images were acquired at 3 kV and 140 pA probe current using InLens secondary electron detectors.

The final position of particles assembled in topographical traps is predominantly affected by the capillary immersion force, which is present during the solvent drying stage after the meniscus is unpinned from the traps.

In particular, assembled particles are driven by the capillary immersion force towards the edges or corners of the topographical trap provided that the trap bottom is flat.<sup>[141,147]</sup> On the contrary, when using funnel traps, as depicted in Figure 3.1g, the volume below the neck of the funnel serves the purpose to accommodate the solvent (in our case 0.3 mM cetyltrimethylammonium bromide, CTAB), which exerts an attraction force onto the assembled AuNP at the center of the trap during the drying stage, resulting in precise placement of the AuNP. Hence, we attribute the less precise centering of the AuNP in cone traps with respect to the funnel traps to the significantly different shape of the volume occupied by the solvent. The probability distribution of AuNP position offset in the cone traps spans from 0 nm (fixed at the center) to 70 nm (fixed at the edge) and has a peak at about 30 nm. Scatter plots of AuNP position vector are shown in Figure 3.6, and more statistical data are listed in Table 3.3.





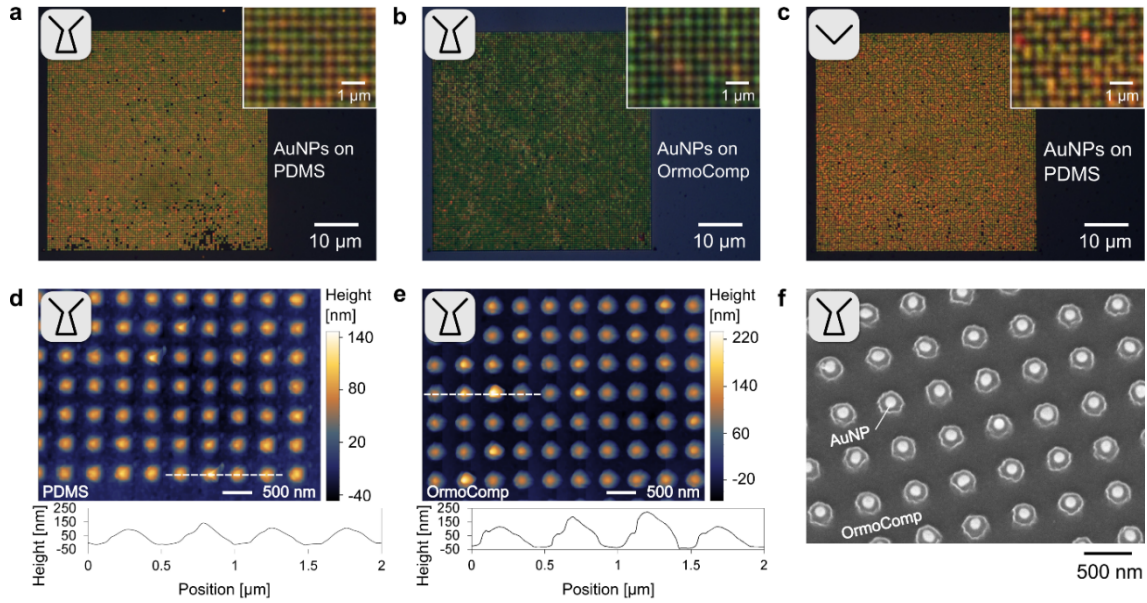
**Figure 3.6.** Scatter plots of the AuNP position offset with respect to the centroid of the trap for (a) the funnel template, 696 and 558 traps are sampled from the first-time used and the recycled funnel template respectively; and for (b) the cone template, 553 and 526 traps are sampled from the first-time used and the recycled cone template respectively. The meniscus movement during the CAPA process is along the Y-direction.

**Table 3.3.** Statistics of AuNP position offset with respect to the centroid of the trap.

Template	Mean [nm]	SD [nm]	Median [nm]	Vector Mean [nm]	X-offset SD [nm]	Y-offset SD [nm]
Funnel, first-time used	12	8	10	(-3, 6)	9	10
Funnel, recycled (once)	12	9	10	(-5, 4)	9	10
Cone, first-time used	29	12	30	(5, -4)	21	22
Cone, recycled (once)	35	16	35	(-6, 4)	25	27

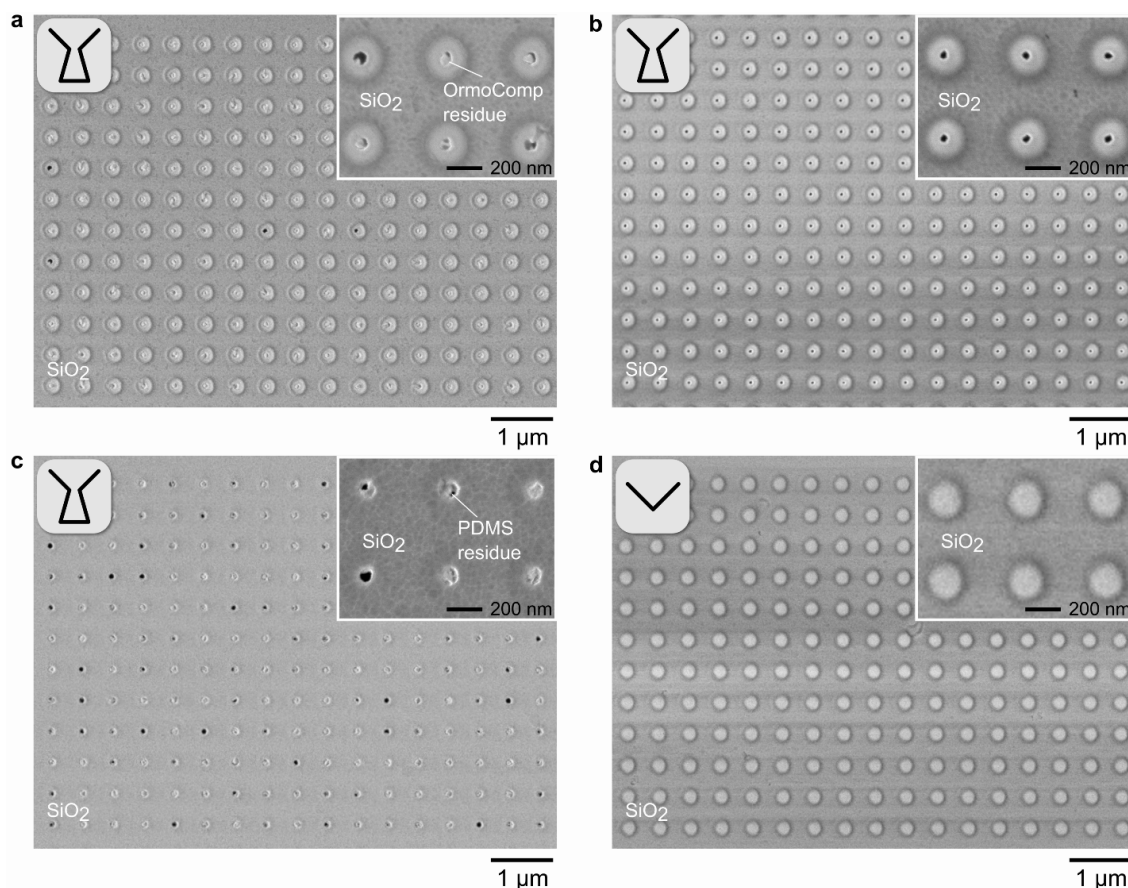
### 3.3.2 AuNP transfer

After SEM imaging of the assembled AuNPs on the CAPA templates for the yield and position offset analysis, the aforementioned funnel and cone templates are subjected to PDMS curing and Al wet etching processes (Figure 3.1h and i) in order to transfer the assembled AuNPs to PDMS substrates. The transfer yield is defined as the ratio of the number of AuNP transferred onto the PDMS substrate versus the number of assembled AuNP in a given array. The transfer yields are both larger than 99% as determined by comparing the SEM images of the assembled AuNPs and the optical microscope (OM, Leica DM800) images acquired under the identical OM configuration from both PDMS substrates (Figure 3.7a and c). Each of the bright dots in the OM images represents single or multiple AuNP in one trap. From the magnified OM images shown as insets, the significant difference in position offset of AuNPs between the funnel (Figure 3.7a) and the cone (Figure 3.7c) templates can be still seen after the wet etching transfer processes. The difference in color among bright dots is mainly due to the variation in the AuNP size, aspect ratio, and the number of AuNP in one trap, which leads to localized surface plasmon resonance (LSPR) peaks at different wavelengths within the visible light range. The high transfer yield is achieved thanks to the use of the Al sacrificial layer,<sup>[37]</sup> which is chemically etched during the wet etching transfer process to release AuNPs from the assembly template. In contrast to the dry peeling transfer process reported previously,<sup>[29,143]</sup> the wet etching transfer process doesn't apply any mechanical normal and shear stress at the interfaces of AuNPs and the PDMS substrate, which allows for more successful transfer of the AuNPs. To highlight the applicability of the method proposed in this work to different substrates, in addition to PDMS substrates, AuNPs assembled on a funnel template are transferred also to an OrmoComp substrate, which is a glass-like, UV-curable rigid and transparent polymer. The transfer yield to OrmoComp is also larger than 99% as shown in Figure 3.7b. The difference in the refractive index of OrmoComp ( $\sim 1.52$ ) and PDMS ( $\sim 1.4$ ) results in the color difference of AuNPs on the OrmoComp (Figure 3.7b) and the PDMS (Figure 3.7a and c) substrates. To further investigate the surfaces of substrates after the wet etching transfer processes, atomic force microscope (AFM) images are taken from the funnel traps on PDMS and OrmoComp substrates as shown in Figure 3.7d and e, respectively. The dimensions of the funnel traps on both assembly templates were designed to be identical. Nevertheless, the maximum peak height and the deviation in peak heights (the negative of funnels) of the OrmoComp substrate are larger than those of the PDMS substrate. This is presumably due to the differences in material preparation and the viscosity of PDMS and OrmoComp. On one hand, OrmoComp is poured on a funnel template and degassed as-purchased with a nominal viscosity of  $(2.0 \pm 0.5)$  Pa·s. During the degassing process, the uncured OrmoComp flows into the bottom part of funnel traps through the neck and the Al sacrificial layer under assembled AuNPs, resulting in large and diversified topographic peak heights.



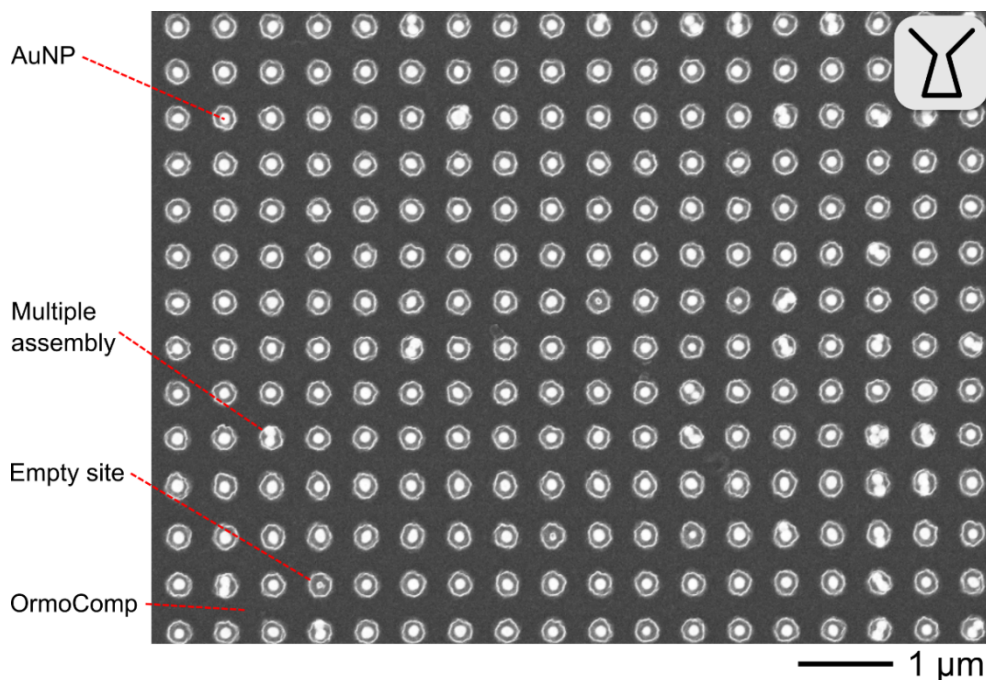
**Figure 3.7.** Results of the wet etching transfer processes of AuNPs on PDMS and OrmoComp substrates. (a) to (c): Bright-field top-view optical microscope images of an AuNP array (100 by 100 with assembly and transfer yield loss) transferred from (a) a funnel template to a PDMS substrate, (b) a funnel template to an OrmoComp substrate, and (c) a cone template to a PDMS substrate. The insets are the corresponding magnified optical microscope images. These optical microscope images are acquired under identical microscope configurations. (d) and (e): AFM images and topographic profiles of the arrays in (a) and (b), respectively. (f) SEM image of the array in (b), with the sample tilted 20° and rotated (with 3 nm Cr coating). The array in (a) and (c) are the arrays studied in Figure 3.4f.

After UV curing and the wet etching transfer process, the cured OrmoComp residues left in funnel traps on the assembly template are observed in SEM images as shown in Figure 3.8a. On the other hand, uncured PDMS is pre-baked at 80 °C for 7 min, which not only partially cures PDMS to increase the viscosity to about 8 Pa·s, but also accelerates the PDMS curing at room temperature.<sup>[148]</sup> This pre-treatment prevents PDMS from flowing through the funnel necks before reaching the gel point, i.e. losing fluidity, without compromising the fidelity of topographic replication and the AuNP transfer yield. As a result, the funnel assembly template subjected to the wet etching transfer process with pre-baked PDMS is residue-free in traps as shown in Figure 3.8b. Since no material contrast is visible in the AFM images (Figure 3.7d and e), SEM images are acquired after the wet etching transfer process as shown in Figure 3.7f and Figure 3.9 to reveal AuNPs embedded in OrmoComp, showing the positions of AuNPs are maintained after the wet etching transfer process.



**Figure 3.8.** SEM top-view images of assembly templates after wet etching transfer processes. (a) A funnel template after non-pretreated OrmoComp transfer. (b) A residue-free funnel template after pre-baked PDMS transfer (80 °C, 7 min.). (c) A funnel template after non-pretreated PDMS transfer. (d) A cone template after non-pretreated PDMS transfer, which is residue-free since the trap necks are clogged by Al thin film. The insets are the corresponding magnified SEM images. The pitch of traps in all images is 500 nm. Images were acquired at 1 kV and 400 pA probe current using InLens secondary electron detectors.

Among the different approaches to recycle CAPA templates,<sup>[137,138,143–145]</sup> assembly areas up to 1 cm<sup>2</sup> on PDMS substrates are reported using the mold replication technique.<sup>[137]</sup> In our work, the dimension of the assembly area in the direction of meniscus moving is currently limited to a few mm in size. However, our process allows to transfer the assembled AuNPs not only onto elastomer substrates such as PDMS ( $E = 1200$  kPa) but also onto rigid substrates such as Ormocomp ( $E = 1$  GPa). The versatility demonstrated here is not straightforward to be achieved in mold replication or dry peeling processes due to the requirement for substrate flexibility. Besides, the use of an Al sacrificial layer is more convenient when a combination of top-down and bottom-up approaches is desired (e.g., adding electrical contacts to assembled particles).

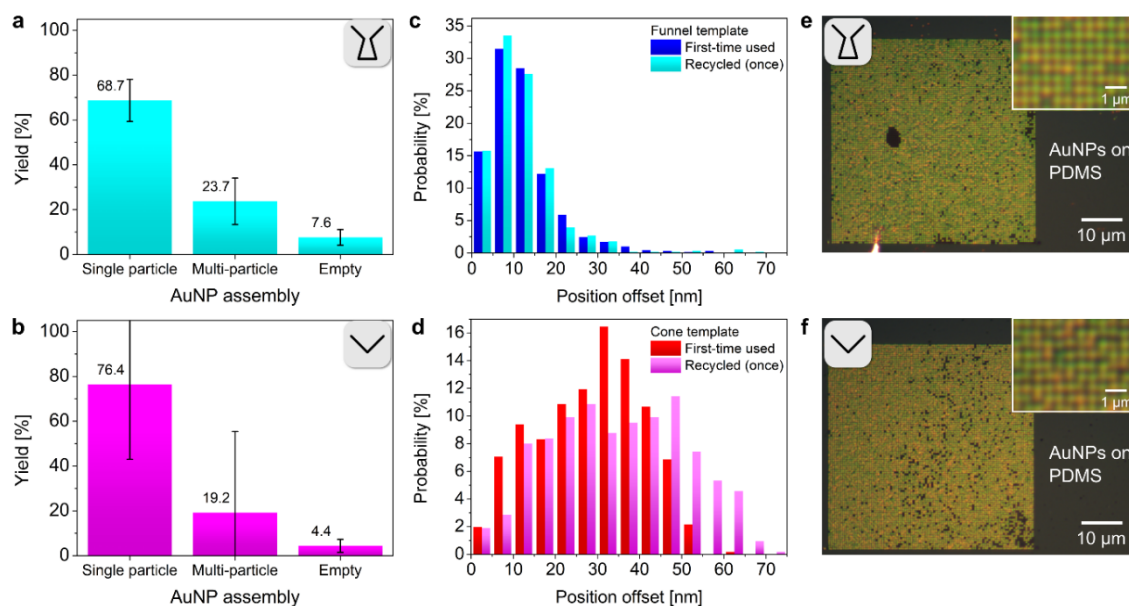


**Figure 3.9.** SEM top-view image of an OrmoComp substrate with AuNPs transferred from a funnel template. The OrmoComp substrate is coated with 3 nm Cr for SEM image recording. The image was acquired at 10 kV and 400 pA probe current using InLens secondary electron detectors in order to probe embedded AuNPs.

### 3.3.3 The reusability of assembly templates

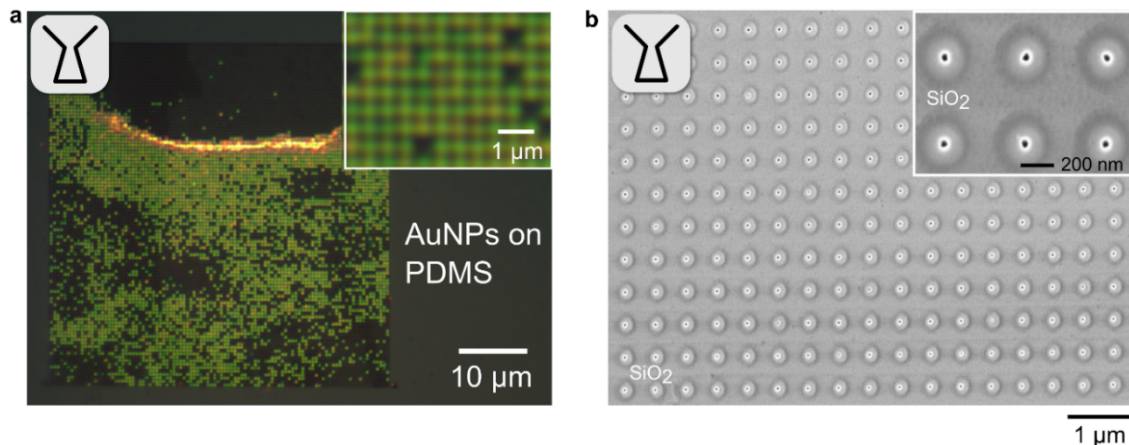
After the transfer of the assembled AuNPs onto PDMS substrates, the funnel template (**Figure 3.4c**) and the cone template (**Figure 3.4d**) are reused for subsequent assembly processes by repeating the processes illustrated in Figure 3.1e to g. The results are shown in Figure 3.10. The average percentage of empty traps with the reused funnel template is 8%, and the standard deviation is 4% (Figure 3.10a), whereas the average percentage of empty traps with the reused cone template is 4%, and the standard deviation is 3% (Figure 3.10b). Both reused templates show low percentages of empty traps but slightly higher than that of the first-time used templates (**Figure 3.4e**). This difference is presumably due to the known CAPA process-to-process variations. The large standard deviations of the multiple particle assembly yields (10% for the funnel template and 36% for the cone template) are due to the reason aforementioned. The probability distributions of AuNP position offset are comparable between first- and second-time used templates as shown in Figure 3.10c and 4d, regardless of the shape of traps. The reused funnel template has a median position offset of 10 nm and a standard deviation of 9 nm, whereas the reused cone template has a median position offset of 35 nm and a standard deviation of 16 nm.





**Figure 3.10.** CAPA assembly template reusability. (a) Assembly yield statistics of multiple arrays of 10000 traps sampled from the reused funnel template and (b) the reused cone template. The error bars represent  $\pm 1\sigma$  among arrays (5 arrays for the funnel type and 4 arrays for the cone type). (c) Comparison of the probability distribution of AuNP position offset. 558 traps are sampled from the same array in Figure 3.4f on the reused funnel template and (d) 526 traps from the same arrays in Figure 3.4f on the reused cone templates. (e) Bright-field top-view optical microscope images of an AuNP array transferred from the reused funnel template to a PDMS substrate, and (f) from the reused cone template to a PDMS substrate. The insets are the corresponding magnified optical microscope images. These optical microscope images are acquired under an identical microscope configuration.

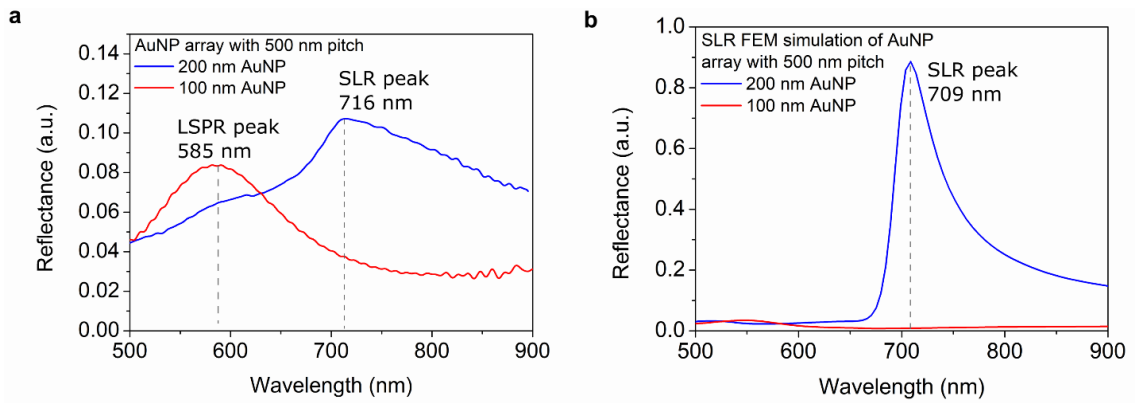
An irregular pinning in the funnel array sampled for Figure 3.10c is observed during the CAPA process and the assembly is not completed for the entire array (see Figure 3.11a). This is probably linked to the micro-scale local inhomogeneity of PFOCTS molecules absorption on the template surface. Therefore, the assembly result from this array is only used for position offset analysis and is not included in the assembly yield statistics of the reused funnel template. The assembled AuNP arrays on the reused templates are also transferred to PDMS substrates by the wet etching transfer process. The OM images of AuNP arrays on PDMS substrates show wet etching transfer yields larger than 99% with both the reused funnel template (Figure 3.10e) and the reused cone template (Figure 3.10f). A SEM image of the reused funnel template after the second-time wet etching transfer process is shown in Figure 3.11b.



**Figure 3.11.** (a) Bright-field top-view optical microscope image (Leica DM800) of an AuNP array transferred from the reused funnel template to a PDMS substrate, the inset is the corresponding magnified optical microscope image. This array is the one selected from the funnel template for position offset analysis (Figure 3.10c). The percentage of empty traps is larger than 50%, which is probably linked to the irregular pinning of the meniscus observed during the CAPA process when the receding contact line of the meniscus is dragged across the array of interest. The micro-scale local inhomogeneity of PFOCTS molecules absorption on the template surface is presumably liable for this irregular pinning. Therefore, the assembly result from this array is only used for position offset analysis and is not included in the assembly yield statistics of the reused funnel template. (b) SEM top-view image of the array in (a) on the reused funnel template after the second-time wet etching transfer process with pre-baked PDMS (80 °C, 7 min.).

### 3.3.4 Optical measurement of the SLR arrays on PDMS

After transferring 100 nm AuNP arrays to PDMS substrates, an optical reflectance spectrum under normal incidence is measured (see Figure 3.12a red curve) with the measurement setup as shown in Figure 3.13. The spectrum shows a peak at 585 nm, which is assigned to the LSPR. In this array, the SLR mode is not visible. This result agrees well with the SLR simulation using the finite element method (FEM, COMSOL) with a normal incidence as shown in Figure 3.12b, where a weak SLR response at ~ 550 nm is identified for the 100 nm AuNP array with 500 nm pitch. In order to enhance the SLR mode, an array of 200 nm AuNP with 500 nm pitch is assembled and transferred to a PDMS substrate using the same processes reported in this work. From the SLR FEM simulation result in Figure 3.12b (blue curve), a peak appears at 709 nm for 200 nm AuNP array with 500 nm pitch, attributed to the SLR mode. The corresponding measured reflectance spectrum (Figure 3.12a) shows an agreement with the FEM calculation, where an asymmetric peak of SLR mode at 716 nm is identified.

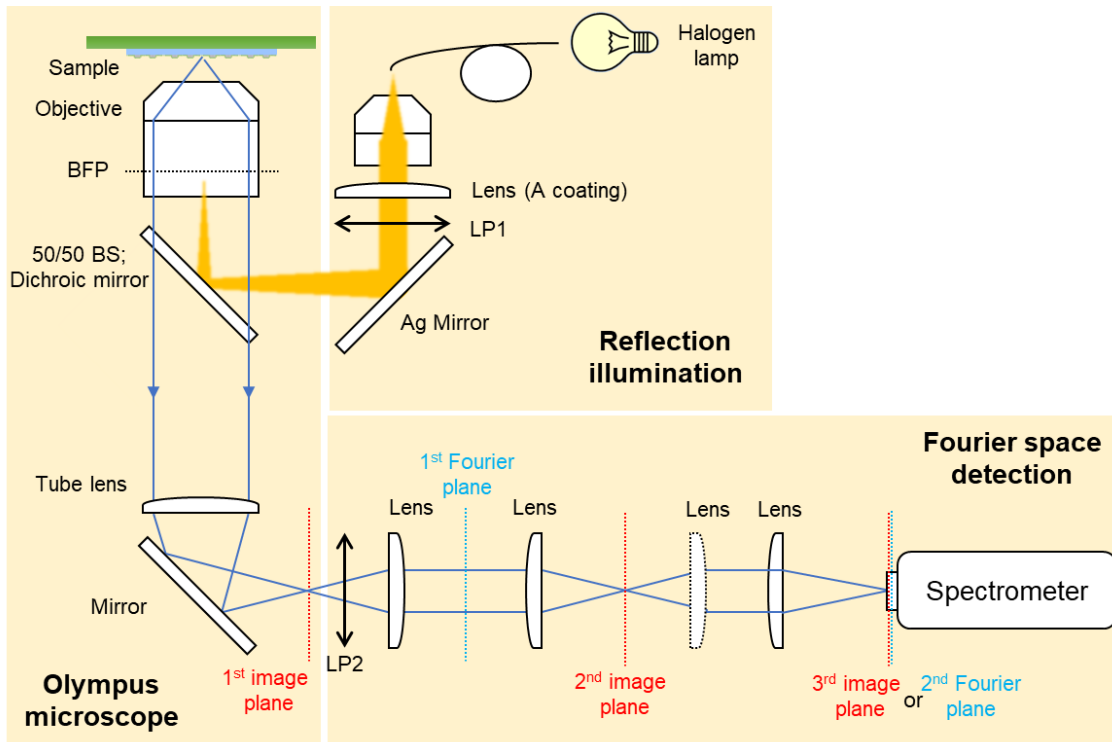


**Figure 3.12.** Optical spectra of AuNP arrays. (a) The reflectance spectra of 100 and 200 nm AuNP arrays with 500 nm pitches on PDMS substrates at normal angle of incidence. (b) The corresponding SLR simulation results using the finite element method (COMSOL).

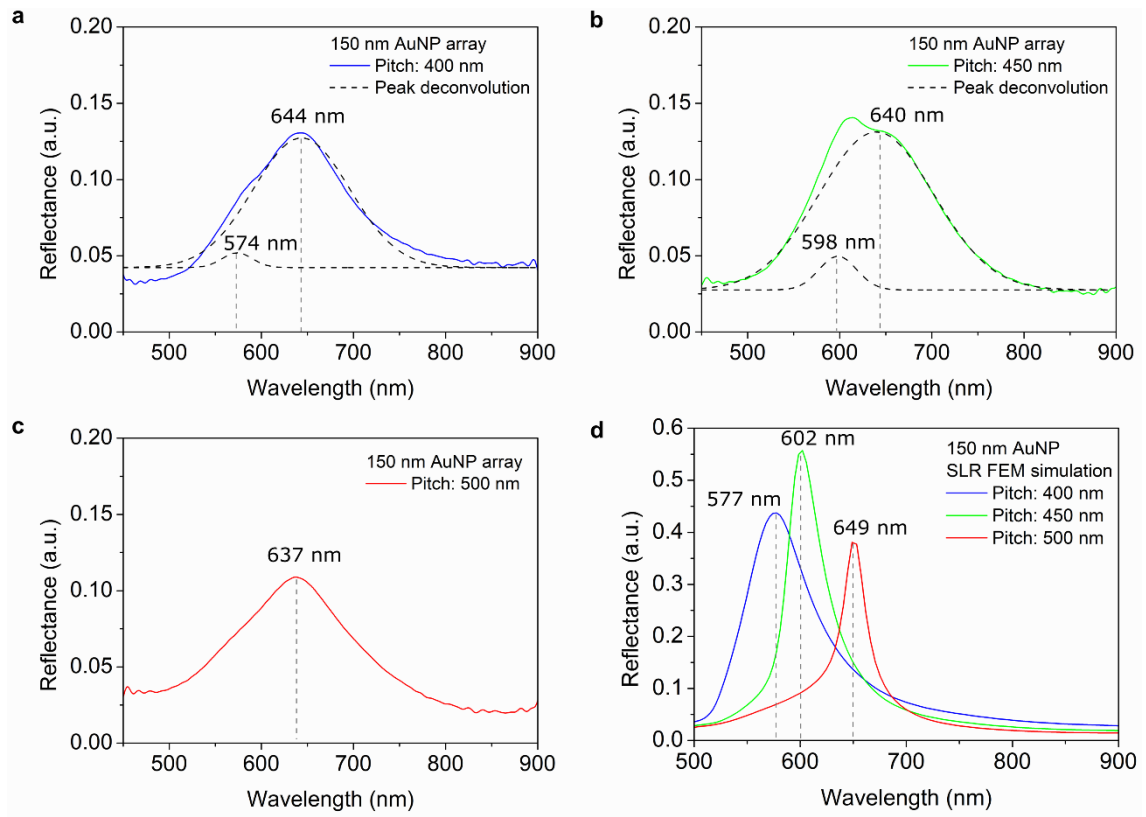
The SLR peak in the measured spectrum is broad as a consequence of the high numerical aperture of the set-up which is 0.9.<sup>[149]</sup> We also conducted SLR simulations of excitations with various incidence angles, resulting in peaks shifted from that of the normal incidence, which confirms this point. The asymmetry of the SLR peak is mainly due to the asymmetric environment, i.e. air, MPTMS, and PDMS, with a contrast of the refractive index that the AuNP array is interacting with.<sup>[150]</sup>

To demonstrate the pitch-related SLR peak shift, arrays of 150 nm AuNP with the pitch of 400 nm, 450 nm, and 500 nm are also assembled and transferred to PDMS substrates for optical characterization. The characterization results are shown in Figure 3.14. The peaks assigned to the LSPR at about 640 nm are identified in all arrays. In Figure 3.14a and FFb, the peaks assigned to the SLR at 574 nm and 598 nm are identified in the spectra of 400 nm and 450 nm pitch, respectively. The COMSOL simulation result in Figure 3.14d shows the pitch-related SLR peak shift, which agrees with the measurement results. The SLR peak and the LSPR peak are overlapping for the array of 500 nm pitch, hence only one peak is measured in Figure 3.14c.





**Figure 3.13.** Schematic diagram of the optical measurement setup in a reflection configuration. The system can be divided into 3 major parts: illumination, microscope, and detection. (Courtesy of Mr. Hsiang-Chu Wang from NAM, EPFL)



**Figure 3.14.** Optical spectra of 150 nm AuNP arrays with various pitches. (a) to (c) The reflectance spectra of 150 nm AuNP arrays with 400 to 500 nm pitches on PDMS substrates at normal angle of incidence. (d) The corresponding SLR simulation results using the finite element method (COMSOL).

### 3.4 Conclusion and outlook

In this work, we demonstrate a process to fabricate reusable templates for precise nanoparticle placement with the CAPA technique and show a systematic yield study of the assembly and transfer step. The assembly yield with arrays of approximately 10000 funnel traps is as high as 94% with a median particle position offset in the order of 10 nm. Cone traps achieve a similar maximum assembly yield of 97% but have a larger median position offset of 30 nm. The assembled AuNPs are then transferred from the assembly template onto PDMS and OrmoComp substrates with transfer yields larger than 99%. The SLR responses of the transferred AuNP arrays are characterized and the measurement results are in agreement with the FEM simulation results. To enable the reusability of the template, a pre-treatment of uncured PDMS is a prerequisite to ensure a residue-free assembly template after the wet etching transfer process. The result of the yield and position offset of AuNPs assembled using the recycled template is comparable

to that of the first use, demonstrating that the proposed process allows for the fabrication of reusable templates.

The process presented here also paves the way for the precise positioning of thousands of bottom-up assembled nanoparticles with precise alignment to top-down fabricated micro- or nano-structures, and therefore enables integrated nanosystems made of lithography-defined patterns and template assembly. The presented process allows in particular the scalable fabrication of advanced nano-devices such as electrically-driven optical antennas and tunable tunneling nanogap electrodes and might ultimately facilitate applications in nano-light sources and single-molecule detection, which remain a challenge for the present cutting-edge transfer printing and dry peeling transfer techniques.

# Chapter 4   NGEs on PDMS fabricated by CAPA

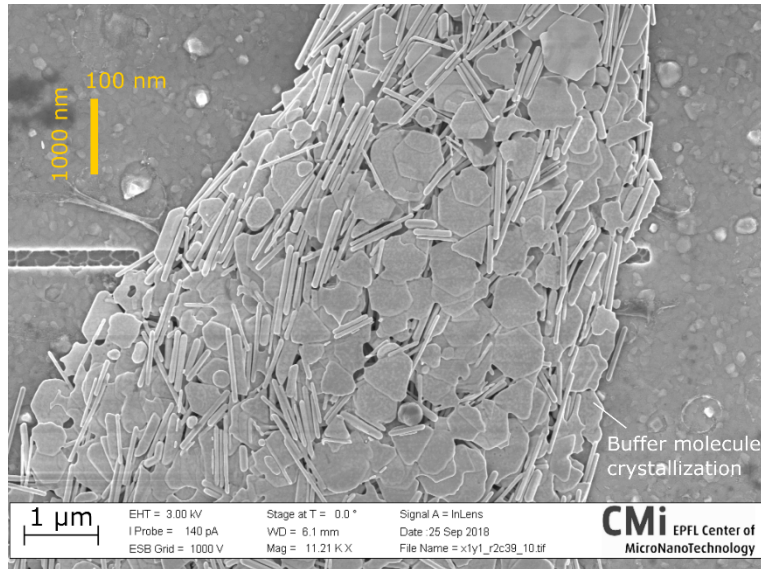
Part of the materials reported in this chapter has been published as a proceeding paper entitled “Harnessing Poisson Effect to Realize Tunable Tunneling Nanogap Electrodes on PDMS Substrates for Strain Sensing” on “IEEE Xplore”<sup>[140]</sup>

Author contribution:

- Henry Shao-Chi Yu: topic development, experiment, data collection and analysis, manuscript writing.
- Giovanni Boero, Jürgen Brugger: advisor, manuscript revision.

## 4.1 Introduction

Apart from using the CAPA technique to fabricate AuNP SLR arrays as reported in the previous chapter, the CAPA technique is also utilized to fabricate NGEs. By assembling a dimer of Au nanomaterials in one assembly trap, a nanogap in between the dimer is formed simultaneously. With the following electrode formation process to extend two electrodes from each end of the dimer, a NGEs device is created. It is challenging to fabricate the electrodes in a scalable manner since the exact position of nanomaterial in each trap is uncertain and the size of the nanomaterial is only at the nanoscale. In this chapter, we report the feasibility study of the scalable NGEs fabrication by CAPA with high aspect ratio Au nanorods (AuNRs) and spherical AuNPs, respectively.



**Figure 4.1.** Top-view SEM image of the nominally 100 nm x 100 nm x 1000 nm Au nanorods. A drawing of 100 nm x 1000 nm yellow rectangle in the image is for dimensional reference, showing that the size of the Au nanorod is quite dispersive. The length of most rods is smaller than 1000 nm.

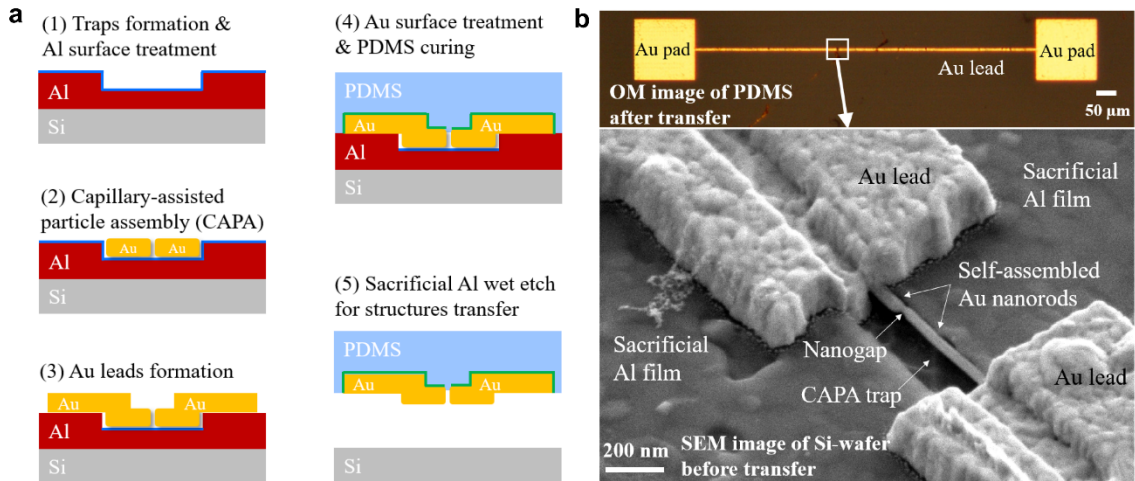
## 4.2 NGEs fabricated by CAPA with Au nanorod

### 4.2.1 High aspect ratio AuNR

As the first attempt, a high aspect ratio Au nanorod (AuNRs) with the nominal dimensions of 100 nm x 100 nm x 1000 nm (Nanopartz, AR=10) is selected. A larger rod length gives a larger tolerance in both overlay shift and resolution for the electrode formation process, and a smaller rod diameter gives a tip-like gap width. As shown in Figure 4.1, the size of AuNR is quite dispersive and the length of most rods is smaller than 1000 nm.

### 4.2.2 NGEs fabrication

Figure 4.2a shows the fabrication process of NGEs, the non-reusable cuboid-shaped assembly traps with dimensions  $L/W/D = 2600 \text{ nm}/200 \text{ nm}/100 \text{ nm}$  are fabricated directly in the 300 nm thick sacrificial Al layer by EBL and RIE. After the CAPA process, a lift-off process of EBL followed by the 150 nm thick Au deposition defines the Au electrodes and pads connecting to the assembled Au nanorod dimer. Finally, the assembled dimer along with the electrodes are transferred onto a PDMS substrate by the wet etching transfer process.



**Figure 4.2.** NGEs fabricated by CAPA with Au nanorods. (a) NGEs fabrication process, the trap is cuboid-shaped and is not reusable. (b) The OM image (top) shows the device after transfer to the PDMS substrate, the SEM image (bottom) shows the NGEs on the Si substrate before the wet etching transfer process. (Scale bars: 50  $\mu\text{m}$  and 200 nm respectively).

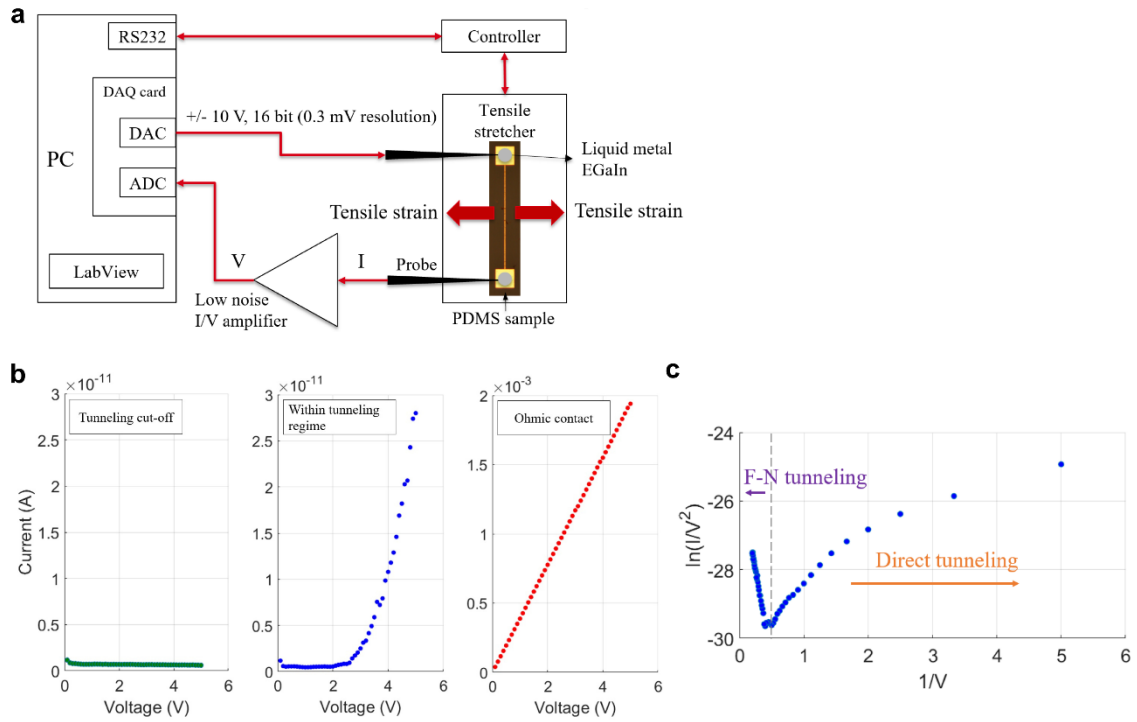
The yield of the CAPA process with a AuNR dimer forming a nanogap is lower than 1%. The traps of failure are either empty, single rod assembly, two rods assembly with a large separation, or multiple rods assembly. Figure 4.2b depicts the result of the NGEs fabrication. The top of the figure shows the OM image of the PDMS sample at the end of the fabrication process. Both, the Au electrodes and pads are successfully transferred from the Si substrate to the PDMS substrate. Au pads and electrodes as small as 1  $\mu\text{m}$  remain intact due to the minimized mechanical stress during the wet etching transfer process. Since it is challenging to image the PDMS sample in a SEM with high resolution, the SEM image of the nanogap is taken on the Si substrate prior to the transfer process. As shown at the bottom in Figure 4.2b, the diameters of the AuNRs are about 50 nm, which are smaller than the nominal diameter of 100 nm. The actual dimension of the nanogap cannot be measured accurately because of the resolution limitation of the SEM. Each Au electrodes comprises of two rectangles: 1 x 1  $\mu\text{m}^2$  contacting the nanorod and 5 x 600 (left) / 860 (right)  $\mu\text{m}^2$  in connection with the pad. The Au electrodes have a thickness of 150 nm.

#### 4.2.3 Electrical measurement

After the observation under OM, the PDMS sample with the NGEs is mechanically clamped in a stretcher (TST350, Linkam Scientific Ltd.) with the electrodes being orthogonal to the stretching direction. The gap distance in between the AuNR dimer can

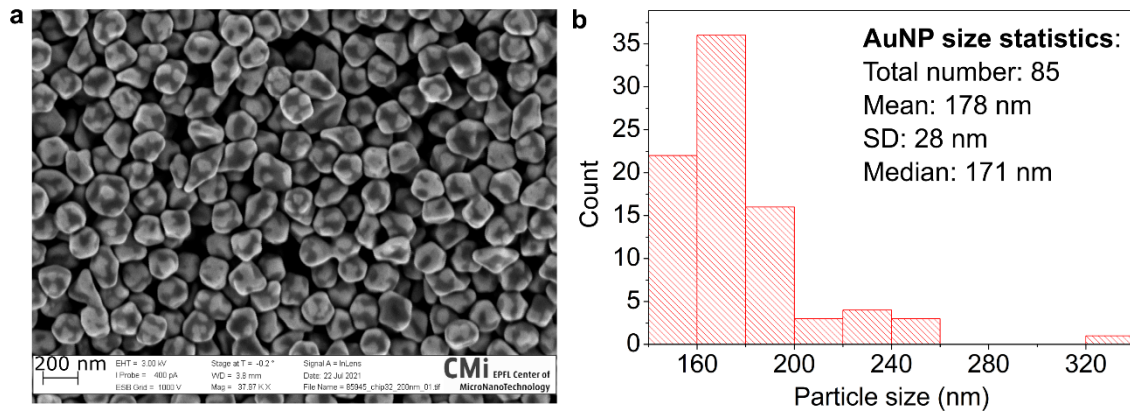
be reduced by the tensile strain applied by the stretcher due to the Poisson effect. Eutectic Ga/In liquid metal (Sigma-Aldrich) is added on the Au pads to ensure a reliable contact between the probing needles and the Au pads during measurements. One of the probing needles is connected to a DAQ card (PCIe-6363, National Instruments), whereas the other probing needle is connected to a low noise I/V amplifier (SR570, Stanford Research Systems), which converts current signals into voltage signals. The output and input voltage signals are applied and detected by the DAQ card, which is controlled by a program written in LabView (National Instruments). The schematic measurement setup is shown in Figure 4.3a.

With such long electrodes as shown in Figure 4.2b, the nanogap is expected to be in the tunneling regime under the applied strain smaller than 0.01%. During the measurement, however, the tunneling current is not detected until the applied strain is 2% to 5%. This could be explained by the strain control at the initial status. As the PDMS slab is fixed in the stretcher, a tensile strain larger than 0.01% could be already applied to the PDMS. Figure 4.3b shows three I-V curves under different strain levels. At initial status, the nanogap is larger than the tunneling cut-off distance and only a leakage current of less than 1 pA is measured. Increasing the strain to 2% to 5%, the nanogap between Au nanorods is narrowed down and the tunneling current is measured. This is confirmed by the Fowler-Nordheim representation of the same I-V data as shown in Figure 4.3c. As the applied strain further increases, a linear I-V curve with a current of several mA is measured, indicating the Au nanorods are in Ohmic contact. The measured resistance is about 2.6 kOhm, which is the resistance originating from the low noise amplifier. This measurement result indicates that the NGEs fabricated by CAPA with AuNRs can be tuned between states of open, tunneling, and ohmic contact.



**Figure 4.3.** Electrical measurement results of the AuNR NGEs. (a) The measurement setup. The PDMS sample with the NGEs is mechanically clamped in a stretcher (TST350, Linkam Scientific Ltd.). Eutectic Ga/In liquid metal (Sigma-Aldrich) is added on the Au pads to ensure a reliable contact between the probing needles and the Au pads during measurements. (b) I-V curves of the NGEs measured under different applied static tensile strain. (c) The Fowler-Nordheim representation of the blue curve in (b).





**Figure 4.4.** 200 nm AuNPs for the NGEs fabricated by CAPA. (a) Top-view SEM image of a cluster of nominally 200 nm AuNPs. Most AuNPs are not spherical but rather polyhedral. (b) Histogram of the particle size estimated from (a), the particle size is on average smaller than 200 nm.

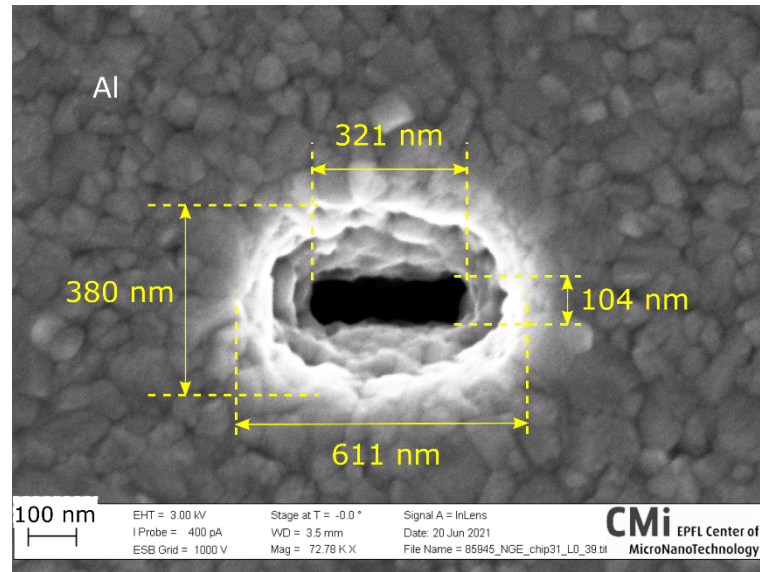
### 4.3 NGEs fabricated by CAPA with AuNP in funnel traps

#### 200 nm AuNP for the dimer assembly

Since the yield of the CAPA process with a AuNR dimer of high AR forming a nanogap is extremely low, an attempt of fabricating NGEs using CAPA with AuNPs is conducted to expect a higher dimer yield. Considering the acceptable tolerance for the electrode formation process, 200 nm AuNP (Nanopartz, USA) is selected for the dimer assembly as shown in Figure 4.4. Most AuNPs are not spherical but rather polyhedral. The particle size, i.e. the largest diameter, has a mean value of 178 nm and a standard deviation of 28 nm.

#### Funnel trap for 200 nm AuNP dimer

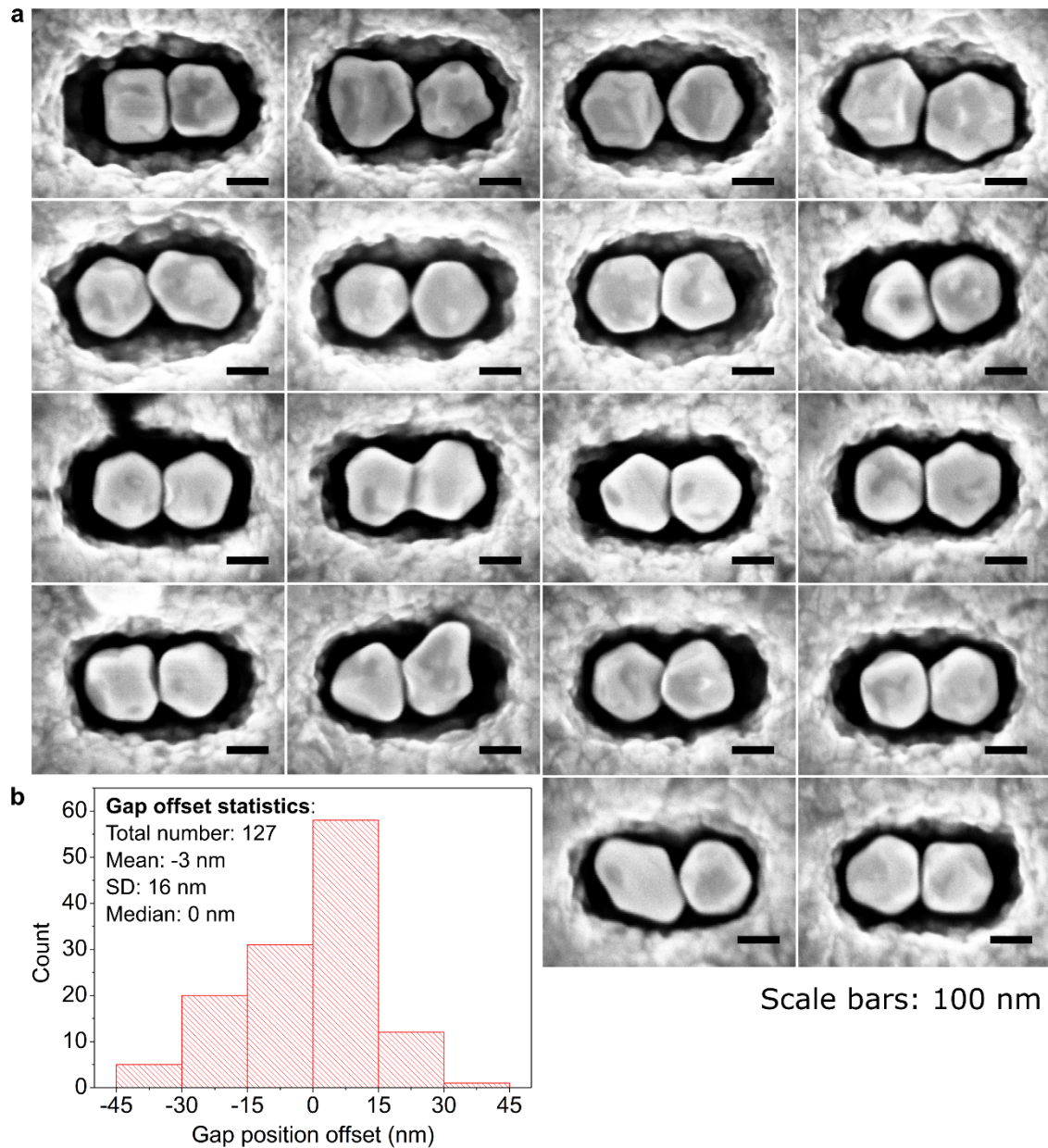
To exploit the precise particle placement of the funnel-shaped traps demonstrated in Chapter 3, anisotropic funnel traps designed for a dimer of 200 nm AuNPs are fabricated using the process as shown in Figure 3.1 and Table 3.1 with adjustments in parameters (see Table 4.1). As shown in Figure 4.5, the dimensions at the top of the funnel after the sacrificial Al deposition are about 580-610 nm by 380-400 nm for the high assembly yield of the 200 nm AuNP dimer. The dimensions of the funnel neck are about 300-340 nm by 80-120 nm to prevent the assembled 200 nm AuNPs from entering the bottom of the trap.



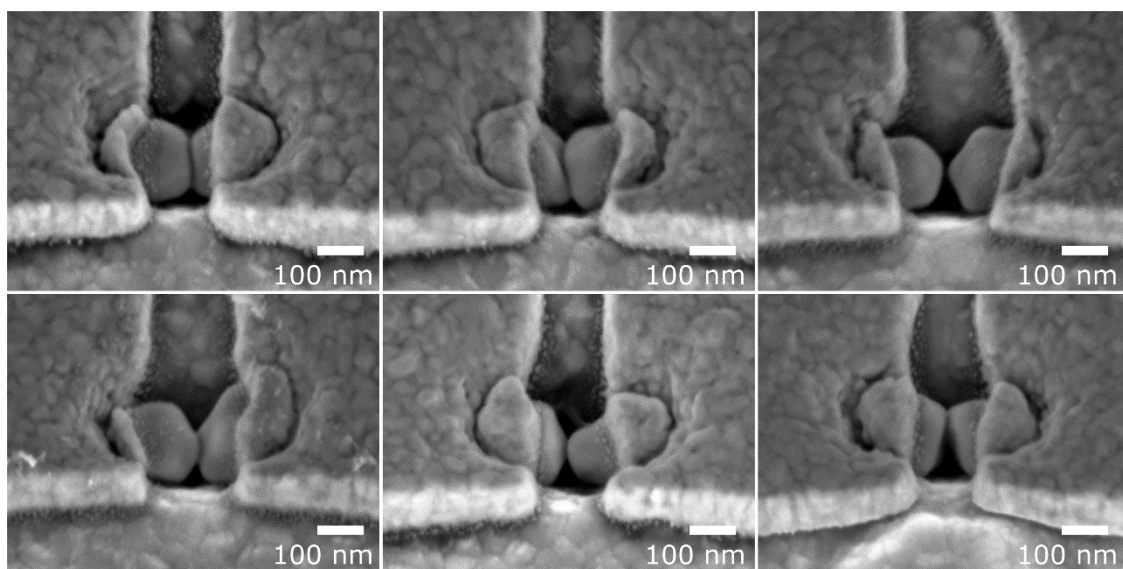
**Figure 4.5.** Top-view SEM image of an anisotropic funnel trap for the assembly of 200 nm AuNP dimer. The trap is fabricated by the processes listed in Table 3.1 with adjustments in parameters. The trap dimensions are designed to accommodate exactly two 200 nm AuNPs.

#### 200 nm AuNP dimer assembly

After the SEM imaging and the silanization process, the assembly templates are subjected to the CAPA processes using the parameters described in section 3.2.2 to assemble 200 nm AuNPs. The yield of the CAPA process with a AuNP dimer forming a nanogap is higher than 70%, which is estimated from two CAPA runs on two templates, in total about 600 traps. Figure 4.6a shows the SEM images of the traps with a AuNP dimer after the CAPA process. Most inter-particle gaps are smaller than 5 nm. The assembly of fused AuNPs is observed, which can be also found in the as-purchased AuNP solution. In order to extract the information for the design of the following electrode formation process, the gap position offset is estimated from the SEM images of 127 traps sampled from two templates, and the statistical analysis results are shown in Figure 4.6b. The gap position offset is defined as the position offset of the nanogap with respect to the trap center in X-axis. The gap position offset of the dimer of 200 nm AuNPs is in the range of -40 to 40 nm which provides a sufficient tolerance for the overlay shift and resolution of the following EBL lift-off process.



**Figure 4.6.** CAPA results of 200 nm AuNP dimer. (a) Top-view SEM images of assembled dimers of 200 nm AuNPs sampled from two CAPA templates. Most inter-particle gaps are smaller than 5 nm, and the assembly of fused AuNPs is observed. (b) The histogram of the position offset of the gap with respect to the trap center in X-axis. The data is extracted from the SEM images of 127 traps sampled from two templates, and the gap position offset is in the range of -40 to 40 nm which provides a sufficient tolerance for the overlay shift and resolution of the following EBL lift-off process.



**Figure 4.7.** NGEs fabricated by CAPA and EBL lift-off process. 30° tilted-view SEM images of NGEs after the fabrication of the Au electrodes by EBL lift-off process. The NGEs are on the same Si substrate, showing that multiple NGEs devices are obtained in parallel thanks to the limited gap position offset in the funnel traps.

#### Au electrodes fabrication

To fabricate two electrodes connecting each end of the assembled AuNP dimer, a 100 nm thick Au layer is deposited and patterned using the EBL lift-off process. The width of the Au electrode is 1  $\mu\text{m}$  in design to avoid the misalignment in the Y-axis, i.e. the minor axis of the trap. The separation between two electrodes is 200 nm in design and the distances of the trap center to each electrode are set to be equal in X-axis, i.e. the major axis of the trap. Thanks to the limited gap position offset in the funnel traps, multiple AuNP dimers are successfully connected by the electrodes in parallel on the same template.

Figure 4.7 shows the SEM images of the NGEs after the EBL lift-off process. The electrodes are precisely in contact with the AuNP dimer at each end without covering the nanogap in between the AuNPs.

#### NGEs on PDMS

After the formation of the NGEs, the PDMS preparation and the wet etching transfer processes described in Table 3.2 are conducted to transfer the NGEs to the PDMS substrate. The result of the transfer process is shown in Figure 4.8. To inspect the NGEs on PDMS without damaging them, the AFM is used to scan all six NGEs devices instead of using SEM. The 3D AFM images in Figure 4.8a-f confirm that the assembled AuNP dimers are also successfully transferred on the PDMS substrate along with the Au electrodes.

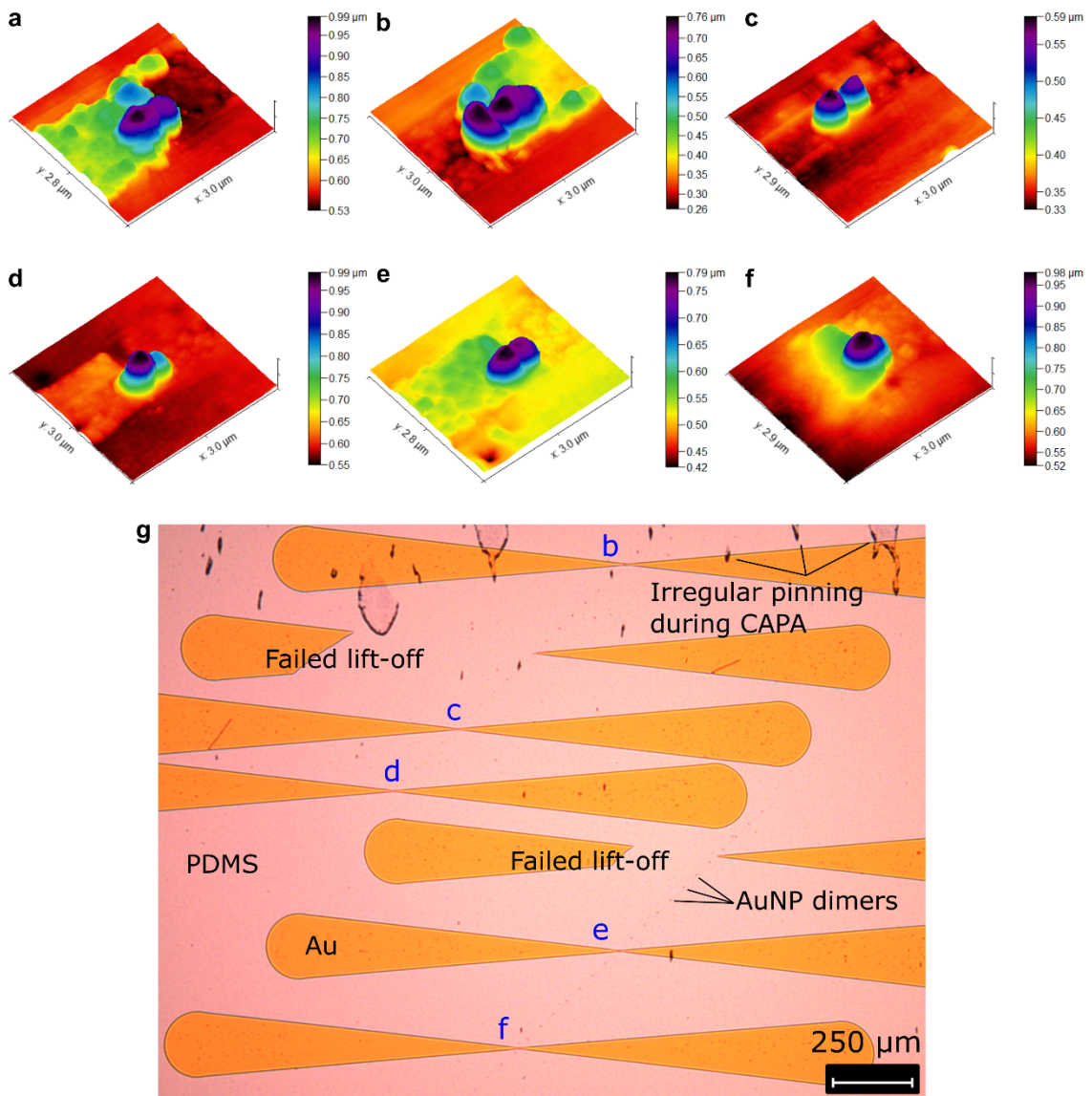


The detailed fabrication processes of the NGEs on PDMS using the CAPA technique are listed in Table 4.1.

### **Electrostatic discharge induced NGEs burn-out**

In order to electrically measure the transferred NGEs, copper wires and EGaIn are used to connect the Au pads on PDMS as described in section 2.2 (see Figure 2.4i). However, the NGEs are burned-out during the copper wire connection procedure due to the electrostatic discharge (ESD), which does not happen to the NGEs fabricated by adhesion lithography in chapter 3. The differences in the initial gap distance and the gap width are presumably the reasons behind this consequence. As seen in Figure 4.7, the gap distance is mostly smaller than 2 nm and the gap width are mostly smaller than 100 nm, whereas both the gap distance and width of the NGEs fabricated by adhesion lithography are larger as discussed in section 2.4.4. Nevertheless, the burn-out of the NGEs also implied that the electrodes are in electrical contact with the AuNP dimer on PDMS, and the gap distance between AuNPs remains at several nanometers even after the transfer process.

For the electrical characterization of the NGEs, more samples need to be fabricated and a better grounding of the metal wires needs to be considered during the wire connection procedure.



**Figure 4.8.** NGEs on PDMS fabricated by CAPA. (a)-(f) 3D AFM images of the corresponding NGEs in Figure 4.7 after being transferred onto the PDMS substrate by the wet etching transfer process. (g) OM image of the PDMS substrate with the NGEs (a)-(f) after the transfer process, showing that multiple NGEs fabricated by CAPA and EBL lift-off processes are successfully transferred in parallel.

**Table 4.1.** Fabrication process of the NGEs on PDMS using the CAPA technique

Step	Process	Equipment	Parameters
1	Alignment mark formation		Table 2.1 Step 1 to Step 5
2	160 nm thick SiO <sub>2</sub> PECVD	Oxford plasmalab system 100	300 °C, RF 20 W, 400 sccm 2% SiH <sub>4</sub> /N <sub>2</sub> , 710 sccm N <sub>2</sub> O, 2.5 min
3	EBL		Table 3.1 Step 2 to Step 6
4	SiO <sub>2</sub> wet etching	Wet bench	7:1 BHF for 30 s, DI water for 5 min, and N <sub>2</sub> drying
5	Funnel formation		Table 3.1 Step 8 to Step 9
6	330 nm thick SiO <sub>2</sub> PECVD	Oxford plasmalab system 100	300 °C, RF 20 W, 400 sccm 2% SiH <sub>4</sub> /N <sub>2</sub> , 710 sccm N <sub>2</sub> O, 308 s
7	Al deposition Silanization		Table 3.1 Step 11 to Step 13
8	CAPA	Custom-made setup	200 nm AuNP (Nanopartz, USA) Procedures are as described in section 3.2.2
9	Surface silane removal	TePla GiGAbatch	600 W, 400 sccm O <sub>2</sub> , 3 min
10	EBL with alignment		Table 2.1 Step 8 to Step 10
11	100 nm Au e-beam evaporation	Leybold Optics LAB 600H	CMi tool recipe: 181 Room temperature, 1010 mm working distance, 2 x 10 <sup>-6</sup> mbar chamber pressure, 4 Å/s deposition rate
12	Au lift-off	Wet bench	4 h in acetone and 10 s sonication
13	PDMS		Table 3.2 Step 2 to Step 4
14	Polystyrene slab mounting		PDMS manual cutting Manually bring polystyrene slab in contact with PDMS top surface with orientation alignment
15	Wet etching transfer	Wet bench	12 to 72 h in diluted hydrochloric acid bath (37% HCl : DI water = 1:6, volume ratio)

## 4.4 Conclusion and outlook

In this chapter, scalable fabrication of NGEs on PDMS by CAPA is demonstrated. The dimers of 200 nm AuNPs are assembled in funnel traps using the CAPA technique to create nanogaps between the assembled AuNPs. Combining a subsequent EBL lift-off process, multiple NGEs are first fabricated on Si substrates and then transferred to PDMS after the wet etching transfer process. The yield of the CAPA process with a AuNP dimer forming a nanogap is higher than 70%, and the NGEs are reliably transferred to PDMS. The electrical measurement result from an earlier attempt using AuNRs to fabricate NGEs also suggests that the NGEs on PDMS fabricated by CAPA can be mechanically tunable.

By further reducing the dimension of the electrodes fabricated by EBL lift-off process, a SLR array of electrically-driven optical antennas on soft substrates could be realized to make a further progression in the fabrication of nano-light sources.





## Chapter 5 Conclusion and outlook

In this thesis, scalable fabrications of metallic nanostructures on stretchable substrates by top-down and bottom-up methods are studied. Metallic nanostructures are first fabricated on Si substrates and subsequently transferred to stretchable substrates. In the first part of this thesis, the fabrication of nanogap electrodes (NGEs) on PDMS using adhesion lithography is reported. In the second part of this thesis, fabrication of ordered gold nanoparticles (AuNPs) on PDMS using capillary-assisted particle assembly (CAPA) technique is reported.

### 5.1 Tunable nanogap electrodes on PDMS fabricated by adhesion lithography

A scalable process to fabricate mechanically tunable NGEs on PDMS substrates is demonstrated. The demonstrated process includes adhesion lithography and the use of TiW and Al as the diffusion barrier layer and the sacrificial layer for the wet etching transfer process, respectively. A COMSOL simulation regarding the gap distance tunability is studied. The simulation results show that the gap distance tunability, i.e. the attenuation factor, is configurable by changing the electrode dimensions, and the gap distance can be tuned at the sub-nanometer scale by controlling the PS cantilever bending at the sub-millimeter scale. A study regarding the diffusion barrier layer is also conducted. A 200 nm thick  $\text{Al}_2\text{O}_3$  layer prevents Au-Al inter-diffusion during the 500 °C, 5 min RTA process, however, the nanogap is significantly enlarged on PDMS after the transfer process due to the residual stress of the thin film stack. The correlation between the Au1 design and the yield of the tape peeling process is systematically studied as well. A combination of a thinner Au2 and a design of Au1 with larger Au1 ring width and a smaller perimeter of the Au2 inside the Au1 ring in general results in a higher yield of the tape peeling process. Finally, the electrical measurement results from the NGEs device on PDMS show that the nanogap distance is mechanically tunable in the tunneling regime. The defects of Au electrodes buckling after mechanically stressing the NGEs indicates that the PDMS-NGEs adhesion is an essential factor to be further improved for a reliable tunability of the gap distance.

To improve the PDMS-NGEs adhesion for a reliable gap distance tunability, 3 possible methods are conceived and discussed. With a reliable nanogap tunability, the NGEs on PDMS fabricated by the process demonstrated in this work might be eventually integrated with micro piezo-electric actuators to become an on-chip, miniaturized mechanically tunable NGEs. The potential to fabricate such a miniaturized device with a scalable method might facilitate the application of a single-molecule detector, or ultimately, next-generation DNA sequencing.

## **5.2 SLR arrays on PDMS fabricated by precise CAPA on reusable templates**

In this work, we demonstrate a process to fabricate reusable templates for precise nanoparticle placement with the CAPA technique and show a systematic yield study of the assembly and transfer step. The assembly yield with arrays of approximately 10000 funnel traps is as high as 94% with a median particle position offset in the order of 10 nm. Cone traps achieve a similar maximum assembly yield of 97% but have a larger median position offset of 30 nm. The assembled AuNPs are then transferred from the assembly template onto PDMS and OrmoComp substrates with transfer yields larger than 99%. The SLR responses of the transferred AuNP arrays are characterized and the measurement results are in agreement with the FEM simulation results. To enable the reusability of the template, a pre-treatment of uncured PDMS is a prerequisite to ensure a residue-free assembly template after the wet etching transfer process. The result of the yield and position offset of AuNPs assembled using the recycled template is comparable to that of the first use, demonstrating that the proposed process allows for the fabrication of reusable templates.

The process presented here also paves the way for the precise positioning of thousands of bottom-up assembled nanoparticles with precise alignment to top-down fabricated micro- or nano-structures, and therefore enables integrated nanosystems made of lithography-defined patterns and template assembly. The presented process allows in particular the scalable fabrication of advanced nano-devices such as electrically-driven optical antennas and tunable tunneling nanogap electrodes and might ultimately facilitate applications in nano-light sources and single-molecule detection, which remain a challenge for the present cutting-edge transfer printing and dry peeling transfer techniques.

## **5.3 NGEs on PDMS fabricated by CAPA**

Apart from using top-down methods to fabricate NGEs, scalable fabrication of NGEs on PDMS by CAPA is demonstrated in this work. The dimers of 200 nm AuNPs are assembled in funnel traps using the CAPA technique to create nanogaps between the

assembled AuNPs. Combining a subsequent EBL lift-off process, multiple NGEs are first fabricated on Si substrates and then transferred to PDMS after the wet etching transfer process. The yield of the CAPA process with a AuNP dimer forming a nanogap is higher than 70%, and the NGEs are reliably transferred to PDMS. The electrical measurement result from an earlier attempt using AuNRs to fabricate NGEs also suggests that the NGEs on PDMS fabricated by CAPA can be mechanically tunable.

By further reducing the dimension of the electrodes fabricated by EBL lift-off process, a SLR array of electrically-driven optical antennas on soft substrates could be realized to make a further progression in the fabrication of nano-light sources.

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# Curriculum Vitae

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### Work Experience

#### Taiwan Semiconductor Manufacturing Company (TSMC)

- 2013 – 2016 **Principal Engineer**, MEMS R&D Program  
Project manager of MEMS WLCSP 3DIC projects, collaborating with Swiss and U.S. companies to realize the smallest commercial pressure sensor, accelerometer in the world.
- 2012 – 2013 **Principal Engineer**, Fab2 PIE Department  
MEMS R&D projects: microphone, accelerometer, and piezoresistive pressure sensor.  
Production project: iPhone 4S MEMS microphone.
- 2010 – 2012 **Senior Engineer**, Fab2 PIE Department  
MEMS R&D projects: gyroscope, autofocus actuator  
Production projects: CMOS ambient light & proximity sensor  
2011 TSMC Operation Division Young Talent Program member  
2010 TSMC Fab2 Indirect Labor Award winner
- 2008 – 2010 **Engineer**, Fab2 PIE Department  
R&D project: MEMS/CMOS monolithic piezoresistive pressure sensor  
2009 TSMC Integration Technical Board Conference Award 1st Prize  
2009 TSMC Fab2 Indirect Labor Award winner

### Education

- 2004 – 2007 **MSc in Physics**, National Taiwan University, Taiwan  
Thesis: "The study on fabrication procedures and electro-optical properties of flexible alignment layer-less liquid crystal cell prepared by nano-imprinting lithography" (Advisor: Prof. Chao, Chih-Yu)
- 1998 – 2004 **BSc in Physics**, National Taiwan University, Taiwan  
**BSc in Civil Engineering**, National Taiwan University, Taiwan

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## Computer Skills

Language C, C++, Basic, PHP, ASP, SQL  
Software MS Office, Inkscape, Blender, Gwyddion, LabView, COMSOL, KLayout, L-Edit, MatLab, Origin

## Languages

Mandarin Native proficiency  
English Professional working proficiency

## Publications

- 2022 H. S. C. Yu, A. Conde-Rubio, H.-C. Wang, O. J. F. Martin, G. Boero, J. Brugger, H. S. C. Yu, A. Conde-Rubio, G. Boero, J. Brugger, H.-C. Wang, O. J. F. Martin, "Precise Capillary-Assisted Nanoparticle Assembly in Reusable Templates", *Particle & Particle Systems Characterization* **2022**, 2100288.
- 2019 Z. Su, H. S. C. Yu, X. Zhang, J. Brugger, H. Zhang, Z. Su, H. Zhang, H. S. C. Yu, J. Brugger, X. Zhang, "Liquid Assembly of Floating Nanomaterial Sheets for Transparent Electronics", *Advanced Materials Technologies* **2019**, 4, 1900398.
- 2009 T. C. Lin, S. C. Yu, P. S. Chen, K. Y. Chi, H. C. Pan, C. Y. Chao, "Fabrication of alignment layer free flexible liquid crystal cells using thermal nanoimprint lithography", *Current Applied Physics* **2009**, 9, 610.

## Patents

- 2018 Structure and method to mitigate soldering offset for wafer-level chip scale package (WLCSP) applications  
SC Yu, CM Hung, H Huang, HF Chen, AT Chang, WC Tai  
US Patent 10,131,540
- 2017 Monolithic MEMS platform for integrated pressure, temperature, and gas sensor  
SC Yu, CM Hung, H Huang, HF Chen, AT Chang, WC Tai  
US Patent 9,845,236
- 2017 Thin film structure for hermetic sealing  
SC Yu, HF Chen, H Huang, CM Hung, WC Tai  
US Patent 9,714,166
- 2015 Structure and method of providing a re-distribution layer (RDL) and a through-silicon via (TSV)  
SC Yu, CM Hung, HF Chen, WC Tai, H Huang  
US Patent 9,202,792
- 2013 Deep well process for MEMS pressure sensor  
SC Yu, HS Shue  
US Patent 8,558,330